12 Squire Circle • Penfield, NY 14526 • 585-210-9125 • kfronczak@gmail.com

Analog circuit designer with experience implementing creative low-noise and low-cost designs for Analog Front Ends

PROFESSIONAL

Synaptics Inc. Rochester, NY

Sr. Mixed Signal IC Design Engineer

February 2014 - Present

- Experience in designing various analog circuits in deep-submicron process
- Designed low-noise, high-bandwidth current-mode capacitive Analog Front End for low-cost fingerprint sensors
- Implemented a novel current-mode mixer topology to improve SNR
- Architected and designed a experimental low-area, ultra-low power reference architecture to reduce standby current by an order of magnitude without reducing performance
- Designed small area and high-performance baseline correction circuit for Touch and TDDI chips
- Circuit design and system-level experience in touch sensing front-ends, display drivers, and fingerprint sensing front-ends
- Designed a sub 1-V bandgap reference with an innovative base-cancellation circuit that generates multiple configurable references for next-generation TDDI products. Currently in mass production on multiple ASICs
- Responsible for the design of critical low-noise, high-performance touch sensing circuits for analog front-end including demodulator, filter, and various amplifiers for TDDI products currently in mass production
- Experience working with multi-functional teams in order to ensure smooth IC bring-up through to production
- Responsible for driving completion of high-speed MIPI D-PHY SERDES architecture from transistor-level design through physical implementation, up to top-level verification and production testing.
- Experience with cadence design flow, as well as circuit modeling in VerilogA and MATLAB
- Helped implement a top-level mixed-signal (AMS) design flow for next-generation fingerprint sensors in order to verify top-level functionality
- Able to break down complex problems in a way that encourages creative design solutions and proper schedule maintenance

Synaptics Inc. Rochester,

NY

Analog Design and Silicon Validation Contractor

June 2013 - February 2014

 Performed extensive validation on LDOs, VCOM drivers, LCD level shifters, and high-speed MIPI D-PHY architecture

EDUCATION

Rochester Institute of Technology

Rochester,

NY

Master of Science and Bachelor of Science, August 2013

Graduate GPA -

4.0

Thesis

Stability Analysis of Switched DC-DC Boost Converters for Integrated Circuits

Investigated small-signal modeling and stability requirements for boost converters, as well as a variety of
OTA-based controller topologies, in order to aid in the design and measurement of boost converter stability on
an ASIC. Also investigated use of genetic algorithms as a way to optimize controller design.

SKILLS

- Attended a **Continuous-Time Delta Sigma Converter** course held by MEAD at UC Santa Cruz in March 2015. Course taught by Dr. Shanthi Pavan, Dr. Richard Schreier, and Dr. Pavan Hanumolu.
- Member of IEEE since 2010, Member of Solid State Circuits Society since 2013