Computer Architecture: Assignment 5 Report

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	Number of Cycles	Number of Instructions	Number of Data Hazard NOPs	Number of Control Hazard NOPs	Throughput IPC
evenorodd	259	6	3	2	0.0231
prime	1219	29	7	26	0.0237
palindrome	2062	49	23	16	0.0237
fibonacci	3581	78	20	34	0.0217
descending	11779	277	53	218	0.0235

IPC is very small because for each instruction 40 cycles are taken just for InstructionFetch stage.