AGASTYA **SETH**

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Education

2023 **Master of Science in Computer Science** (Fall '23)
Arizona State University, *Tempe, AZ*

2016-2020 **Bachelor of Technology in Electronics and Communication Engineering** | Minor in Mathematics
Shiv Nadar University, *UP, IN* **GPA**: 8/10

2018 **Summer Session**, Data Science & Technology Entrepreneurship
Stanford University, *Stanford, CA* **GPA:** 4.1/4.3

Experience

July 2023 – May 2021 | **Senior Software Engineer , Cadence Design Systems, Noida, India**
Worked in the software engineering (R&D) team for the Quantus Parasitic Extraction Cell-level tool, utilized by digital design companies to estimate RC parasitics for sign-off designs.
- Handled customer-critical enhancements and issues for core libraries - preprocessing, IVMF Flow, 3DIC flow, and messaging infrastructure.
- Developed high-performing graph theoretical, geometry processing, and pattern matching algorithms.
- Spearheaded the novel 3DIC flow for inter-die crosstalk extraction and submitted a paper at CIC2022.
- Deployed a Flex/Bison-based parser library for subckt parsing within the 3DIC Flow.
- Owned multiple enhancement requests/issues for Rccompare (SPEF/DSPF comparison tool).

C++ | Python | Qt Creator | Perforce | Shell-scripting | Linux

April 2021 – Aug 2020 | **Software Enigeering Intern, Cadence Design Systems, Noida, India**
Worked in the software engineering (R&D) team for Quantus Parasitic Extraction Cell-level tool.
- Worked on customer enhancements & bug fixes for various libraries in the tool.
- Was handed over enhancement requests for Rccompare (SPEF/DSPF comparison tool)
- Handled requests for memory and clock-based profiling, and memory leak issues for various stages of the tool

C++ | Python | Qt Creator | Perforce | Shell-scripting | Linux

Sep 2021 – Aug 2020 | **Data Science Consultant, LiqVid English Edge <> SNU Research Group,**
Headed the research group led by Prof. Rajeev Kumar (SNU) with the e-learning company LiqVid English Edge
- Researched & experimented with SOTA transformer-based deep language models and NLP libraries/frameworks.
- Delivered a tool for AES (Automated Essay Scoring) - employing a hybrid architecture using 3 ensemble DistilBERT-based models along with handcrafted features which allows for better fine-tuning and explainability of results.

BERT | Seq-to-seq | Python | TensorFlow | Keras | PyTorch | GCP

July 2020 – Jan 2020 | **Data Science Intern , ViSenze, Singapore**
Worked as a data scientist at one of the leading AI-based visual search startups based in Singapore.
- Was responsible for sourcing datasets, model training & optimization, and deployment for projects undertaken.
- Improved their flagship fashion-attributes models by augmenting the datasets and adding attention models in the pre-processing stage and hyperparameter tuning.
- Worked on perspective classification models for various products. Built group classification models for various fashion accessories.
- Built various pipelining and workflow scripts including web scraping utilities for internal tools. Created a novel algorithm to auto-parse & source images based on T-SNE sufficiency.

JupyterLab | PyTorch | OpenCV | Selenium | BS4 | Docker | ONNX | Jenkins | JIRA

July 2019 – May 2019 | **Computer Vision Intern , Vi-Dimensions, Singapore**
Singapore startup working on real-time anomaly detection on surveillance cameras.
- Researched various background learning/subtraction models for their anomaly detection solution (ARVAS).
- Built a novel background segmentation model using distributed Hough Transform, achieving low inferencing time and robustness to lighting conditions.
- Also built a Faster-RCNN based model layer for detecting persons and bags in surveillance camera feeds.

Python | OpenCV | TensorFlow | Keras

May 2017 – July 2017 | **IoT Intern , Bisquare Systems, Noida**

Worked on R&D of an end-to-end product solution for smart home lights.

- Designed **an ESP8266 WiFi microcontroller-based IoT module** for an end-to-end IoT platform.
- Designed a mood-light and an IR remote-control module based on the designed module.
- Created AWS Lambda based backend for product registration, control and monitoring, and collected data for BDA.

Microcontroller programming | MERN Development | C++ | AWS Lambda | MongoDB

Key Undergrad Projects

Massive MIMO Channel Estimation using Deep Image Prior (Major Project - I) — 2019

Project Report | github.com/agastyaseth/mimo-channel-estimation

Explored various deep learning techniques for Massive MIMO channel estimation to minimize pilot contamination and channel noise (under the guidance of Prof. Vijay Kumar Chakka) and designed and simulated a DIP-based (Deep Image Prior) DNN architecture for de-noising the received signal

MATLAB | Python | PyTorch | TensorFlow | Keras

Schizophrenia Detection and Prediction (UG Research) — 2019

SNU Undergraduate Research Opportunity

Used EEG signals and resting state fMRI neuro-biomarkers for Schizophrenia detection and prediction. Performed a comparative study of various 3D-CNN models for discrimination and built an ensemble model achieving high AUC (0.98)

Medical Diagnostics | Python | TensorFlow | Keras

SkiNet - Skin Segmentation and Melanoma Classification (Deep Learning Course Project) — 2019

Project Report

Explored and evaluated various SOTA deep learning techniques for skin segmentation. (under the guidance of Prof. Niteesh Sahni). Worked on an explainable model to be able to explain the diagnosis by using various XAI algorithms like GradCam++

Medical Diagnostics | Image Classification | Image Segmentation | PyTorch

Analog VLSI implementation of Support Vector Machine (VLSI Course Project) — 2019

Project Report

Designed analog VLSI approach to implementing projection neural networks adapted for support vector machine with radial-basis function (RBF) kernel and validated and performed characteristic simulations for the same on Cadence Virtuoso.

VLSI CAD | Analog Design | Virtuoso | Support Vector Machine

RNBIP - Single Bus Processor Architecture — 2017-2018

github.com/digital-design-snu/RNBIP_SingleBusProcessor

Built an 8-Bit Single Bus Processor Architecture using HDL synthesis, and successfully flashed it on Xilinx Artix FPGA (under the guidance of Dr. R.N. Biswas. Also researched on embedding the same in a microcontroller with a compiler and ports.

VHDL | FPGA | Embedded | Compiler design

Stanford Silicon Valley Innovation Academy — 2018

Green Score | Stanford SVIA

Conceptualized a solution to make consumer product production lifecycle more transparent using DLT. Developed a platform for users to track their carbon footprint wrt. their daily consumption (electricity, gas, water, products etc.)

UN Sustainable Development Goals | Blockchain | Green Score | Carbon Footprint

Key Additional Coursework

MOOCs	Introduction to Machine Learning, Deep Learning Specialization, Full-Stack Web Development, Operating Systems, Computer Architecture
Cadence TPP Program	VLSI CAD, SystemVerilog for Design and Verification v20.6, Digital Systems, C++ For C Programmers, Data Structures

Achievements

Winner | Smart India Hackathon 2019 - Hardware Edition
Worked with Tata Motors on range anxiety for their EVs.

Regional Finalist | Google Science Fair 2014
Built an Android app to empower Indian farmers with real-time crop prices. Featured in Scientific American.

Trinity Guildhall London - Level 5 | Piano

70% Merit Based Scholarship Shiv Nadar University

Societies & Clubs

- **Roboyantriki - Robotics Society of SNU** Core Technical Commitee Member: Conducted various intra-university workshops on Arduino, IoT etc.
- **Snuphoria - Music Club of SNU** Working Committee | Social Media Manager: Hosted SMP (Student Mentorship Program) to teach Piano to University