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Version 1.0 (May 25, 2007)
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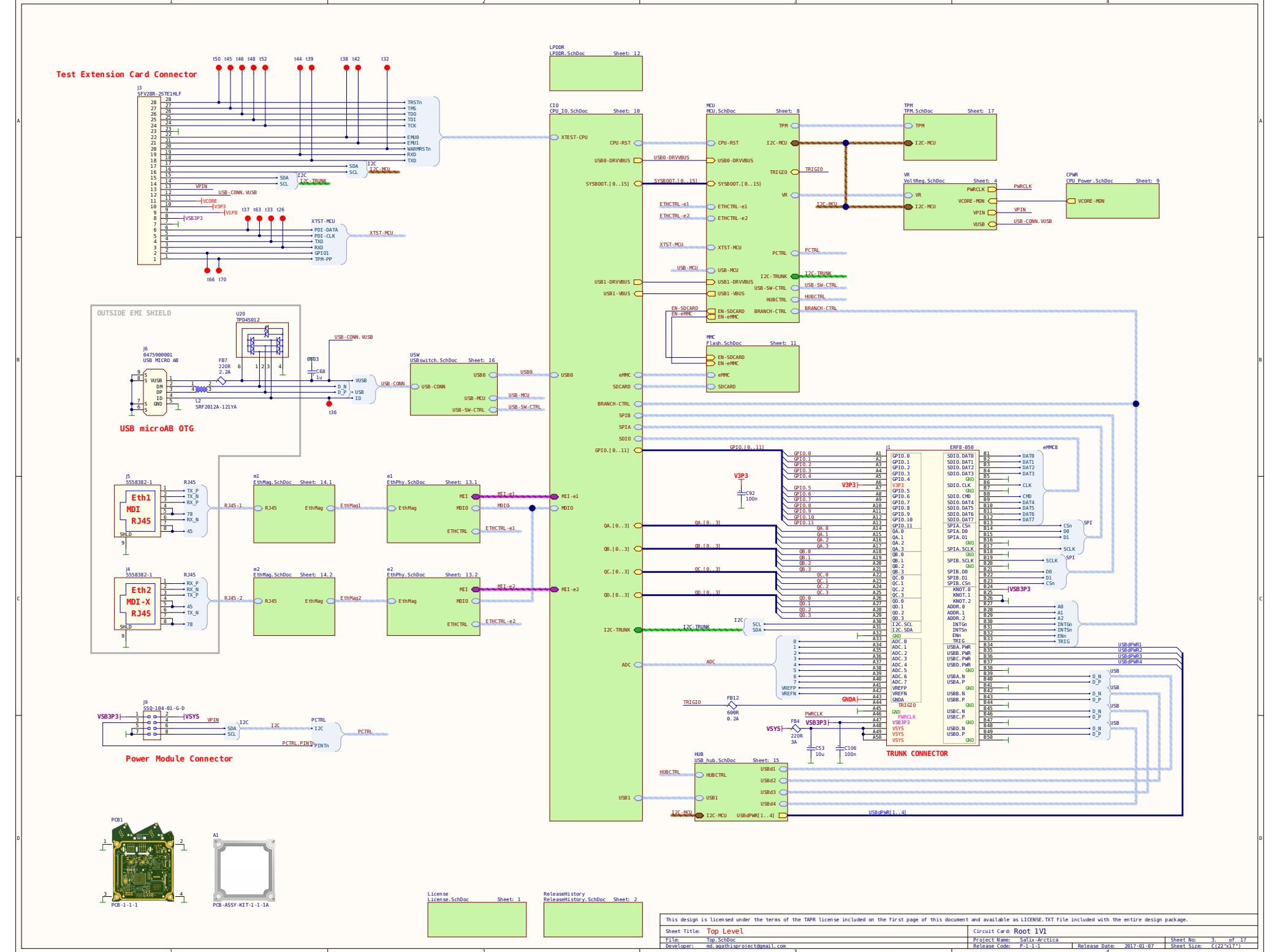
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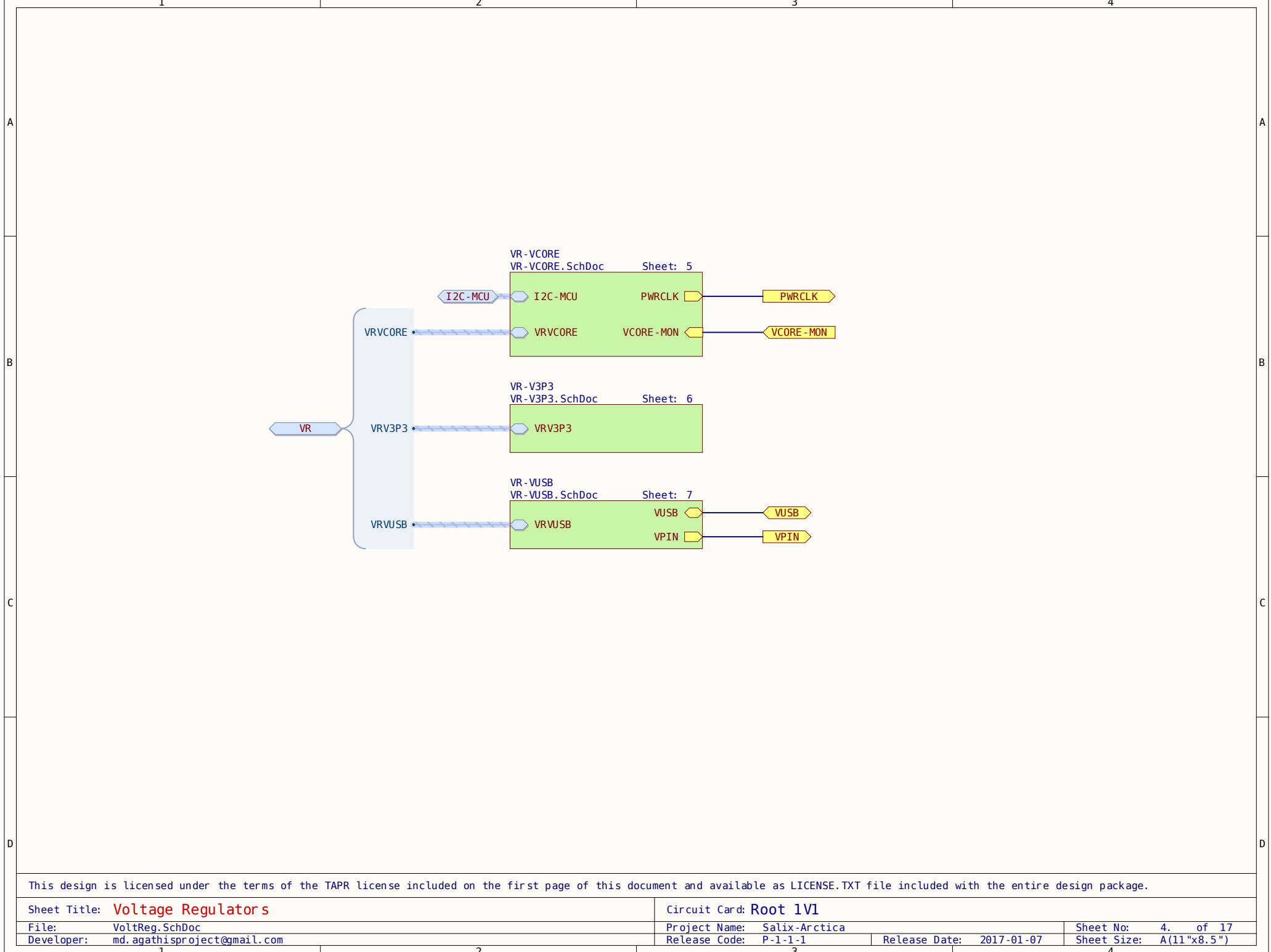
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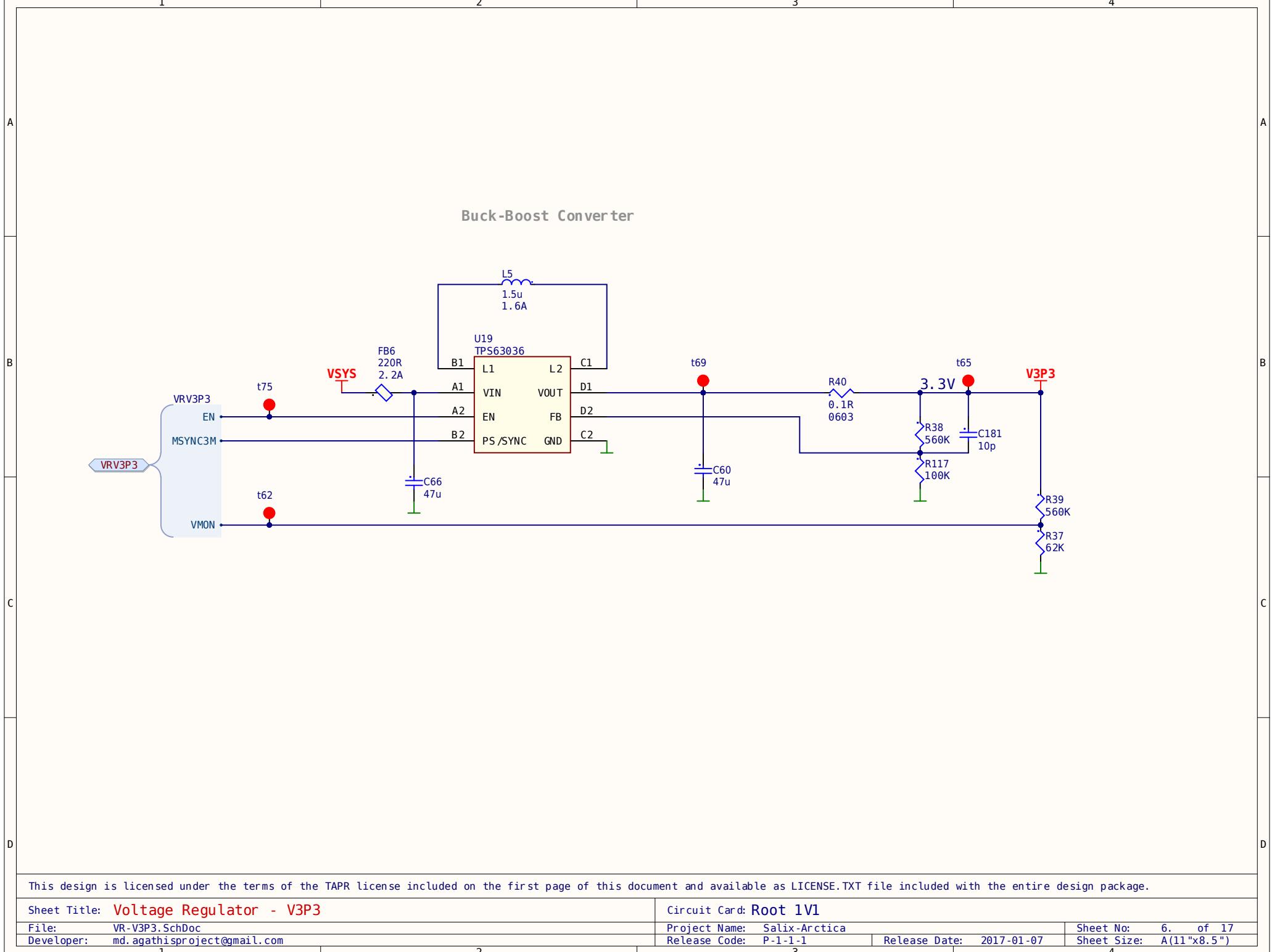
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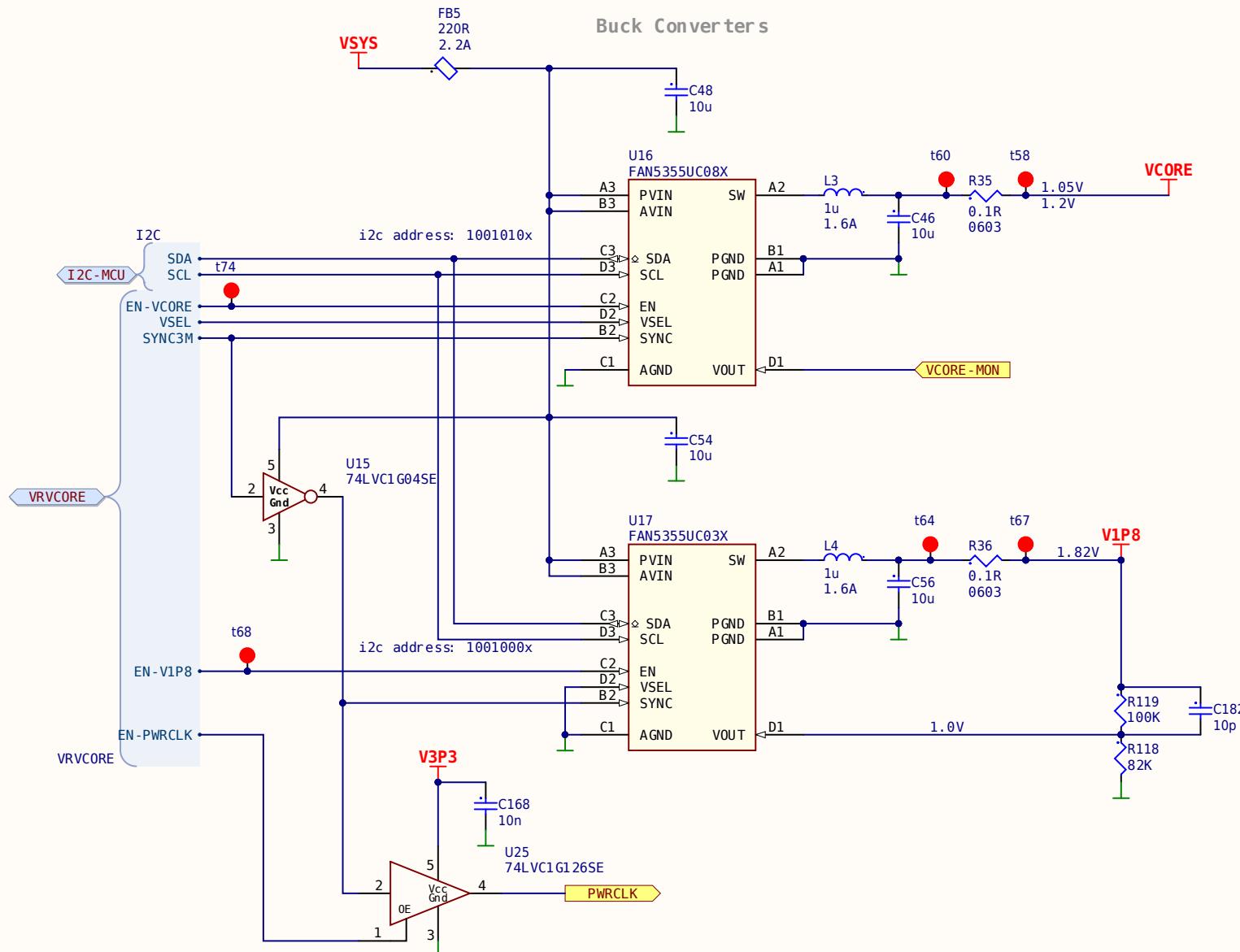
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Sheet Title: Licensing	Circuit Card: Root 1V1
File: License.SchDoc	Project Name: Salix-Arctica
Developer: md.agathisproject@gmail.com	Sheet No: 1. of 17
Release Code: P-1-1-1	Release Date: 2017-01-07
	Sheet Size: B(17"x11")

	1	2	3	4		
Release	Date	Description				
A	P-1-1-1	files released for prototype manufacturing				
	P-1-1-1	formating and appearance improvements for github publishing				
	P-1-1-1A	***	patches added during prototype validation: 1.			
B				B		
C				C		
D	*** pending release			D		
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Sheet Title: Revision History			Circuit Card: Root 1V1			
File: ReleaseHistory.SchDoc			Project Name: Salix-Arctica	Sheet No: 2. of 17		
Developer: md.agathisproject@gmail.com			Release Code: P-1-1-1	Release Date: 2017-01-07		
			Sheet Size: A(11"x8.5")			









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Sheet Title: **Voltage Regulator - VCORE and V1P8**

Circuit Card: **Root 1V1**

File: **VR-VCORE.SchDoc**

Project Name: **Salix-Arctica**

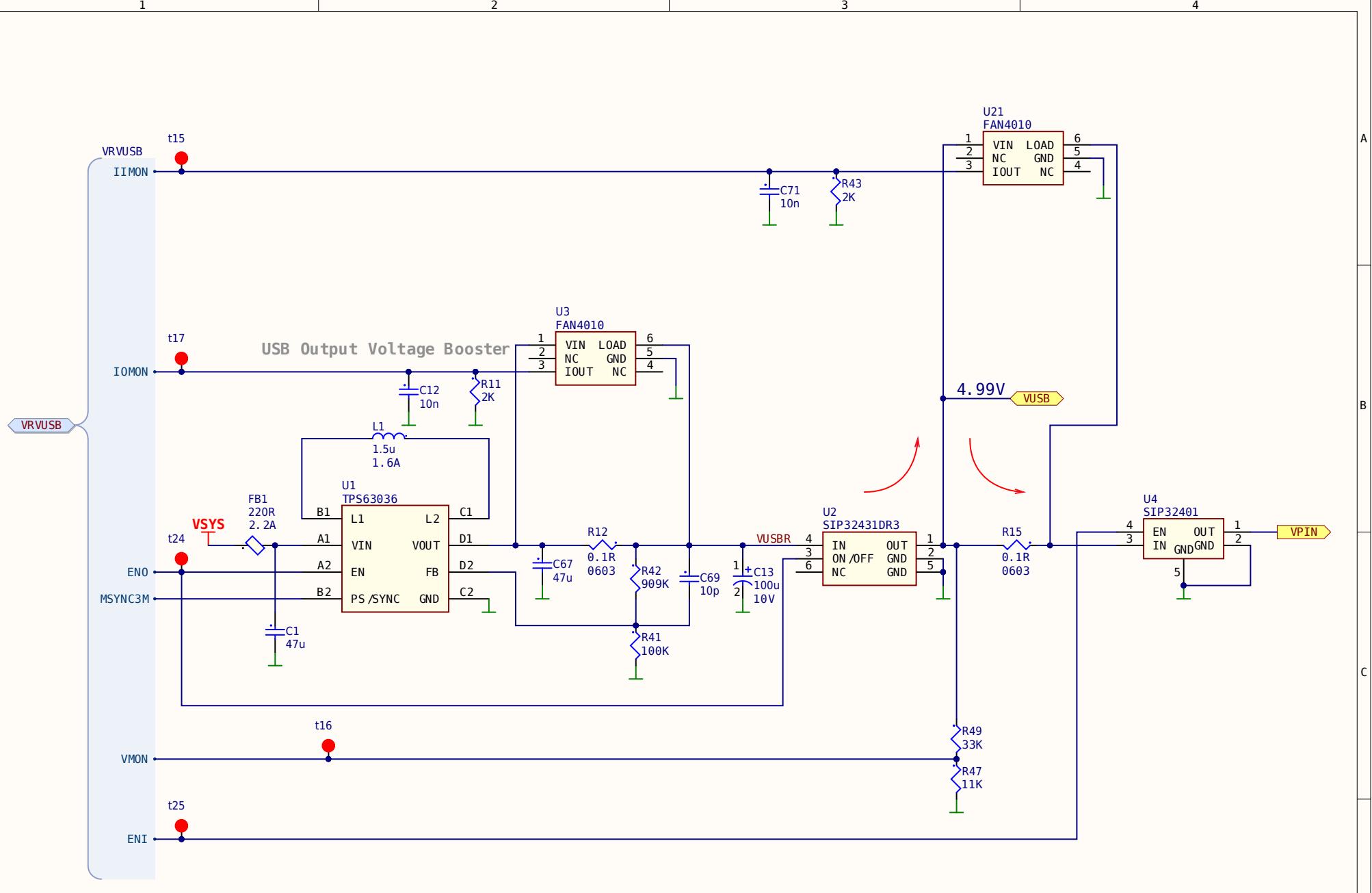
Sheet No: **5. of 17**

Developer: **md.agathisproject@gmail.com**

Release Code: **P-1-1-1**

Release Date: **2017-01-07**

Sheet Size: **A(11"x8.5")**



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Sheet Title: Voltage Regulator - VUSB

Circuit Card: Root 1VI

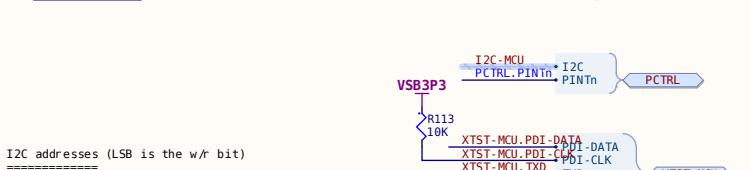
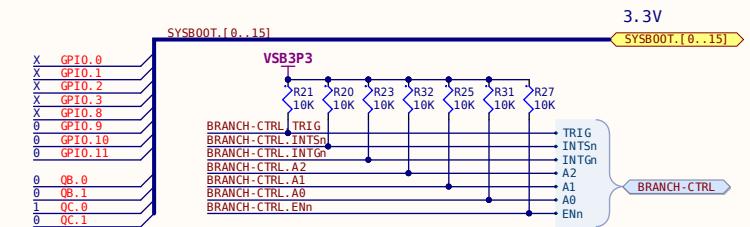
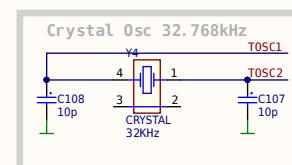
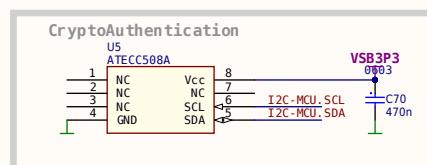
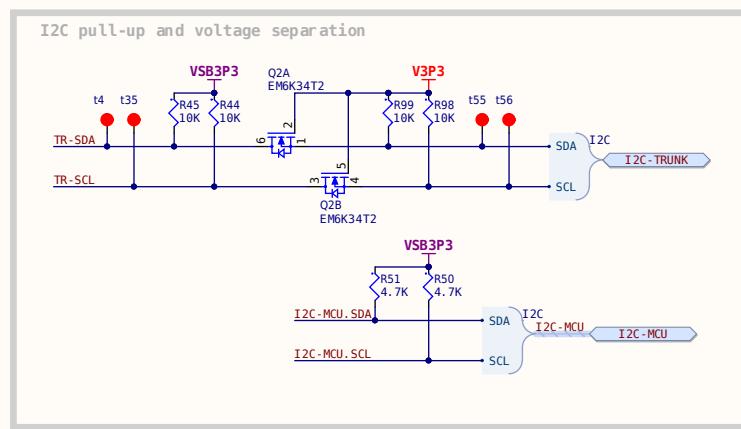
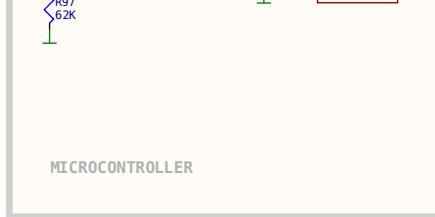
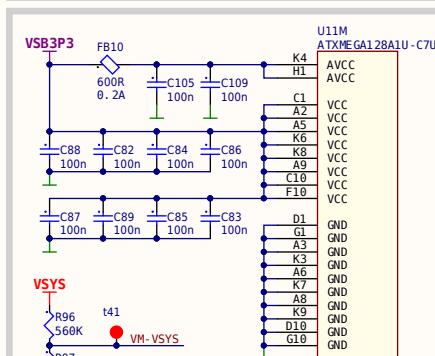
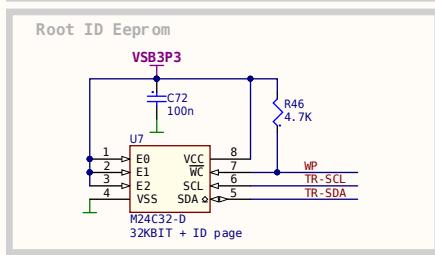
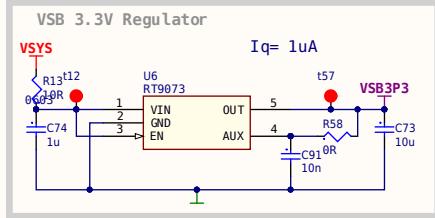
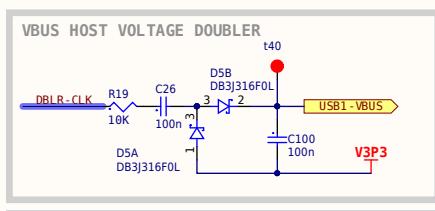
File: VR - VUSB.SchDoc

Project Name: Salix-Arctica

Developer: md.agathisproject@gmail.com

Sheet No: 7. of 17

Sheet Size: A(11"x8.5")



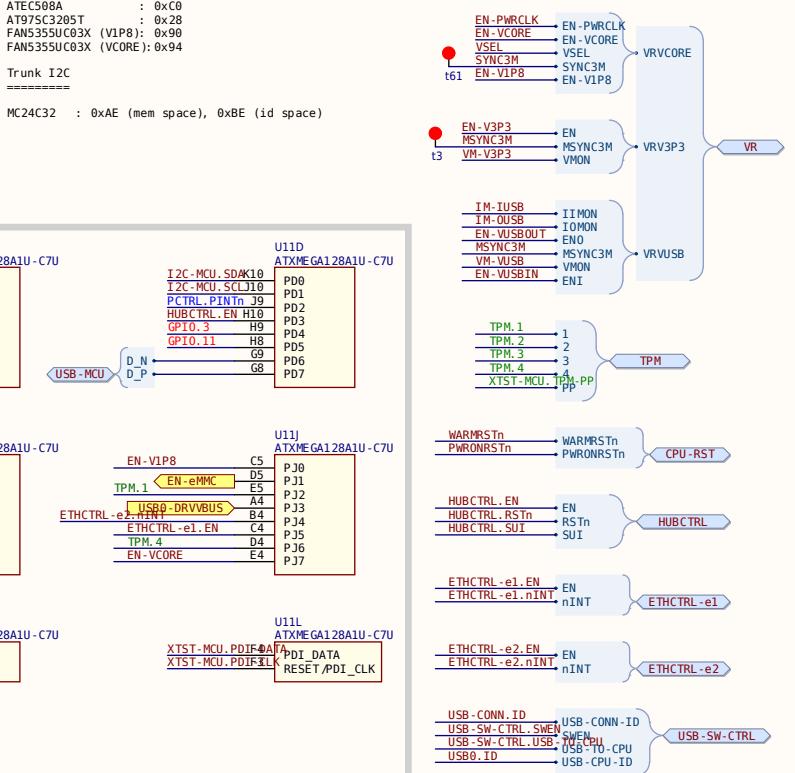
I₂C addresses (LSB is the w/r bit)

MCU root I2C

USB2514B : 0x58
ATEC508A : 0xC0
AT97SC3205T : 0x28
FAN5355UC03X (V1P8) : 0x90
FAN5355UC03X (VCORE) : 0x94

Trunk I2C

MC24C32 : 0xAE (mem space), 0xBE (id space)



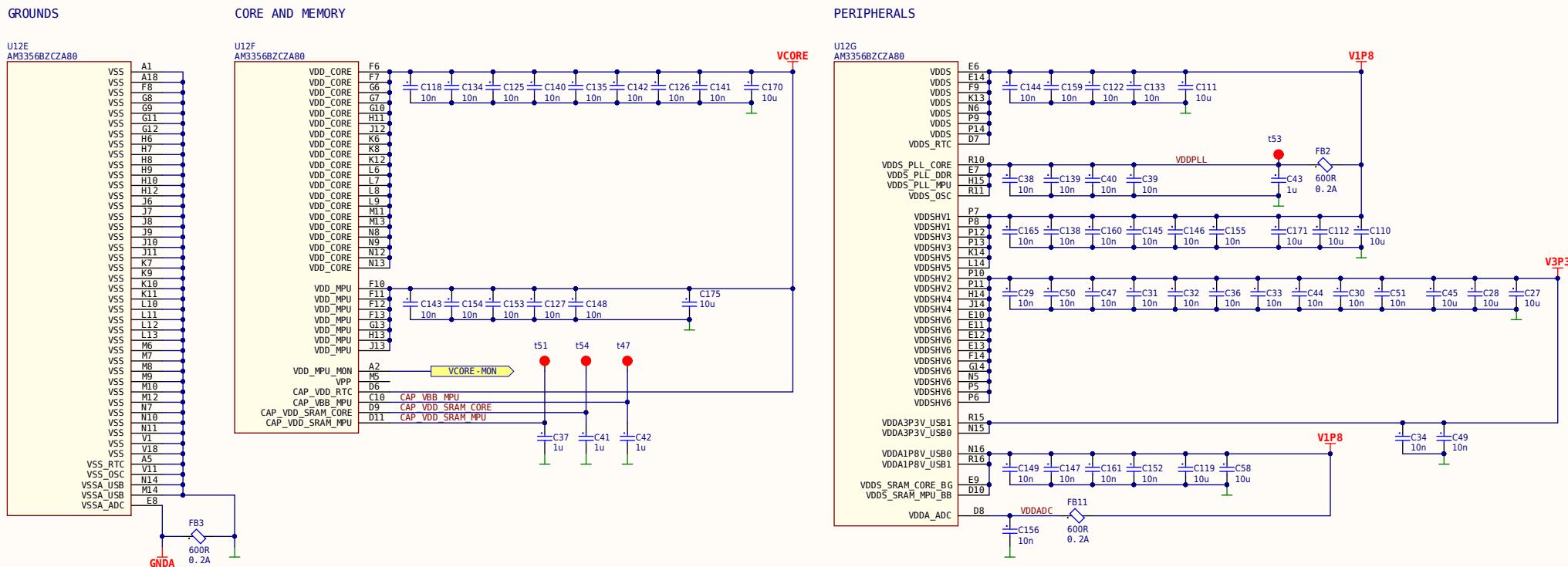
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Sheet Title: Microcontroller

File: MCU.SchDoc
Developer: md.agathisproject@gmail.com

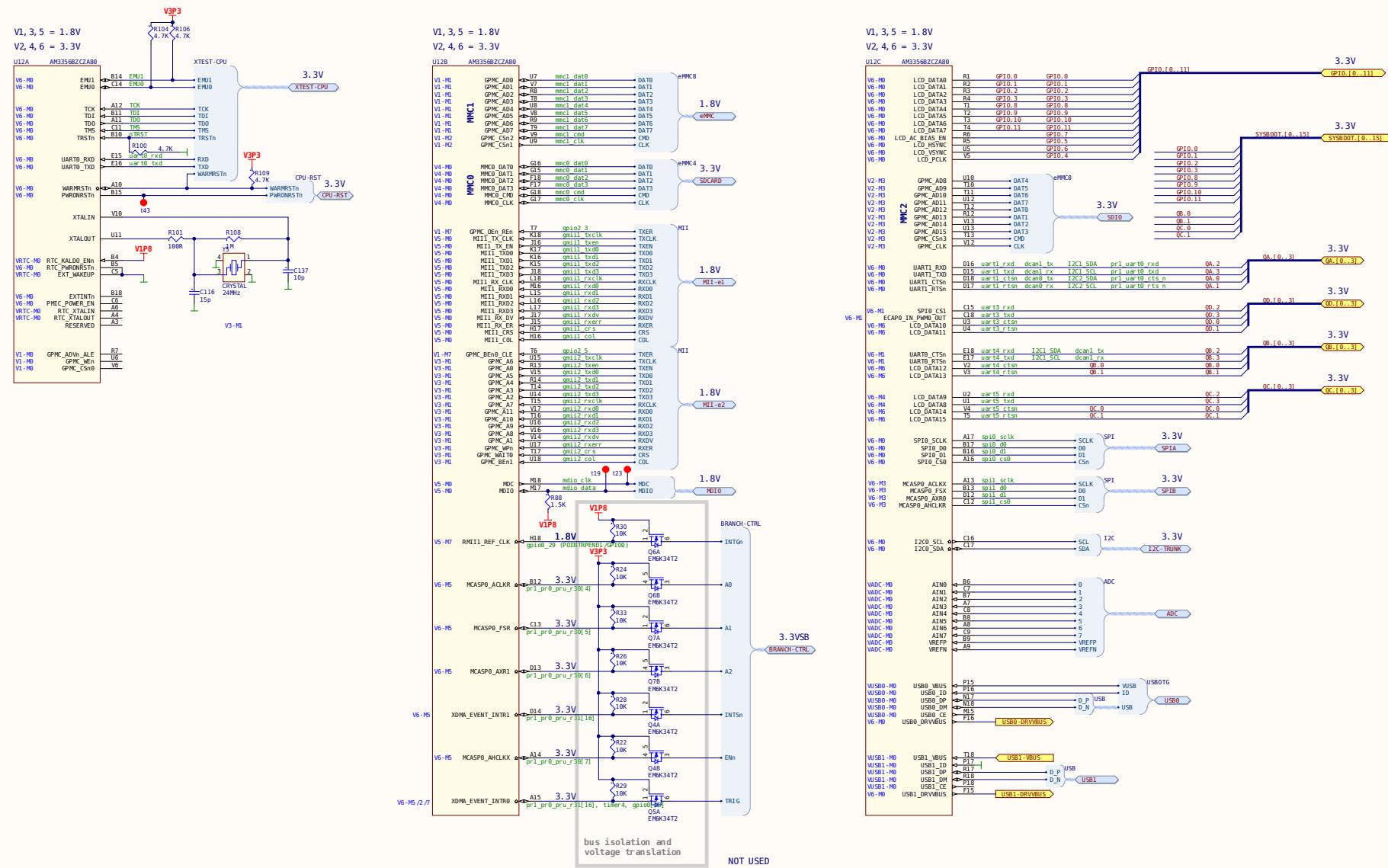
Circuit Card: Root 1V1

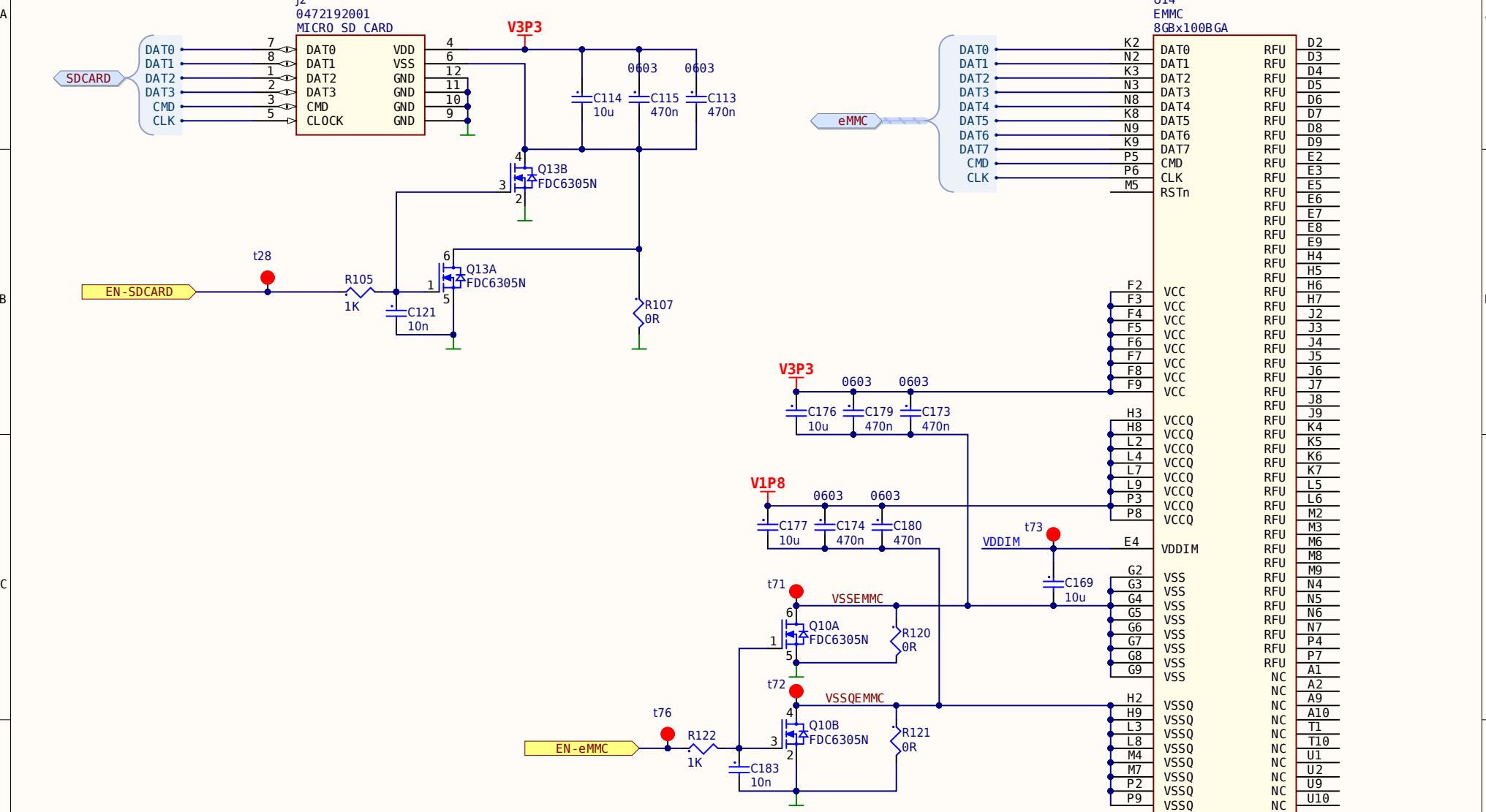
Project Name: Salix-Arctic
Release Code: P-1-1-1



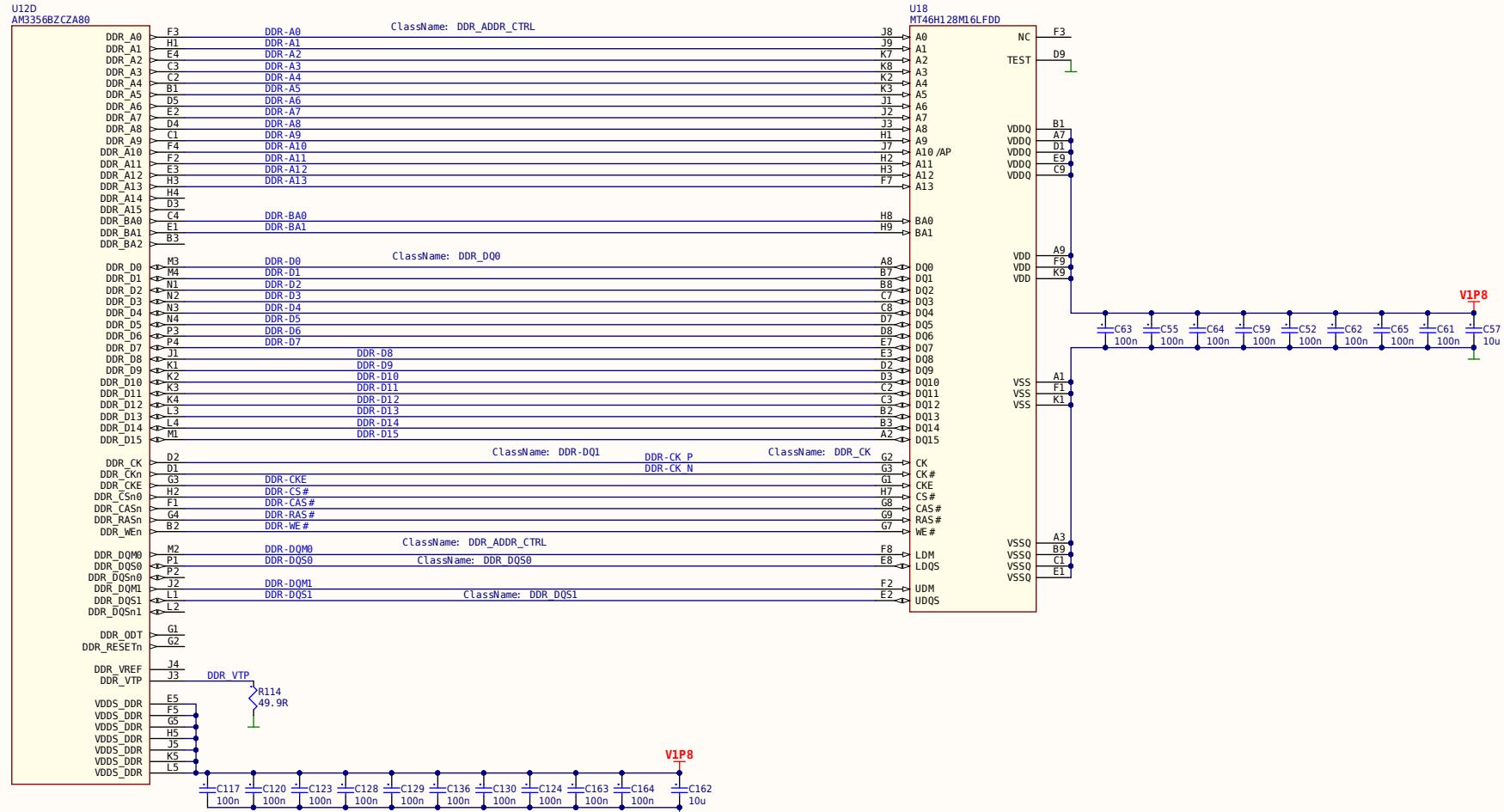
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Sheet Title: Microprocessor Power	Circuit Card: Root 1V1
File: CPU Power.SchDoc	Project Name: Salix-Arctica
Developer: md.agathisproject@gmail.com	Release Code: P-1-1-1
	Release Date: 2017-01-07
	Sheet No: 9, of: 17 Sheet Size: B(17"x11")



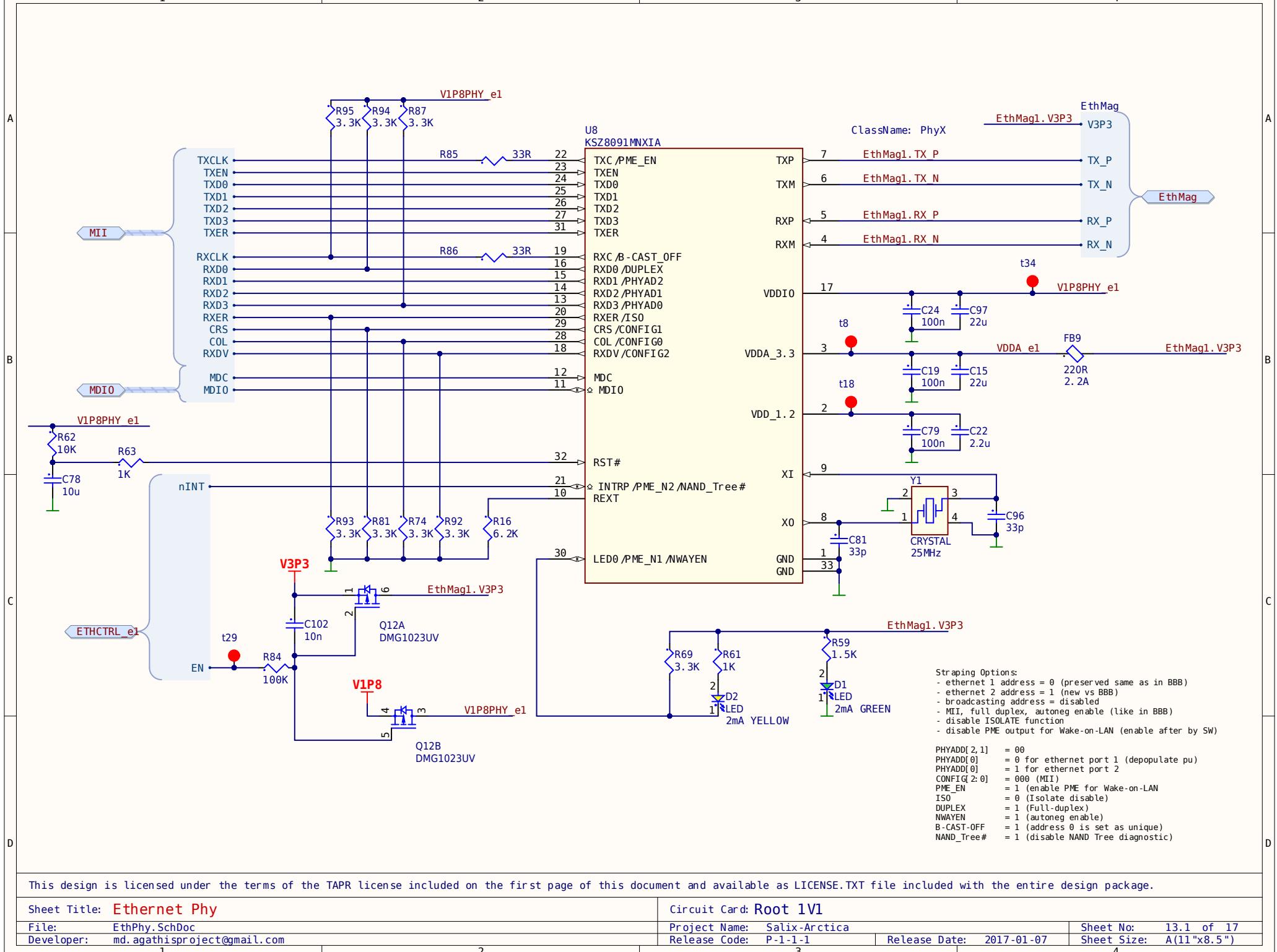
uSD Card (hinge connector)**eMMC (BGA)**

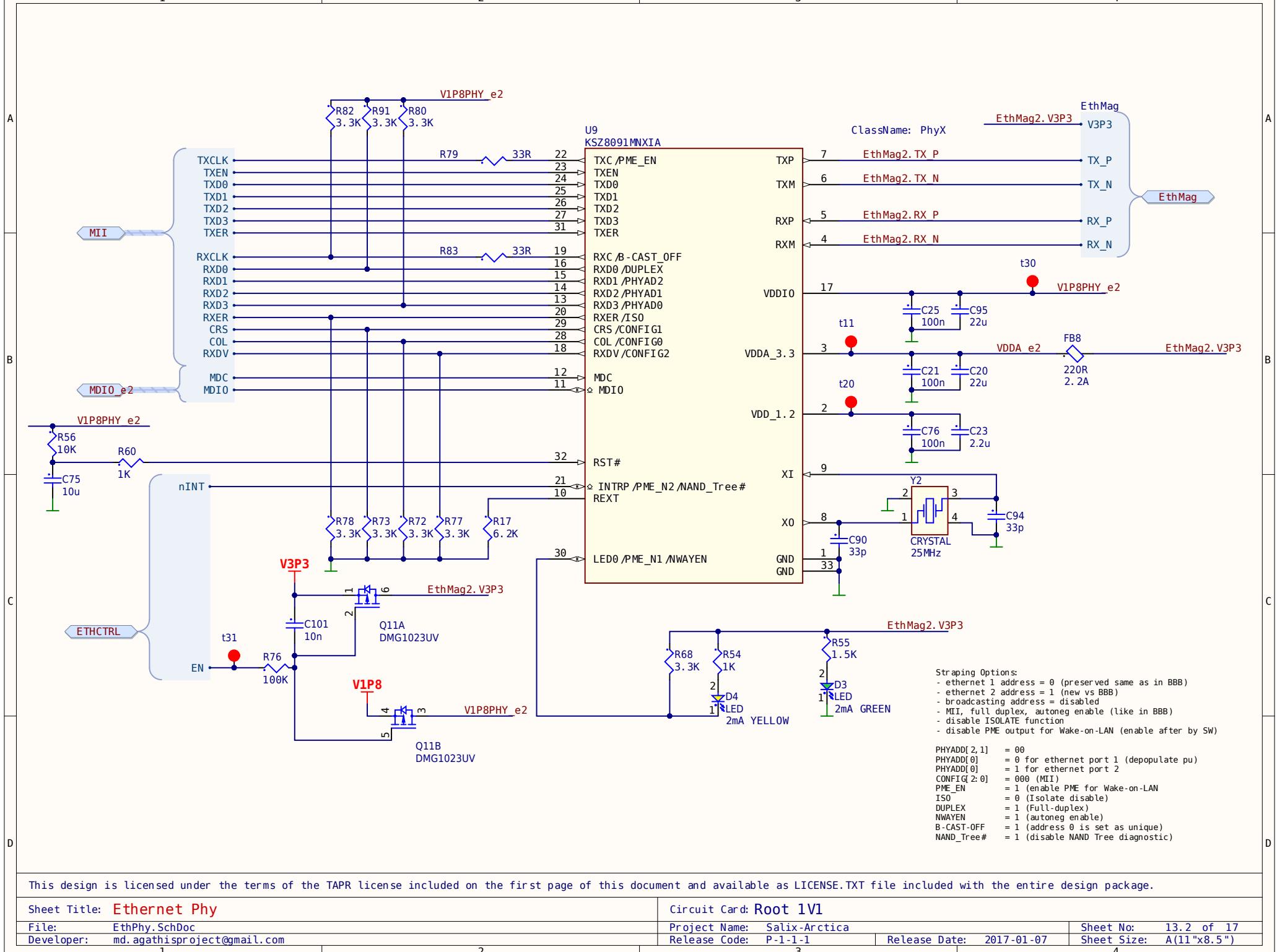
CPU

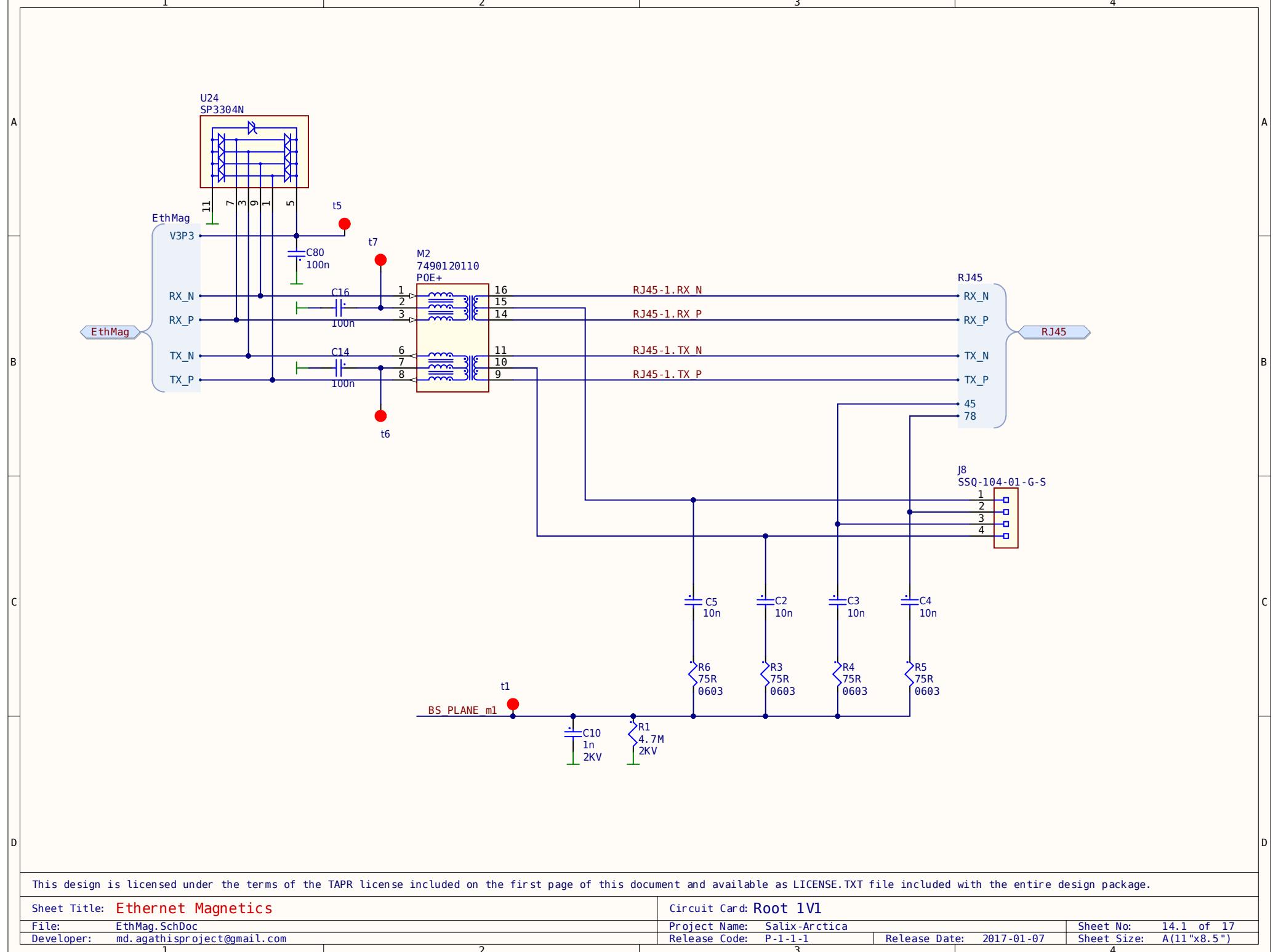


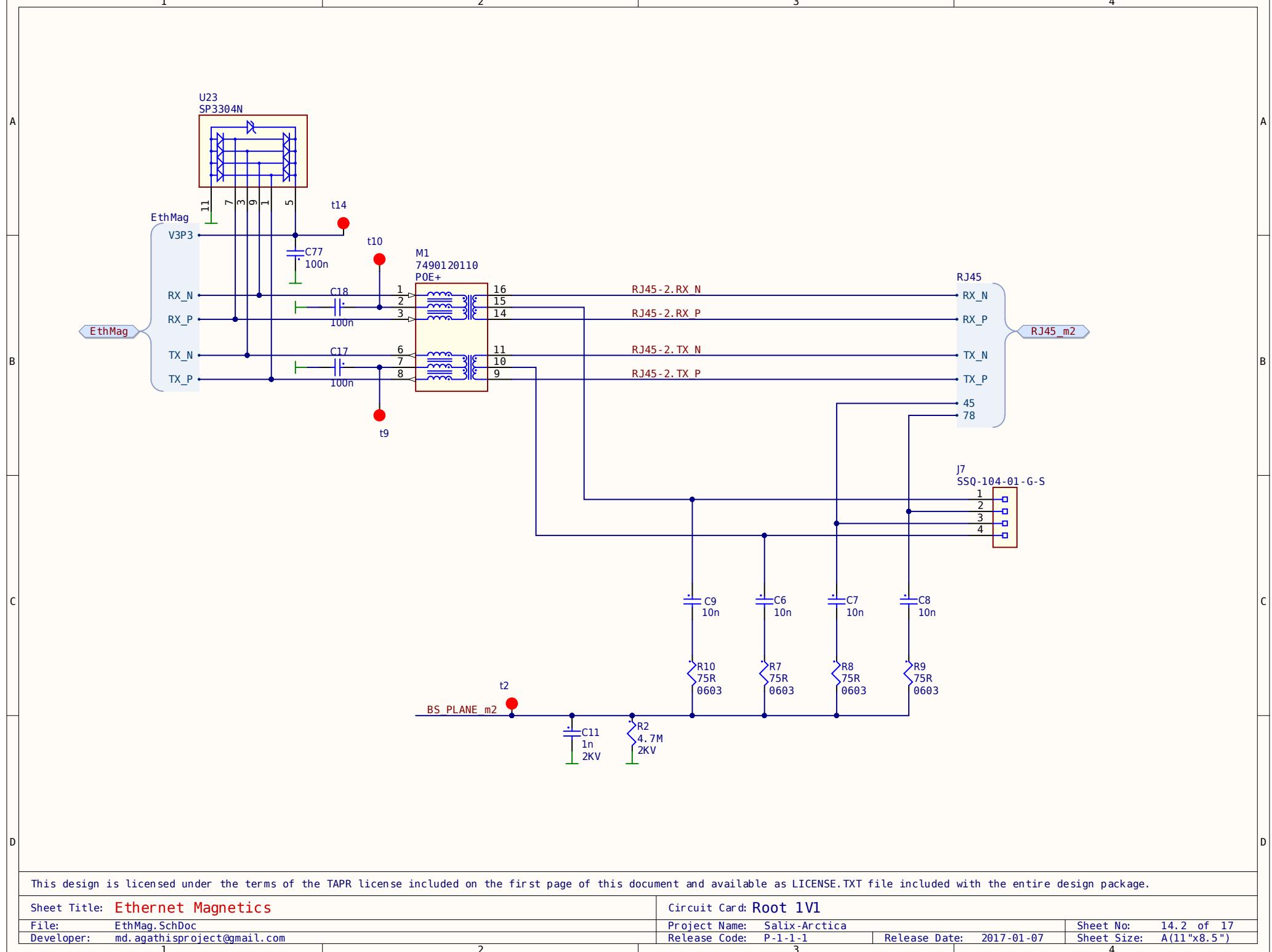
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Sheet Title: Low Power DDR	Circuit Card: Root 1V1
File: LPDDR.SchDoc	Project Name: Salix-Arctica
Developer: md.agathisproject@gmail.com	Release Code: P-1-1-1 Release Date: 2017-01-07



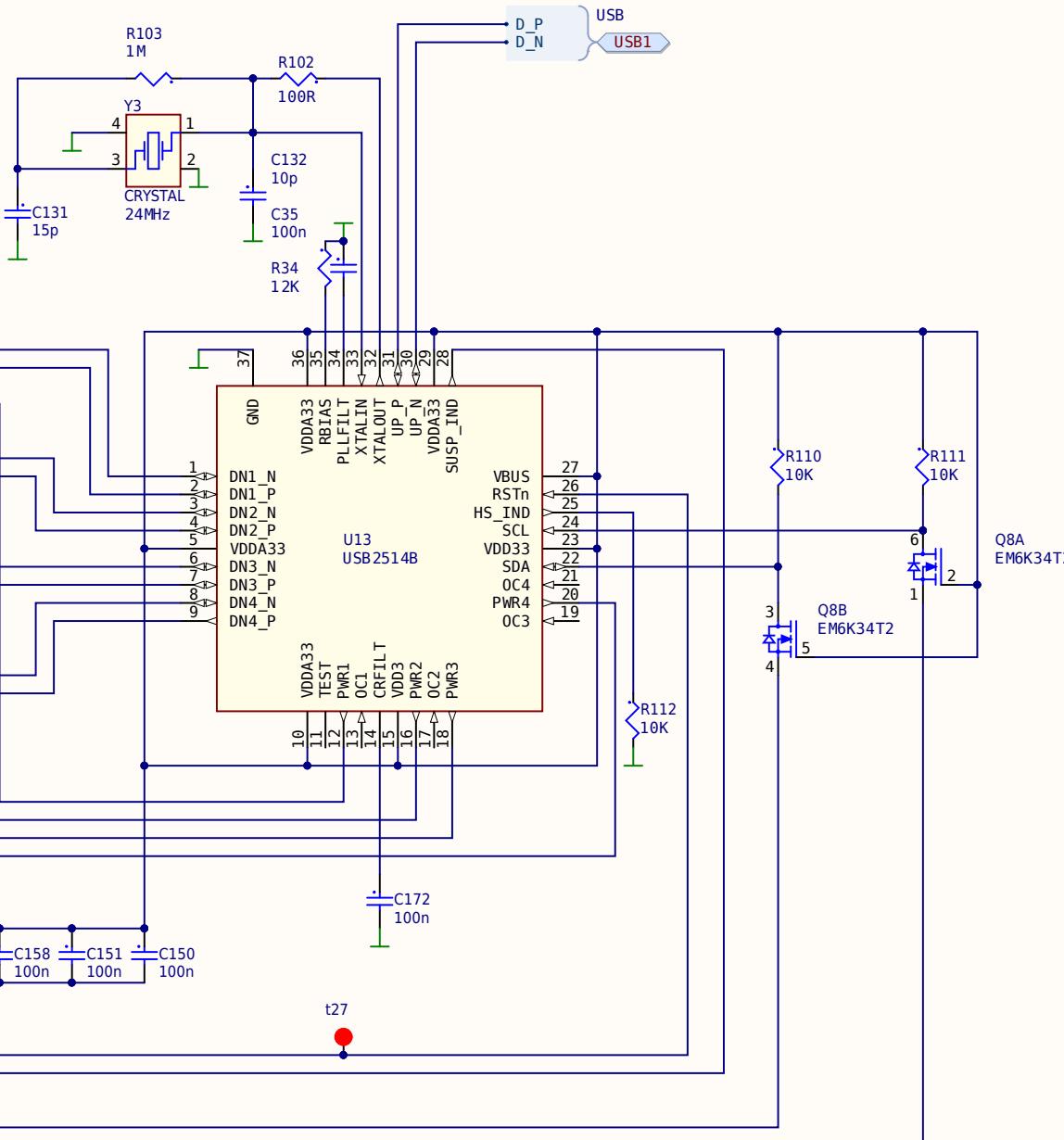






A

CFG_SEL[0] = 1 (SCL pu)
 CFG_SEL[1] = 0 (HS_IND pd)
 The hub is configured externally over SMBus (as an SMBus slave device):
 * Strap options disabled
 * All registers configured over SMBus



B

B

C

C

D

D

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Sheet Title: **USB Hub**

Circuit Card: **Root 1V1**

File: **USB_hub.SchDoc**

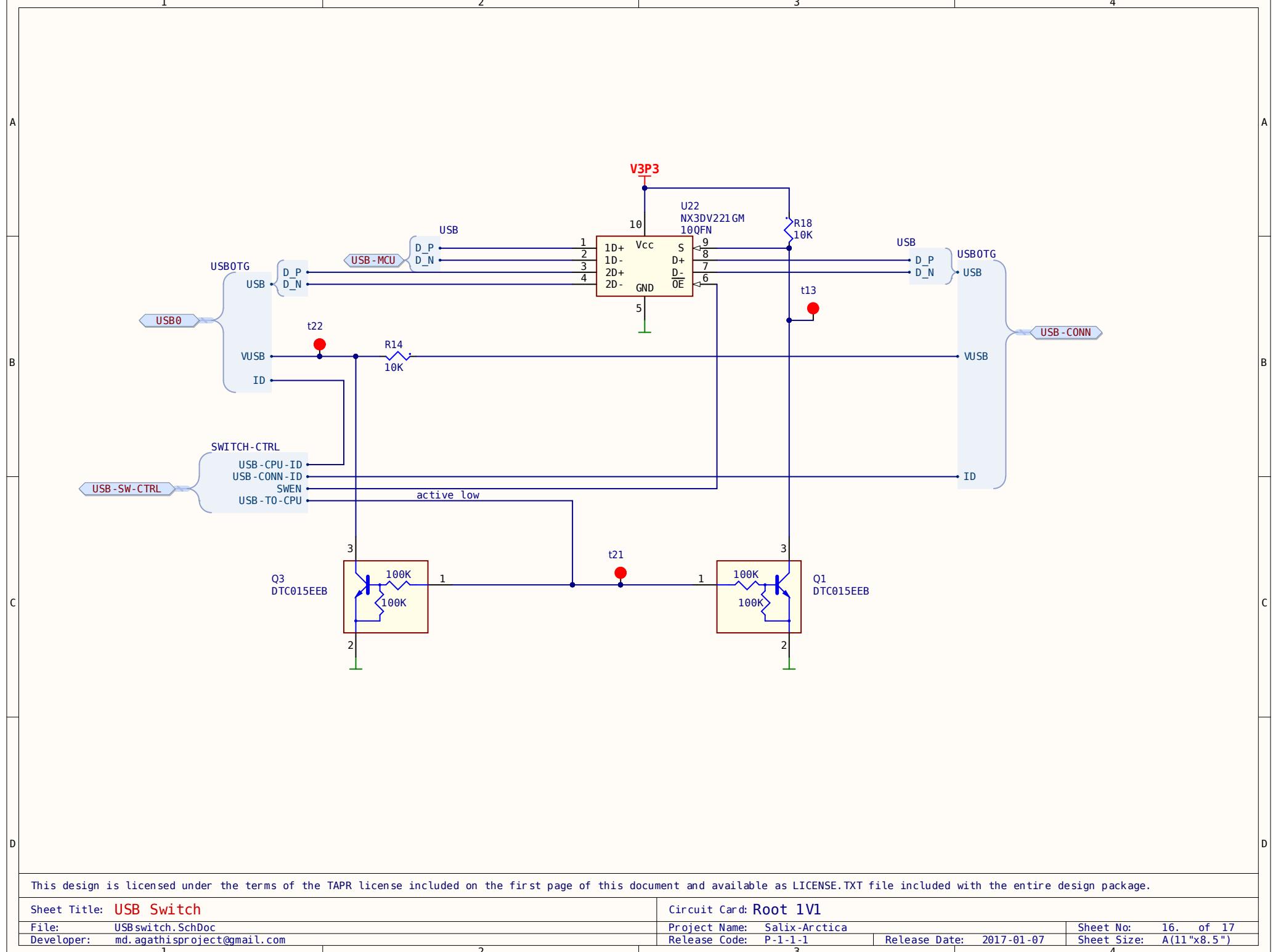
Project Name: **Salix-Arctica**

Sheet No: **15. of 17**

Developer: **md.agathisproject@gmail.com**

Release Code: **P-1-1-1**

Sheet Size: **A(11"x8.5")**

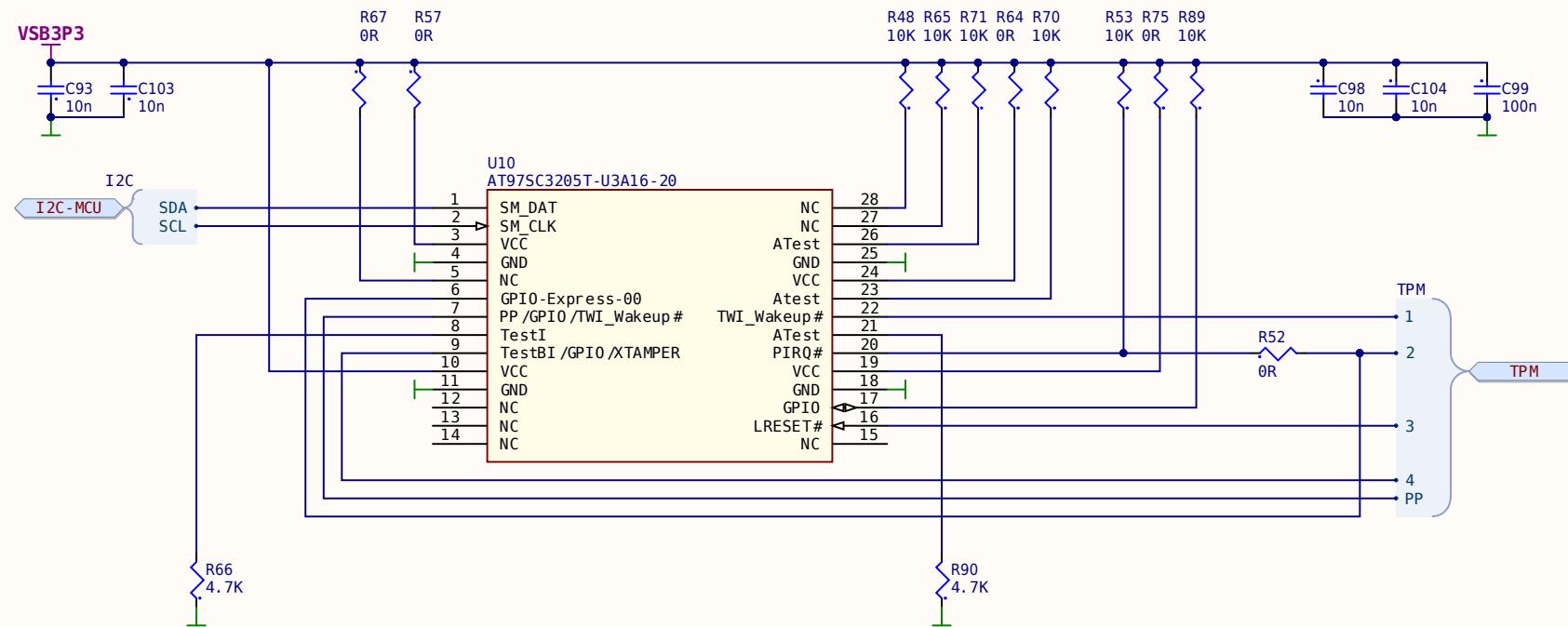


A

TPM harness signal mapping for alternate parts:

	AT97SC3205T(Atmel)	ST19NP18(STMicro)	SLB9645(Infineon)
1	TWI_WakeUp.22	pu	nc
2	GPIO-EXPRESS-00 AND PIRQ#	DataAvailable	DataAvailable
3	LRESET#	LRESET#	nc
4	GPIO /XTamper	AcceptCmd	RESET#
PP	PP /TWI_Wakeup.7	PP	PP

B



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Sheet Title: Trusted Platform Module (TPM)

Circuit Card: Root 1V1

File: TPM.SchDoc

Project Name: Salix-Arctica

Sheet No: 17. of 17

Developer: md.agathisproject@gmail.com

Release Code: P-1-1-1

Sheet Size: A(11"x8.5")