

TUTORIAL NINE**Memory Organization (Part 2)**

1. Considering a computer system with a 10-bit logical address. Translate the logical address 1000011011 to the corresponding physical address for the following two cases:
 - a) Assuming paging is used, the page size is 128 bytes and the page table is as given in Figure Q4a.
 - b) Assuming segmentation is used, the maximum segment size that the system can support is 256 bytes, and the segment table is as given in Figure Q4b.

0	01011
1	00010
2	00010
3	10101
4	01001
5	01100
6	11010
7	00110

Figure Q1a

0	00010000	010000000000
1	00001000	100000000000
2	00100000	010011010000
3	00011000	100001100000

Figure Q1b

2. A paged memory system uses the page size of 1024 bytes. Size of a page table entry is 4 bytes and the logical address space is 2^{30} bytes.
 - a) What is the size of the page table if single level of paging is used?
 - b) What is the minimum number of levels of page tables needed in this system to ensure that the outmost page table will fit within a single page frame?
 - c) Draw an address translation diagram to show how logical address translation is performed.

Virtual Memory (Part 1)

3. A computer has four page frames. The time of loading, time of last access, and the R bit for each page are as shown below (the times are in clock ticks):

<u>PAGE</u>	<u>LOADED</u>	<u>LAST ACCESS.</u>	<u>R</u>
0	126	279	0
1	230	260	0
2	120	272	1
3	160	280	1

- a) Which page will FIFO replace?
- b) Which page will second chance replace?
- c) Which page will LRU replace?

4. For each of the page replacement policies listed below, calculate the number of page faults encountered when referencing the following pages:

0 1 6 0 3 4 0 1 0 3 4 6 3 4

Assume the availability of 4 empty page frames.

- a) FIFO
- b) CLOCK
- c) LRU