CORE 64 INTERACTIVE CORE MEMORY BADGE V0.4 LOGIC BOARD

Sheet: Power — File: Core64 LB v0.4 Power.sch

Sheet: Driver — File: Core64 LB v0.4 Driver.sch

Sheet: Sense_LEDs_ID — File: Core64 LB v0.4 Sense_LEDs_ID.sch

Sheet: Expansion — File: Core64 LB v0.4 Expansion.sch

*** MUST CUT THE USB–VIN on back of TEENSY 3.2 ***

TEENSY 3.2 MCU CONNECTIONS

Teensy LC has incoming USB power/programming on board.
Because VIN–VUSB is cut on the back of the Teensy, power into the Teensy's USB port is routed in this order:
TEENSY VUSB –> ON/OFF & LIPO –> 5V REG –> TEENSY VIN

R5 10K — TEENSY_3V3

Teensy 3V3 is only used for AREF and TeensyView. Current is limited, do not use for anything else.

J4 PRG

SILKSCREEN UNDER TEENSY: CUT VIN–BUSB

U2 Teensy3.2

TEENSY_VUSB — TEENSY_VIN 3.6–6.0V — J12 TEENSY Cur. Mon.

Spare IO	SPI Devices [OPTIONAL]	8 Core Plane Selector [OPTIONAL] Requires other modifications.	PRIMARY USE 1 Core Plane
		SAO_G1_or_SPARE_1_or_CP_ADDR_0	Q1P
		SAO_G2_or_SPARE_2_or_CP_ADDR_1	Q1N
	OLED_SPI_CS		Q2P
	TOUCH_SPI_CS		Q2N
IR_OUT			Q3P
	SD_SPI_CS		Q3N
		TFT_SPI_CS	Q4P
		TFT_SPI_DC	Q4N
SPARE_4_IR_IN	TEENSYVIEW_SPI_CS		
		SPI_SDO	
		SPI_SDI	
SPARE_ADC_DAC			
		SPI_CLK	
		SPARE_3_or_CP_ADDR_2	
SPARE_5		SPI_RESET	
			Q5P
			Q5N
I2C_DATA			
I2C_CLOCK			
		TFT_BACKLIGHT	LED_ARRAY_3V3_SIG

All analog–only pins (A10–A14), AREF, Program and Reset are 3.3V only.

I2C here, there, and everywhere.

3.2" TFT as LED Array Replacement [OPTIONAL]

Left Edge		Back R7		Back L7		Back 1x4		Right Edge	
1	GND		A13	51					
2	0_RX1_Touch		3.3V	50					
3	1_TX1_Touch		33_Touch	49	Q10N				
4	2		32_Touch_PWM	48	Q10P				
5	3_TX_PWM		31_A20_TX2	47	Q9N				
6	4_RX_PWM		30_A19_SDA1	46	Q9P				
7	5_TX1_PWM		29_A18_SCL1	45	Q8N				
8	6_PWM			44	Q8P				
9	7_RX3_DOUT			43	Q7N				
10	8_TX3_DIN			42	Q7P				
11	9_RX2_CS_PWM		28_A17	41	Q6N				
12	10_TX2_CS_PWM		27_A16	40	Q6P				
13	11_DOUT		26_A15_RX2	39					
14	12_DIN		25_Touch_PWM	38	SPARE_ANA_7				
15	VBat	Bottom Edge	24	37	SD_SPI_CD				
16	3.3V		GND	36	SPARE_ANA_6				
17	GND		A12	35					
18	Program		A11	34					
19	A14/DAC		A10	33					
20	13_LED_SCK		AREF	32					
21	14_A0_SCK		VUSB	31					
22	15_A1_CS_Touch		Vin	30	WRITE_ENABLE		OLED_SPI_DC		
23	16_A2_SCL0_Touch		AGND	29	SENSE_PULSE				
24	17_A3_SDA0_Touch		3.3V_max100mA	28	SENSE_RESET		TEENSYVIEW_SPI_DC		
25	18_A4_SDA0_Touch		23_A9_Touch_PWM						
26	19_A5_SCL0_Touch		22_A8_Touch_PWM						
27	20_A6_CS_PWM		21_A7_RX1_CS_PWM						

PRIMARY USE 1 Core Plane	SPI Devices [OPTIONAL]	Spare Analog
SPARE_ANA_8		
		All analog–only pins (A10–A14), AREF, Program and Reset are 3.3V only.
SPARE_ANA_7		
SPARE_ANA_6		

VBAT_MON — Reads 1/4 voltage of +VSW (after RPP) before regulators.

GNDD

RTC CLOCK BATTERY [OPTIONAL]

BT1 3V

SILKSCREEN: RTC BAT. CR2032

To use the Teensy 3.2 RTC you must add two things:
1) Crystal: 32.768 kHz, 12.5 pF Citizen CFS–206, Digi–Key 300–8763–ND (5ppm) (on bottom side of the Teensy board, not shown in this schematic)
2) Battery Holder: MPD BC–2003, Digi–Key BC–2003–TR–CT–ND
3) Battery: 3V CR2032 Digi–Key P189–ND (battery and holder on backside of logic board)

QxP (PNP) is normally high, low to activate matrix transistor.
QxN (NPN) is normally low, high to activate matrix transistor.

SILKSCREEN FRONT

Interactive Core Memory
All logic is 3V3 Level

L1 Core_64_Logo

L2 Core_64_Logo

SILKSCREEN BACK

Core 64 Logo
Interactive Core Memory
QR Code
Maker
Website
RTC Battery CR2032
PCB Maker
Assembler
Serial Number
P/N
REV

L3 Core_64_Machineldeas_Link

All non–polarized capacitors are X7R or X5R ceramic unless otherwise noted.

BOM TO DO: TEENSY requires at least three headers that do not get auto populated in the BOM from KICAD.

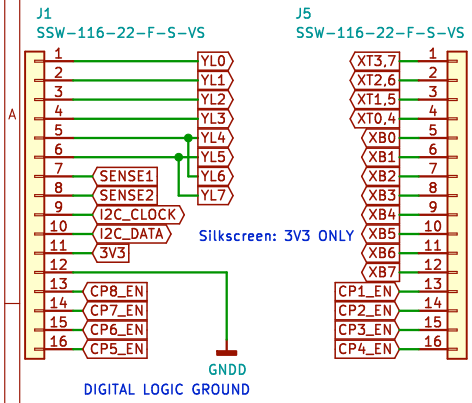
Andy Geppert
As fabricated
Core64.Machineldeas.com

Sheet: /
File: Core64 LB v0.4.sch

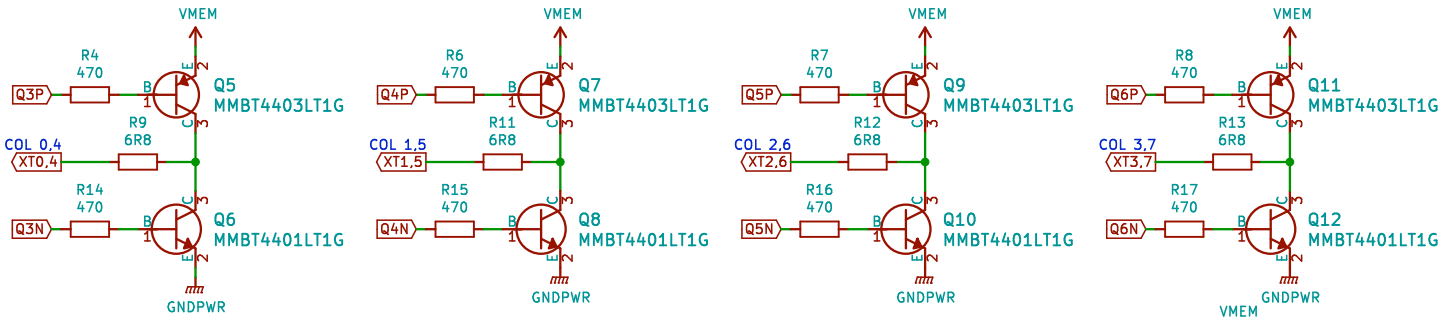
Title: Core 64 – Main Sheet Index

Size: A	Date: 2020–11–19	Rev: 0.4
KiCad E.D.A. kicad (5.1.2–1)–1		Id: 1/5

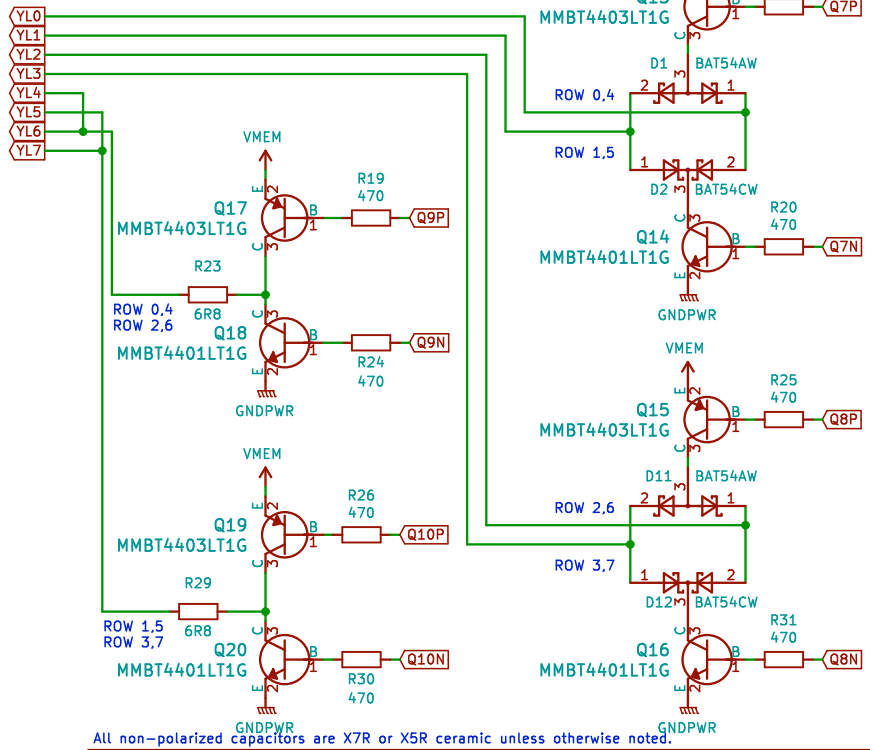
CORE BOARD INTERCONNECTS



CORE MATRIX TOP COLUMN DRIVERS

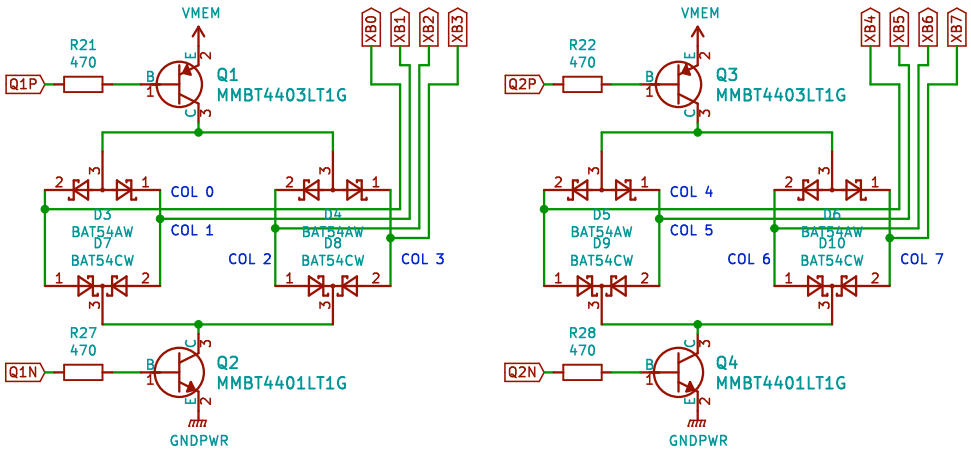


CORE MATRIX ROW DRIVERS

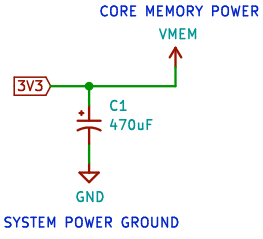


QxP (PNP) is normally high, low to activate matrix transistor.
QxN (NPN) is normally low, high to activate matrix transistor.

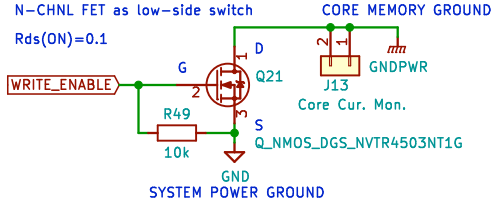
CORE MATRIX BOTTOM COLUMN DRIVERS



CORE MATRIX POWER



CORE MATRIX WRITE ENABLE



All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

Drive Transistor current: 3.3/470=7mA (too much for Teensy LC)
Matrix 1/2 select current: 3.3/6.8= 485 mA (does not acccount for voltage drop in transistors)

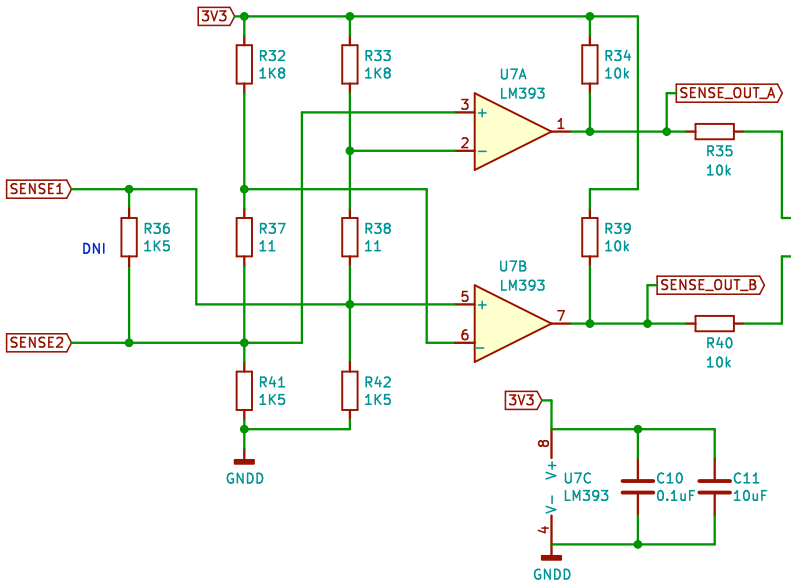
Andy Geppert
As fabricated
Core64.Machineldeas.com

Sheet: /Driver/
File: Core64 LB v0.4 Driver.sch

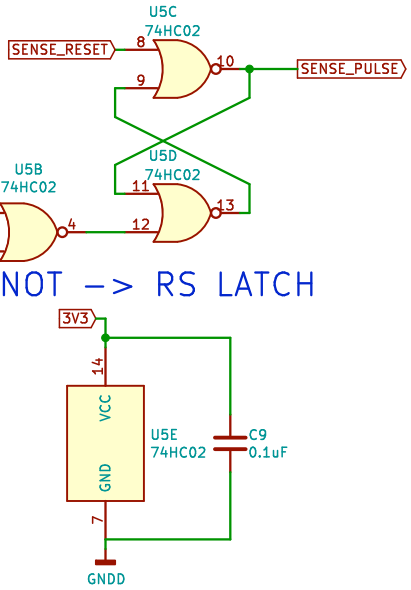
Title: Core 64 – Core Matrix Driver

Size: A	Date: 2020-11-19	**Rev: 0.4**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 2/5

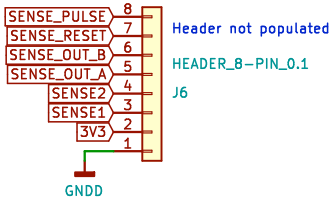
SENSE SIGNAL DIFFERENTIAL AMPLIFIERS



SENSE SIGNAL LATCH

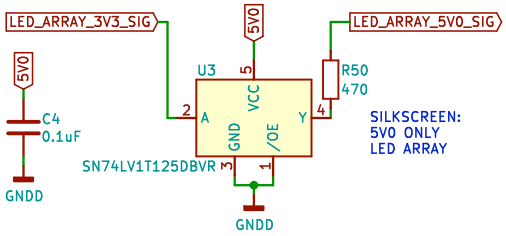


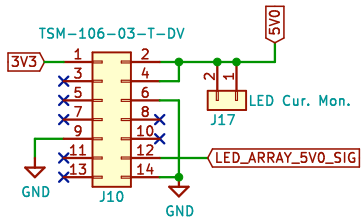
SENSE DEBUG



SILKSCREEN: 3V3 ONLY
SENSE DEBUG

LED ARRAY DRIVE AND LEVEL SHIFT



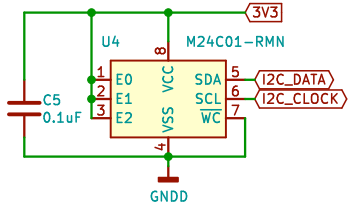


TSM-106 (2x6) required
TSM-107 (2x7) alternate

Symbol view is looking down on the front face of the Logic Board, with the male header pins pointing up at you.

BOARD ID AND S/N

EEPROM I2C ADDRESS: 0b1010111, 0x57 (87)



All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

Andy Geppert
As fabricated
Core64.MachineIdeas.com

Sheet: /Sense_LEDs_ID/
File: Core64 LB v0.4 Sense_LEDs_ID.sch

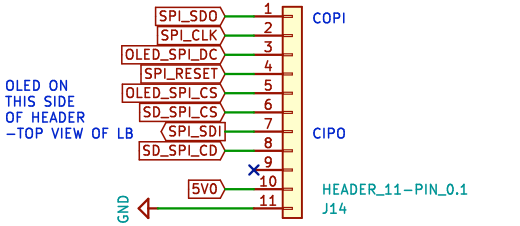
Title: Core 64 - Sense

Size: A	Date: 2020-11-19	**Rev: 0.4**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 3/5

EVERYTHING ON THIS SHEET IS USER-PROVIDED OPTIONAL ADD-ONS

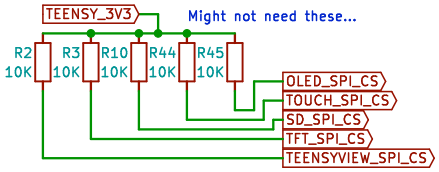
OLED COLOR SPI w/MicroSD

Compatible: https://www.adafruit.com/product/1431
1.5" 128x128, 16-bit color w/MicroSD holder
OLED has 5V -> 3V3 regulator onboard.
MicroSD card standalone pins shared between TFT and OLED boards.

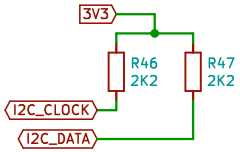


SILKSCREEN: 3V3 Logic ONLY, 3V3/GND sides of jumpers, SPI OLED

SPI CS PULL-UPS

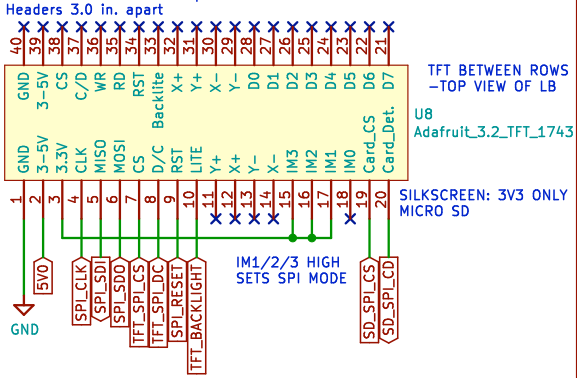


I2C PULL-UPS



3.2" TFT LCD SPI w/MicroSD

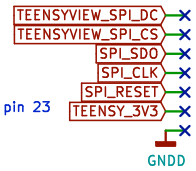
Compatible with https://www.adafruit.com/product/1743
TFT has 5V -> 3V3 regulator onboard.
MicroSD card standalone pins shared between TFT and OLED boards.
Headers 3.0 in. apart



OLED TEENSYVIEW SPI

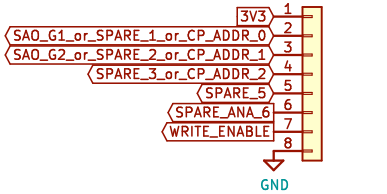
Monochrome 128x32
The TeensyView is designed to stack on the Teensy 3.2
Configuration: https://www.sparkfun.com/products/14048

Use only these Teensy pins:
21: D/C (default is 5)
10: CS
11: MOSI
13: SCLK
15: RESET
3.3V Power from Teensy next to pin 23
GND at corner next to pin 0

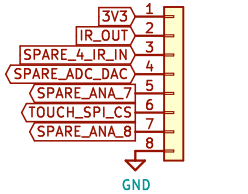


GPIO#1

Silkscreen: 3V3 ONLY pin names



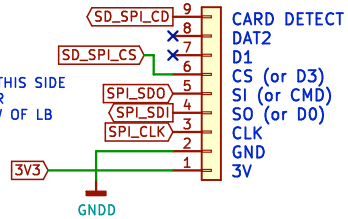
GPIO#2



MICRO SD CARD

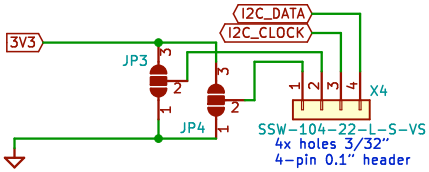
Compatible with https://www.adafruit.com/product/4682
MicroSD card standalone pins shared between TFT and OLED boards.

SILKSCREEN: 3V3 ONLY MICRO SD



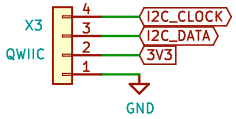
OLED MONOCHROME I2C

0.96" (128x64)
I2C 4-pins, ADDRESS: 0x3C (60 decimal)
Alternate is 0x3D, not 0x7A or 0x78 (wrong 8-bit)!
Must choose power polarity by soldering SJS.



SILKSCREEN: 3V3 ONLY, 3V3/GND sides of jumpers, I2C OLED and pin names

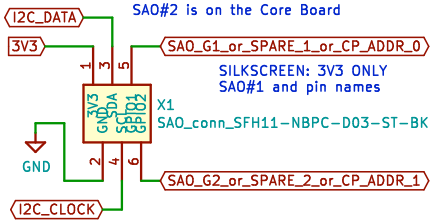
QWIIC I2C



SILKSCREEN: 3V3 ONLY
QWIIC I2C and pin names

SAO #1 SUPERIOR ADD-ON

SAO#2 is on the Core Board



SAO v1.69bis (https://hackaday.io/project/52950-shitty-add-ons)
using Sullins SFH11-NBPC-D03-ST-BK female header
https://www.digikey.com/product-detail/en/sullins-connector-solutions/SFH11-NBPC-D03-ST-BK/S9717-ND/4558818

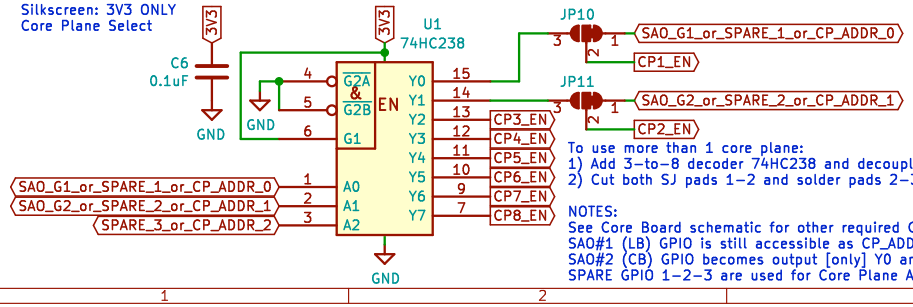
I2C ADDRESS TABLE

INCLUDED:	
AMBIENT LIGHT SENSOR	0X29 (47)
HALL SENSOR 1	0x30 (48)
HALL SENSOR 2	0x31 (49)
HALL SENSOR 3	0x32 (50)
HALL SENSOR 4	0x33 (51)
EEPROM (BOARD ID)	0x57 (87)
OPTIONAL:	
OLED	0x3C (60)
AND!XOR IO Exp. MCP23017	0x20 (32)
AND!XOR EEPROM AT24C32r	0x50 (80)
NFC CLICK PN7120	0x50-53
PIMORONI UNICORN HAT	0x50 (N.C.)

All 7-bit addresses should be greater than 0x07 and less than 0x78 (120).

CORE PLANE & CORE BOARD SAO #2 GPIO SELECT

Silkscreen: 3V3 ONLY
Core Plane Select



To use more than 1 core plane:
1) Add 3-to-8 decoder 74HC238 and decoupling capacitor.
2) Cut both SJ pads 1-2 and solder pads 2-3.

NOTES:
See Core Board schematic for other required CB changes.
SAO#1 (LB) GPIO is still accessible as CP_ADDR_0 and 1, shared.
SAO#2 (CB) GPIO becomes output [only] Y0 and Y1 of CP selector.
SPARE GPIO 1-2-3 are used for Core Plane Addressing.

All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

Andy Geppert
As fabricated
Core64.Machineldeas.com
Sheet: /Expansion/
File: Core64 LB v0.4 Expansion.sch

Title: Core 64 - Expansion

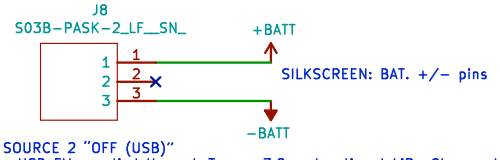
Size: A	Date: 2020-11-19	**Rev: 0.4**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 4/5

STANDARD KIT CONFIGURATION – AS MANUFACTURED

TWO POWER INPUT SOURCES SELECTED BY SPDT SWITCH

SOURCE 1 "ON (BAT)"
BUILT-IN BATTERY PACK (Keystone 2482CN) WITH 4X "AAA" Primary/Alkaline Cells
OK to use Energizer Ultimate Lithium (light weight!) with open cell 7.2V, loaded will be <7V.
Battery Pack includes wires and 3-pin plug.

Socket: TH, Side Entry, JST PA S03B-PASK-2(LF)(SN), Digikey 455-1848-ND ($0.44/ea)
Socket: SMT, Top Entry, JST PA BM03B-PASS-1-TFT(LF)(SN), Digikey 455-2638-1-ND ($0.80)
Socket: SMT, Side Entry, Keystone 976, Digikey 36-976CT-ND ($2.71/ea)



SILKSCREEN:
7.5V MAX !!!
Limitation of 5V0 regulator.

SOURCE 2 "OFF (USB)"
USB 5V supplied through Teensy 3.2 and optional LiPo Charger USB port.
With the VIN-VUSB trace cut on the back of the Teensy, the TEENSY_VUSB is taken off of the Teensy Board and routed on the Core64 LB to the lower position of the power switch. From here, it powers the whole Core64 system and routes back to the TEENSY_VIN after passing through the 5V LDO regulator.

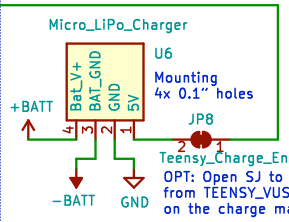
ALTERNATE 1S LIPO BATTERY – USER SUPPLIED

1) Remove the 4x "AAA" battery pack AND the battery connector (so you don't try to charge AAAs with a LiPo charger!).

2) Purchase and install a LiPo charge manager.
a) The logic board is designed to accept this one: https://www.adafruit.com/product/1904.
b) Solder the the charge manager directly to the board without headers to keep a low profile to allow the stylus to fit.

3) Purchase and install a 1S LiPo using double-sided tape.
a) Choose a 1S Lipo with built-in cell over/under voltage protection. Recommended:
2500mAh https://www.adafruit.com/product/328 1.8" x 2.4" x 0.26" (47mm x 61mm x 6.7mm)
2000mAh https://www.adafruit.com/product/2011 2.4" x 1.4" x 0.3" (60mm x 36mm x 7mm)
1200mAh https://www.adafruit.com/product/258 1.3" x 2.4" x 0.2" (34mm x 62mm x 5mm)
b) The LiPo can be up to 50 x 65 x 15mm. A maximum SILKSCREEN: +/- pins
a) Make sure no part of the LiPo foil pouch can short-out adjacent pins or pads in the area.
b) Insulate it with Kapton tape or similar.

* The LiPo charger 5V pin and USB port are also connected to the Teensy USB port, through TEENSY_VUSB.
* Connecting a USB cable to the Teensy will power the Core64 board, charge the battery and connect to the serial port of the Teensy. If you do NOT want the Core64 board to be powered from the USB port of the charger, cut the Teensy_Charge_Enable solder jumper. Then, connecting a USB cable to the LiPO charger will ONLY charge the battery and power the logic board, when the power switch is ON (up position).



SILKSCREEN: LIPO CHARGER

1S LIPO ONLY !!!

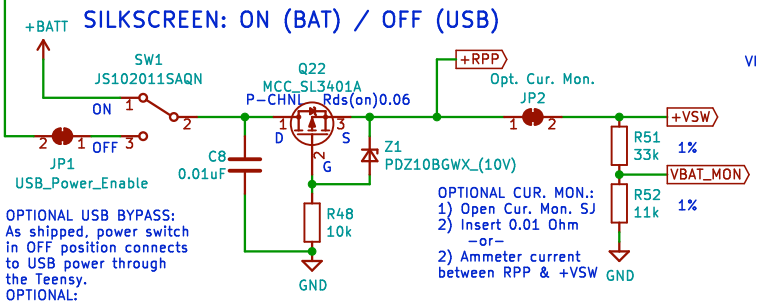
SILKSCREEN: BAT. + BAT. –

***** ALL CONFIGURATIONS REQUIRE CUTTING VIN-VUSB TRACE ON BACK OF TEENSY *****

TEENSY_VUSB

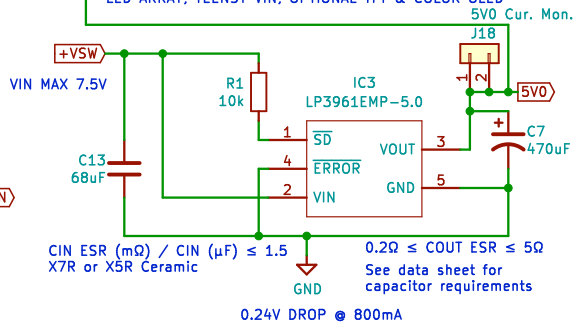
TEENSY_VIN

POWER SWITCH, RPP, V & I MONITOR



5V POWER SUPPLY

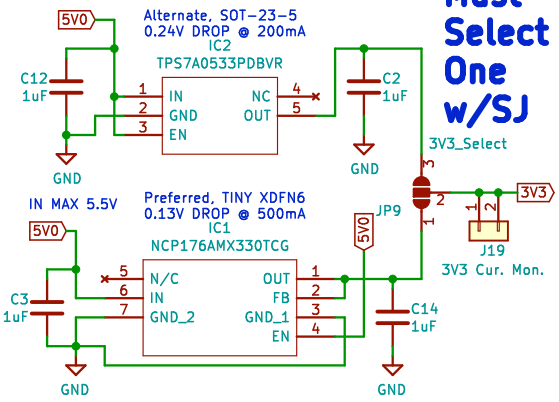
LED ARRAY, TEENSY VIN, OPTIONAL TFT & COLOR OLED



3.3V POWER SUPPLY

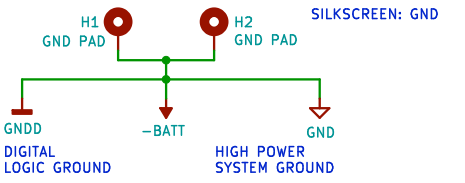
CORES, ACCESSORIES, ALL LOGIC

Must Select One w/SJ

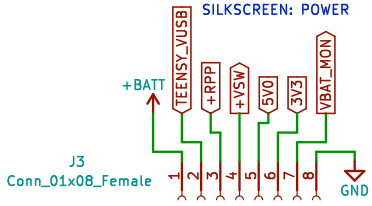


ALL SYSTEM GROUND

GND PAD 3.2 mm (.125 in) thru-hole for M3 or #4 screw



POWER RAILS



All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

Andy Geppert
As fabricated
Core64.Machineldeas.com
Sheet: /Power/
File: Core64 LB v0.4 Power.sch

Title: Core 64 – Power Schematic

Size: A	Date: 2020-11-19	**Rev: 0.4**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 5/5