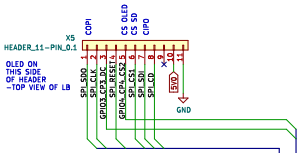
HACKER PLAYGROUND

USER-PROVIDED OPTIONAL ADD-ONS SEE CORE64 HACKER GUIDE

OLED COLOR SPI W/MICRO SD

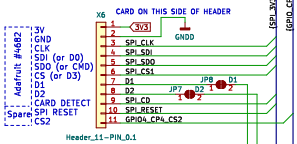
Compatible: https://www.adafruit.com/product/1431
1.5" 128x128 16-bit color w/MicroSD holder
OLED has 5V -> 3V3 regulator onboard.
MicroSD card standalone pins shared between TFT and OLED boards.



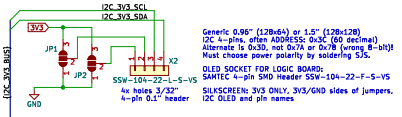
SILKSCREEN: 3V3 Logic ONLY, 3V3/GND sides of jumpers, SPI OLED

MICRO SD CARD, SPI

Compatible with https://www.adafruit.com/product/4682 (pins 1-6, 9)
MicroSD card standalone pins shared between TFT and OLED boards.



OLED MONOCHROME I2C

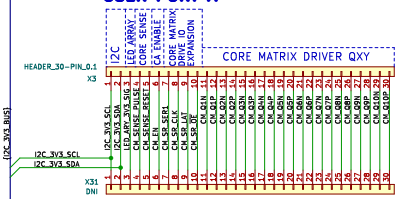


Generic 0.96" (128x64) or 1.5" (128x128)
I2C 4-pins, often ADDRESS: 0x3C (60 decimal)
Alternate is 0x3D, not 0x7A or 0x7B (wrong 8-bit)t
Must choose power polarity by soldering SJ5.

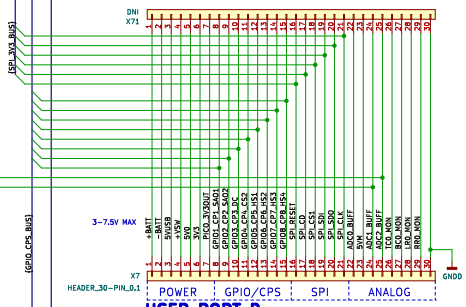
OLED SOCKET FOR LOGIC BOARD:
SAMTEC 4-pin SMD Header S5W-104-22-F-S-VS

SILKSCREEN: 3V3 ONLY, 3V3/GND sides of jumpers, I2C OLED and pin names

USER PORT A



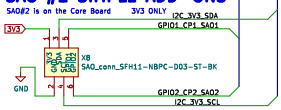
0.1" PIN GRID



USER PORT B

SAO #1 SIMPLE ADD-ONS

SAO#2 is on the Core Board 3V3 ONLY



https://hackaday.io/project/175182-simple-add-ons-sao
using Sullins SFH11-NBPC-D03-ST-BK female header
https://www.digikey.com/product-detail/en/sullins-connector-solutions/SFH11-NBPC-D03-ST-BK/S9717-ND/4558818

QWIIC I2C

3V3 ONLY

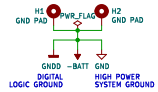
I2C ADDRESS TABLE

OPTIONAL:

AMBIENT PROX. SENSOR	0x38 (56)
OLED	0x3C (60)
ANDKOR IO Exp. MCP23017	0x20 (32)
ANDKOR EEPROM AT24C32C	0x50 (80)
NFC CLICK PN7120	0x50-53

SYSTEM GROUNDS

2x GND PAD 3.2 mm (.125 in) thru-hole for M3 or #4 screw



CORE MATRIX DRIVE AND SHIFT REGISTER

Some of the spare IO on the Logic Board is not accessible on the Hacker Board:
Spare SR Shift Register Outputs A, B, C, D

If you intend to directly drive the Core Matrix Transistors (CM_QxN and CM_QxP) you need to make sure the Shift Registers outputs do not interfere. To set those outputs to a high impedance (disconnected) state, pull User Port A pin 10 CM_SR_/OE high to 3.3V with a 1-5K resistor.

If you intend to use the Shift Registers to indirectly drive the Core Matrix Transistors you need to pull User Port A pin 10 CM_SR_/OE low to GND with a 1-5K resistor.

ANALOG

All eight analog pins are pre-connected to different parts of the Logic Board.
To use the analog pins for your own purposes, review the Logic Board connections and cut the traces associated with the solder jumpers and net-ties on the signal paths you want to use.

Two of the analog pins are shared with the Micro SD Card (SPI) header using solder jumpers (default open) on the Logic Board.

User Port B Pin 22, Analog A is connected to Pico ADC0, defaults as
User Port B Pin 23, Analog B is connected to
User Port B Pin 24, Analog C is connected to Pico ADC1 and defaults as VMEM_MON
User Port B Pin 25, Analog D is connected to Pico ADC2 and defaults as GMEM_MON
User Port B Pin 26, Analog E is connected to TCO_MON
User Port B Pin 27, Analog F is connected to BCO_MON
User Port B Pin 28, Analog G is connected to LCO_MON
User Port B Pin 29, Analog H is connected to RCO_MON
User Port B Pin 30, is connected to ground

ADC0, 1, 2 are bufferred to the Pico (of connected) with resistors.

POWER

Power switched is all done on the Logic Board.
Do not inject power into 5V0, 3V3, or P3V3. Those are regulated power outputs ONLY.

PASS-THROUGH PORTS

These headers are available on the Hacker Board and are wired in parallel to the same port that is on the Logic Board and Hacker Board.

USER PORT A
USER PORT B
OLED MONOCHROME I2C
OLED COLOR SPI W/MICRO SD
MICRO SD CARD, SPI (the D1 and D2 pins are shared with analog pins)
SAO #1
QWIIC I2C

Two of the analog pins are shared with the Micro SD Card (SPI) header using solder jumpers (D1, D2 default open) on the Logic Board and the Hacker Board.

SPI

Both SPI chip select lines are may be pulled high with resistors on the Logic Board.
Some Logic Boards do not include the pull-up resistors.

SILKSCREEN FRONT

SILKSCREEN BACK

Core64.io

Core64.io

I2C ADDRESS TABLE

All 7-bit addresses should be greater than 0x07 and less than 0x78 (120).

INCLUDED:

AMBIENT LIGHT SENSOR	0x29 (41)
HALL SENSOR 1	0x30 (48)
HALL SENSOR 2	0x31 (49)
HALL SENSOR 3	0x32 (50)
HALL SENSOR 4	0x33 (51)
EEPROM (BOARD ID)	0x57 (87)

All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.
WIP
Visit www.Core64.io for information on assembly and optional features.
Please read the Core64 User Guide for more details.
Concept and design by Andy Geppert @ www.MachineIdeas.com

Sheet: /		
File: Core64 HB.kicad_sch		
Title: Core64 Hacker Board (HB)		
Size: C	Date: 2023-02-16	**Rev: 0.1**
KiCad E.D.A. kicad (6.0.7-1)-1		Id: 1/1