CORE 64 INTERACTIVE CORE MEMORY BADGE V0.3 DUAL BOARD

Sheet: Power

File: Interactive Core Memory Badge (Logic) Power v0.3.sch

Sheet: MCUs

File: Interactive Core Memory Badge (Logic) MCU v0.3.sch

Sheet: Core Array Driver

File: Interactive Core Memory Badge (Logic) Driver v0.3.sch

Sheet: SENSE

File: Interactive Core Memory Badge (Logic) Sense v0.3.sch

Sheet: IO Expansion

File: Interactive Core Memory Badge (Logic) IO Expansion V0.3.sch

TO DO: Move the two MCUs to this top level sheet and remove the MCU logic sheet?

Andy Geppert – Machine Ideas, LLC

Sheet: /

File: Interactive Core Memory Badge (Logic) Main v0.3.sch

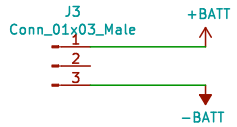
Title: Core 64 – Main Sheet Index

Size: A4	Date: 2020-03-20	**Rev: 0.3**
KiCad E.D.A. eeschema (5.1.2-1)-1		Id: 1/6

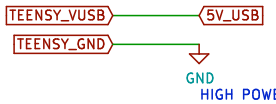
TEENSY LC OR 3.2 AND ALKALINE/NIMH BATTERY PACK
*** MUST CUT VIN-VUSB TRACE ***
THIS IS THE STANDARD MANUFACTURED KIT CONFIGURATION

TWO POWER MODES SELECTED BY DOUBLE-THROW SWITCH:

MODE 1
BUILT-IN BATTERY PACK (Keystone 2482CN) WITH 4X "AAA" ALKALINE OR NIMH CELLS
...or 3-4 "AA" alkaline/NiMh, or 1S LiPo, but the logic board does not recharge these batteries automatically from USB power.
CONNECTED TO 3 PIN input for Battery Pack
On PCB: SMT CONN, 3 TERM, HORZ, 2mm spacing, detent lock
Such as: Keystone 976, JST PA BM03B-PASS-1-TFT(LF)(SN), Adafruit 4391 (JST PH 3-pin aka STEMMA)
from KAWEEI Technology CW2001-03T-H01-BD-A,



MODE 2
USB 5V through Teensy LC or 3.2
VUSB is 5V from USB cable.
VIN must be supplied TO the Teensy and Core 64 Logic Board provides it.



HIGH POWER SYSTEM GROUND

BOTH MODES REQUIRE:
VIN must be supplied TO the Teensy and
the Core 64 Logic Board provides it here.

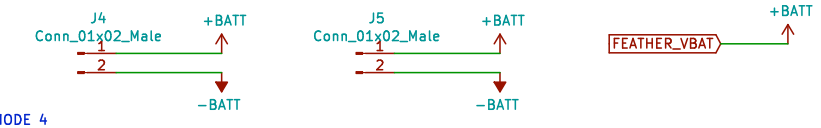
TO DO: Teensy and feather power to -Batt or GND?
Do they need to avoid the reverse polarity detector?
Or will they interfere?

HACKER POWER OPTION: ADAFRUIT FEATHER WITH REQUIRED LIPO
*** MUST REMOVE ALKALINE/NIMH BATTERY PACK ***
USER MODIFICATION REQUIRED

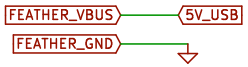
HACKER UPGRADE TO USE FEATHER REQUIRES EITHER:
A) REPLACE THE ALKALINE/NIMH BATTERY PACK WITH 1S LIPO IN THE SAME POWER PORT, OR ONE OF THE ALTERNATE PORTS
>>> ALTERNATE CONNECTOR 1 - Adafruit (1769) SMT 2-pin JST-PH (used with the Feather and Adafruit batteries)
>>> ALTERNATE CONNECTOR 2 - Generic SMT 2-pin .1" header option for everything else.
B) REMOVE THE ALKALINE/NIMH BATTERY PACK AND CONNECT 1S LIPO DIRECTLY TO FEATHER JST-PH BATTERY/CHARGING PORT.

TWO ALTERNATIVE POWER MODES SELECTED BY DOUBLE-THROW SWITCH:

MODE 3
USER REPLACED 1S LIPO BATTERY 3.7 OR 4.2V
THE FEATHER WILL TRY TO CHARGE THE BATTERY AT 100MA WHEN USB POWER IS CONNECTED.
FAILURE TO USE A 1S LIPO WILL DESTROY THE CHARGER CIRCUIT ON THE FEATHER.



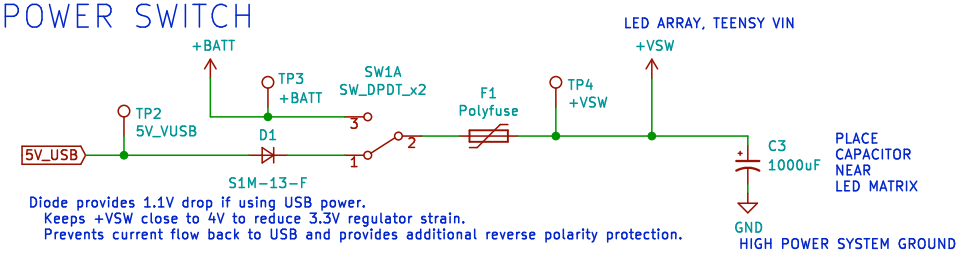
MODE 4
USB 5V through the Feather.
Automatically recharges a connected 1s LiPo at 100mA.



HIGH POWER SYSTEM GROUND

TO DO: Does Feather receive power to MCU directly from battery?
Does Feather require a battery to be connected in order to work?

POWER SWITCH

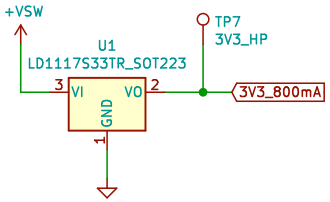


HIGH POWER SYSTEM GROUND

Diode provides 1.1V drop if using USB power.
Keeps +VSW close to 4V to reduce 3.3V regulator strain.
Prevents current flow back to USB and provides additional reverse polarity protection.

3.3V HIGH POWER SUPPLY

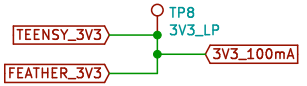
CORES AND ACCESSORIES



HIGH POWER SYSTEM GROUND

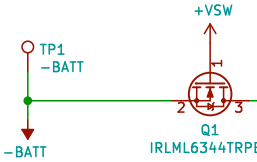
3.3V LOW POWER SUPPLY

TEENSY OR FEATHER 3.3V REGULATOR USED BY:
MCU, Analog reference, Core Sense Op-Amps, Magnetic Hall switches.



*** USE ONE 3V3 SOURCE AT A TIME ***

REVERSE POLARITY PROTECTION

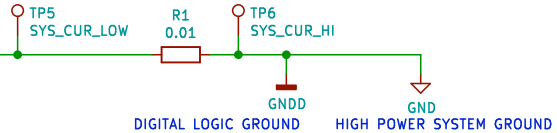


REVERSE POLARITY DETECTION AND SYSTEM
CURRENT MEASUREMENT CLOSE TO BATTERY.

REF: https://www.instructables.com/id/Reverse-polarity-protection-for-your-circuit-with/
IRLML6344TRPBF https://www.digikey.com/product-detail/en/infineon-technologies/IRLML6344TRPBF/IRLML6344TRPBFCT-ND/2538168

SYSTEM CURRENT MEASUREMENT

TO DO: Connect to analog inputs of MCU for self-test and diagnostics.



DIGITAL LOGIC GROUND
HIGH POWER SYSTEM GROUND

STAR GROUND AS MUCH AS POSSIBLE REVERSE
POLARITY FET TO GNDD (DIGITAL) AND GND (POWER).

Andy Geppert - Machine Ideas, LLC

Sheet: /Power/
File: Interactive Core Memory Badge (Logic) Power v0.3.sch

Title: Core 64 - Power Schematic

Size: A4	Date: 2020-03-15	**Rev: 0.3**
KiCad E.D.A. eeschema (5.1.2-1)-1		Id: 2/6

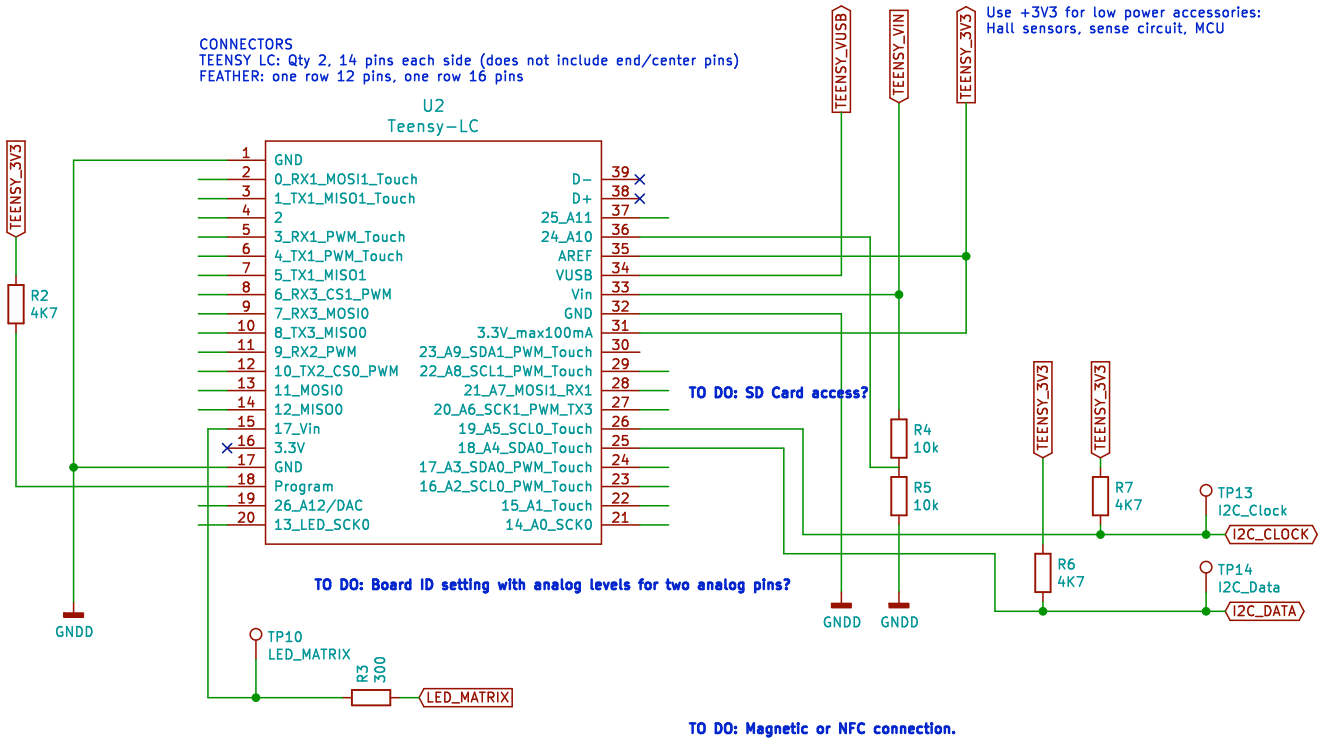
Teensy LC has incoming USB power/programming on board.

*** CUT THE USB-VIN bridge. ***

Battery Voltage Monitor for +VSW
Analog reads 1/2 battery voltage

TO DO: Add Feather module.

CONNECTORS
TEENSY LC: Qty 2, 14 pins each side (does not include end/center pins)
FEATHER: one row 12 pins, one row 16 pins



TO DO: SD Card access?

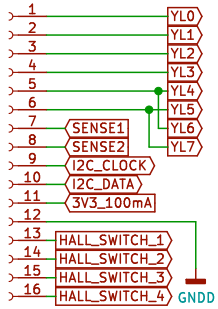
TO DO: Board ID setting with analog levels for two analog pins?

TO DO: Magnetic or NFC connection.

Andy Geppert – Machine Ideas, LLC		
Sheet: /MCUs/		
File: Interactive Core Memory Badge (Logic) MCU v0.3.sch		
Title: Core 64 – MCU Logic		
Size: A4	Date: 2020-03-15	**Rev: 0.3**
KiCad E.D.A. eeschema (5.1.2-1)-1		Id: 3/6

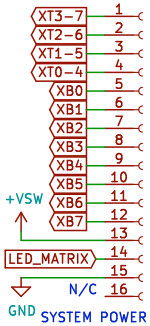
CORE BOARD INTERCONNECTS

YL: 6
SENSE: 2
SPARE: 2
GND, 3V3: 2
MHS: 4 (hall switches)
TOTAL=16
J1
Conn_01x16_Female



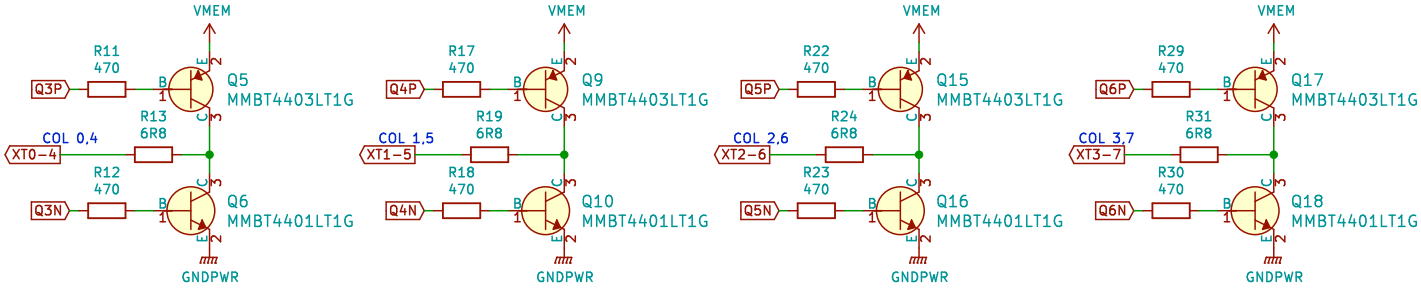
DIGITAL LOGIC GROUND

XT: 4
XB :8
LED MATRIX: 3
(V+, SIGNAL, GND)
SPARE: 1
TOTAL=16
J2
Conn_01x16_Female

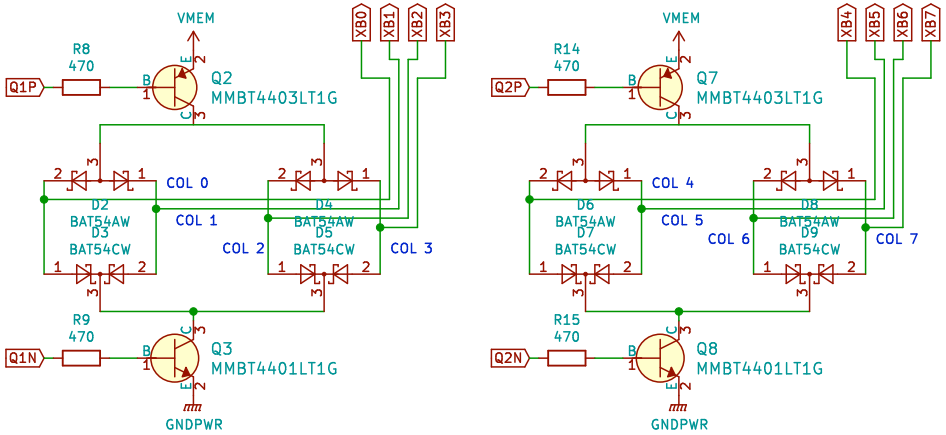


GND SYSTEM POWER GROUND

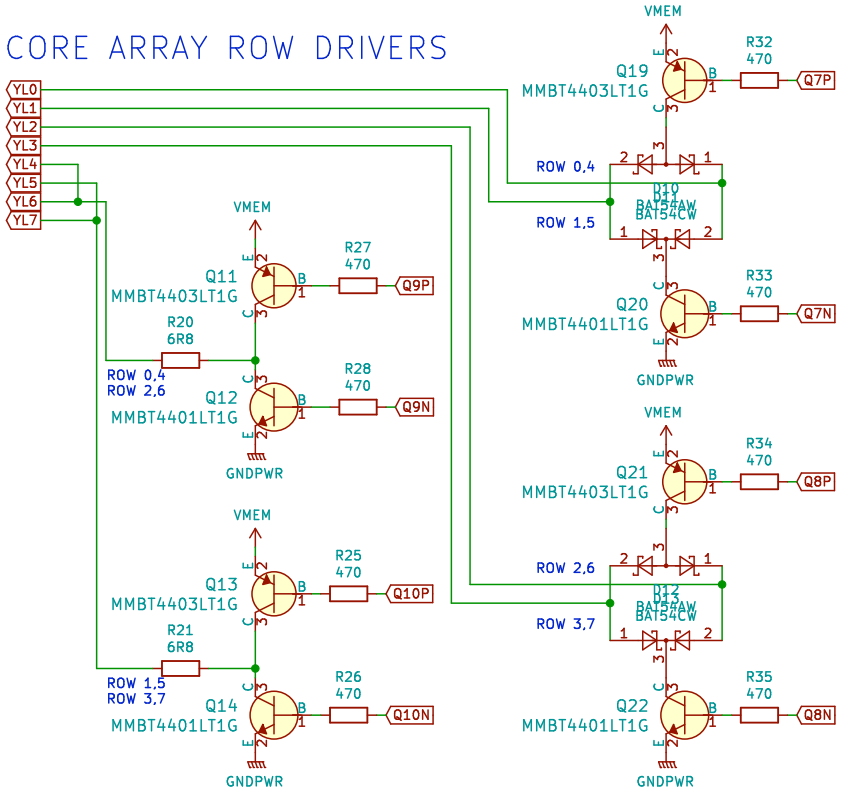
CORE ARRAY TOP COLUMN DRIVERS



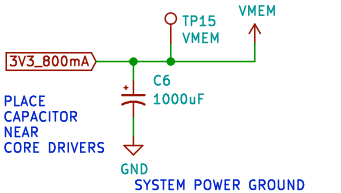
CORE ARRAY BOTTOM COLUMN DRIVERS



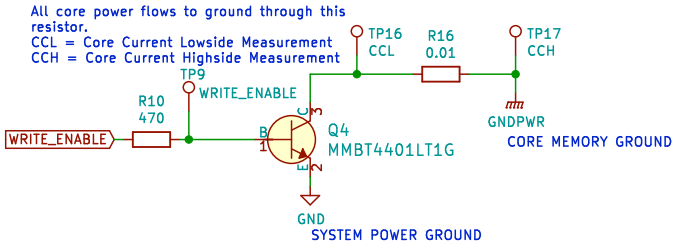
CORE ARRAY ROW DRIVERS



CORE ARRAY POWER



CORE ARRAY ENABLE



Drive Transistor current: 3.3/470=7mA (too much for Teensy LC)
Matrix 1/2 select current: 3.3/6.8= 485 mA (does not acccount for voltage drop in transistors)

Andy Geppert – Machine Ideas, LLC

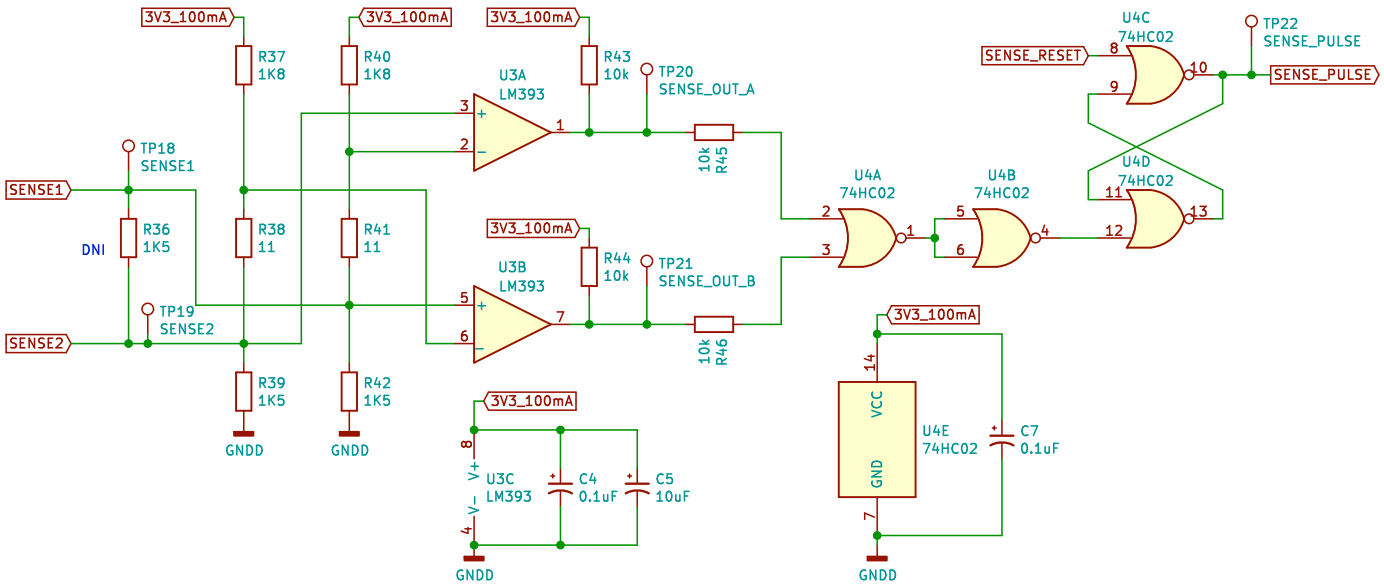
Sheet: /Core Array Driver/
File: Interactive Core Memory Badge (Logic) Driver v0.3.sch

Title: Core 64 – Core Array Driver

Size: A	Date: 2020-03-15	**Rev: 0.3**
KiCad E.D.A. eeschema (5.1.2-1)-1		Id: 4/6

SENSE SIGNAL PROCESSING

SENSE SIGNAL RS LATCH



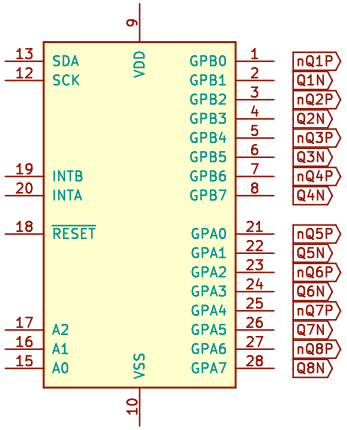
Andy Geppert – Machine Ideas, LLC	
Sheet: /SENSE/	
File: Interactive Core Memory Badge (Logic) Sense v0.3.sch	
Title: Core 64 – Sense	
Size: A4	Date: 2020-03-15
KiCad E.D.A. eeschema (5.1.2-1)-1	Id: 5/6

Rev: 0.3

IO EXPANSION

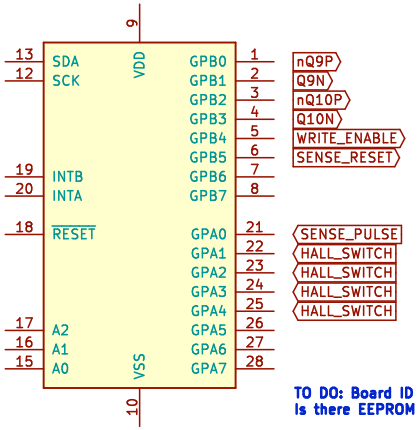
TO DO: I2C Address conflicts?

U5
MCP23017_SS



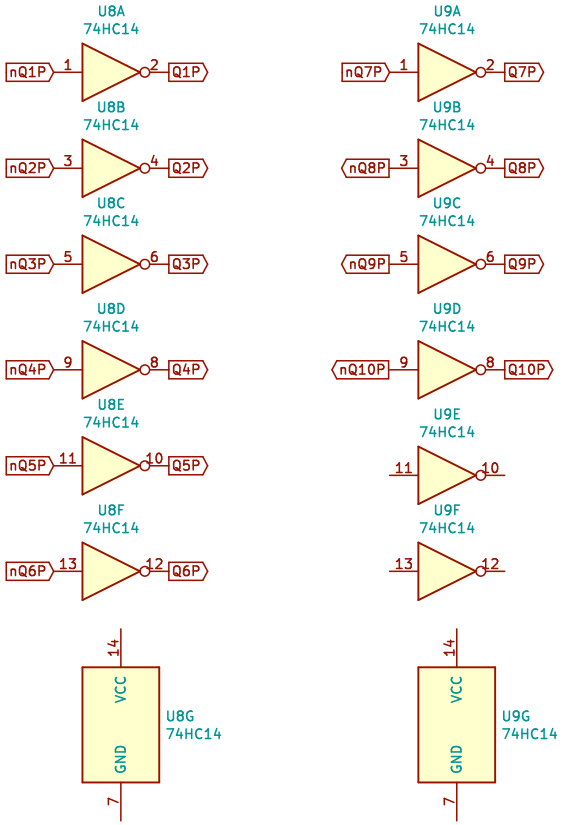
I2C ID: 0100xxx
I2C address range is 32 decimal to 37 decimal or 0x20 to 0x27.

U6
MCP23017_SS

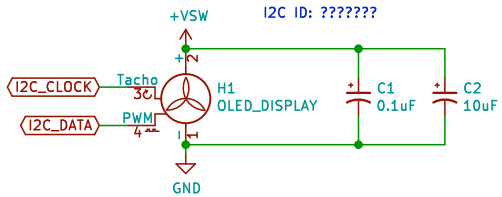


TO DO: Board ID pin setting?
Is there EEPROM setting in any of the I2C devices I'm using?

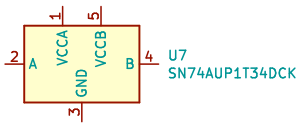
Invert PNP transistor drives



TO DO: Update this to be SAO, and some easy to add I2C OLED 4-pin header.



TO DO: Level shifter (74AHCT125 or 74HCT245) not required if using 3.7V.
or SN74LV1T34DCKR
Is it fast enough?



Sheet: /IO Expansion/
File: Interactive Core Memory Badge (Logic) IO Expansion V0.3.sch

Title: Core 64 – IO Expansion

Size: A4	Date: 2020-03-24	**Rev: v0.3**
KiCad E.D.A. eeschema (5.1.2-1)-1		Id: 6/6