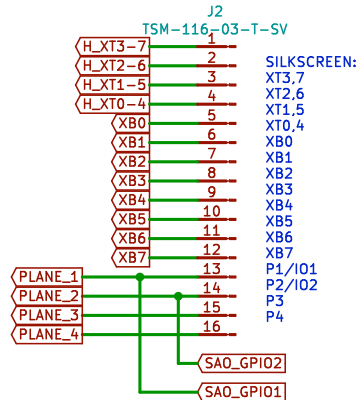
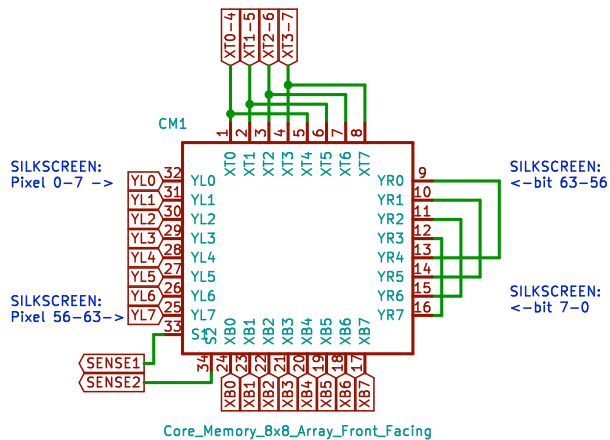


Pin 16 connection diagram for the TSM-03-T-SV module. The diagram shows a vertical column of 16 pins on the left, labeled J1, TSM-03-T-SV, and various signals. On the right, there are connections to H_YL0 through H_YL7, SENSE1, SENSE2, I2C_CLOCK, I2C_DATA, 3V3_800mA, and PLANE_8 through PLANE_5. A green line connects pin 16 to a common ground point labeled GND, DIGITAL, LOGIC, and GROUND.



3V3_800mA

I2C_DATA

I2C_CLOCK

SILKSCREEN: 0x30

SILKSCREEN: 0x31

SILKSCREEN: 0x32

SILKSCREEN: 0x33

U1
SI7210-B-01

SDA ALERT
GND GND
SCL VDD

C1
0.1uF

Ceramic

U2
SI7210-B-02

SDA ALERT
GND GND
SCL VDD

C2
0.1uF

Ceramic

U3
SI7210-B-03

SDA ALERT
GND GND
SCL VDD

C3
0.1uF

Ceramic

U4
SI7210-B-04

SDA ALERT
GND GND
SCL VDD

C4
0.1uF

Ceramic

GND

DIGITAL LOGIC GROUND

I2C configurable hall sensors, not just a switch.
Silicon Labs SI7210-B-01-IVR through 04-IVR
Low (push-pull) up to 20 mT, SOT23-5
<https://www.digikey.com/product-detail/en/silicon-labs/SI7210-B-04-IVR/336-4129-1-ND/7648844>

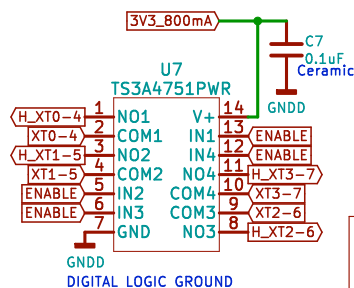
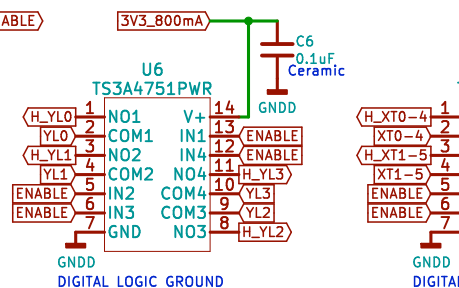
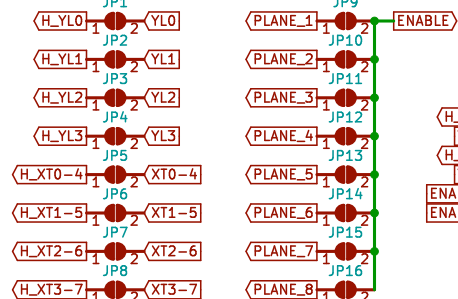
STEP 1: Solder all eight header-to-matrix SJs. JP1 through JP8.

STEP 2: Do NOT solder any JP9 through JP16.

STEP 3: No additional components needed.

STEP 4 (LOGIC BOARD): See instructions on Logic Board.

STEP 1: Do NOT solder any JP1 through JP8.	STEP 2: Solder ONE plane JP9 to JP16.	STEP 3: Install two quad switches and two decoupling caps.	STEP 4 (LOGIC BOARD): See instructions on Logic Board.
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SILKSCREEN: ALS I2C 0x29

U5

LTR-329ALS-01

3V3_800mA

C5 1uF Ceramic

GND

DIGITAL LOGIC GROUND

1 VDD

2 GND

3 SDA

4 SCL

I2C_CLOCK

I2C_DATA

Andy Geppert – Machine Ideas, LLC

Title: Core64 CB (Core Board)

Rev: 0.4

Id: 1/1

CORE BOARD V0.4 [REL. DATE]. ANDY GEPPERT
Core64.MachineIdeas.com
Interactive Core Memory

L1	L2
Core_64_Logo_9mm_tall	Core_64_M-+S_Buttons_4mm