CORE 64 INTERACTIVE CORE MEMORY BADGE VO.3 DUAL BOARD (LOGIC)

Sheet: Power

Sheet:	10	Expansion	

Sheet:	Core	Array	Driver			

Sheet	: SENSE			

File: Interactive Core Memory Badge (Logic) Power v0.3.sch

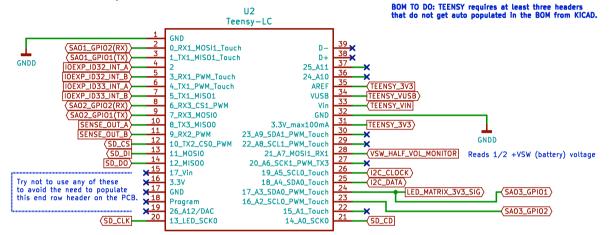
File: Interactive Core Memory Badge (Logic) 10 Expansion V0.3.sch

File: Interactive Core Memory Badge (Logic) Driver v0.3.sch

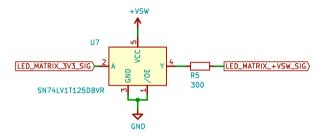
File: Interactive Core Memory Badge (Logic) Sense v0.3.sch

TEENSY MCU CONNECTIONS

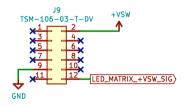
Teensy LC has incoming USB power/programming on board. *** CUT THE USB-VIN bridge. ***



LED ARRAY DRIVE LEVEL SHIFT

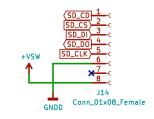


PARTIAL RASPI HEADER FOR LED ARRAY



MicroSD Card (OPTIONAL)

Suggested: https://www.adafruit.com/product/254



Andy Geppert - Machine Ideas, LLC

Sheet: /

File: Interactive Core Memory Badge (Logic) Main v0.3.sch

Title: Core 64 - Main Sheet Index

 Size: A4
 Date: 2020-04-24
 Rev: 0.3

 KiCad E.D.A. eeschema (5.1.2-1)-1
 Id: 1/5

I2C ADDRESS TABLE

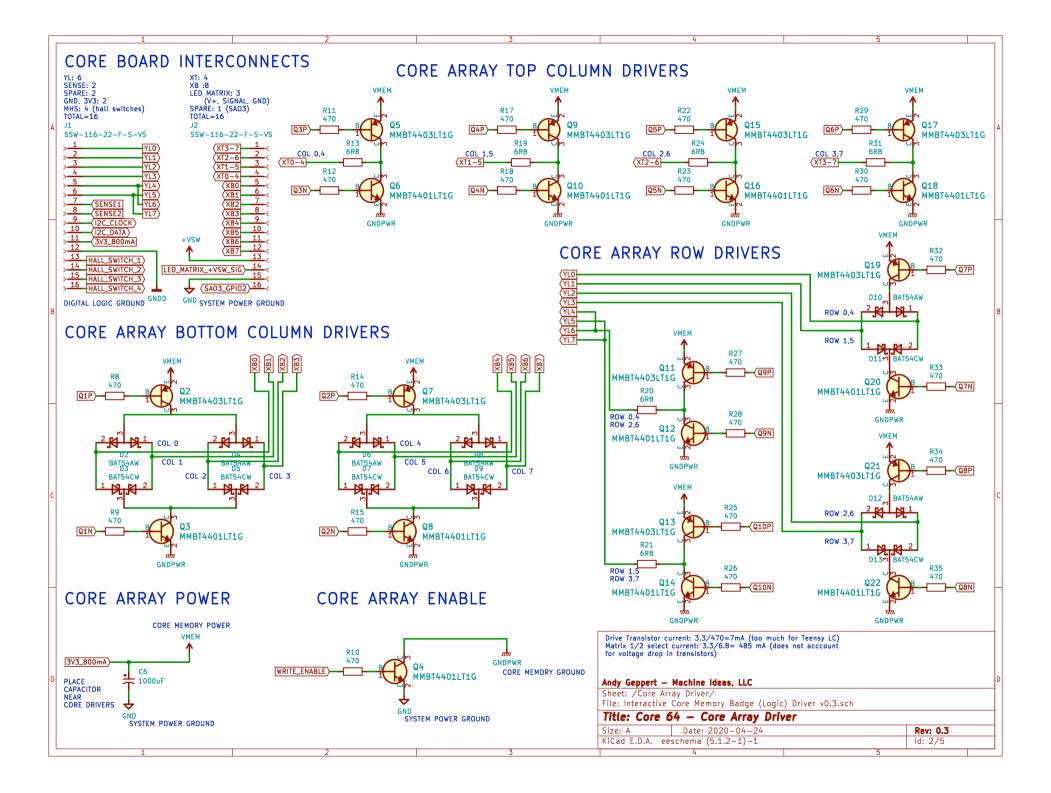
Required
IO EXPANDER 1: 0x26 (38 decimal)
IO EXPANDER 2: 0x27 (39 decimal)
HALL SENSOR 1: 0x30 (48 decimal)
HALL SENSOR 2: 0x31 (49 decimal)

HALL SENSOR 1: 0x30 (48 decimal)
HALL SENSOR 2: 0x31 (49 decimal)
HALL SENSOR 3: 0x32 (50 decimal)
HALL SENSOR 4: 0x33 (51 decimal)
EEPROM: 0b1010111, 0x57 (87 decimal)

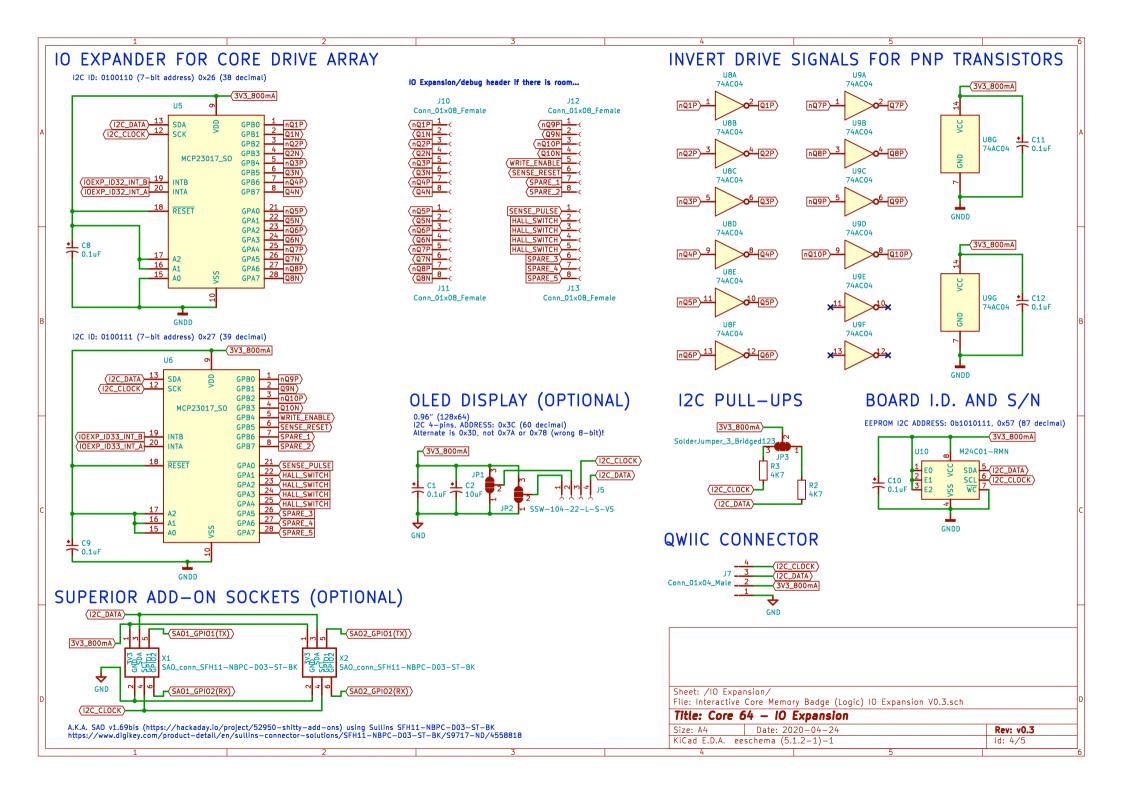
Optional
OLED: 0x3C (60 decimal)

OLED: 0x3C (60 decimal) ANDIXOR GPIO Expander MCP23017 0x20 (32 decimal) ANDIXOR EEPROM AT24C32r 0x50 (80 decimal)

All 7-bit addresses should be greater than 0x07 and less than 0x78 (120).

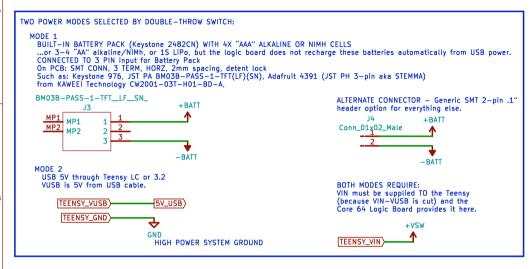


SENSE SIGNAL PROCESSING SENSE SIGNAL RS LATCH 3V3_800mA SENSE_RESET R37 R40 R43 10k 1K8 1K8 U3A SENSE_PULSE LM393 SENSE_OUT_A 10k R45 U4A U4B 74HC02 SENSE1> 74HC02 R36 1K5 R38 11 R41 11 10k DNI U3B SENSE_OUT_B LM393 3V3_800mA SENSE2 10k R46 R42 1K5 R39 3V3_800mA 1K5 U4E C7 74HC02 0.1uF GNDD ⁻ U3C GNDD GNDD SENSE DEBUG SOCKET GNDD SENSE1 3 SENSE1 5 J6
SENSE_OUT_A 6 Conn_01x08_Female
SENSE_RESET 7
SENSE_PULSE 8 Andy Geppert - Machine Ideas, LLC Sheet: /SENSE/ File: Interactive Core Memory Badge (Logic) Sense v0.3.sch Title: Core 64 - Sense Size: A4 Date: 2020-04-24 Rev: 0.3 KiCad E.D.A. eeschema (5.1.2-1)-1ld: 3/5



TEENSY LC OR 3.2 AND ALKALINE/NIMH BATTERY PACK *** MUST CUT VIN-VUSB TRACE ON TEENSY *** THIS IS THE STANDARD MANUFACTURED KIT CONFIGURATION

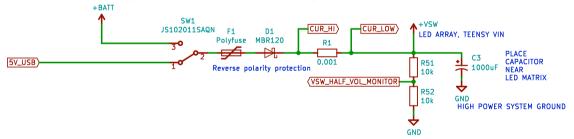
HACKER POWER OPTION: ADAFRUIT FEATHER WITH REQUIRED LIPO *** MUST REMOVE ALKALINE/NIMH BATTERY PACK *** USER MODIFICATION REQUIRED



A) REPLACE THE ALKALINE/NIMH BATTERY PACK WITH 1S LIPO IN THE SAME POWER PORT, OR THE ALTERNATE PORT.

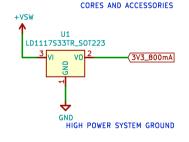
B) REMOVE THE ALKALINE/NIMH BATTERY PACK AND CONNECT 1S LIPO DIRECTLY TO FEATHER JST-PH BATTERY/CHARGING PORT.

POWER SWITCH, POWER PROTECTION, VOLTAGE & CURRENT MONITOR

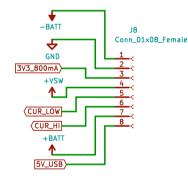


3.3V POWER SUPPLY

HACKER UPGRADE TO USE FEATHER-TEENSY ADAPTER BOARD REQUIRES:



POWER RAILS



REVERSE POLARITY **PROTECTION**

ALL SYSTEM STAR GROUNDING



REVERSE POLARITY DETECTION AND SYSTEM CURRENT MEASUREMENT CLOSE TO BATTERY.

REF: https://www.instructables.com/id/Reverse-polarity-protection-for-your-circuit-with/ IRLML6344TRPBF https://www.digikey.com/product-detail/en/infineon-technologies/IRLML6344TRPBF/IRLML6344TRPBFCT-ND/2538168 Andy Geppert - Machine Ideas, LLC

Sheet: /Power/

File: Interactive Core Memory Badge (Logic) Power v0.3.sch

Title: Core 64 - Power Schematic

Date: 2020-04-24 Size: A4 Rev: 0.3 KiCad E.D.A. eeschema (5.1.2-1)-1ld: 5/5