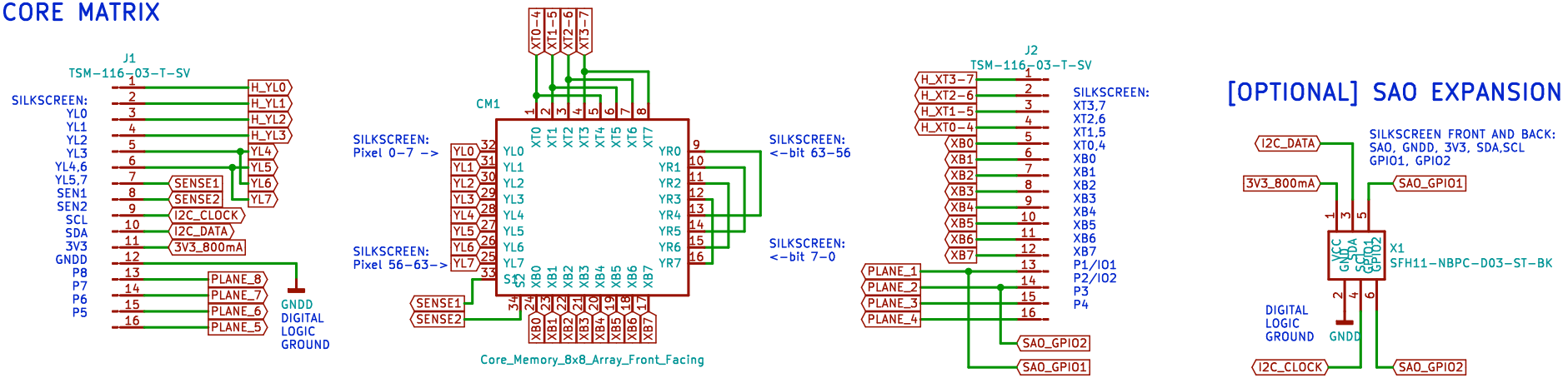
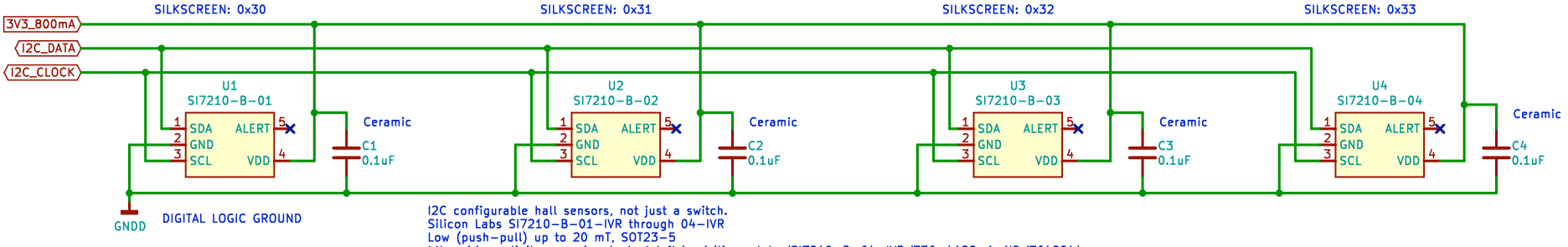
CORE MATRIX



[OPTIONAL] SAO EXPANSION

HALL SENSORS



I2C configurable hall sensors, not just a switch.
Silicon Labs SI7210-B-01-IVR through 04-IVR
Low (push-pull) up to 20 mT, SOT23-5
https://www.digikey.com/product-detail/en/silicon-labs/SI7210-B-04-IVR/336-4129-1-ND/7648844

DEFAULT FOR ONE CORE PLANE ONLY

STEP 1: Solder all eight header-to-matrix SJs. JP1 through JP8.

STEP 2: Do NOT solder any JP9 through JP16.

STEP 3: No additional components needed.

STEP 4 (LOGIC BOARD): See instructions on Logic Board.

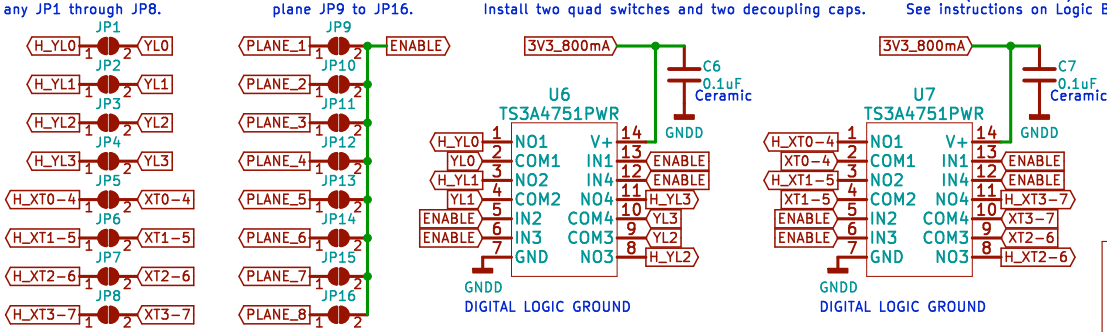
[OPTIONAL] CORE PLANE SELECT

STEP 1: Do NOT solder any JP1 through JP8.

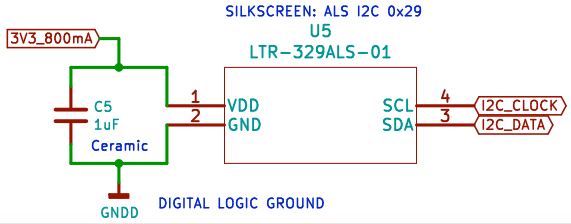
STEP 2: Solder ONE plane JP9 to JP16.

STEP 3: Install two quad switches and two decoupling caps.

STEP 4 (LOGIC BOARD): See instructions on Logic Board.



AUTOMATIC LIGHT SENSOR I2C 0x29



SILKSCREEN MISC.

CORE BOARD V0.4 [REL. DATE]. ANDY GEPPERT
Core64.MachineIdeas.com
Interactive Core Memory

SILKSCREEN GRAPHICS

L1
Core_64_Logo_9mm_tall

L2
Core_64_M-+S_Buttons_4mm

AS PROTOTYPED 22AUG2020

Andy Geppert – Machine Ideas, LLC

Sheet: /
File: Core64 CB v0.4.sch

Title: Core64 CB (Core Board)

Size: A	Date: 2020-08-22	**Rev: 0.4**
KiCad E.D.A. eeschema (5.1.2-1)-1		Id: 1/1