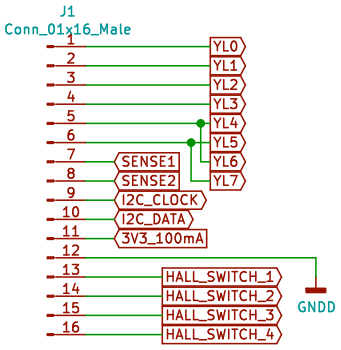
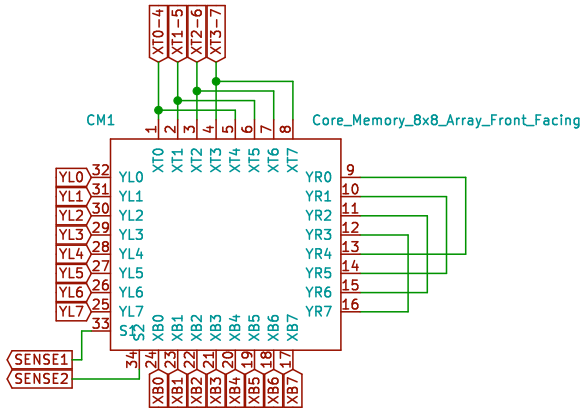
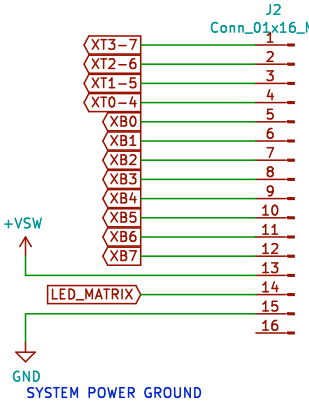
Orientation of core array is the user view.
The user view is the FRONT COPPER of the PCB where only the core array is installed.
The other side of the board is the BACK COPPER PCB where all other compnents are populated, out of sight of the user.
The PCB layout is viewed from the FRONT COPPER PCB side.

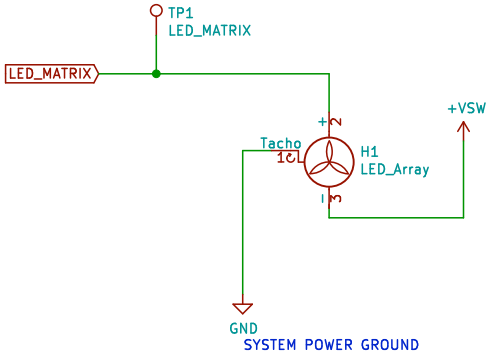
YL: 6
SENSE: 2
I2C: 2
GND, 3V3: 2
MHS: 4 (hall switches)
TOTAL=16

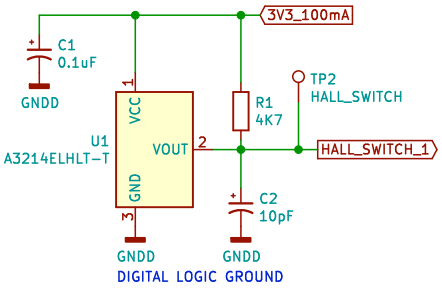


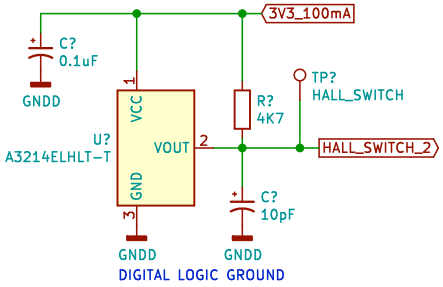


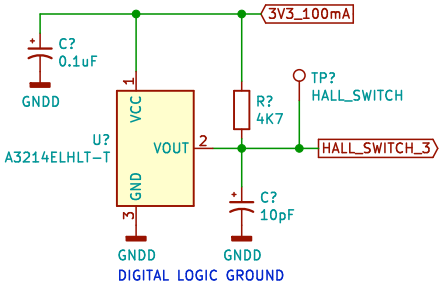
XT: 4
XB :8
LED MATRIX: 3
(V+, SIGNAL, GND)
SPARE: 1
TOTAL=16

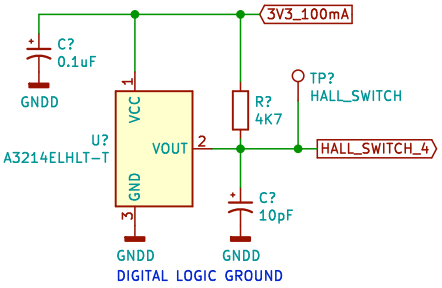












v0.1 used hall sensor Allegro A3214ELHLT-T, Omnipolar N/S, ±7mT trip, ±1mT release SOT23W
https://www.digikey.com/product-detail/en/allegro-microsystems/A3214ELHLT-T/620-1519-1-ND/4171832

TO DO: Read app note for layout, verify pads, circuit config for push-pull.
v0.3 Try more sensitive option, TI DRV5032FADBZR Omni 4.8mT, 20Hz, Push-Pull output, SOT23-3
https://www.digikey.com/product-detail/en/texas-instruments/DRV5032FADBZR/296-47765-1-ND/8133114
-OR-
DRV5032DU, ±1.2mT Trip, ±3.5mT Release, Unipolar, Push-pull, 20 Hz
https://www.digikey.com/product-detail/en/texas-instruments/DRV5032DUDBZR/296-DRV5032DUDBZRCT-ND/10435200

TO DO: ADD I2C options for testing.
Silicon Labs SI7210-B-04-IVR (configurable with 4 addresses, 0x30 up to 0x33 as P/N SI7210-B-01- IV(R) through SI7210-B-04- IV(R)
Low (push-pull) up to 20 mT, SOT23-5
https://www.digikey.com/product-detail/en/silicon-labs/SI7210-B-04-IVR/336-4129-1-ND/7648844

NOTES:

Andy Geppert – Machine Ideas, LLC

Sheet: /
File: Interactive Core Memory Badge (Cores) v0.3.sch

Title: Core 64 – Interactive Core Memory Badge (Cores)

Size: A	Date: 2020-03-15	**Rev: 0.3**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 1/1