

# CORE 64 INTERACTIVE CORE MEMORY BADGE V0.3 DUAL BOARD (LOGIC)

Sheet: Power

File: Interactive Core Memory Badge (Logic) Power v0.3.sch

Sheet: IO Expansion

File: Interactive Core Memory Badge (Logic) IO Expansion V0.3.sch

Sheet: Core Array Driver

File: Interactive Core Memory Badge (Logic) Driver v0.3.sch

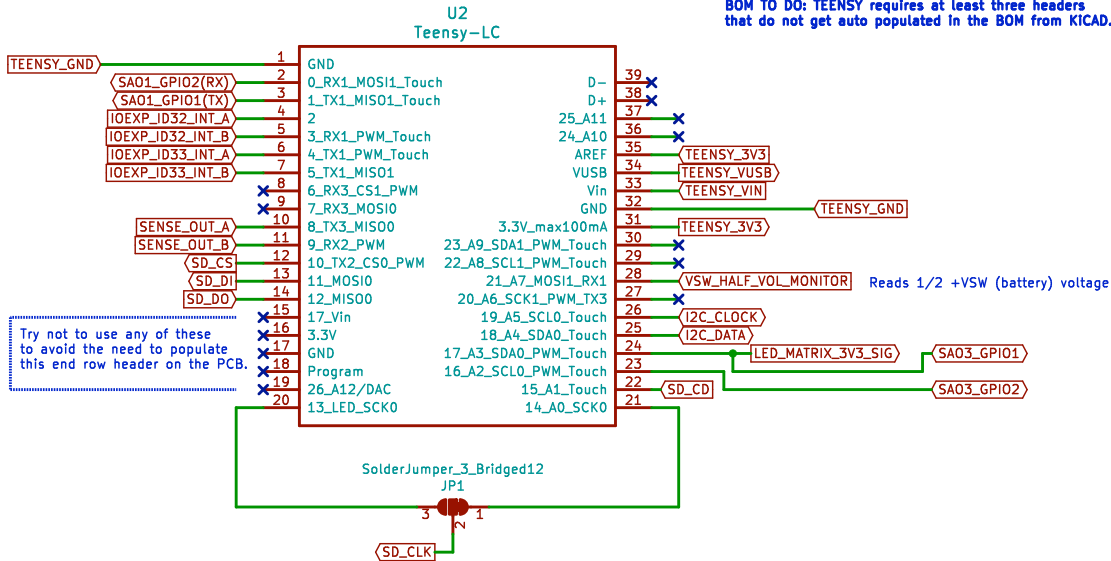
Sheet: SENSE

File: Interactive Core Memory Badge (Logic) Sense v0.3.sch

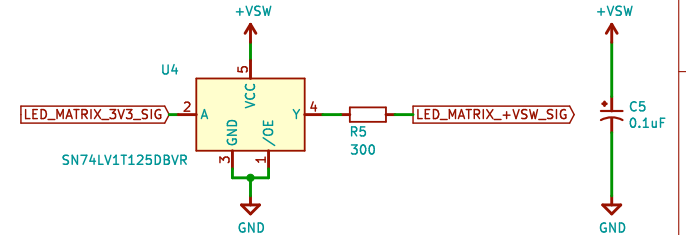
## TEENSY MCU CONNECTIONS

Teensy LC has incoming USB power/programming on board.  
\*\*\* CUT THE USB-VIN bridge. \*\*\*

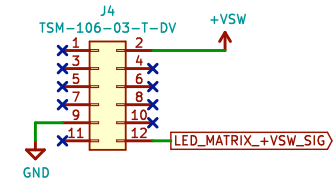
BOM TO DO: TEENSY requires at least three headers that do not get auto populated in the BOM from KICAD.



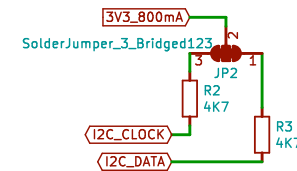
## LED ARRAY DRIVE LEVEL SHIFT



## LED ARRAY (PARTIAL RASPI HEADER)

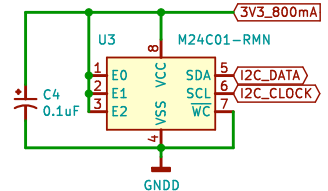


## I2C PULL-UPS



## BOARD I.D. AND S/N

EEPROM I2C ADDRESS: 0b1010111, 0x57 (87 decimal)



### I2C ADDRESS TABLE

Required

IO EXPANDER 1: 0x26 (38 decimal)  
IO EXPANDER 2: 0x27 (39 decimal)  
HALL SENSOR 1: 0x30 (48 decimal)  
HALL SENSOR 2: 0x31 (49 decimal)  
HALL SENSOR 3: 0x32 (50 decimal)  
HALL SENSOR 4: 0x33 (51 decimal)  
EEPROM: 0b1010111, 0x57 (87 decimal)

Optional

OLED: 0x3C (60 decimal)  
ANDIXOR GPIO Expander MCP23017 0x20 (32 decimal)  
ANDIXOR EEPROM AT24C32r 0x50 (80 decimal)

All 7-bit addresses should be greater than 0x07 and less than 0x78 (120).

L4  
Core\_64\_Github\_Link

L3  
Core\_64\_Github\_Link

L2  
Core\_64\_Logo

L1  
Core\_64\_Logo

As prototyped 2020-05-18

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Sheet: /  
File: Interactive Core Memory Badge (Logic) Main v0.3.sch

Title: Core 64 - Main Sheet Index

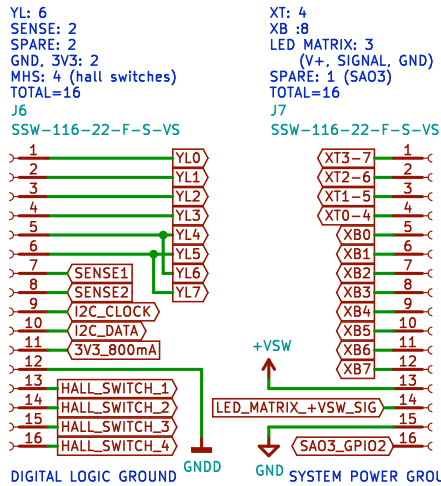
Size: A4 Date: 2020-05-18

KICad E.D.A. eeschema (5.1.2-1)-1

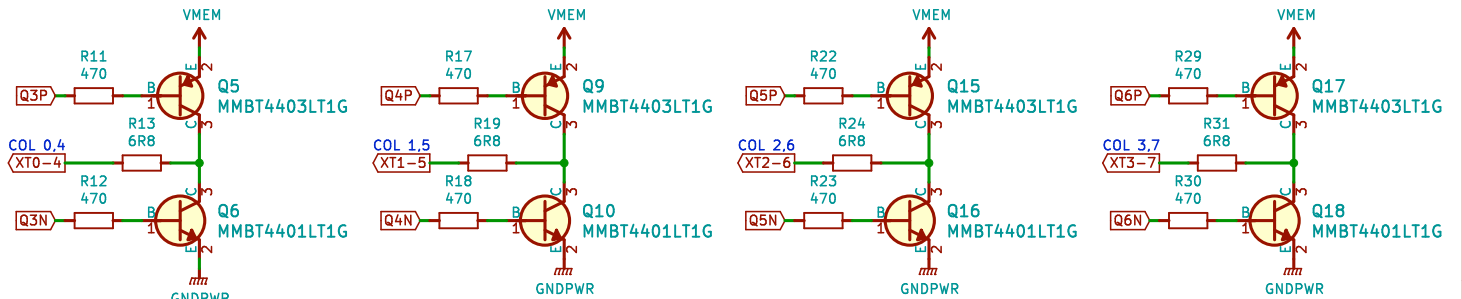
Rev: 0.3

Id: 1/5

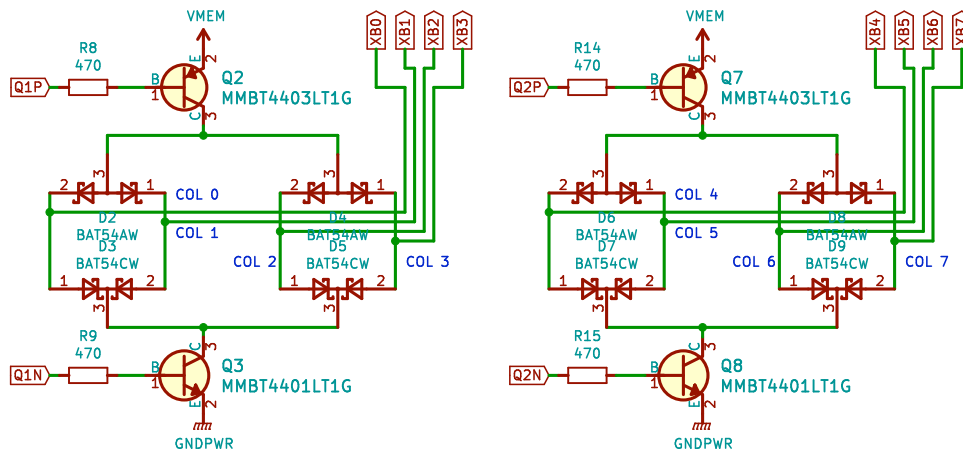
## CORE BOARD INTERCONNECTS



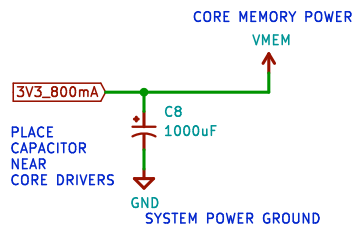
## CORE ARRAY TOP COLUMN DRIVERS



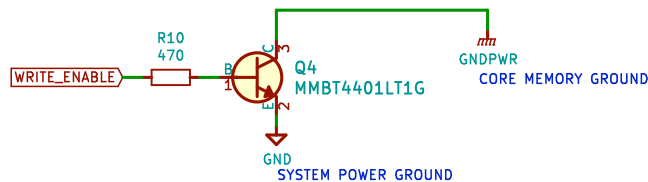
## CORE ARRAY BOTTOM COLUMN DRIVERS



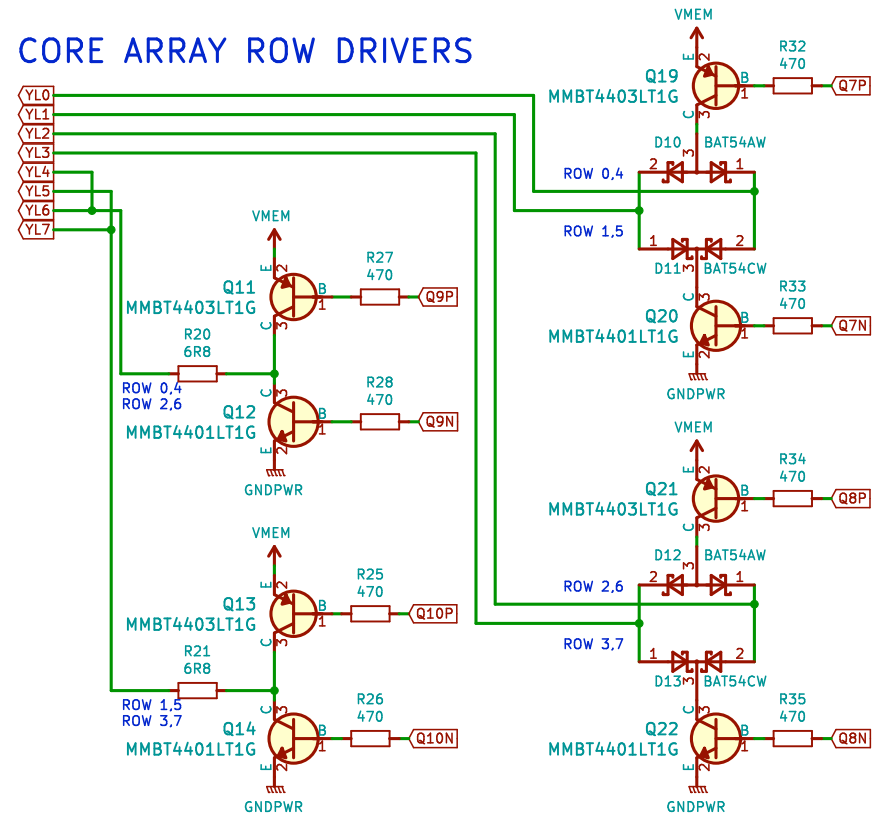
## CORE ARRAY POWER



## CORE ARRAY ENABLE



## CORE ARRAY ROW DRIVERS



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Drive Transistor current: 3.3/470=7mA (too much for Teensy LC)  
Matrix 1/2 select current: 3.3/6.8= 485 mA (does not account for voltage drop in transistors)

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Sheet: /Core Array Driver/

File: Interactive Core Memory Badge (Logic) Driver v0.3.sch

**Title: Core 64 - Core Array Driver**

Size: A Date: 2020-05-18

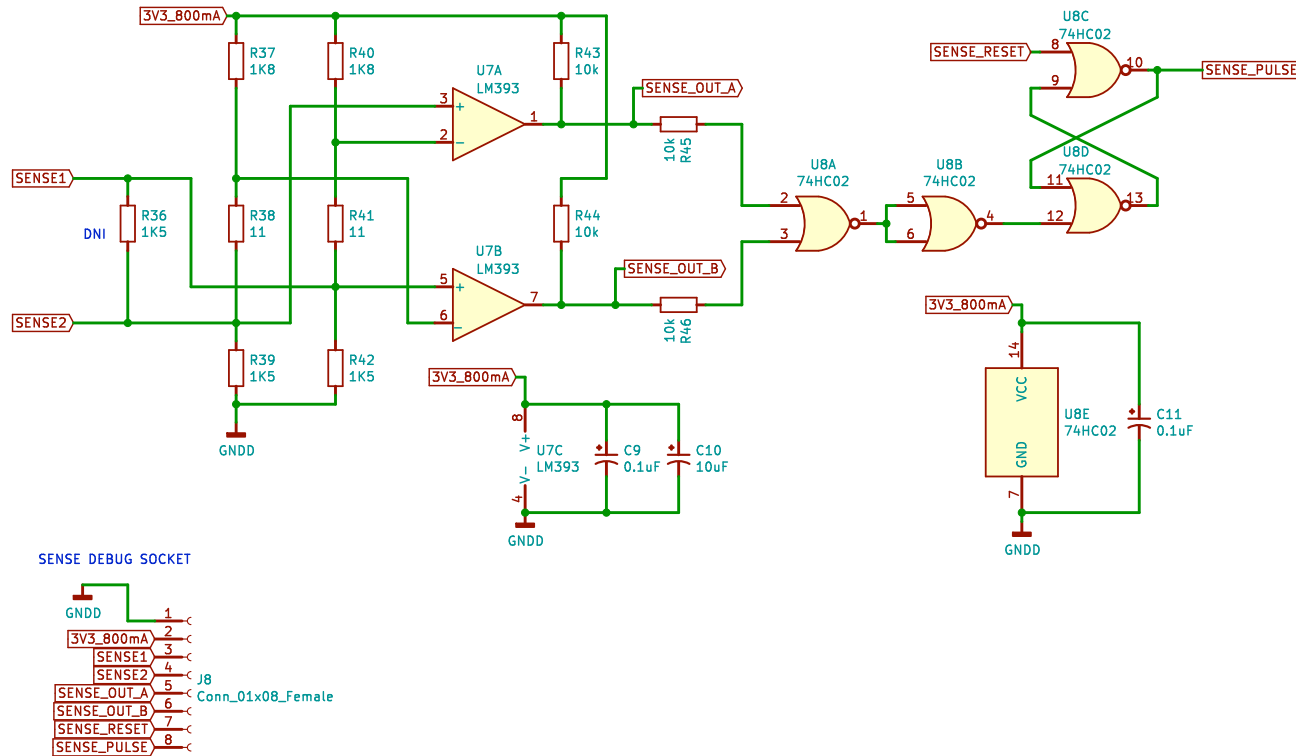
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Rev: 0.3

Id: 2/5

## SENSE SIGNAL PROCESSING

## SENSE SIGNAL RS LATCH



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Sheet: /SENSE/

File: Interactive Core Memory Badge (Logic) Sense v0.3.sch

**Title: Core 64 – Sense**

Size: A4

Date: 2020-05-18

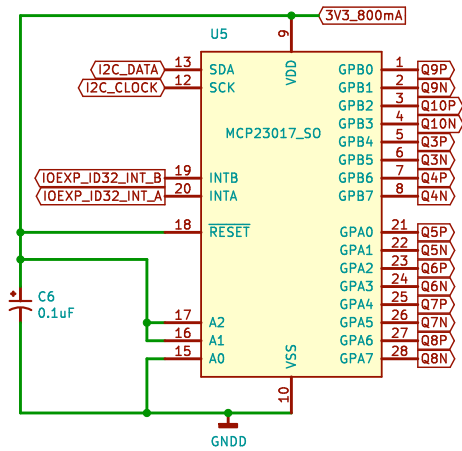
**Rev: 0.3**

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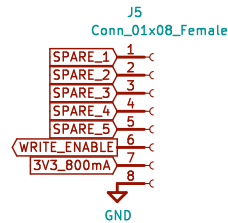
Id: 3/5

## IO EXPANDER FOR CORE DRIVE ARRAY

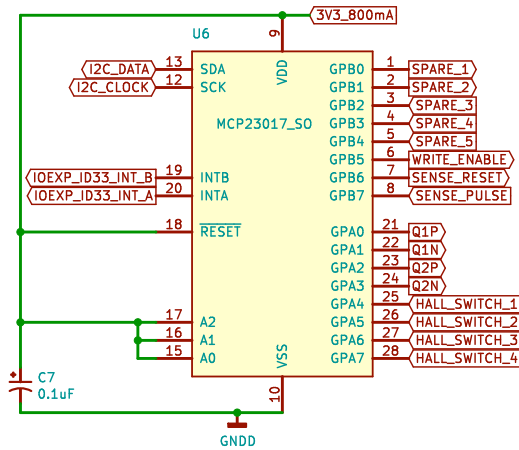
I2C ID: 0100110 (7-bit address) 0x26 (38 decimal)



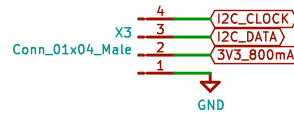
IO Expansion header



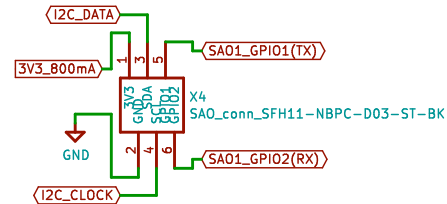
I2C ID: 0100111 (7-bit address) 0x27 (39 decimal)



### QWIIC (OPTIONAL)



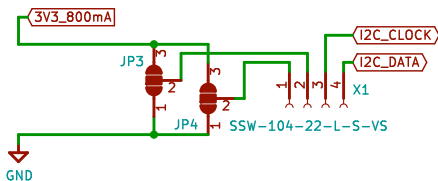
### SUPERIOR ADD-ON SOCKET (OPTIONAL)



SA0 v1.69bis (<https://hackaday.io/project/52950-shitty-add-ons>) using Sullins SFH11-NBPC-D03-ST-BK female header <https://www.digikey.com/product-detail/en/sullins-connector-solutions/SFH11-NBPC-D03-ST-BK/S9717-ND/4558818>

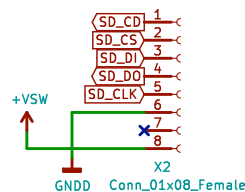
### OLED DISPLAY (OPTIONAL)

0.96" (128x64)  
I2C 4-pins, ADDRESS: 0x3C (60 decimal)  
Alternate is 0x3D, not 0x7A or 0x78 (wrong 8-bit)!



### MICRO SD CARD (OPTIONAL)

Suggested: <https://www.adafruit.com/product/254>



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Sheet: /IO Expansion/  
File: Interactive Core Memory Badge (Logic) IO Expansion V0.3.sch

**Title: Core 64 - IO Expansion**

Size: A4

Date: 2020-05-18

Rev: v0.3

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Id: 4/5

# TEENSY LC OR 3.2 AND ALKALINE/NIMH BATTERY PACK

\*\*\* MUST CUT VIN-VUSB TRACE ON TEENSY \*\*\*

## THIS IS THE STANDARD MANUFACTURED KIT CONFIGURATION

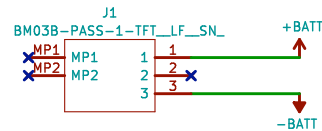
# HACKER POWER OPTION: ADAFRUIT FEATHER WITH REQUIRED LIPO

\*\*\* MUST REMOVE ALKALINE/NIMH BATTERY PACK \*\*\*

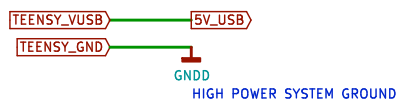
## USER MODIFICATION REQUIRED

### TWO POWER MODES SELECTED BY DOUBLE-THROW SWITCH:

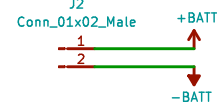
**MODE 1**  
BUILT-IN BATTERY PACK (Keystone 24B2CN) WITH 4X "AAA" ALKALINE OR NIMH CELLS  
...or 3-4 "AA" alkaline/NiMH, or 1S LiPo, but the logic board does not recharge these batteries automatically from USB power.  
CONNECTED TO 3 PIN input for Battery Pack  
On PCB: SMT CONN, 3 TERM, HORZ, 2mm spacing, detent lock  
Such as: Keystone 976, JST PA BM03B-PASS-1-TFT(LF)(SN), Adafruit 4391 (JST PH 3-pin aka STEMMA)  
from KAWEEI Technology CW2001-03T-H01-BD-A,



**MODE 2**  
USB 5V through Teensy LC or 3.2  
VUSB is 5V from USB cable.



ALTERNATE CONNECTOR - Generic SMT 2-pin .1" header option for everything else.



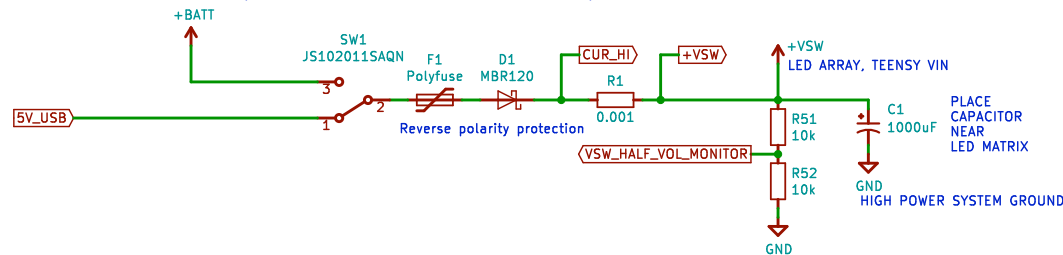
BOTH MODES REQUIRE:  
VIN must be supplied to the Teensy  
(because VIN-VUSB is cut) and the  
Core 64 Logic Board provides it here.



### HACKER UPGRADE TO USE FEATHER-TEENSY ADAPTER BOARD REQUIRES:

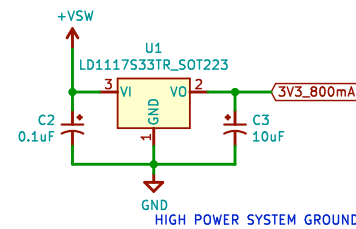
- REPLACE THE ALKALINE/NIMH BATTERY PACK WITH 1S LIPO IN THE SAME POWER PORT, OR THE ALTERNATE PORT.
- REMOVE THE ALKALINE/NIMH BATTERY PACK AND CONNECT 1S LIPO DIRECTLY TO FEATHER JST-PH BATTERY/CHARGING PORT.

## POWER SWITCH, POWER PROTECTION, VOLTAGE & CURRENT MONITOR

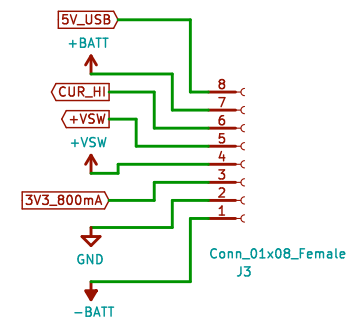


## 3.3V POWER SUPPLY

CORES AND ACCESSORIES



## POWER RAILS



## REVERSE POLARITY PROTECTION

## ALL SYSTEM STAR GROUNDING

**TO DO: Choose BIG CAP footprint**



REVERSE POLARITY DETECTION AND SYSTEM  
CURRENT MEASUREMENT CLOSE TO BATTERY.

REF: <https://www.instructables.com/id/Reverse-polarity-protection-for-your-circuit-with-IRLML6344TRPBF> <https://www.digikey.com/product-detail/en/infinion-technologies/IRLML6344TRPBF/IRLML6344TRPBFCT-ND/2538168>

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Sheet: /Power/

File: Interactive Core Memory Badge (Logic) Power v0.3.sch

**Title: Core 64 - Power Schematic**

Size: A4

Date: 2020-05-18

Rev: 0.3

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