

CORE 64 INTERACTIVE CORE MEMORY BADGE V0.4 LOGIC BOARD

Sheet: Power

Sheet: Driver

Sheet: Sense_LEDs_ID

Sheet: Expansion

File: Core64 LB v0.4 Power.sch

File: Core64 LB v0.4 Driver.sch

File: Core64 LB v0.4 Sense_LEDs_ID.sch

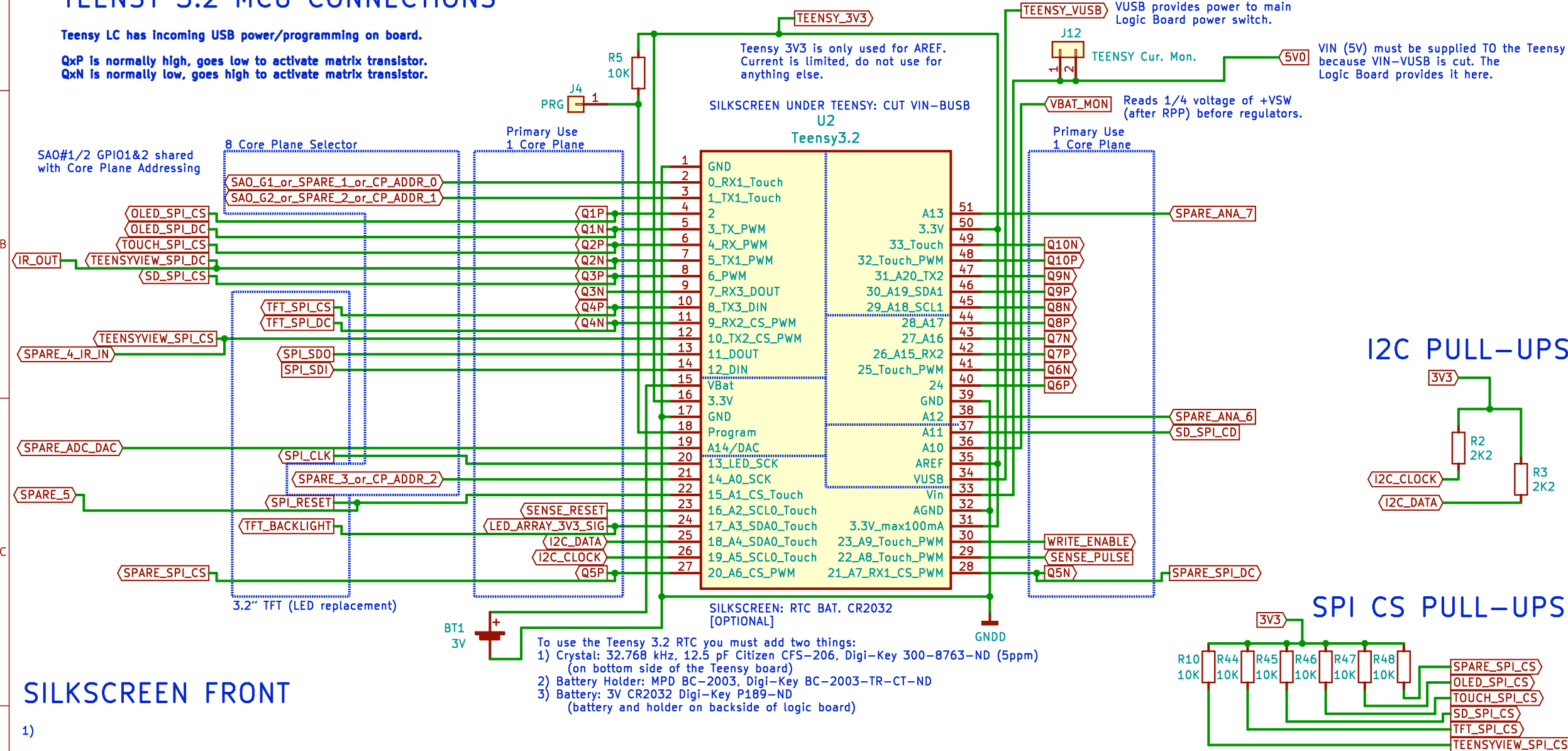
File: Core64 LB v0.4 Expansion.sch

*** CUT THE USB-VIN bridge on TEENSY 3.2 ***

TEENSY 3.2 MCU CONNECTIONS

Teensy LC has Incoming USB power/programming on board.

QxP is normally high, goes low to activate matrix transistor.
QxN is normally low, goes high to activate matrix transistor.



SILKSCREEN FRONT

1)

SILKSCREEN BACK

- 1) Serial Number Sticker Zone
- 2) Board name, version, date, Machine Ideas

BOM TO DO: TEENSY requires at least three headers that do not get auto populated in the BOM from KICAD.

SILKSCREEN GRAPHICS

- L3
Core_64_Github_Link
- L2
Core_64_Logo
- L1
Core_64_Logo

All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

Andy Geppert – Machine Ideas, LLC

Sheet: /
File: Core64 LB v0.4.sch

Title: Core 64 – Main Sheet Index

Size: A Date: 2020-08-27

Rev: 0.4

KiCad E.D.A. kicad (5.1.2-1)-1

Id: 1/5

J1 SSW-116-22-F-S-V5

J5 SSW-116-22-F-S-V5

1 YL0 XT3,7 1

2 YL1 XT2,6 2

3 YL2 XT1,5 3

4 YL3 XT0,4 4

5 YL4 XB0 5

6 YL5 XB1 6

7 YL6 XB2 7

8 SENSE1 YL7 8

9 SENSE2 9

10 I2C_CLOCK XB3 10

11 I2C_DATA XB4 11

12 3V3 XB5 12

13 CP8_EN XB6 13

14 CP7_EN XB7 14

15 CP6_EN CP1_EN 15

16 CP5_EN CP2_EN 16

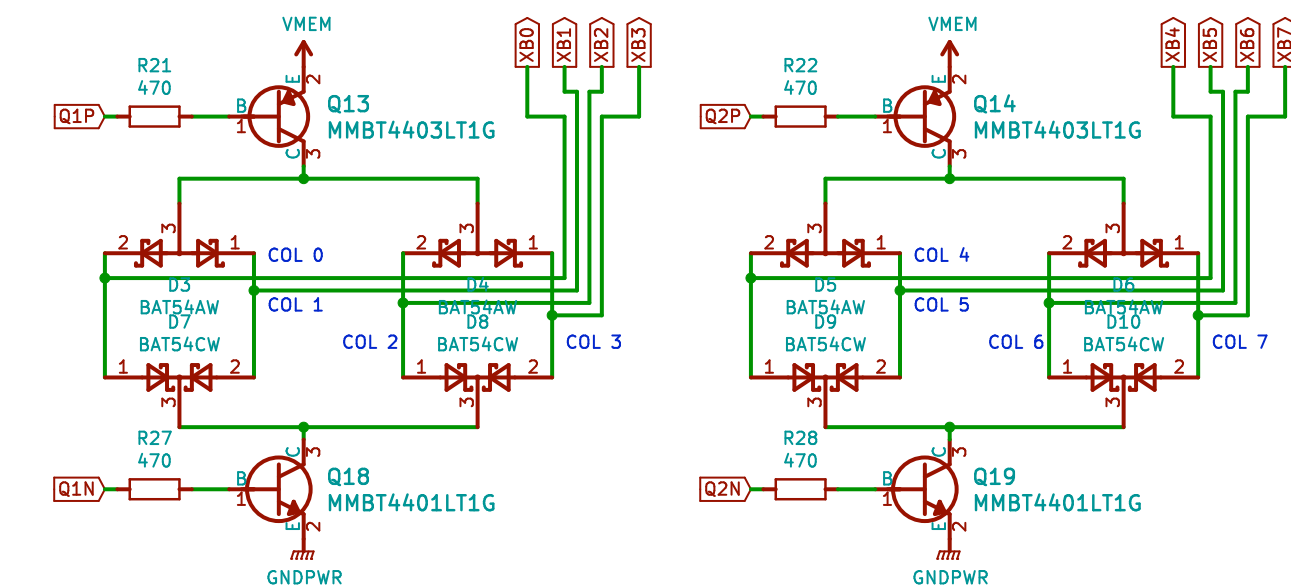
CP3_EN

CP4_EN

Silkscreen: 3V3 ONLY

GND

DIGITAL LOGIC GROUND



Core Cur. Mon. J13

CORE MEMORY POWER

VMEM

3V3

C1 470uF

GND

SYSTEM POWER GROUND

All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

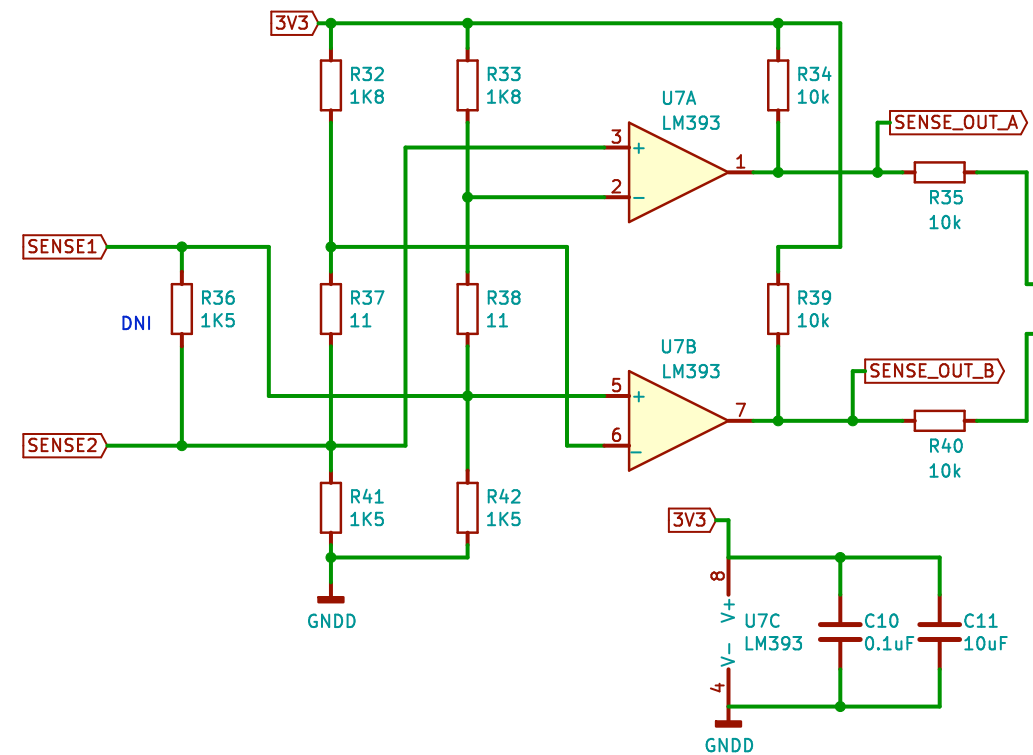
Drive Transistor current: $3.3/470=7\text{mA}$ (too much for Teensy LC)
Matrix 1/2 select current: $3.3/6.8= 485\text{ mA}$ (does not account for voltage drop in transistors)

Sheet: /Driver/
File: Core64 LB v0.4 Driver.sch

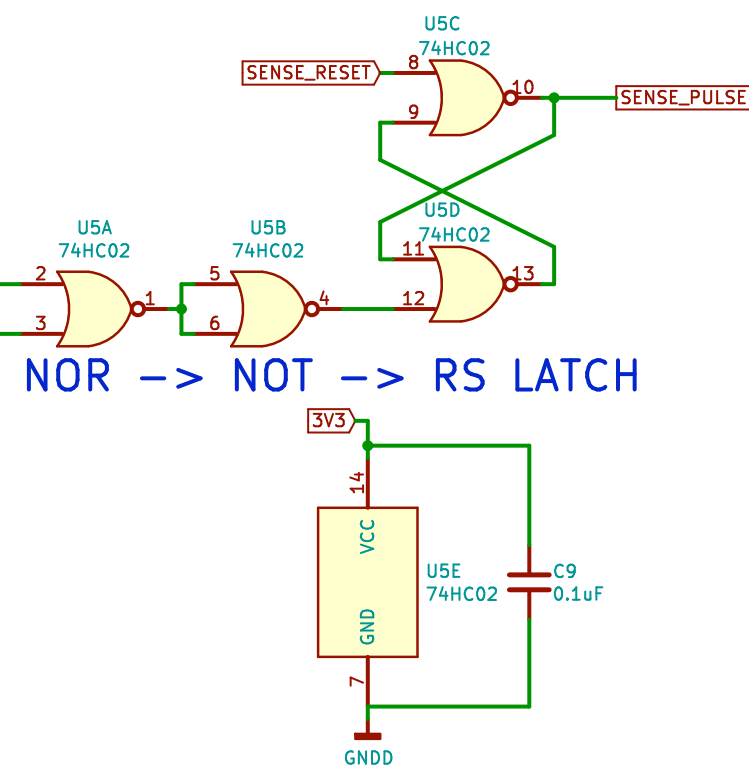
Size: A	Date: 2020-08-27
KiCad E.D.A. kicad (5.1.2-1)-1	

Rev: 0.4
Id: 2/5

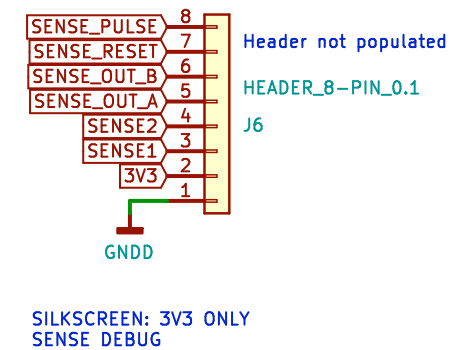
SENSE SIGNAL DIFFERENTIAL AMPLIFIERS



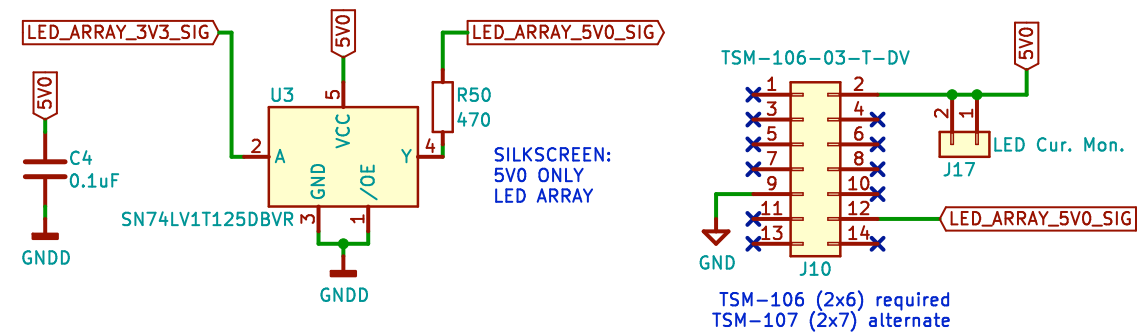
SENSE SIGNAL LATCH



SENSE DEBUG

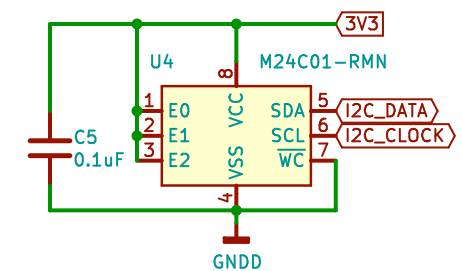


LED ARRAY DRIVE AND LEVEL SHIFT



BOARD ID AND S/N

EEPROM I2C ADDRESS: 0b1010111, 0x57 (87)



All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

Andy Geppert – Machine Ideas, LLC

Sheet: /Sense_LEDs_ID/

File: Core64 LB v0.4 Sense_LEDs_ID.sch

Title: Core 64 – Sense

Size: A	Date: 2020-08-27
---------	------------------

Size: A	Date: 2020-0
KiCad E.D.A.	kicad (5.1.2-1)-1

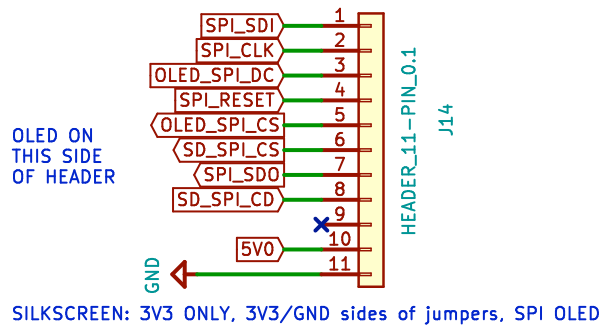
Rev: 0.4

Id: 3/5

EVERYTHING ON THIS SHEET IS USER-PROVIDED OPTIONAL ADD-ONS

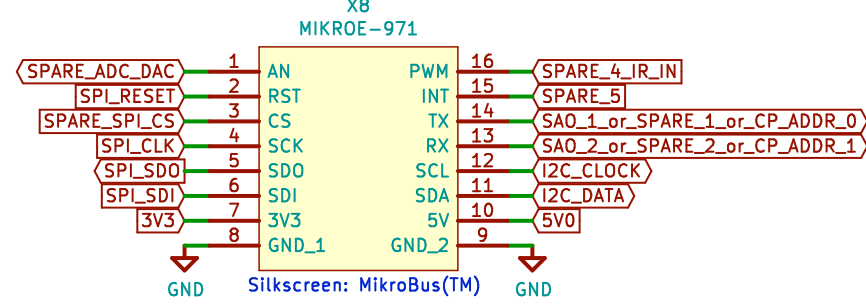
OLED COLOR SPI w/MicroSD

Compatible: <https://www.adafruit.com/product/1431>
1.5" 128x128, 16-bit color w/MicroSD holder
MicroSD card standalone pins shared between TFT and OLED boards.



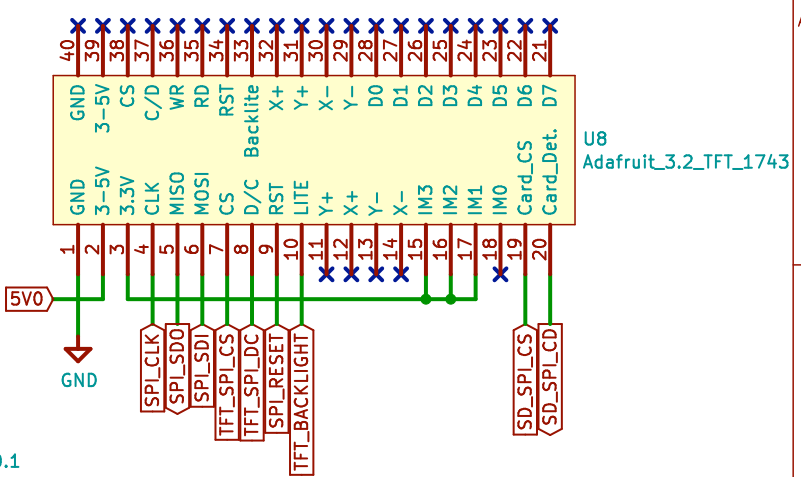
MIKRO BUS

See specifications: <https://www.mikroe.com/mikrobus>
8-pin 0.1 in. pitch headers spaced 0.9 in. apart



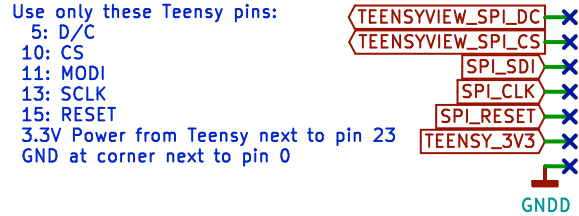
3.2" TFT LCD SPI w/MicroSD

Compatible with <https://www.adafruit.com/product/1743>
MicroSD card standalone pins shared between TFT and OLED boards.
Headers 3.0 in. apart



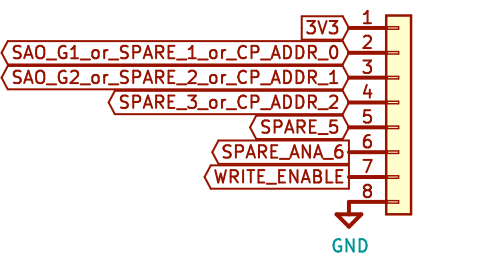
OLED TEENSYVIEW SPI

Monochrome 128x32
The TeensyView is designed to stack on the Teensy 3.2
Configuration: <https://www.sparkfun.com/products/14048>



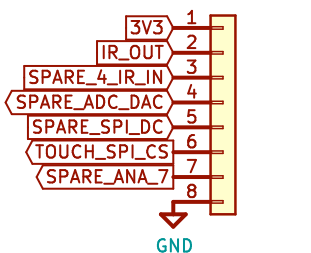
GPIO#1

Silkscreen: 3V3 ONLY
pin names



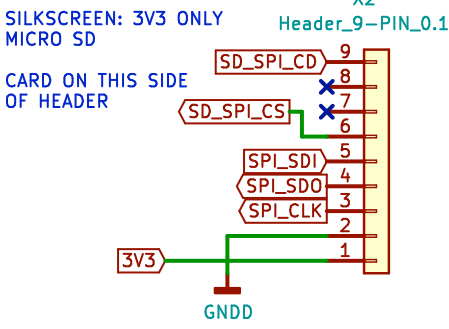
GPIO#2

Silkscreen: 3V3 ONLY
pin names



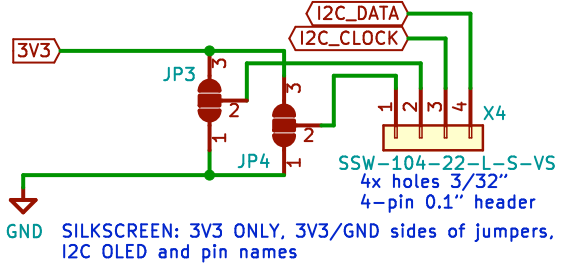
MICRO SD CARD

Compatible with <https://www.adafruit.com/product/4682>
MicroSD card standalone pins shared between TFT and OLED boards.

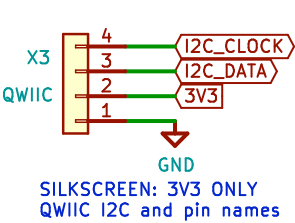


OLED MONOCHROME I2C

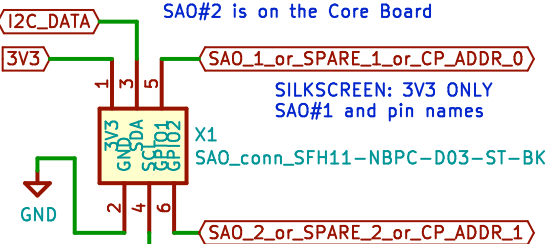
0.96" (128x64)
I2C 4-pins, ADDRESS: 0x3C (60 decimal)
Alternate is 0x3D, not 0x7A or 0x78 (wrong 8-bit!)
Must choose power polarity by soldering SJS.



QWIIC I2C



SAO #1 SUPERIOR ADD-ON

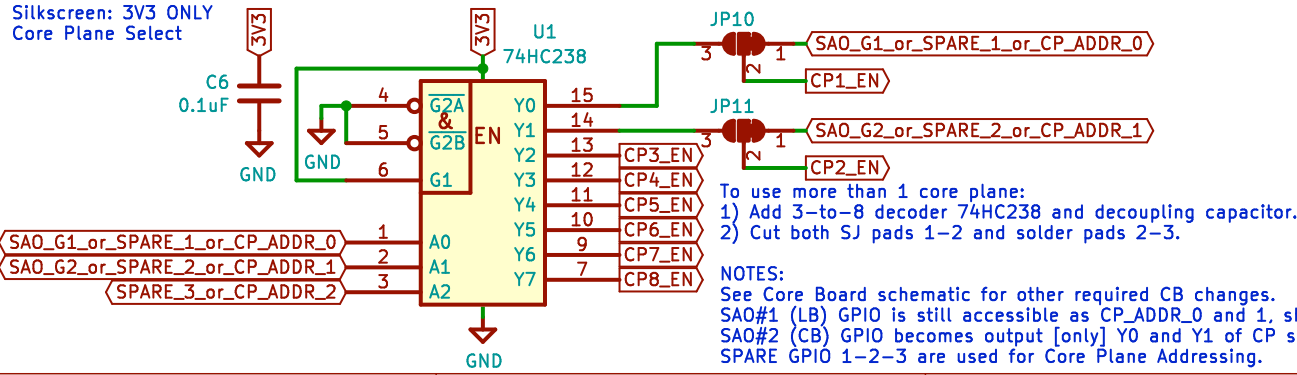


I2C ADDRESS TABLE

INCLUDED:	
AMBIENT LIGHT SENSOR	0x29 (47)
HALL SENSOR 1	0x30 (48)
HALL SENSOR 2	0x31 (49)
HALL SENSOR 3	0x32 (50)
HALL SENSOR 4	0x33 (51)
EEPROM (BOARD ID)	0x57 (87)
OPTIONAL:	
OLED	0x3C (60)
AND!XOR IO Exp. MCP23017	0x20 (32)
AND!XOR EEPROM AT24C32r	0x50 (80)
NFC CLICK PN7120	0x50-53

All 7-bit addresses should be greater than 0x07 and less than 0x78 (120).

CORE PLANE & CORE BOARD SAO #2 GPIO SELECT



All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

