CORE 64 INTERACTIVE CORE MEMORY BADGE V0.4 LOGIC BOARD

Power
Core64 LB v0.4 Power.sch

Driver
Core64 LB v0.4 Driver.sch

Sense LEDs ID
Core64 LB v0.4 Sense_LEDs_ID.sch

Expansion
Core64 LB v0.4 Expansion.sch

*** MUST CUT THE USB–VIN on back of TEENSY 3.2 ***

Teensy LC has incoming USB power/programming on board.
Because VIN–VUSB is cut on the back of the Teensy, power
into the Teensy's USB port is routed in this order:
TEENSY VUSB –> ON/OFF & LIPO –> 5V REG –> TEENSY VIN

TEENSY 3.2 MCU CONNECTIONS

R5
10K

J4
PRG
1

TEENSY_3V3

Teensy 3V3 is only used for AREF and
TeensyView. Current is limited, do not
use for anything else.

SILKSCREEN UNDER TEENSY: CUT VIN–BUSB
U2
Teensy3.2

TEENSY_VUSB

TEENSY_VIN
3.6–6.0V

J12
TEENSY Cur. Mon.

Spare IO | SPI Devices [OPTIONAL] | 8 Core Plane Selector [OPTIONAL] Requires other modifications. | PRIMARY USE 1 Core Plane | | PRIMARY USE 1 Core Plane | SPI Devices [OPTIONAL] | Spare Analog

SAO_G1_or_SPARE_1_or_CP_ADDR_0
SAO_G2_or_SPARE_2_or_CP_ADDR_1

OLED_SPI_CS
TOUCH_SPI_CS
SD_SPI_CS

IR_OUT

TFT_SPI_CS
TFT_SPI_DC

SPARE_4_IR_IN
TEENSYVIEW_SPI_CS

SPI_SDO
SPI_SDI

Q1P
Q1N
Q2P
Q2N
Q3P
Q3N
Q4P
Q4N

Left Edge
1 GND
2 0_RX1_Touch
3 1_TX1_Touch
4 2
5 3_TX_PWM
6 4_RX_PWM
7 5_TX1_PWM
8 6_PWM
9 7_RX3_DOUT
10 8_TX3_DIN
11 9_RX2_CS_PWM
12 10_TX2_CS_PWM
13 11_DOUT
14 12_DIN
15 VBat
16 3.3V
17 GND
18 Program
19 A14/DAC
20 13_LED_SCK
21 14_A0_SCK
22 15_A1_CS_Touch
23 16_A2_SCL0_Touch
24 17_A3_SDA0_Touch
25 18_A4_SDA0_Touch
26 19_A5_SCL0_Touch
27 20_A6_CS_PWM

Back R7

A13 51
3.3V 50
33_Touch 49
32_Touch_PWM 48
31_A20_TX2 47
30_A19_SDA1 46
29_A18_SCL1 45

Back L7
28_A17 44
27_A16 43
26_A15_RX2 42
25_Touch_PWM 41
24 40

Bottom Edge

A12 39
GND 38
A11 37
A10 36
AREF 35
VUSB 34
Vin 33
AGND 32
3.3V_max100mA 31
23_A9_Touch_PWM 30
22_A8_Touch_PWM 29
21_A7_RX1_CS_PWM 28

Back 1x4

Right Edge

SPARE_ANA_8

Q10N
Q10P
Q9N
Q9P
Q8N
Q8P
Q7N
Q7P
Q6N
Q6P

All analog–only
pins (A10–A14),
AREF, Program
and Reset are
3.3V only.

SD_SPI_CD
SPARE_ANA_7
SPARE_ANA_6

WRITE_ENABLE
SENSE_PULSE
SENSE_RESET

OLED_SPI_DC
TEENSYVIEW_SPI_DC

All analog–only
pins (A10–A14),
AREF, Program
and Reset are
3.3V only.

SPARE_ADC_DAC

SPI_CLK
SPARE_3_or_CP_ADDR_2
SPI_RESET

SPARE_5

Q5P
Q5N

I2C_DATA
I2C_CLOCK

TFT_BACKLIGHT
LED_ARRAY_3V3_SIG

VBAT_MON

GNDD

Reads 1/4 voltage of +VSW
(after RPP) before regulators.

I2C here, there, and everywhere.

3.2" TFT as LED
Array Replacement
[OPTIONAL]

RTC CLOCK BATTERY [OPTIONAL]

BT1
3V
+

SILKSCREEN:
RTC BAT. CR2032

To use the Teensy 3.2 RTC you must add two things:
1) Crystal: 32.768 kHz, 12.5 pF Citizen CFS–206, Digi-Key 300–8763–ND (5ppm)
   (on bottom side of the Teensy board, not shown in this schematic)
2) Battery Holder: MPD BC–2003, Digi-Key BC–2003–TR-CT-ND
3) Battery: 3V CR2032 Digi-Key P189-ND
   (battery and holder on backside of logic board)

QxP (PNP) is normally high, low to activate matrix transistor.
QxN (NPN) is normally low, high to activate matrix transistor.

SILKSCREEN FRONT

1)

L1
Core_64_Logo

SILKSCREEN BACK

1) Serial Number Sticker Zone
2) Board name, version, date, Machine Ideas

L2
Core_64_Logo

L3
Core_64_Github_Link

All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

BOM TO DO: TEENSY requires at least three headers
that do not get auto populated in the BOM from KiCAD.

Andy Geppert
DRAFT – UNRELEASED
Core64.MachineIdeas.com

Sheet: /
File: Core64 LB v0.4.sch
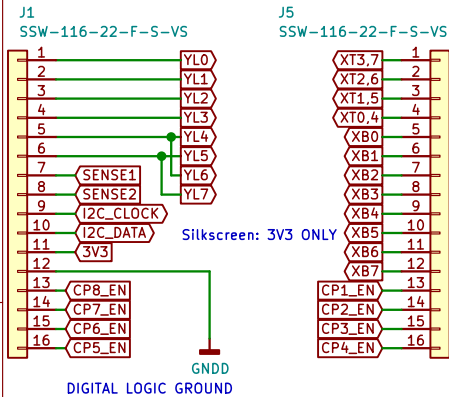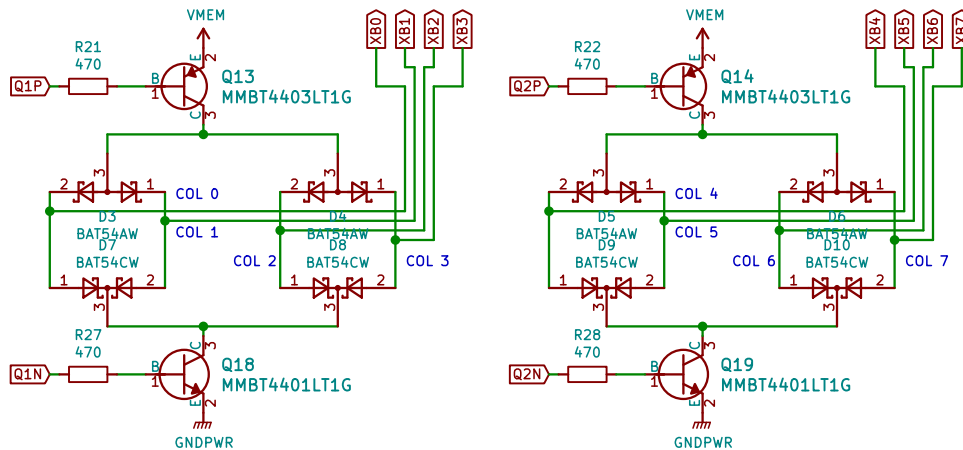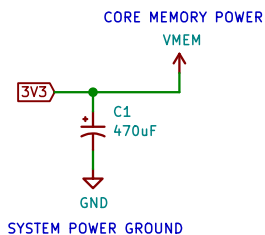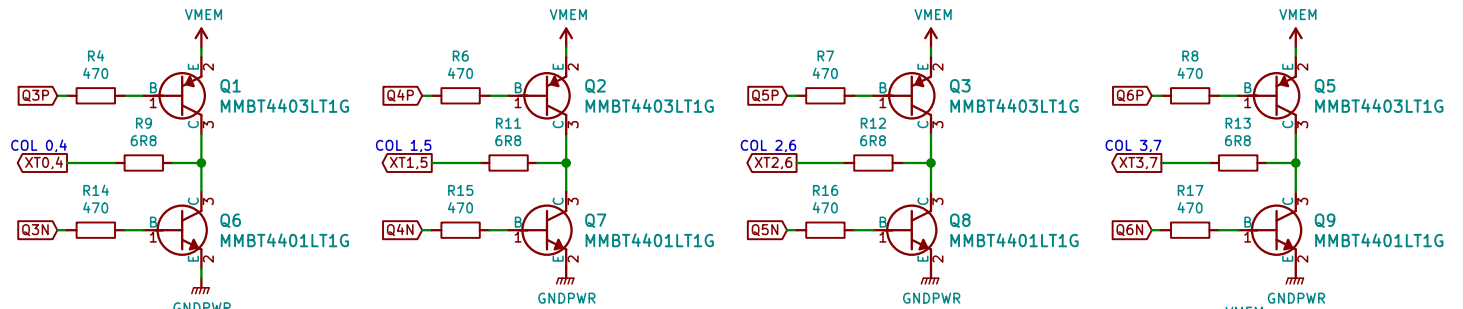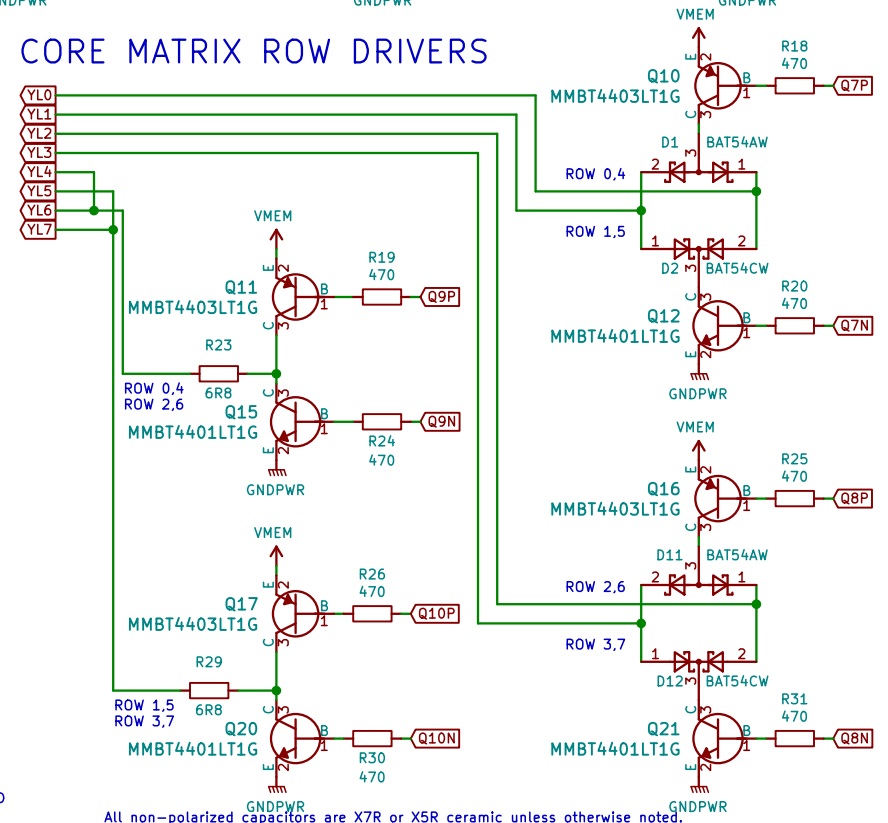
Title: Core 64 – Main Sheet Index

| Size: A | Date: 2020-11-14 | **Rev: 0.4** |
| KiCad E.D.A. kicad (5.1.2-1)-1 | | Id: 1/5 |

CORE BOARD INTERCONNECTS

J1
SSW-116-22-F-S-VS

1	YL0
2	YL1
3	YL2
4	YL3
5	YL4
6	YL5
7	SENSE1 / YL6
8	SENSE2 / YL7
9	I2C_CLOCK
10	I2C_DATA
11	3V3
12	
13	CP8_EN
14	CP7_EN
15	CP6_EN
16	CP5_EN

J5
SSW-116-22-F-S-VS

1	XT3,7
2	XT2,6
3	XT1,5
4	XT0,4
5	XB0
6	XB1
7	XB2
8	XB3
9	XB4
10	XB5
11	XB6
12	XB7
13	CP1_EN
14	CP2_EN
15	CP3_EN
16	CP4_EN

Silkscreen: 3V3 ONLY

GNDD
DIGITAL LOGIC GROUND

QxP (PNP) is normally high, low to activate matrix transistor.
QxN (NPN) is normally low, high to activate matrix transistor.
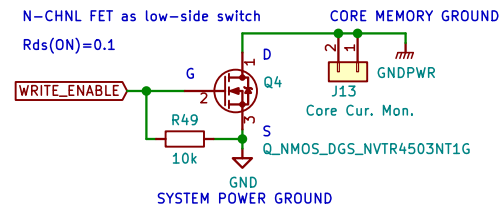
CORE MATRIX TOP COLUMN DRIVERS

R4 470 — Q3P — Q1 MMBT4403LT1G — VMEM
R9 6R8 — COL 0,4 — XT0,4
R14 470 — Q3N — Q6 MMBT4401LT1G — GNDPWR

R6 470 — Q4P — Q2 MMBT4403LT1G — VMEM
R11 6R8 — COL 1,5 — XT1,5
R15 470 — Q4N — Q7 MMBT4401LT1G — GNDPWR

R7 470 — Q5P — Q3 MMBT4403LT1G — VMEM
R12 6R8 — COL 2,6 — XT2,6
R16 470 — Q5N — Q8 MMBT4401LT1G — GNDPWR

R8 470 — Q6P — Q5 MMBT4403LT1G — VMEM
R13 6R8 — COL 3,7 — XT3,7
R17 470 — Q6N — Q9 MMBT4401LT1G — GNDPWR

CORE MATRIX BOTTOM COLUMN DRIVERS

R21 470 — Q1P — Q13 MMBT4403LT1G — VMEM
XB0 XB1 XB2 XB3
D3 BAT54AW — COL 0
D7 BAT54CW
D4 BAT54AW — COL 1
D8 BAT54CW
COL 2
COL 3
R27 470 — Q1N — Q18 MMBT4401LT1G — GNDPWR

R22 470 — Q2P — Q14 MMBT4403LT1G — VMEM
XB4 XB5 XB6 XB7
D5 BAT54AW — COL 4
D9 BAT54CW
D6 BAT54AW — COL 5
D10 BAT54CW
COL 6
COL 7
R28 470 — Q2N — Q19 MMBT4401LT1G — GNDPWR

CORE MATRIX ROW DRIVERS

YL0
YL1
YL2
YL3
YL4
YL5
YL6
YL7

Q10 MMBT4403LT1G — VMEM — R18 470 — Q7P
D1 BAT54AW — ROW 0,4
D2 BAT54CW — ROW 1,5
Q12 MMBT4401LT1G — R20 470 — Q7N — GNDPWR

Q11 MMBT4403LT1G — VMEM — R19 470 — Q9P
R23 6R8 — ROW 0,4 ROW 2,6
Q15 MMBT4401LT1G — R24 470 — Q9N — GNDPWR

Q17 MMBT4403LT1G — VMEM — R26 470 — Q10P
R29 6R8 — ROW 1,5 ROW 3,7
Q20 MMBT4401LT1G — R30 470 — Q10N — GNDPWR

Q16 MMBT4403LT1G — VMEM — R25 470 — Q8P
D11 BAT54AW — ROW 2,6
D12 BAT54CW — ROW 3,7
Q21 MMBT4401LT1G — R31 470 — Q8N — GNDPWR

All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

CORE MATRIX POWER

3V3 — C1 470uF — VMEM
CORE MEMORY POWER
GND
SYSTEM POWER GROUND

CORE MATRIX WRITE ENABLE

N-CHNL FET as low-side switch
Rds(ON)=0.1

WRITE_ENABLE — G — Q4 — D
R49 10k — S
Q_NMOS_DGS_NVTR4503NT1G
GND
SYSTEM POWER GROUND

J13
Core Cur. Mon.
CORE MEMORY GROUND
GNDPWR

Drive Transistor current: 3.3/470=7mA (too much for Teensy LC)
Matrix 1/2 select current: 3.3/6.8= 485 mA (does not account for voltage drop in transistors)

Andy Geppert
DRAFT – UNRELEASED
Core64.MachineIdeas.com

Sheet: /Driver/
File: Core64 LB v0.4 Driver.sch
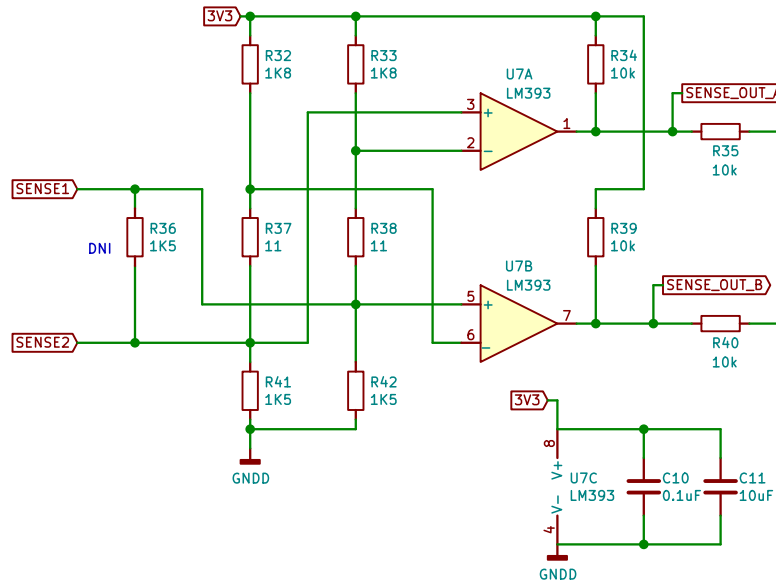
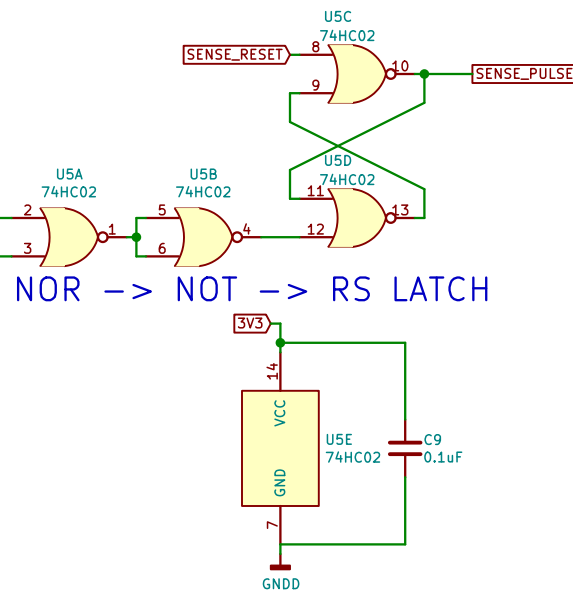Title: Core 64 – Core Matrix Driver

Size: A	Date: 2020-11-14	Rev: 0.4
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 2/5

SENSE SIGNAL DIFFERENTIAL AMPLIFIERS

3V3

R32 1K8
R33 1K8
R34 10k

U7A LM393

SENSE_OUT_A

R35 10k

SENSE1

DNI R36 1K5

R37 11
R38 11

U7B LM393

SENSE_OUT_B

R39 10k

R40 10k

SENSE2

R41 1K5
R42 1K5

GNDD

3V3

U7C LM393
V+
V-
C10 0.1uF
C11 10uF

GNDD

SENSE SIGNAL LATCH

U5C 74HC02

SENSE_RESET

SENSE_PULSE

U5A 74HC02

U5B 74HC02

U5D 74HC02

NOR -> NOT -> RS LATCH

3V3

U5E 74HC02
VCC
GND
C9 0.1uF

GNDD

SENSE DEBUG

SENSE_PULSE
SENSE_RESET
SENSE_OUT_B
SENSE_OUT_A
SENSE2
SENSE1
3V3

Header not populated

HEADER_8-PIN_0.1

J6

GNDD

SILKSCREEN: 3V3 ONLY
SENSE DEBUG

LED ARRAY DRIVE AND LEVEL SHIFT

LED_ARRAY_3V3_SIG

5V0

LED_ARRAY_5V0_SIG

5V0

C4 0.1uF

U3
A
GND
VCC
/OE
Y

R50 470

SN74LV1T125DBVR

SILKSCREEN:
5V0 ONLY
LED ARRAY

GNDD

GNDD

TSM-106-03-T-DV

3V3

5V0

LED Cur. Mon.

J17

LED_ARRAY_5V0_SIG

GND

J10

GND
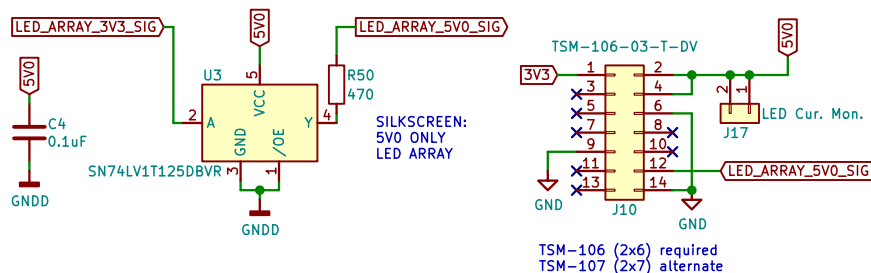
TSM-106 (2x6) required
TSM-107 (2x7) alternate

Symbol view is looking down
on the front face of the Logic
Board, with the male header
pins pointing up at you.

BOARD ID AND S/N

EEPROM I2C ADDRESS: 0b1010111, 0x57 (87)
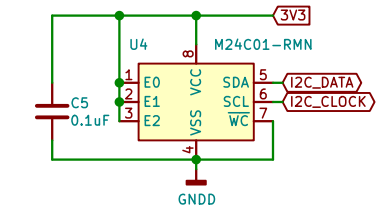
3V3

C5 0.1uF

U4
E0
E1
E2
VSS
VCC
SDA
SCL
WC

M24C01-RMN

I2C_DATA

I2C_CLOCK

GNDD

All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

EVERYTHING ON THIS SHEET IS USER-PROVIDED OPTIONAL ADD-ONS
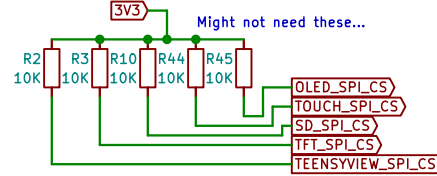
OLED COLOR SPI w/MicroSD

Compatible: https://www.adafruit.com/product/1431
1.5" 128x128, 16-bit color w/MicroSD holder
OLED has 5V -> 3V3 regulator onboard.
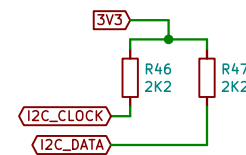MicroSD card standalone pins shared between TFT and OLED boards.

OLED ON THIS SIDE OF HEADER — TOP VIEW OF LB

HEADER_11-PIN_0.1 J14

Pin	Signal
1	SPI_SDO (COPI)
2	SPI_CLK
3	OLED_SPI_DC
4	SPI_RESET
5	OLED_SPI_CS
6	SD_SPI_CS
7	SPI_SDI (CIPO)
8	SD_SPI_CD
9	x
10	5V0
11	GND
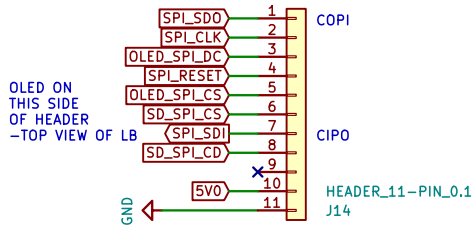
SILKSCREEN: 3V3 Logic ONLY, 3V3/GND sides of jumpers, SPI OLED
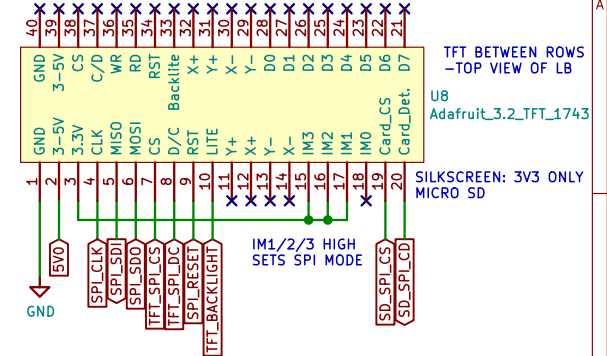
OLED TEENSYVIEW SPI

Monochrome 128x32
The TeensyView is designed to stack on the Teensy 3.2
Configuration: https://www.sparkfun.com/products/14048

Use only these Teensy pins:
21: D/C (default is 5)
10: CS
11: MODI
13: SCLK
15: RESET
3.3V Power from Teensy next to pin 23
GND at corner next to pin 0

TEENSYVIEW_SPI_DC
TEENSYVIEW_SPI_CS
SPI_SDO (COPI)
SPI_CLK
SPI_RESET
TEENSY_3V3
GNDD

OLED MONOCHROME I2C

0.96" (128x64)
I2C 4-pins, ADDRESS: 0x3C (60 decimal)
Alternate is 0x3D, not 0x7A or 0x78 (wrong 8-bit)!
Must choose power polarity by soldering SJS.

I2C_DATA
I2C_CLOCK
JP3 JP4
X4 SSW-104-22-L-S-VS
4x holes 3/32"
4-pin 0.1" header
3V3 GND

SILKSCREEN: 3V3 ONLY, 3V3/GND sides of jumpers,
I2C OLED and pin names

SPI CS PULL-UPS

Might not need these...
3V3

| R2 10K | R3 10K | R10 10K | R44 10K | R45 10K |

OLED_SPI_CS
TOUCH_SPI_CS
SD_SPI_CS
TFT_SPI_CS
TEENSYVIEW_SPI_CS

I2C PULL-UPS

3V3
R46 2K2   R47 2K2
I2C_CLOCK
I2C_DATA

GPIO#1

Silkscreen: 3V3 ONLY
pin names

J7 HEADER_8-PIN_0.1

Pin	Signal
1	3V3
2	SAO_G1_or_SPARE_1_or_CP_ADDR_0
3	SAO_G2_or_SPARE_2_or_CP_ADDR_1
4	SPARE_3_or_CP_ADDR_2
5	SPARE_5
6	SPARE_ANA_6
7	WRITE_ENABLE
8	GND

GPIO#2

J16 HEADER_8-PIN_0.1

Pin	Signal
1	3V3
2	IR_OUT
3	SPARE_4_IR_IN
4	SPARE_ADC_DAC
5	SPARE_ANA_7
6	TOUCH_SPI_CS
7	SPARE_ANA_8
8	GND

QWIIC I2C

X3 QWIIC

4	I2C_CLOCK
3	I2C_DATA
2	3V3
1	GND

SILKSCREEN: 3V3 ONLY
QWIIC I2C and pin names

SAO #1 SUPERIOR ADD-ON

SAO#2 is on the Core Board

I2C_DATA
3V3
SAO_G1_or_SPARE_1_or_CP_ADDR_0

SILKSCREEN: 3V3 ONLY
SAO#1 and pin names

X1 SAO_conn_SFH11-NBPC-D03-ST-BK
(3V3, GND, SDA, GPIO2, GPIO1)
GND
SAO_G2_or_SPARE_2_or_CP_ADDR_1
I2C_CLOCK

SAO v1.69bis (https://hackaday.io/project/52950-shitty-add-ons)
using Sullins SFH11-NBPC-D03-ST-BK female header
https://www.digikey.com/product-detail/en/sullins-connector-solutions/
SFH11-NBPC-D03-ST-BK/S9717-ND/4558818

3.2" TFT LCD SPI w/MicroSD

Compatible with https://www.adafruit.com/product/1743
TFT has 5V -> 3V3 regulator onboard.
MicroSD card standalone pins shared between TFT and OLED boards.
Headers 3.0 in. apart

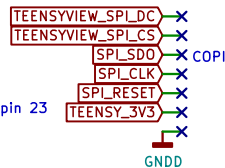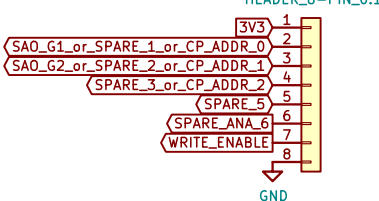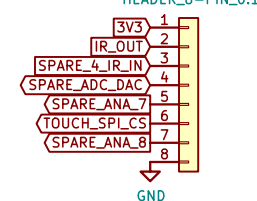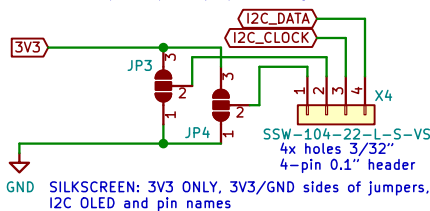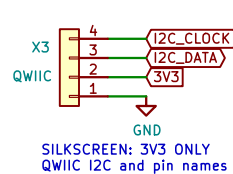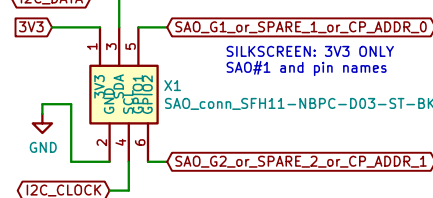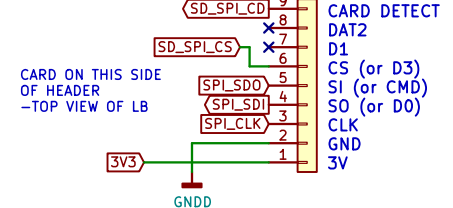U8 Adafruit_3.2_TFT_1743

TFT BETWEEN ROWS — TOP VIEW OF LB

Top row (40...21): GND 3-5V CS C/D WR RD RST Backlite X+ Y+ X- Y- D0 D1 D2 D3 D4 D5 D6 D7
Bottom row (1...20): GND 3-5V CLK MISO MOSI CS D/C RST LITE Y+ X+ Y- X- IM3 IM2 IM1 IM0 Card_CS Card_Det.

IM1/2/3 HIGH SETS SPI MODE

SILKSCREEN: 3V3 ONLY MICRO SD

5V0 GND
SPI_CLK
SPI_SDI
SPI_SDO
TFT_SPI_CS
TFT_SPI_DC
SPI_RESET
TFT_BACKLIGHT
SD_SPI_CS
SD_SPI_CD

MICRO SD CARD

Compatible with https://www.adafruit.com/product/4682
MicroSD card standalone pins shared between TFT and OLED boards.

SILKSCREEN: 3V3 ONLY MICRO SD

X2 Header_9-PIN_0.1

CARD ON THIS SIDE OF HEADER — TOP VIEW OF LB

Pin	Signal
9	SD_SPI_CD — CARD DETECT
8	DAT2
7	x — D1
6	SD_SPI_CS — CS (or D3)
5	SPI_SDO — SI (or CMD)
4	SPI_SDI — SO (or D0)
3	SPI_CLK — CLK
2	GND
1	3V3 — 3V

GNDD

I2C ADDRESS TABLE

INCLUDED:

Device	Address
AMBIENT LIGHT SENSOR	0X29 (47)
HALL SENSOR 1	0x30 (48)
HALL SENSOR 2	0x31 (49)
HALL SENSOR 3	0x32 (50)
HALL SENSOR 4	0x33 (51)
EEPROM (BOARD ID)	0x57 (87)

OPTIONAL:

Device	Address
OLED	0x3C (60)
ANDiXOR IO Exp. MCP23017	0x20 (32)
ANDiXOR EEPROM AT24C32r	0x50 (80)
NFC CLICK PN7120	0x50-53
PIMORONI UNICORN HAT	0x50 (N.C.)

All 7-bit addresses should be greater than 0x07 and less than 0x78 (120).

CORE PLANE & CORE BOARD SAO #2 GPIO SELECT

Silkscreen: 3V3 ONLY
Core Plane Select

3V3
C6 0.1uF
GND

U1 74HC238

Pin	Signal
4	G2A
5	G2B (& EN)
6	G1
1	A0
2	A1
3	A2
15	Y0
14	Y1
13	Y2 — CP3_EN
12	Y3 — CP4_EN
11	Y4 — CP5_EN
10	Y5 — CP6_EN
9	Y6 — CP7_EN
7	Y7 — CP8_EN

A0: SAO_G1_or_SPARE_1_or_CP_ADDR_0
A1: SAO_G2_or_SPARE_2_or_CP_ADDR_1
A2: SPARE_3_or_CP_ADDR_2

3V3
JP10: SAO_G1_or_SPARE_1_or_CP_ADDR_0 / CP1_EN
JP11: SAO_G2_or_SPARE_2_or_CP_ADDR_1 / CP2_EN

GND

To use more than 1 core plane:
1) Add 3-to-8 decoder 74HC238 and decoupling capacitor.
2) Cut both SJ pads 1-2 and solder pads 2-3.

NOTES:
See Core Board schematic for other required CB changes.
SAO#1 (LB) GPIO is still accessible as CP_ADDR_0 and 1, shared.
SAO#2 (CB) GPIO becomes output [only] Y0 and Y1 of CP selector.
SPARE GPIO 1-2-3 are used for Core Plane Addressing.

All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

Andy Geppert
DRAFT — UNRELEASED
Core64.MachineIdeas.com
Sheet: /Expansion/
File: Core64 LB v0.4 Expansion.sch

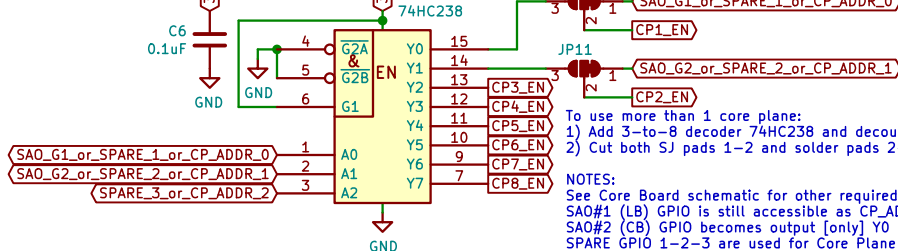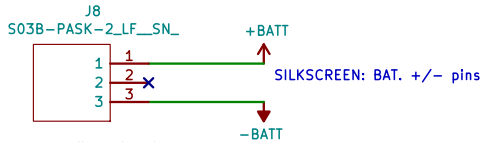**Title: Core 64 — Expansion**

Size: A	Date: 2020-11-14	Rev: 0.4
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 4/5

STANDARD KIT CONFIGURATION — AS MANUFACTURED

TWO POWER INPUT SOURCES SELECTED BY SPDT SWITCH

SOURCE 1 "ON (BAT)"
BUILT—IN BATTERY PACK (Keystone 2482CN) WITH 4X "AAA" Primary/Alkaline Cells
OK to use Energizer Ultimate Lithium (light weight!) with open cell 7.2V, loaded will be <7V.
Battery Pack includes wires and 3-pin plug.

Socket: TH, Side Entry, JST PA S03B-PASK-2(LF)(SN), Digikey 455-1848-ND ($0.44/ea)
Socket: SMT, Top Entry, JST PA BM03B-PASS-1-TFT(LF)(SN), Digikey 455-2638-1-ND ($0.80)
Socket: SMT, Side Entry, Keystone 976, Digikey 36-976CT-ND ($2.71/ea)

J8
S03B-PASK-2_LF_SN_

1 → +BATT

2 ✕

3 → −BATT

SILKSCREEN: BAT. +/− pins

7.5V MAX !!!

Limitation of 5V0 regulator.

SOURCE 2 "OFF (USB)"
USB 5V supplied through Teensy 3.2 and optional LiPo Charger USB port.
With the VIN-VUSB trace cut on the back of the Teensy, the TEENSY_VUSB is taken off of the
Teensy Board and routed on the Core64 LB to the lower position of the power switch. From
here, it powers the whole Core64 system and routes back to the TEENSY_VIN after passing
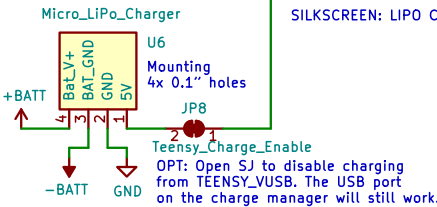through the 5V LDO regulator.

ALTERNATE 1S LIPO BATTERY — USER SUPPLIED

1) Remove the 4x "AAA" battery pack AND the battery connector (so you don't try to charge AAAs with a LiPo charger!).

2) Purchase and install a LiPo charge manager.
   a) The logic board is designed to accept this one: https://www.adafruit.com/product/1904.
   b) Solder the the charge manager directly to the board without headers to keep a low profile to allow the stylus to fit.

3) Purchase and install a 1S LiPo using double-sided tape.
   a) Choose a 1S Lipo with built—in cell over/under voltage protection. Recommended:
      2500mAh https://www.adafruit.com/product/328   1.8" x 2.4" x 0.26" (47mm x 61mm x 6.7mm)
      2000mAh https://www.adafruit.com/product/2011   2.4" x 1.4" x 0.3" (60mm x 36mm x 7mm)
      1200mAh https://www.adafruit.com/product/258   1.3" x 2.4" x 0.2" (34mm x 62mm x 5mm)
   b) The LiPo can be up to 50 x 65 x 15mm. A maximum   SILKSCREEN: +/− pins
   a) Make sure no part of the LiPo foil pouch can short-out adjacent pins or pads in the area.
   b) Insulate it with Kapton tape or similar.

* The LiPo charger 5V pin and USB port are also connected to the Teensy USB port, through TEENSY_VUSB.
* Connecting a USB cable to the Teensy will power the Core64 board, charge the battery and connect to the serial port of the
  Teensy. If you do NOT want the Core64 board to be powered from the USB port of the charger, cut the Teensy_Charge_Enable
  solder jumper. Then, connecting a USB cable to the LiPo charger will ONLY charge the battery and power the logic board,
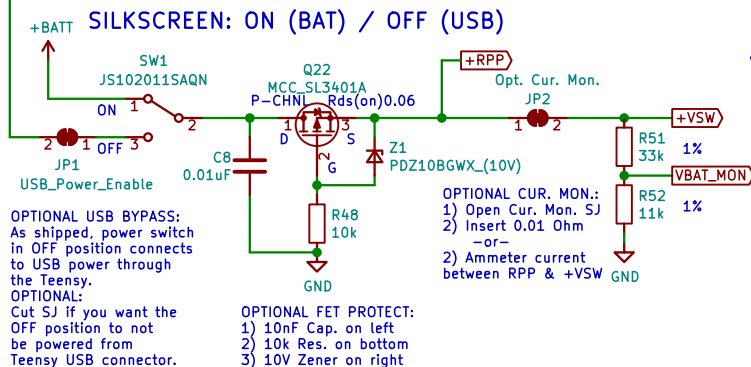 when the power switch is ON (up position).

Micro_LiPo_Charger

U6
Mounting
4x 0.1" holes
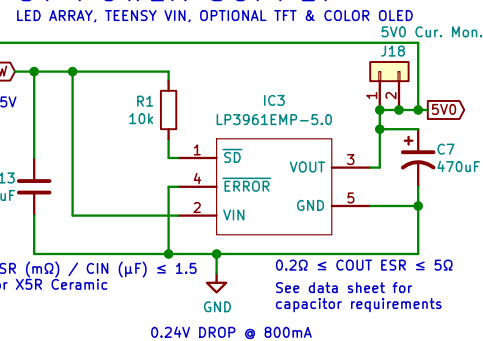
+BATT

Bat.V+
BAT_GND
GND
5V

JP8
Teensy_Charge_Enable

−BATT   GND

OPT: Open SJ to disable charging
from TEENSY_VUSB. The USB port
on the charge manager will still work.

SILKSCREEN: LIPO CHARGER

1S LIPO ONLY !!!

SILKSCREEN: BAT. + BAT. −

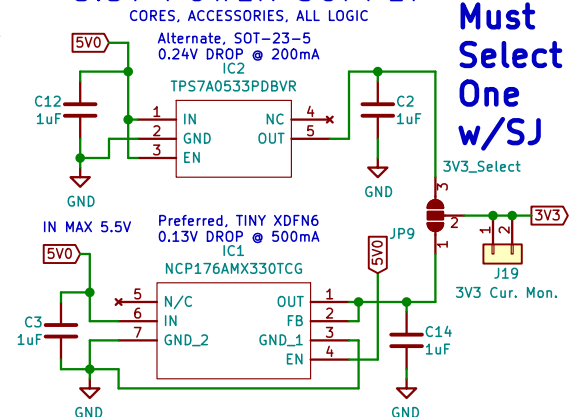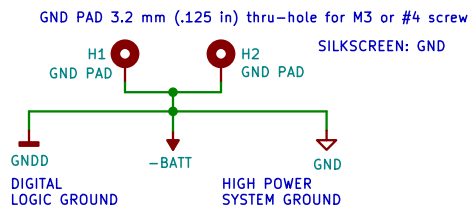## *** ALL CONFIGURATIONS REQUIRE CUTTING VIN-VUSB TRACE ON BACK OF TEENSY ***

TEENSY_VUSB   TEENSY_VIN

POWER SWITCH, RPP, V & I MONITOR

SILKSCREEN: ON (BAT) / OFF (USB)

+BATT

SW1
JS102011SAQN
ON

OFF

JP1
USB_Power_Enable

OPTIONAL USB BYPASS:
As shipped, power switch
in OFF position connects
to USB power through
the Teensy.
OPTIONAL:
Cut SJ if you want the
OFF position to not
be powered from
Teensy USB connector.

C8
0.01uF

Q22
MCC_SL3401A
P-CHNL Rds(on)0.06

R48
10k

GND

Z1
PDZ10BGWX_(10V)

OPTIONAL FET PROTECT:
1) 10nF Cap. on left
2) 10k Res. on bottom
3) 10V Zener on right

+RPP
Opt. Cur. Mon.
JP2

OPTIONAL CUR. MON.:
1) Open Cur. Mon. SJ
2) Insert 0.01 Ohm
   -or-
2) Ammeter current
between RPP & +VSW

R51
33k   1%

R52
11k   1%

+VSW

VBAT_MON

GND

5V POWER SUPPLY

LED ARRAY, TEENSY VIN, OPTIONAL TFT & COLOR OLED

5V0 Cur. Mon.
J18

+VSW

VIN MAX 7.5V

R1
10k

IC3
LP3961EMP-5.0

C13
68uF

SD

ERROR

VIN

VOUT

GND

5V0

C7
470uF

CIN ESR (mΩ) / CIN (µF) ≤ 1.5
X7R or X5R Ceramic

0.2Ω ≤ COUT ESR ≤ 5Ω

See data sheet for
capacitor requirements

0.24V DROP @ 800mA

GND

3.3V POWER SUPPLY

CORES, ACCESSORIES, ALL LOGIC

5V0

Alternate, SOT-23-5
0.24V DROP @ 200mA
IC2
TPS7A0533PDBVR

C12
1uF

IN

GND

EN

NC

OUT

C2
1uF

GND

3V3_Select

GND

IN MAX 5.5V

5V0

Preferred, TINY XDFN6
0.13V DROP @ 500mA
IC1
NCP176AMX330TCG

C3
1uF

N/C

IN

GND_2

OUT

FB

GND_1

EN

GND

5V0

JP9

3V3

C14
1uF

GND

J19
3V3 Cur. Mon.

Must Select One w/SJ

ALL SYSTEM GROUND

GND PAD 3.2 mm (.125 in) thru-hole for M3 or #4 screw

SILKSCREEN: GND

H1
GND PAD

H2
GND PAD

GNDD   −BATT   GND

DIGITAL
LOGIC GROUND

HIGH POWER
SYSTEM GROUND

POWER RAILS

SILKSCREEN: POWER

+BATT
TEENSY_VUSB
+RPP
+VSW
5V0
3V3
VBAT_MON

GND

J3
Conn_01x08_Female

All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.