CORE64C INTERACTIVE CORE MEMORY LOGIC BOARD

Sheet: Power
File: Core64C LB v0.2 Power.sch

Sheet: Driver
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Sheet: Sense_LEDs_ID
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Sheet: Expansion
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RASPBERRY PI PICO RP2040 CONNECTIONS

RP2040 PINS RESERVED FOR USE ON PICO BOARD:
GPIO29 : IP Used in ADC mode (ADC3) to measure VSYS/3 (Core64C as 5V0/3)
GPIO25 : OP User LED built-in to Pico
GPIO24 : IP VBUS sense - high if VBUS is present, else low
GPIO23 : OP Controls the on-board SMPS Power Save pin

Spare IO
PRIMARY USE
U1
SC0915_PICO
Pico has incoming USB power/programming on board.

	SENSE_RESET	1	UART0_TX/I2C0_SDA/SPI0_RX/GP0	GND	D
SAO_G1_or_SPARE1_or_CP1		2	UART0_RX/I2C0_SCL/GPI0_CSn/GP1	GND	C
		3	GND	GND	B
SAO_G2_or_SPARE2_or_CP2		4	I2C1_SDA/SPI0_SCK/GP2	GND	A
SPARE3_or_CP3		5	I2C1_SCL/SPI0_TX/GP3	BOOTSEL	TP6
SPARE4_or_CP4		6	UART1_TX/I2C0_SDA/SPI0_RX/GP4	GPIO25/LED	TP5
HS1_or_SPARE5_or_CP5		7	UART1_RX/I2C0_SCL/SPI0_CSn/GP5	GPIO/SMPS	TP4
		8	GND	USB_DP	TP3
HS2_or_SPARE6_or_CP6		9	I2C1_SDA/SPI0_SCK/GP6	USB_DM	TP2
HS3_or_SPARE7_or_CP7		10	I2C1_SCL/SPI0_TX/GP7	GND	TP1
HS4_or_SPARE8_or_CP8		11	UART1_TX/I2C0_SDA/SPI1_RX/GP8	SWDIO	D3
	SR_LAT	12	UART1_RX/I2C0_SCL/SPI1_CSn/GP9	GND	D2
		13	GND	SWCLK	D1
	I2C_DATA	14	I2C1_SDA/SPI1_SCK/GP10	VBUS	40
	I2C_CLOCK	15	I2C1_SCL/SPI1_TX/GP11	VSYS	39
	SR_SER	16	UART0_TX/I2C0_SDA/GPI1_RX/GP12	GND	38
	SR_CLK	17	UART0_RX/I2C0_SCL/SPI1_CSn/GP13	3V3_EN	37
		18	GND	3V3OUT	36
SPI_CD		19	I2C1_SDA/SPI1_SCK/GP14	ADC_VREF	35
SPI_RESET		20	I2C1_SCL/SPI1_TX/GP15	ADC2/GP28	34
SPI_SDI		21	UART0_TX/I2C0_SDA/SPI0_RX/GP16	AGND/GND	33
SPI_CS1		22	UART0_RX/I2C0_SCL/SPI0_CSn/GP17	I2C1_SCL/ADC1/GP27	32
		23	GND	I2C1_SDA/ADC0/GP26	31
SPI_CLK		24	I2C1_SDA/SPI0_SCK/GP18	RUN	30
SPI_SDO		25	I2C1_SCL/SPI0_TX/GP19	GP22	29
	CORE_ARRAY_ENABLE	26	I2C0_SDA/GP20	GND	28
				I2C0_SCL/GP21	27

ALTERNATE HALL SWITCHES OR
OPTIONAL CORE PLANE SELECT

CP1_EN	SAO_G1_or_SPARE1_or_CP1
CP2_EN	SAO_G2_or_SPARE2_or_CP2
CP3_EN	SPARE3_or_CP3
CP4_EN	SPARE4_or_CP4
CP5_EN	HS1_or_SPARE5_or_CP5
CP6_EN	HS2_or_SPARE6_or_CP6
CP7_EN	HS3_or_SPARE7_or_CP7
CP8_EN	HS4_or_SPARE8_or_CP8

SPI Bus
GNDD
GNDD

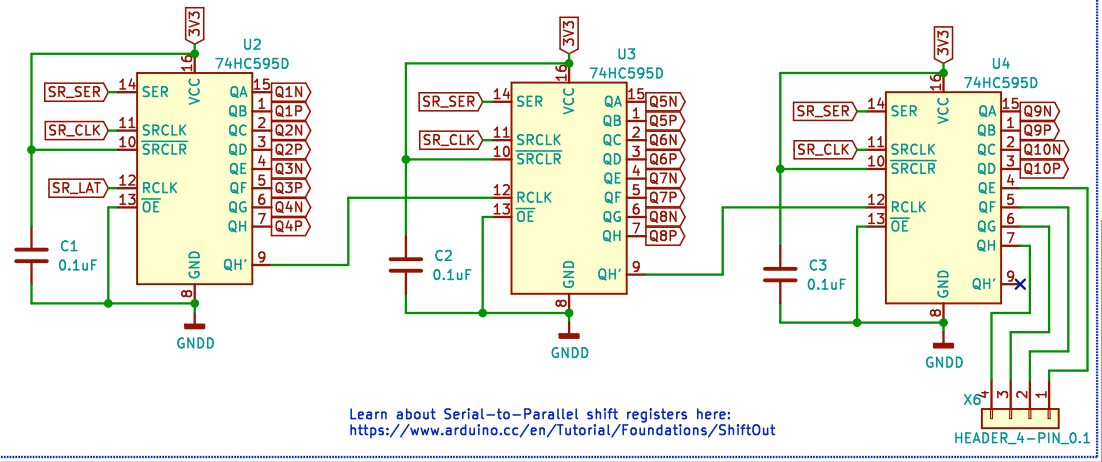
PRIMARY USE
PICO_VBUS
5V if USB
(Limit 1.8-5.5V)
PICO_VSYS
3V3_MON
BAT_MON
+VSW/3
LED_MATRIX_3V3_SIG
SENSE_PULSE

Spare
3.3V only
SPARE_ADC2
Remove BAT and 3V3_MON resistors on Power sheet to use SPARE_ADC0 and 1.
SPARE_ADC1
SPARE_ADC0

300 mA
PICO_3V3OUT
Pico 3V3OUT is only used for ADC_AREF. Current is limited. Be careful if you use it.

QxN (NPN) is normally low, high to activate matrix transistor.
QxP (PNP) is normally high, low to activate matrix transistor.

OUTPUT EXPANSION TO CORE MATRIX DRIVER



Learn about Serial-to-Parallel shift registers here:
https://www.arduino.cc/en/Tutorial/Foundations/ShiftOut

SILKSCREEN FRONT

Interactive Core Memory
All logic is 3V3 Level

L1
Core_64c_Logo_7mm_tall
Core64c_7mm

SILKSCREEN BACK

Core 64 Logo
Interactive Core Memory
QR Code
Maker
Website
PCB Maker
Assembler
Serial Number
P/N
REV

L2
Core_64c_Logo_7mm_tall
Core64c_7mm

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As fabricated 2021-06-04
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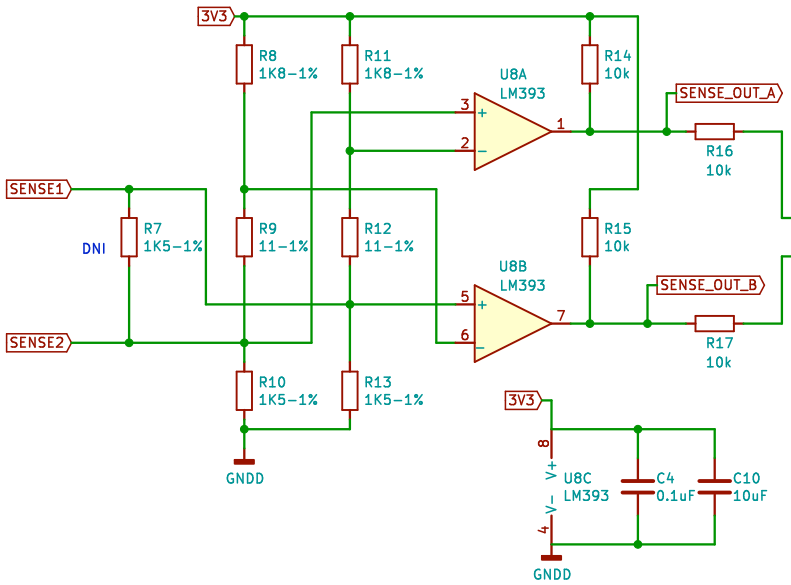
Concept and design by Andy Geppert @ www.MachineIdeas.com

Sheet: /
File: Core64c LB v0.2.sch

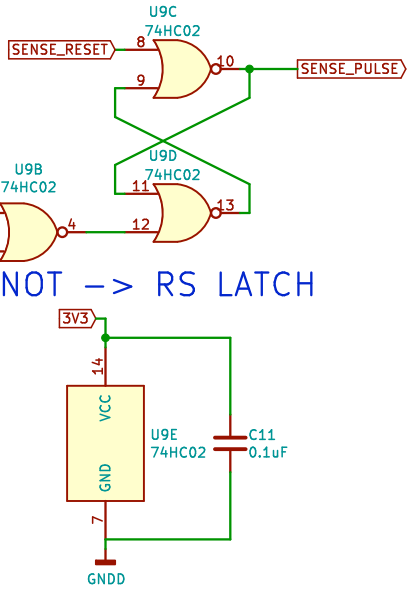
Title: Core64c - Main Sheet Index

Size: A	Date: 2021-06-04	**Rev: 0.2**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 1/5

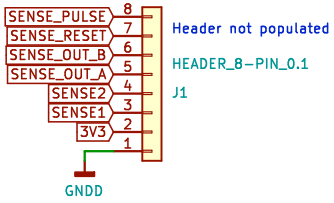
SENSE SIGNAL DIFFERENTIAL AMPLIFIERS



SENSE SIGNAL LATCH

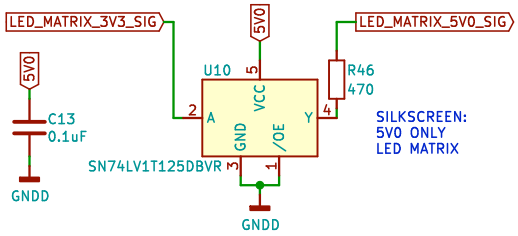


SENSE DEBUG



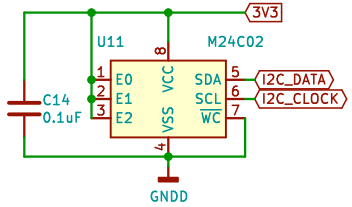
SILKSCREEN: 3V3 ONLY
SENSE DEBUG

LED MATRIX DRIVE AND LEVEL SHIFT



BOARD ID AND S/N

EEPROM I2C ADDRESS: 0b1010111, 0x57 (87)



All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

As fabricated 2021-06-04
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Concept and design by Andy Geppert © www.MachineIdeas.com

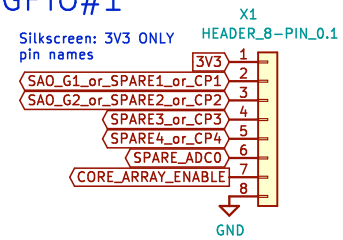
Sheet: /Sense_LEDs_ID/
File: Core64C LB v0.2 Sense_LEDs_ID.sch

Title: Core64C – Sense

Size: A	Date: 2021-06-04	**Rev: 0.2**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 2/5

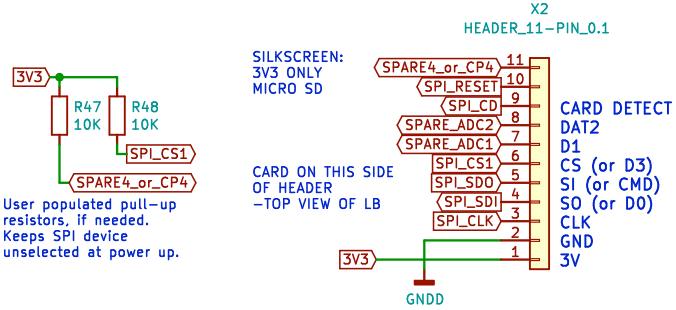
EVERYTHING ON THIS SHEET IS USER-PROVIDED OPTIONAL ADD-ONS

GPIO#1



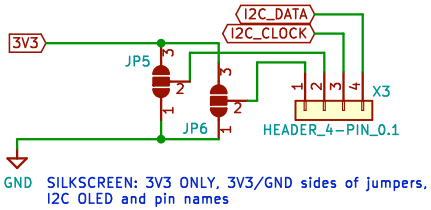
GPIO#2, SPI, SD CARD

Compatible with MicroSD Card Adapter https://www.adafruit.com/product/4682 (use pins 1-6, 9)



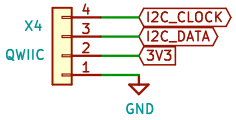
OLED MONOCHROME I2C

Generic 0.96" (128x64) or 1.5" (128x128)
I2C 4-pins, often ADDRESS: 0x3C (60 decimal)
Alternate is 0x3D, not 0x7A or 0x78 (wrong 8-bit)!
Must choose power polarity by soldering SJS.



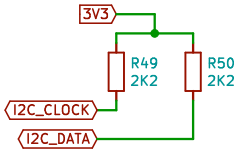
SILKSCREEN: 3V3 ONLY, 3V3/GND sides of jumpers,
I2C OLED and pin names

QWIIC I2C



SILKSCREEN: 3V3 ONLY
QWIIC I2C and pin names

I2C PULL-UPS



I2C ADDRESS TABLE

INCLUDED:	
AMBIENT LIGHT SENSOR	0X29 (47)
HALL SENSOR 1	0x30 (48)
HALL SENSOR 2	0x31 (49)
HALL SENSOR 3	0x32 (50)
HALL SENSOR 4	0x33 (51)
EEPROM (BOARD ID)	0x57 (87)
OPTIONAL:	
OLED	0x3C (60)
AND!XOR IO Exp. MCP23017	0x20 (32)
AND!XOR EEPROM AT24C32r	0x50 (80)
NFC CLICK PN7120	0x50-53
PIMORONI UNICORN HAT	0x50 (N.C.)

All 7-bit addresses should be greater
than 0x07 and less than 0x78 (120).

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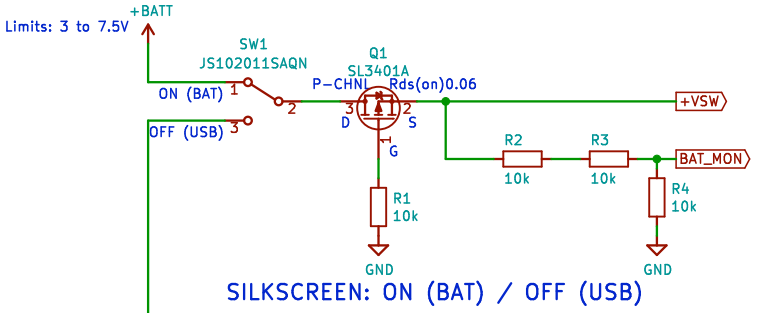
Sheet: /Expansion/
File: Core64C LB v0.2 Expansion.sch

Title: Core64C - Expansion

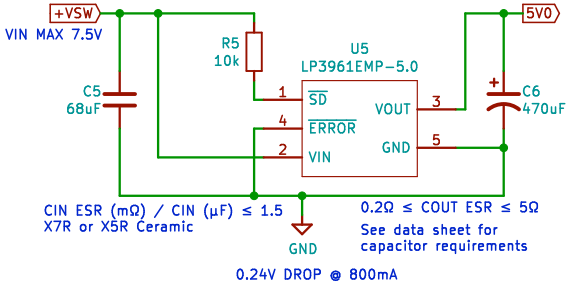
Size: A	Date: 2021-06-04	**Rev: 0.2**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 3/5

POWER SWITCH, REVERSE POLARITY PROTECTION, BATTERY VOLTAGE MONITOR

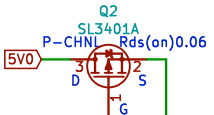


5V POWER SUPPLY

LED MATRIX, PICO, 3V3 REGULATOR, OPTIONAL ACCESSORIES



PICO VUSB / VSYS AUTOMATIC "OR" SWITCH



PICO_VBUS is the USB voltage of the cable plugged into the PICO or the optional 1s LiPo charger (on LED Matrix Board) if the USB cable is plugged into the LiPo charger and the USB charge enable solder jumper is closed on the back of the LED Matrix board.

This diode is built-in to the Pico. It is shown here for clarity in the operational description below.

POWER PATH DESCRIPTION

TWO POWER INPUT SOURCES SELECTED BY SPDT SWITCH.

Power Switch ON (BAT), USB cable is NOT connected:
P-FET (gate is low) conducts 5V0 (or less if the battery is less than about 5.2V) so that PICO_SYS is powered. PICO_VBUS is not energized because of built-in Zener diode on the Pico.

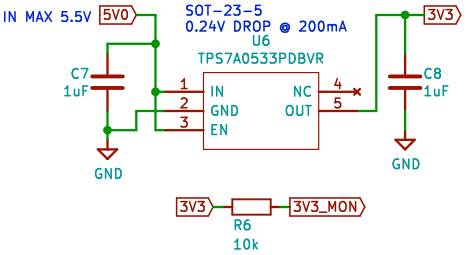
Power Switch OFF (USB), USB cable is NOT connected:
System is off and does not receive power from the battery.

Power Switch ON (BAT), USB cable IS connected:
If USB voltage is greater than 5V0, the Pico will operate with VSYS at the USB voltage. The rest of the system will operate from whatever the 5V0 rail voltage is. If USB voltage is less than 5V0, the Pico will operate with VSYS at 5V0 along with the rest of the system. The Pico diode prevents current flow from 5V0 back out through USB.

Power Switch OFF (USB), USB cable IS connected:
The USB voltage will be greater than 5V0 (because there is a voltage drop through the 5V0 regulator). The P-FET will be off, the Pico will run at the USB voltage, the rest of the system will run at slightly less than the USB voltage.

3.3V POWER SUPPLY

CORE MATRIX, OPTIONAL ACCESSORIES, ALL LOGIC

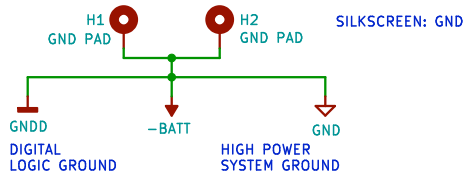


IMPORTANT NOTES

1) Battery pack absolute maximum voltage is 7.5V.
2) In Core64C, the battery is normally installed on the back of the LED Matrix and connects to the Logic Board through the lower right (second from bottom) pin (+BAT) in the 2x20 sockets.
3) The standard built-in battery pack is Keystone 2482 with 4X "AAA" primary/alkaline cells.
4) OK to use Energizer Ultimate Lithium (very light weight!) with combined open cell voltage of 7.2V. It will be <7V when there is a load on the cells.
5) If the 1s LiPo option is used on the LED Matrix, the LiPo battery voltage (3.7V nominal) is used and works down to about 3.1V, where the batteries built-in low voltage cutoff should kick in.

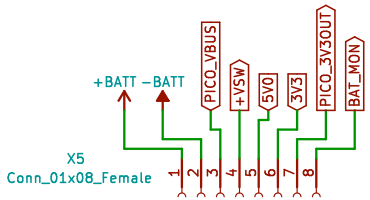
ALL SYSTEM GROUND

GND PAD 3.2 mm (.125 in) thru-hole for M3 or #4 screw



POWER RAILS

SILKSCREEN: POWER



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Sheet: /Power/
File: Core64C LB v0.2 Power.sch

Title: Core64C – Power Schematic

Size: A	Date: 2021-06-04	**Rev: 0.2**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 4/5

Drive Transistor current: 3.3/470=7mA

CORE BOARD INTERCONNECTS

J2
HDR100IMP40F-G-V-TH

J3
HDR100IMP40F-G-V-TH

Silkscreen: 3V3 ONLY

GNDD
DIGITAL
LOGIC
GROUND

5VUSB if LED MATRIX
USB SJ IS CLOSED ON
BACK OF BOARD.

CORE MATRIX TOP COLUMN DRIVERS

Q6 MMBT4403LT1G
Q7 MMBT4403LT1G
Q8 MMBT4403LT1G
Q9 MMBT4403LT1G
Q16 MMBT4401LT1G
Q17 MMBT4401LT1G
Q18 MMBT4401LT1G
Q19 MMBT4401LT1G

CORE MATRIX ROW DRIVERS

Q10 MMBT4403LT1G
Q11 MMBT4403LT1G
Q12 MMBT4403LT1G
Q13 MMBT4403LT1G
Q20 MMBT4401LT1G
Q21 MMBT4401LT1G
Q22 MMBT4401LT1G
Q23 MMBT4401LT1G

CORE MATRIX BOTTOM COLUMN DRIVERS

Q4 MMBT4403LT1G
Q5 MMBT4403LT1G
Q14 MMBT4401LT1G
Q15 MMBT4401LT1G

CORE MATRIX POWER

CORE MEMORY POWER

C9 470uF

SYSTEM POWER GROUND

CORE MATRIX WRITE ENABLE

N-CHNL FET as low-side switch

Rds(ON)=0.1

CORE MEMORY GROUND

Q3 Q_NMOS_DGS_NVTR4503NT1G

SYSTEM POWER GROUND

QxP (PNP) is normally high, low to activate matrix transistor.
QxN (NPN) is normally low, high to activate matrix transistor.

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Sheet: /Driver/
File: Core64C LB v0.2 Driver.sch

Title: Core64C – Core Matrix Driver

Size: A	Date: 2021-06-04	**Rev: 0.2**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 5/5