

# CORE64C INTERACTIVE CORE MEMORY LOGIC BOARD

Sheet: Power

File: Core64C LB v0.4 Power.sch

Sheet: Driver

File: Core64C LB v0.4 Driver.sch

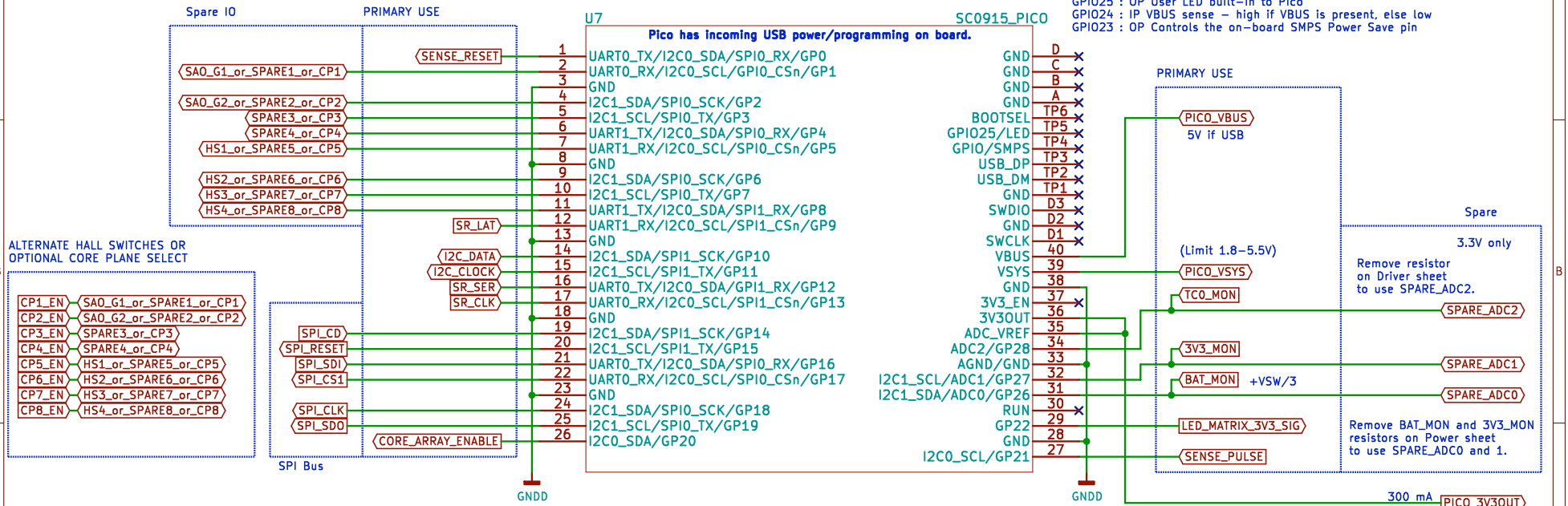
Sheet: Sense\_LEDs\_ID

File: Core64C LB v0.4 Sense\_LEDs\_ID.sch

Sheet: Expansion

File: Core64C LB v0.4 Expansion.sch

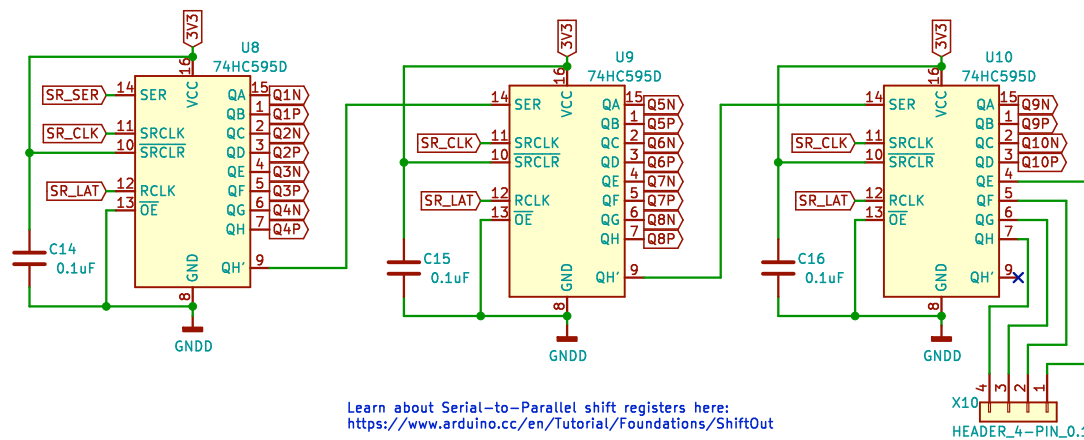
## RASPBERRY PI PICO RP2040 CONNECTIONS



QxN (NPN) is normally low, high to activate matrix transistor.

QxP (PNP) is normally high, low to activate matrix transistor.

## OUTPUT EXPANSION TO CORE MATRIX DRIVER



## SILKSCREEN FRONT

Interactive Core Memory  
 All logic is 3V3 Level

L1  
 Core\_64c\_Logo\_7mm\_tall  
 Core64c\_7mm

## SILKSCREEN BACK

Core 64 Logo  
 Interactive Core Memory  
 QR Code  
 Maker  
 Website  
 PCB Maker  
 Assembler  
 Serial Number  
 P/N  
 REV



L2  
 Core\_64c\_Logo\_7mm\_tall  
 Core64c\_7mm

All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

As released 2022-06-11

Visit [www.Core64.io](http://www.Core64.io) for information on assembly and optional features.

Concept and design by Andy Geppert © [www.MachineIdeas.com](http://www.MachineIdeas.com)

Sheet: /

File: Core64c LB v0.4.sch

**Title: Core64c – Main Sheet Index**

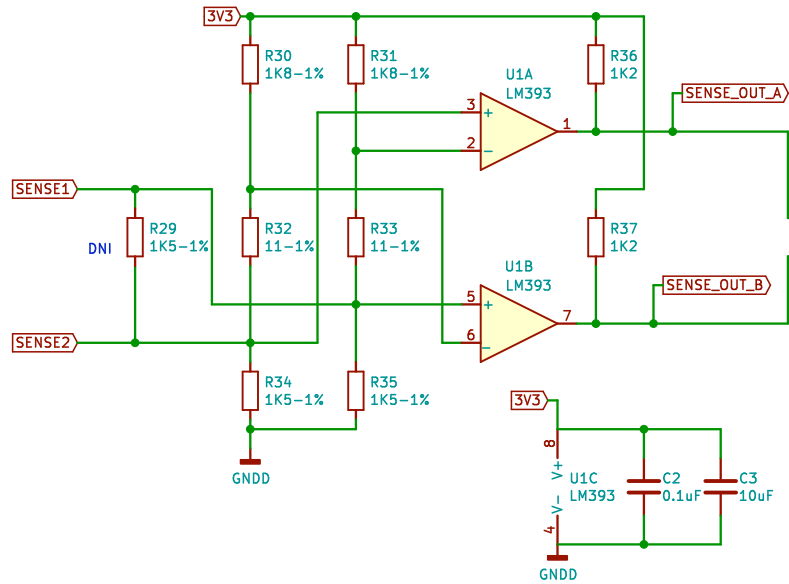
Size: A Date: 2022-06-11

KiCad E.D.A. kicad (5.1.2-1)-1

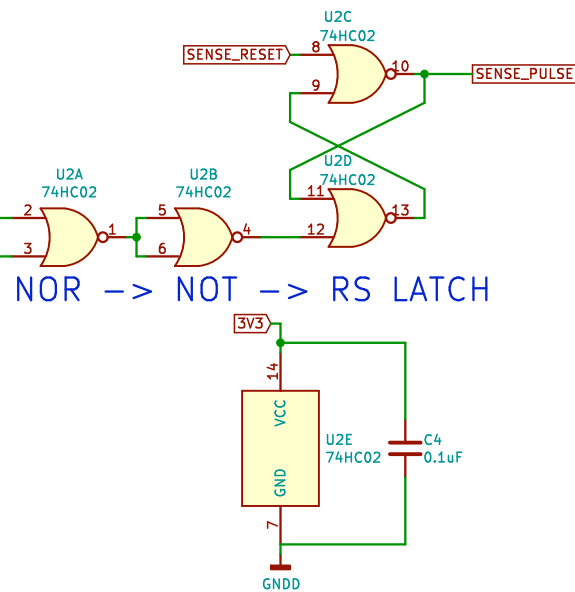
Rev: 0.4

Id: 1/5

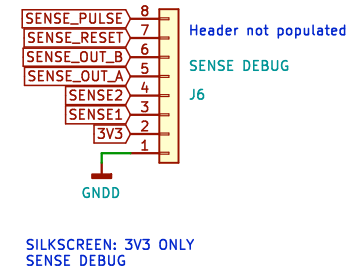
## SENSE SIGNAL DIFFERENTIAL AMPLIFIERS



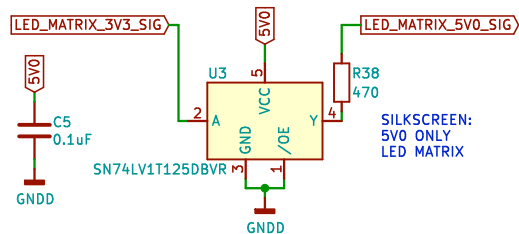
## SENSE SIGNAL LATCH



## SENSE DEBUG

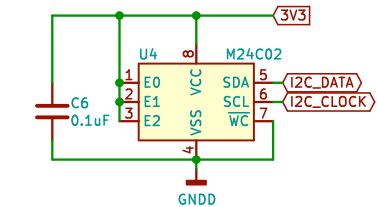


## LED MATRIX DRIVE AND LEVEL SHIFT



## BOARD ID AND S/N

EEPROM I2C ADDRESS: 0b1010111, 0x57 (87)



All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

As released 2022-06-11

Visit [www.Core64.io](http://www.Core64.io) for information on assembly and optional features.

Concept and design by Andy Geppert © [www.MachineIdeas.com](http://www.MachineIdeas.com)

Sheet: /Sense\_LEDs\_ID/

File: Core64C LB v0.4 Sense\_LEDs\_ID.sch

**Title: Core64C – Sense**

Size: A Date: 2022-06-11

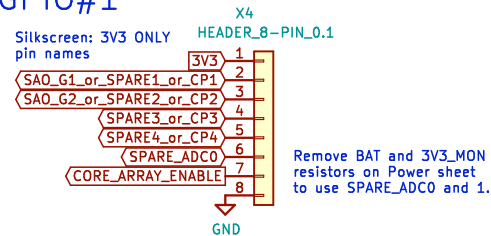
KiCad E.D.A. kicad (5.1.2-1)-1

Rev: 0.4

Id: 2/5

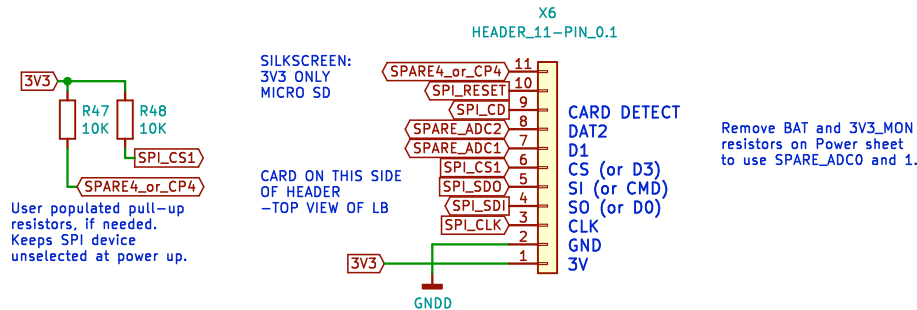
# EVERYTHING ON THIS SHEET IS USER-PROVIDED OPTIONAL ADD-ONS

## GPIO#1



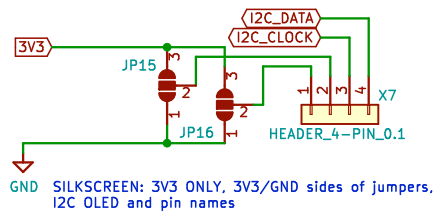
## GPIO#2, SPI, SD CARD

Compatible with MicroSD Card Adapter <https://www.adafruit.com/product/4682> (use pins 1-6, 9)

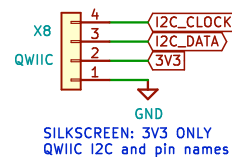


## OLED MONOCHROME I2C

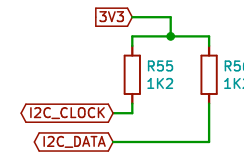
Generic 0.96" (128x64) or 1.5" (128x128)  
I2C 4-pins, often ADDRESS: 0x3C (60 decimal)  
Alternate is 0x3D, not 0x7A or 0x78 (wrong 8-bit)!  
Must choose power polarity by soldering SJS.



## QWIIC I2C



## I2C PULL-UPS



## I2C ADDRESS TABLE

INCLUDED:	
AMBIENT LIGHT SENSOR	0x29 (47)
HALL SENSOR 1	0x30 (48)
HALL SENSOR 2	0x31 (49)
HALL SENSOR 3	0x32 (50)
HALL SENSOR 4	0x33 (51)
EEPROM (BOARD ID)	0x57 (87)
OPTIONAL:	
OLED	0x3C (60)
AND1XOR IO Exp. MCP23017	0x20 (32)
AND1XOR EEPROM AT24C32r	0x50 (80)
NFC CLICK PN7120	0x50-53

All 7-bit addresses should be greater than 0x07 and less than 0x78 (120).

All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

As released 2022-06-11

Visit [www.Core64C.io](http://www.Core64C.io) for information on assembly and optional features.

Concept and design by Andy Geppert @ [www.MachineIdeas.com](http://www.MachineIdeas.com)

Sheet: /Expansion/

File: Core64C LB v0.4 Expansion.sch

**Title: Core64C - Expansion**

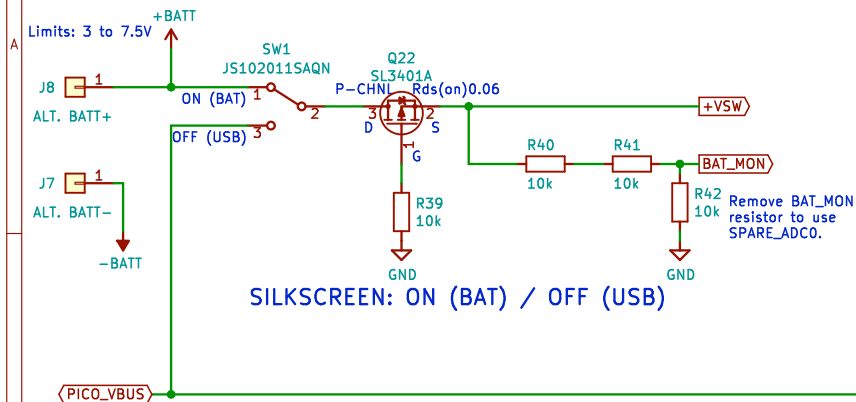
Size: A Date: 2022-06-11

KiCad E.D.A. kicad (5.1.2-1)-1

Rev: 0.4

Id: 3/5

## POWER SWITCH, REVERSE POLARITY PROTECTION, BATTERY VOLTAGE MONITOR



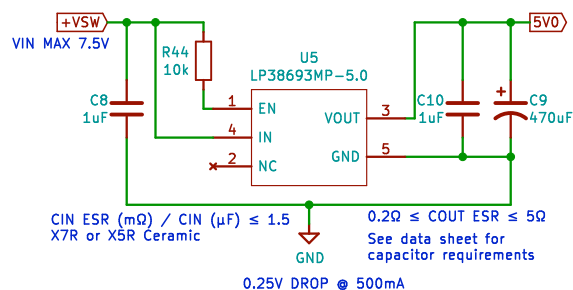
PICO\_VBUS is the USB voltage of the cable plugged into the PICO or the optional 1s LiPo charger (on LED Matrix Board) if the USB cable is plugged into the LiPo charger and the USB charge enable solder jumper is closed on the back of the LED Matrix board.

VBUS/VSYS: For more information see Raspberry Pi Pico Datasheet.

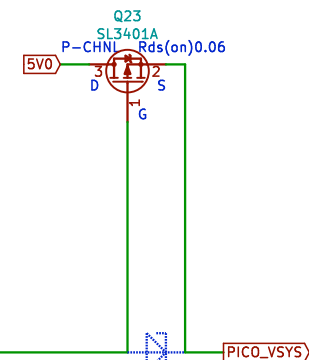
This diode is built-in to the Pico. It is shown here for clarity in the operational description below.

## 5V POWER SUPPLY

LED MATRIX, PICO, 3V3 REGULATOR, OPTIONAL ACCESSORIES



## PICO VUSB / VSYS AUTOMATIC "OR" SWITCH



## POWER PATH DESCRIPTION

TWO POWER INPUT SOURCES SELECTED BY SPDT SWITCH.

Power Switch ON (BAT), USB cable is NOT connected:  
P-FET (gate is low) conducts 5V0 (or less if the battery is less than about 5.2V) so that PICO\_SYS is powered. PICO\_VBUS is not energized because of built-in Zener diode on the Pico.

Power Switch OFF (USB), USB cable is NOT connected:  
System is off and does not receive power from the battery.

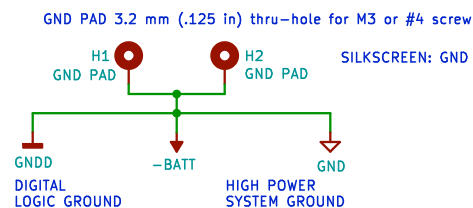
Power Switch ON (BAT), USB cable IS connected:  
If USB voltage is greater than 5V0, the Pico will operate with VSYS at the USB voltage. The rest of the system will operate from whatever the 5V0 rail voltage is. If USB voltage is less than 5V0, the Pico will operate with VSYS at 5V0 along with the rest of the system. The Pico diode prevents current flow from 5V0 back out through USB.

Power Switch OFF (USB), USB cable IS connected:  
The USB voltage will be greater than 5V0 (because there is a voltage drop through the 5V0 regulator). The P-FET will be off, the Pico will run at the USB voltage, the rest of the system will run at slightly less than the USB voltage.

## IMPORTANT NOTES

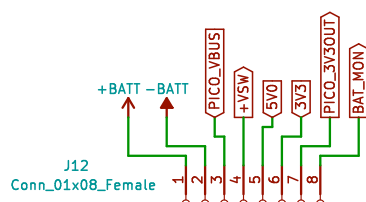
- 1) Battery pack absolute maximum voltage is 7.5V.
- 2) In Core64C, the battery is normally installed on the back of the LED Matrix and connects to the Logic Board through the lower right (second from bottom) pin (+BAT) in the 2x20 sockets.
- 3) The standard built-in battery pack is Keystone 2482 with 4X "AAA" primary/alkaline cells.
- 4) OK to use Energizer Ultimate Lithium (very light weight!) with combined open cell voltage of 7.2V. It will be <7V when there is a load on the cells.
- 5) If the 1s LiPo option is used on the LED Matrix, the LiPo battery voltage (3.7V nominal) is used and works down to about 3.1V, where the batteries built-in low voltage cutoff should kick in.

## ALL SYSTEM GROUND



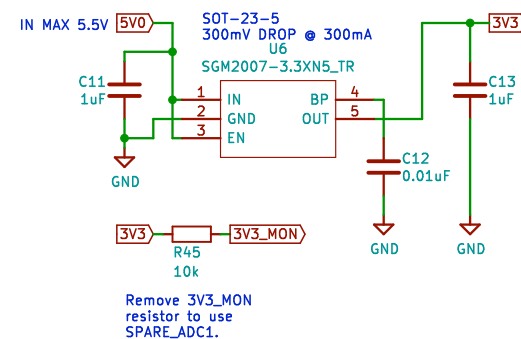
## POWER RAILS

SILKSCREEN: POWER



## 3.3V POWER SUPPLY

CORE MATRIX, OPTIONAL ACCESSORIES, ALL LOGIC



All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

As released 2022-06-11

Visit [www.Core64.io](http://www.Core64.io) for information on assembly and optional features.

Concept and design by Andy Geppert @ [www.MachineIdeas.com](http://www.MachineIdeas.com)

Sheet: /Power/

File: Core64C LB V0.4 Power.sch

**Title: Core64C - Power Schematic**

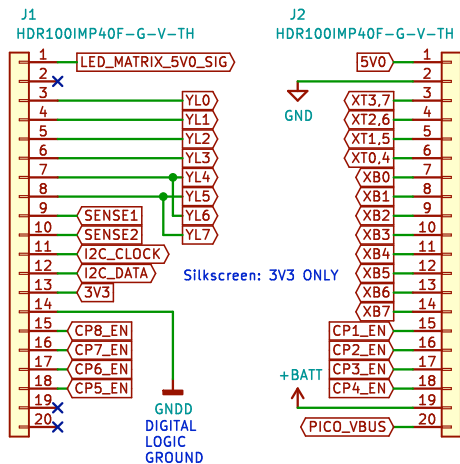
Size: A Date: 2022-06-11

KiCad E.D.A. kicad (5.1.2-1)-1

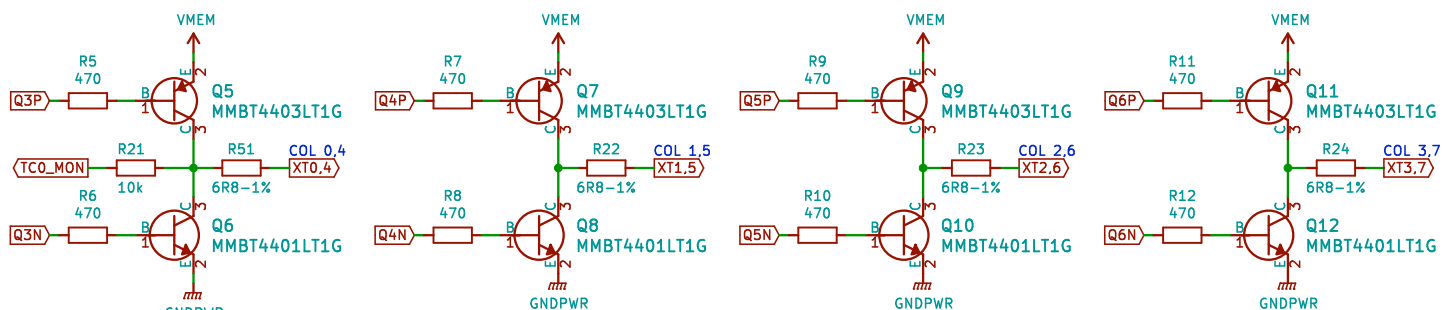
Rev: 0.4

Id: 4/5

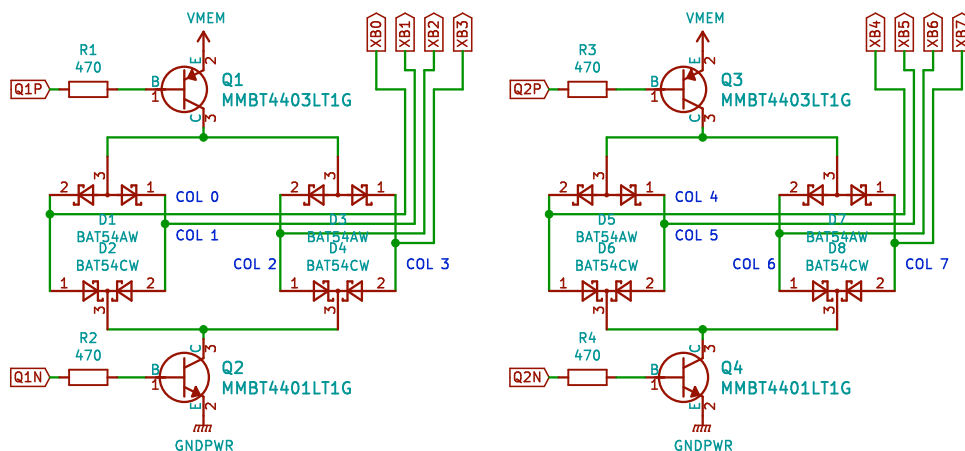
## CORE BOARD INTERCONNECTS



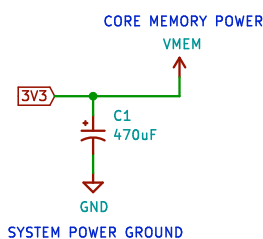
## CORE MATRIX TOP COLUMN DRIVERS



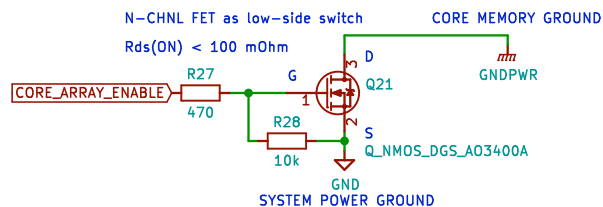
## CORE MATRIX BOTTOM COLUMN DRIVERS



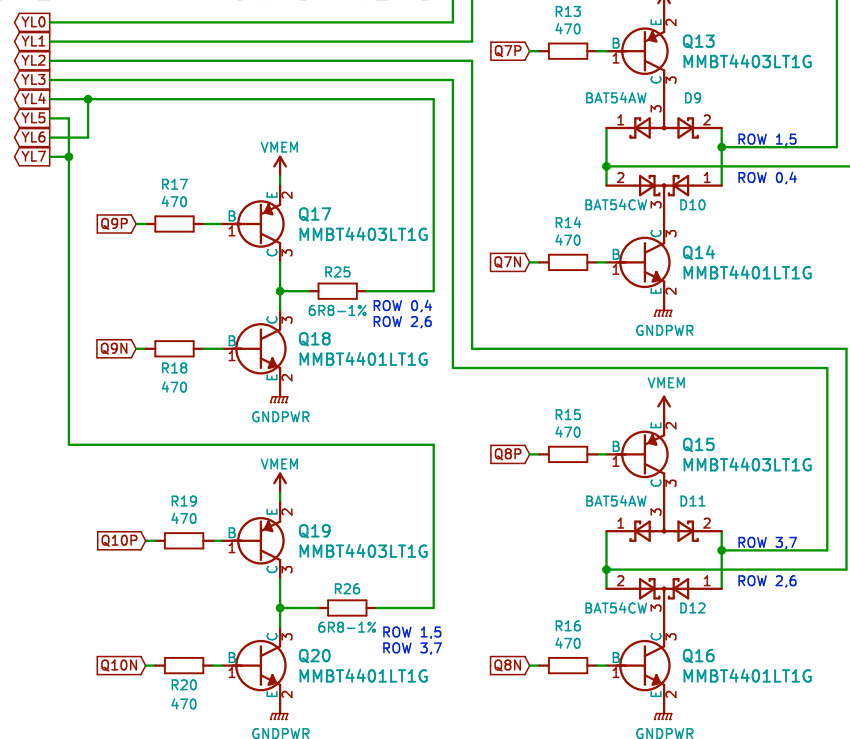
## CORE MATRIX POWER



## CORE MATRIX WRITE ENABLE



## CORE MATRIX ROW DRIVERS



All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

As released 2022-06-11

Visit [www.Core64.io](http://www.Core64.io) for information on assembly and optional features.

Concept and design by Andy Geppert © [www.MachineIdeas.com](http://www.MachineIdeas.com)

Sheet: /Driver/

File: Core64C LB v0.4 Driver.sch

**Title: Core64C - Core Matrix Driver**

Size: A Date: 2022-06-11

KiCad E.D.A. kicad (5.1.2-1)-1

Rev: 0.4

Id: 5/5

QxP (PNP) is normally high, low to activate matrix transistor.  
QxN (NPN) is normally low, high to activate matrix transistor.