POWER SUPPLY

BATTERY POWER INPUT 3.0 to 7.5V MAX!

(1) PRIMARY: LED ARRAY BOARD BATTERY
+LABB, −LABB, +BATT, PWR_FLAG

(2) ALT: LOGIC BOARD BATTERY
J3 Conn_1x02, −BATT

5V0 REGULATOR

LED ARRAY, MCU, 3V3 REGULATOR, OPTIONAL ACCESSORIES

SYS_CUR_MON, +VSW, JP15, R45 4K7, C5 1uF
VIN MAX 7.5V
0.25V DROP @ 500mA
U6 LP38693MP-5.0
EN, IN, NC, VOUT, GND
5V0_CUR_MON, JP16, 5V0, C6 1uF, C7 C8 C9 220uF 220uF 220uF
CIN ESR (mΩ) / CIN (µF) ≤ 1.5
X7R or X5R Ceramic
0.2Ω ≤ COUT ESR ≤ 5Ω
See data sheet for capacitor requirements
GND

3V3 REGULATOR

CORE MATRIX, OPTIONAL ACCESSORIES, ALL LOGIC

VIN MAX 5.5V, C10 1uF
SOT-23-5
300mV DROP @ 300mA
U7 SSP9193-33M5R
IN, GND, EN, BP, OUT
3V3, JP17 3V3_CUR_MON, C11 0.01uF, C12 1uF
GND GND

POWER SWITCH RPP

ON (BAT) M1
OFF (USB) M2
SW1 SK12D07L4B
Q22 SL3401A
REVERSE POLARITY PROTECTION
P-CHNL Rds(on)0.06
R44 4K7
GND

USB POWER INPUT 5V

(3) ALT: USB POWER LED ARRAY BOARD LIPO CHARGE MANAGER
5VUSB, 5VUSB
JP14 VBUS_5VUSB_TIE

SYSTEM GROUNDS

GND PAD 3.2 mm (.125 in) thru-hole for M3 or #4 screw
H1 GND PAD, PWR_FLAG, H2 GND PAD
GNDD DIGITAL LOGIC GROUND
−BATT
GND HIGH POWER SYSTEM GROUND

CORE MATRIX POWER

PWR_FLAG, VMEM, 3V3
C13 220uF, C14 220uF, C15 220uF
GND

PICO VBUS/VSYS "OR" SWITCH

Rds(on)0.06 P-CHNL Q23 SL3401A
If Pico is not used, disregard the circuit in dashed line section.

(4) ALT: USB POWER PICO USB PORT
PICO_VBUS, 5VUSB, PWR_FLAG, PICO_VSYS, (Limit 1.8–5.5V)
PICO USB PORT PROVIDES POWER TO PICO_VBUS.
For more information on VBUS/VSYS see the Raspberry Pi Pico Datasheet.
This diode is built-in to the Pico.

RASPBERRY PI PICO (PART 2 OF 2)

PICO USB PORT CONNECTED TO ALL PICO GROUNDS.

PICO VBUS BACKFLOW PREVENTER

GNDD

There are four ways to supply power to the system.
For more information on the power management see the Core64 User Guide.

* PWR_FLAG is a KiCAD formality.

LED ARRAY DRIVE VOLTAGE LEVEL SHIFT

5V0, PWR_FLAG, C16 0.1uF, GNDD
U8 SN74LV1T125DBVR
LED_ARY_5V0_SIG, R46 470, LED_ARY_3V3_SIG

CORE MATRIX SENSE

SENSE SIGNAL DIFFERENTIAL AMPLIFIERS

3V3, R48 1K8-1%, R51 1K8-1%, R54 4K7
U9A LM393
CM_SENSE_1_IN, TP20 S1 IN, R47 1K5-1%, DNI, R49 11-1%, R52 11-1%, R55 4K7
CA_SENSE_2_OUT, CA_SENSE_1_OUT
U9B LM393
CM_SENSE_2_IN, TP21 S2 IN, R50 1K5-1%, R53 1K5-1%
GNDD

SENSE SIGNAL OUTPUT LATCH

CM_SENSE_2_IN, CM_SENSE_1_IN
CM_SENSE_RESET, U10C 74HC02, CM_SENSE_PULSE
NOR -> NOT
U10A 74HC02, U10B 74HC02, U10D 74HC02
S2 OUT TP22, S1 OUT TP23
[OR] -> RS LATCH
U9C LM393, C17 0.1uF, C18 10uF
U10E 74HC02, C19 0.1uF

CORE MATRIX DRIVER

QxN (NPN) is normally low, high to activate matrix transistor. QxP (PNP) is normally high, low to activate matrix transistor.

CORE MATRIX ROW DRIVERS

LED_ARY_5V0_SIG
VMEM, R13 470, CM_Q7P, Q13 MMBT4403LT1G, ROW 0.4
BAT54AW D9, BAT54CW D10, ROW 1.5
R14 470, CM_Q7N, Q14 MMBT4401LT1G, GMEM
R15 470, CM_Q8P, Q15 MMBT4403LT1G
BAT54AW D11, ROW 2.6
BAT54CW D12, ROW 3.7
R16 470, CM_Q8N, Q16 MMBT4401LT1G
R17 470, CM_Q9P, Q17 MMBT4403LT1G
R25 8R2-1%, ROW 0.4, ROW 2.6
R18 470, CM_Q9N, Q18 MMBT4401LT1G
R19 470, CM_Q10P, Q19 MMBT4403LT1G
R26 8R2-1%, ROW 1.5, ROW 3.7
R20 470, CM_Q10N, Q20 MMBT4401LT1G

CORE MATRIX TOP COLUMN DRIVERS

R5 470, CM_Q3P, Q5 MMBT4403LT1G
R21 8R2-1%
R6 470, CM_Q3N, Q6 MMBT4401LT1G
R7 470, CM_Q4P, Q7 MMBT4403LT1G
COL 1,5, R22 8R2-1%
R8 470, CM_Q4N, Q8 MMBT4401LT1G
R9 470, CM_Q5P, Q9 MMBT4403LT1G
R23 8R2-1%
R10 470, CM_Q5N, Q10 MMBT4401LT1G
R11 470, CM_Q6P, Q11 MMBT4403LT1G
COL 3,7, R24 8R2-1%
R12 470, CM_Q6N, Q12 MMBT4401LT1G

CORE MATRIX AND LED ARRAY BOARD INTERCONNECTS

LABB = LED ARRAY BOARD BATTERY, IF PRESENT.
Pixels 0–7, J1 HDR100IMP40F-G-V-TH
LED_ARY_5V0_SIG, USER1, YL0, YL1, YL2, YL3, YL4,6, YL5,7, CM_SENSE_1_IN, CM_SENSE_2_IN, I2C_3V3_SCL, I2C_3V3_SDA, 3V3, GPIO8_CP8_HS4, GPIO7_CP7_HS3, GPIO6_CP6_HS2, GPIO5_CP5_HS1, USER2, USER3
Pixels 56–63
XT0, XT1, XT2, XT3, XT4, XT5, XT6, XT7
XB0, XB1, XB2, XB3, XB4, XB5, XB6, XB7
Bits 63–56, J2 HDR100IMP40F-G-V-TH
5V0, −LABB, XT3,7, XT2,6, XT1,5, XT0,4, XB0, XB1, XB2, XB3, XB4, XB5, XB6, XB7, GPIO1_CP1_SAO1, GPIO2_CP2_SAO2, GPIO3_CP3_DC, GPIO4_CP4_CS2, +LABB, 5VUSB
Bits 7–0
{GPIO_CPS_BUS}

CORE MATRIX BOTTOM COLUMN DRIVERS

R1 470, CM_Q1P, Q1 MMBT4403LT1G
D1 BAT54AW, D3 BAT54AW, COL 0, COL 1, COL 2, COL 3
D2 BAT54CW, D4 BAT54CW
R2 470, CM_Q1N, Q2 MMBT4401LT1G, GMEM
R3 470, CM_Q2P, Q3 MMBT4403LT1G
D5 BAT54AW, D7 BAT54AW, COL 4, COL 5, COL 6, COL 7
D6 BAT54CW, D8 BAT54CW
R4 470, CM_Q2N, Q4 MMBT4401LT1G, GMEM
{GPIO_CPS_BUS}, {CM_TRANSISTOR_DRIVE_BUS}
Drive Transistor Current: 3.3/470=7mA

CORE MATRIX ENABLE

N-CHNL FET as low-side switch
Rds(ON)=0.1
CM_EN, R28 470, CORE_CURR_MON, JP3, GMEM, CORE MEMORY GROUND
Q21 Q_NMOS_DGS_AO3400A, R27 4K7, GND
{I2C_3V3_BUS}

HACKER PLAYGROUND

USER-PROVIDED OPTIONAL ADD-ONS
SEE CORE64 HACKER GUIDE

CM DRIVER IO EXPANDER

{I2C_3V3_BUS}, {GPIO_CPS_BUS}, {CM_TRANSISTOR_DRIVE_BUS}
CM_SENSE_PULSE, CM_SENSE_RESET, LED_ARY_3V3_SIG, CM_EN, {I2C_3V3_BUS}, {GPIO_CPS_BUS}

U3 74HC595D
CM_SR_SER1, CM_SR_CLK, CM_SR_LAT, CM_SR_OE, R29 4K7, C2 0.1uF
SER, SRCLK, SRCLR, RCLK, OE, GND, VCC
QA CM_Q1N, QB CM_Q1P, QC CM_Q2N, QD CM_Q2P, QE CM_Q3N, QF CM_Q3P, QG CM_Q4N, QH CM_Q4P, QH'
4K7 Pull-down to default OE active
GNDD

U4 74HC595D
CA_SR_SER2, CM_SR_CLK, CM_SR_LAT, CM_SR_OE, C3 0.1uF
QA CM_Q5N, QB CM_Q5P, QC CM_Q6N, QD CM_Q6P, QE CM_Q7N, QF CM_Q7P, QG CM_Q8N, QH CM_Q8P, QH'
{CA_SHIFT_REGISTER_BUS}

U5 74HC595D
CA_SR_SER3, CM_SR_CLK, CM_SR_LAT, CM_SR_OE, C4 0.1uF
QA CM_Q9N, QB CM_Q9P, QC CM_Q10N, QD CM_Q10P, QE CA_SR_GPO_E, QF CA_SR_GPO_F, QG CA_SR_GPO_G, QH CA_SR_GPO_H, QH'
Learn about Serial-to-Parallel shift registers here: https://www.arduino.cc/en/Tutorial/Foundations/ShiftOut

USER PORT A1

X3 DNI Conn_01x10_Female
I2C, LED ARRAY, CORE SENSE, CM ENABLE, CORE MATRIX DRIVE IO EXPANSION
I2C_3V3_SCL, I2C_3V3_SDA, LED_ARY_3V3_SIG, CM_SENSE_PULSE, CM_SENSE_RESET, CM_EN, CM_SR_SER1, CM_SR_CLK, CM_SR_LAT, CM_SR_OE

SPARE SR GPO

CA_SR_GPO_EFGH, X4
CA_SR_GPO_E, CA_SR_GPO_F, CA_SR_GPO_G, CA_SR_GPO_H
{CM_TRANSISTOR_DRIVE_BUS}

PICO MICROCONTROLLER

See Core64 User Manual for more detail on Pico and optional Pico W.

RASPBERRY PI PICO (PART 1 OF 2)

RP2040 PINS RESERVED FOR USE ON PICO BOARD:
GPIO29 : Input, used in ADC mode (ADC3) to measure VSYS/3 (approx. 5/3=1.667)
GPIO25 : Output, User LED built-in to Pico
GPIO24 : Input, VBUS sense – high if VBUS is present, else low
GPIO23 : Output, controls the on-board SMPS Power Save pin

U1 SC0915_PICO
Pico has incoming USB power/programming on board.
UART0_TX/I2C0_SDA/SPI0_RX/GP0, UART0_RX/I2C0_SCL/SPI0_CSn/GP1, GND, I2C1_SDA/SPI0_SCK/GP2, I2C1_SCL/SPI0_TX/GP3, UART1_TX/I2C0_SDA/SPI0_RX/GP4, UART1_RX/I2C0_SCL/SPI0_CSn/GP5, GND, I2C1_SDA/SPI0_SCK/GP6, I2C1_SCL/SPI0_TX/GP7, UART1_TX/I2C0_SDA/SPI1_RX/GP8, UART1_RX/I2C0_SCL/SPI1_CSn/GP9, GND, I2C1_SDA/SPI1_SCK/GP10, I2C1_SCL/SPI1_TX/GP11, UART0_TX/I2C0_SDA/SPI1_RX/GP12, UART0_RX/I2C0_SCL/SPI1_CSn/GP13, GND, I2C1_SDA/SPI1_SCK/GP14, I2C1_SCL/SPI1_TX/GP15, UART0_TX/I2C0_SDA/SPI0_RX/GP16, UART0_RX/I2C0_SCL/SPI0_CSn/GP17, GND, I2C1_SDA/SPI0_SCK/GP18, I2C1_SCL/SPI0_TX/GP19, I2C0_SDA/GP20
GND, GND, GND, GND, BOOTSEL, GPIO25/LED, GPIO/SMPS, USB_DP, USB_DM, GND, SWDIO, GND, SWCLK, VBUS, VSYS, GND, 3V3_EN, 3V3OUT, ADC_VREF, ADC2/GP28, AGND/GND, I2C1_SCL/ADC1/GP27, I2C1_SDA/ADC0/GP26, RUN, GP22, GND, I2C0_SCL/GP21
PICO_VBUS, PICO_VSYS, PICO_3V3OUT
PICO_3V3OUT is only used for ADC_VREF. Current is limited to 300 mA. Be careful if you use this.
ADC2 Default: GMEM
ADC1 Default: 3V3_MON
ADC0 Default: BAT_MON
LED_ARY_3V3_SIG, CM_SENSE_PULSE
GNDD

OLED COLOR SPI W/MICRO SD

Compatible: https://www.adafruit.com/product/1431
1.5" 128x128, 16-bit color w/MicroSD holder
OLED has 5V -> 3V3 regulator onboard.
MicroSD card standalone pins shared between TFT and OLED boards.

X5 DNI Conn_01x11_Female
COPI, CS OLED, CS SD, CIPO
SPI_SDO, SPI_CLK, GPIO3_CP3_DC, SPI_RESET, GPIO4_CP4_CS2, SPI_CS1, SPI_SDI, SPI_CD, 5V0
OLED ON THIS SIDE OF HEADER -TOP VIEW OF LB
SILKSCREEN: 3V3 Logic ONLY, 3V3/GND sides of jumpers, SPI OLED

{CA_SHIFT_REGISTER_BUS}, CM_EN, CM_SENSE_RESET, CM_SENSE_PULSE, LED_ARY_3V3_SIG, {I2C_3V3_BUS}, {GPIO_CPS_BUS}, {SPI_3V3_BUS}

SPI CHIP SELECT PULL-UPS

3V3, R34 4K7 DNI, R35 4K7 DNI
{GPIO_CPS_BUS}, {SPI_3V3_BUS}, SPI_CS1
+VSW, R36 4K7, R37 4K7, R38 4K7, JP8 BAT_MON, BVM, GND
JP10 VMEM, JP11 GMEM

USER PORT B1 POWER

−BATT, 3-7.5V MAX, +BATT
X71 Conn_01x07_Female DNI
5VUSB, +VSW, 5V0, 3V3, PICO_3V3OUT

USER PORT B2 GPIO/ANALOG

X72 Conn_01x07_Female DNI
GPIO5_CP5_HS1, GPIO6_CP6_HS2, GPIO7_CP7_HS3, GPIO8_CP8_HS4, ADC0, ADC1, ADC2

QWIIC I2C

3V3 ONLY
X9 Conn_4_QWIIC
I2C_3V3_SCL, I2C_3V3_SDA, 3V3, GND

I2C ADDRESS TABLE

AMBIENT PROX. SENSOR	0x38 (56)
OLED	0x3C (60)
AND!XOR IO Exp. MCP23017	0x20 (32)
AND!XOR EEPROM AT24C32r	0x50 (80)
NFC CLICK PN7120	0x50-53

I2C BUS INTERFACE

3V3, R30 1K2, R31 1K2
I2C_CLOCK, 68 R32, I2C_3V3_SCL
I2C_DATA, 68 R33, I2C_3V3_SDA
{I2C_3V3_BUS}

BOARD ID AND S/N

EEPROM I2C ADDRESS: 0b1010111, 0x57 (87)
U2 M24C02
E0, E1, E2, VSS, VCC, SDA, SCL, WC
I2C_3V3_SDA, I2C_3V3_SCL, C1 0.1uF, GNDD

I2C ADDRESS TABLE

All 7-bit addresses should be greater than 0x07 and less than 0x78 (120).
INCLUDED:

AMBIENT LIGHT SENSOR	0x29 (47)
HALL SENSOR 1	0x30 (48)
HALL SENSOR 2	0x31 (49)
HALL SENSOR 3	0x32 (50)
HALL SENSOR 4	0x33 (51)
EEPROM (BOARD ID)	0x57 (87)

SILKSCREEN FRONT

Interactive Core Memory
All logic is 3V3 Level

L1 Core_64c_Logo_7mm_tall Core64c_7mm
L4 MI LOGO Core64c_7mm

SILKSCREEN BACK

Core 64 Logo
Interactive Core Memory
QR Code
Maker
Website
PCB Maker
Assembler
Serial Number
P/N
REV

L2 Core_64c_Logo_7mm_tall Core64c_7mm

All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

Visit www.Core64.io for information on assembly and optional features.
Please read the Core64 User Guide for more details.
Concept and design by Andy Geppert © www.MachineIdeas.com

Sheet: /
File: Core64c LB.kicad_sch

Title: Core64c Logic Board – Raspberry Pi Pico W RP2040

Size: C	Date: 2024-07-07	Rev: 0.6
KiCad E.D.A. 8.0.4		Id: 1/1