POWER SUPPLY

BATTERY SWITCH RPP

REVERSE POLARITY PROTECTION

+V SWITCHED = 5V0

LED ARRAY, MCU, 3V3 REGULATOR, OPTIONAL ACCESSORIES

3V3 REGULATOR

CORE MATRIX, OPTIONAL ACCESSORIES, ALL LOGIC

J3 ALT. BATT. LIMIT BATTERY 3.0 TO 5.5V

+BATT PWR_FLAG ON (BAT) OFF (USB) SL3401A P-CHNL Rds(on)0.06 Q22 R44 10k SW1 SK12D07L4B

CORE16: flipped switch inputs so UP is ON when installed on PCB

* PWR_FLAG is a KiCAD formality.

+VSW NT11 NetTie_2 5V0 VIN MAX 5.5V

"Sys. Cur." System Current

CORE16: Removed 5V regulator. Kept Caps to keep LEDs stable with core pulsing loads on 3V3. This means incoming battery voltage must not exceed 5.5V per the 3V3 regulator spec sheet.

C7 220uF C8 220uF C9 220uF P-CHNL Rds(on)0.06 Q23 SL3401A C10 1uF

SOT-23-5 .3V DROP @300mA U7 SSP9193-33M5R IN GND EN BP OUT C11 0.01uF C12 1uF 3V3

If Pico is not used, ignore this FET, the VSYS, and VBUS rails.

USB POWER INPUT

5VUSB NT9 NetTie_2 PICO_VBUS PWR_FLAG

For more information on VBUS/VSYS see the Raspberry Pi Pico Datasheet.
For more information on the power management see the Core64 User Guide.

This diode is built-in to the Pico.

PICO_VSYS PWR_FLAG PICO_VSYS (Limit 1.8-5.5V)

RASPBERRY PI PICO (PART 2 OF 2)

PICO VBUS/VSYS "OR" SWITCH

POWER FLOW
MORE DETAIL IN CORE64 USER GUIDE

PRIMARY SWITCHED POWER SOURCES:
ON (BAT) : From battery on LED Array Board
OFF (USB) : From USB port on Pico

ALTERNATE/OPTIONAL SWITCHED POWER SOURCES:
ON (BAT) : From battery on Logic Board
OFF (USB) : From USB port of LiPo Charger on LED Array Board
* Requires closing USB Charge Enable solder jumper on the back of the LED Array Board. *

TWO POWER INPUT SOURCES SELECTED BY SPDT SWITCH.

Power Switch ON (BAT), USB cable is NOT connected:
P-FET (gate is low) conducts 5V0 (or less if the battery is less than about 5.2V) so that PICO_SYS is powered.
PICO_VBUS is not energized because of built-in Zener diode on the Pico.

Power Switch OFF (USB), USB cable is NOT connected:
System is off and does not receive power from the battery.

Power Switch ON (BAT), USB cable IS connected:
If USB voltage is greater than 5V0, the Pico will operate with VSYS at the USB voltage. The rest of the system will operate from whatever the 5V0 rail voltage is.
If USB voltage is less than 5V0, the Pico will operate with VSYS at 5V0 along with the rest of the system. The Pico diode prevents current flow from 5V0 back out through USB.

Power Switch OFF (USB), USB cable IS connected:
The USB voltage will be greater than 5V0 (because there is a voltage drop through the 5V0 regulator). The P-FET will be off, the Pico will run at the USB voltage, the rest of the system will run at slightly less than the USB voltage.

SYSTEM GROUNDS

Core16: Removed large ground rings.

PWR_FLAG GNDD DIGITAL LOGIC GROUND -BATT GND HIGH POWER SYSTEM GROUND

CORE MATRIX POWER

"VMEM" 3V3 CORE MEMORY PWR_FLAG NT10 VMEM CM_CUR_MON C13 C14 C15 220uF 220uF 220uF "VMEM" 3V3 CORE MEMORY

Core16: Moved LED driver to lower left sheet.

CORE MATRIX SENSE

SENSE SIGNAL DIFFERENTIAL AMPLIFIERS

SENSE SIGNAL OUTPUT LATCH

CM_SENSE_1_IN CM_SENSE_2_IN R48 1K8-1% R51 1K8-1% R54 1K2 R47 1K5-1% DNI R49 11-1% R52 11-1% R55 1K2 R50 1K5-1% R53 1K5-1% U9A LM393 U9B LM393 CA_SENSE_2_OUT CA_SENSE_1_OUT

SILKSCREEN: 3V3 ONLY SENSE DEBUG

U10A SN74HC02DR U10B SN74HC02DR U10C SN74HC02DR U10D SN74HC02DR U10E SN74HC02DR CM_SENSE_RESET CM_SENSE_PULSE

NOR -> NOT -> RS LATCH

U9C LM393 C17 0.1uF C18 10uF C19 0.1uF

CORE MATRIX DRIVER

CORE MATRIX ROW DRIVERS

QxN (NPN) is normally low, high to activate matrix transistor. QxP (PNP) is normally high, low to activate matrix transistor.

VMEM CM_Q7P R13 470 Q13 MMBT4403LT1G BAT54AW D10 ROW 0,2 BAT54CW D9 ROW 1,3 CM_Q7N R14 470 Q14 MMBT4401LT1G GMEM

Core16: Removed 2x transistors and diodes from horizontal drive.

Core16: Removed net-ties and core column 0 / row 0 voltage monitors.

CORE MATRIX TOP COLUMN DRIVERS

CM_Q3P R5 470 Q5 MMBT4403LT1G COL 0 6R8-5% R21 CM_Q3N R6 470 Q6 MMBT4401LT1G GMEM

CM_Q4P R7 470 Q7 MMBT4403LT1G COL 1 6R8-5% R22 CM_Q4N R8 470 Q8 MMBT4401LT1G GMEM

CM_Q5P R9 470 Q9 MMBT4403LT1G COL 2 6R8-5% R23 CM_Q5N R10 470 Q10 MMBT4401LT1G GMEM

CM_Q6P R11 470 Q11 MMBT4403LT1G COL 3 6R8-5% R24 CM_Q6N R12 470 Q12 MMBT4401LT1G GMEM

CORE MATRIX

Core_Memory_4x4_Matrix_Front_Facing CM1 Pixels 0-3 Pixels 12-15 Bits 15-12 Bits 3-0 XT0 XT1 XT2 XT3 YL0 YL1 YL2 YL3 YR0 YR1 YR2 YR3 YL0,2 YL1,3 CM_SENSE_2_IN CM_SENSE_1_IN XB0 XB1 XB2 XB3

CM_Q9P R17 470 Q17 MMBT4403LT1G ROW 0,2 R25 6R8-5% CM_Q9N R18 470 Q18 MMBT4401LT1G GMEM

CM_Q10P R19 470 Q19 MMBT4403LT1G ROW 1,3 R26 6R8-5% CM_Q10N R20 470 Q20 MMBT4401LT1G GMEM

Core16: Removed stacked headers.

Core16: Removed battery access along with the stacked headers.

CORE MATRIX BOTTOM COLUMN DRIVERS

CM_Q1P R1 470 Q1 MMBT4403LT1G D2 BAT54AW BAT54AW D4 COL 0 COL 1 COL 2 COL 3 D1 BAT54CW BAT54CW D3 CM_Q1N R2 470 Q2 MMBT4401LT1G GMEM

Drive Transistor Current: 3.3/470=7mA

Core16: Reorganized QxP and QxN to be 1-8 instead of intermittent to 12.

Core16: Removed test points.

Core16: Removed 2x transistors and diodes from vertical drive.

Core16: Organize transistor and resistor ref. des. numbers CCW from lower left. The six current limiting resistors are 21-26.

CORE MATRIX ENABLE

N-CHNL FET as low-side switch Rds(ON)=0.1

CM_EN R28 470 NT5 GMEM_MON Q21 R27 10k NVTR4503NT1G_NMOS_GSD "GMEM" GROUND CORE MEMORY

RGB LED MATRIX AND HALL SENSOR BUTTONS

HALL SENSORS

SILKSCREEN: 0x30 SILKSCREEN: 0x31 SILKSCREEN: 0x32 SILKSCREEN: 0x33

I2C_3V3_SDA I2C_3V3_SCL {I2C_3V3_BUS}

U11 SI7210-B-00-IV R101 10K C20 0.1uF U12 SI7210-B-02-IV R102 10K C21 0.1uF U13 SI7210-B-03-IV R103 10K C22 0.1uF U14 SI7210-B-04-IV R104 10K C23 0.1uF

GNDD DIGITAL LOGIC GROUND

I2C configurable hall sensors, not just a switch.
Silicon Labs SI7210-B-xx-IV (00, 02, 03, 04)
Low (push-pull) up to 20 mT, SOT23-5
Recommended sensitivity ± (N and S) 3-7 mT (30-70 Gauss)

L3 Core_64_M-+S_Buttons_4mm

LED ARRAY DRIVE VOLTAGE LEVEL SHIFT

LED_ARY_5V0_SIG D21 D22 D23 D24 D25 D26 D27 D28 D29 D30 D31 D32 D33 D34 D35 D36 SK6812

PWR_FLAG C16 0.1uF U8 SN74LV1T125DBVR R46 470 LED_ARY_3V3_SIG

R36 10k R37 10k R38 10k B_M

On the bottom side: ADC0_BUFF ADC1_BUFF ADC2_BUFF ADC0 ADC1 ADC2 VMEM GMEM 1k2 R41 1k2 R42 1k2 R43

PICO MICROCONTROLLER

RASPBERRY PI PICO (PART 1 OF 2)

See Core64 User Manual for more detail on Pico and optional Pico W.

RP2040 PINS RESERVED FOR USE ON PICO BOARD:
GPIO29 : Input, used in ADC mode (ADC3) to measure VSYS/3 (approx. 5/3=1.667)
GPIO25 : Output, User LED built-in to Pico
GPIO24 : Input, VBUS sense - high if VBUS is present, else low
GPIO23 : Output, controls the on-board SMPS Power Save pin

PICO_3V3OUT is only used for ADC_VREF. Current is limited to 300 mA. Be careful if you use this.

U1 PICO Pico has incoming USB power/programming on board.

SILKSCREEN FRONT SILKSCREEN BACK

SPI AVAILABLE WHEN CORE MATRIX DISABLED.

HACKER PLAYGROUND

USER-PROVIDED OPTIONAL ADD-ONS
SEE CORE64 HACKER GUIDE

OLED MONOCHROME I2C

Connect via SAO.

Generic 0.96" (128x64) or 1.5" (128x128)
I2C 4-pins, often ADDRESS: 0x3C (60 decimal)
Alternate is 0x3D, not 0x7A or 0x78 (wrong 8-bit)!

SAO #1 SIMPLE ADD-ONS

SAO#2 is on the Core Board 3V3 ONLY I2C_3V3_SDA GPIO1_SAO1 GPIO2_SAO2 I2C_3V3_SCL X8 SAO_conn_SFH11-NBPC-D03-ST-BK

https://hackaday.io/project/175182-simple-add-ons-sao
using Sullins SFH11-NBPC-D03-ST-BK female header
https://www.digikey.com/product-detail/en/sullins-connector-solutions/SFH11-NBPC-D03-ST-BK/S9717-ND/4558818

QWIIC I2C

3V3 ONLY X9 QWIIC I2C_3V3_SCL I2C_3V3_SDA 3V3

I2C ADDRESS TABLE

OPTIONAL:

AMBIENT PROX. SENSOR	0x38 (56)
OLED	0x3C (60)
ANDIXOR IO Exp. MCP23017	0x20 (32)
ANDIXOR EEPROM AT24C32r	0x50 (80)
NFC CLICK PN7120	0x50-53

BOARD ID AND S/N

EEPROM I2C ADDRESS: 0b1010111, 0x57 (87)

U2 M24C02-RMN C1 0.1uF

I2C ADDRESS TABLE

All 7-bit addresses should be greater than 0x07 and less than 0x78 (120).

INCLUDED:

AMBIENT LIGHT SENSOR	0x29 (47)
HALL SENSOR 1	0x30 (48)
HALL SENSOR 2	0x31 (49)
HALL SENSOR 3	0x32 (50)
HALL SENSOR 4	0x33 (51)
EEPROM (BOARD ID)	0x57 (87)

I2C BUS INTERFACE

3V3 R30 1K2 R31 1K2 I2C_CLOCK I2C_DATA 68 R32 68 R33 I2C_3V3_SCL I2C_3V3_SDA {I2C_3V3_BUS}

Core16 Core64 Logo

All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.
As prototyped
Visit www.Core64.io for information on assembly and optional features.
Please read the Core64 User Guide for more details.
Concept and design by Andy Geppert @ www.MachineIdeas.com

Sheet: /
File: Core16_LB.kicad_sch

Title: Core16 Logic Board

Size: C	Date: 2023-08-27	**Rev: 0.1**
KiCad E.D.A. kicad (7.0.0-0)		Id: 1/1