

# POWER SUPPLY

## BATTERY

## SWITCH

## RPP

REVERSE  
POLARITY  
PROTECTION

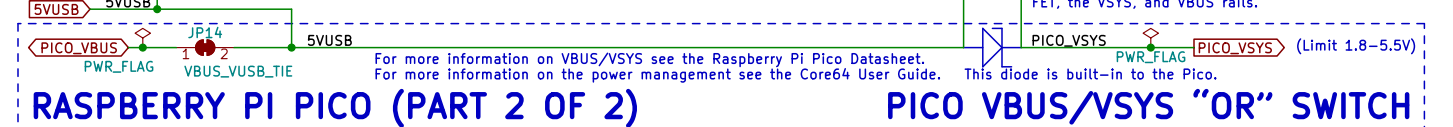
## 5V0 REGULATOR

LED ARRAY, MCU, 3V3 REGULATOR, OPTIONAL ACCESSORIES

## 3V3 REGULATOR

CORE MATRIX, OPTIONAL ACCESSORIES, ALL LOGIC

## USB POWER INPUT



## POWER FLOW

## MORE DETAIL IN CORE64 USER GUIDE

PRIMARY SWITCHED POWER SOURCES:  
ON (BAT) : From battery on LED Array Board  
OFF (USB) : From USB port on Pico

ALTERNATE/OPTIONAL SWITCHED POWER SOURCES:  
ON (BAT) : From battery on Logic Board  
OFF (USB) : From USB port of LiPo Charger on LED Array Board  
\* Requires closing USB Charge Enable solder jumper on the back of the LED Array Board.\*

TWO POWER INPUT SOURCES SELECTED BY SPDT SWITCH.

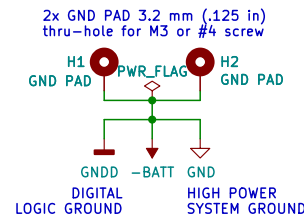
Power Switch ON (BAT), USB cable is NOT connected:  
P-FET (gate is low) conducts 5V0 (or less if the battery is less than about 5.2V) so that PICO\_SYS is powered.  
PICO\_VBUS is not energized because of built-in Zener diode on the Pico.

Power Switch OFF (USB), USB cable is NOT connected:  
System is off and does not receive power from the battery.

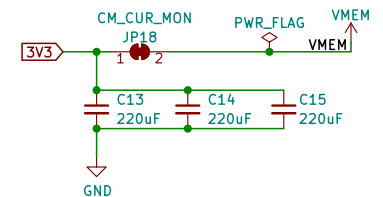
Power Switch ON (BAT), USB cable IS connected:  
If USB voltage is greater than 5V0, the Pico will operate with VSYS at the USB voltage. The rest of the system will operate from whatever the 5V0 rail voltage is.  
If USB voltage is less than 5V0, the Pico will operate with VSYS at 5V0 along with the rest of the system. The Pico diode prevents current flow from 5V0 back out through USB.

Power Switch OFF (USB), USB cable IS connected:  
The USB voltage will be greater than 5V0 (because there is a voltage drop through the 5V0 regulator). The P-FET will be off, the Pico will run at the USB voltage, the rest of the system will run at slightly less than the USB voltage.

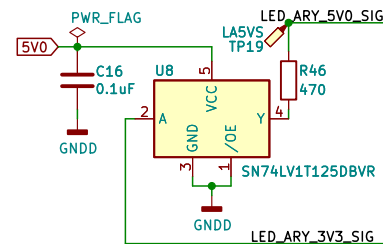
## SYSTEM GROUNDS



## CORE MATRIX POWER



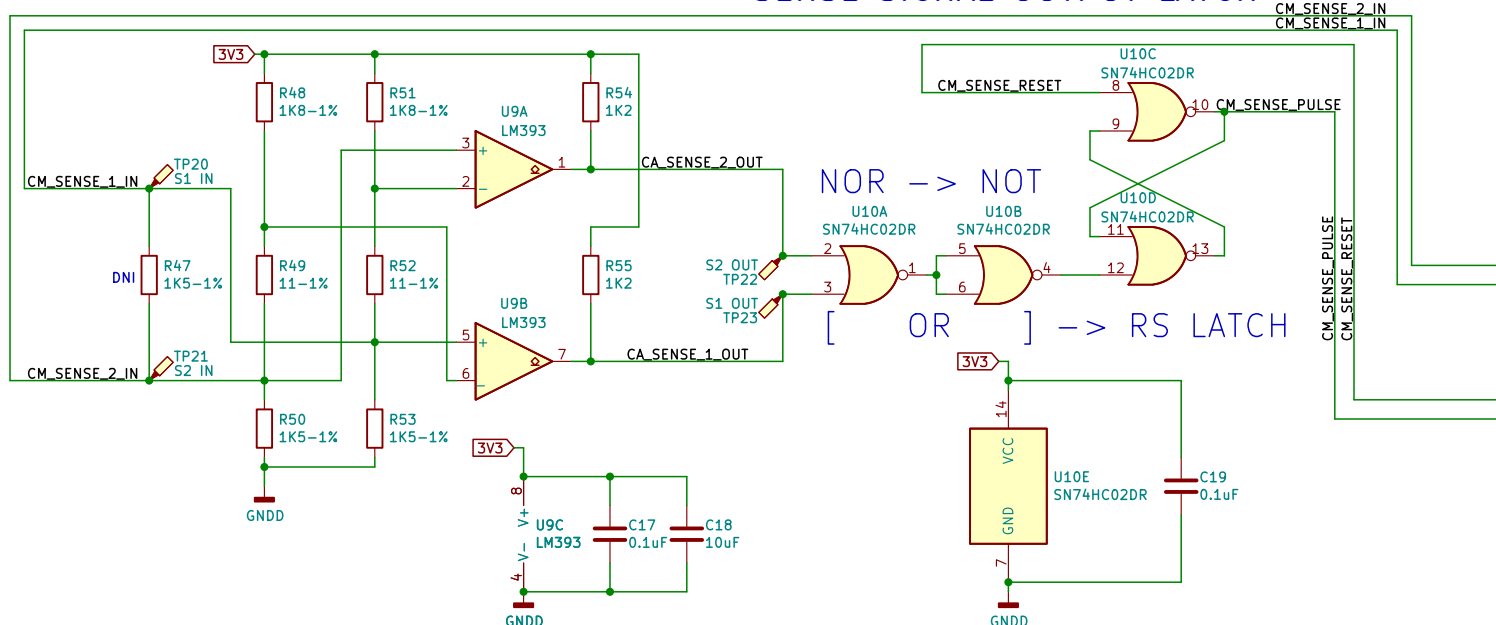
## LED ARRAY DRIVE VOLTAGE LEVEL SHIFT



# CORE MATRIX SENSE

## SENSE SIGNAL DIFFERENTIAL AMPLIFIERS

## SENSE SIGNAL OUTPUT LATCH



## CORE MATRIX ROW DRIVERS

# CORE MATRIX DRIVER

QxN (NPN) is normally low, high to activate matrix transistor.

QxP (PNP) is normally high, low to activate matrix transistor.

## CORE MATRIX TOP COLUMN DRIVERS

## CORE MATRIX AND LED ARRAY BOARD INTERCONNECTS

## CORE MATRIX BOTTOM COLUMN DRIVERS

## CORE MATRIX ENABLE

N-CHNL FET as low-side switch  
Rds(ON)=0.1

CORE MEMORY  
GROUND

## BATTERY

Limit: 3-7.5V

5VUSB

5V0

-BATT

GPIO1 CP1 SA01

GPIO2 CP2 SA02

GPIO3 CP3 DC

GPIO4 CP4 CS2

GPIO5 CP5 HS1

GPIO6 CP6 HS2

GPIO7 CP7 HS3

GPIO8 CP8 HS4

GPIO9 CP9 HS5

GPIO10 CP10 HS6

GPIO11 CP11 HS7

GPIO12 CP12 HS8

GPIO13 CP13 HS9

GPIO14 CP14 HS10

GPIO15 CP15 HS11

GPIO16 CP16 HS12

GPIO17 CP17 HS13

GPIO18 CP18 HS14

GPIO19 CP19 HS15

GPIO20 CP20 HS16

GPIO21 CP21 HS17

GPIO22 CP22 HS18

GPIO23 CP23 HS19

GPIO24 CP24 HS20

GPIO25 CP25 HS21

GPIO26 CP26 HS22

GPIO27 CP27 HS23

GPIO28 CP28 HS24

GPIO29 CP29 HS25

GPIO30 CP30 HS26

GPIO31 CP31 HS27

GPIO32 CP32 HS28

GPIO33 CP33 HS29

GPIO34 CP34 HS30

GPIO35 CP35 HS31

GPIO36 CP36 HS32

GPIO37 CP37 HS33

GPIO38 CP38 HS34

GPIO39 CP39 HS35

GPIO40 CP40 HS36

GPIO41 CP41 HS37

GPIO42 CP42 HS38

GPIO43 CP43 HS39

GPIO44 CP44 HS40

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GPIO46 CP46 HS42

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GPIO186 CP186 HS182

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GPIO212 CP212 HS208

GPIO213 CP213 HS209

GPIO214 CP214 HS210

GPIO215 CP215 HS211

GPIO216 CP216 HS212

GPIO217 CP217 HS213

GPIO218 CP218 HS214

GPIO219 CP219 HS215

GPIO220 CP220 HS216

GPIO221 CP221 HS217

GPIO222 CP222 HS218

GPIO223 CP223 HS219

GPIO224 CP224 HS220

GPIO225 CP225 HS221

GPIO226 CP226 HS222

GPIO227 CP227 HS223

GPIO228 CP228 HS224

GPIO229 CP229 HS225

GPIO230 CP230 HS226

GPIO231 CP231 HS227

GPIO232 CP232 HS228

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GPIO234 CP234 HS230

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GPIO246 CP246 HS242

GPIO247 CP247 HS243

GPIO248 CP248 HS244

GPIO249 CP249 HS245

GPIO250 CP250 HS246

GPIO251 CP251 HS247

GPIO252 CP252 HS248

GPIO253 CP253 HS249

GPIO254 CP254 HS250

GPIO255 CP255 HS251

GPIO256 CP256 HS252

GPIO257 CP257 HS253

GPIO258 CP258 HS254

## {I2C, 3V3, BUS}

OPTIONAL:	
AMBIENT PROX. SENSOR	0x38 (56)
OLED	0x3C (60)
AND!XOR IO Exp. MCP23017	0x20 (32)
AND!XOR EEPROM AT24C32r	0x50 (80)
NFC CLICK PN7120	0x50-53

<https://hackaday.io/project/175182-simple-add-ons-sao>  
using Sullins SFH11-NBPC-D03-ST-BK female header  
<https://www.digikey.com/product-detail/en/sullins-connector-solutions/SFH11-NBPC-D03-ST-BK/59717-ND/4558818>

# CM DRIVER IO EXPANDER

## PICO MICROCONTROLLER

See Core64 User Manual for more detail on Pico and optional Pico W.

## RASPBERRY PI PICO (PART 1 OF 2)

RP2040 PINS RESERVED FOR USE ON PICO BOARD:  
GPIO29 : Input, used in ADC mode (ADC3) to measure VSYS/3 (approx. 5/3=1.667)  
GPIO25 : Output, User LED built-in to Pico  
GPIO24 : Input, VBUS sense - high if VBUS is present, else low  
GPIO23 : Output, controls the on-board SMPS Power Save pin

PICO\_3V3OUT is only used for ADC\_VREF. Current is limited to 300 mA. Be careful if you use this.

SILKSCREEN FRONT

SILKSCREEN BACK



All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

Visit [www.Core64.io](http://www.Core64.io) for information on assembly and optional features.  
Please read the Core64 User Guide for more details.

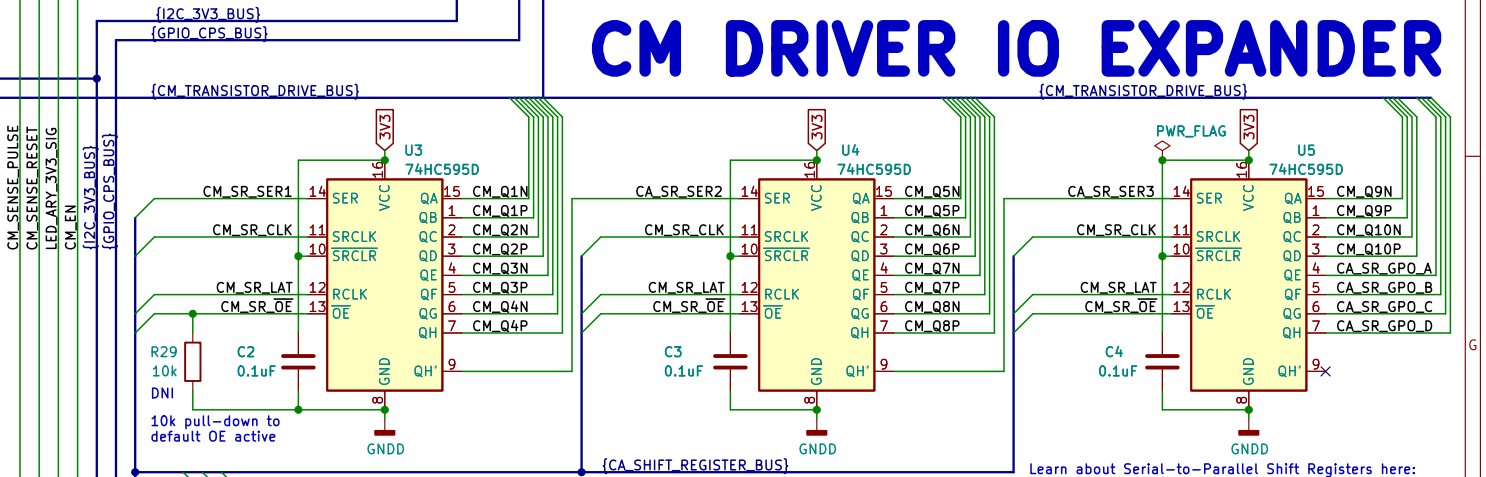
Concept and design by Andy Geppert © [www.MachineIdeas.com](http://www.MachineIdeas.com)

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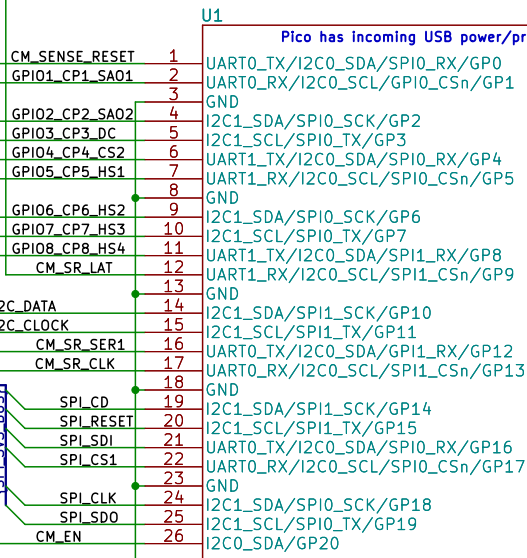
**Title: Core64 Logic Board - Raspberry Pi Pico RP2040**

Size: C Date: 2023-03-19  
KiCad E.D.A. eeschema (6.0.7-1)-1

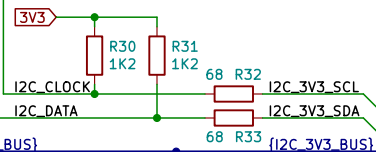
Rev: 0.8  
Id: 1/1



Learn about Serial-to-Parallel Shift Registers here:  
<https://www.arduino.cc/en/Tutorial/Foundations/ShiftOut>



### I2C BUS INTERFACE



### BOARD ID AND S/N

EEPROM I2C ADDRESS: 0b1010111, 0x57 (87)

### I2C ADDRESS TABLE

All 7-bit addresses should be greater than 0x07 and less than 0x78 (120).  
INCLUDED:  
AMBIENT LIGHT SENSOR 0x29 (47)  
HALL SENSOR 1 0x30 (48)  
HALL SENSOR 2 0x31 (49)  
HALL SENSOR 3 0x32 (50)  
HALL SENSOR 4 0x33 (51)  
EEPROM (BOARD ID) 0x57 (87)

