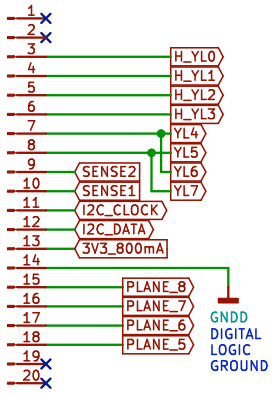
CORE MATRIX

Cut header 36-pin into two 16-pin headers, install centered with two pins on each end not inserted.

Required 12 pins

SILKSCREEN:
LSIG
USR1
YL0
YL1
YL2
YL3
YL4,6
YL5,7
SEN2
SEN1
SCL
SDA
3V3
GNDD
CP8
CP7
CP6
CP5
USR2
USR3

J1 929834-04-36-RK



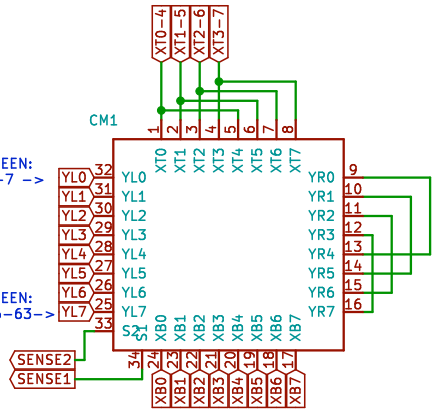
CM1

SILKSCREEN:
Pixel 0-7 ->

SILKSCREEN:
Pixel 56-63->

SILKSCREEN:
<-bit 63-56

SILKSCREEN:
<-bit 7-0

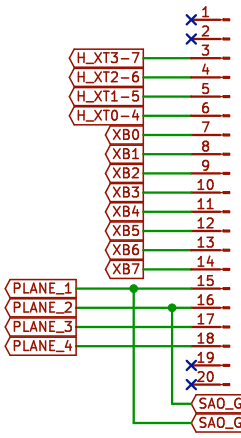


Core_Memory_8x8_Array_Front_Facing

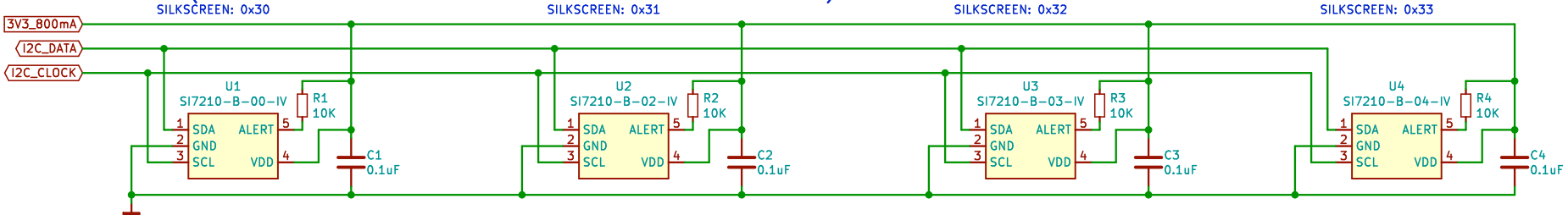
929834-04-36-RK J2

SILKSCREEN:
5V0
GND
XT3,7
XT2,6
XT1,5
XT0,4
XB0
XB1
XB2
XB3
XB4
XB5
XB6
XB7
P1G1
P2G2
CP3
CP4
+BATT
5VUSB

Required 14 pins



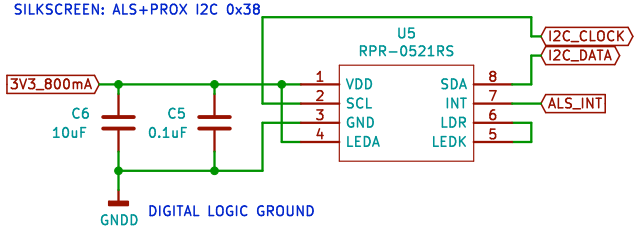
HALL SENSORS (SEE SECOND SHEET FOR HALL SWITCH ALTERNATES)



I2C configurable hall sensors, not just a switch.
Silicon Labs SI7210-B-xx-IV (00, 02, 03, 04)
Low (push-pull) up to 20 mT, SOT23-5
Recommended sensitivity ± (N and S) 3-7 mT (30-70 Gauss)

AMBIENT LIGHT SENSOR I2C 0x29 or 0x38 (SEE SECOND SHEET FOR ALTERNATIVES)

SILKSCREEN: ALS+PROX I2C 0x38



REQUIRED: CONFIGURE FOR SINGLE CORE PLANE

STEP 1: Solder eight SJs JP9 through JP16.

STEP 2: Do NOT solder any JPs JP1 through JP8.

STEP 3: No additional components needed.

STEP 4 (LOGIC BOARD): See instructions on Logic Board, if any.

Sheet: Core64 CB v0.6 Optional

File: Core64 CB v0.6 Optional.sch

All capacitors ceramic X7R unless otherwise noted.

Visit www.Core64.io for information on assembly and optional features.

Concept and design by Andy Geppert @ www.MachineIdeas.com

Sheet: /

File: Core64 CB v0.6.sch

Title: Core64 CB (Core Board)

Size: A	Date: 2021-10-14	**Rev: 0.6**
KiCad E.D.A. eeschema (5.1.2-1)-1		Id: 1/2

SILKSCREEN MISC.

CORE BOARD VERSION [REL. DATE]. ANDY GEPPERT
www.MachineIdeas.com
Interactive Core Memory
www.Core64.io

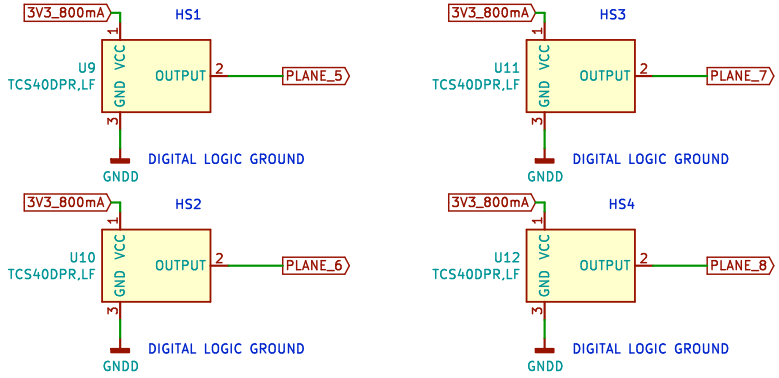
SILKSCREEN GRAPHICS

L1
Core_64_Logo_9mm_tall

L2
Core_64_M-+S_Buttons_4mm

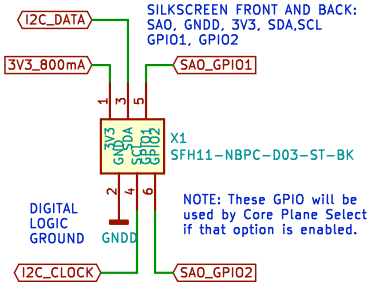
[ALTERNATE] HALL SWITCH ALTERNATES

If Hall Switches are inserted, keep the decoupling caps on the first sheet.
Recommended sensitivity ± (N and S) 3–7 mT (30–70 Gauss)
(Toshiba TCS40DPR,LF is 4.4mT. Maybe Honeywell SM353LT ±2mT.)



[OPTIONAL] SAO #2 EXPANSION

SIMPLE ADD ONS see:
https://hackaday.io/project/175182-simple-add-ons-sao



[OPTIONAL] MULTI CORE PLANE SELECT

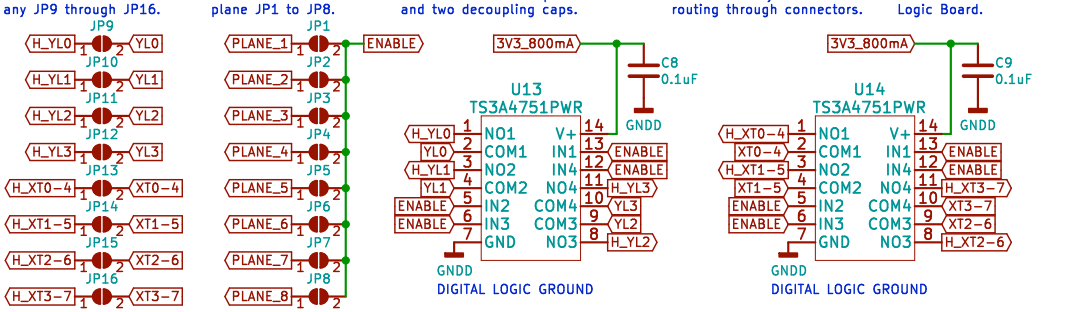
STEP 1: Do NOT solder any JP9 through JP16.

STEP 2: Solder ONE plane JP1 to JP8.

STEP 3: Install two quad switches and two decoupling caps.

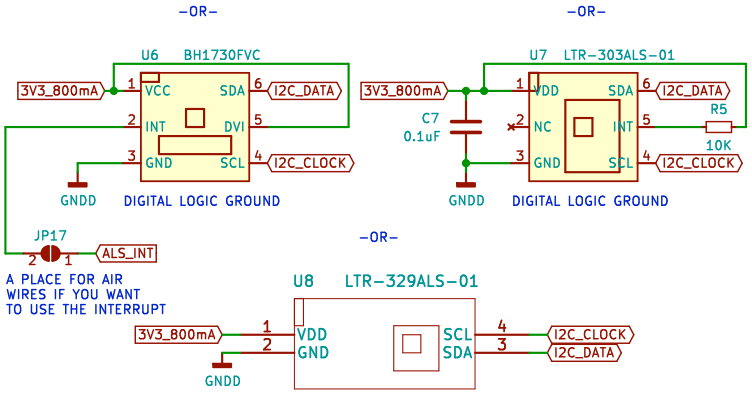
STEP 4: Modify sense wire routing through connectors.

STEP 5 (LOGIC BOARD): See instructions on Logic Board.



[ALTERNATE] AMBIENT LIGHT SENSORS I2C 0x29

SILKSCREEN: ALS I2C 0x29



All capacitors ceramic X7R unless otherwise noted.

Visit www.Core64.io for information on assembly and optional features.

Concept and design by Andy Geppert ● www.MachineIdeas.com

Sheet: /Core64 CB v0.6 Optional/
File: Core64 CB v0.6 Optional.sch

Title: Core64 CB (Core Board)

Size: A4	Date: 2021-10-14	**Rev: 0.6**
KiCad E.D.A. eeschema (5.1.2-1)-1		Id: 2/2