

CORE 64 INTERACTIVE CORE MEMORY BADGE V0.6 LOGIC BOARD

Sheet: Power

File: Core64 LB v0.6 Power.sch

Sheet: Driver

File: Core64 LB v0.6 Driver.sch

Sheet: Sense_LEDs_ID

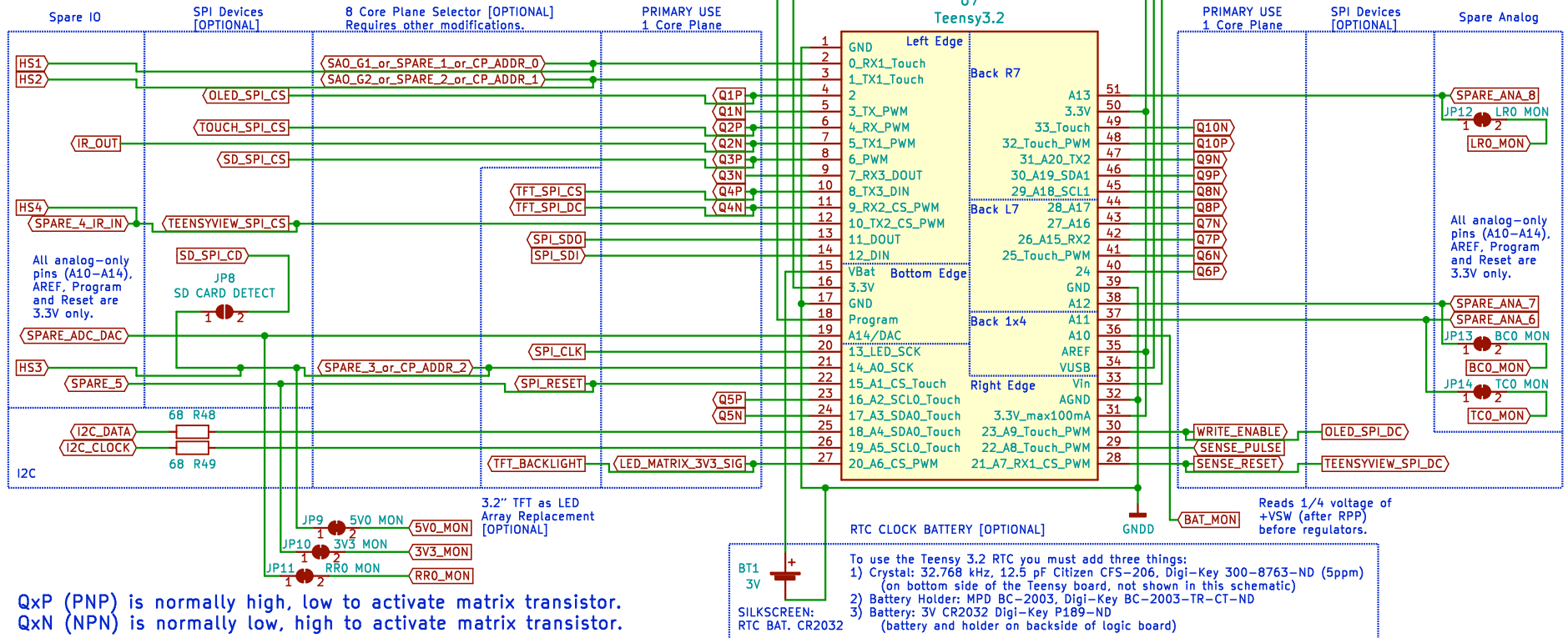
File: Core64 LB v0.6 Sense_LEDs_ID.sch

Sheet: Expansion

File: Core64 LB v0.6 Expansion.sch

*** MUST CUT THE USB-VIN on back of TEENSY 3.2 ***

TEENSY 3.2 MCU CONNECTIONS



SILKSCREEN FRONT

Interactive Core Memory
All logic is 3V3 Level

L1 Core_64_Logo



L2 Core_64_Logo

SILKSCREEN BACK

Core 64 Logo
Interactive Core Memory
Maker, Assembler, S/N
RTC Battery CR2032
PCB Maker
P/N
REV
DESCRIPTION VERSION [REL. DATE]. ANDY GEPPERT
Designed by Andy Geppert | www.MachineIdeas.com
www.Core64.io

All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

As released

Visit www.Core64.io for information on assembly and optional features.

Concept and design by Andy Geppert @ www.MachineIdeas.com

Sheet: /

File: Core64 LB v0.6.sch

Title: Core 64 - Main Sheet Index

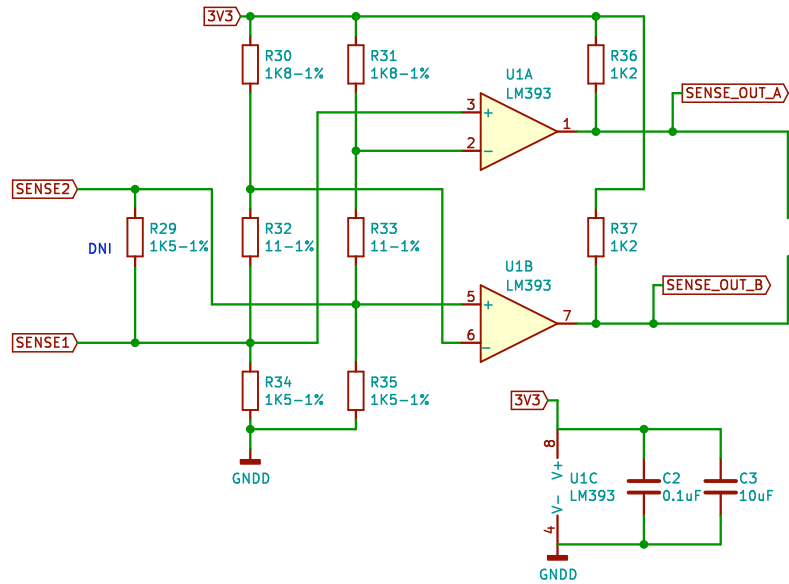
Size: A Date: 2021-11-09

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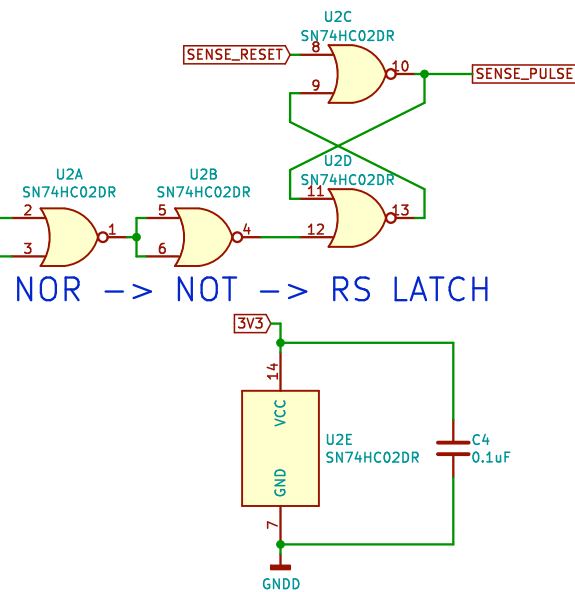
Rev: 0.6

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SENSE SIGNAL DIFFERENTIAL AMPLIFIERS

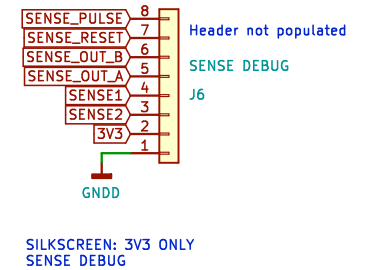


SENSE SIGNAL LATCH

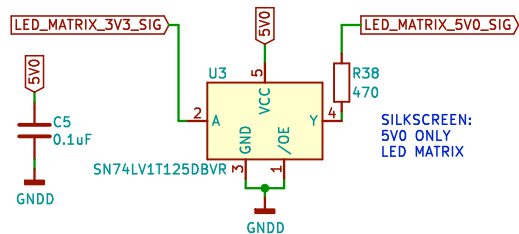


NOR -> NOT -> RS LATCH

SENSE DEBUG

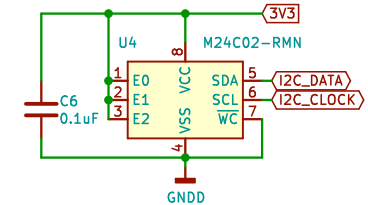


LED MATRIX DRIVE AND LEVEL SHIFT



BOARD ID AND S/N

EEPROM I2C ADDRESS: 0b1010111, 0x57 (87)



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Sheet: /Sense_LEDs_ID/

File: Core64 LB v0.6 Sense_LEDs_ID.sch

Title: Core 64 - Sense

Size: A Date: 2021-11-09

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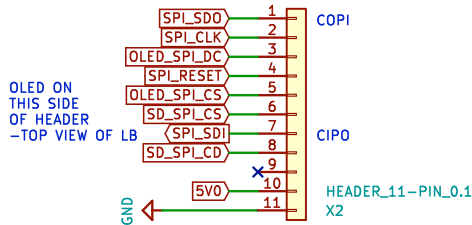
Rev: 0.6

Id: 2/5

EVERYTHING ON THIS SHEET IS USER-PROVIDED OPTIONAL ADD-ONS

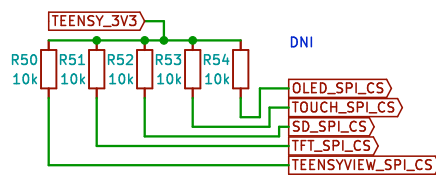
OLED COLOR SPI w/MicroSD

Compatible: <https://www.adafruit.com/product/1431>
1.5" 128x128, 16-bit color w/MicroSD holder
OLED has 5V -> 3V3 regulator onboard.
MicroSD card standalone pins shared between TFT and OLED boards.

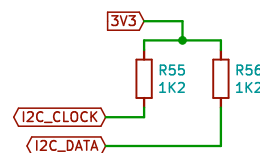


SILKSCREEN: 3V3 Logic ONLY, 3V3/GND sides of jumpers, SPI OLED

SPI CS PULL-UPS



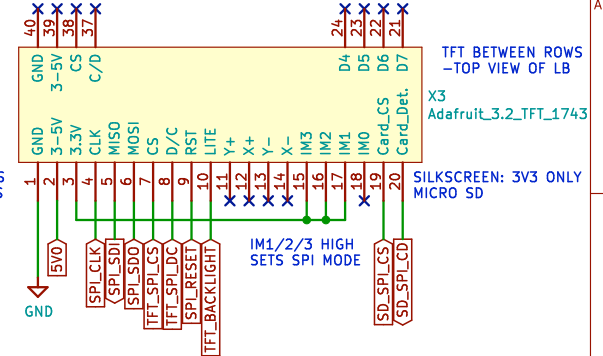
I2C PULL-UPS



TFT LCD SOCKETS FOR LOGIC BOARD:
1x SAMTEC 20-pin SMD Header SSW-120-22-F-S-VS
2x SAMTEC 4-pin SMD Header SSW-104-22-F-S-VS

3.2" TFT LCD SPI w/MicroSD

Compatible with <https://www.adafruit.com/product/1743>
TFT has 5V -> 3V3 regulator onboard.
MicroSD card standalone pins shared between TFT and OLED boards.
Headers 3.0 in. apart



TFT BETWEEN ROWS
-TOP VIEW OF LB

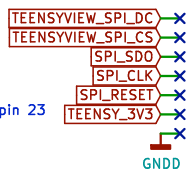
X3
Adafruit_3.2-TFT_1743

SILKSCREEN: 3V3 ONLY
MICRO SD

OLED TEENSYVIEW SPI

Monochrome 128x32
The TeensyView is designed to stack on the Teensy 3.2
Configuration: <https://www.sparkfun.com/products/14048>

Use only these Teensy pins:
21: D/C (default is 5)
10: CS
11: MOSI
13: SCLK
15: RESET
3.3V Power from Teensy next to pin 23
GND at corner next to pin 0

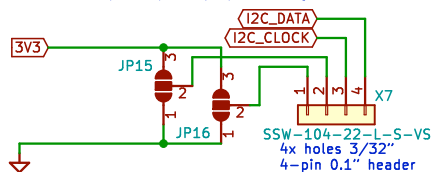


GNDD

OLED SOCKET FOR LOGIC BOARD:
SAMTEC 4-pin SMD Header SSW-104-22-F-S-VS

OLED MONOCHROME I2C

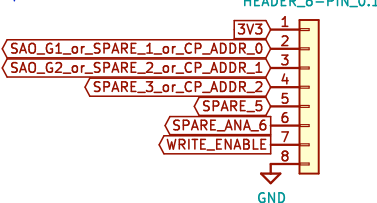
Generic 0.96" (128x64) or 1.5" (128x128)
I2C 4-pins, often ADDRESS: 0x3C (60 decimal)
Alternate is 0x3D, not 0x7A or 0x78 (wrong 8-bit!)
Must choose power polarity by soldering SJS.



GND SILKSCREEN: 3V3 ONLY, 3V3/GND sides of jumpers,
I2C OLED and pin names

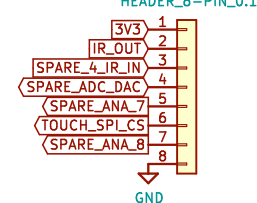
GPIO#1

Silkscreen: 3V3 ONLY
pin names



GPIO#2

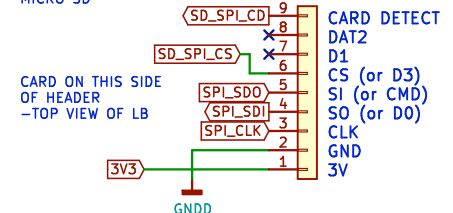
Silkscreen: 3V3 ONLY
pin names



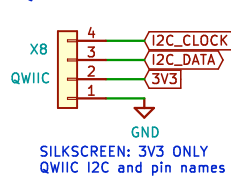
MICRO SD CARD

Compatible with <https://www.adafruit.com/product/4682>
MicroSD card standalone pins shared between TFT and OLED boards.

SILKSCREEN: 3V3 ONLY
MICRO SD



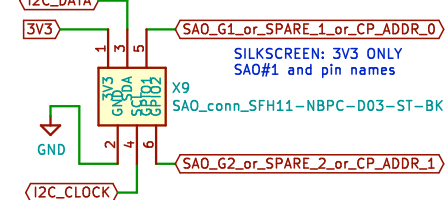
QWIIIC I2C



SILKSCREEN: 3V3 ONLY
QWIIIC I2C and pin names

SAO #1 SIMPLE ADD ONS

SAO#2 is on the Core Board



<https://hackaday.io/project/175182-simple-add-ons-sao>
using Sullins SFH11-NBPC-D03-ST-BK female header
<https://www.digikey.com/product-detail/en/sullins-connector-solutions/SFH11-NBPC-D03-ST-BK/S9717-ND/4558818>

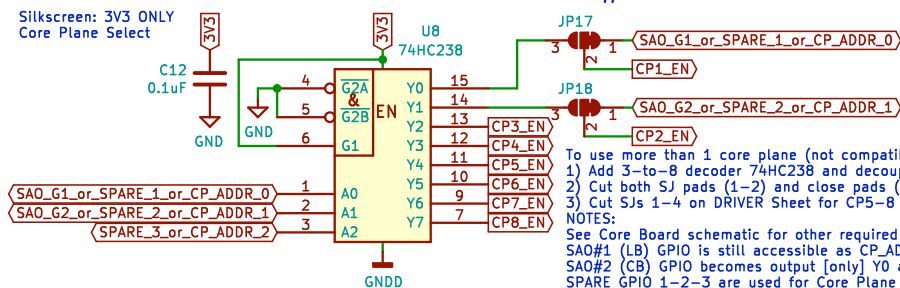
I2C ADDRESS TABLE

INCLUDED:	
AMBIENT LIGHT SENSOR	0x29 (47)
HALL SENSOR 1	0x30 (48)
HALL SENSOR 2	0x31 (49)
HALL SENSOR 3	0x32 (50)
HALL SENSOR 4	0x33 (51)
EEPROM (BOARD ID)	0x57 (87)
OPTIONAL:	
AMBIENT PROX. SENSOR	0x38 (56)
OLED	0x3C (60)
ANDIXOR IO Exp. MCP23017	0x20 (32)
ANDIXOR EEPROM AT24C32r	0x50 (80)
NFC CLICK PN7120	0x50-53

All 7-bit addresses should be greater than 0x07 and less than 0x78 (120).

CORE PLANE & CORE BOARD SAO #2 GPIO SELECT

Silkscreen: 3V3 ONLY
Core Plane Select



To use more than 1 core plane (not compatible with Hall Switches):
1) Add 3-to-8 decoder 74HC238 and decoupling capacitor.
2) Cut both SJ pads (1-2) and close pads (2-3) for CP1 and 2_EN.
3) Cut SJs 1-4 on DRIVER Sheet for CP5-8 if Hall Switches installed.
NOTES:
See Core Board schematic for other required CB changes.
SAO#1 (LB) GPIO is still accessible as CP_ADDR_0 and 1, shared.
SAO#2 (CB) GPIO becomes output [only] Y0 and Y1 of CP selector.
SPARE GPIO 1-2-3 are used for Core Plane Addressing.

All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

As released

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Concept and design by Andy Geppert © www.MachineIdeas.com

Sheet: /Expansion/

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Size: A Date: 2021-11-09

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Rev: 0.6

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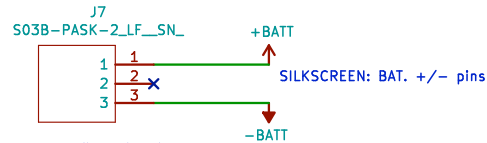
STANDARD KIT CONFIGURATION – AS MANUFACTURED

TWO POWER INPUT SOURCES SELECTED BY SPDT SWITCH

SOURCE 1 "ON (BAT)"

BUILT-IN BATTERY PACK (Keystone 2482 or 2482CN) WITH 4X "AAA" primary/Alkaline Cells OK to use Energizer Ultimate Lithium (light weight!) with open cell 7.2V, loaded will be <7V. Battery Pack includes wires and may or may not have a 3-pin plug.

Optional Socket: TH, Side Entry, JST PA S03B-PASK-2(LF)(SN), Digikey 455-1848-ND



SILKSCREEN:

7.5V MAX !!!

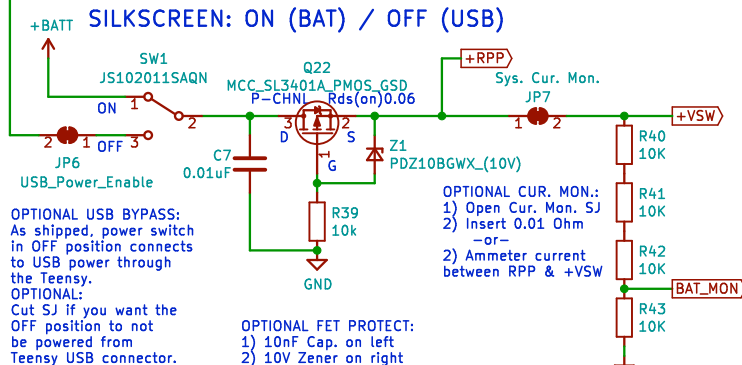
Limitation of 5V0 regulator.

SOURCE 2 "OFF (USB)"

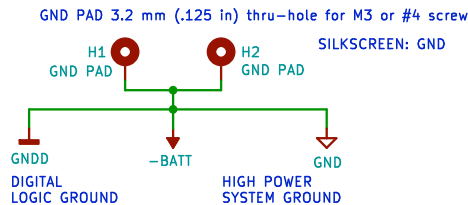
USB 5V supplied through Teensy and optional LiPo Charger USB port. With the VIN-VUSB trace cut on the back of the Teensy, the TEENSY_VUSB is taken off of the Teensy Board and routed on the Core64 LB to the lower position of the power switch. From here, it powers the whole Core64 system and routes back to the TEENSY_VIN after passing through the 5V LDO regulator.

***** ALL CONFIGURATIONS REQUIRE CUTTING VIN-VUSB TRACE ON BACK OF TEENSY *****

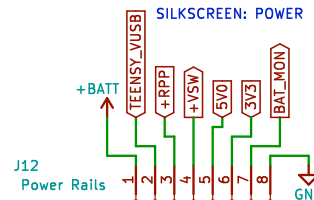
POWER SWITCH, RPP, V & I MONITOR



ALL SYSTEM GROUND



POWER RAILS



ALTERNATE 1S LIPO BATTERY – USER SUPPLIED

- 1) Remove the 4x "AAA" battery pack AND the battery connector, if installed.
- 2) Purchase and install a LiPo charge manager.
 - a) The Logic Board accepts <https://www.adafruit.com/product/1904> (Micro USB) and LED Matrix #4410 (USB C).
 - b) Solder the charge manager directly to the board to keep a low profile.
- 3) Purchase and install a 1S LiPo using double-sided tape.
 - a) Choose a 1S LiPo with built-in cell over/under voltage protection. Recommended: 2500mAh <https://www.adafruit.com/product/328> 1.8" x 2.4" x 0.26" (47mm x 61mm x 6.7mm) 2000mAh <https://www.adafruit.com/product/2011> 2.4" x 1.4" x 0.3" (60mm x 36mm x 7mm) 1200mAh <https://www.adafruit.com/product/258> 1.3" x 2.4" x 0.2" (34mm x 62mm x 5mm)
 - b) The LiPo can be up to 50 x 65 x 14mm maximum.
 - c) Make sure no part of the LiPo foil pouch can short-out adjacent pins or pads in the area. Insulate with Kapton tape.

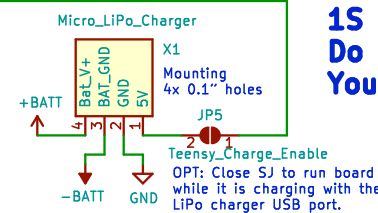
Configuration of the Teensy_Charge_Enable Solder Jumper (SJ):

A) DEFAULT SJ OPEN:

If you do NOT want the system to be powered from the USB port of the charger, leave the SJ open. Connecting a USB cable to the LiPo charger will ONLY charge the battery and power the system when the power switch is ON (up/battery) position. Connecting a USB cable to the Teensy will NOT charge the battery, but it will power the system when the power switch is in OFF (down/USB) position.

B) OPTIONAL SJ CLOSED:

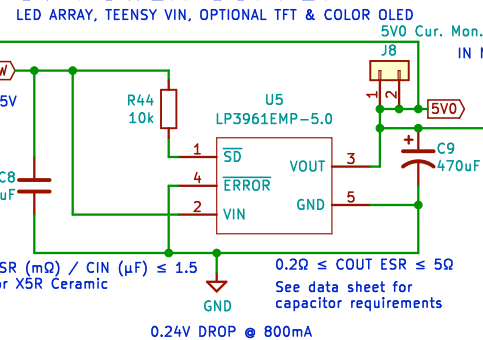
The LiPo charger 5V pin (LiPo Charger USB port) may be connected to the Teensy USB port by closing the SJ. Connecting a USB cable to the LiPo charger will charge the battery and power the system. It will not connect to the serial port of the Teensy. Connecting a USB cable to the Teensy will power the board and charge the battery and connect to the serial port of the Teensy.



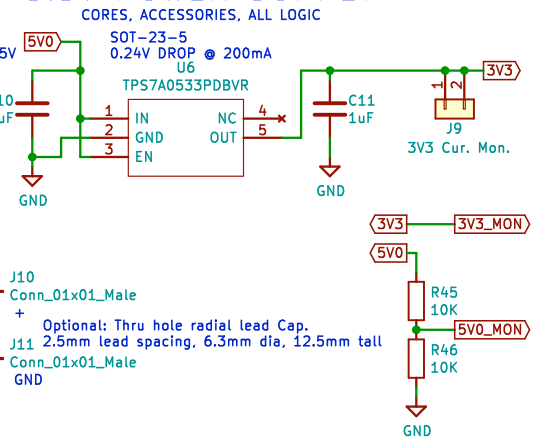
1S LIPO ONLY !!!
Do NOT connect AAAs to a LiPo charger!
You will destroy the charging chip.

SILKSCREEN: BAT. + BAT. -
SILKSCREEN: +/- pins
SILKSCREEN: LIPO CHARGER

5V POWER SUPPLY



3.3V POWER SUPPLY



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Sheet: /Power/
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Title: Core 64 – Power Schematic

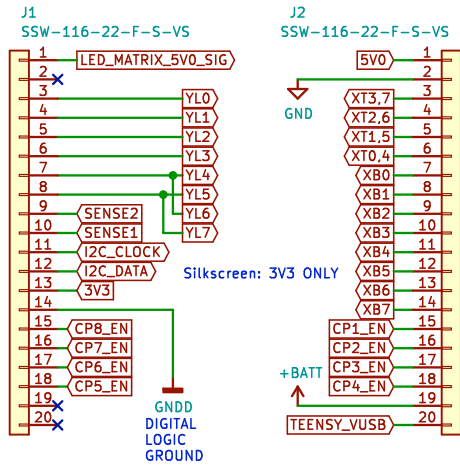
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Rev: 0.6

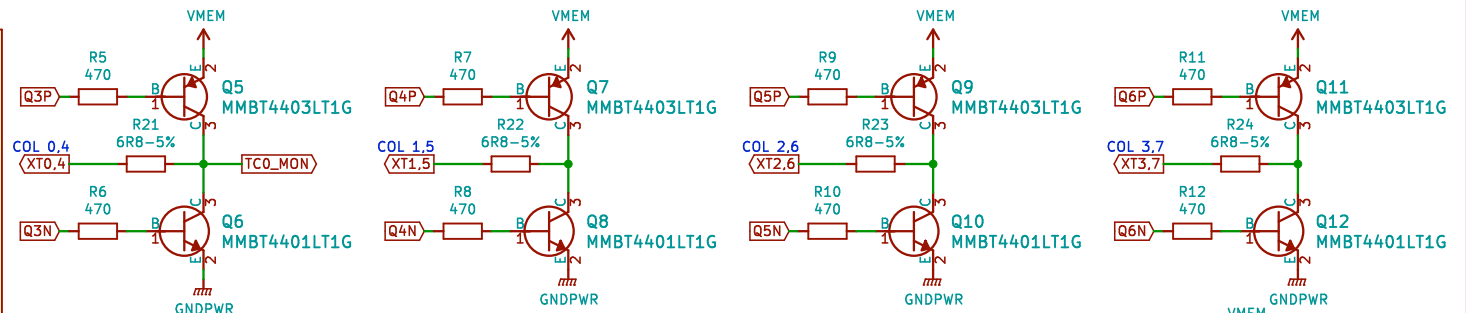
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CORE BOARD INTERCONNECTS



CORE MATRIX TOP COLUMN DRIVERS

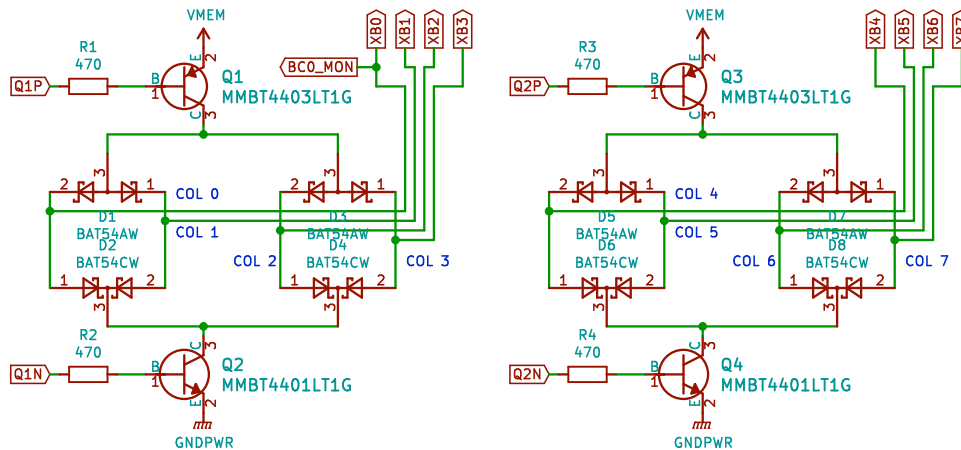
Drive Transistor current: $3.3/470=7\text{mA}$



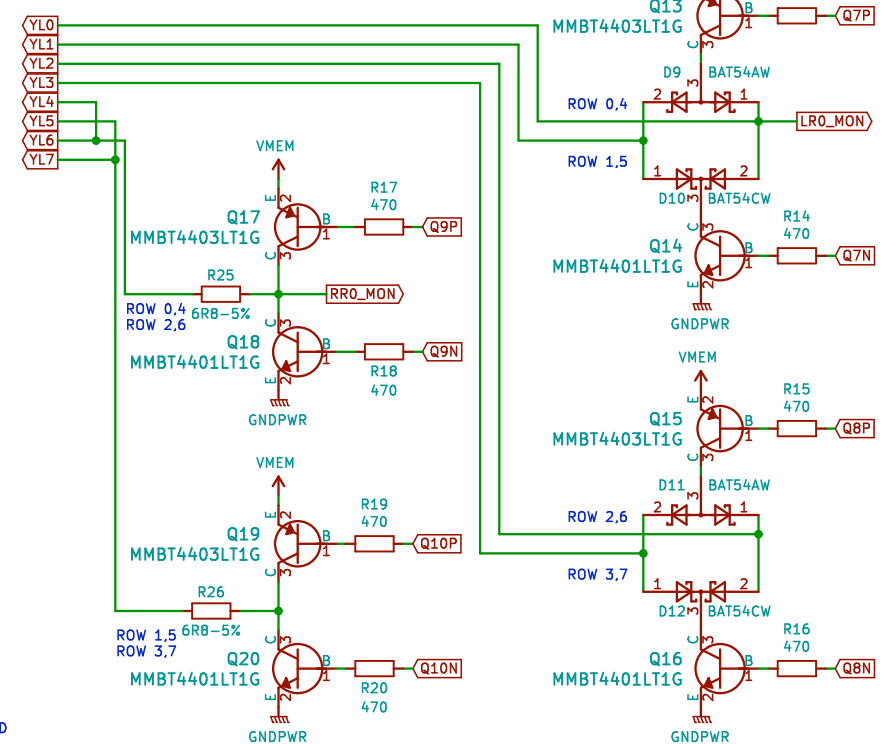
HALL SWITCHES (PLAN B...)



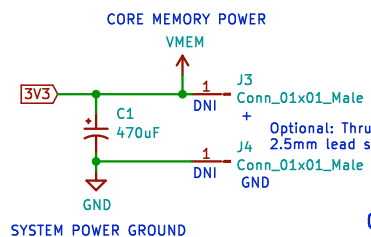
CORE MATRIX BOTTOM COLUMN DRIVERS



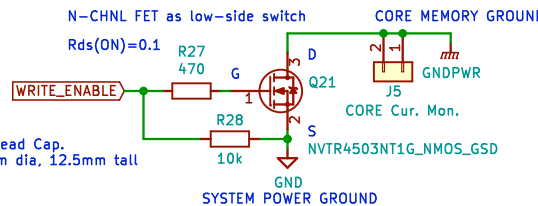
CORE MATRIX ROW DRIVERS



CORE MATRIX POWER



CORE MATRIX WRITE ENABLE



QxP (PNP) is normally high, low to activate matrix transistor.
QxN (NPN) is normally low, high to activate matrix transistor.

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Sheet: /Driver/

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Title: Core 64 – Core Matrix Driver

Size: A Date: 2021-11-09

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