Assignment 3 Report
Group-11
(Roll no -20111058, 20111070)

In this assignment a directory based multicore cache coherence protocol was simulated using the trace files generated from prog1.c, prog2.c, prog3.c and prog4.c . The results obtained on simulation are as follow.

Different messages received at L1 caches

GET : This is a forwarded message from the home bank received at some private cache.
GETX: This is a forwarded message from the home bank received at some private cache.
PUT: This is a response for the GET message coming from home bank.
PUTX: This is a response for the GETX message coming from home bank.
INV: This is coming from home bank, when we have to invalidate something in some private cache.
ACK: This is one of the acknowledge of invalidation received from some other private cache.
NACK: This is received from home bank, when state is pending in home bank.
UPGR_ACK: This is a response for UPGR msg, received from home bank.

Different messages received at L2 cache banks

GET : This is coming from some private cache, when a core wants block in shared state.
GETX : This is coming from some private cache, when a core want block in modified state.
UPGR : This is coming from some provate cache, when a core wants to upgrade state of it's block from shared to modified.
ACK : This is coming from a private cache, when it provides the block to some other core in modified state.
SWB : This is coming from a private cache, when it provides the block to some other core in shared state.
WB : This is coming from some private cache, when a block is evicted from it in modified state.

Results:

For Program: 1

Number of Simulated Cycles: 140347750

L1 Caches (Private Caches):

The number of L1 cache accesses and misses are mentioned in the below table:

Core number of Private Cache	Number of L1 Cache Accesses	Number of Read Misses	Number of Write Misses	Number of Upgrade Misses
0	1573003	217	721165	12
1	982946	720916	7	196318
2	863081	611691	7	196321
3	719881	458772	7	196313
4	721449	524307	7	196320

5	983111	720916	7	196315
6	830220	580482	7	196285
7	262943	196627	7	65407

Number of L2 cache misses:

The number of L2 misses are mentioned in the below table

Bank ID	Misses
0	389259
1	389173
2	389122
3	389232
4	389230
5	389222
6	389217
7	389174

:

Names and counts of all messages received by Private Caches:

S. No.	Name of the message received	Number of messages received
1	GET	373354
2	GETX	360279
3	PUT	3813928
4	PUTX	721214
5	INV	225997
6	ACK	51462
7	UPGR_ACK	1243291

Names and counts of all messages received by L2 Cache banks:

S. No.	Name of the message received	Number of messages received
1	GET	3813928
2	GETX	271214
3	UPGR	1243291
4	ACK	3602719
5	SWB	373354

Observations:

For the program 1, there are less write misses compared to read and upgrade misses. As a result of this, we can see that number of PUT and UPGR_ACK are more compared to PUTX messages received at L1 caches. We can also observe that number of PUTX are same as the combined write misses at L1 caches. This distribution of misses at L1 caches, can also be seen at L2 messages. There are more GET and UPGR messages compared to GETX messages at L2 cache banks.

For Program: 2

Number of Simulated Cycles: 2510749

L1 Caches (Private Caches):

The number of L1 cache accesses and misses are mentioned in the below table:

Core number of Private Cache	Number of L1 Cache Accesses	Number of Read Misses	Number of Write Misses	Number of Upgrade Misses
0	190837	197	65783	11
1	78400	24593	8	8112
2	80643	24593	8	8108
3	77564	24593	8	8104
4	77571	24593	8	8115
5	77574	24593	8	8120
6	79133	24593	8	8117
7	57216	24593	8	8111

Number of L2 cache misses:

Bank ID	Misses
0	5152
1	5106
2	5098
3	5092
4	5118
5	5100
6	5124
7	5126

Names and counts of all messages received by L1 (Private) Caches:

S. No.	Name of the message received	Number of messages received
1	GET	86951
2	GETX	31197
3	PUT	164156
4	PUTX	65839
5	INV	41723
6	ACK	39760
7	UPGR_ACK	56798

Names and counts of all messages received by L2 Cache banks:

S. No.	Name of the message received	Number of messages received
1	GET	164156
2	GETX	65839
3	UPGR	56798
4	ACK	31197
5	SWB	86951

Observations:

In this program, first core (core 0) is performing writes in large number compared to other cores. Other cores are simply using the results generated by core 0 to a large extent. So we can see at L2 cache banks, there are large number of GET messages received compared to GETX and UPGR.

For Program: 3

Number of Simulated Cycles: 10240406

L1 Caches (Private Caches):

The number of L1 cache accesses and misses are mentioned in the below table:

Core number of Private Cache	Number of L1 Cache Accesses	Number of Read Misses	Number of Write Misses	Number of Upgrade Misses
0	189815	194	65784	9
1	196457	65551	8	65350
2	196495	65551	8	65388
3	196513	65551	8	65406
4	196422	65551	8	65315
5	196452	65551	8	65346

6	196483	65551	8	65376
7	196488	65551	8	65381

Number of L2 cache misses:

Bank ID	Misses
0	9109
1	9057
2	9057
3	9060
4	9088
5	9071
6	9095
7	9100

Names and counts of all messages received by L1 (Private) Caches:

S. No.	Name of the message received	Number of messages received
1	GET	420208
2	GETX	30941
3	PUT	459051
4	PUTX	65840
5	INV	248610
6	ACK	221565
7	UPGR_ACK	475571

Names and counts of all messages received by L2 Cache banks:

S. No.	Name of the message received	Number of messages received
1	GET	459051
2	GETX	65840
3	UPGR	457571
4	ACK	30941
5	SWB	420208

Observations:

In this program read misses and upgrade misses are comparable at L1 caches. As a result number of GET and UPGR messages at L2 cache banks is also similar.

For Program: 4

Number of Simulated Cycles: 1063024

L1 Caches (Private Caches):

The number of L1 cache accesses and misses are mentioned in the below table:

Core number of Private Cache	Number of L1 Cache Accesses	Number of Read Misses	Number of Write Misses	Number of Upgrade Misses
0	190324	194	65785	10
1	28631	8209	9	2
2	28638	8209	9	2
3	28624	8209	9	2
4	28614	8209	9	2
5	28624	8209	9	2
6	28615	8209	9	2
7	30344	8209	9	2

Number of L2 cache misses:

Bank ID	Misses
0	4382
1	4368
2	4374
3	4367
4	4369
5	4372
6	4375
7	4378

Names and counts of all messages received by L1 (Private) Caches:

S. No.	Name of the message received	Number of messages received
1	GET	30439
2	GETX	31074
3	PUT	57657
4	PUTX	65848
5	INV	2093
6	ACK	14
7	UPGR_ACK	24

Names and counts of all messages received by L2 Cache banks:

S. No.	Name of the message received	Number of messages received
1	GET	57657
2	GETX	65858
3	UPGR	24
4	ACK	31074
5	SWB	30439

Observations:

In this program there is very less upgrade misses at L1 caches, so we receive very less UPGR messages at L2 cache banks. Also the read and write misses at L1 caches are comparable, so at L2 cache banks, GET and GETX message counts are also comparable.

We can observe that there are different kinds of sharing patterns accross 4 programs. For example, in program 4, core 0 is producing values, and all other threads are consuming that value, so this pattern is similar to producer-consumer sharing pattern. We can explain the high frequency of certain kind of messages with this pattern (these patterns are written seperately with results of each program).