	10: Low/Hiz 25%/75% duty 4Hz; 11: drive low;			
3		RO	/	0
2:1	CHGLED pin display function configuration 00: display with type A function 01: display with type B function 10: output controlled by the register of chgled_out_ctrl 11: reserved	RW	POR	EFUSE
0	CHGLED pin enable 0: disable CHGLED pin function 1: enable CHGLED pin function	RW	POR	1b

6.13.2.67 REG 6A：Button battery charge termination voltage setting

Bit	Description	R/W	Reset	Default
7:3		RO	/	0
2:0	Button Battery charge termination voltage 2.6~3.3V，100mV/step，8steps 000: 2.6V 001: 2.7V 010: 2.8V 011: 2.9V 100: 3.0V 101: 3.1V 110: 3.2V 111: 3.3V	RW	POR	011b

6.13.2.68 REG 80：DCDCS ON/OFF and DVM control

Bit	Description	R/W	Reset	Default
7		RO	/	0b
6	force DCDC work in CCM mode 0: disable 1: enable	RW	System Reset	0b
5	DVM voltage ramp control 0: 15.625 us/step 1: 31.250 us/step	RW	System Reset	0b
4	DCDC5 enable 0: disable 1: enable	RW	System Reset	EFUSE
3	DCDC4 enable 0: disable 1: enable	RW	System Reset	EFUSE
2	DCDC3 enable 0: disable 1: enable	RW	System Reset	EFUSE
1	DCDC2 enable 0: disable 1: enable	RW	System Reset	EFUSE
0	DCDC1 enable 0: disable 1: enable	RW	System Reset	EFUSE

6.13.2.69 REG 81：DCDCS force PWM control

Bit	Description	R/W	Reset	Default
7	DCDC frequency spread enable 0: disable 1: enable	RW	System Reset	0b
6	DCDC frequency spread range control 0: 50KHz 1: 100kHz	RW	System Reset	0b
5	DCDC4 PWM/PFM Control 0: Auto Switch 1: Always PWM	RW	System Reset	0b
4	DCDC3 PWM/PFM Control 0: Auto Switch 1: Always PWM	RW	System Reset	0b
3	DCDC2 PWM/PFM Control 0: Auto Switch 1: Always PWM	RW	System Reset	0b
2	DCDC1 PWM/PFM Control 0: Auto Switch 1: Always PWM	RW	System Reset	0b
1:0	DCDC UVP debounce time configuration 00: 60us 01: 120us 10: 180us 11: 240us	RW	POR	00b

6.13.2.70 REG 82：DCDC1 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	DCDC1 output voltage configuration 1.5~3.4V,100mV/step,20steps 00000: 1.5V 00001: 1.6V …… 10011: 3.4V 10100~11111: reserved	RW	System Reset	EFUSE

6.13.2.71 REG 83：DCDC2 voltage setting

Bit	Description	R/W	Reset	Default
7	DCDC2 DVM enable control 0: disable 1: enable	RW	System Reset	0b
6:0	DCDC2 output voltage configuration 0.5~1.2V,10mV/step,71steps 1.22~1.54V,20mV/step,17steps 0000000: 0.50V 0000001: 0.51V …… 1000110: 1.20V	RW	System Reset	EFUSE

	1000111: 1.22V 1001000: 1.24V …… 1010111: 1.54V 1011000~1111111: reserved			

6.13.2.72 REG 84：DCDC3 voltage setting

Bit	Description	R/W	Reset	Default
7	DCDC3 DVM enable control 0: disable 1: enable	RW	System Reset	0b
6:0	DCDC3 output voltage configuration 0.5~1.2V,10mV/step,71steps 1.22~1.54V,20mV/step,17steps 1.6~3.4V,100mV/step,19steps 0000000: 0.50V 0000001: 0.51V …… 1000110: 1.20V 1000111: 1.22V 1001000: 1.24V …… 1010111: 1.54V 1011000: 1.60V 1011001: 1.70V …… 1101011: 3.40V 1101100~1111111: reserved	RW	System Reset	EFUSE

6.13.2.73 REG 85：DCDC4 voltage setting

Bit	Description	R/W	Reset	Default
7		RO	/	0
6:0	DCDC4 output voltage configuration 0.5~1.2V,10mV/step,71steps 1.22~1.84V,20mV/step,32steps 0000000: 0.50V 0000001: 0.51V …… 1000110: 1.20V 1000111: 1.22V 1001000: 1.24V …… 1100110: 1.84V 1100111~1101000: reserved	RW	System Reset	EFUSE

6.13.2.74 REG 86：DCDC5 voltage setting

Bit	Description	R/W	Reset	Default
7:6		RO	/	0
5	slow down dcdc5 frequency compensation enable 0: disable 1: enable	RW	System Reset	0b
4:0	DCDC5 output voltage configuration 1.4~3.7V,100mV/step,24steps 11001: 1.2V 00000: 1.4V 00001: 1.5V …… 10111: 3.7V 11000~11111: reserved	RW	System Reset	EFUSE

6.13.2.75 REG 90：LDOS ON/OFF control 0

Bit	Description	R/W	Reset	Default
7	dldo1 enable 0: disable 1: enable	RW	System Reset	EFUSE
6	cpusldo enable 0: disable 1: enable	RW	System Reset	EFUSE
5	bldo2 enable 0: disable 1: enable	RW	System Reset	EFUSE
4	aldo1 enable 0: disable 1: enable	RW	System Reset	EFUSE
3	aldo4 enable 0: disable 1: enable	RW	System Reset	EFUSE
2	aldo3 enable 0: disable 1: enable	RW	System Reset	EFUSE
1	aldo2 enable 0: disable 1: enable	RW	System Reset	EFUSE
0	aldo1 enable 0: disable 1: enable	RW	System Reset	EFUSE

6.13.2.76 REG 91：LDOS ON/OFF control 1

Bit	Description	R/W	Reset	Default
7:1		RO	/	0
0	dldo2 enable 0: disable 1: enable	RW	System Reset	EFUSE

6.13.2.77 REG 92：ALDO1 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	aldo1 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: reserved	RW	System Reset	EFUSE

6.13.2.78 REG 93：ALDO2 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	aldo2 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: reserved	RW	System Reset	EFUSE

6.13.2.79 REG 94：ALDO3 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	aldo3 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: reserved	RW	System Reset	EFUSE

6.13.2.80 REG 95：ALDO4 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	aldo4 output voltage configuration	RW	System Reset	EFUSE

	0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: reserved			

6.13.2.81 REG 96：BLDO1 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	bldo1 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: reserved	RW	System Reset	EFUSE

6.13.2.82 REG 97：BLDO2 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	bldo2 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: reserved	RW	System Reset	EFUSE

6.13.2.83 REG 98：CPUSLDO voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	cpusldo output voltage configuration 0.5~1.4V，50mV/step，20steps 00000: 0.50V 00001: 0.55V …… 10011: 1.40V 10100~11111: reserved	RW	System Reset	EFUSE

6.13.2.84 REG 99：DLDO1 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	dldo1 output voltage configuration 0.5~3.4V，100mV/step，29steps 00000: 0.5V 00001: 0.6V …… 11100: 3.3V 11101~11111: reserved	RW	System Reset	EFUSE

6.13.2.85 REG 9A：DLDO2 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	dldo2 output voltage configuration 0.5~1.4V，50mV/step，20steps 00000: 0.50V 00001: 0.55V …… 10011: 1.40V 10100~11111: reserved	RW	System Reset	EFUSE

6.13.2.86 REG A1：Battery parameter

Bit	Description	R/W	Reset	Default
7:0	Battery parameter ROM	RO	POR	xx

6.13.2.87 REG A2：Fuel gauge control

Bit	Description	R/W	Reset	Default
7:6	reserved	RO	/	0b
5	reserved	RW	POR	0b
4	ROM or SRAM select 1：select sram; 0：select rom;	RW	POR	0b
3:1	reserved	RO	/	0b
0	brom writer control 1:enable 0:disable	RW	POR	0b