Assembly	Field Values						Machine Code						
	$imm_{12,10:5}$	rs2	rs1	funct3	$imm_{4:1,11}$	op	$imm_{12,10:5}$	rs2	rs1	funct3	$imm_{4:1,11}$	op	
`beq s0, t5, L1` `beq x8, x30, 16`	0000 000	30	8	0	1000 0	99	0000 000	11110	01000	000	1000 0	110 0011	(0x01E40863)
	7 bits	5 bits	5 bits	3 bits	5 bits	7 bits	7 bits	5 bits	5 bits	3 bits	5 bits	7 bits	

Figure 6.21 **B-type instruction format and calculations for** `beq`

Figure 6.13 **Machine code for R-type instructions**

Assembly	Field Values					Machine Code					
	$imm_{11:0}$	rs1	funct3	rd	op	$imm_{11:0}$	rs1	funct3	rd	op	
`addi s0, s1, 12` `addi x8, x9, 12`	12	9	0	8	19	0000 0000 1100	01001	000	01000	001 0011	(0x00C48413)
`addi s2, t1, -14` `addi x18,x6, -14`	-14	6	0	18	19	1111 1111 0010	00110	000	10010	001 0011	(0xFF230913)
`lw t2, -6(s3)` `lw x7, -6(x19)`	-6	19	2	7	3	1111 1111 1010	10011	010	00111	000 0011	(0xFFA9A383)
`lb s4, 0x1F(s4)` `lb x20,0x1F(x20)`	0x1F	20	0	20	3	0000 0001 1111	10100	000	10100	000 0011	(0x01FA0A03)
`slli s2, s7, 5` `slli x18, x23, 5`	5	23	1	18	19	0000 0000 0101	10111	001	10010	001 0011	(0x005B9913)
`srai t1, t2, 29` `srai x6, x7, 29`	(upper 7 bits = 32) 29	7	5	6	19	0100 0001 1101	00111	101	00110	001 0011	(0x41D3D313)
	12 bits	5 bits	3 bits	5 bits	7 bits	12 bits	5 bits	3 bits	5 bits	7 bits	

Figure 6.17 **Machine code for I-type instructions**

Assembly	Field Values						Machine Code					
	$imm_{11:5}$	rs2	rs1	funct3	$imm_{4:0}$	op	$imm_{11:5}$	rs2	rs1	funct3	$imm_{4:0}$	op
`sw t2, -6(s3)` `sw x7, -6(x19)`	1111 111	7	19	2	11010	35	1111 111	00111	10011	010	11010	010 0011
`sh s4, 23(t0)` `sh x20,23(x5)`	0000 000	20	5	1	10111	35	0000 000	10100	00101	001	10111	010 0011
`sb t5, 0x2D(zero)` `sb x30,0x2D(x0)`	0000 001	30	0	0	01101	35	0000 001	11110	00000	000	01101	010 0011
	7 bits	5 bits	5 bits	3 bits	5 bits	7 bits	7 bits	5 bits	5 bits	3 bits	5 bits	7 bits

Figure 6.20 **Machine code for S-type instructions**

31:12	11:7	6:0	
$imm_{31:12}$	rd	op	U-Type
$imm_{20,10:1,11,19:12}$	rd	op	J-Type
20 bits	5 bits	7 bits	

Figure 6.23 **U- a**
instruction format

Assembly	Field Values			Machine Code		
	$imm_{31:12}$	rd	op	$imm_{31:12}$	rd	op
`lui s5, 0x8CDEF` `lui x21,0x8CDEF`	0x8CDEF	21	55	1000 1100 1101 1110 1111	10101	011 0111
	20 bits	5 bits	7 bits	20 bits	5 bits	7 bits

Figure 6.24 **Machine code for U-type instruction** `lui`

imm_{11}		$imm_{11:1}$	imm_0	I, S
imm_{12}		$imm_{11:1}$	0	B
$imm_{31:21}$	$imm_{20:12}$	0		U
imm_{20}	$imm_{20:12}$	$imm_{11:1}$	0	J

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0