```
In archive fpu.lib:

umqtoa.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_umqtoa@8>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 ec                add    esp,0xfffffec
   6:   53                      push   ebx
   7:   56                      push   esi
   8:   57                      push   edi
   9:   8b 75 08                mov    esi,DWORD PTR [ebp+0x8]
   c:   8b 7d 0c                mov    edi,DWORD PTR [ebp+0xc]
   f:   8b 1e                   mov    ebx,DWORD PTR [esi]
  11:   8b 76 04                mov    esi,DWORD PTR [esi+0x4]
  14:   83 c7 14                add    edi,0x14
  17:   57                      push   edi
  18:   c6 07 00                mov    BYTE PTR [edi],0x0
  1b:   c7 45 f8 cd cc cc cc    mov    DWORD PTR [ebp-0x8],0xcccccccd
  22:   c7 45 f4 cc cc cc cc    mov    DWORD PTR [ebp-0xc],0xcccccccc
  29:   c7 45 fc 0a 00 00 00    mov    DWORD PTR [ebp-0x4],0xa
  30:   0b f6                   or     esi,esi
  32:   74 50                   je     84 <_umqtoa@8+0x84>
  34:   33 c9                   xor    ecx,ecx
  36:   8b 45 f8                mov    eax,DWORD PTR [ebp-0x8]
  39:   f7 e3                   mul    ebx
  3b:   89 55 f0                mov    DWORD PTR [ebp-0x10],edx
  3e:   8b 45 f4                mov    eax,DWORD PTR [ebp-0xc]
  41:   f7 e3                   mul    ebx
  43:   01 45 f0                add    DWORD PTR [ebp-0x10],eax
  46:   83 d2 00                adc    edx,0x0
  49:   89 55 ec                mov    DWORD PTR [ebp-0x14],edx
  4c:   8b 45 f8                mov    eax,DWORD PTR [ebp-0x8]
  4f:   f7 e6                   mul    esi
  51:   01 45 f0                add    DWORD PTR [ebp-0x10],eax
  54:   11 55 ec                adc    DWORD PTR [ebp-0x14],edx
  57:   83 d1 00                adc    ecx,0x0
  5a:   8b 45 f4                mov    eax,DWORD PTR [ebp-0xc]
  5d:   f7 e6                   mul    esi
  5f:   03 45 ec                add    eax,DWORD PTR [ebp-0x14]
  62:   13 d1                   adc    edx,ecx
  64:   8b 4d f0                mov    ecx,DWORD PTR [ebp-0x10]
  67:   0f ac c1 03             shrd   ecx,eax,0x3
  6b:   0f ac d0 03             shrd   eax,edx,0x3
  6f:   41                      inc    ecx
  70:   c1 ea 03                shr    edx,0x3
  73:   8b d8                   mov    ebx,eax
  75:   8b f2                   mov    esi,edx
  77:   8b c1                   mov    eax,ecx
  79:   f7 65 fc                mul    DWORD PTR [ebp-0x4]
  7c:   80 c2 30                add    dl,0x30
  7f:   4f                      dec    edi
  80:   88 17                   mov    BYTE PTR [edi],dl
  82:   eb ac                   jmp    30 <_umqtoa@8+0x30>
  84:   8b c3                   mov    eax,ebx
  86:   f7 65 f8                mul    DWORD PTR [ebp-0x8]
  89:   0f ac d0 03             shrd   eax,edx,0x3
  8d:   c1 ea 03                shr    edx,0x3
  90:   40                      inc    eax
  91:   8b da                   mov    ebx,edx
  93:   f7 65 fc                mul    DWORD PTR [ebp-0x4]
  96:   4f                      dec    edi
  97:   80 c2 30                add    dl,0x30
  9a:   88 17                   mov    BYTE PTR [edi],dl
  9c:   85 db                   test   ebx,ebx
  9e:   75 e4                   jne    84 <_umqtoa@8+0x84>
  a0:   59                      pop    ecx
```

```
  a1:   8b c7                   mov    eax,edi
  a3:   2b cf                   sub    ecx,edi
  a5:   5f                      pop    edi
  a6:   5e                      pop    esi
  a7:   5b                      pop    ebx
  a8:   c9                      leave
  a9:   c2 08 00                ret    0x8

umdtoa.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_umdtoa@8>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   53                      push   ebx
   4:   57                      push   edi
   5:   8b 7d 0c                mov    edi,DWORD PTR [ebp+0xc]
   8:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
   b:   83 c7 0a                add    edi,0xa
   e:   57                      push   edi
   f:   b9 cd cc cc cc          mov    ecx,0xcccccccd
  14:   bb 0a 00 00 00          mov    ebx,0xa
  19:   c6 07 00                mov    BYTE PTR [edi],0x0
  1c:   f7 e1                   mul    ecx
  1e:   0f ac d0 03             shrd   eax,edx,0x3
  22:   c1 ea 03                shr    edx,0x3
  25:   40                      inc    eax
  26:   52                      push   edx
  27:   f7 e3                   mul    ebx
  29:   4f                      dec    edi
  2a:   80 c2 30                add    dl,0x30
  2d:   88 17                   mov    BYTE PTR [edi],dl
  2f:   58                      pop    eax
  30:   85 c0                   test   eax,eax
  32:   75 e8                   jne    1c <_umdtoa@8+0x1c>
  34:   59                      pop    ecx
  35:   8b c7                   mov    eax,edi
  37:   2b cf                   sub    ecx,edi
  39:   5f                      pop    edi
  3a:   5b                      pop    ebx
  3b:   c9                      leave
  3c:   c2 08 00                ret    0x8

smqtoa.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_smqtoa@8>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 ec                add    esp,0xffffffec
   6:   53                      push   ebx
   7:   56                      push   esi
   8:   57                      push   edi
   9:   8b 75 08                mov    esi,DWORD PTR [ebp+0x8]
   c:   8b 7d 0c                mov    edi,DWORD PTR [ebp+0xc]
   f:   8b 1e                   mov    ebx,DWORD PTR [esi]
  11:   8b 76 04                mov    esi,DWORD PTR [esi+0x4]
  14:   83 c7 15                add    edi,0x15
  17:   57                      push   edi
  18:   c6 07 00                mov    BYTE PTR [edi],0x0
  1b:   c7 45 f8 cd cc cc cc    mov    DWORD PTR [ebp-0x8],0xcccccccd
  22:   c7 45 f4 cc cc cc cc    mov    DWORD PTR [ebp-0xc],0xcccccccc
  29:   c7 45 fc 0a 00 00 00    mov    DWORD PTR [ebp-0x4],0xa
  30:   85 f6                   test   esi,esi
  32:   56                      push   esi
  33:   79 0a                   jns    3f <_smqtoa@8+0x3f>
```

```
  35:   f7 d6                   not    esi
  37:   f7 d3                   not    ebx
  39:   83 c3 01                add    ebx,0x1
  3c:   83 d6 00                adc    esi,0x0
  3f:   0b f6                   or     esi,esi
  41:   74 50                   je     93 <_smqtoa@8+0x93>
  43:   33 c9                   xor    ecx,ecx
  45:   8b 45 f8                mov    eax,DWORD PTR [ebp-0x8]
  48:   f7 e3                   mul    ebx
  4a:   89 55 f0                mov    DWORD PTR [ebp-0x10],edx
  4d:   8b 45 f4                mov    eax,DWORD PTR [ebp-0xc]
  50:   f7 e3                   mul    ebx
  52:   01 45 f0                add    DWORD PTR [ebp-0x10],eax
  55:   83 d2 00                adc    edx,0x0
  58:   89 55 ec                mov    DWORD PTR [ebp-0x14],edx
  5b:   8b 45 f8                mov    eax,DWORD PTR [ebp-0x8]
  5e:   f7 e6                   mul    esi
  60:   01 45 f0                add    DWORD PTR [ebp-0x10],eax
  63:   11 55 ec                adc    DWORD PTR [ebp-0x14],edx
  66:   83 d1 00                adc    ecx,0x0
  69:   8b 45 f4                mov    eax,DWORD PTR [ebp-0xc]
  6c:   f7 e6                   mul    esi
  6e:   03 45 ec                add    eax,DWORD PTR [ebp-0x14]
  71:   13 d1                   adc    edx,ecx
  73:   8b 4d f0                mov    ecx,DWORD PTR [ebp-0x10]
  76:   0f ac c1 03             shrd   ecx,eax,0x3
  7a:   0f ac d0 03             shrd   eax,edx,0x3
  7e:   41                      inc    ecx
  7f:   c1 ea 03                shr    edx,0x3
  82:   8b d8                   mov    ebx,eax
  84:   8b f2                   mov    esi,edx
  86:   8b c1                   mov    eax,ecx
  88:   f7 65 fc                mul    DWORD PTR [ebp-0x4]
  8b:   80 c2 30                add    dl,0x30
  8e:   4f                      dec    edi
  8f:   88 17                   mov    BYTE PTR [edi],dl
  91:   eb ac                   jmp    3f <_smqtoa@8+0x3f>
  93:   8b c3                   mov    eax,ebx
  95:   f7 65 f8                mul    DWORD PTR [ebp-0x8]
  98:   0f ac d0 03             shrd   eax,edx,0x3
  9c:   c1 ea 03                shr    edx,0x3
  9f:   40                      inc    eax
  a0:   8b da                   mov    ebx,edx
  a2:   f7 65 fc                mul    DWORD PTR [ebp-0x4]
  a5:   4f                      dec    edi
  a6:   80 c2 30                add    dl,0x30
  a9:   88 17                   mov    BYTE PTR [edi],dl
  ab:   85 db                   test   ebx,ebx
  ad:   75 e4                   jne    93 <_smqtoa@8+0x93>
  af:   5e                      pop    esi
  b0:   85 f6                   test   esi,esi
  b2:   79 04                   jns    b8 <_smqtoa@8+0xb8>
  b4:   4f                      dec    edi
  b5:   c6 07 2d                mov    BYTE PTR [edi],0x2d
  b8:   59                      pop    ecx
  b9:   8b c7                   mov    eax,edi
  bb:   2b cf                   sub    ecx,edi
  bd:   5f                      pop    edi
  be:   5e                      pop    esi
  bf:   5b                      pop    ebx
  c0:   c9                      leave
  c1:   c2 08 00                ret    0x8

smdtoa.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_smdtoa@8>:
   0:   55                      push   ebp
```

```
   1:   8b ec                   mov    ebp,esp
   3:   53                      push   ebx
   4:   57                      push   edi
   5:   8b 7d 0c                mov    edi,DWORD PTR [ebp+0xc]
   8:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
   b:   83 c7 0b                add    edi,0xb
   e:   57                      push   edi
   f:   b9 cd cc cc cc          mov    ecx,0xcccccccd
  14:   bb 0a 00 00 00          mov    ebx,0xa
  19:   c6 07 00                mov    BYTE PTR [edi],0x0
  1c:   85 c0                   test   eax,eax
  1e:   79 02                   jns    22 <_smdtoa@8+0x22>
  20:   f7 d8                   neg    eax
  22:   f7 e1                   mul    ecx
  24:   0f ac d0 03             shrd   eax,edx,0x3
  28:   c1 ea 03                shr    edx,0x3
  2b:   40                      inc    eax
  2c:   52                      push   edx
  2d:   f7 e3                   mul    ebx
  2f:   4f                      dec    edi
  30:   80 c2 30                add    dl,0x30
  33:   88 17                   mov    BYTE PTR [edi],dl
  35:   58                      pop    eax
  36:   85 c0                   test   eax,eax
  38:   75 e8                   jne    22 <_smdtoa@8+0x22>
  3a:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  3d:   85 c0                   test   eax,eax
  3f:   79 04                   jns    45 <_smdtoa@8+0x45>
  41:   4f                      dec    edi
  42:   c6 07 2d                mov    BYTE PTR [edi],0x2d
  45:   59                      pop    ecx
  46:   8b c7                   mov    eax,edi
  48:   2b cf                   sub    ecx,edi
  4a:   5f                      pop    edi
  4b:   5b                      pop    ebx
  4c:   c9                      leave
  4d:   c2 08 00                ret    0x8

FpuXexpY.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuXexpY@16>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 14 01 01 00 00    test   DWORD PTR [ebp+0x14],0x101
   d:   74 0d                   je     1c <_FpuXexpY@16+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuXexpY@16+0x1c>
  18:   7a 02                   jp     1c <_FpuXexpY@16+0x1c>
  1a:   74 76                   je     92 <_FpuXexpY@16+0x92>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 14 01 00 00 00    test   DWORD PTR [ebp+0x14],0x1
  27:   74 0b                   je     34 <_FpuXexpY@16+0x34>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   e9 80 00 00 00          jmp    b4 <_FpuXexpY@16+0xb4>
  34:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  37:   f7 45 14 10 00 00 00    test   DWORD PTR [ebp+0x14],0x10
  3e:   75 58                   jne    98 <_FpuXexpY@16+0x98>
  40:   f7 45 14 02 00 00 00    test   DWORD PTR [ebp+0x14],0x2
  47:   74 04                   je     4d <_FpuXexpY@16+0x4d>
  49:   db 28                   fld    TBYTE PTR [eax]
  4b:   eb 67                   jmp    b4 <_FpuXexpY@16+0xb4>
  4d:   f7 45 14 00 00 02 00    test   DWORD PTR [ebp+0x14],0x20000
```

```
  54:   74 04                   je     5a <_FpuXexpY@16+0x5a>
  56:   dd 00                   fld    QWORD PTR [eax]
  58:   eb 5a                   jmp    b4 <_FpuXexpY@16+0xb4>
  5a:   f7 45 14 00 00 01 00    test   DWORD PTR [ebp+0x14],0x10000
  61:   74 04                   je     67 <_FpuXexpY@16+0x67>
  63:   d9 00                   fld    DWORD PTR [eax]
  65:   eb 4d                   jmp    b4 <_FpuXexpY@16+0xb4>
  67:   f7 45 14 04 00 00 00    test   DWORD PTR [ebp+0x14],0x4
  6e:   74 04                   je     74 <_FpuXexpY@16+0x74>
  70:   db 00                   fild   DWORD PTR [eax]
  72:   eb 40                   jmp    b4 <_FpuXexpY@16+0xb4>
  74:   f7 45 14 00 00 00 01    test   DWORD PTR [ebp+0x14],0x1000000
  7b:   74 04                   je     81 <_FpuXexpY@16+0x81>
  7d:   df 28                   fild   QWORD PTR [eax]
  7f:   eb 33                   jmp    b4 <_FpuXexpY@16+0xb4>
  81:   f7 45 14 08 00 00 00    test   DWORD PTR [ebp+0x14],0x8
  88:   74 05                   je     8f <_FpuXexpY@16+0x8f>
  8a:   db 45 08                fild   DWORD PTR [ebp+0x8]
  8d:   eb 25                   jmp    b4 <_FpuXexpY@16+0xb4>
  8f:   dd 65 94                frstor [ebp-0x6c]
  92:   33 c0                   xor    eax,eax
  94:   c9                      leave
  95:   c2 10 00                ret    0x10
  98:   83 f8 01                cmp    eax,0x1
  9b:   75 04                   jne    a1 <_FpuXexpY@16+0xa1>
  9d:   d9 eb                   fldpi
  9f:   eb 13                   jmp    b4 <_FpuXexpY@16+0xb4>
  a1:   83 f8 02                cmp    eax,0x2
  a4:   75 e9                   jne    8f <_FpuXexpY@16+0x8f>
  a6:   d9 e8                   fld1
  a8:   d9 ea                   fldl2e
  aa:   d8 e1                   fsub   st,st(1)
  ac:   d9 f0                   f2xm1
  ae:   d8 c1                   fadd   st,st(1)
  b0:   d9 fd                   fscale
  b2:   dd d9                   fstp   st(1)
  b4:   f7 45 14 00 01 00 00    test   DWORD PTR [ebp+0x14],0x100
  bb:   74 0b                   je     c8 <_FpuXexpY@16+0xc8>
  bd:   8d 45 94                lea    eax,[ebp-0x6c]
  c0:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  c3:   e9 80 00 00 00          jmp    148 <_FpuXexpY@16+0x148>
  c8:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  cb:   f7 45 14 00 10 00 00    test   DWORD PTR [ebp+0x14],0x1000
  d2:   75 54                   jne    128 <_FpuXexpY@16+0x128>
  d4:   f7 45 14 00 02 00 00    test   DWORD PTR [ebp+0x14],0x200
  db:   74 04                   je     e1 <_FpuXexpY@16+0xe1>
  dd:   db 28                   fld    TBYTE PTR [eax]
  df:   eb 67                   jmp    148 <_FpuXexpY@16+0x148>
  e1:   f7 45 14 00 00 08 00    test   DWORD PTR [ebp+0x14],0x80000
  e8:   74 04                   je     ee <_FpuXexpY@16+0xee>
  ea:   dd 00                   fld    QWORD PTR [eax]
  ec:   eb 5a                   jmp    148 <_FpuXexpY@16+0x148>
  ee:   f7 45 14 00 00 04 00    test   DWORD PTR [ebp+0x14],0x40000
  f5:   74 04                   je     fb <_FpuXexpY@16+0xfb>
  f7:   d9 00                   fld    DWORD PTR [eax]
  f9:   eb 4d                   jmp    148 <_FpuXexpY@16+0x148>
  fb:   f7 45 14 00 04 00 00    test   DWORD PTR [ebp+0x14],0x400
 102:   74 04                   je     108 <_FpuXexpY@16+0x108>
 104:   db 00                   fild   DWORD PTR [eax]
 106:   eb 40                   jmp    148 <_FpuXexpY@16+0x148>
 108:   f7 45 14 00 00 00 02    test   DWORD PTR [ebp+0x14],0x2000000
 10f:   74 04                   je     115 <_FpuXexpY@16+0x115>
 111:   df 28                   fild   QWORD PTR [eax]
 113:   eb 33                   jmp    148 <_FpuXexpY@16+0x148>
 115:   f7 45 14 00 08 00 00    test   DWORD PTR [ebp+0x14],0x800
 11c:   74 05                   je     123 <_FpuXexpY@16+0x123>
 11e:   db 45 0c                fild   DWORD PTR [ebp+0xc]
 121:   eb 25                   jmp    148 <_FpuXexpY@16+0x148>
 123:   e9 67 ff ff ff          jmp    8f <_FpuXexpY@16+0x8f>
 128:   83 f8 01                cmp    eax,0x1
```

```
 12b:   75 04                   jne    131 <_FpuXexpY@16+0x131>
 12d:   d9 eb                   fldpi
 12f:   eb 17                   jmp    148 <_FpuXexpY@16+0x148>
 131:   83 f8 02                cmp    eax,0x2
 134:   0f 85 55 ff ff ff       jne    8f <_FpuXexpY@16+0x8f>
 13a:   d9 e8                   fld1
 13c:   d9 ea                   fldl2e
 13e:   d8 e1                   fsub   st,st(1)
 140:   d9 f0                   f2xm1
 142:   d8 c1                   fadd   st,st(1)
 144:   d9 fd                   fscale
 146:   dd d9                   fstp   st(1)
 148:   d9 c9                   fxch   st(1)
 14a:   d9 f1                   fyl2x
 14c:   d9 c0                   fld    st(0)
 14e:   d9 fc                   frndint
 150:   dc e9                   fsubr  st(1),st
 152:   d9 c9                   fxch   st(1)
 154:   d9 f0                   f2xm1
 156:   d9 e8                   fld1
 158:   de c1                   faddp  st(1),st
 15a:   d9 fd                   fscale
 15c:   9b df e0                fstsw  ax
 15f:   9b                      fwait
 160:   d0 e8                   shr    al,1
 162:   0f 82 27 ff ff ff       jb     8f <_FpuXexpY@16+0x8f>
 168:   dd d9                   fstp   st(1)
 16a:   f7 45 14 80 00 00 00    test   DWORD PTR [ebp+0x14],0x80
 171:   74 05                   je     178 <_FpuXexpY@16+0x178>
 173:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
 176:   eb 1f                   jmp    197 <_FpuXexpY@16+0x197>
 178:   8b 45 10                mov    eax,DWORD PTR [ebp+0x10]
 17b:   f7 45 14 00 00 10 00    test   DWORD PTR [ebp+0x14],0x100000
 182:   74 04                   je     188 <_FpuXexpY@16+0x188>
 184:   d9 18                   fstp   DWORD PTR [eax]
 186:   eb 0f                   jmp    197 <_FpuXexpY@16+0x197>
 188:   f7 45 14 00 00 20 00    test   DWORD PTR [ebp+0x14],0x200000
 18f:   74 04                   je     195 <_FpuXexpY@16+0x195>
 191:   dd 18                   fstp   QWORD PTR [eax]
 193:   eb 02                   jmp    197 <_FpuXexpY@16+0x197>
 195:   db 38                   fstp   TBYTE PTR [eax]
 197:   dd 65 94                frstor [ebp-0x6c]
 19a:   f7 45 14 01 01 00 00    test   DWORD PTR [ebp+0x14],0x101
 1a1:   74 02                   je     1a5 <_FpuXexpY@16+0x1a5>
 1a3:   dd d8                   fstp   st(0)
 1a5:   f7 45 14 80 00 00 00    test   DWORD PTR [ebp+0x14],0x80
 1ac:   74 05                   je     1b3 <_FpuXexpY@16+0x1b3>
 1ae:   dd c7                   ffree  st(7)
 1b0:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
 1b3:   0c 01                   or     al,0x1
 1b5:   c9                      leave
 1b6:   c2 10 00                ret    0x10

FpuTrunc.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuTrunc@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuTrunc@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuTrunc@12+0x1c>
  18:   7a 02                   jp     1c <_FpuTrunc@12+0x1c>
```

```
  1a:   74 42                   je     5e <_FpuTrunc@12+0x5e>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 08                   je     31 <_FpuTrunc@12+0x31>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   eb 33                   jmp    64 <_FpuTrunc@12+0x64>
  31:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  34:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
  3b:   74 04                   je     41 <_FpuTrunc@12+0x41>
  3d:   db 28                   fld    TBYTE PTR [eax]
  3f:   eb 23                   jmp    64 <_FpuTrunc@12+0x64>
  41:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
  48:   74 04                   je     4e <_FpuTrunc@12+0x4e>
  4a:   dd 00                   fld    QWORD PTR [eax]
  4c:   eb 16                   jmp    64 <_FpuTrunc@12+0x64>
  4e:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
  55:   74 04                   je     5b <_FpuTrunc@12+0x5b>
  57:   d9 00                   fld    DWORD PTR [eax]
  59:   eb 09                   jmp    64 <_FpuTrunc@12+0x64>
  5b:   dd 65 94                frstor [ebp-0x6c]
  5e:   33 c0                   xor    eax,eax
  60:   c9                      leave
  61:   c2 0c 00                ret    0xc
  64:   50                      push   eax
  65:   9b d9 3c 24             fstcw  WORD PTR [esp]
  69:   9b                      fwait
  6a:   66 8b 04 24             mov    ax,WORD PTR [esp]
  6e:   66 0d 00 0c             or     ax,0xc00
  72:   50                      push   eax
  73:   d9 2c 24                fldcw  WORD PTR [esp]
  76:   d9 fc                   frndint
  78:   58                      pop    eax
  79:   d9 2c 24                fldcw  WORD PTR [esp]
  7c:   9b                      fwait
  7d:   58                      pop    eax
  7e:   9b df e0                fstsw  ax
  81:   9b                      fwait
  82:   d0 e8                   shr    al,1
  84:   72 d5                   jb     5b <_FpuTrunc@12+0x5b>
  86:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  8d:   74 05                   je     94 <_FpuTrunc@12+0x94>
  8f:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
  92:   eb 39                   jmp    cd <_FpuTrunc@12+0xcd>
  94:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  97:   f7 45 10 40 00 00 00    test   DWORD PTR [ebp+0x10],0x40
  9e:   74 04                   je     a4 <_FpuTrunc@12+0xa4>
  a0:   db 18                   fistp  DWORD PTR [eax]
  a2:   eb 4b                   jmp    ef <_FpuTrunc@12+0xef>
  a4:   f7 45 10 00 00 40 00    test   DWORD PTR [ebp+0x10],0x400000
  ab:   74 04                   je     b1 <_FpuTrunc@12+0xb1>
  ad:   df 38                   fistp  QWORD PTR [eax]
  af:   eb 3e                   jmp    ef <_FpuTrunc@12+0xef>
  b1:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
  b8:   74 04                   je     be <_FpuTrunc@12+0xbe>
  ba:   d9 18                   fstp   DWORD PTR [eax]
  bc:   eb 0f                   jmp    cd <_FpuTrunc@12+0xcd>
  be:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
  c5:   74 04                   je     cb <_FpuTrunc@12+0xcb>
  c7:   dd 18                   fstp   QWORD PTR [eax]
  c9:   eb 02                   jmp    cd <_FpuTrunc@12+0xcd>
  cb:   db 38                   fstp   TBYTE PTR [eax]
  cd:   dd 65 94                frstor [ebp-0x6c]
  d0:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  d7:   74 02                   je     db <_FpuTrunc@12+0xdb>
  d9:   dd d8                   fstp   st(0)
  db:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  e2:   74 05                   je     e9 <_FpuTrunc@12+0xe9>
  e4:   dd c7                   ffree  st(7)
  e6:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
```

```
  e9:   0c 01                   or     al,0x1
  eb:   c9                      leave
  ec:   c2 0c 00                ret    0xc
  ef:   9b df e0                fstsw  ax
  f2:   9b                      fwait
  f3:   d0 e8                   shr    al,1
  f5:   0f 82 60 ff ff ff       jb     5b <_FpuTrunc@12+0x5b>
  fb:   eb d0                   jmp    cd <_FpuTrunc@12+0xcd>

FpuTexpX.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuTexpX@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuTexpX@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuTexpX@12+0x1c>
  18:   7a 02                   jp     1c <_FpuTexpX@12+0x1c>
  1a:   74 76                   je     92 <_FpuTexpX@12+0x92>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 0b                   je     34 <_FpuTexpX@12+0x34>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   e9 80 00 00 00          jmp    b4 <_FpuTexpX@12+0xb4>
  34:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  37:   f7 45 10 10 00 00 00    test   DWORD PTR [ebp+0x10],0x10
  3e:   75 58                   jne    98 <_FpuTexpX@12+0x98>
  40:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
  47:   74 04                   je     4d <_FpuTexpX@12+0x4d>
  49:   db 28                   fld    TBYTE PTR [eax]
  4b:   eb 67                   jmp    b4 <_FpuTexpX@12+0xb4>
  4d:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
  54:   74 04                   je     5a <_FpuTexpX@12+0x5a>
  56:   dd 00                   fld    QWORD PTR [eax]
  58:   eb 5a                   jmp    b4 <_FpuTexpX@12+0xb4>
  5a:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
  61:   74 04                   je     67 <_FpuTexpX@12+0x67>
  63:   d9 00                   fld    DWORD PTR [eax]
  65:   eb 4d                   jmp    b4 <_FpuTexpX@12+0xb4>
  67:   f7 45 10 04 00 00 00    test   DWORD PTR [ebp+0x10],0x4
  6e:   74 04                   je     74 <_FpuTexpX@12+0x74>
  70:   db 00                   fild   DWORD PTR [eax]
  72:   eb 40                   jmp    b4 <_FpuTexpX@12+0xb4>
  74:   f7 45 10 00 00 00 01    test   DWORD PTR [ebp+0x10],0x1000000
  7b:   74 04                   je     81 <_FpuTexpX@12+0x81>
  7d:   df 28                   fild   QWORD PTR [eax]
  7f:   eb 33                   jmp    b4 <_FpuTexpX@12+0xb4>
  81:   f7 45 10 08 00 00 00    test   DWORD PTR [ebp+0x10],0x8
  88:   74 05                   je     8f <_FpuTexpX@12+0x8f>
  8a:   db 45 08                fild   DWORD PTR [ebp+0x8]
  8d:   eb 25                   jmp    b4 <_FpuTexpX@12+0xb4>
  8f:   dd 65 94                frstor [ebp-0x6c]
  92:   33 c0                   xor    eax,eax
  94:   c9                      leave
  95:   c2 0c 00                ret    0xc
  98:   83 f8 01                cmp    eax,0x1
  9b:   74 04                   je     a1 <_FpuTexpX@12+0xa1>
  9d:   d9 eb                   fldpi
  9f:   eb 13                   jmp    b4 <_FpuTexpX@12+0xb4>
  a1:   83 f8 02                cmp    eax,0x2
  a4:   74 e9                   je     8f <_FpuTexpX@12+0x8f>
```

```
  a6:   d9 e8                   fld1
  a8:   d9 ea                   fldl2e
  aa:   d8 e1                   fsub   st,st(1)
  ac:   d9 f0                   f2xm1
  ae:   d8 c1                   fadd   st,st(1)
  b0:   d9 fd                   fscale
  b2:   dd d9                   fstp   st(1)
  b4:   d9 e9                   fldl2t
  b6:   de c9                   fmulp  st(1),st
  b8:   d9 c0                   fld    st(0)
  ba:   d9 fc                   frndint
  bc:   dc e9                   fsubr  st(1),st
  be:   d9 c9                   fxch   st(1)
  c0:   d9 f0                   f2xm1
  c2:   d9 e8                   fld1
  c4:   de c1                   faddp  st(1),st
  c6:   d9 fd                   fscale
  c8:   9b df e0                fstsw  ax
  cb:   9b                      fwait
  cc:   d0 e8                   shr    al,1
  ce:   72 bf                   jb     8f <_FpuTexpX@12+0x8f>
  d0:   dd d9                   fstp   st(1)
  d2:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  d9:   74 05                   je     e0 <_FpuTexpX@12+0xe0>
  db:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
  de:   eb 1f                   jmp    ff <_FpuTexpX@12+0xff>
  e0:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  e3:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
  ea:   74 04                   je     f0 <_FpuTexpX@12+0xf0>
  ec:   d9 18                   fstp   DWORD PTR [eax]
  ee:   eb 0f                   jmp    ff <_FpuTexpX@12+0xff>
  f0:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
  f7:   74 04                   je     fd <_FpuTexpX@12+0xfd>
  f9:   dd 18                   fstp   QWORD PTR [eax]
  fb:   eb 02                   jmp    ff <_FpuTexpX@12+0xff>
  fd:   db 38                   fstp   TBYTE PTR [eax]
  ff:   dd 65 94                frstor [ebp-0x6c]
 102:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
 109:   74 02                   je     10d <_FpuTexpX@12+0x10d>
 10b:   dd d8                   fstp   st(0)
 10d:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
 114:   74 05                   je     11b <_FpuTexpX@12+0x11b>
 116:   dd c7                   ffree  st(7)
 118:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
 11b:   0c 01                   or     al,0x1
 11d:   c9                      leave
 11e:   c2 0c 00                ret    0xc

FpuTanh.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuTanh@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuTanh@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuTanh@12+0x1c>
  18:   7a 02                   jp     1c <_FpuTanh@12+0x1c>
  1a:   74 6a                   je     86 <_FpuTanh@12+0x86>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 08                   je     31 <_FpuTanh@12+0x31>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
```

```
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   eb 5b                   jmp    8c <_FpuTanh@12+0x8c>
  31:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  34:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
  3b:   74 04                   je     41 <_FpuTanh@12+0x41>
  3d:   db 28                   fld    TBYTE PTR [eax]
  3f:   eb 4b                   jmp    8c <_FpuTanh@12+0x8c>
  41:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
  48:   74 04                   je     4e <_FpuTanh@12+0x4e>
  4a:   dd 00                   fld    QWORD PTR [eax]
  4c:   eb 3e                   jmp    8c <_FpuTanh@12+0x8c>
  4e:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
  55:   74 04                   je     5b <_FpuTanh@12+0x5b>
  57:   d9 00                   fld    DWORD PTR [eax]
  59:   eb 31                   jmp    8c <_FpuTanh@12+0x8c>
  5b:   f7 45 10 04 00 00 00    test   DWORD PTR [ebp+0x10],0x4
  62:   74 04                   je     68 <_FpuTanh@12+0x68>
  64:   db 00                   fild   DWORD PTR [eax]
  66:   eb 24                   jmp    8c <_FpuTanh@12+0x8c>
  68:   f7 45 10 00 00 00 01    test   DWORD PTR [ebp+0x10],0x1000000
  6f:   74 04                   je     75 <_FpuTanh@12+0x75>
  71:   df 28                   fild   QWORD PTR [eax]
  73:   eb 17                   jmp    8c <_FpuTanh@12+0x8c>
  75:   f7 45 10 08 00 00 00    test   DWORD PTR [ebp+0x10],0x8
  7c:   74 05                   je     83 <_FpuTanh@12+0x83>
  7e:   db 45 08                fild   DWORD PTR [ebp+0x8]
  81:   eb 09                   jmp    8c <_FpuTanh@12+0x8c>
  83:   dd 65 94                frstor [ebp-0x6c]
  86:   33 c0                   xor    eax,eax
  88:   c9                      leave
  89:   c2 0c 00                ret    0xc
  8c:   d9 c0                   fld    st(0)
  8e:   68 81 00 00 00          push   0x81
  93:   6a 00                   push   0x0
  95:   6a 00                   push   0x0
  97:   e8 00 00 00 00          call   9c <_FpuTanh@12+0x9c>
  9c:   0b c0                   or     eax,eax
  9e:   74 e3                   je     83 <_FpuTanh@12+0x83>
  a0:   d9 c9                   fxch   st(1)
  a2:   68 81 00 00 00          push   0x81
  a7:   6a 00                   push   0x0
  a9:   6a 00                   push   0x0
  ab:   e8 00 00 00 00          call   b0 <_FpuTanh@12+0xb0>
  b0:   0b c0                   or     eax,eax
  b2:   74 cf                   je     83 <_FpuTanh@12+0x83>
  b4:   de f9                   fdivrp st(1),st
  b6:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  bd:   74 05                   je     c4 <_FpuTanh@12+0xc4>
  bf:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
  c2:   eb 1f                   jmp    e3 <_FpuTanh@12+0xe3>
  c4:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  c7:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
  ce:   74 04                   je     d4 <_FpuTanh@12+0xd4>
  d0:   d9 18                   fstp   DWORD PTR [eax]
  d2:   eb 0f                   jmp    e3 <_FpuTanh@12+0xe3>
  d4:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
  db:   74 04                   je     e1 <_FpuTanh@12+0xe1>
  dd:   dd 18                   fstp   QWORD PTR [eax]
  df:   eb 02                   jmp    e3 <_FpuTanh@12+0xe3>
  e1:   db 38                   fstp   TBYTE PTR [eax]
  e3:   dd 65 94                frstor [ebp-0x6c]
  e6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  ed:   74 02                   je     f1 <_FpuTanh@12+0xf1>
  ef:   dd d8                   fstp   st(0)
  f1:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  f8:   74 05                   je     ff <_FpuTanh@12+0xff>
  fa:   dd c7                   ffree  st(7)
  fc:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
  ff:   0c 01                   or     al,0x1
 101:   c9                      leave
```

```
 102:   c2 0c 00                ret    0xc

Disassembly of section .drectve:

00000000 <.drectve>:
   0:   2d 64 65 66 61          sub    eax,0x61666564
   5:   75 6c                   jne    73 <.drectve+0x73>
   7:   74 6c                   je     75 <.drectve+0x75>
   9:   69 62 3a 46 70 75 2e    imul   esp,DWORD PTR [edx+0x3a],0x2e757046
  10:   6c                      ins    BYTE PTR es:[edi],dx
  11:   69                      .byte 0x69
  12:   62 20                   bound  esp,QWORD PTR [eax]

FpuTan.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuTan@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuTan@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuTan@12+0x1c>
  18:   7a 02                   jp     1c <_FpuTan@12+0x1c>
  1a:   74 6a                   je     86 <_FpuTan@12+0x86>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 08                   je     31 <_FpuTan@12+0x31>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   eb 5b                   jmp    8c <_FpuTan@12+0x8c>
  31:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  34:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
  3b:   74 04                   je     41 <_FpuTan@12+0x41>
  3d:   db 28                   fld    TBYTE PTR [eax]
  3f:   eb 4b                   jmp    8c <_FpuTan@12+0x8c>
  41:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
  48:   74 04                   je     4e <_FpuTan@12+0x4e>
  4a:   dd 00                   fld    QWORD PTR [eax]
  4c:   eb 3e                   jmp    8c <_FpuTan@12+0x8c>
  4e:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
  55:   74 04                   je     5b <_FpuTan@12+0x5b>
  57:   d9 00                   fld    DWORD PTR [eax]
  59:   eb 31                   jmp    8c <_FpuTan@12+0x8c>
  5b:   f7 45 10 04 00 00 00    test   DWORD PTR [ebp+0x10],0x4
  62:   74 04                   je     68 <_FpuTan@12+0x68>
  64:   db 00                   fild   DWORD PTR [eax]
  66:   eb 24                   jmp    8c <_FpuTan@12+0x8c>
  68:   f7 45 10 00 00 00 01    test   DWORD PTR [ebp+0x10],0x1000000
  6f:   74 04                   je     75 <_FpuTan@12+0x75>
  71:   df 28                   fild   QWORD PTR [eax]
  73:   eb 17                   jmp    8c <_FpuTan@12+0x8c>
  75:   f7 45 10 08 00 00 00    test   DWORD PTR [ebp+0x10],0x8
  7c:   74 05                   je     83 <_FpuTan@12+0x83>
  7e:   db 45 08                fild   DWORD PTR [ebp+0x8]
  81:   eb 09                   jmp    8c <_FpuTan@12+0x8c>
  83:   dd 65 94                frstor [ebp-0x6c]
  86:   33 c0                   xor    eax,eax
  88:   c9                      leave
  89:   c2 0c 00                ret    0xc
  8c:   d9 eb                   fldpi
  8e:   d8 c0                   fadd   st,st(0)
  90:   d9 c9                   fxch   st(1)
  92:   f7 45 10 20 00 00 00    test   DWORD PTR [ebp+0x10],0x20
```

```
  99:   75 0c                   jne    a7 <_FpuTan@12+0xa7>
  9b:   d8 c9                   fmul   st,st(1)
  9d:   68 68 01 00 00          push   0x168
  a2:   de 34 24                fidiv  WORD PTR [esp]
  a5:   9b                      fwait
  a6:   58                      pop    eax
  a7:   d9 f8                   fprem
  a9:   d9 f2                   fptan
  ab:   9b df e0                fstsw  ax
  ae:   9b                      fwait
  af:   d0 e8                   shr    al,1
  b1:   72 d0                   jb     83 <_FpuTan@12+0x83>
  b3:   9e                      sahf
  b4:   7a f1                   jp     a7 <_FpuTan@12+0xa7>
  b6:   dd d8                   fstp   st(0)
  b8:   dd d9                   fstp   st(1)
  ba:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  c1:   74 05                   je     c8 <_FpuTan@12+0xc8>
  c3:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
  c6:   eb 1f                   jmp    e7 <_FpuTan@12+0xe7>
  c8:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  cb:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
  d2:   74 04                   je     d8 <_FpuTan@12+0xd8>
  d4:   d9 18                   fstp   DWORD PTR [eax]
  d6:   eb 0f                   jmp    e7 <_FpuTan@12+0xe7>
  d8:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
  df:   74 04                   je     e5 <_FpuTan@12+0xe5>
  e1:   dd 18                   fstp   QWORD PTR [eax]
  e3:   eb 02                   jmp    e7 <_FpuTan@12+0xe7>
  e5:   db 38                   fstp   TBYTE PTR [eax]
  e7:   dd 65 94                frstor [ebp-0x6c]
  ea:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  f1:   74 02                   je     f5 <_FpuTan@12+0xf5>
  f3:   dd d8                   fstp   st(0)
  f5:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  fc:   74 05                   je     103 <_FpuTan@12+0x103>
  fe:   dd c7                   ffree  st(7)
 100:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
 103:   0c 01                   or     al,0x1
 105:   c9                      leave
 106:   c2 0c 00                ret    0xc

FpuSub.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuSub@16>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 14 01 01 00 00    test   DWORD PTR [ebp+0x14],0x101
   d:   74 0d                   je     1c <_FpuSub@16+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuSub@16+0x1c>
  18:   7a 02                   jp     1c <_FpuSub@16+0x1c>
  1a:   74 76                   je     92 <_FpuSub@16+0x92>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 14 01 00 00 00    test   DWORD PTR [ebp+0x14],0x1
  27:   74 0b                   je     34 <_FpuSub@16+0x34>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   e9 80 00 00 00          jmp    b4 <_FpuSub@16+0xb4>
  34:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  37:   f7 45 14 10 00 00 00    test   DWORD PTR [ebp+0x14],0x10
  3e:   75 58                   jne    98 <_FpuSub@16+0x98>
  40:   f7 45 14 02 00 00 00    test   DWORD PTR [ebp+0x14],0x2
```

```
 47:   74 04                   je     4d <_FpuSub@16+0x4d>
 49:   db 28                   fld    TBYTE PTR [eax]
 4b:   eb 67                   jmp    b4 <_FpuSub@16+0xb4>
 4d:   f7 45 14 00 00 02 00    test   DWORD PTR [ebp+0x14],0x20000
 54:   74 04                   je     5a <_FpuSub@16+0x5a>
 56:   dd 00                   fld    QWORD PTR [eax]
 58:   eb 5a                   jmp    b4 <_FpuSub@16+0xb4>
 5a:   f7 45 14 00 00 01 00    test   DWORD PTR [ebp+0x14],0x10000
 61:   74 04                   je     67 <_FpuSub@16+0x67>
 63:   d9 00                   fld    DWORD PTR [eax]
 65:   eb 4d                   jmp    b4 <_FpuSub@16+0xb4>
 67:   f7 45 14 04 00 00 00    test   DWORD PTR [ebp+0x14],0x4
 6e:   74 04                   je     74 <_FpuSub@16+0x74>
 70:   db 00                   fild   DWORD PTR [eax]
 72:   eb 40                   jmp    b4 <_FpuSub@16+0xb4>
 74:   f7 45 14 00 00 00 01    test   DWORD PTR [ebp+0x14],0x1000000
 7b:   74 04                   je     81 <_FpuSub@16+0x81>
 7d:   df 28                   fild   QWORD PTR [eax]
 7f:   eb 33                   jmp    b4 <_FpuSub@16+0xb4>
 81:   f7 45 14 08 00 00 00    test   DWORD PTR [ebp+0x14],0x8
 88:   74 05                   je     8f <_FpuSub@16+0x8f>
 8a:   db 45 08                fild   DWORD PTR [ebp+0x8]
 8d:   eb 25                   jmp    b4 <_FpuSub@16+0xb4>
 8f:   dd 65 94                frstor [ebp-0x6c]
 92:   33 c0                   xor    eax,eax
 94:   c9                      leave
 95:   c2 10 00                ret    0x10
 98:   83 f8 01                cmp    eax,0x1
 9b:   75 04                   jne    a1 <_FpuSub@16+0xa1>
 9d:   d9 eb                   fldpi
 9f:   eb 13                   jmp    b4 <_FpuSub@16+0xb4>
 a1:   83 f8 02                cmp    eax,0x2
 a4:   75 e9                   jne    8f <_FpuSub@16+0x8f>
 a6:   d9 e8                   fld1
 a8:   d9 ea                   fldl2e
 aa:   d8 e1                   fsub   st,st(1)
 ac:   d9 f0                   f2xm1
 ae:   d8 c1                   fadd   st,st(1)
 b0:   d9 fd                   fscale
 b2:   dd d9                   fstp   st(1)
 b4:   f7 45 14 00 01 00 00    test   DWORD PTR [ebp+0x14],0x100
 bb:   74 0b                   je     c8 <_FpuSub@16+0xc8>
 bd:   8d 45 94                lea    eax,[ebp-0x6c]
 c0:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
 c3:   e9 80 00 00 00          jmp    148 <_FpuSub@16+0x148>
 c8:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
 cb:   f7 45 14 00 10 00 00    test   DWORD PTR [ebp+0x14],0x1000
 d2:   75 54                   jne    128 <_FpuSub@16+0x128>
 d4:   f7 45 14 00 02 00 00    test   DWORD PTR [ebp+0x14],0x200
 db:   74 04                   je     e1 <_FpuSub@16+0xe1>
 dd:   db 28                   fld    TBYTE PTR [eax]
 df:   eb 67                   jmp    148 <_FpuSub@16+0x148>
 e1:   f7 45 14 00 00 08 00    test   DWORD PTR [ebp+0x14],0x80000
 e8:   74 04                   je     ee <_FpuSub@16+0xee>
 ea:   dd 00                   fld    QWORD PTR [eax]
 ec:   eb 5a                   jmp    148 <_FpuSub@16+0x148>
 ee:   f7 45 14 00 00 04 00    test   DWORD PTR [ebp+0x14],0x40000
 f5:   74 04                   je     fb <_FpuSub@16+0xfb>
 f7:   d9 00                   fld    DWORD PTR [eax]
 f9:   eb 4d                   jmp    148 <_FpuSub@16+0x148>
 fb:   f7 45 14 00 04 00 00    test   DWORD PTR [ebp+0x14],0x400
102:   74 04                   je     108 <_FpuSub@16+0x108>
104:   db 00                   fild   DWORD PTR [eax]
106:   eb 40                   jmp    148 <_FpuSub@16+0x148>
108:   f7 45 14 00 00 00 02    test   DWORD PTR [ebp+0x14],0x2000000
10f:   74 04                   je     115 <_FpuSub@16+0x115>
111:   df 28                   fild   QWORD PTR [eax]
113:   eb 33                   jmp    148 <_FpuSub@16+0x148>
115:   f7 45 14 00 08 00 00    test   DWORD PTR [ebp+0x14],0x800
11c:   74 05                   je     123 <_FpuSub@16+0x123>
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 11e:   db 45 0c                fild   DWORD PTR [ebp+0xc]
 121:   eb 25                   jmp    148 <_FpuSub@16+0x148>
 123:   e9 67 ff ff ff          jmp    8f <_FpuSub@16+0x8f>
 128:   83 f8 01                cmp    eax,0x1
 12b:   75 04                   jne    131 <_FpuSub@16+0x131>
 12d:   d9 eb                   fldpi
 12f:   eb 17                   jmp    148 <_FpuSub@16+0x148>
 131:   83 f8 02                cmp    eax,0x2
 134:   0f 85 55 ff ff ff       jne    8f <_FpuSub@16+0x8f>
 13a:   d9 e8                   fld1
 13c:   d9 ea                   fldl2e
 13e:   d8 e1                   fsub   st,st(1)
 140:   d9 f0                   f2xm1
 142:   d8 c1                   fadd   st,st(1)
 144:   d9 fd                   fscale
 146:   dd d9                   fstp   st(1)
 148:   de e9                   fsubrp st(1),st
 14a:   9b df e0                fstsw  ax
 14d:   9b                      fwait
 14e:   d1 e8                   shr    eax,1
 150:   0f 82 39 ff ff ff       jb     8f <_FpuSub@16+0x8f>
 156:   f7 45 14 80 00 00 00    test   DWORD PTR [ebp+0x14],0x80
 15d:   74 05                   je     164 <_FpuSub@16+0x164>
 15f:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
 162:   eb 1f                   jmp    183 <_FpuSub@16+0x183>
 164:   8b 45 10                mov    eax,DWORD PTR [ebp+0x10]
 167:   f7 45 14 00 00 10 00    test   DWORD PTR [ebp+0x14],0x100000
 16e:   74 04                   je     174 <_FpuSub@16+0x174>
 170:   d9 18                   fstp   DWORD PTR [eax]
 172:   eb 0f                   jmp    183 <_FpuSub@16+0x183>
 174:   f7 45 14 00 00 20 00    test   DWORD PTR [ebp+0x14],0x200000
 17b:   74 04                   je     181 <_FpuSub@16+0x181>
 17d:   dd 18                   fstp   QWORD PTR [eax]
 17f:   eb 02                   jmp    183 <_FpuSub@16+0x183>
 181:   db 38                   fstp   TBYTE PTR [eax]
 183:   dd 65 94                frstor [ebp-0x6c]
 186:   f7 45 14 01 01 00 00    test   DWORD PTR [ebp+0x14],0x101
 18d:   74 02                   je     191 <_FpuSub@16+0x191>
 18f:   dd d8                   fstp   st(0)
 191:   f7 45 14 80 00 00 00    test   DWORD PTR [ebp+0x14],0x80
 198:   74 05                   je     19f <_FpuSub@16+0x19f>
 19a:   dd c7                   ffree  st(7)
 19c:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
 19f:   0c 01                   or     al,0x1
 1a1:   c9                      leave
 1a2:   c2 10 00                ret    0x10

FpuState.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuState@8>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 90                add    esp,0xffffff90
   6:   9c                      pushf
   7:   60                      pusha
   8:   9b dd 75 94             fsave  [ebp-0x6c]
   c:   9b                      fwait
   d:   8d 75 94                lea    esi,[ebp-0x6c]
  10:   8b 7d 08                mov    edi,DWORD PTR [ebp+0x8]
  13:   b8 49 44 20 20          mov    eax,0x20204449
  18:   ab                      stos   DWORD PTR es:[edi],eax
  19:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  1c:   33 c9                   xor    ecx,ecx
  1e:   51                      push   ecx
  1f:   b1 0a                   mov    cl,0xa
  21:   33 d2                   xor    edx,edx
  23:   f7 f1                   div    ecx
```

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  25:   80 c2 30                add    dl,0x30
  28:   52                      push   edx
  29:   0b c0                   or     eax,eax
  2b:   75 f4                   jne    21 <_FpuState@8+0x21>
  2d:   58                      pop    eax
  2e:   0b c0                   or     eax,eax
  30:   74 03                   je     35 <_FpuState@8+0x35>
  32:   aa                      stos   BYTE PTR es:[edi],al
  33:   eb f8                   jmp    2d <_FpuState@8+0x2d>
  35:   66 b8 0d 0a             mov    ax,0xa0d
  39:   66 ab                   stos   WORD PTR es:[edi],ax
  3b:   b8 43 57 20 20          mov    eax,0x20205743
  40:   ab                      stos   DWORD PTR es:[edi],eax
  41:   ad                      lods   eax,DWORD PTR ds:[esi]
  42:   c1 e0 10                shl    eax,0x10
  45:   b9 04 00 00 00          mov    ecx,0x4
  4a:   b0 00                   mov    al,0x0
  4c:   d1 c0                   rol    eax,1
  4e:   b4 20                   mov    ah,0x20
  50:   04 30                   add    al,0x30
  52:   66 ab                   stos   WORD PTR es:[edi],ax
  54:   49                      dec    ecx
  55:   75 f3                   jne    4a <_FpuState@8+0x4a>
  57:   66 33 c0                xor    ax,ax
  5a:   c1 c0 02                rol    eax,0x2
  5d:   66 d1 c8                ror    ax,1
  60:   d0 c4                   rol    ah,1
  62:   66 05 30 30             add    ax,0x3030
  66:   66 ab                   stos   WORD PTR es:[edi],ax
  68:   b0 20                   mov    al,0x20
  6a:   aa                      stos   BYTE PTR es:[edi],al
  6b:   66 33 c0                xor    ax,ax
  6e:   c1 c0 02                rol    eax,0x2
  71:   66 d1 c8                ror    ax,1
  74:   d0 c4                   rol    ah,1
  76:   66 05 30 30             add    ax,0x3030
  7a:   66 ab                   stos   WORD PTR es:[edi],ax
  7c:   66 b8 20 20             mov    ax,0x2020
  80:   66 ab                   stos   WORD PTR es:[edi],ax
  82:   b9 08 00 00 00          mov    ecx,0x8
  87:   b0 00                   mov    al,0x0
  89:   d1 c0                   rol    eax,1
  8b:   b4 20                   mov    ah,0x20
  8d:   04 30                   add    al,0x30
  8f:   66 ab                   stos   WORD PTR es:[edi],ax
  91:   49                      dec    ecx
  92:   75 f3                   jne    87 <_FpuState@8+0x87>
  94:   4f                      dec    edi
  95:   66 b8 0d 0a             mov    ax,0xa0d
  99:   66 ab                   stos   WORD PTR es:[edi],ax
  9b:   b8 53 57 20 20          mov    eax,0x20205753
  a0:   ab                      stos   DWORD PTR es:[edi],eax
  a1:   ad                      lods   eax,DWORD PTR ds:[esi]
  a2:   c1 e0 10                shl    eax,0x10
  a5:   b9 02 00 00 00          mov    ecx,0x2
  aa:   b0 00                   mov    al,0x0
  ac:   d1 c0                   rol    eax,1
  ae:   b4 20                   mov    ah,0x20
  b0:   04 30                   add    al,0x30
  b2:   66 ab                   stos   WORD PTR es:[edi],ax
  b4:   49                      dec    ecx
  b5:   75 f3                   jne    aa <_FpuState@8+0xaa>
  b7:   66 33 c0                xor    ax,ax
  ba:   c1 c0 03                rol    eax,0x3
  bd:   88 45 90                mov    BYTE PTR [ebp-0x70],al
  c0:   50                      push   eax
  c1:   83 e0 07                and    eax,0x7
  c4:   66 d1 c8                ror    ax,1
  c7:   d1 c0                   rol    eax,1
  c9:   66 c1 c8 02             ror    ax,0x2
```

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  cd:   d0 c4                   rol    ah,1
  cf:   05 30 30 30 20          add    eax,0x20303030
  d4:   ab                      stos   DWORD PTR es:[edi],eax
  d5:   58                      pop    eax
  d6:   b9 03 00 00 00          mov    ecx,0x3
  db:   b0 00                   mov    al,0x0
  dd:   d1 c0                   rol    eax,1
  df:   b4 20                   mov    ah,0x20
  e1:   04 30                   add    al,0x30
  e3:   66 ab                   stos   WORD PTR es:[edi],ax
  e5:   49                      dec    ecx
  e6:   75 f3                   jne    db <_FpuState@8+0xdb>
  e8:   b0 20                   mov    al,0x20
  ea:   aa                      stos   BYTE PTR es:[edi],al
  eb:   b0 00                   mov    al,0x0
  ed:   d1 c0                   rol    eax,1
  ef:   04 30                   add    al,0x30
  f1:   b4 20                   mov    ah,0x20
  f3:   66 ab                   stos   WORD PTR es:[edi],ax
  f5:   b9 07 00 00 00          mov    ecx,0x7
  fa:   eb 08                   jmp    104 <szflags+0x8>

000000fc <szflags>:
  fc:   20 49 44                and    BYTE PTR [ecx+0x44],cl
  ff:   5a                      pop    edx
 100:   4f                      dec    edi
 101:   55                      push   ebp
 102:   50                      push   eax
 103:   53                      push   ebx
 104:   b0 00                   mov    al,0x0
 106:   d1 c0                   rol    eax,1
 108:   b4 20                   mov    ah,0x20
 10a:   3c 01                   cmp    al,0x1
 10c:   75 08                   jne    116 <szflags+0x1a>
 10e:   8a 81 00 00 00 00       mov    al,BYTE PTR [ecx+0x0]
 114:   eb 08                   jmp    11e <szflags+0x22>
 116:   8a 81 00 00 00 00       mov    al,BYTE PTR [ecx+0x0]
 11c:   0c 20                   or     al,0x20
 11e:   66 ab                   stos   WORD PTR es:[edi],ax
 120:   49                      dec    ecx
 121:   75 e1                   jne    104 <szflags+0x8>
 123:   4f                      dec    edi
 124:   66 b8 0d 0a             mov    ax,0xa0d
 128:   66 ab                   stos   WORD PTR es:[edi],ax
 12a:   b8 54 57 20 20          mov    eax,0x20205754
 12f:   ab                      stos   DWORD PTR es:[edi],eax
 130:   ad                      lods   eax,DWORD PTR ds:[esi]
 131:   8a 4d 90                mov    cl,BYTE PTR [ebp-0x70]
 134:   d0 e1                   shl    cl,1
 136:   66 d3 c8                ror    ax,cl
 139:   c1 e0 10                shl    eax,0x10
 13c:   b9 08 00 00 00          mov    ecx,0x8
 141:   b0 00                   mov    al,0x0
 143:   c1 c8 02                ror    eax,0x2
 146:   66 c1 c0 02             rol    ax,0x2
 14a:   50                      push   eax
 14b:   0a c0                   or     al,al
 14d:   75 07                   jne    156 <szflags+0x5a>
 14f:   b8 56 41 4c 20          mov    eax,0x204c4156
 154:   eb 1b                   jmp    171 <szflags+0x75>
 156:   3c 01                   cmp    al,0x1
 158:   75 07                   jne    161 <szflags+0x65>
 15a:   b8 4e 55 4c 20          mov    eax,0x204c554e
 15f:   eb 10                   jmp    171 <szflags+0x75>
 161:   3c 02                   cmp    al,0x2
 163:   75 07                   jne    16c <szflags+0x70>
 165:   b8 4e 61 4e 20          mov    eax,0x204e614e
 16a:   eb 05                   jmp    171 <szflags+0x75>
 16c:   b8 46 52 45 20          mov    eax,0x20455246
 171:   ab                      stos   DWORD PTR es:[edi],eax
```

```
172:   58                      pop    eax
173:   49                      dec    ecx
174:   75 cb                   jne    141 <szflags+0x45>
176:   4f                      dec    edi
177:   66 b8 0d 0a            mov    ax,0xa0d
17b:   66 ab                   stos   WORD PTR es:[edi],ax
17d:   b8 49 50 20 20          mov    eax,0x20205049
182:   ab                      stos   DWORD PTR es:[edi],eax
183:   ad                      lods   eax,DWORD PTR ds:[esi]
184:   b9 08 00 00 00          mov    ecx,0x8
189:   c1 c0 04                rol    eax,0x4
18c:   50                      push   eax
18d:   24 0f                   and    al,0xf
18f:   04 30                   add    al,0x30
191:   3c 39                   cmp    al,0x39
193:   76 02                   jbe    197 <szflags+0x9b>
195:   04 07                   add    al,0x7
197:   aa                      stos   BYTE PTR es:[edi],al
198:   58                      pop    eax
199:   49                      dec    ecx
19a:   75 ed                   jne    189 <szflags+0x8d>
19c:   66 b8 0d 0a            mov    ax,0xa0d
1a0:   66 ab                   stos   WORD PTR es:[edi],ax
1a2:   b8 43 53 20 20          mov    eax,0x20205343
1a7:   ab                      stos   DWORD PTR es:[edi],eax
1a8:   ad                      lods   eax,DWORD PTR ds:[esi]
1a9:   c1 e0 10                shl    eax,0x10
1ac:   b9 04 00 00 00          mov    ecx,0x4
1b1:   c1 c0 04                rol    eax,0x4
1b4:   50                      push   eax
1b5:   24 0f                   and    al,0xf
1b7:   04 30                   add    al,0x30
1b9:   3c 39                   cmp    al,0x39
1bb:   76 02                   jbe    1bf <szflags+0xc3>
1bd:   04 07                   add    al,0x7
1bf:   aa                      stos   BYTE PTR es:[edi],al
1c0:   58                      pop    eax
1c1:   49                      dec    ecx
1c2:   75 ed                   jne    1b1 <szflags+0xb5>
1c4:   66 b8 0d 0a            mov    ax,0xa0d
1c8:   66 ab                   stos   WORD PTR es:[edi],ax
1ca:   b8 4f 41 20 20          mov    eax,0x2020414f
1cf:   ab                      stos   DWORD PTR es:[edi],eax
1d0:   ad                      lods   eax,DWORD PTR ds:[esi]
1d1:   b9 08 00 00 00          mov    ecx,0x8
1d6:   c1 c0 04                rol    eax,0x4
1d9:   50                      push   eax
1da:   24 0f                   and    al,0xf
1dc:   04 30                   add    al,0x30
1de:   3c 39                   cmp    al,0x39
1e0:   76 02                   jbe    1e4 <szflags+0xe8>
1e2:   04 07                   add    al,0x7
1e4:   aa                      stos   BYTE PTR es:[edi],al
1e5:   58                      pop    eax
1e6:   49                      dec    ecx
1e7:   75 ed                   jne    1d6 <szflags+0xda>
1e9:   66 b8 0d 0a            mov    ax,0xa0d
1ed:   66 ab                   stos   WORD PTR es:[edi],ax
1ef:   b8 44 53 20 20          mov    eax,0x20205344
1f4:   ab                      stos   DWORD PTR es:[edi],eax
1f5:   ad                      lods   eax,DWORD PTR ds:[esi]
1f6:   c1 e0 10                shl    eax,0x10
1f9:   b9 04 00 00 00          mov    ecx,0x4
1fe:   c1 c0 04                rol    eax,0x4
201:   50                      push   eax
202:   24 0f                   and    al,0xf
204:   04 30                   add    al,0x30
206:   3c 39                   cmp    al,0x39
208:   76 02                   jbe    20c <szflags+0x110>
20a:   04 07                   add    al,0x7
```

```
20c:   aa                      stos   BYTE PTR es:[edi],al
20d:   58                      pop    eax
20e:   49                      dec    ecx
20f:   75 ed                   jne    1fe <szflags+0x102>
211:   66 b8 0d 0a             mov    ax,0xa0d
215:   66 ab                   stos   WORD PTR es:[edi],ax
217:   33 c9                   xor    ecx,ecx
219:   66 b8 0d 0a             mov    ax,0xa0d
21d:   66 ab                   stos   WORD PTR es:[edi],ax
21f:   51                      push   ecx
220:   b8 53 54 30 20          mov    eax,0x20305453
225:   c1 e1 10                shl    ecx,0x10
228:   03 c1                   add    eax,ecx
22a:   ab                      stos   DWORD PTR es:[edi],eax
22b:   c1 e9 10                shr    ecx,0x10
22e:   02 4d 90                add    cl,BYTE PTR [ebp-0x70]
231:   80 e1 07                and    cl,0x7
234:   d0 e1                   shl    cl,1
236:   8d 45 9c                lea    eax,[ebp-0x64]
239:   66 8b 00                mov    ax,WORD PTR [eax]
23c:   d3 e8                   shr    eax,cl
23e:   24 03                   and    al,0x3
240:   3c 03                   cmp    al,0x3
242:   75 0e                   jne    252 <szflags+0x156>
244:   b8 20 45 4d 50          mov    eax,0x504d4520
249:   ab                      stos   DWORD PTR es:[edi],eax
24a:   66 b8 54 59             mov    ax,0x5954
24e:   66 ab                   stos   WORD PTR es:[edi],ax
250:   eb 79                   jmp    2cb <szflags+0x1cf>
252:   3c 01                   cmp    al,0x1
254:   75 1d                   jne    273 <szflags+0x177>
256:   6a 02                   push   0x2
258:   56                      push   esi
259:   e8 00 00 00 00          call   25e <szflags+0x162>
25e:   b2 2b                   mov    dl,0x2b
260:   a9 04 00 00 00          test   eax,0x4
265:   74 02                   je     269 <szflags+0x16d>
267:   b2 2d                   mov    dl,0x2d
269:   b8 20 20 30 20          mov    eax,0x20302020
26e:   8a e2                   mov    ah,dl
270:   ab                      stos   DWORD PTR es:[edi],eax
271:   eb 58                   jmp    2cb <szflags+0x1cf>
273:   0a c0                   or     al,al
275:   75 13                   jne    28a <szflags+0x18e>
277:   68 02 88 00 00          push   0x8802
27c:   57                      push   edi
27d:   6a 0f                   push   0xf
27f:   56                      push   esi
280:   e8 00 00 00 00          call   285 <szflags+0x189>
285:   83 c7 18                add    edi,0x18
288:   eb 41                   jmp    2cb <szflags+0x1cf>
28a:   6a 02                   push   0x2
28c:   56                      push   esi
28d:   e8 00 00 00 00          call   292 <szflags+0x196>
292:   a9 01 00 00 00          test   eax,0x1
297:   75 14                   jne    2ad <szflags+0x1b1>
299:   b8 20 49 4e 44          mov    eax,0x444e4920
29e:   ab                      stos   DWORD PTR es:[edi],eax
29f:   b8 45 46 49 4e          mov    eax,0x4e494645
2a4:   ab                      stos   DWORD PTR es:[edi],eax
2a5:   b8 49 54 45 20          mov    eax,0x20455449
2aa:   ab                      stos   DWORD PTR es:[edi],eax
2ab:   eb 1e                   jmp    2cb <szflags+0x1cf>
2ad:   66 ba 20 2b             mov    dx,0x2b20
2b1:   a9 04 00 00 00          test   eax,0x4
2b6:   74 02                   je     2ba <szflags+0x1be>
2b8:   b6 2d                   mov    dh,0x2d
2ba:   66 8b c2                mov    ax,dx
2bd:   66 ab                   stos   WORD PTR es:[edi],ax
2bf:   b8 49 4e 46 49          mov    eax,0x49464e49
```

```
 2c4:   ab                      stos   DWORD PTR es:[edi],eax
 2c5:   b8 4e 49 54 59          mov    eax,0x5954494e
 2ca:   ab                      stos   DWORD PTR es:[edi],eax
 2cb:   83 c6 0a                add    esi,0xa
 2ce:   59                      pop    ecx
 2cf:   41                      inc    ecx
 2d0:   80 f9 08                cmp    cl,0x8
 2d3:   0f 82 40 ff ff ff       jb     219 <szflags+0x11d>
 2d9:   c6 07 00                mov    BYTE PTR [edi],0x0
 2dc:   dd 65 94                frstor [ebp-0x6c]
 2df:   9b                      fwait
 2e0:   61                      popa
 2e1:   9d                      popf
 2e2:   c9                      leave
 2e3:   c2 08 00                ret    0x8

Disassembly of section .drectve:

00000000 <.drectve>:
   0:   2d 64 65 66 61          sub    eax,0x61666564
   5:   75 6c                   jne    73 <.drectve+0x73>
   7:   74 6c                   je     75 <.drectve+0x75>
   9:   69 62 3a 46 70 75 2e    imul   esp,DWORD PTR [edx+0x3a],0x2e757046
  10:   6c                      ins    BYTE PTR es:[edi],dx
  11:   69                      .byte 0x69
  12:   62 20                   bound  esp,QWORD PTR [eax]

FpuSqrt.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuSqrt@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuSqrt@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuSqrt@12+0x1c>
  18:   7a 02                   jp     1c <_FpuSqrt@12+0x1c>
  1a:   74 76                   je     92 <_FpuSqrt@12+0x92>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 0b                   je     34 <_FpuSqrt@12+0x34>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   e9 80 00 00 00          jmp    b4 <_FpuSqrt@12+0xb4>
  34:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  37:   f7 45 10 10 00 00 00    test   DWORD PTR [ebp+0x10],0x10
  3e:   75 58                   jne    98 <_FpuSqrt@12+0x98>
  40:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
  47:   74 04                   je     4d <_FpuSqrt@12+0x4d>
  49:   db 28                   fld    TBYTE PTR [eax]
  4b:   eb 67                   jmp    b4 <_FpuSqrt@12+0xb4>
  4d:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
  54:   74 04                   je     5a <_FpuSqrt@12+0x5a>
  56:   dd 00                   fld    QWORD PTR [eax]
  58:   eb 5a                   jmp    b4 <_FpuSqrt@12+0xb4>
  5a:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
  61:   74 04                   je     67 <_FpuSqrt@12+0x67>
  63:   d9 00                   fld    DWORD PTR [eax]
  65:   eb 4d                   jmp    b4 <_FpuSqrt@12+0xb4>
  67:   f7 45 10 04 00 00 00    test   DWORD PTR [ebp+0x10],0x4
  6e:   74 04                   je     74 <_FpuSqrt@12+0x74>
  70:   db 00                   fild   DWORD PTR [eax]
  72:   eb 40                   jmp    b4 <_FpuSqrt@12+0xb4>
```

```
  74:   f7 45 10 00 00 00 01    test   DWORD PTR [ebp+0x10],0x1000000
  7b:   74 04                   je     81 <_FpuSqrt@12+0x81>
  7d:   df 28                   fild   QWORD PTR [eax]
  7f:   eb 33                   jmp    b4 <_FpuSqrt@12+0xb4>
  81:   f7 45 10 08 00 00 00    test   DWORD PTR [ebp+0x10],0x8
  88:   74 05                   je     8f <_FpuSqrt@12+0x8f>
  8a:   db 45 08                fild   DWORD PTR [ebp+0x8]
  8d:   eb 25                   jmp    b4 <_FpuSqrt@12+0xb4>
  8f:   dd 65 94                frstor [ebp-0x6c]
  92:   33 c0                   xor    eax,eax
  94:   c9                      leave
  95:   c2 0c 00                ret    0xc
  98:   83 f8 01                cmp    eax,0x1
  9b:   74 04                   je     a1 <_FpuSqrt@12+0xa1>
  9d:   d9 eb                   fldpi
  9f:   eb 13                   jmp    b4 <_FpuSqrt@12+0xb4>
  a1:   83 f8 02                cmp    eax,0x2
  a4:   74 e9                   je     8f <_FpuSqrt@12+0x8f>
  a6:   d9 e8                   fld1
  a8:   d9 ea                   fldl2e
  aa:   d8 e1                   fsub   st,st(1)
  ac:   d9 f0                   f2xm1
  ae:   d8 c1                   fadd   st,st(1)
  b0:   d9 fd                   fscale
  b2:   dd d9                   fstp   st(1)
  b4:   d9 fa                   fsqrt
  b6:   9b df e0                fstsw  ax
  b9:   9b                      fwait
  ba:   d0 e8                   shr    al,1
  bc:   72 d1                   jb     8f <_FpuSqrt@12+0x8f>
  be:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  c5:   74 05                   je     cc <_FpuSqrt@12+0xcc>
  c7:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
  ca:   eb 1f                   jmp    eb <_FpuSqrt@12+0xeb>
  cc:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  cf:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
  d6:   74 04                   je     dc <_FpuSqrt@12+0xdc>
  d8:   d9 18                   fstp   DWORD PTR [eax]
  da:   eb 0f                   jmp    eb <_FpuSqrt@12+0xeb>
  dc:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
  e3:   74 04                   je     e9 <_FpuSqrt@12+0xe9>
  e5:   dd 18                   fstp   QWORD PTR [eax]
  e7:   eb 02                   jmp    eb <_FpuSqrt@12+0xeb>
  e9:   db 38                   fstp   TBYTE PTR [eax]
  eb:   dd 65 94                frstor [ebp-0x6c]
  ee:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  f5:   74 02                   je     f9 <_FpuSqrt@12+0xf9>
  f7:   dd d8                   fstp   st(0)
  f9:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
 100:   74 05                   je     107 <_FpuSqrt@12+0x107>
 102:   dd c7                   ffree  st(7)
 104:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
 107:   0c 01                   or     al,0x1
 109:   c9                      leave
 10a:   c2 0c 00                ret    0xc

FpuSize.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuSize@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuSize@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
```

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  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuSize@12+0x1c>
  18:   7a 02                   jp     1c <_FpuSize@12+0x1c>
  1a:   74 6a                   je     86 <_FpuSize@12+0x86>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 08                   je     31 <_FpuSize@12+0x31>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   eb 5b                   jmp    8c <_FpuSize@12+0x8c>
  31:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  34:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
  3b:   74 04                   je     41 <_FpuSize@12+0x41>
  3d:   db 28                   fld    TBYTE PTR [eax]
  3f:   eb 4b                   jmp    8c <_FpuSize@12+0x8c>
  41:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
  48:   74 04                   je     4e <_FpuSize@12+0x4e>
  4a:   dd 00                   fld    QWORD PTR [eax]
  4c:   eb 3e                   jmp    8c <_FpuSize@12+0x8c>
  4e:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
  55:   74 04                   je     5b <_FpuSize@12+0x5b>
  57:   d9 00                   fld    DWORD PTR [eax]
  59:   eb 31                   jmp    8c <_FpuSize@12+0x8c>
  5b:   f7 45 10 04 00 00 00    test   DWORD PTR [ebp+0x10],0x4
  62:   74 04                   je     68 <_FpuSize@12+0x68>
  64:   db 00                   fild   DWORD PTR [eax]
  66:   eb 24                   jmp    8c <_FpuSize@12+0x8c>
  68:   f7 45 10 00 00 00 01    test   DWORD PTR [ebp+0x10],0x1000000
  6f:   74 04                   je     75 <_FpuSize@12+0x75>
  71:   df 28                   fild   QWORD PTR [eax]
  73:   eb 17                   jmp    8c <_FpuSize@12+0x8c>
  75:   f7 45 10 08 00 00 00    test   DWORD PTR [ebp+0x10],0x8
  7c:   74 05                   je     83 <_FpuSize@12+0x83>
  7e:   db 45 08                fild   DWORD PTR [ebp+0x8]
  81:   eb 09                   jmp    8c <_FpuSize@12+0x8c>
  83:   dd 65 94                frstor [ebp-0x6c]
  86:   33 c0                   xor    eax,eax
  88:   c9                      leave
  89:   c2 0c 00                ret    0xc
  8c:   d9 e1                   fabs
  8e:   d9 e4                   ftst
  90:   9b df e0                fstsw  ax
  93:   9b                      fwait
  94:   9e                      sahf
  95:   75 0d                   jne    a4 <_FpuSize@12+0xa4>
  97:   72 ea                   jb     83 <_FpuSize@12+0x83>
  99:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  9c:   c7 00 00 00 00 80       mov    DWORD PTR [eax],0x80000000
  a2:   eb 28                   jmp    cc <_FpuSize@12+0xcc>
  a4:   d9 ec                   fldlg2
  a6:   d9 c9                   fxch   st(1)
  a8:   d9 f1                   fyl2x
  aa:   50                      push   eax
  ab:   9b d9 3c 24             fstcw  WORD PTR [esp]
  af:   9b                      fwait
  b0:   66 8b 04 24             mov    ax,WORD PTR [esp]
  b4:   66 25 ff f3             and    ax,0xf3ff
  b8:   66 0d 00 04             or     ax,0x400
  bc:   50                      push   eax
  bd:   d9 2c 24                fldcw  WORD PTR [esp]
  c0:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  c3:   db 18                   fistp  DWORD PTR [eax]
  c5:   d9 6c 24 04             fldcw  WORD PTR [esp+0x4]
  c9:   83 c4 08                add    esp,0x8
  cc:   dd 65 94                frstor [ebp-0x6c]
  cf:   0c 01                   or     al,0x1
  d1:   c9                      leave
  d2:   c2 0c 00                ret    0xc

FpuSinh.obj:     file format pe-i386
```

```
Disassembly of section .text:

00000000 <_FpuSinh@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuSinh@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuSinh@12+0x1c>
  18:   7a 02                   jp     1c <_FpuSinh@12+0x1c>
  1a:   74 6a                   je     86 <_FpuSinh@12+0x86>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 08                   je     31 <_FpuSinh@12+0x31>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   eb 5b                   jmp    8c <_FpuSinh@12+0x8c>
  31:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  34:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
  3b:   74 04                   je     41 <_FpuSinh@12+0x41>
  3d:   db 28                   fld    TBYTE PTR [eax]
  3f:   eb 4b                   jmp    8c <_FpuSinh@12+0x8c>
  41:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
  48:   74 04                   je     4e <_FpuSinh@12+0x4e>
  4a:   dd 00                   fld    QWORD PTR [eax]
  4c:   eb 3e                   jmp    8c <_FpuSinh@12+0x8c>
  4e:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
  55:   74 04                   je     5b <_FpuSinh@12+0x5b>
  57:   d9 00                   fld    DWORD PTR [eax]
  59:   eb 31                   jmp    8c <_FpuSinh@12+0x8c>
  5b:   f7 45 10 04 00 00 00    test   DWORD PTR [ebp+0x10],0x4
  62:   74 04                   je     68 <_FpuSinh@12+0x68>
  64:   db 00                   fild   DWORD PTR [eax]
  66:   eb 24                   jmp    8c <_FpuSinh@12+0x8c>
  68:   f7 45 10 00 00 00 01    test   DWORD PTR [ebp+0x10],0x1000000
  6f:   74 04                   je     75 <_FpuSinh@12+0x75>
  71:   df 28                   fild   QWORD PTR [eax]
  73:   eb 17                   jmp    8c <_FpuSinh@12+0x8c>
  75:   f7 45 10 08 00 00 00    test   DWORD PTR [ebp+0x10],0x8
  7c:   74 05                   je     83 <_FpuSinh@12+0x83>
  7e:   db 45 08                fild   DWORD PTR [ebp+0x8]
  81:   eb 09                   jmp    8c <_FpuSinh@12+0x8c>
  83:   dd 65 94                frstor [ebp-0x6c]
  86:   33 c0                   xor    eax,eax
  88:   c9                      leave
  89:   c2 0c 00                ret    0xc
  8c:   d9 ea                   fldl2e
  8e:   de c9                   fmulp  st(1),st
  90:   d9 c0                   fld    st(0)
  92:   d9 fc                   frndint
  94:   d9 c9                   fxch   st(1)
  96:   d8 e1                   fsub   st,st(1)
  98:   d9 f0                   f2xm1
  9a:   d9 e8                   fld1
  9c:   de c1                   faddp  st(1),st
  9e:   d9 fd                   fscale
  a0:   dd d9                   fstp   st(1)
  a2:   d9 c0                   fld    st(0)
  a4:   d9 e8                   fld1
  a6:   de f1                   fdivp  st(1),st
  a8:   de e9                   fsubrp st(1),st
  aa:   d9 e8                   fld1
  ac:   d9 e0                   fchs
  ae:   d9 c9                   fxch   st(1)
```

```
  b0:   d9 fd                   fscale
  b2:   dd d9                   fstp   st(1)
  b4:   9b df e0                fstsw  ax
  b7:   9b                      fwait
  b8:   d0 e8                   shr    al,1
  ba:   72 c7                   jb     83 <_FpuSinh@12+0x83>
  bc:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  c3:   74 05                   je     ca <_FpuSinh@12+0xca>
  c5:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
  c8:   eb 1f                   jmp    e9 <_FpuSinh@12+0xe9>
  ca:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  cd:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
  d4:   74 04                   je     da <_FpuSinh@12+0xda>
  d6:   d9 18                   fstp   DWORD PTR [eax]
  d8:   eb 0f                   jmp    e9 <_FpuSinh@12+0xe9>
  da:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
  e1:   74 04                   je     e7 <_FpuSinh@12+0xe7>
  e3:   dd 18                   fstp   QWORD PTR [eax]
  e5:   eb 02                   jmp    e9 <_FpuSinh@12+0xe9>
  e7:   db 38                   fstp   TBYTE PTR [eax]
  e9:   dd 65 94                frstor [ebp-0x6c]
  ec:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  f3:   74 02                   je     f7 <_FpuSinh@12+0xf7>
  f5:   dd d8                   fstp   st(0)
  f7:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  fe:   74 05                   je     105 <_FpuSinh@12+0x105>
 100:   dd c7                   ffree  st(7)
 102:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
 105:   0c 01                   or     al,0x1
 107:   c9                      leave
 108:   c2 0c 00                ret    0xc

FpuSin.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuSin@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuSin@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuSin@12+0x1c>
  18:   7a 02                   jp     1c <_FpuSin@12+0x1c>
  1a:   74 6a                   je     86 <_FpuSin@12+0x86>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 08                   je     31 <_FpuSin@12+0x31>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   eb 5b                   jmp    8c <_FpuSin@12+0x8c>
  31:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  34:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
  3b:   74 04                   je     41 <_FpuSin@12+0x41>
  3d:   db 28                   fld    TBYTE PTR [eax]
  3f:   eb 4b                   jmp    8c <_FpuSin@12+0x8c>
  41:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
  48:   74 04                   je     4e <_FpuSin@12+0x4e>
  4a:   dd 00                   fld    QWORD PTR [eax]
  4c:   eb 3e                   jmp    8c <_FpuSin@12+0x8c>
  4e:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
  55:   74 04                   je     5b <_FpuSin@12+0x5b>
  57:   d9 00                   fld    DWORD PTR [eax]
  59:   eb 31                   jmp    8c <_FpuSin@12+0x8c>
  5b:   f7 45 10 04 00 00 00    test   DWORD PTR [ebp+0x10],0x4
```

```
  62:   74 04                   je     68 <_FpuSin@12+0x68>
  64:   db 00                   fild   DWORD PTR [eax]
  66:   eb 24                   jmp    8c <_FpuSin@12+0x8c>
  68:   f7 45 10 00 00 00 01    test   DWORD PTR [ebp+0x10],0x1000000
  6f:   74 04                   je     75 <_FpuSin@12+0x75>
  71:   df 28                   fild   QWORD PTR [eax]
  73:   eb 17                   jmp    8c <_FpuSin@12+0x8c>
  75:   f7 45 10 08 00 00 00    test   DWORD PTR [ebp+0x10],0x8
  7c:   74 05                   je     83 <_FpuSin@12+0x83>
  7e:   db 45 08                fild   DWORD PTR [ebp+0x8]
  81:   eb 09                   jmp    8c <_FpuSin@12+0x8c>
  83:   dd 65 94                frstor [ebp-0x6c]
  86:   33 c0                   xor    eax,eax
  88:   c9                      leave
  89:   c2 0c 00                ret    0xc
  8c:   f7 45 10 20 00 00 00    test   DWORD PTR [ebp+0x10],0x20
  93:   75 0e                   jne    a3 <_FpuSin@12+0xa3>
  95:   d9 eb                   fldpi
  97:   de c9                   fmulp  st(1),st
  99:   68 b4 00 00 00          push   0xb4
  9e:   de 34 24                fidiv  WORD PTR [esp]
  a1:   9b                      fwait
  a2:   58                      pop    eax
  a3:   d9 eb                   fldpi
  a5:   d8 c0                   fadd   st,st(0)
  a7:   d9 c9                   fxch   st(1)
  a9:   d9 f8                   fprem
  ab:   d9 fe                   fsin
  ad:   9b df e0                fstsw  ax
  b0:   9b                      fwait
  b1:   d0 e8                   shr    al,1
  b3:   72 ce                   jb     83 <_FpuSin@12+0x83>
  b5:   9e                      sahf
  b6:   7a f1                   jp     a9 <_FpuSin@12+0xa9>
  b8:   dd d9                   fstp   st(1)
  ba:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  c1:   74 05                   je     c8 <_FpuSin@12+0xc8>
  c3:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
  c6:   eb 1f                   jmp    e7 <_FpuSin@12+0xe7>
  c8:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  cb:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
  d2:   74 04                   je     d8 <_FpuSin@12+0xd8>
  d4:   d9 18                   fstp   DWORD PTR [eax]
  d6:   eb 0f                   jmp    e7 <_FpuSin@12+0xe7>
  d8:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
  df:   74 04                   je     e5 <_FpuSin@12+0xe5>
  e1:   dd 18                   fstp   QWORD PTR [eax]
  e3:   eb 02                   jmp    e7 <_FpuSin@12+0xe7>
  e5:   db 38                   fstp   TBYTE PTR [eax]
  e7:   dd 65 94                frstor [ebp-0x6c]
  ea:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  f1:   74 02                   je     f5 <_FpuSin@12+0xf5>
  f3:   dd d8                   fstp   st(0)
  f5:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  fc:   74 05                   je     103 <_FpuSin@12+0x103>
  fe:   dd c7                   ffree  st(7)
 100:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
 103:   0c 01                   or     al,0x1
 105:   c9                      leave
 106:   c2 0c 00                ret    0xc

FpuRound.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuRound@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
```

```
  6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  d:   74 0d                   je     1c <_FpuRound@12+0x1c>
  f:   d9 e5                   fxam
 11:   9b df e0                fstsw  ax
 14:   9b                      fwait
 15:   9e                      sahf
 16:   73 04                   jae    1c <_FpuRound@12+0x1c>
 18:   7a 02                   jp     1c <_FpuRound@12+0x1c>
 1a:   74 42                   je     5e <_FpuRound@12+0x5e>
 1c:   9b dd 75 94             fsave  [ebp-0x6c]
 20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
 27:   74 08                   je     31 <_FpuRound@12+0x31>
 29:   8d 45 94                lea    eax,[ebp-0x6c]
 2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
 2f:   eb 33                   jmp    64 <_FpuRound@12+0x64>
 31:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
 34:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
 3b:   74 04                   je     41 <_FpuRound@12+0x41>
 3d:   db 28                   fld    TBYTE PTR [eax]
 3f:   eb 23                   jmp    64 <_FpuRound@12+0x64>
 41:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
 48:   74 04                   je     4e <_FpuRound@12+0x4e>
 4a:   dd 00                   fld    QWORD PTR [eax]
 4c:   eb 16                   jmp    64 <_FpuRound@12+0x64>
 4e:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
 55:   74 04                   je     5b <_FpuRound@12+0x5b>
 57:   d9 00                   fld    DWORD PTR [eax]
 59:   eb 09                   jmp    64 <_FpuRound@12+0x64>
 5b:   dd 65 94                frstor [ebp-0x6c]
 5e:   33 c0                   xor    eax,eax
 60:   c9                      leave
 61:   c2 0c 00                ret    0xc
 64:   50                      push   eax
 65:   9b d9 3c 24             fstcw  WORD PTR [esp]
 69:   9b                      fwait
 6a:   66 8b 04 24             mov    ax,WORD PTR [esp]
 6e:   66 25 ff f3             and    ax,0xf3ff
 72:   50                      push   eax
 73:   d9 2c 24                fldcw  WORD PTR [esp]
 76:   d9 fc                   frndint
 78:   58                      pop    eax
 79:   d9 2c 24                fldcw  WORD PTR [esp]
 7c:   9b df e0                fstsw  ax
 7f:   9b                      fwait
 80:   d0 e8                   shr    al,1
 82:   58                      pop    eax
 83:   72 d6                   jb     5b <_FpuRound@12+0x5b>
 85:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
 8c:   74 05                   je     93 <_FpuRound@12+0x93>
 8e:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
 91:   eb 39                   jmp    cc <_FpuRound@12+0xcc>
 93:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
 96:   f7 45 10 40 00 00 00    test   DWORD PTR [ebp+0x10],0x40
 9d:   74 04                   je     a3 <_FpuRound@12+0xa3>
 9f:   db 18                   fistp  DWORD PTR [eax]
 a1:   eb 4b                   jmp    ee <_FpuRound@12+0xee>
 a3:   f7 45 10 00 00 40 00    test   DWORD PTR [ebp+0x10],0x400000
 aa:   74 04                   je     b0 <_FpuRound@12+0xb0>
 ac:   df 38                   fistp  QWORD PTR [eax]
 ae:   eb 3e                   jmp    ee <_FpuRound@12+0xee>
 b0:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
 b7:   74 04                   je     bd <_FpuRound@12+0xbd>
 b9:   d9 18                   fstp   DWORD PTR [eax]
 bb:   eb 0f                   jmp    cc <_FpuRound@12+0xcc>
 bd:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
 c4:   74 04                   je     ca <_FpuRound@12+0xca>
 c6:   dd 18                   fstp   QWORD PTR [eax]
 c8:   eb 02                   jmp    cc <_FpuRound@12+0xcc>
 ca:   db 38                   fstp   TBYTE PTR [eax]
 cc:   dd 65 94                frstor [ebp-0x6c]
```

```
  cf:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  d6:   74 02                   je     da <_FpuRound@12+0xda>
  d8:   dd d8                   fstp   st(0)
  da:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  e1:   74 05                   je     e8 <_FpuRound@12+0xe8>
  e3:   dd c7                   ffree  st(7)
  e5:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
  e8:   0c 01                   or     al,0x1
  ea:   c9                      leave
  eb:   c2 0c 00                ret    0xc
  ee:   9b df e0                fstsw  ax
  f1:   9b                      fwait
  f2:   d0 e8                   shr    al,1
  f4:   0f 82 61 ff ff ff       jb     5b <_FpuRound@12+0x5b>
  fa:   eb d0                   jmp    cc <_FpuRound@12+0xcc>

FpuMul.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuMul@16>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 14 01 01 00 00    test   DWORD PTR [ebp+0x14],0x101
   d:   74 0d                   je     1c <_FpuMul@16+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuMul@16+0x1c>
  18:   7a 02                   jp     1c <_FpuMul@16+0x1c>
  1a:   74 76                   je     92 <_FpuMul@16+0x92>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 14 01 00 00 00    test   DWORD PTR [ebp+0x14],0x1
  27:   74 0b                   je     34 <_FpuMul@16+0x34>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   e9 80 00 00 00          jmp    b4 <_FpuMul@16+0xb4>
  34:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  37:   f7 45 14 10 00 00 00    test   DWORD PTR [ebp+0x14],0x10
  3e:   75 58                   jne    98 <_FpuMul@16+0x98>
  40:   f7 45 14 02 00 00 00    test   DWORD PTR [ebp+0x14],0x2
  47:   74 04                   je     4d <_FpuMul@16+0x4d>
  49:   db 28                   fld    TBYTE PTR [eax]
  4b:   eb 67                   jmp    b4 <_FpuMul@16+0xb4>
  4d:   f7 45 14 00 00 02 00    test   DWORD PTR [ebp+0x14],0x20000
  54:   74 04                   je     5a <_FpuMul@16+0x5a>
  56:   dd 00                   fld    QWORD PTR [eax]
  58:   eb 5a                   jmp    b4 <_FpuMul@16+0xb4>
  5a:   f7 45 14 00 00 01 00    test   DWORD PTR [ebp+0x14],0x10000
  61:   74 04                   je     67 <_FpuMul@16+0x67>
  63:   d9 00                   fld    DWORD PTR [eax]
  65:   eb 4d                   jmp    b4 <_FpuMul@16+0xb4>
  67:   f7 45 14 04 00 00 00    test   DWORD PTR [ebp+0x14],0x4
  6e:   74 04                   je     74 <_FpuMul@16+0x74>
  70:   db 00                   fild   DWORD PTR [eax]
  72:   eb 40                   jmp    b4 <_FpuMul@16+0xb4>
  74:   f7 45 14 00 00 00 01    test   DWORD PTR [ebp+0x14],0x1000000
  7b:   74 04                   je     81 <_FpuMul@16+0x81>
  7d:   df 28                   fild   QWORD PTR [eax]
  7f:   eb 33                   jmp    b4 <_FpuMul@16+0xb4>
  81:   f7 45 14 08 00 00 00    test   DWORD PTR [ebp+0x14],0x8
  88:   74 05                   je     8f <_FpuMul@16+0x8f>
  8a:   db 45 08                fild   DWORD PTR [ebp+0x8]
  8d:   eb 25                   jmp    b4 <_FpuMul@16+0xb4>
  8f:   dd 65 94                frstor [ebp-0x6c]
  92:   33 c0                   xor    eax,eax
  94:   c9                      leave
```

```
 95:   c2 10 00                ret    0x10
 98:   83 f8 01                cmp    eax,0x1
 9b:   75 04                   jne    a1 <_FpuMul@16+0xa1>
 9d:   d9 eb                   fldpi
 9f:   eb 13                   jmp    b4 <_FpuMul@16+0xb4>
 a1:   83 f8 02                cmp    eax,0x2
 a4:   75 e9                   jne    8f <_FpuMul@16+0x8f>
 a6:   d9 e8                   fld1
 a8:   d9 ea                   fldl2e
 aa:   d8 e1                   fsub   st,st(1)
 ac:   d9 f0                   f2xm1
 ae:   d8 c1                   fadd   st,st(1)
 b0:   d9 fd                   fscale
 b2:   dd d9                   fstp   st(1)
 b4:   f7 45 14 00 01 00 00    test   DWORD PTR [ebp+0x14],0x100
 bb:   74 0b                   je     c8 <_FpuMul@16+0xc8>
 bd:   8d 45 94                lea    eax,[ebp-0x6c]
 c0:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
 c3:   e9 80 00 00 00          jmp    148 <_FpuMul@16+0x148>
 c8:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
 cb:   f7 45 14 00 10 00 00    test   DWORD PTR [ebp+0x14],0x1000
 d2:   75 54                   jne    128 <_FpuMul@16+0x128>
 d4:   f7 45 14 00 02 00 00    test   DWORD PTR [ebp+0x14],0x200
 db:   74 04                   je     e1 <_FpuMul@16+0xe1>
 dd:   db 28                   fld    TBYTE PTR [eax]
 df:   eb 67                   jmp    148 <_FpuMul@16+0x148>
 e1:   f7 45 14 00 00 08 00    test   DWORD PTR [ebp+0x14],0x80000
 e8:   74 04                   je     ee <_FpuMul@16+0xee>
 ea:   dd 00                   fld    QWORD PTR [eax]
 ec:   eb 5a                   jmp    148 <_FpuMul@16+0x148>
 ee:   f7 45 14 00 00 04 00    test   DWORD PTR [ebp+0x14],0x40000
 f5:   74 04                   je     fb <_FpuMul@16+0xfb>
 f7:   d9 00                   fld    DWORD PTR [eax]
 f9:   eb 4d                   jmp    148 <_FpuMul@16+0x148>
 fb:   f7 45 14 00 04 00 00    test   DWORD PTR [ebp+0x14],0x400
102:   74 04                   je     108 <_FpuMul@16+0x108>
104:   db 00                   fild   DWORD PTR [eax]
106:   eb 40                   jmp    148 <_FpuMul@16+0x148>
108:   f7 45 14 00 00 00 02    test   DWORD PTR [ebp+0x14],0x2000000
10f:   74 04                   je     115 <_FpuMul@16+0x115>
111:   df 28                   fild   QWORD PTR [eax]
113:   eb 33                   jmp    148 <_FpuMul@16+0x148>
115:   f7 45 14 00 08 00 00    test   DWORD PTR [ebp+0x14],0x800
11c:   74 05                   je     123 <_FpuMul@16+0x123>
11e:   db 45 0c                fild   DWORD PTR [ebp+0xc]
121:   eb 25                   jmp    148 <_FpuMul@16+0x148>
123:   e9 67 ff ff ff          jmp    8f <_FpuMul@16+0x8f>
128:   83 f8 01                cmp    eax,0x1
12b:   75 04                   jne    131 <_FpuMul@16+0x131>
12d:   d9 eb                   fldpi
12f:   eb 17                   jmp    148 <_FpuMul@16+0x148>
131:   83 f8 02                cmp    eax,0x2
134:   0f 85 55 ff ff ff       jne    8f <_FpuMul@16+0x8f>
13a:   d9 e8                   fld1
13c:   d9 ea                   fldl2e
13e:   d8 e1                   fsub   st,st(1)
140:   d9 f0                   f2xm1
142:   d8 c1                   fadd   st,st(1)
144:   d9 fd                   fscale
146:   dd d9                   fstp   st(1)
148:   de c9                   fmulp  st(1),st
14a:   9b df e0                fstsw  ax
14d:   9b                      fwait
14e:   d1 e8                   shr    eax,1
150:   0f 82 39 ff ff ff       jb     8f <_FpuMul@16+0x8f>
156:   f7 45 14 80 00 00 00    test   DWORD PTR [ebp+0x14],0x80
15d:   74 05                   je     164 <_FpuMul@16+0x164>
15f:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
162:   eb 1f                   jmp    183 <_FpuMul@16+0x183>
164:   8b 45 10                mov    eax,DWORD PTR [ebp+0x10]
```

```
 167:   f7 45 14 00 00 10 00    test   DWORD PTR [ebp+0x14],0x100000
 16e:   74 04                   je     174 <_FpuMul@16+0x174>
 170:   d9 18                   fstp   DWORD PTR [eax]
 172:   eb 0f                   jmp    183 <_FpuMul@16+0x183>
 174:   f7 45 14 00 00 20 00    test   DWORD PTR [ebp+0x14],0x200000
 17b:   74 04                   je     181 <_FpuMul@16+0x181>
 17d:   dd 18                   fstp   QWORD PTR [eax]
 17f:   eb 02                   jmp    183 <_FpuMul@16+0x183>
 181:   db 38                   fstp   TBYTE PTR [eax]
 183:   dd 65 94                frstor [ebp-0x6c]
 186:   f7 45 14 01 01 00 00    test   DWORD PTR [ebp+0x14],0x101
 18d:   74 02                   je     191 <_FpuMul@16+0x191>
 18f:   dd d8                   fstp   st(0)
 191:   f7 45 14 80 00 00 00    test   DWORD PTR [ebp+0x14],0x80
 198:   74 05                   je     19f <_FpuMul@16+0x19f>
 19a:   dd c7                   ffree  st(7)
 19c:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
 19f:   0c 01                   or     al,0x1
 1a1:   c9                      leave
 1a2:   c2 10 00                ret    0x10

FpuMod.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuMod@16>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 14 01 01 00 00    test   DWORD PTR [ebp+0x14],0x101
   d:   74 0d                   je     1c <_FpuMod@16+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuMod@16+0x1c>
  18:   7a 02                   jp     1c <_FpuMod@16+0x1c>
  1a:   74 76                   je     92 <_FpuMod@16+0x92>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 14 01 00 00 00    test   DWORD PTR [ebp+0x14],0x1
  27:   74 0b                   je     34 <_FpuMod@16+0x34>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   e9 84 00 00 00          jmp    b8 <_FpuMod@16+0xb8>
  34:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  37:   f7 45 14 10 00 00 00    test   DWORD PTR [ebp+0x14],0x10
  3e:   75 58                   jne    98 <_FpuMod@16+0x98>
  40:   f7 45 14 02 00 00 00    test   DWORD PTR [ebp+0x14],0x2
  47:   74 04                   je     4d <_FpuMod@16+0x4d>
  49:   db 28                   fld    TBYTE PTR [eax]
  4b:   eb 6b                   jmp    b8 <_FpuMod@16+0xb8>
  4d:   f7 45 14 00 00 02 00    test   DWORD PTR [ebp+0x14],0x20000
  54:   74 04                   je     5a <_FpuMod@16+0x5a>
  56:   dd 00                   fld    QWORD PTR [eax]
  58:   eb 5e                   jmp    b8 <_FpuMod@16+0xb8>
  5a:   f7 45 14 00 00 01 00    test   DWORD PTR [ebp+0x14],0x10000
  61:   74 04                   je     67 <_FpuMod@16+0x67>
  63:   d9 00                   fld    DWORD PTR [eax]
  65:   eb 51                   jmp    b8 <_FpuMod@16+0xb8>
  67:   f7 45 14 04 00 00 00    test   DWORD PTR [ebp+0x14],0x4
  6e:   74 04                   je     74 <_FpuMod@16+0x74>
  70:   db 00                   fild   DWORD PTR [eax]
  72:   eb 44                   jmp    b8 <_FpuMod@16+0xb8>
  74:   f7 45 14 00 00 00 01    test   DWORD PTR [ebp+0x14],0x1000000
  7b:   74 04                   je     81 <_FpuMod@16+0x81>
  7d:   df 28                   fild   QWORD PTR [eax]
  7f:   eb 37                   jmp    b8 <_FpuMod@16+0xb8>
  81:   f7 45 14 08 00 00 00    test   DWORD PTR [ebp+0x14],0x8
  88:   74 05                   je     8f <_FpuMod@16+0x8f>
```

```
  8a:   db 45 08                fild   DWORD PTR [ebp+0x8]
  8d:   eb 29                   jmp    b8 <_FpuMod@16+0xb8>
  8f:   dd 65 94                frstor [ebp-0x6c]
  92:   33 c0                   xor    eax,eax
  94:   c9                      leave
  95:   c2 10 00                ret    0x10
  98:   a9 01 00 00 00          test   eax,0x1
  9d:   74 04                   je     a3 <_FpuMod@16+0xa3>
  9f:   d9 eb                   fldpi
  a1:   eb 15                   jmp    b8 <_FpuMod@16+0xb8>
  a3:   a9 02 00 00 00          test   eax,0x2
  a8:   74 e5                   je     8f <_FpuMod@16+0x8f>
  aa:   d9 e8                   fld1
  ac:   d9 ea                   fldl2e
  ae:   d8 e1                   fsub   st,st(1)
  b0:   d9 f0                   f2xm1
  b2:   d8 c1                   fadd   st,st(1)
  b4:   d9 fd                   fscale
  b6:   dd d9                   fstp   st(1)
  b8:   f7 45 14 00 01 00 00    test   DWORD PTR [ebp+0x14],0x100
  bf:   74 0b                   je     cc <_FpuMod@16+0xcc>
  c1:   8d 45 94                lea    eax,[ebp-0x6c]
  c4:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  c7:   e9 80 00 00 00          jmp    14c <_FpuMod@16+0x14c>
  cc:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  cf:   f7 45 14 00 10 00 00    test   DWORD PTR [ebp+0x14],0x1000
  d6:   75 54                   jne    12c <_FpuMod@16+0x12c>
  d8:   f7 45 14 00 02 00 00    test   DWORD PTR [ebp+0x14],0x200
  df:   74 04                   je     e5 <_FpuMod@16+0xe5>
  e1:   db 28                   fld    TBYTE PTR [eax]
  e3:   eb 67                   jmp    14c <_FpuMod@16+0x14c>
  e5:   f7 45 14 00 00 08 00    test   DWORD PTR [ebp+0x14],0x80000
  ec:   74 04                   je     f2 <_FpuMod@16+0xf2>
  ee:   dd 00                   fld    QWORD PTR [eax]
  f0:   eb 5a                   jmp    14c <_FpuMod@16+0x14c>
  f2:   f7 45 14 00 00 04 00    test   DWORD PTR [ebp+0x14],0x40000
  f9:   74 04                   je     ff <_FpuMod@16+0xff>
  fb:   d9 00                   fld    DWORD PTR [eax]
  fd:   eb 4d                   jmp    14c <_FpuMod@16+0x14c>
  ff:   f7 45 14 00 04 00 00    test   DWORD PTR [ebp+0x14],0x400
 106:   74 04                   je     10c <_FpuMod@16+0x10c>
 108:   db 00                   fild   DWORD PTR [eax]
 10a:   eb 40                   jmp    14c <_FpuMod@16+0x14c>
 10c:   f7 45 14 00 00 00 02    test   DWORD PTR [ebp+0x14],0x2000000
 113:   74 04                   je     119 <_FpuMod@16+0x119>
 115:   df 28                   fild   QWORD PTR [eax]
 117:   eb 33                   jmp    14c <_FpuMod@16+0x14c>
 119:   f7 45 14 00 08 00 00    test   DWORD PTR [ebp+0x14],0x800
 120:   74 05                   je     127 <_FpuMod@16+0x127>
 122:   db 45 0c                fild   DWORD PTR [ebp+0xc]
 125:   eb 25                   jmp    14c <_FpuMod@16+0x14c>
 127:   e9 63 ff ff ff          jmp    8f <_FpuMod@16+0x8f>
 12c:   83 f8 01                cmp    eax,0x1
 12f:   75 04                   jne    135 <_FpuMod@16+0x135>
 131:   d9 eb                   fldpi
 133:   eb 17                   jmp    14c <_FpuMod@16+0x14c>
 135:   83 f8 02                cmp    eax,0x2
 138:   0f 85 51 ff ff ff       jne    8f <_FpuMod@16+0x8f>
 13e:   d9 e8                   fld1
 140:   d9 ea                   fldl2e
 142:   d8 e1                   fsub   st,st(1)
 144:   d9 f0                   f2xm1
 146:   d8 c1                   fadd   st,st(1)
 148:   d9 fd                   fscale
 14a:   dd d9                   fstp   st(1)
 14c:   d9 c9                   fxch   st(1)
 14e:   d9 f8                   fprem
 150:   9b df e0                fstsw  ax
 153:   9b                      fwait
 154:   d0 e8                   shr    al,1
```

```
 156:   0f 82 33 ff ff ff       jb     8f <_FpuMod@16+0x8f>
 15c:   9e                      sahf
 15d:   7a ef                   jp     14e <_FpuMod@16+0x14e>
 15f:   f7 45 14 80 00 00 00    test   DWORD PTR [ebp+0x14],0x80
 166:   74 05                   je     16d <_FpuMod@16+0x16d>
 168:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
 16b:   eb 1f                   jmp    18c <_FpuMod@16+0x18c>
 16d:   8b 45 10                mov    eax,DWORD PTR [ebp+0x10]
 170:   f7 45 14 00 00 10 00    test   DWORD PTR [ebp+0x14],0x100000
 177:   74 04                   je     17d <_FpuMod@16+0x17d>
 179:   d9 18                   fstp   DWORD PTR [eax]
 17b:   eb 0f                   jmp    18c <_FpuMod@16+0x18c>
 17d:   f7 45 14 00 00 20 00    test   DWORD PTR [ebp+0x14],0x200000
 184:   74 04                   je     18a <_FpuMod@16+0x18a>
 186:   dd 18                   fstp   QWORD PTR [eax]
 188:   eb 02                   jmp    18c <_FpuMod@16+0x18c>
 18a:   db 38                   fstp   TBYTE PTR [eax]
 18c:   dd 65 94                frstor [ebp-0x6c]
 18f:   f7 45 14 01 01 00 00    test   DWORD PTR [ebp+0x14],0x101
 196:   74 02                   je     19a <_FpuMod@16+0x19a>
 198:   dd d8                   fstp   st(0)
 19a:   f7 45 14 80 00 00 00    test   DWORD PTR [ebp+0x14],0x80
 1a1:   74 05                   je     1a8 <_FpuMod@16+0x1a8>
 1a3:   dd c7                   ffree  st(7)
 1a5:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
 1a8:   0c 01                   or     al,0x1
 1aa:   c9                      leave
 1ab:   c2 10 00                ret    0x10

FpuLogx.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuLogx@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuLogx@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuLogx@12+0x1c>
  18:   7a 02                   jp     1c <_FpuLogx@12+0x1c>
  1a:   74 76                   je     92 <_FpuLogx@12+0x92>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 0b                   je     34 <_FpuLogx@12+0x34>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   e9 80 00 00 00          jmp    b4 <_FpuLogx@12+0xb4>
  34:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  37:   f7 45 10 10 00 00 00    test   DWORD PTR [ebp+0x10],0x10
  3e:   75 58                   jne    98 <_FpuLogx@12+0x98>
  40:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
  47:   74 04                   je     4d <_FpuLogx@12+0x4d>
  49:   db 28                   fld    TBYTE PTR [eax]
  4b:   eb 67                   jmp    b4 <_FpuLogx@12+0xb4>
  4d:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
  54:   74 04                   je     5a <_FpuLogx@12+0x5a>
  56:   dd 00                   fld    QWORD PTR [eax]
  58:   eb 5a                   jmp    b4 <_FpuLogx@12+0xb4>
  5a:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
  61:   74 04                   je     67 <_FpuLogx@12+0x67>
  63:   d9 00                   fld    DWORD PTR [eax]
  65:   eb 4d                   jmp    b4 <_FpuLogx@12+0xb4>
  67:   f7 45 10 04 00 00 00    test   DWORD PTR [ebp+0x10],0x4
  6e:   74 04                   je     74 <_FpuLogx@12+0x74>
```

```
  70:   db 00                   fild   DWORD PTR [eax]
  72:   eb 40                   jmp    b4 <_FpuLogx@12+0xb4>
  74:   f7 45 10 00 00 00 01    test   DWORD PTR [ebp+0x10],0x1000000
  7b:   74 04                   je     81 <_FpuLogx@12+0x81>
  7d:   df 28                   fild   QWORD PTR [eax]
  7f:   eb 33                   jmp    b4 <_FpuLogx@12+0xb4>
  81:   f7 45 10 08 00 00 00    test   DWORD PTR [ebp+0x10],0x8
  88:   74 05                   je     8f <_FpuLogx@12+0x8f>
  8a:   db 45 08                fild   DWORD PTR [ebp+0x8]
  8d:   eb 25                   jmp    b4 <_FpuLogx@12+0xb4>
  8f:   dd 65 94                frstor [ebp-0x6c]
  92:   33 c0                   xor    eax,eax
  94:   c9                      leave
  95:   c2 0c 00                ret    0xc
  98:   83 f8 01                cmp    eax,0x1
  9b:   74 04                   je     a1 <_FpuLogx@12+0xa1>
  9d:   d9 eb                   fldpi
  9f:   eb 13                   jmp    b4 <_FpuLogx@12+0xb4>
  a1:   83 f8 02                cmp    eax,0x2
  a4:   74 e9                   je     8f <_FpuLogx@12+0x8f>
  a6:   d9 e8                   fld1
  a8:   d9 ea                   fldl2e
  aa:   d8 e1                   fsub   st,st(1)
  ac:   d9 f0                   f2xm1
  ae:   d8 c1                   fadd   st,st(1)
  b0:   d9 fd                   fscale
  b2:   dd d9                   fstp   st(1)
  b4:   d9 ec                   fldlg2
  b6:   d9 c9                   fxch   st(1)
  b8:   d9 f1                   fyl2x
  ba:   9b df e0                fstsw  ax
  bd:   9b                      fwait
  be:   d0 e8                   shr    al,1
  c0:   72 cd                   jb     8f <_FpuLogx@12+0x8f>
  c2:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  c9:   74 05                   je     d0 <_FpuLogx@12+0xd0>
  cb:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
  ce:   eb 1f                   jmp    ef <_FpuLogx@12+0xef>
  d0:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  d3:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
  da:   74 04                   je     e0 <_FpuLogx@12+0xe0>
  dc:   d9 18                   fstp   DWORD PTR [eax]
  de:   eb 0f                   jmp    ef <_FpuLogx@12+0xef>
  e0:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
  e7:   74 04                   je     ed <_FpuLogx@12+0xed>
  e9:   dd 18                   fstp   QWORD PTR [eax]
  eb:   eb 02                   jmp    ef <_FpuLogx@12+0xef>
  ed:   db 38                   fstp   TBYTE PTR [eax]
  ef:   dd 65 94                frstor [ebp-0x6c]
  f2:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  f9:   74 02                   je     fd <_FpuLogx@12+0xfd>
  fb:   dd d8                   fstp   st(0)
  fd:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
 104:   74 05                   je     10b <_FpuLogx@12+0x10b>
 106:   dd c7                   ffree  st(7)
 108:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
 10b:   0c 01                   or     al,0x1
 10d:   c9                      leave
 10e:   c2 0c 00                ret    0xc

FpuLnx.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuLnx@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
```

```
 d:   74 0d                   je     1c <_FpuLnx@12+0x1c>
 f:   d9 e5                   fxam
11:   9b df e0                fstsw  ax
14:   9b                      fwait
15:   9e                      sahf
16:   73 04                   jae    1c <_FpuLnx@12+0x1c>
18:   7a 02                   jp     1c <_FpuLnx@12+0x1c>
1a:   74 76                   je     92 <_FpuLnx@12+0x92>
1c:   9b dd 75 94             fsave  [ebp-0x6c]
20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
27:   74 0b                   je     34 <_FpuLnx@12+0x34>
29:   8d 45 94                lea    eax,[ebp-0x6c]
2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
2f:   e9 80 00 00 00          jmp    b4 <_FpuLnx@12+0xb4>
34:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
37:   f7 45 10 10 00 00 00    test   DWORD PTR [ebp+0x10],0x10
3e:   75 58                   jne    98 <_FpuLnx@12+0x98>
40:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
47:   74 04                   je     4d <_FpuLnx@12+0x4d>
49:   db 28                   fld    TBYTE PTR [eax]
4b:   eb 67                   jmp    b4 <_FpuLnx@12+0xb4>
4d:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
54:   74 04                   je     5a <_FpuLnx@12+0x5a>
56:   dd 00                   fld    QWORD PTR [eax]
58:   eb 5a                   jmp    b4 <_FpuLnx@12+0xb4>
5a:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
61:   74 04                   je     67 <_FpuLnx@12+0x67>
63:   d9 00                   fld    DWORD PTR [eax]
65:   eb 4d                   jmp    b4 <_FpuLnx@12+0xb4>
67:   f7 45 10 04 00 00 00    test   DWORD PTR [ebp+0x10],0x4
6e:   74 04                   je     74 <_FpuLnx@12+0x74>
70:   db 00                   fild   DWORD PTR [eax]
72:   eb 40                   jmp    b4 <_FpuLnx@12+0xb4>
74:   f7 45 10 00 00 00 01    test   DWORD PTR [ebp+0x10],0x1000000
7b:   74 04                   je     81 <_FpuLnx@12+0x81>
7d:   df 28                   fild   QWORD PTR [eax]
7f:   eb 33                   jmp    b4 <_FpuLnx@12+0xb4>
81:   f7 45 10 08 00 00 00    test   DWORD PTR [ebp+0x10],0x8
88:   74 05                   je     8f <_FpuLnx@12+0x8f>
8a:   db 45 08                fild   DWORD PTR [ebp+0x8]
8d:   eb 25                   jmp    b4 <_FpuLnx@12+0xb4>
8f:   dd 65 94                frstor [ebp-0x6c]
92:   33 c0                   xor    eax,eax
94:   c9                      leave
95:   c2 0c 00                ret    0xc
98:   83 f8 01                cmp    eax,0x1
9b:   74 04                   je     a1 <_FpuLnx@12+0xa1>
9d:   d9 eb                   fldpi
9f:   eb 13                   jmp    b4 <_FpuLnx@12+0xb4>
a1:   83 f8 02                cmp    eax,0x2
a4:   74 e9                   je     8f <_FpuLnx@12+0x8f>
a6:   d9 e8                   fld1
a8:   d9 ea                   fldl2e
aa:   d8 e1                   fsub   st,st(1)
ac:   d9 f0                   f2xm1
ae:   d8 c1                   fadd   st,st(1)
b0:   d9 fd                   fscale
b2:   dd d9                   fstp   st(1)
b4:   d9 ed                   fldln2
b6:   d9 c9                   fxch   st(1)
b8:   d9 f1                   fyl2x
ba:   9b df e0                fstsw  ax
bd:   9b                      fwait
be:   d0 e8                   shr    al,1
c0:   72 cd                   jb     8f <_FpuLnx@12+0x8f>
c2:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
c9:   74 05                   je     d0 <_FpuLnx@12+0xd0>
cb:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
ce:   eb 1f                   jmp    ef <_FpuLnx@12+0xef>
d0:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
```

```
  d3:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
  da:   74 04                   je     e0 <_FpuLnx@12+0xe0>
  dc:   d9 18                   fstp   DWORD PTR [eax]
  de:   eb 0f                   jmp    ef <_FpuLnx@12+0xef>
  e0:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
  e7:   74 04                   je     ed <_FpuLnx@12+0xed>
  e9:   dd 18                   fstp   QWORD PTR [eax]
  eb:   eb 02                   jmp    ef <_FpuLnx@12+0xef>
  ed:   db 38                   fstp   TBYTE PTR [eax]
  ef:   dd 65 94                frstor [ebp-0x6c]
  f2:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  f9:   74 02                   je     fd <_FpuLnx@12+0xfd>
  fb:   dd d8                   fstp   st(0)
  fd:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
 104:   74 05                   je     10b <_FpuLnx@12+0x10b>
 106:   dd c7                   ffree  st(7)
 108:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
 10b:   0c 01                   or     al,0x1
 10d:   c9                      leave
 10e:   c2 0c 00                ret    0xc

FpuFLtoA.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuFLtoA@16>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   81 c4 54 ff ff ff       add    esp,0xffffff54
   9:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
   c:   f7 45 14 00 04 00 00    test   DWORD PTR [ebp+0x14],0x400
  13:   74 02                   je     17 <_FpuFLtoA@16+0x17>
  15:   8b 00                   mov    eax,DWORD PTR [eax]
  17:   50                      push   eax
  18:   0f b6 c0                movzx  eax,al
  1b:   83 f8 0f                cmp    eax,0xf
  1e:   76 05                   jbe    25 <_FpuFLtoA@16+0x25>
  20:   b8 0f 00 00 00          mov    eax,0xf
  25:   89 45 f0                mov    DWORD PTR [ebp-0x10],eax
  28:   58                      pop    eax
  29:   0f b6 c4                movzx  eax,ah
  2c:   83 f8 11                cmp    eax,0x11
  2f:   76 05                   jbe    36 <_FpuFLtoA@16+0x36>
  31:   b8 11 00 00 00          mov    eax,0x11
  36:   89 45 f4                mov    DWORD PTR [ebp-0xc],eax
  39:   f7 45 14 01 00 00 00    test   DWORD PTR [ebp+0x14],0x1
  40:   74 0d                   je     4f <_FpuFLtoA@16+0x4f>
  42:   d9 e5                   fxam
  44:   9b df e0                fstsw  ax
  47:   9b                      fwait
  48:   9e                      sahf
  49:   73 04                   jae    4f <_FpuFLtoA@16+0x4f>
  4b:   7a 02                   jp     4f <_FpuFLtoA@16+0x4f>
  4d:   74 42                   je     91 <_FpuFLtoA@16+0x91>
  4f:   9b dd 75 80             fsave  [ebp-0x80]
  53:   f7 45 14 01 00 00 00    test   DWORD PTR [ebp+0x14],0x1
  5a:   74 08                   je     64 <_FpuFLtoA@16+0x64>
  5c:   8d 45 80                lea    eax,[ebp-0x80]
  5f:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  62:   eb 44                   jmp    a8 <_FpuFLtoA@16+0xa8>
  64:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  67:   f7 45 14 02 00 00 00    test   DWORD PTR [ebp+0x14],0x2
  6e:   74 04                   je     74 <_FpuFLtoA@16+0x74>
  70:   db 28                   fld    TBYTE PTR [eax]
  72:   eb 34                   jmp    a8 <_FpuFLtoA@16+0xa8>
  74:   f7 45 14 00 00 02 00    test   DWORD PTR [ebp+0x14],0x20000
  7b:   74 04                   je     81 <_FpuFLtoA@16+0x81>
  7d:   dd 00                   fld    QWORD PTR [eax]
  7f:   eb 27                   jmp    a8 <_FpuFLtoA@16+0xa8>
```

```
 81:   f7 45 14 00 00 01 00    test   DWORD PTR [ebp+0x14],0x10000
 88:   74 04                   je     8e <_FpuFLtoA@16+0x8e>
 8a:   d9 00                   fld    DWORD PTR [eax]
 8c:   eb 1a                   jmp    a8 <_FpuFLtoA@16+0xa8>
 8e:   dd 65 80                frstor [ebp-0x80]
 91:   57                      push   edi
 92:   8b 7d 10                mov    edi,DWORD PTR [ebp+0x10]
 95:   b8 45 52 52 4f          mov    eax,0x4f525245
 9a:   ab                      stos   DWORD PTR es:[edi],eax
 9b:   66 b8 52 00             mov    ax,0x52
 9f:   66 ab                   stos   WORD PTR es:[edi],ax
 a1:   5f                      pop    edi
 a2:   33 c0                   xor    eax,eax
 a4:   c9                      leave
 a5:   c2 10 00                ret    0x10
 a8:   d9 e5                   fxam
 aa:   9b df e0                fstsw  ax
 ad:   9b                      fwait
 ae:   9e                      sahf
 af:   74 25                   je     d6 <_FpuFLtoA@16+0xd6>
 b1:   7b db                   jnp    8e <_FpuFLtoA@16+0x8e>
 b3:   73 4b                   jae    100 <_FpuFLtoA@16+0x100>
 b5:   51                      push   ecx
 b6:   56                      push   esi
 b7:   57                      push   edi
 b8:   8b 7d 10                mov    edi,DWORD PTR [ebp+0x10]
 bb:   b0 2b                   mov    al,0x2b
 bd:   f6 c4 02                test   ah,0x2
 c0:   74 02                   je     c4 <_FpuFLtoA@16+0xc4>
 c2:   b0 2d                   mov    al,0x2d
 c4:   aa                      stos   BYTE PTR es:[edi],al
 c5:   b8 49 4e 46 49          mov    eax,0x49464e49
 ca:   ab                      stos   DWORD PTR es:[edi],eax
 cb:   b8 4e 49 54 59          mov    eax,0x5954494e
 d0:   ab                      stos   DWORD PTR es:[edi],eax
 d1:   e9 0d 02 00 00          jmp    2e3 <_FpuFLtoA@16+0x2e3>
 d6:   7a 28                   jp     100 <_FpuFLtoA@16+0x100>
 d8:   dd d8                   fstp   st(0)
 da:   51                      push   ecx
 db:   56                      push   esi
 dc:   57                      push   edi
 dd:   8b 7d 10                mov    edi,DWORD PTR [ebp+0x10]
 e0:   f7 45 14 00 80 00 00    test   DWORD PTR [ebp+0x14],0x8000
 e7:   75 0c                   jne    f5 <_FpuFLtoA@16+0xf5>
 e9:   8b 4d f4                mov    ecx,DWORD PTR [ebp-0xc]
 ec:   83 e9 02                sub    ecx,0x2
 ef:   7e 04                   jle    f5 <_FpuFLtoA@16+0xf5>
 f1:   b0 20                   mov    al,0x20
 f3:   f3 aa                   rep stos BYTE PTR es:[edi],al
 f5:   66 b8 20 30             mov    ax,0x3020
 f9:   66 ab                   stos   WORD PTR es:[edi],ax
 fb:   e9 e3 01 00 00          jmp    2e3 <_FpuFLtoA@16+0x2e3>
100:   d9 ec                   fldlg2
102:   d9 c1                   fld    st(1)
104:   d9 e1                   fabs
106:   d9 f1                   fyl2x
108:   9b d9 bd 6a ff ff ff    fstcw  WORD PTR [ebp-0x96]
10f:   9b                      fwait
110:   66 8b 85 6a ff ff ff    mov    ax,WORD PTR [ebp-0x96]
117:   66 0d 00 0c             or     ax,0xc00
11b:   66 89 85 68 ff ff ff    mov    WORD PTR [ebp-0x98],ax
122:   d9 ad 68 ff ff ff       fldcw  WORD PTR [ebp-0x98]
128:   db 55 f8                fist   DWORD PTR [ebp-0x8]
12b:   d9 ad 6a ff ff ff       fldcw  WORD PTR [ebp-0x96]
131:   d9 e4                   ftst
133:   9b df e0                fstsw  ax
136:   9b                      fwait
137:   9e                      sahf
138:   83 5d f8 00             sbb    DWORD PTR [ebp-0x8],0x0
13c:   dd d8                   fstp   st(0)
```

```
13e:   8b 45 14                mov    eax,DWORD PTR [ebp+0x14]
141:   25 00 80 00 00          and    eax,0x8000
146:   c7 45 ec 00 00 00 00    mov    DWORD PTR [ebp-0x14],0x0
14d:   0b c0                   or     eax,eax
14f:   75 32                   jne    183 <_FpuFLtoA@16+0x183>
151:   8b 45 f8                mov    eax,DWORD PTR [ebp-0x8]
154:   0b c0                   or     eax,eax
156:   78 23                   js     17b <_FpuFLtoA@16+0x17b>
158:   83 f8 0f                cmp    eax,0xf
15b:   76 10                   jbe    16d <_FpuFLtoA@16+0x16d>
15d:   81 4d 14 00 80 00 00    or     DWORD PTR [ebp+0x14],0x8000
164:   c7 45 f0 0f 00 00 00    mov    DWORD PTR [ebp-0x10],0xf
16b:   eb 16                   jmp    183 <_FpuFLtoA@16+0x183>
16d:   03 45 f0                add    eax,DWORD PTR [ebp-0x10]
170:   83 f8 0f                cmp    eax,0xf
173:   76 06                   jbe    17b <_FpuFLtoA@16+0x17b>
175:   83 e8 0f                sub    eax,0xf
178:   29 45 f0                sub    DWORD PTR [ebp-0x10],eax
17b:   ff 75 f0                push   DWORD PTR [ebp-0x10]
17e:   8f 45 fc                pop    DWORD PTR [ebp-0x4]
181:   eb 1b                   jmp    19e <_FpuFLtoA@16+0x19e>
183:   8b 45 f0                mov    eax,DWORD PTR [ebp-0x10]
186:   2b 45 f8                sub    eax,DWORD PTR [ebp-0x8]
189:   3d 43 13 00 00          cmp    eax,0x1343
18e:   7e 0b                   jle    19b <_FpuFLtoA@16+0x19b>
190:   b9 43 13 00 00          mov    ecx,0x1343
195:   2b c1                   sub    eax,ecx
197:   91                      xchg   ecx,eax
198:   89 4d ec                mov    DWORD PTR [ebp-0x14],ecx
19b:   89 45 fc                mov    DWORD PTR [ebp-0x4],eax
19e:   83 7d fc 00             cmp    DWORD PTR [ebp-0x4],0x0
1a2:   74 3c                   je     1e0 <_FpuFLtoA@16+0x1e0>
1a4:   db 45 fc                fild   DWORD PTR [ebp-0x4]
1a7:   d9 e9                   fldl2t
1a9:   de c9                   fmulp  st(1),st
1ab:   d9 c0                   fld    st(0)
1ad:   d9 fc                   frndint
1af:   d9 c9                   fxch   st(1)
1b1:   d8 e1                   fsub   st,st(1)
1b3:   d9 f0                   f2xm1
1b5:   d9 e8                   fld1
1b7:   de c1                   faddp  st(1),st
1b9:   d9 fd                   fscale
1bb:   dd d9                   fstp   st(1)
1bd:   de c9                   fmulp  st(1),st
1bf:   83 7d ec 00             cmp    DWORD PTR [ebp-0x14],0x0
1c3:   74 1b                   je     1e0 <_FpuFLtoA@16+0x1e0>
1c5:   db 45 ec                fild   DWORD PTR [ebp-0x14]
1c8:   d9 e9                   fldl2t
1ca:   de c9                   fmulp  st(1),st
1cc:   d9 c0                   fld    st(0)
1ce:   d9 fc                   frndint
1d0:   d9 c9                   fxch   st(1)
1d2:   d8 e1                   fsub   st,st(1)
1d4:   d9 f0                   f2xm1
1d6:   d9 e8                   fld1
1d8:   de c1                   faddp  st(1),st
1da:   d9 fd                   fscale
1dc:   dd d9                   fstp   st(1)
1de:   de c9                   fmulp  st(1),st
1e0:   df b5 6c ff ff ff       fbstp  TBYTE PTR [ebp-0x94]
1e6:   9b df e0                fstsw  ax
1e9:   9b                      fwait
1ea:   d1 e8                   shr    eax,1
1ec:   0f 82 9c fe ff ff       jb     8e <_FpuFLtoA@16+0x8e>
1f2:   51                      push   ecx
1f3:   56                      push   esi
1f4:   57                      push   edi
1f5:   8d b5 75 ff ff ff       lea    esi,[ebp-0x8b]
1fb:   8d bd 54 ff ff ff       lea    edi,[ebp-0xac]
```

```
201:   b8 20 30 00 00          mov    eax,0x3020
206:   8a 0e                   mov    cl,BYTE PTR [esi]
208:   80 f9 80                cmp    cl,0x80
20b:   75 02                   jne    20f <_FpuFLtoA@16+0x20f>
20d:   b0 2d                   mov    al,0x2d
20f:   66 ab                   stos   WORD PTR es:[edi],ax
211:   b9 09 00 00 00          mov    ecx,0x9
216:   4e                      dec    esi
217:   0f b6 06                movzx  eax,BYTE PTR [esi]
21a:   66 c1 c8 04             ror    ax,0x4
21e:   c0 cc 04                ror    ah,0x4
221:   66 05 30 30             add    ax,0x3030
225:   66 ab                   stos   WORD PTR es:[edi],ax
227:   49                      dec    ecx
228:   75 ec                   jne    216 <_FpuFLtoA@16+0x216>
22a:   8b 7d 10                mov    edi,DWORD PTR [ebp+0x10]
22d:   8d b5 54 ff ff ff       lea    esi,[ebp-0xac]
233:   f7 45 14 00 80 00 00    test   DWORD PTR [ebp+0x14],0x8000
23a:   75 55                   jne    291 <_FpuFLtoA@16+0x291>
23c:   8b 4d f4                mov    ecx,DWORD PTR [ebp-0xc]
23f:   0b c9                   or     ecx,ecx
241:   74 16                   je     259 <_FpuFLtoA@16+0x259>
243:   ba 02 00 00 00          mov    edx,0x2
248:   8b 45 f8                mov    eax,DWORD PTR [ebp-0x8]
24b:   0b c0                   or     eax,eax
24d:   78 02                   js     251 <_FpuFLtoA@16+0x251>
24f:   03 d0                   add    edx,eax
251:   2b ca                   sub    ecx,edx
253:   7e 04                   jle    259 <_FpuFLtoA@16+0x259>
255:   b0 20                   mov    al,0x20
257:   f3 aa                   rep stos BYTE PTR es:[edi],al
259:   9c                      pushf
25a:   a4                      movs   BYTE PTR es:[edi],BYTE PTR ds:[esi]
25b:   b9 01 00 00 00          mov    ecx,0x1
260:   8b 45 f8                mov    eax,DWORD PTR [ebp-0x8]
263:   0b c0                   or     eax,eax
265:   78 02                   js     269 <_FpuFLtoA@16+0x269>
267:   03 c8                   add    ecx,eax
269:   8b 45 f0                mov    eax,DWORD PTR [ebp-0x10]
26c:   03 c1                   add    eax,ecx
26e:   83 e8 13                sub    eax,0x13
271:   2b f0                   sub    esi,eax
273:   58                      pop    eax
274:   80 7e ff 31             cmp    BYTE PTR [esi-0x1],0x31
278:   75 07                   jne    281 <_FpuFLtoA@16+0x281>
27a:   4e                      dec    esi
27b:   41                      inc    ecx
27c:   50                      push   eax
27d:   9d                      popf
27e:   7e 01                   jle    281 <_FpuFLtoA@16+0x281>
280:   4f                      dec    edi
281:   f3 a4                   rep movs BYTE PTR es:[edi],BYTE PTR ds:[esi]
283:   8b 4d f0                mov    ecx,DWORD PTR [ebp-0x10]
286:   0b c9                   or     ecx,ecx
288:   74 05                   je     28f <_FpuFLtoA@16+0x28f>
28a:   b0 2e                   mov    al,0x2e
28c:   aa                      stos   BYTE PTR es:[edi],al
28d:   f3 a4                   rep movs BYTE PTR es:[edi],BYTE PTR ds:[esi]
28f:   eb 52                   jmp    2e3 <_FpuFLtoA@16+0x2e3>
291:   a4                      movs   BYTE PTR es:[edi],BYTE PTR ds:[esi]
292:   8b 4d f0                mov    ecx,DWORD PTR [ebp-0x10]
295:   b8 12 00 00 00          mov    eax,0x12
29a:   2b c1                   sub    eax,ecx
29c:   03 f0                   add    esi,eax
29e:   80 7e ff 31             cmp    BYTE PTR [esi-0x1],0x31
2a2:   9c                      pushf
2a3:   75 01                   jne    2a6 <_FpuFLtoA@16+0x2a6>
2a5:   4e                      dec    esi
2a6:   a4                      movs   BYTE PTR es:[edi],BYTE PTR ds:[esi]
2a7:   b0 2e                   mov    al,0x2e
```

```
 2a9:   aa                      stos   BYTE PTR es:[edi],al
 2aa:   f3 a4                   rep movs BYTE PTR es:[edi],BYTE PTR ds:[esi]
 2ac:   b0 45                   mov    al,0x45
 2ae:   aa                      stos   BYTE PTR es:[edi],al
 2af:   b0 2b                   mov    al,0x2b
 2b1:   8b 4d f8                mov    ecx,DWORD PTR [ebp-0x8]
 2b4:   9d                      popf
 2b5:   75 01                   jne    2b8 <_FpuFLtoA@16+0x2b8>
 2b7:   41                      inc    ecx
 2b8:   0b c9                   or     ecx,ecx
 2ba:   79 04                   jns    2c0 <_FpuFLtoA@16+0x2c0>
 2bc:   b0 2d                   mov    al,0x2d
 2be:   f7 d9                   neg    ecx
 2c0:   aa                      stos   BYTE PTR es:[edi],al
 2c1:   8b c1                   mov    eax,ecx
 2c3:   b1 64                   mov    cl,0x64
 2c5:   f6 f1                   div    cl
 2c7:   50                      push   eax
 2c8:   25 ff 00 00 00          and    eax,0xff
 2cd:   b1 0a                   mov    cl,0xa
 2cf:   f6 f1                   div    cl
 2d1:   66 05 30 30             add    ax,0x3030
 2d5:   66 ab                   stos   WORD PTR es:[edi],ax
 2d7:   58                      pop    eax
 2d8:   c1 e8 08                shr    eax,0x8
 2db:   f6 f1                   div    cl
 2dd:   66 05 30 30             add    ax,0x3030
 2e1:   66 ab                   stos   WORD PTR es:[edi],ax
 2e3:   33 c0                   xor    eax,eax
 2e5:   aa                      stos   BYTE PTR es:[edi],al
 2e6:   5f                      pop    edi
 2e7:   5e                      pop    esi
 2e8:   59                      pop    ecx
 2e9:   dd 65 80                frstor [ebp-0x80]
 2ec:   0c 01                   or     al,0x1
 2ee:   c9                      leave
 2ef:   c2 10 00                ret    0x10

FpuExam.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuExam@8>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 94                add    esp,0xffffff94
   6:   52                      push   edx
   7:   f7 45 0c 01 00 00 00    test   DWORD PTR [ebp+0xc],0x1
   e:   74 0d                   je     1d <_FpuExam@8+0x1d>
  10:   d9 e5                   fxam
  12:   9b df e0                fstsw  ax
  15:   9b                      fwait
  16:   9e                      sahf
  17:   73 04                   jae    1d <_FpuExam@8+0x1d>
  19:   7a 02                   jp     1d <_FpuExam@8+0x1d>
  1b:   74 42                   je     5f <_FpuExam@8+0x5f>
  1d:   9b dd 75 94             fsave  [ebp-0x6c]
  21:   f7 45 0c 01 00 00 00    test   DWORD PTR [ebp+0xc],0x1
  28:   74 08                   je     32 <_FpuExam@8+0x32>
  2a:   8d 45 94                lea    eax,[ebp-0x6c]
  2d:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  30:   eb 34                   jmp    66 <_FpuExam@8+0x66>
  32:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  35:   f7 45 0c 02 00 00 00    test   DWORD PTR [ebp+0xc],0x2
  3c:   74 04                   je     42 <_FpuExam@8+0x42>
  3e:   db 28                   fld    TBYTE PTR [eax]
  40:   eb 24                   jmp    66 <_FpuExam@8+0x66>
  42:   f7 45 0c 00 00 02 00    test   DWORD PTR [ebp+0xc],0x20000
  49:   74 04                   je     4f <_FpuExam@8+0x4f>
```

```
  4b:   dd 00                   fld    QWORD PTR [eax]
  4d:   eb 17                   jmp    66 <_FpuExam@8+0x66>
  4f:   f7 45 0c 00 00 01 00    test   DWORD PTR [ebp+0xc],0x10000
  56:   74 04                   je     5c <_FpuExam@8+0x5c>
  58:   d9 00                   fld    DWORD PTR [eax]
  5a:   eb 0a                   jmp    66 <_FpuExam@8+0x66>
  5c:   dd 65 94                frstor [ebp-0x6c]
  5f:   33 c0                   xor    eax,eax
  61:   5a                      pop    edx
  62:   c9                      leave
  63:   c2 08 00                ret    0x8
  66:   d9 e4                   ftst
  68:   9b df e0                fstsw  ax
  6b:   9b                      fwait
  6c:   d0 e8                   shr    al,1
  6e:   72 ec                   jb     5c <_FpuExam@8+0x5c>
  70:   33 d2                   xor    edx,edx
  72:   9e                      sahf
  73:   75 07                   jne    7c <_FpuExam@8+0x7c>
  75:   72 28                   jb     9f <_FpuExam@8+0x9f>
  77:   83 ca 0a                or     edx,0xa
  7a:   eb 17                   jmp    93 <_FpuExam@8+0x93>
  7c:   73 03                   jae    81 <_FpuExam@8+0x81>
  7e:   83 ca 04                or     edx,0x4
  81:   d9 e1                   fabs
  83:   d9 e8                   fld1
  85:   de d9                   fcompp
  87:   9b df e0                fstsw  ax
  8a:   9b                      fwait
  8b:   9e                      sahf
  8c:   72 05                   jb     93 <_FpuExam@8+0x93>
  8e:   74 03                   je     93 <_FpuExam@8+0x93>
  90:   83 ca 08                or     edx,0x8
  93:   dd 65 94                frstor [ebp-0x6c]
  96:   8b c2                   mov    eax,edx
  98:   0c 01                   or     al,0x1
  9a:   5a                      pop    edx
  9b:   c9                      leave
  9c:   c2 08 00                ret    0x8
  9f:   d9 e5                   fxam
  a1:   9b df e0                fstsw  ax
  a4:   9b                      fwait
  a5:   9e                      sahf
  a6:   7b b4                   jnp    5c <_FpuExam@8+0x5c>
  a8:   83 ca 10                or     edx,0x10
  ab:   eb e6                   jmp    93 <_FpuExam@8+0x93>

FpuEexpX.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuEexpX@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuEexpX@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuEexpX@12+0x1c>
  18:   7a 02                   jp     1c <_FpuEexpX@12+0x1c>
  1a:   74 76                   je     92 <_FpuEexpX@12+0x92>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 0b                   je     34 <_FpuEexpX@12+0x34>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
```

```
  2f:   e9 80 00 00 00          jmp    b4 <_FpuEexpX@12+0xb4>
  34:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  37:   f7 45 10 10 00 00 00    test   DWORD PTR [ebp+0x10],0x10
  3e:   75 58                   jne    98 <_FpuEexpX@12+0x98>
  40:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
  47:   74 04                   je     4d <_FpuEexpX@12+0x4d>
  49:   db 28                   fld    TBYTE PTR [eax]
  4b:   eb 67                   jmp    b4 <_FpuEexpX@12+0xb4>
  4d:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
  54:   74 04                   je     5a <_FpuEexpX@12+0x5a>
  56:   dd 00                   fld    QWORD PTR [eax]
  58:   eb 5a                   jmp    b4 <_FpuEexpX@12+0xb4>
  5a:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
  61:   74 04                   je     67 <_FpuEexpX@12+0x67>
  63:   d9 00                   fld    DWORD PTR [eax]
  65:   eb 4d                   jmp    b4 <_FpuEexpX@12+0xb4>
  67:   f7 45 10 04 00 00 00    test   DWORD PTR [ebp+0x10],0x4
  6e:   74 04                   je     74 <_FpuEexpX@12+0x74>
  70:   db 00                   fild   DWORD PTR [eax]
  72:   eb 40                   jmp    b4 <_FpuEexpX@12+0xb4>
  74:   f7 45 10 00 00 00 01    test   DWORD PTR [ebp+0x10],0x1000000
  7b:   74 04                   je     81 <_FpuEexpX@12+0x81>
  7d:   df 28                   fild   QWORD PTR [eax]
  7f:   eb 33                   jmp    b4 <_FpuEexpX@12+0xb4>
  81:   f7 45 10 08 00 00 00    test   DWORD PTR [ebp+0x10],0x8
  88:   74 05                   je     8f <_FpuEexpX@12+0x8f>
  8a:   db 45 08                fild   DWORD PTR [ebp+0x8]
  8d:   eb 25                   jmp    b4 <_FpuEexpX@12+0xb4>
  8f:   dd 65 94                frstor [ebp-0x6c]
  92:   33 c0                   xor    eax,eax
  94:   c9                      leave
  95:   c2 0c 00                ret    0xc
  98:   83 f8 01                cmp    eax,0x1
  9b:   74 04                   je     a1 <_FpuEexpX@12+0xa1>
  9d:   d9 eb                   fldpi
  9f:   eb 13                   jmp    b4 <_FpuEexpX@12+0xb4>
  a1:   83 f8 02                cmp    eax,0x2
  a4:   74 e9                   je     8f <_FpuEexpX@12+0x8f>
  a6:   d9 e8                   fld1
  a8:   d9 ea                   fldl2e
  aa:   d8 e1                   fsub   st,st(1)
  ac:   d9 f0                   f2xm1
  ae:   d8 c1                   fadd   st,st(1)
  b0:   d9 fd                   fscale
  b2:   dd d9                   fstp   st(1)
  b4:   d9 ea                   fldl2e
  b6:   de c9                   fmulp  st(1),st
  b8:   d9 c0                   fld    st(0)
  ba:   d9 fc                   frndint
  bc:   dc e9                   fsubr  st(1),st
  be:   d9 c9                   fxch   st(1)
  c0:   d9 f0                   f2xm1
  c2:   d9 e8                   fld1
  c4:   de c1                   faddp  st(1),st
  c6:   d9 fd                   fscale
  c8:   9b df e0                fstsw  ax
  cb:   9b                      fwait
  cc:   d0 e8                   shr    al,1
  ce:   72 bf                   jb     8f <_FpuEexpX@12+0x8f>
  d0:   dd d9                   fstp   st(1)
  d2:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  d9:   74 05                   je     e0 <_FpuEexpX@12+0xe0>
  db:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
  de:   eb 1f                   jmp    ff <_FpuEexpX@12+0xff>
  e0:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  e3:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
  ea:   74 04                   je     f0 <_FpuEexpX@12+0xf0>
  ec:   d9 18                   fstp   DWORD PTR [eax]
  ee:   eb 0f                   jmp    ff <_FpuEexpX@12+0xff>
  f0:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
```

```
  f7:   74 04                   je     fd <_FpuEexpX@12+0xfd>
  f9:   dd 18                   fstp   QWORD PTR [eax]
  fb:   eb 02                   jmp    ff <_FpuEexpX@12+0xff>
  fd:   db 38                   fstp   TBYTE PTR [eax]
  ff:   dd 65 94                frstor [ebp-0x6c]
 102:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
 109:   74 02                   je     10d <_FpuEexpX@12+0x10d>
 10b:   dd d8                   fstp   st(0)
 10d:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
 114:   74 05                   je     11b <_FpuEexpX@12+0x11b>
 116:   dd c7                   ffree  st(7)
 118:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
 11b:   0c 01                   or     al,0x1
 11d:   c9                      leave
 11e:   c2 0c 00                ret    0xc

FpuDiv.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuDiv@16>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 14 01 01 00 00    test   DWORD PTR [ebp+0x14],0x101
   d:   74 0d                   je     1c <_FpuDiv@16+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuDiv@16+0x1c>
  18:   7a 02                   jp     1c <_FpuDiv@16+0x1c>
  1a:   74 76                   je     92 <_FpuDiv@16+0x92>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 14 01 00 00 00    test   DWORD PTR [ebp+0x14],0x1
  27:   74 0b                   je     34 <_FpuDiv@16+0x34>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   e9 80 00 00 00          jmp    b4 <_FpuDiv@16+0xb4>
  34:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  37:   f7 45 14 10 00 00 00    test   DWORD PTR [ebp+0x14],0x10
  3e:   75 58                   jne    98 <_FpuDiv@16+0x98>
  40:   f7 45 14 02 00 00 00    test   DWORD PTR [ebp+0x14],0x2
  47:   74 04                   je     4d <_FpuDiv@16+0x4d>
  49:   db 28                   fld    TBYTE PTR [eax]
  4b:   eb 67                   jmp    b4 <_FpuDiv@16+0xb4>
  4d:   f7 45 14 00 00 02 00    test   DWORD PTR [ebp+0x14],0x20000
  54:   74 04                   je     5a <_FpuDiv@16+0x5a>
  56:   dd 00                   fld    QWORD PTR [eax]
  58:   eb 5a                   jmp    b4 <_FpuDiv@16+0xb4>
  5a:   f7 45 14 00 00 01 00    test   DWORD PTR [ebp+0x14],0x10000
  61:   74 04                   je     67 <_FpuDiv@16+0x67>
  63:   d9 00                   fld    DWORD PTR [eax]
  65:   eb 4d                   jmp    b4 <_FpuDiv@16+0xb4>
  67:   f7 45 14 04 00 00 00    test   DWORD PTR [ebp+0x14],0x4
  6e:   74 04                   je     74 <_FpuDiv@16+0x74>
  70:   db 00                   fild   DWORD PTR [eax]
  72:   eb 40                   jmp    b4 <_FpuDiv@16+0xb4>
  74:   f7 45 14 00 00 00 01    test   DWORD PTR [ebp+0x14],0x1000000
  7b:   74 04                   je     81 <_FpuDiv@16+0x81>
  7d:   df 28                   fild   QWORD PTR [eax]
  7f:   eb 33                   jmp    b4 <_FpuDiv@16+0xb4>
  81:   f7 45 14 08 00 00 00    test   DWORD PTR [ebp+0x14],0x8
  88:   74 05                   je     8f <_FpuDiv@16+0x8f>
  8a:   db 45 08                fild   DWORD PTR [ebp+0x8]
  8d:   eb 25                   jmp    b4 <_FpuDiv@16+0xb4>
  8f:   dd 65 94                frstor [ebp-0x6c]
  92:   33 c0                   xor    eax,eax
  94:   c9                      leave
```

```
 95:   c2 10 00                ret    0x10
 98:   83 f8 01                cmp    eax,0x1
 9b:   75 04                   jne    a1 <_FpuDiv@16+0xa1>
 9d:   d9 eb                   fldpi
 9f:   eb 13                   jmp    b4 <_FpuDiv@16+0xb4>
 a1:   83 f8 02                cmp    eax,0x2
 a4:   75 e9                   jne    8f <_FpuDiv@16+0x8f>
 a6:   d9 e8                   fld1
 a8:   d9 ea                   fldl2e
 aa:   d8 e1                   fsub   st,st(1)
 ac:   d9 f0                   f2xm1
 ae:   d8 c1                   fadd   st,st(1)
 b0:   d9 fd                   fscale
 b2:   dd d9                   fstp   st(1)
 b4:   f7 45 14 00 01 00 00    test   DWORD PTR [ebp+0x14],0x100
 bb:   74 0b                   je     c8 <_FpuDiv@16+0xc8>
 bd:   8d 45 94                lea    eax,[ebp-0x6c]
 c0:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
 c3:   e9 80 00 00 00          jmp    148 <_FpuDiv@16+0x148>
 c8:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
 cb:   f7 45 14 00 10 00 00    test   DWORD PTR [ebp+0x14],0x1000
 d2:   75 54                   jne    128 <_FpuDiv@16+0x128>
 d4:   f7 45 14 00 02 00 00    test   DWORD PTR [ebp+0x14],0x200
 db:   74 04                   je     e1 <_FpuDiv@16+0xe1>
 dd:   db 28                   fld    TBYTE PTR [eax]
 df:   eb 67                   jmp    148 <_FpuDiv@16+0x148>
 e1:   f7 45 14 00 00 08 00    test   DWORD PTR [ebp+0x14],0x80000
 e8:   74 04                   je     ee <_FpuDiv@16+0xee>
 ea:   dd 00                   fld    QWORD PTR [eax]
 ec:   eb 5a                   jmp    148 <_FpuDiv@16+0x148>
 ee:   f7 45 14 00 00 04 00    test   DWORD PTR [ebp+0x14],0x40000
 f5:   74 04                   je     fb <_FpuDiv@16+0xfb>
 f7:   d9 00                   fld    DWORD PTR [eax]
 f9:   eb 4d                   jmp    148 <_FpuDiv@16+0x148>
 fb:   f7 45 14 00 04 00 00    test   DWORD PTR [ebp+0x14],0x400
102:   74 04                   je     108 <_FpuDiv@16+0x108>
104:   db 00                   fild   DWORD PTR [eax]
106:   eb 40                   jmp    148 <_FpuDiv@16+0x148>
108:   f7 45 14 00 00 00 02    test   DWORD PTR [ebp+0x14],0x2000000
10f:   74 04                   je     115 <_FpuDiv@16+0x115>
111:   df 28                   fild   QWORD PTR [eax]
113:   eb 33                   jmp    148 <_FpuDiv@16+0x148>
115:   f7 45 14 00 08 00 00    test   DWORD PTR [ebp+0x14],0x800
11c:   74 05                   je     123 <_FpuDiv@16+0x123>
11e:   db 45 0c                fild   DWORD PTR [ebp+0xc]
121:   eb 25                   jmp    148 <_FpuDiv@16+0x148>
123:   e9 67 ff ff ff          jmp    8f <_FpuDiv@16+0x8f>
128:   83 f8 01                cmp    eax,0x1
12b:   75 04                   jne    131 <_FpuDiv@16+0x131>
12d:   d9 eb                   fldpi
12f:   eb 17                   jmp    148 <_FpuDiv@16+0x148>
131:   83 f8 02                cmp    eax,0x2
134:   0f 85 55 ff ff ff       jne    8f <_FpuDiv@16+0x8f>
13a:   d9 e8                   fld1
13c:   d9 ea                   fldl2e
13e:   d8 e1                   fsub   st,st(1)
140:   d9 f0                   f2xm1
142:   d8 c1                   fadd   st,st(1)
144:   d9 fd                   fscale
146:   dd d9                   fstp   st(1)
148:   de f9                   fdivrp st(1),st
14a:   9b df e0                fstsw  ax
14d:   9b                      fwait
14e:   d0 e8                   shr    al,1
150:   0f 82 39 ff ff ff       jb     8f <_FpuDiv@16+0x8f>
156:   f7 45 14 80 00 00 00    test   DWORD PTR [ebp+0x14],0x80
15d:   74 05                   je     164 <_FpuDiv@16+0x164>
15f:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
162:   eb 1f                   jmp    183 <_FpuDiv@16+0x183>
164:   8b 45 10                mov    eax,DWORD PTR [ebp+0x10]
```

```
 167:   f7 45 14 00 00 10 00    test   DWORD PTR [ebp+0x14],0x100000
 16e:   74 04                   je     174 <_FpuDiv@16+0x174>
 170:   d9 18                   fstp   DWORD PTR [eax]
 172:   eb 0f                   jmp    183 <_FpuDiv@16+0x183>
 174:   f7 45 14 00 00 20 00    test   DWORD PTR [ebp+0x14],0x200000
 17b:   74 04                   je     181 <_FpuDiv@16+0x181>
 17d:   dd 18                   fstp   QWORD PTR [eax]
 17f:   eb 02                   jmp    183 <_FpuDiv@16+0x183>
 181:   db 38                   fstp   TBYTE PTR [eax]
 183:   dd 65 94                frstor [ebp-0x6c]
 186:   f7 45 14 01 01 00 00    test   DWORD PTR [ebp+0x14],0x101
 18d:   74 02                   je     191 <_FpuDiv@16+0x191>
 18f:   dd d8                   fstp   st(0)
 191:   f7 45 14 80 00 00 00    test   DWORD PTR [ebp+0x14],0x80
 198:   74 05                   je     19f <_FpuDiv@16+0x19f>
 19a:   dd c7                   ffree  st(7)
 19c:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
 19f:   0c 01                   or     al,0x1
 1a1:   c9                      leave
 1a2:   c2 10 00                ret    0x10

FpuCosh.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuCosh@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuCosh@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuCosh@12+0x1c>
  18:   7a 02                   jp     1c <_FpuCosh@12+0x1c>
  1a:   74 65                   je     81 <_FpuCosh@12+0x81>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 08                   je     31 <_FpuCosh@12+0x31>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   eb 59                   jmp    8a <_FpuCosh@12+0x8a>
  31:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  34:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
  3b:   74 04                   je     41 <_FpuCosh@12+0x41>
  3d:   db 28                   fld    TBYTE PTR [eax]
  3f:   eb 49                   jmp    8a <_FpuCosh@12+0x8a>
  41:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
  48:   74 04                   je     4e <_FpuCosh@12+0x4e>
  4a:   dd 00                   fld    QWORD PTR [eax]
  4c:   eb 3c                   jmp    8a <_FpuCosh@12+0x8a>
  4e:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
  55:   74 04                   je     5b <_FpuCosh@12+0x5b>
  57:   d9 00                   fld    DWORD PTR [eax]
  59:   eb 2f                   jmp    8a <_FpuCosh@12+0x8a>
  5b:   f7 45 10 04 00 00 00    test   DWORD PTR [ebp+0x10],0x4
  62:   74 04                   je     68 <_FpuCosh@12+0x68>
  64:   db 00                   fild   DWORD PTR [eax]
  66:   eb 22                   jmp    8a <_FpuCosh@12+0x8a>
  68:   f7 45 10 00 00 00 01    test   DWORD PTR [ebp+0x10],0x1000000
  6f:   74 04                   je     75 <_FpuCosh@12+0x75>
  71:   df 28                   fild   QWORD PTR [eax]
  73:   eb 15                   jmp    8a <_FpuCosh@12+0x8a>
  75:   f7 45 10 08 00 00 00    test   DWORD PTR [ebp+0x10],0x8
  7c:   75 09                   jne    87 <_FpuCosh@12+0x87>
  7e:   dd 65 94                frstor [ebp-0x6c]
  81:   33 c0                   xor    eax,eax
```

```
  83:   c9                      leave
  84:   c2 0c 00                ret    0xc
  87:   db 45 08                fild   DWORD PTR [ebp+0x8]
  8a:   d9 ea                   fldl2e
  8c:   de c9                   fmulp  st(1),st
  8e:   d9 c0                   fld    st(0)
  90:   d9 fc                   frndint
  92:   d9 c9                   fxch   st(1)
  94:   d8 e1                   fsub   st,st(1)
  96:   d9 f0                   f2xm1
  98:   d9 e8                   fld1
  9a:   de c1                   faddp  st(1),st
  9c:   d9 fd                   fscale
  9e:   dd d9                   fstp   st(1)
  a0:   d9 c0                   fld    st(0)
  a2:   d9 e8                   fld1
  a4:   de f1                   fdivp  st(1),st
  a6:   de c1                   faddp  st(1),st
  a8:   d9 e8                   fld1
  aa:   d9 e0                   fchs
  ac:   d9 c9                   fxch   st(1)
  ae:   d9 fd                   fscale
  b0:   dd d9                   fstp   st(1)
  b2:   9b df e0                fstsw  ax
  b5:   9b                      fwait
  b6:   d0 e8                   shr    al,1
  b8:   72 c4                   jb     7e <_FpuCosh@12+0x7e>
  ba:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  c1:   74 05                   je     c8 <_FpuCosh@12+0xc8>
  c3:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
  c6:   eb 1f                   jmp    e7 <_FpuCosh@12+0xe7>
  c8:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  cb:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
  d2:   74 04                   je     d8 <_FpuCosh@12+0xd8>
  d4:   d9 18                   fstp   DWORD PTR [eax]
  d6:   eb 0f                   jmp    e7 <_FpuCosh@12+0xe7>
  d8:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
  df:   74 04                   je     e5 <_FpuCosh@12+0xe5>
  e1:   dd 18                   fstp   QWORD PTR [eax]
  e3:   eb 02                   jmp    e7 <_FpuCosh@12+0xe7>
  e5:   db 38                   fstp   TBYTE PTR [eax]
  e7:   dd 65 94                frstor [ebp-0x6c]
  ea:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  f1:   74 02                   je     f5 <_FpuCosh@12+0xf5>
  f3:   dd d8                   fstp   st(0)
  f5:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  fc:   74 05                   je     103 <_FpuCosh@12+0x103>
  fe:   dd c7                   ffree  st(7)
 100:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
 103:   0c 01                   or     al,0x1
 105:   c9                      leave
 106:   c2 0c 00                ret    0xc

FpuCos.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuCos@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuCos@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuCos@12+0x1c>
  18:   7a 02                   jp     1c <_FpuCos@12+0x1c>
```

```
  1a:   74 65                   je     81 <_FpuCos@12+0x81>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 08                   je     31 <_FpuCos@12+0x31>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   eb 59                   jmp    8a <_FpuCos@12+0x8a>
  31:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  34:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
  3b:   74 04                   je     41 <_FpuCos@12+0x41>
  3d:   db 28                   fld    TBYTE PTR [eax]
  3f:   eb 49                   jmp    8a <_FpuCos@12+0x8a>
  41:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
  48:   74 04                   je     4e <_FpuCos@12+0x4e>
  4a:   dd 00                   fld    QWORD PTR [eax]
  4c:   eb 3c                   jmp    8a <_FpuCos@12+0x8a>
  4e:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
  55:   74 04                   je     5b <_FpuCos@12+0x5b>
  57:   d9 00                   fld    DWORD PTR [eax]
  59:   eb 2f                   jmp    8a <_FpuCos@12+0x8a>
  5b:   f7 45 10 04 00 00 00    test   DWORD PTR [ebp+0x10],0x4
  62:   74 04                   je     68 <_FpuCos@12+0x68>
  64:   db 00                   fild   DWORD PTR [eax]
  66:   eb 22                   jmp    8a <_FpuCos@12+0x8a>
  68:   f7 45 10 00 00 00 01    test   DWORD PTR [ebp+0x10],0x1000000
  6f:   74 04                   je     75 <_FpuCos@12+0x75>
  71:   df 28                   fild   QWORD PTR [eax]
  73:   eb 15                   jmp    8a <_FpuCos@12+0x8a>
  75:   f7 45 10 08 00 00 00    test   DWORD PTR [ebp+0x10],0x8
  7c:   75 09                   jne    87 <_FpuCos@12+0x87>
  7e:   dd 65 94                frstor [ebp-0x6c]
  81:   33 c0                   xor    eax,eax
  83:   c9                      leave
  84:   c2 0c 00                ret    0xc
  87:   db 45 08                fild   DWORD PTR [ebp+0x8]
  8a:   f7 45 10 20 00 00 00    test   DWORD PTR [ebp+0x10],0x20
  91:   75 0e                   jne    a1 <_FpuCos@12+0xa1>
  93:   d9 eb                   fldpi
  95:   de c9                   fmulp  st(1),st
  97:   68 b4 00 00 00          push   0xb4
  9c:   de 34 24                fidiv  WORD PTR [esp]
  9f:   9b                      fwait
  a0:   58                      pop    eax
  a1:   d9 eb                   fldpi
  a3:   d8 c0                   fadd   st,st(0)
  a5:   d9 c9                   fxch   st(1)
  a7:   d9 f8                   fprem
  a9:   d9 ff                   fcos
  ab:   9b df e0                fstsw  ax
  ae:   9b                      fwait
  af:   d0 e8                   shr    al,1
  b1:   72 cb                   jb     7e <_FpuCos@12+0x7e>
  b3:   9e                      sahf
  b4:   7a f1                   jp     a7 <_FpuCos@12+0xa7>
  b6:   dd d9                   fstp   st(1)
  b8:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  bf:   74 05                   je     c6 <_FpuCos@12+0xc6>
  c1:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
  c4:   eb 1f                   jmp    e5 <_FpuCos@12+0xe5>
  c6:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  c9:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
  d0:   74 04                   je     d6 <_FpuCos@12+0xd6>
  d2:   d9 18                   fstp   DWORD PTR [eax]
  d4:   eb 0f                   jmp    e5 <_FpuCos@12+0xe5>
  d6:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
  dd:   74 04                   je     e3 <_FpuCos@12+0xe3>
  df:   dd 18                   fstp   QWORD PTR [eax]
  e1:   eb 02                   jmp    e5 <_FpuCos@12+0xe5>
  e3:   db 38                   fstp   TBYTE PTR [eax]
  e5:   dd 65 94                frstor [ebp-0x6c]
```

```
  e8:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  ef:   74 02                   je     f3 <_FpuCos@12+0xf3>
  f1:   dd d8                   fstp   st(0)
  f3:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  fa:   74 05                   je     101 <_FpuCos@12+0x101>
  fc:   dd c7                   ffree  st(7)
  fe:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
 101:   0c 01                   or     al,0x1
 103:   c9                      leave
 104:   c2 0c 00                ret    0xc

FpuComp.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuComp@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 01 00 00    test   DWORD PTR [ebp+0x10],0x101
   d:   74 0d                   je     1c <_FpuComp@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuComp@12+0x1c>
  18:   7a 02                   jp     1c <_FpuComp@12+0x1c>
  1a:   74 76                   je     92 <_FpuComp@12+0x92>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 0b                   je     34 <_FpuComp@12+0x34>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   e9 80 00 00 00          jmp    b4 <_FpuComp@12+0xb4>
  34:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  37:   f7 45 10 10 00 00 00    test   DWORD PTR [ebp+0x10],0x10
  3e:   75 58                   jne    98 <_FpuComp@12+0x98>
  40:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
  47:   74 04                   je     4d <_FpuComp@12+0x4d>
  49:   db 28                   fld    TBYTE PTR [eax]
  4b:   eb 67                   jmp    b4 <_FpuComp@12+0xb4>
  4d:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
  54:   74 04                   je     5a <_FpuComp@12+0x5a>
  56:   dd 00                   fld    QWORD PTR [eax]
  58:   eb 5a                   jmp    b4 <_FpuComp@12+0xb4>
  5a:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
  61:   74 04                   je     67 <_FpuComp@12+0x67>
  63:   d9 00                   fld    DWORD PTR [eax]
  65:   eb 4d                   jmp    b4 <_FpuComp@12+0xb4>
  67:   f7 45 10 04 00 00 00    test   DWORD PTR [ebp+0x10],0x4
  6e:   74 04                   je     74 <_FpuComp@12+0x74>
  70:   db 00                   fild   DWORD PTR [eax]
  72:   eb 40                   jmp    b4 <_FpuComp@12+0xb4>
  74:   f7 45 10 00 00 00 01    test   DWORD PTR [ebp+0x10],0x1000000
  7b:   74 04                   je     81 <_FpuComp@12+0x81>
  7d:   df 28                   fild   QWORD PTR [eax]
  7f:   eb 33                   jmp    b4 <_FpuComp@12+0xb4>
  81:   f7 45 10 08 00 00 00    test   DWORD PTR [ebp+0x10],0x8
  88:   74 05                   je     8f <_FpuComp@12+0x8f>
  8a:   db 45 08                fild   DWORD PTR [ebp+0x8]
  8d:   eb 25                   jmp    b4 <_FpuComp@12+0xb4>
  8f:   dd 65 94                frstor [ebp-0x6c]
  92:   33 c0                   xor    eax,eax
  94:   c9                      leave
  95:   c2 0c 00                ret    0xc
  98:   83 f8 01                cmp    eax,0x1
  9b:   75 04                   jne    a1 <_FpuComp@12+0xa1>
  9d:   d9 eb                   fldpi
  9f:   eb 13                   jmp    b4 <_FpuComp@12+0xb4>
```

```
 a1:   83 f8 02                cmp    eax,0x2
 a4:   75 e9                   jne    8f <_FpuComp@12+0x8f>
 a6:   d9 e8                   fld1
 a8:   d9 ea                   fldl2e
 aa:   d8 e1                   fsub   st,st(1)
 ac:   d9 f0                   f2xm1
 ae:   d8 c1                   fadd   st,st(1)
 b0:   d9 fd                   fscale
 b2:   dd d9                   fstp   st(1)
 b4:   f7 45 10 00 01 00 00    test   DWORD PTR [ebp+0x10],0x100
 bb:   74 0b                   je     c8 <_FpuComp@12+0xc8>
 bd:   8d 45 94                lea    eax,[ebp-0x6c]
 c0:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
 c3:   e9 80 00 00 00          jmp    148 <_FpuComp@12+0x148>
 c8:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
 cb:   f7 45 10 00 10 00 00    test   DWORD PTR [ebp+0x10],0x1000
 d2:   75 54                   jne    128 <_FpuComp@12+0x128>
 d4:   f7 45 10 00 02 00 00    test   DWORD PTR [ebp+0x10],0x200
 db:   74 04                   je     e1 <_FpuComp@12+0xe1>
 dd:   db 28                   fld    TBYTE PTR [eax]
 df:   eb 67                   jmp    148 <_FpuComp@12+0x148>
 e1:   f7 45 10 00 00 08 00    test   DWORD PTR [ebp+0x10],0x80000
 e8:   74 04                   je     ee <_FpuComp@12+0xee>
 ea:   dd 00                   fld    QWORD PTR [eax]
 ec:   eb 5a                   jmp    148 <_FpuComp@12+0x148>
 ee:   f7 45 10 00 00 04 00    test   DWORD PTR [ebp+0x10],0x40000
 f5:   74 04                   je     fb <_FpuComp@12+0xfb>
 f7:   d9 00                   fld    DWORD PTR [eax]
 f9:   eb 4d                   jmp    148 <_FpuComp@12+0x148>
 fb:   f7 45 10 00 04 00 00    test   DWORD PTR [ebp+0x10],0x400
102:   74 04                   je     108 <_FpuComp@12+0x108>
104:   db 00                   fild   DWORD PTR [eax]
106:   eb 40                   jmp    148 <_FpuComp@12+0x148>
108:   f7 45 10 00 00 00 02    test   DWORD PTR [ebp+0x10],0x2000000
10f:   74 04                   je     115 <_FpuComp@12+0x115>
111:   df 28                   fild   QWORD PTR [eax]
113:   eb 33                   jmp    148 <_FpuComp@12+0x148>
115:   f7 45 10 00 08 00 00    test   DWORD PTR [ebp+0x10],0x800
11c:   74 05                   je     123 <_FpuComp@12+0x123>
11e:   db 45 0c                fild   DWORD PTR [ebp+0xc]
121:   eb 25                   jmp    148 <_FpuComp@12+0x148>
123:   e9 67 ff ff ff          jmp    8f <_FpuComp@12+0x8f>
128:   83 f8 01                cmp    eax,0x1
12b:   75 04                   jne    131 <_FpuComp@12+0x131>
12d:   d9 eb                   fldpi
12f:   eb 17                   jmp    148 <_FpuComp@12+0x148>
131:   83 f8 02                cmp    eax,0x2
134:   0f 85 55 ff ff ff       jne    8f <_FpuComp@12+0x8f>
13a:   d9 e8                   fld1
13c:   d9 ea                   fldl2e
13e:   d8 e1                   fsub   st,st(1)
140:   d9 f0                   f2xm1
142:   d8 c1                   fadd   st,st(1)
144:   d9 fd                   fscale
146:   dd d9                   fstp   st(1)
148:   d9 c9                   fxch   st(1)
14a:   d8 d1                   fcom   st(1)
14c:   9b df e0                fstsw  ax
14f:   9b                      fwait
150:   d0 e8                   shr    al,1
152:   0f 82 37 ff ff ff       jb     8f <_FpuComp@12+0x8f>
158:   9e                      sahf
159:   0f 8a 30 ff ff ff       jp     8f <_FpuComp@12+0x8f>
15f:   77 10                   ja     171 <_FpuComp@12+0x171>
161:   72 07                   jb     16a <_FpuComp@12+0x16a>
163:   b8 01 00 00 00          mov    eax,0x1
168:   eb 0c                   jmp    176 <_FpuComp@12+0x176>
16a:   b8 04 00 00 00          mov    eax,0x4
16f:   eb 05                   jmp    176 <_FpuComp@12+0x176>
171:   b8 02 00 00 00          mov    eax,0x2
```

```
 176:   dd 65 94                frstor [ebp-0x6c]
 179:   c9                      leave
 17a:   c2 0c 00                ret    0xc

FpuChs.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuChs@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuChs@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuChs@12+0x1c>
  18:   7a 02                   jp     1c <_FpuChs@12+0x1c>
  1a:   74 42                   je     5e <_FpuChs@12+0x5e>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 08                   je     31 <_FpuChs@12+0x31>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   eb 38                   jmp    69 <_FpuChs@12+0x69>
  31:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  34:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
  3b:   74 04                   je     41 <_FpuChs@12+0x41>
  3d:   db 28                   fld    TBYTE PTR [eax]
  3f:   eb 28                   jmp    69 <_FpuChs@12+0x69>
  41:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
  48:   74 04                   je     4e <_FpuChs@12+0x4e>
  4a:   dd 00                   fld    QWORD PTR [eax]
  4c:   eb 1b                   jmp    69 <_FpuChs@12+0x69>
  4e:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
  55:   74 04                   je     5b <_FpuChs@12+0x5b>
  57:   d9 00                   fld    DWORD PTR [eax]
  59:   eb 0e                   jmp    69 <_FpuChs@12+0x69>
  5b:   dd 65 94                frstor [ebp-0x6c]
  5e:   33 c0                   xor    eax,eax
  60:   c9                      leave
  61:   c2 0c 00                ret    0xc
  64:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  67:   db 28                   fld    TBYTE PTR [eax]
  69:   d9 e0                   fchs
  6b:   9b df e0                fstsw  ax
  6e:   9b                      fwait
  6f:   d0 e8                   shr    al,1
  71:   72 e8                   jb     5b <_FpuChs@12+0x5b>
  73:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  7a:   74 05                   je     81 <_FpuChs@12+0x81>
  7c:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
  7f:   eb 1f                   jmp    a0 <_FpuChs@12+0xa0>
  81:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  84:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
  8b:   74 04                   je     91 <_FpuChs@12+0x91>
  8d:   d9 18                   fstp   DWORD PTR [eax]
  8f:   eb 0f                   jmp    a0 <_FpuChs@12+0xa0>
  91:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
  98:   74 04                   je     9e <_FpuChs@12+0x9e>
  9a:   dd 18                   fstp   QWORD PTR [eax]
  9c:   eb 02                   jmp    a0 <_FpuChs@12+0xa0>
  9e:   db 38                   fstp   TBYTE PTR [eax]
  a0:   dd 65 94                frstor [ebp-0x6c]
  a3:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  aa:   74 02                   je     ae <_FpuChs@12+0xae>
  ac:   dd d8                   fstp   st(0)
```

```
  ae:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  b5:   74 05                   je     bc <_FpuChs@12+0xbc>
  b7:   dd c7                   ffree  st(7)
  b9:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
  bc:   0c 01                   or     al,0x1
  be:   c9                      leave
  bf:   c2 0c 00                ret    0xc

FpuAtoFL.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuAtoFL@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   81 c4 74 ff ff ff       add    esp,0xffffff74
   9:   9b dd 75 94             fsave  [ebp-0x6c]
   d:   53                      push   ebx
   e:   51                      push   ecx
   f:   52                      push   edx
  10:   56                      push   esi
  11:   57                      push   edi
  12:   33 c0                   xor    eax,eax
  14:   33 db                   xor    ebx,ebx
  16:   33 d2                   xor    edx,edx
  18:   8d bd 76 ff ff ff       lea    edi,[ebp-0x8a]
  1e:   ab                      stos   DWORD PTR es:[edi],eax
  1f:   ab                      stos   DWORD PTR es:[edi],eax
  20:   ab                      stos   DWORD PTR es:[edi],eax
  21:   ab                      stos   DWORD PTR es:[edi],eax
  22:   ab                      stos   DWORD PTR es:[edi],eax
  23:   8d bd 7e ff ff ff       lea    edi,[ebp-0x82]
  29:   8b 75 08                mov    esi,DWORD PTR [ebp+0x8]
  2c:   b9 12 00 00 00          mov    ecx,0x12
  31:   ac                      lods   al,BYTE PTR ds:[esi]
  32:   3c 20                   cmp    al,0x20
  34:   74 fb                   je     31 <_FpuAtoFL@12+0x31>
  36:   0a c0                   or     al,al
  38:   75 0e                   jne    48 <_FpuAtoFL@12+0x48>
  3a:   dd 65 94                frstor [ebp-0x6c]
  3d:   33 c0                   xor    eax,eax
  3f:   5f                      pop    edi
  40:   5e                      pop    esi
  41:   5a                      pop    edx
  42:   59                      pop    ecx
  43:   5b                      pop    ebx
  44:   c9                      leave
  45:   c2 0c 00                ret    0xc
  48:   3c 2b                   cmp    al,0x2b
  4a:   74 06                   je     52 <_FpuAtoFL@12+0x52>
  4c:   3c 2d                   cmp    al,0x2d
  4e:   75 0b                   jne    5b <_FpuAtoFL@12+0x5b>
  50:   b4 80                   mov    ah,0x80
  52:   88 67 01                mov    BYTE PTR [edi+0x1],ah
  55:   88 67 0b                mov    BYTE PTR [edi+0xb],ah
  58:   33 c0                   xor    eax,eax
  5a:   ac                      lods   al,BYTE PTR ds:[esi]
  5b:   3c 2e                   cmp    al,0x2e
  5d:   75 19                   jne    78 <_FpuAtoFL@12+0x78>
  5f:   8d bd 76 ff ff ff       lea    edi,[ebp-0x8a]
  65:   e8 c4 02 00 00          call   32e <_FpuAtoFL@12+0x32e>
  6a:   ac                      lods   al,BYTE PTR ds:[esi]
  6b:   8d 7d 88                lea    edi,[ebp-0x78]
  6e:   b1 12                   mov    cl,0x12
  70:   80 e7 04                and    bh,0x4
  73:   e9 13 01 00 00          jmp    18b <_FpuAtoFL@12+0x18b>
  78:   3c 65                   cmp    al,0x65
  7a:   75 17                   jne    93 <_FpuAtoFL@12+0x93>
  7c:   80 f9 12                cmp    cl,0x12
```

```
  7f:   75 02                   jne    83 <_FpuAtoFL@12+0x83>
  81:   eb b7                   jmp    3a <_FpuAtoFL@12+0x3a>
  83:   8d bd 76 ff ff ff       lea    edi,[ebp-0x8a]
  89:   e8 a0 02 00 00          call   32e <_FpuAtoFL@12+0x32e>
  8e:   e9 31 02 00 00          jmp    2c4 <_FpuAtoFL@12+0x2c4>
  93:   3c 45                   cmp    al,0x45
  95:   75 17                   jne    ae <_FpuAtoFL@12+0xae>
  97:   80 f9 12                cmp    cl,0x12
  9a:   75 02                   jne    9e <_FpuAtoFL@12+0x9e>
  9c:   eb 9c                   jmp    3a <_FpuAtoFL@12+0x3a>
  9e:   8d bd 76 ff ff ff       lea    edi,[ebp-0x8a]
  a4:   e8 85 02 00 00          call   32e <_FpuAtoFL@12+0x32e>
  a9:   e9 16 02 00 00          jmp    2c4 <_FpuAtoFL@12+0x2c4>
  ae:   0a c0                   or     al,al
  b0:   75 15                   jne    c7 <_FpuAtoFL@12+0xc7>
  b2:   f6 c7 04                test   bh,0x4
  b5:   74 83                   je     3a <_FpuAtoFL@12+0x3a>
  b7:   8d bd 76 ff ff ff       lea    edi,[ebp-0x8a]
  bd:   e8 6c 02 00 00          call   32e <_FpuAtoFL@12+0x32e>
  c2:   e9 a8 01 00 00          jmp    26f <_FpuAtoFL@12+0x26f>
  c7:   2c 30                   sub    al,0x30
  c9:   0f 82 6b ff ff ff       jb     3a <_FpuAtoFL@12+0x3a>
  cf:   75 0e                   jne    df <_FpuAtoFL@12+0xdf>
  d1:   f6 c7 02                test   bh,0x2
  d4:   75 09                   jne    df <_FpuAtoFL@12+0xdf>
  d6:   80 cf 04                or     bh,0x4
  d9:   ac                      lods   al,BYTE PTR ds:[esi]
  da:   e9 7c ff ff ff          jmp    5b <_FpuAtoFL@12+0x5b>
  df:   3c 09                   cmp    al,0x9
  e1:   0f 87 53 ff ff ff       ja     3a <_FpuAtoFL@12+0x3a>
  e7:   80 cf 06                or     bh,0x6
  ea:   83 e9 01                sub    ecx,0x1
  ed:   0f 82 47 ff ff ff       jb     3a <_FpuAtoFL@12+0x3a>
  f3:   8a e0                   mov    ah,al
  f5:   ac                      lods   al,BYTE PTR ds:[esi]
  f6:   3c 2e                   cmp    al,0x2e
  f8:   75 1e                   jne    118 <_FpuAtoFL@12+0x118>
  fa:   b0 00                   mov    al,0x0
  fc:   66 c1 c8 04             ror    ax,0x4
 100:   88 07                   mov    BYTE PTR [edi],al
 102:   8d bd 76 ff ff ff       lea    edi,[ebp-0x8a]
 108:   e8 21 02 00 00          call   32e <_FpuAtoFL@12+0x32e>
 10d:   8d 7d 88                lea    edi,[ebp-0x78]
 110:   b1 12                   mov    cl,0x12
 112:   80 e7 04                and    bh,0x4
 115:   ac                      lods   al,BYTE PTR ds:[esi]
 116:   eb 73                   jmp    18b <_FpuAtoFL@12+0x18b>
 118:   3c 65                   cmp    al,0x65
 11a:   75 18                   jne    134 <_FpuAtoFL@12+0x134>
 11c:   b0 00                   mov    al,0x0
 11e:   66 c1 c8 04             ror    ax,0x4
 122:   88 07                   mov    BYTE PTR [edi],al
 124:   8d bd 76 ff ff ff       lea    edi,[ebp-0x8a]
 12a:   e8 ff 01 00 00          call   32e <_FpuAtoFL@12+0x32e>
 12f:   e9 90 01 00 00          jmp    2c4 <_FpuAtoFL@12+0x2c4>
 134:   3c 45                   cmp    al,0x45
 136:   75 18                   jne    150 <_FpuAtoFL@12+0x150>
 138:   b0 00                   mov    al,0x0
 13a:   66 c1 c8 04             ror    ax,0x4
 13e:   88 07                   mov    BYTE PTR [edi],al
 140:   8d bd 76 ff ff ff       lea    edi,[ebp-0x8a]
 146:   e8 e3 01 00 00          call   32e <_FpuAtoFL@12+0x32e>
 14b:   e9 74 01 00 00          jmp    2c4 <_FpuAtoFL@12+0x2c4>
 150:   0a c0                   or     al,al
 152:   75 16                   jne    16a <_FpuAtoFL@12+0x16a>
 154:   66 c1 c8 04             ror    ax,0x4
 158:   88 07                   mov    BYTE PTR [edi],al
 15a:   8d bd 76 ff ff ff       lea    edi,[ebp-0x8a]
 160:   e8 c9 01 00 00          call   32e <_FpuAtoFL@12+0x32e>
 165:   e9 05 01 00 00          jmp    26f <_FpuAtoFL@12+0x26f>
```

```
16a:   2c 30                   sub    al,0x30
16c:   0f 82 c8 fe ff ff       jb     3a <_FpuAtoFL@12+0x3a>
172:   3c 09                   cmp    al,0x9
174:   0f 87 c0 fe ff ff       ja     3a <_FpuAtoFL@12+0x3a>
17a:   49                      dec    ecx
17b:   c0 c0 04                rol    al,0x4
17e:   66 c1 c8 04             ror    ax,0x4
182:   88 07                   mov    BYTE PTR [edi],al
184:   4f                      dec    edi
185:   ac                      lods   al,BYTE PTR ds:[esi]
186:   e9 d0 fe ff ff          jmp    5b <_FpuAtoFL@12+0x5b>
18b:   3c 65                   cmp    al,0x65
18d:   75 0d                   jne    19c <_FpuAtoFL@12+0x19c>
18f:   8d 7d 80                lea    edi,[ebp-0x80]
192:   e8 e8 01 00 00          call   37f <_FpuAtoFL@12+0x37f>
197:   e9 28 01 00 00          jmp    2c4 <_FpuAtoFL@12+0x2c4>
19c:   3c 45                   cmp    al,0x45
19e:   75 0d                   jne    1ad <_FpuAtoFL@12+0x1ad>
1a0:   8d 7d 80                lea    edi,[ebp-0x80]
1a3:   e8 d7 01 00 00          call   37f <_FpuAtoFL@12+0x37f>
1a8:   e9 17 01 00 00          jmp    2c4 <_FpuAtoFL@12+0x2c4>
1ad:   0a c0                   or     al,al
1af:   75 16                   jne    1c7 <_FpuAtoFL@12+0x1c7>
1b1:   f6 c7 04                test   bh,0x4
1b4:   0f 84 80 fe ff ff       je     3a <_FpuAtoFL@12+0x3a>
1ba:   8d 7d 80                lea    edi,[ebp-0x80]
1bd:   e8 bd 01 00 00          call   37f <_FpuAtoFL@12+0x37f>
1c2:   e9 a8 00 00 00          jmp    26f <_FpuAtoFL@12+0x26f>
1c7:   2c 30                   sub    al,0x30
1c9:   0f 82 6b fe ff ff       jb     3a <_FpuAtoFL@12+0x3a>
1cf:   3c 09                   cmp    al,0x9
1d1:   0f 87 63 fe ff ff       ja     3a <_FpuAtoFL@12+0x3a>
1d7:   80 cf 04                or     bh,0x4
1da:   0a c0                   or     al,al
1dc:   74 03                   je     1e1 <_FpuAtoFL@12+0x1e1>
1de:   80 cf 02                or     bh,0x2
1e1:   83 e9 01                sub    ecx,0x1
1e4:   73 0d                   jae    1f3 <_FpuAtoFL@12+0x1f3>
1e6:   0a c0                   or     al,al
1e8:   75 04                   jne    1ee <_FpuAtoFL@12+0x1ee>
1ea:   41                      inc    ecx
1eb:   ac                      lods   al,BYTE PTR ds:[esi]
1ec:   eb 9d                   jmp    18b <_FpuAtoFL@12+0x18b>
1ee:   e9 47 fe ff ff          jmp    3a <_FpuAtoFL@12+0x3a>
1f3:   8a e0                   mov    ah,al
1f5:   ac                      lods   al,BYTE PTR ds:[esi]
1f6:   3c 65                   cmp    al,0x65
1f8:   75 15                   jne    20f <_FpuAtoFL@12+0x20f>
1fa:   b0 00                   mov    al,0x0
1fc:   66 c1 c8 04             ror    ax,0x4
200:   88 07                   mov    BYTE PTR [edi],al
202:   8d 7d 80                lea    edi,[ebp-0x80]
205:   e8 75 01 00 00          call   37f <_FpuAtoFL@12+0x37f>
20a:   e9 b5 00 00 00          jmp    2c4 <_FpuAtoFL@12+0x2c4>
20f:   3c 45                   cmp    al,0x45
211:   75 15                   jne    228 <_FpuAtoFL@12+0x228>
213:   b0 00                   mov    al,0x0
215:   66 c1 c8 04             ror    ax,0x4
219:   88 07                   mov    BYTE PTR [edi],al
21b:   8d 7d 80                lea    edi,[ebp-0x80]
21e:   e8 5c 01 00 00          call   37f <_FpuAtoFL@12+0x37f>
223:   e9 9c 00 00 00          jmp    2c4 <_FpuAtoFL@12+0x2c4>
228:   0a c0                   or     al,al
22a:   75 1b                   jne    247 <_FpuAtoFL@12+0x247>
22c:   f6 c7 04                test   bh,0x4
22f:   0f 84 05 fe ff ff       je     3a <_FpuAtoFL@12+0x3a>
235:   b0 00                   mov    al,0x0
237:   66 c1 c8 04             ror    ax,0x4
23b:   88 07                   mov    BYTE PTR [edi],al
23d:   8d 7d 80                lea    edi,[ebp-0x80]
```

```
240:   e8 3a 01 00 00          call   37f <_FpuAtoFL@12+0x37f>
245:   eb 28                   jmp    26f <_FpuAtoFL@12+0x26f>
247:   2c 30                   sub    al,0x30
249:   0f 82 eb fd ff ff       jb     3a <_FpuAtoFL@12+0x3a>
24f:   3c 09                   cmp    al,0x9
251:   0f 87 e3 fd ff ff       ja     3a <_FpuAtoFL@12+0x3a>
257:   0a c0                   or     al,al
259:   74 03                   je     25e <_FpuAtoFL@12+0x25e>
25b:   80 cf 02                or     bh,0x2
25e:   49                      dec    ecx
25f:   c0 c0 04                rol    al,0x4
262:   66 c1 c8 04             ror    ax,0x4
266:   88 07                   mov    BYTE PTR [edi],al
268:   4f                      dec    edi
269:   ac                      lods   al,BYTE PTR ds:[esi]
26a:   e9 1c ff ff ff          jmp    18b <_FpuAtoFL@12+0x18b>
26f:   9b df e0                fstsw  ax
272:   9b                      fwait
273:   d0 e8                   shr    al,1
275:   0f 82 bf fd ff ff       jb     3a <_FpuAtoFL@12+0x3a>
27b:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
282:   74 05                   je     289 <_FpuAtoFL@12+0x289>
284:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
287:   eb 1f                   jmp    2a8 <_FpuAtoFL@12+0x2a8>
289:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
28c:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
293:   74 04                   je     299 <_FpuAtoFL@12+0x299>
295:   d9 18                   fstp   DWORD PTR [eax]
297:   eb 0f                   jmp    2a8 <_FpuAtoFL@12+0x2a8>
299:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
2a0:   74 04                   je     2a6 <_FpuAtoFL@12+0x2a6>
2a2:   dd 18                   fstp   QWORD PTR [eax]
2a4:   eb 02                   jmp    2a8 <_FpuAtoFL@12+0x2a8>
2a6:   db 38                   fstp   TBYTE PTR [eax]
2a8:   dd 65 94                frstor [ebp-0x6c]
2ab:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
2b2:   74 05                   je     2b9 <_FpuAtoFL@12+0x2b9>
2b4:   dd c7                   ffree  st(7)
2b6:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
2b9:   0c 01                   or     al,0x1
2bb:   5f                      pop    edi
2bc:   5e                      pop    esi
2bd:   5a                      pop    edx
2be:   59                      pop    ecx
2bf:   5b                      pop    ebx
2c0:   c9                      leave
2c1:   c2 0c 00                ret    0xc
2c4:   33 c0                   xor    eax,eax
2c6:   33 d2                   xor    edx,edx
2c8:   ac                      lods   al,BYTE PTR ds:[esi]
2c9:   3c 2b                   cmp    al,0x2b
2cb:   74 07                   je     2d4 <_FpuAtoFL@12+0x2d4>
2cd:   3c 2d                   cmp    al,0x2d
2cf:   75 04                   jne    2d5 <_FpuAtoFL@12+0x2d5>
2d1:   f9                      stc
2d2:   d1 d8                   rcr    eax,1
2d4:   ac                      lods   al,BYTE PTR ds:[esi]
2d5:   50                      push   eax
2d6:   25 ff 00 00 00          and    eax,0xff
2db:   75 06                   jne    2e3 <_FpuAtoFL@12+0x2e3>
2dd:   58                      pop    eax
2de:   e9 57 fd ff ff          jmp    3a <_FpuAtoFL@12+0x3a>
2e3:   2c 30                   sub    al,0x30
2e5:   72 f6                   jb     2dd <_FpuAtoFL@12+0x2dd>
2e7:   3c 09                   cmp    al,0x9
2e9:   77 f2                   ja     2dd <_FpuAtoFL@12+0x2dd>
2eb:   03 d2                   add    edx,edx
2ed:   8d 14 92                lea    edx,[edx+edx*4]
2f0:   03 d0                   add    edx,eax
2f2:   81 fa 43 13 00 00       cmp    edx,0x1343
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2f8:   77 e3                 ja     2dd <_FpuAtoFL@12+0x2dd>
2fa:   ac                    lods   al,BYTE PTR ds:[esi]
2fb:   0a c0                 or     al,al
2fd:   75 e4                 jne    2e3 <_FpuAtoFL@12+0x2e3>
2ff:   58                    pop    eax
300:   d1 d0                 rcl    eax,1
302:   73 02                 jae    306 <_FpuAtoFL@12+0x306>
304:   f7 da                 neg    edx
306:   e8 07 00 00 00        call   312 <_FpuAtoFL@12+0x312>
30b:   de c9                 fmulp  st(1),st
30d:   e9 5d ff ff ff        jmp    26f <_FpuAtoFL@12+0x26f>
312:   52                    push   edx
313:   db 04 24              fild   DWORD PTR [esp]
316:   d9 e9                 fldl2t
318:   de c9                 fmulp  st(1),st
31a:   5a                    pop    edx
31b:   d9 c0                 fld    st(0)
31d:   d9 fc                 frndint
31f:   dc e9                 fsubr  st(1),st
321:   d9 c9                 fxch   st(1)
323:   d9 f0                 f2xm1
325:   d9 e8                 fld1
327:   de c1                 faddp  st(1),st
329:   d9 fd                 fscale
32b:   dd d9                 fstp   st(1)
32d:   c3                    ret
32e:   56                    push   esi
32f:   80 f9 12              cmp    cl,0x12
332:   75 04                 jne    338 <_FpuAtoFL@12+0x338>
334:   d9 ee                 fldz
336:   eb 45                 jmp    37d <_FpuAtoFL@12+0x37d>
338:   8b f7                 mov    esi,edi
33a:   83 e9 12              sub    ecx,0x12
33d:   f7 d9                 neg    ecx
33f:   d1 e9                 shr    ecx,1
341:   57                    push   edi
342:   72 0d                 jb     351 <_FpuAtoFL@12+0x351>
344:   ba 09 00 00 00        mov    edx,0x9
349:   2b d1                 sub    edx,ecx
34b:   03 f2                 add    esi,edx
34d:   f3 a4                 rep movs BYTE PTR es:[edi],BYTE PTR ds:[esi]
34f:   eb 23                 jmp    374 <_FpuAtoFL@12+0x374>
351:   ba 08 00 00 00        mov    edx,0x8
356:   2b d1                 sub    edx,ecx
358:   03 f2                 add    esi,edx
35a:   33 c0                 xor    eax,eax
35c:   ac                    lods   al,BYTE PTR ds:[esi]
35d:   66 c1 c0 04           rol    ax,0x4
361:   85 c9                 test   ecx,ecx
363:   74 0c                 je     371 <_FpuAtoFL@12+0x371>
365:   c0 c4 04              rol    ah,0x4
368:   ac                    lods   al,BYTE PTR ds:[esi]
369:   66 c1 c0 04           rol    ax,0x4
36d:   aa                    stos   BYTE PTR es:[edi],al
36e:   49                    dec    ecx
36f:   75 f4                 jne    365 <_FpuAtoFL@12+0x365>
371:   88 27                 mov    BYTE PTR [edi],ah
373:   47                    inc    edi
374:   8b ca                 mov    ecx,edx
376:   33 c0                 xor    eax,eax
378:   f3 aa                 rep stos BYTE PTR es:[edi],al
37a:   5f                    pop    edi
37b:   df 27                 fbld   TBYTE PTR [edi]
37d:   5e                    pop    esi
37e:   c3                    ret
37f:   f6 c7 02              test   bh,0x2
382:   75 01                 jne    385 <_FpuAtoFL@12+0x385>
384:   c3                    ret
385:   80 f9 12              cmp    cl,0x12
388:   75 04                 jne    38e <_FpuAtoFL@12+0x38e>
```

```
 38a:   d9 ee                   fldz
 38c:   eb 0e                   jmp    39c <_FpuAtoFL@12+0x39c>
 38e:   df 27                   fbld   TBYTE PTR [edi]
 390:   ba ee ff ff ff          mov    edx,0xfffffee
 395:   e8 78 ff ff ff          call   312 <_FpuAtoFL@12+0x312>
 39a:   de c9                   fmulp  st(1),st
 39c:   de c1                   faddp  st(1),st
 39e:   c3                      ret

FpuArctanh.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuArctanh@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuArctanh@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuArctanh@12+0x1c>
  18:   7a 02                   jp     1c <_FpuArctanh@12+0x1c>
  1a:   74 42                   je     5e <_FpuArctanh@12+0x5e>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 08                   je     31 <_FpuArctanh@12+0x31>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   eb 38                   jmp    69 <_FpuArctanh@12+0x69>
  31:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  34:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
  3b:   74 04                   je     41 <_FpuArctanh@12+0x41>
  3d:   db 28                   fld    TBYTE PTR [eax]
  3f:   eb 28                   jmp    69 <_FpuArctanh@12+0x69>
  41:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
  48:   74 04                   je     4e <_FpuArctanh@12+0x4e>
  4a:   dd 00                   fld    QWORD PTR [eax]
  4c:   eb 1b                   jmp    69 <_FpuArctanh@12+0x69>
  4e:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
  55:   74 04                   je     5b <_FpuArctanh@12+0x5b>
  57:   d9 00                   fld    DWORD PTR [eax]
  59:   eb 0e                   jmp    69 <_FpuArctanh@12+0x69>
  5b:   dd 65 94                frstor [ebp-0x6c]
  5e:   33 c0                   xor    eax,eax
  60:   c9                      leave
  61:   c2 0c 00                ret    0xc
  64:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  67:   db 28                   fld    TBYTE PTR [eax]
  69:   d9 c0                   fld    st(0)
  6b:   d9 e8                   fld1
  6d:   de c1                   faddp  st(1),st
  6f:   d9 c9                   fxch   st(1)
  71:   d9 e8                   fld1
  73:   de e1                   fsubp  st(1),st
  75:   de f9                   fdivrp st(1),st
  77:   d9 ed                   fldln2
  79:   d9 c9                   fxch   st(1)
  7b:   d9 f1                   fyl2x
  7d:   d9 e8                   fld1
  7f:   d9 e0                   fchs
  81:   d9 c9                   fxch   st(1)
  83:   d9 fd                   fscale
  85:   dd d9                   fstp   st(1)
  87:   9b df e0                fstsw  ax
  8a:   9b                      fwait
  8b:   d1 e8                   shr    eax,1
```

```
  8d:   72 cc                   jb     5b <_FpuArctanh@12+0x5b>
  8f:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  96:   74 05                   je     9d <_FpuArctanh@12+0x9d>
  98:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
  9b:   eb 1f                   jmp    bc <_FpuArctanh@12+0xbc>
  9d:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  a0:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
  a7:   74 04                   je     ad <_FpuArctanh@12+0xad>
  a9:   d9 18                   fstp   DWORD PTR [eax]
  ab:   eb 0f                   jmp    bc <_FpuArctanh@12+0xbc>
  ad:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
  b4:   74 04                   je     ba <_FpuArctanh@12+0xba>
  b6:   dd 18                   fstp   QWORD PTR [eax]
  b8:   eb 02                   jmp    bc <_FpuArctanh@12+0xbc>
  ba:   db 38                   fstp   TBYTE PTR [eax]
  bc:   dd 65 94                frstor [ebp-0x6c]
  bf:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  c6:   74 02                   je     ca <_FpuArctanh@12+0xca>
  c8:   dd d8                   fstp   st(0)
  ca:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  d1:   74 05                   je     d8 <_FpuArctanh@12+0xd8>
  d3:   dd c7                   ffree  st(7)
  d5:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
  d8:   0c 01                   or     al,0x1
  da:   c9                      leave
  db:   c2 0c 00                ret    0xc

FpuArctan.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuArctan@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuArctan@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuArctan@12+0x1c>
  18:   7a 02                   jp     1c <_FpuArctan@12+0x1c>
  1a:   74 42                   je     5e <_FpuArctan@12+0x5e>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 08                   je     31 <_FpuArctan@12+0x31>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   eb 38                   jmp    69 <_FpuArctan@12+0x69>
  31:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  34:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
  3b:   74 04                   je     41 <_FpuArctan@12+0x41>
  3d:   db 28                   fld    TBYTE PTR [eax]
  3f:   eb 28                   jmp    69 <_FpuArctan@12+0x69>
  41:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
  48:   74 04                   je     4e <_FpuArctan@12+0x4e>
  4a:   dd 00                   fld    QWORD PTR [eax]
  4c:   eb 1b                   jmp    69 <_FpuArctan@12+0x69>
  4e:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
  55:   74 04                   je     5b <_FpuArctan@12+0x5b>
  57:   d9 00                   fld    DWORD PTR [eax]
  59:   eb 0e                   jmp    69 <_FpuArctan@12+0x69>
  5b:   dd 65 94                frstor [ebp-0x6c]
  5e:   33 c0                   xor    eax,eax
  60:   c9                      leave
  61:   c2 0c 00                ret    0xc
  64:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  67:   db 28                   fld    TBYTE PTR [eax]
```

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  69:   d9 e8                   fld1
  6b:   d9 f3                   fpatan
  6d:   9b df e0                fstsw  ax
  70:   9b                      fwait
  71:   d1 e8                   shr    eax,1
  73:   72 e6                   jb     5b <_FpuArctan@12+0x5b>
  75:   f7 45 10 20 00 00 00    test   DWORD PTR [ebp+0x10],0x20
  7c:   75 20                   jne    9e <_FpuArctan@12+0x9e>
  7e:   68 b4 00 00 00          push   0xb4
  83:   da 0c 24                fimul  DWORD PTR [esp]
  86:   d9 eb                   fldpi
  88:   de f9                   fdivrp st(1),st
  8a:   58                      pop    eax
  8b:   d9 e4                   ftst
  8d:   9b df e0                fstsw  ax
  90:   9b                      fwait
  91:   9e                      sahf
  92:   73 0a                   jae    9e <_FpuArctan@12+0x9e>
  94:   68 68 01 00 00          push   0x168
  99:   da 04 24                fiadd  DWORD PTR [esp]
  9c:   9b                      fwait
  9d:   58                      pop    eax
  9e:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  a5:   74 05                   je     ac <_FpuArctan@12+0xac>
  a7:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
  aa:   eb 1f                   jmp    cb <_FpuArctan@12+0xcb>
  ac:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  af:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
  b6:   74 04                   je     bc <_FpuArctan@12+0xbc>
  b8:   d9 18                   fstp   DWORD PTR [eax]
  ba:   eb 0f                   jmp    cb <_FpuArctan@12+0xcb>
  bc:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
  c3:   74 04                   je     c9 <_FpuArctan@12+0xc9>
  c5:   dd 18                   fstp   QWORD PTR [eax]
  c7:   eb 02                   jmp    cb <_FpuArctan@12+0xcb>
  c9:   db 38                   fstp   TBYTE PTR [eax]
  cb:   dd 65 94                frstor [ebp-0x6c]
  ce:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  d5:   74 02                   je     d9 <_FpuArctan@12+0xd9>
  d7:   dd d8                   fstp   st(0)
  d9:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  e0:   74 05                   je     e7 <_FpuArctan@12+0xe7>
  e2:   dd c7                   ffree  st(7)
  e4:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
  e7:   0c 01                   or     al,0x1
  e9:   c9                      leave
  ea:   c2 0c 00                ret    0xc

FpuArcsinh.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuArcsinh@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuArcsinh@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuArcsinh@12+0x1c>
  18:   7a 02                   jp     1c <_FpuArcsinh@12+0x1c>
  1a:   74 65                   je     81 <_FpuArcsinh@12+0x81>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 08                   je     31 <_FpuArcsinh@12+0x31>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
```

```
 2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
 2f:   eb 59                   jmp    8a <_FpuArcsinh@12+0x8a>
 31:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
 34:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
 3b:   74 04                   je     41 <_FpuArcsinh@12+0x41>
 3d:   db 28                   fld    TBYTE PTR [eax]
 3f:   eb 49                   jmp    8a <_FpuArcsinh@12+0x8a>
 41:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
 48:   74 04                   je     4e <_FpuArcsinh@12+0x4e>
 4a:   dd 00                   fld    QWORD PTR [eax]
 4c:   eb 3c                   jmp    8a <_FpuArcsinh@12+0x8a>
 4e:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
 55:   74 04                   je     5b <_FpuArcsinh@12+0x5b>
 57:   d9 00                   fld    DWORD PTR [eax]
 59:   eb 2f                   jmp    8a <_FpuArcsinh@12+0x8a>
 5b:   f7 45 10 04 00 00 00    test   DWORD PTR [ebp+0x10],0x4
 62:   74 04                   je     68 <_FpuArcsinh@12+0x68>
 64:   db 00                   fild   DWORD PTR [eax]
 66:   eb 22                   jmp    8a <_FpuArcsinh@12+0x8a>
 68:   f7 45 10 00 00 00 01    test   DWORD PTR [ebp+0x10],0x1000000
 6f:   74 04                   je     75 <_FpuArcsinh@12+0x75>
 71:   df 28                   fild   QWORD PTR [eax]
 73:   eb 15                   jmp    8a <_FpuArcsinh@12+0x8a>
 75:   f7 45 10 08 00 00 00    test   DWORD PTR [ebp+0x10],0x8
 7c:   75 09                   jne    87 <_FpuArcsinh@12+0x87>
 7e:   dd 65 94                frstor [ebp-0x6c]
 81:   33 c0                   xor    eax,eax
 83:   c9                      leave
 84:   c2 0c 00                ret    0xc
 87:   db 45 08                fild   DWORD PTR [ebp+0x8]
 8a:   d9 e4                   ftst
 8c:   9b df e0                fstsw  ax
 8f:   9b                      fwait
 90:   9e                      sahf
 91:   7a eb                   jp     7e <_FpuArcsinh@12+0x7e>
 93:   66 9c                   pushfw
 95:   d9 e1                   fabs
 97:   d9 c0                   fld    st(0)
 99:   d8 c8                   fmul   st,st(0)
 9b:   d9 e8                   fld1
 9d:   de c1                   faddp  st(1),st
 9f:   d9 fa                   fsqrt
 a1:   de c1                   faddp  st(1),st
 a3:   d9 ed                   fldln2
 a5:   d9 c9                   fxch   st(1)
 a7:   d9 f1                   fyl2x
 a9:   66 9d                   popfw
 ab:   73 02                   jae    af <_FpuArcsinh@12+0xaf>
 ad:   d9 e0                   fchs
 af:   9b df e0                fstsw  ax
 b2:   9b                      fwait
 b3:   d1 e8                   shr    eax,1
 b5:   72 c7                   jb     7e <_FpuArcsinh@12+0x7e>
 b7:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
 be:   74 05                   je     c5 <_FpuArcsinh@12+0xc5>
 c0:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
 c3:   eb 1f                   jmp    e4 <_FpuArcsinh@12+0xe4>
 c5:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
 c8:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
 cf:   74 04                   je     d5 <_FpuArcsinh@12+0xd5>
 d1:   d9 18                   fstp   DWORD PTR [eax]
 d3:   eb 0f                   jmp    e4 <_FpuArcsinh@12+0xe4>
 d5:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
 dc:   74 04                   je     e2 <_FpuArcsinh@12+0xe2>
 de:   dd 18                   fstp   QWORD PTR [eax]
 e0:   eb 02                   jmp    e4 <_FpuArcsinh@12+0xe4>
 e2:   db 38                   fstp   TBYTE PTR [eax]
 e4:   dd 65 94                frstor [ebp-0x6c]
 e7:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
 ee:   74 02                   je     f2 <_FpuArcsinh@12+0xf2>
```

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  f0:   dd d8                   fstp   st(0)
  f2:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  f9:   74 05                   je     100 <_FpuArcsinh@12+0x100>
  fb:   dd c7                   ffree  st(7)
  fd:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
 100:   0c 01                   or     al,0x1
 102:   c9                      leave
 103:   c2 0c 00                ret    0xc

FpuArcsin.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuArcsin@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuArcsin@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuArcsin@12+0x1c>
  18:   7a 02                   jp     1c <_FpuArcsin@12+0x1c>
  1a:   74 42                   je     5e <_FpuArcsin@12+0x5e>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 08                   je     31 <_FpuArcsin@12+0x31>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   eb 38                   jmp    69 <_FpuArcsin@12+0x69>
  31:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  34:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
  3b:   74 04                   je     41 <_FpuArcsin@12+0x41>
  3d:   db 28                   fld    TBYTE PTR [eax]
  3f:   eb 28                   jmp    69 <_FpuArcsin@12+0x69>
  41:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
  48:   74 04                   je     4e <_FpuArcsin@12+0x4e>
  4a:   dd 00                   fld    QWORD PTR [eax]
  4c:   eb 1b                   jmp    69 <_FpuArcsin@12+0x69>
  4e:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
  55:   74 04                   je     5b <_FpuArcsin@12+0x5b>
  57:   d9 00                   fld    DWORD PTR [eax]
  59:   eb 0e                   jmp    69 <_FpuArcsin@12+0x69>
  5b:   dd 65 94                frstor [ebp-0x6c]
  5e:   33 c0                   xor    eax,eax
  60:   c9                      leave
  61:   c2 0c 00                ret    0xc
  64:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  67:   db 28                   fld    TBYTE PTR [eax]
  69:   d9 c0                   fld    st(0)
  6b:   d8 c8                   fmul   st,st(0)
  6d:   d9 e8                   fld1
  6f:   de e1                   fsubp  st(1),st
  71:   d9 fa                   fsqrt
  73:   d9 f3                   fpatan
  75:   9b df e0                fstsw  ax
  78:   9b                      fwait
  79:   d1 e8                   shr    eax,1
  7b:   72 de                   jb     5b <_FpuArcsin@12+0x5b>
  7d:   f7 45 10 20 00 00 00    test   DWORD PTR [ebp+0x10],0x20
  84:   75 20                   jne    a6 <_FpuArcsin@12+0xa6>
  86:   68 b4 00 00 00          push   0xb4
  8b:   da 0c 24                fimul  DWORD PTR [esp]
  8e:   d9 eb                   fldpi
  90:   de f9                   fdivrp st(1),st
  92:   58                      pop    eax
  93:   d9 e4                   ftst
```

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  95:   9b df e0                fstsw  ax
  98:   9b                      fwait
  99:   9e                      sahf
  9a:   73 0a                   jae    a6 <_FpuArcsin@12+0xa6>
  9c:   68 68 01 00 00          push   0x168
  a1:   da 04 24                fiadd  DWORD PTR [esp]
  a4:   9b                      fwait
  a5:   58                      pop    eax
  a6:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  ad:   74 05                   je     b4 <_FpuArcsin@12+0xb4>
  af:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
  b2:   eb 1f                   jmp    d3 <_FpuArcsin@12+0xd3>
  b4:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  b7:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
  be:   74 04                   je     c4 <_FpuArcsin@12+0xc4>
  c0:   d9 18                   fstp   DWORD PTR [eax]
  c2:   eb 0f                   jmp    d3 <_FpuArcsin@12+0xd3>
  c4:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
  cb:   74 04                   je     d1 <_FpuArcsin@12+0xd1>
  cd:   dd 18                   fstp   QWORD PTR [eax]
  cf:   eb 02                   jmp    d3 <_FpuArcsin@12+0xd3>
  d1:   db 38                   fstp   TBYTE PTR [eax]
  d3:   dd 65 94                frstor [ebp-0x6c]
  d6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  dd:   74 02                   je     e1 <_FpuArcsin@12+0xe1>
  df:   dd d8                   fstp   st(0)
  e1:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  e8:   74 05                   je     ef <_FpuArcsin@12+0xef>
  ea:   dd c7                   ffree  st(7)
  ec:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
  ef:   0c 01                   or     al,0x1
  f1:   c9                      leave
  f2:   c2 0c 00                ret    0xc

FpuArccosh.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuArccosh@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuArccosh@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuArccosh@12+0x1c>
  18:   7a 02                   jp     1c <_FpuArccosh@12+0x1c>
  1a:   74 65                   je     81 <_FpuArccosh@12+0x81>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 08                   je     31 <_FpuArccosh@12+0x31>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   eb 59                   jmp    8a <_FpuArccosh@12+0x8a>
  31:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  34:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
  3b:   74 04                   je     41 <_FpuArccosh@12+0x41>
  3d:   db 28                   fld    TBYTE PTR [eax]
  3f:   eb 49                   jmp    8a <_FpuArccosh@12+0x8a>
  41:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
  48:   74 04                   je     4e <_FpuArccosh@12+0x4e>
  4a:   dd 00                   fld    QWORD PTR [eax]
  4c:   eb 3c                   jmp    8a <_FpuArccosh@12+0x8a>
  4e:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
  55:   74 04                   je     5b <_FpuArccosh@12+0x5b>
  57:   d9 00                   fld    DWORD PTR [eax]
```

```
  59:   eb 2f                   jmp    8a <_FpuArccosh@12+0x8a>
  5b:   f7 45 10 04 00 00 00    test   DWORD PTR [ebp+0x10],0x4
  62:   74 04                   je     68 <_FpuArccosh@12+0x68>
  64:   db 00                   fild   DWORD PTR [eax]
  66:   eb 22                   jmp    8a <_FpuArccosh@12+0x8a>
  68:   f7 45 10 00 00 00 01    test   DWORD PTR [ebp+0x10],0x1000000
  6f:   74 04                   je     75 <_FpuArccosh@12+0x75>
  71:   df 28                   fild   QWORD PTR [eax]
  73:   eb 15                   jmp    8a <_FpuArccosh@12+0x8a>
  75:   f7 45 10 08 00 00 00    test   DWORD PTR [ebp+0x10],0x8
  7c:   75 09                   jne    87 <_FpuArccosh@12+0x87>
  7e:   dd 65 94                frstor [ebp-0x6c]
  81:   33 c0                   xor    eax,eax
  83:   c9                      leave
  84:   c2 0c 00                ret    0xc
  87:   db 45 08                fild   DWORD PTR [ebp+0x8]
  8a:   d9 c0                   fld    st(0)
  8c:   d8 c8                   fmul   st,st(0)
  8e:   d9 e8                   fld1
  90:   de e9                   fsubrp st(1),st
  92:   d9 fa                   fsqrt
  94:   de c1                   faddp  st(1),st
  96:   d9 ed                   fldln2
  98:   d9 c9                   fxch   st(1)
  9a:   d9 f1                   fyl2x
  9c:   9b df e0                fstsw  ax
  9f:   9b                      fwait
  a0:   d1 e8                   shr    eax,1
  a2:   72 da                   jb     7e <_FpuArccosh@12+0x7e>
  a4:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  ab:   74 05                   je     b2 <_FpuArccosh@12+0xb2>
  ad:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
  b0:   eb 1f                   jmp    d1 <_FpuArccosh@12+0xd1>
  b2:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  b5:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
  bc:   74 04                   je     c2 <_FpuArccosh@12+0xc2>
  be:   d9 18                   fstp   DWORD PTR [eax]
  c0:   eb 0f                   jmp    d1 <_FpuArccosh@12+0xd1>
  c2:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
  c9:   74 04                   je     cf <_FpuArccosh@12+0xcf>
  cb:   dd 18                   fstp   QWORD PTR [eax]
  cd:   eb 02                   jmp    d1 <_FpuArccosh@12+0xd1>
  cf:   db 38                   fstp   TBYTE PTR [eax]
  d1:   dd 65 94                frstor [ebp-0x6c]
  d4:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  db:   74 02                   je     df <_FpuArccosh@12+0xdf>
  dd:   dd d8                   fstp   st(0)
  df:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  e6:   74 05                   je     ed <_FpuArccosh@12+0xed>
  e8:   dd c7                   ffree  st(7)
  ea:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
  ed:   0c 01                   or     al,0x1
  ef:   c9                      leave
  f0:   c2 0c 00                ret    0xc

FpuArccos.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuArccos@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuArccos@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
```

```
 16:   73 04                   jae    1c <_FpuArccos@12+0x1c>
 18:   7a 02                   jp     1c <_FpuArccos@12+0x1c>
 1a:   74 42                   je     5e <_FpuArccos@12+0x5e>
 1c:   9b dd 75 94             fsave  [ebp-0x6c]
 20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
 27:   74 08                   je     31 <_FpuArccos@12+0x31>
 29:   8d 45 94                lea    eax,[ebp-0x6c]
 2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
 2f:   eb 38                   jmp    69 <_FpuArccos@12+0x69>
 31:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
 34:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
 3b:   74 04                   je     41 <_FpuArccos@12+0x41>
 3d:   db 28                   fld    TBYTE PTR [eax]
 3f:   eb 28                   jmp    69 <_FpuArccos@12+0x69>
 41:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
 48:   74 04                   je     4e <_FpuArccos@12+0x4e>
 4a:   dd 00                   fld    QWORD PTR [eax]
 4c:   eb 1b                   jmp    69 <_FpuArccos@12+0x69>
 4e:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
 55:   74 04                   je     5b <_FpuArccos@12+0x5b>
 57:   d9 00                   fld    DWORD PTR [eax]
 59:   eb 0e                   jmp    69 <_FpuArccos@12+0x69>
 5b:   dd 65 94                frstor [ebp-0x6c]
 5e:   33 c0                   xor    eax,eax
 60:   c9                      leave
 61:   c2 0c 00                ret    0xc
 64:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
 67:   db 28                   fld    TBYTE PTR [eax]
 69:   d9 c0                   fld    st(0)
 6b:   d8 c8                   fmul   st,st(0)
 6d:   d9 e8                   fld1
 6f:   de e1                   fsubp  st(1),st
 71:   d9 fa                   fsqrt
 73:   d9 c9                   fxch   st(1)
 75:   d9 f3                   fpatan
 77:   9b df e0                fstsw  ax
 7a:   9b                      fwait
 7b:   d1 e8                   shr    eax,1
 7d:   72 dc                   jb     5b <_FpuArccos@12+0x5b>
 7f:   f7 45 10 20 00 00 00    test   DWORD PTR [ebp+0x10],0x20
 86:   75 0d                   jne    95 <_FpuArccos@12+0x95>
 88:   68 b4 00 00 00          push   0xb4
 8d:   da 0c 24                fimul  DWORD PTR [esp]
 90:   d9 eb                   fldpi
 92:   de f9                   fdivrp st(1),st
 94:   58                      pop    eax
 95:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
 9c:   74 05                   je     a3 <_FpuArccos@12+0xa3>
 9e:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
 a1:   eb 1f                   jmp    c2 <_FpuArccos@12+0xc2>
 a3:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
 a6:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
 ad:   74 04                   je     b3 <_FpuArccos@12+0xb3>
 af:   d9 18                   fstp   DWORD PTR [eax]
 b1:   eb 0f                   jmp    c2 <_FpuArccos@12+0xc2>
 b3:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
 ba:   74 04                   je     c0 <_FpuArccos@12+0xc0>
 bc:   dd 18                   fstp   QWORD PTR [eax]
 be:   eb 02                   jmp    c2 <_FpuArccos@12+0xc2>
 c0:   db 38                   fstp   TBYTE PTR [eax]
 c2:   dd 65 94                frstor [ebp-0x6c]
 c5:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
 cc:   74 02                   je     d0 <_FpuArccos@12+0xd0>
 ce:   dd d8                   fstp   st(0)
 d0:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
 d7:   74 05                   je     de <_FpuArccos@12+0xde>
 d9:   dd c7                   ffree  st(7)
 db:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
 de:   0c 01                   or     al,0x1
 e0:   c9                      leave
```

```
  e1:   c2 0c 00                ret    0xc

FpuAdd.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuAdd@16>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 14 01 01 00 00    test   DWORD PTR [ebp+0x14],0x101
   d:   74 0d                   je     1c <_FpuAdd@16+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuAdd@16+0x1c>
  18:   7a 02                   jp     1c <_FpuAdd@16+0x1c>
  1a:   74 76                   je     92 <_FpuAdd@16+0x92>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 14 01 00 00 00    test   DWORD PTR [ebp+0x14],0x1
  27:   74 0b                   je     34 <_FpuAdd@16+0x34>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   e9 80 00 00 00          jmp    b4 <_FpuAdd@16+0xb4>
  34:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  37:   f7 45 14 10 00 00 00    test   DWORD PTR [ebp+0x14],0x10
  3e:   75 58                   jne    98 <_FpuAdd@16+0x98>
  40:   f7 45 14 02 00 00 00    test   DWORD PTR [ebp+0x14],0x2
  47:   74 04                   je     4d <_FpuAdd@16+0x4d>
  49:   db 28                   fld    TBYTE PTR [eax]
  4b:   eb 67                   jmp    b4 <_FpuAdd@16+0xb4>
  4d:   f7 45 14 00 00 02 00    test   DWORD PTR [ebp+0x14],0x20000
  54:   74 04                   je     5a <_FpuAdd@16+0x5a>
  56:   dd 00                   fld    QWORD PTR [eax]
  58:   eb 5a                   jmp    b4 <_FpuAdd@16+0xb4>
  5a:   f7 45 14 00 00 01 00    test   DWORD PTR [ebp+0x14],0x10000
  61:   74 04                   je     67 <_FpuAdd@16+0x67>
  63:   d9 00                   fld    DWORD PTR [eax]
  65:   eb 4d                   jmp    b4 <_FpuAdd@16+0xb4>
  67:   f7 45 14 04 00 00 00    test   DWORD PTR [ebp+0x14],0x4
  6e:   74 04                   je     74 <_FpuAdd@16+0x74>
  70:   db 00                   fild   DWORD PTR [eax]
  72:   eb 40                   jmp    b4 <_FpuAdd@16+0xb4>
  74:   f7 45 14 00 00 00 01    test   DWORD PTR [ebp+0x14],0x1000000
  7b:   74 04                   je     81 <_FpuAdd@16+0x81>
  7d:   df 28                   fild   QWORD PTR [eax]
  7f:   eb 33                   jmp    b4 <_FpuAdd@16+0xb4>
  81:   f7 45 14 08 00 00 00    test   DWORD PTR [ebp+0x14],0x8
  88:   74 05                   je     8f <_FpuAdd@16+0x8f>
  8a:   db 45 08                fild   DWORD PTR [ebp+0x8]
  8d:   eb 25                   jmp    b4 <_FpuAdd@16+0xb4>
  8f:   dd 65 94                frstor [ebp-0x6c]
  92:   33 c0                   xor    eax,eax
  94:   c9                      leave
  95:   c2 10 00                ret    0x10
  98:   83 f8 01                cmp    eax,0x1
  9b:   75 04                   jne    a1 <_FpuAdd@16+0xa1>
  9d:   d9 eb                   fldpi
  9f:   eb 13                   jmp    b4 <_FpuAdd@16+0xb4>
  a1:   83 f8 02                cmp    eax,0x2
  a4:   75 e9                   jne    8f <_FpuAdd@16+0x8f>
  a6:   d9 e8                   fld1
  a8:   d9 ea                   fldl2e
  aa:   d8 e1                   fsub   st,st(1)
  ac:   d9 f0                   f2xm1
  ae:   d8 c1                   fadd   st,st(1)
  b0:   d9 fd                   fscale
  b2:   dd d9                   fstp   st(1)
```

```
 b4:   f7 45 14 00 01 00 00    test   DWORD PTR [ebp+0x14],0x100
 bb:   74 0b                   je     c8 <_FpuAdd@16+0xc8>
 bd:   8d 45 94                lea    eax,[ebp-0x6c]
 c0:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
 c3:   e9 80 00 00 00          jmp    148 <_FpuAdd@16+0x148>
 c8:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
 cb:   f7 45 14 00 10 00 00    test   DWORD PTR [ebp+0x14],0x1000
 d2:   75 54                   jne    128 <_FpuAdd@16+0x128>
 d4:   f7 45 14 00 02 00 00    test   DWORD PTR [ebp+0x14],0x200
 db:   74 04                   je     e1 <_FpuAdd@16+0xe1>
 dd:   db 28                   fld    TBYTE PTR [eax]
 df:   eb 67                   jmp    148 <_FpuAdd@16+0x148>
 e1:   f7 45 14 00 00 08 00    test   DWORD PTR [ebp+0x14],0x80000
 e8:   74 04                   je     ee <_FpuAdd@16+0xee>
 ea:   dd 00                   fld    QWORD PTR [eax]
 ec:   eb 5a                   jmp    148 <_FpuAdd@16+0x148>
 ee:   f7 45 14 00 00 04 00    test   DWORD PTR [ebp+0x14],0x40000
 f5:   74 04                   je     fb <_FpuAdd@16+0xfb>
 f7:   d9 00                   fld    DWORD PTR [eax]
 f9:   eb 4d                   jmp    148 <_FpuAdd@16+0x148>
 fb:   f7 45 14 00 04 00 00    test   DWORD PTR [ebp+0x14],0x400
102:   74 04                   je     108 <_FpuAdd@16+0x108>
104:   db 00                   fild   DWORD PTR [eax]
106:   eb 40                   jmp    148 <_FpuAdd@16+0x148>
108:   f7 45 14 00 00 00 02    test   DWORD PTR [ebp+0x14],0x2000000
10f:   74 04                   je     115 <_FpuAdd@16+0x115>
111:   df 28                   fild   QWORD PTR [eax]
113:   eb 33                   jmp    148 <_FpuAdd@16+0x148>
115:   f7 45 14 00 08 00 00    test   DWORD PTR [ebp+0x14],0x800
11c:   74 05                   je     123 <_FpuAdd@16+0x123>
11e:   db 45 0c                fild   DWORD PTR [ebp+0xc]
121:   eb 25                   jmp    148 <_FpuAdd@16+0x148>
123:   e9 67 ff ff ff          jmp    8f <_FpuAdd@16+0x8f>
128:   83 f8 01                cmp    eax,0x1
12b:   75 04                   jne    131 <_FpuAdd@16+0x131>
12d:   d9 eb                   fldpi
12f:   eb 17                   jmp    148 <_FpuAdd@16+0x148>
131:   83 f8 02                cmp    eax,0x2
134:   0f 85 55 ff ff ff       jne    8f <_FpuAdd@16+0x8f>
13a:   d9 e8                   fld1
13c:   d9 ea                   fldl2e
13e:   d8 e1                   fsub   st,st(1)
140:   d9 f0                   f2xm1
142:   d8 c1                   fadd   st,st(1)
144:   d9 fd                   fscale
146:   dd d9                   fstp   st(1)
148:   de c1                   faddp  st(1),st
14a:   9b df e0                fstsw  ax
14d:   9b                      fwait
14e:   d1 e8                   shr    eax,1
150:   0f 82 39 ff ff ff       jb     8f <_FpuAdd@16+0x8f>
156:   f7 45 14 80 00 00 00    test   DWORD PTR [ebp+0x14],0x80
15d:   74 05                   je     164 <_FpuAdd@16+0x164>
15f:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
162:   eb 1f                   jmp    183 <_FpuAdd@16+0x183>
164:   8b 45 10                mov    eax,DWORD PTR [ebp+0x10]
167:   f7 45 14 00 00 10 00    test   DWORD PTR [ebp+0x14],0x100000
16e:   74 04                   je     174 <_FpuAdd@16+0x174>
170:   d9 18                   fstp   DWORD PTR [eax]
172:   eb 0f                   jmp    183 <_FpuAdd@16+0x183>
174:   f7 45 14 00 00 20 00    test   DWORD PTR [ebp+0x14],0x200000
17b:   74 04                   je     181 <_FpuAdd@16+0x181>
17d:   dd 18                   fstp   QWORD PTR [eax]
17f:   eb 02                   jmp    183 <_FpuAdd@16+0x183>
181:   db 38                   fstp   TBYTE PTR [eax]
183:   dd 65 94                frstor [ebp-0x6c]
186:   f7 45 14 01 01 00 00    test   DWORD PTR [ebp+0x14],0x101
18d:   74 02                   je     191 <_FpuAdd@16+0x191>
18f:   dd d8                   fstp   st(0)
191:   f7 45 14 80 00 00 00    test   DWORD PTR [ebp+0x14],0x80
```

```
 198:   74 05                   je     19f <_FpuAdd@16+0x19f>
 19a:   dd c7                   ffree  st(7)
 19c:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
 19f:   0c 01                   or     al,0x1
 1a1:   c9                      leave
 1a2:   c2 10 00                ret    0x10

FpuAbs.obj:     file format pe-i386


Disassembly of section .text:

00000000 <_FpuAbs@12>:
   0:   55                      push   ebp
   1:   8b ec                   mov    ebp,esp
   3:   83 c4 88                add    esp,0xffffff88
   6:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
   d:   74 0d                   je     1c <_FpuAbs@12+0x1c>
   f:   d9 e5                   fxam
  11:   9b df e0                fstsw  ax
  14:   9b                      fwait
  15:   9e                      sahf
  16:   73 04                   jae    1c <_FpuAbs@12+0x1c>
  18:   7a 02                   jp     1c <_FpuAbs@12+0x1c>
  1a:   74 42                   je     5e <_FpuAbs@12+0x5e>
  1c:   9b dd 75 94             fsave  [ebp-0x6c]
  20:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  27:   74 08                   je     31 <_FpuAbs@12+0x31>
  29:   8d 45 94                lea    eax,[ebp-0x6c]
  2c:   db 68 1c                fld    TBYTE PTR [eax+0x1c]
  2f:   eb 33                   jmp    64 <_FpuAbs@12+0x64>
  31:   8b 45 08                mov    eax,DWORD PTR [ebp+0x8]
  34:   f7 45 10 02 00 00 00    test   DWORD PTR [ebp+0x10],0x2
  3b:   74 04                   je     41 <_FpuAbs@12+0x41>
  3d:   db 28                   fld    TBYTE PTR [eax]
  3f:   eb 23                   jmp    64 <_FpuAbs@12+0x64>
  41:   f7 45 10 00 00 02 00    test   DWORD PTR [ebp+0x10],0x20000
  48:   74 04                   je     4e <_FpuAbs@12+0x4e>
  4a:   dd 00                   fld    QWORD PTR [eax]
  4c:   eb 16                   jmp    64 <_FpuAbs@12+0x64>
  4e:   f7 45 10 00 00 01 00    test   DWORD PTR [ebp+0x10],0x10000
  55:   74 04                   je     5b <_FpuAbs@12+0x5b>
  57:   d9 00                   fld    DWORD PTR [eax]
  59:   eb 09                   jmp    64 <_FpuAbs@12+0x64>
  5b:   dd 65 94                frstor [ebp-0x6c]
  5e:   33 c0                   xor    eax,eax
  60:   c9                      leave
  61:   c2 0c 00                ret    0xc
  64:   d9 e1                   fabs
  66:   9b df e0                fstsw  ax
  69:   9b                      fwait
  6a:   d0 e8                   shr    al,1
  6c:   72 ed                   jb     5b <_FpuAbs@12+0x5b>
  6e:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  75:   74 05                   je     7c <_FpuAbs@12+0x7c>
  77:   db 7d 8a                fstp   TBYTE PTR [ebp-0x76]
  7a:   eb 1f                   jmp    9b <_FpuAbs@12+0x9b>
  7c:   8b 45 0c                mov    eax,DWORD PTR [ebp+0xc]
  7f:   f7 45 10 00 00 10 00    test   DWORD PTR [ebp+0x10],0x100000
  86:   74 04                   je     8c <_FpuAbs@12+0x8c>
  88:   d9 18                   fstp   DWORD PTR [eax]
  8a:   eb 0f                   jmp    9b <_FpuAbs@12+0x9b>
  8c:   f7 45 10 00 00 20 00    test   DWORD PTR [ebp+0x10],0x200000
  93:   74 04                   je     99 <_FpuAbs@12+0x99>
  95:   dd 18                   fstp   QWORD PTR [eax]
  97:   eb 02                   jmp    9b <_FpuAbs@12+0x9b>
  99:   db 38                   fstp   TBYTE PTR [eax]
  9b:   dd 65 94                frstor [ebp-0x6c]
  9e:   f7 45 10 01 00 00 00    test   DWORD PTR [ebp+0x10],0x1
  a5:   74 02                   je     a9 <_FpuAbs@12+0xa9>
```

```
  a7:   dd d8                   fstp   st(0)
  a9:   f7 45 10 80 00 00 00    test   DWORD PTR [ebp+0x10],0x80
  b0:   74 05                   je     b7 <_FpuAbs@12+0xb7>
  b2:   dd c7                   ffree  st(7)
  b4:   db 6d 8a                fld    TBYTE PTR [ebp-0x76]
  b7:   0c 01                   or     al,0x1
  b9:   c9                      leave
  ba:   c2 0c 00                ret    0xc
```