ELEC 422/527: VLSI Systems Design

Project Checklist as if for MOSIS

Spring 2024, Saturday April 6, 2024

Group project work.

Due: Tuesday, April 30, 2024, at 11:59pm on Canvas.

Please enter Group Topic: Minesweeper Game

Team Members: Agha Sukerim, Alexis Le Glaunec, Liam Waite

Please Complete and Upload this Final Project Design Checklist in the "Project Design" Group Assignment on Canvas

- ☑ ~~*Please upload all of your Verilog files and testbench files. Also please upload your compile scripts for Design Compiler and Innovus. Upload these in one .zip file.*~~

- ☑ ~~*Verify no design rule errors in your design when viewed in the magic layout editor.*~~

- ☑ ~~*Please make sure that you have added the necessary fill to the poly (15%), metal1 (30%), and metal2 (30%) layers in magic and have verified.*~~

- ☑ ~~*Please upload your final Project Design File in GDS and also CIF format.*~~

- ☑ ~~*Please pick a project name about 8 characters.* ***Enter here:***~~

  Minesweep

- ☑ ~~*Please enter a 100 word abstract of your project function.* ***Enter here:***~~

  Our project is a VLSI chip implementation of the traditional Minesweeper computer puzzle game. At start, up to three hidden mines are pseudo-randomly placed on a 5x5 grid. The goal of the user is to choose (i.e. "clear") all of the cells where the mines are not. In each round, the user picks a cell. If a mine was placed at the chosen cell, the player has lost and the game restarts. If a mine is not there, the design returns the number of mines directly adjacent to the chosen

cell and a 1-dimensional mapping of all of the cells the user has cleared so far. If the player has “cleared” every cell on the grid except for the mine-placed cells, the user wins and the global score increments.

☑ ~~*Please upload a text file listing I/O pin and signal direction (input/output/bi-directional) and signal name, and also a screenshot of your chip layout and label the I/O pins with the signal names.*~~

File titled pin_direction.txt

☑ ~~*Please make sure that you have tested your design from the I/O pads with Irsim where the pads are labeled as "p_xxx" to verify functionality. Please upload your .sim netlist.*~~

☑ ~~*Please upload an Irsim command file to test the design and a text file describing the test function and a screen shot of the expected results. (This can be duplicated from the project report, but it helps to have it here for test verification.)*~~

☑ ~~*Please include a statement indicating if the project was a fair 25/25/25/25 or 33/33/33 division of work, that is each team member contributed equally. If any team member feels that the workload was unbalanced by a significant amount, indicate that here and also send a personal email to the instructor, so that we can discuss how this will affect a fair grade for each team member.* ***Enter statement here if balanced or unbalanced:***~~

The work for this project was distributed as equally as we saw fit throughout the development of our design. Alexis: 42%

☑ ~~*Please upload* ***this completed checklist*** *to indicate the completion of each of these items.*~~