Ahmed Z. Ghonem

Senior Neuromorphic Computing Engineer

Senior Engineer with 7+ years of experience leading the design and implementation of cutting-edge neuromorphic processors, AI-accelerated SoCs, and low-power digital systems. Proven track record of driving innovation from architecture to GDSII, optimizing PPA, and delivering high-impact solutions for commercial applications. Adept at leading cross-functional teams, managing complex projects, and aligning technical development with business goals.

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EDUCATION

Master of Business Administration
University of Illinois Urbana-Champaign

M.Sc. in Electrical & Computer Engineering
The Ohio State University

PROFESSIONAL EXPERIENCE

Senior SoC Design Engineer
NVIDIA

01/2024 - Present — *Santa Clara, CA, USA*

Achievements/Tasks

- Spearheaded RUBIN GPU Emulation setup, automating workflows and reducing engineering effort by 60%, accelerating development cycles.
- Designed and deployed a top-level connectivity linting tool (Python) used across 10+ teams, boosting debugging efficiency by 3x**.**
- Developed an automated dielet-dielet connectivity framework for multi-chip designs, streamlining DFX verification and reducing design cycles by 50%.
- Led execution of SOCD-FCV-EMU flow, collaborating with global cross-functional teams to drive seamless implementation across multiple time zones.

Graduate Research Associate
Electroscience Lab - The Ohio State University

09/2021 - 12/2023 — *Columbus, OH, USA*

Achievements/Tasks

- Developed a 512-Neuron 256K-Synapses Digital Neuromorphic Processor with On-Chip Encoding for efficient inference on the edge.
- Implemented algorithmic modeling in Python and hardware design in SystemVerilog, taking the design from RTL to GDSII in GF22nm technology.
- Designed and verified an SPI-based programming interface for an eFPGA and integrated it within a large SoC through an SPI-TileLink bridge.
- Built the entire Digital Physical Design flow infrastructure for GF22nm (i.e., Synthesis, APR scripts, physical verification (DRC, LVS and DFM)).
- Led the physical design of an SoC with RISC-V processors, TileLink Bus, eFPGA, and security engines, optimizing PPA through a bottom-up approach.
- Created a custom package and evaluation board for the SoC, enabling the chip to achieve a speed of 650MHz and streamlining post-silicon validation.
- Established the silicon bring-up setup using testing FPGAs, a logic analyzer, and an oscilloscope, improving test efficiency and accuracy.

Co-Founder / Head of HW Engineering
Embedded A.I. Systems

12/2019 - 05/2022 — *Singapore*

Achievements/Tasks

- Led the architecture and development of three > 1W hardware-accelerated AI chips featuring SoTA NVMe (MRAMs, RRAMs), DL accelerators, and RISC-V processors for edge applications, managing the entire design and prototyping lifecycle from concept to functional prototype.
- Defined and developed the company's business strategy, including the business model canvas and revenue model, aligning product roadmaps with market and investor needs.
- Collaborated with co-founders to prepare investor due diligence, building pitch decks, financial models, technical documentation, and optimizing company operations to streamline fundraising efforts.

PROFESSIONAL EXPERIENCE

Senior ASIC/SoC Design Engineer
A*STAR

10/2020 - 09/2021 *Singapore*

Achievements/Tasks

- Led the design and verification of an SoC based on TSMC22ULL technology. The SoC, ECSDoT, surpassed state-of-the-art energy efficiency for AI workloads, featuring a RISC-V processor, high-performance DL/AI accelerator, on/off-chip communication (JTAG, UART, uDMA), and more.
- Integrated and verified a Deep Learning Accelerator (NVDLA) through an AXI4 interface into a RISCV-based SoC improving processing of DL workloads.
- Developed an FPGA-RaspberryPi wearable demo, emulating the SoC and showcasing activity recognition as a practical use case.

AI Hardware Acceleration Engineer
Nanyang Technological University (NTU)

03/2019 - 10/2020 *Singapore*

Achievements/Tasks

- Spearheaded the design, verification, and physical implementation of the ECS- α, SoC using UMC40ULP technology, incorporating a 32-bit RISC-V core, inhouse designed ReRAM controller, 4Mb ReRAM**,** and an energy-efficient convolution engine (ML Accelerator).
- Led the design, verification, and testing of an SoC on TSMC22ULL technology. The SoC, ECS- 1, featured a RISC-V processor, an MRAM controller, 16Mb MRAM**,** and in-house developed energy-efficient 8-bit neural processing engine (ML Accelerator).
- Designed a custom SRAM readout circuit with thin-film transistors, for flexible electronics applications.

SoC Methodology Engineer
Suitera LLC

07/2018 - 03/2019 *Cairo, Egypt*

Achievements/Tasks

- Developed the first version of Model Order Reduction (MOR) tool using C++ and MATLAB delivered to Mentor Graphics, Siemens.
- Provided algorithmic advancement for MOR and EDA software tools for faster and more accurate IP and SOC development and modeling.
- Led a knowledge exchange session at Helic, SA (Greece), where the MOR tool was validated against SoTA netlists.

Device Modelling Engineer
ONE Lab

01/2017 - 06/2018 *Cairo, Egypt*

Achievements/Tasks

- Developed the first compact model using Verliog-A for Triboelectronic Nanogenerators (TENGs) energy harvesters.
- Formulated and validated two novel TENG modes, providing all of the analytical FEM modeling, mathematical modeling, and compact modeling.
- Designed a full energy harvesting circuit using Verilog-A modeling and a custom AC-DC circuit for low-power applications on TSMC65nm.

TECHNICAL SKILLS

Analytical	Deep understanding of low-power design across the stack from architecture, RTL, synthesis, PPA, to IP and hierarchical PnR.
ASIC - Flow Tools	Cadence (Xceluim, Genus, Innovus, Tempus, voltus), Synopsys (VCS and DC, ICC II), Vivado and QuestaSim.
IC Design Tools	Cadence Virtuoso, Mentor IC-Station, layout editor, x-Layout, DRC, LVS, PEX, and post-layout simulation and verification.
Languages	Verilog, SystemVeilog, Python (NNs, PyTorch), Matlab, C++, Verilog-A, Latex, TCL, PERL and bash scripting.

DOMAIN INTERESTS

Hardware Acceleration for AI/DL | Neuromorphic Computing | Secure Hardware Architectures | Low-Power SoC Design

PUBLICATIONS

IEEE TCAS-I

State-of-the-Art ASCON ASIC Achieving 4.3 Gbps@0.8V and 3.5Tb/J@0.6V Outperforming AES By 25 Times

2025

IEEE ISCAS 2024

ASIC Implementation of Efficient 512-Neuron 256K-Synapses Digital Neuromorphic Processor with On-Chip Encoding in 22nmFDX

2024

PUBLICATIONS

IEEE NEWCAS 2024
Towards Efficient and Reconfigurable Neuromorphic Computing Using an Embedded FPGA in 22nmFDX
2024

IEEE MWSCAS 2024
Dynamic Security Management of Systems on Chip via Embedded FPGA in 22nm CMOS Technology
2024

IEEE International Computer Engineering Conference
Ultra Low-Power Encryption/Decryption Core for Lightwieght IoT Applications
2019

Journal of Low Power Electronics
Complete study for diagonal Triboelectric Nanogenerators based energy harvester with computer aided design tool
2019

IEEE MWSCAS 2018 Conference
In-Out Cylindrical Triboelectric Nanogenerators Based Energy Harvester
2018

IEEE MWSCAS 2017 Conference
Characterization and model validation of triboelectric nanogenerators using Verilog-A
2017

Design, Automation and Test in Europe (DATE) Conference
Fledge: Flexible edge platforms enabled byin-memory computing
2020

Design, Automation and Test in Europe (DATE) Conference
Quantifying the benefits of Monolithic 3D Computing Systems Enabled by TFT and RRAM
2020

ACHIEVEMENTS

Al-Amal Graduate Student Award (AGSA) (08/2024 - Present)
Founder of Al-Amal (i.e., Hope) Graduate Student Award. The award is dedicated to help incoming graduate students throughout their application journey.

Zewailcity Outstanding Student Scholarship (2013)
I was awarded a full scholarship for my BSc studies granted for outstanding students in recognition of my ranking 5th out of ~27,000 students nationwide in high school.

Microelectronics Olympiad - USA (06/2023)
First place in the USA chapter of Synopsys microelectronics Olympiad.

Zewailcity Research Excellence Award (2018)
A prestigious award given for outstanding research efforts during undergraduate studies.

IEEE HOST Microelectronics Challenge (06/2022)
Placing first in the SoC security challenge.

MEMS Design Contest - Semi finalist (02/2017 - 01/2018)
Chosen as semi-finalist in" MEMS Design Contest" held by Cadence. XFAB and Coventor.

Founder of Nanotechnology Club - ZC (2016 - 2018)
Educating new students on the major and the market trends in the industry.

Best poster award (2015 - 2016)
First place out of 50 posters exhibiting research and scientific work at ZC 1st (2015) and 2nd (2016) undergraduate research conference.