# User Manual

for S32 PORT Driver

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# Chapter 1

# **Revision History**

Revision	Date	Author	Description
1.0	31.10.2022	NXP RTD Team	Prepared for release S32 RTD AUTOSAR 4.4 Version 4.0.0 Release

# **Chapter 2**

### Introduction

- Supported Derivatives
- Overview
- About This Manual
- Acronyms and Definitions
- Reference List

This User Manual describes NXP Semiconductor AUTOSAR Port for S32. AUTOSAR Port driver configuration parameters and deviations from the specification are described in Driver chapter of this document. AUTOSAR Port driver requirements and APIs are described in the AUTOSAR Port driver software specification document.

# 2.1 Supported Derivatives

The software described in this document is intended to be used with the following microcontroller devices of NXP Semiconductors:

- s32g274a bga525
- s32g254a\_bga525
- s32g233a\_bga525
- s32g234m\_bga525
- s32g378a\_bga525
- s32g379a\_bga525
- s32g398a\_bga525
- $s32g399a\_bga525$
- s32g338m\_bga525
- $s32g339m\_bga525$
- s32g358a\_bga525
- $s32g359a\_bga525$
- s32r45\_bga780

All of the above microcontroller devices are collectively named as S32.

#### Introduction

#### 2.2 Overview

AUTOSAR (AUTomotive Open System ARchitecture) is an industry partnership working to establish standards for software interfaces and software modules for automobile electronic control systems.

#### AUTOSAR:

- paves the way for innovative electronic systems that further improve performance, safety and environmental friendliness.
- is a strong global partnership that creates one common standard: "Cooperate on standards, compete on implementation".
- is a key enabling technology to manage the growing electrics/electronics complexity. It aims to be prepared for the upcoming technologies and to improve cost-efficiency without making any compromise with respect to quality.
- facilitates the exchange and update of software and hardware over the service life of the vehicle.

#### 2.3 About This Manual

This Technical Reference employs the following typographical conventions:

- Boldface style: Used for important terms, notes and warnings.
- *Italic* style: Used for code snippets in the text. Note that C language modifiers such "const" or "volatile" are sometimes omitted to improve readability of the presented code.

Notes and warnings are shown as below:

Note

This is a note.

Warning

This is a warning

# 2.4 Acronyms and Definitions

Term	Definition	
API	Application Programming Interface	
ASM	Assembler	
BSMI	Basic Software Make file Interface	
CAN	Controller Area Network	
C/CPP	C and C++ Source Code	
CS	Chip Select	
CTU	Cross Trigger Unit	
DEM	Diagnostic Event Manager	
DET	Development Error Tracer	
DMA	Direct Memory Access	
ECU	Electronic Control Unit	
FIFO	First In First Out	
LSB	Least Signifigant Bit	
MCU	Micro Controller Unit	
MIDE	Multi Integrated Development Environment	
MSB	Most Significant Bit	
N/A	Not Applicable	
RAM	Random Access Memory	
SIU	Systems Integration Unit	
SWS	Software Specification	
VLE	Variable Length Encoding	
XML	Extensible Markup Language	

# 2.5 Reference List

#	Title	Version
1	Specification of Port Driver	AUTOSAR Release 4.4.0
		S32G2 Reference Manual, Rev 5, May 2022
2	Reference Manual	S32G3 Reference Manual, Rev.2 Draft C, June 2022
		S32R45 Reference Manual, Rev. 3, 12/2021
3	Datasheet	S32G2 Data Sheet, Rev 5, May 2022
		S32G3 Data Sheet, Rev 2, Draft B, June 2022
		VR5510 Data Sheet, Rev 5, April 2022
		S32R45 Data Sheet, Rev. 2 — 12/2021
4	Errata	S32G2: Mask Set Errata for Mask 0P77B, Rev. 2.4
		S32G3: Mask Set Errata for Mask 0P72B, Rev. 1.1
		S32R45: Mask Set Errata for Mask P57D, Rev. 2.0

# **Chapter 3**

# **Driver**

- Requirements
- Driver Design Summary
- Hardware Resources
- Deviations from Requirements
- Driver Limitations
- Driver usage and configuration tips
- Runtime errors
- Symbolic Names Disclaimer

# 3.1 Requirements

Requirements for this driver are detailed in the Autosar Driver Software Specification document (See Table Reference List ).

# 3.2 Driver Design Summary

This module provides the service for initializing the whole PORT structure of the microcontroller. Many ports and port pins can be assigned to various functionalities, e.g.

- General purpose I/O
- ADC
- $\bullet$  SPI
- SCI
- PWM
- CAN

- LIN
- etc

For this reason, there is an overall configuration and initialization of this port structure. The configuration and mode of these port pins is microcontroller and ECU dependent.

Port initialisation data are written to each port as efficiently as possible. This PORT driver module completes the overall configuration and initialisation of the port structure which is used in the DIO driver module. Therefore, the DIO driver works on pins and ports which are configured by the PORT driver.

The PORT driver is initialised prior to use of the DIO functions. Otherwise DIO functions will exhibit undefined behaviour.

#### 3.3 Hardware Resources

The hardware configured by the Port driver is SIUL2.

Every PortPin configured in a PortContainer of the Port plugin can be mapped to one and only one microcontroller pin. The following steps must be followed in order to correctly map a Port plugin pin over a specific microcontroller pin:

#### For S32G2

- 1. Open the S32G2 IOMUX Excel file attached to the Reference Manual
- 2. Go to 'IO Signal Table' sheet
- 3. Identify the microcontroller pin you want to use (eg. PB[3]), searching after the values in columns 'Module' and 'Function'. Scroll to the Excel row where the pin's name appear first in column 'Port'. On the column 'CR' there is a number which represents the numeric value of the Multiplexed Signal Configuration Register. Note down this number (eg. 19)
- 4. Go to port container inside the Port plugin where you want to add the pin
- 5. Add a new PortPin in the port container list then double click the newly added PortPin to open it's properties
- 6. Go to the 'PortPin Mscr' attribute and type the number noted down at step 3
- 7. Go to the 'PortPin SIUL2 Instance' attribute and choose the instance for the selected pin
- 8. Go to the 'PortPin Mode' attribute and choose the functionality you want to use for the selected pin

#### For S32G3

- 1. Open the S32G3 IOMUX Excel file attached to the Reference Manual
- 2. Go to 'IO Signal Table' sheet
- 3. Identify the microcontroller pin you want to use (eg. PB[3]), searching after the values in columns 'Module' and 'Function'. Scroll to the Excel row where the pin's name appear first in column 'Port'. On the column 'CR' there is a number which represents the numeric value of the Multiplexed Signal Configuration Register. Note down this number (eg. 19)

#### Driver

- 4. Go to port container inside the Port plugin where you want to add the pin
- 5. Add a new PortPin in the port container list then double click the newly added PortPin to open it's properties
- 6. Go to the 'PortPin Mscr' attribute and type the number noted down at step 3
- 7. Go to the 'PortPin SIUL2 Instance' attribute and choose the instance for the selected pin
- 8. Go to the 'PortPin Mode' attribute and choose the functionality you want to use for the selected pin

#### For S32R45

- 1. Open the S32R45 IOMUX Excel file attached to the Reference Manual
- 2. Go to 'IO Signal Table' sheet
- 3. Identify the microcontroller pin you want to use (eg. PB[3]), searching after the values in columns 'Module' and 'Function'. Scroll to the Excel row where the pin's name appear first in column 'Port'. On the column 'CR' there is a number which represents the numeric value of the Multiplexed Signal Configuration Register. Note down this number (eg. 19)
- 4. Go to port container inside the Port plugin where you want to add the pin
- 5. Add a new PortPin in the port container list then double click the newly added PortPin to open it's properties
- 6. Go to the 'PortPin Mscr' attribute and type the number noted down at step 3
- 7. Go to the 'PortPin SIUL2 Instance' attribute and choose the instance for the selected pin
- 8. Go to the 'PortPin Mode' attribute and choose the functionality you want to use for the selected pin

# 3.4 Deviations from Requirements

The driver deviates from the AUTOSAR Port Driver software specification in some places. The table identifies the AUTOSAR requirements that are not fully implemented, not implemented or out of scope for the Port Driver.

Term	Definition	
N/S	Out of scope	
N/I	Not implemented	
N/F	Not fully implemented	

Below table identifies the AUTOSAR requirements that are not fully implemented, not implemented or out of scope for the driver.

Requirement	Status	Description	Notes
SWS_Port_00220	N/S	The type Port_PinDirectionType shall be of enumeration type having range as PORT_PIN_IN and PORT_PIN← _OUT.	The type Port_PinDirectionType shall be of enumeration type having range as PORT_PIN_IN, PORT ←PIN_OUT and PORT_PIN_ ← INOUT.
SWS_Port_00227	N/S	These requirements are not applicable to this specification. (SRS← BSW_00005, SRS_BSW_00006, SRS_BSW_00006, SRS_BSW_00007, SRS_BSW_00101, SRS_BSW_00160, SRS_BSW_00161, SRS_BSW_00162, SRS_BSW_00164, SRS_BSW_00164, SRS_BSW_00167, SRS_BSW_00164, SRS_BSW_00167, SRS_BSW_00168, SRS_BSW_00170, SRS_BSW_00172, SRS_BSW_00307, SRS_BSW_00308, SRS_BSW_00309, SRS← BSW_00321, SRS_BSW_00325, SRS_BSW_00321, SRS_BSW_00331, SRS← BSW_00333, SRS_BSW_00331, SRS_BSW_00333, SRS_BSW_00334, SRS_BSW_00335, SRS_BSW_00341, SRS_BSW_00342, SRS_BSW_00341, SRS_BSW_00342, SRS_BSW_00344, SRS_BSW_00344, SRS_BSW_00347, SRS_BSW_00357, SRS← BSW_00359, SRS_BSW_00360, SRS_SPAL_12463, SRS_SPAL_← 12462, SRS_SPAL_12265, SRS← SPAL_12067, SRS_SPAL_12064, SRS_SPAL_12067, SRS_SPAL_12064, SRS_SPAL_12067, SRS_SPAL_12064, SRS_SPAL_12069, SRS_SPAL_12068, SRS_SPAL_12069, SRS_SPAL_12068, SRS_SPAL_12267, SRS_SPAL_61266, SRS_SPAL_12267, SRS_SPAL_61266, SRS_SPAL_12267, SRS_SPAL_61266, SRS_SPAL_12267, SRS_SPAL_612056, SRS_BSW_00440, SRS← SPAL_12267, SRS_BSW_00437, SRS_BSW_00439, SRS_BSW_00447, SRS_BSW_00439, SRS_BSW_004427, SRS_BSW_00428, SRS_BSW_00427, SRS_BSW_00428, SRS_BSW_004419, SRS_BSW_004417, SRS_BSW_004413, SRS← BSW_004416, SRS_BSW_004417, SRS_BSW_004413, SRS← BSW_004416, SRS_BSW_004417, SRS_BSW_004413, SRS← BSW_00375, SRS_BSW_00375, SRS_BSW_00377, SRS_BSW_00371)	This is not a requirement

#### Driver

Requirement	Status	Description	Notes
ECUC_Port_00128	N/S	"Name - PortPinInitialMode - Par-	Currently implemented in a difffer-
		ent Container - PortPin - Descrip-	ent mode in MCAL 4.3.0. This re-
		tion - Port pin mode from mode	quirement was replaced by require-
		list for use with Port_Init() func-	ment ECUC_Port_00130.
		tion Multiplicity - 1 - Type -	
		EcucEnumerationParamDef - Range	
		- PORT_PIN_MODE_ADC - Port	
		Pin used by ADC - PORT_PIN↔	
		_MODE_CAN - Port Pin used for	
		CAN - PORT_PIN_MODE_DIO -	
		Port Pin configured for DIO. It shall	
		be used under control of the DIO	
		driver PORT_PIN_MODE_←	
		DIO_GPT - Port Pin configured for	
		DIO. It shall be used under con-	
		trol of the general purpose timer	
		driver PORT_PIN_MODE_←	
		DIO_WDG - Port Pin configured	
		for DIO. It shall be used under	
		control of the watchdog driver	
		PORT_PIN_MODE_FLEXRAY -	
		Port Pin used for FlexRay - PORT←	
		_PIN_MODE_ICU - Port Pin used	
		by ICU - PORT_PIN_MODE_LIN	
		- Port Pin used for LIN - PORT_←	
		PIN_MODE_MEM - Port Pin used	
		for external memory under control of	
		a memory driver PORT_PIN↔	
		_MODE_PWM - Port Pin used by	
		PWM - PORT_PIN_MODE_SPI -	
		Port Pin used by SPI - Post-Build	
		Variant Value - true - Value Config-	
		uration Class - Pre-compile time - X - VARIANT-PRE-COMPILE - Link	
		time Post-build time - X -	
		VARIANT-POST-BUILD - Scope /	
		- ,	
		Dependency - scope: local - "	

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Requirement	Status	Description	Notes
CPR_RTD_00544.port	N/S	"Name - PortPinMode - Parent Container - PortPin - Description - Port pin mode from mode list. Note that more than one mode is allowed by default. That way it is e.g. possible to combine DIO with another mode such as ICU Multiplicity - 1* - Type - EcucEnumerationParamDef - Range - PORT_PIN_MODE_ADC - Port Pin used by ADC - PORT_\(-\text{PIN_MODE_CAN}\) - Port Pin used for CAN - PORT_PIN_MODE_\(-\text{PIN_MODE_CAN}\) - PORT_PIN_\(-\text{MODE_DIO_GPT}\) - Port Pin configured for DIO. It shall be used under control of the DIO driver PORT_PIN_\(-\text{MODE_DIO_GPT}\) - Port Pin configured for DIO. It shall be used under control of the general purpose timer driver PORT_PIN_\(-\text{MODE_DIO_WDG}\) - PORT_PIN_\(-\text{MODE_DIO_WDG}\) - PORT_PIN_\(-\text{MODE_IOIO_WDG}\) - PORT_PIN_\(-\text{MODE_FLEXRAY}\) - PORT_PIN_\(-\text{MODE_FLEXRAY}\) - PORT_PIN_\(-\text{MODE_ICU}\) - PORT_PIN_\(-\text{MODE_ICU}\) - PORT_PIN_\(-\text{MODE_IUN}\) - PORT_\(-\text{PIN_MODE_ICU}\) - PORT_\(-\text{PIN_MODE_LIN}\) - PORT_\(-\text{PIN_MODE_MEM}\) - PORT_\(-\text{PIN_MODE_MEM}\) - PORT_\(-\text{PIN_MODE_SPI}\) - Post-Build Variant Multiplicity - true - Post-\(-\text{PIN_BUILD}\) - Value Configuration Class - Precompile time - X - VARIANT-\(-\text{PRE-COMPILE}\) - Link time - \(-\text{POST-BUILD}\) - Value Configuration Class - Precompile time - X - VARIANT-\(-\text{POST-BUILD}\) - Scope / Dependency - scope: local - "	Replaced by requirement CPR_← RTD_00372.port
OF K_K1D_00344.port	11/5	dard configuration format for the IP layer. Note: EPD file for the IP shall be provided.	release by default is not supporting cross configuration. ARTD-15712 was raised to implement this feature but it was postponed until we have the support from S32CT teams.

#### Driver

As a deviation from standard:

Port\_PBcfg\_VariantNo.c files will contain the definition for all parameters that are variant aware, independent of the configuration class that will be selected (PC, LT, PB).

Port Cfg.c file will contain the definition for all parameters that are not variant aware.

#### 3.5 Driver Limitations

- Pins Tool should be disabled when Port component is used.
- Siul2 Port should be disabled when Port component is used.
- VSMD reports for PORT have some errors: due to ECUC\_PORT\_00130 requirement is no longer apply on RTD product (AAI-192).

### 3.6 Driver usage and configuration tips

The Port driver is responsible with configuring the functionality that should be active on a platform hardware pin. The information about the functionalities available on each of the hardware pins of the platform can be found in the S32 IO Muxing table Excel file attached to the Reference Manual pdf. Note when configuring the pins: The user can set the pin sequentially to be able to read the result correctly (for this the user can use a semaphore written by core 0 and read by core 1).

The Port plugin allows the user to configure each pin's functionality using 3 distinct mechanisms:

- A. Define the functionality of a specific pin. This can be done by adding a new entry in the PortContainer/← PortPin list and setting the attributes of the pin. The following steps should be followed:
  - 1. Go to PortEcucPartitionRef container inside the Port plugin where you want to add a new partition
  - 2. Open the IOSignal description Excel file
  - 3. Go to 'IO Signal Table' sheet
  - 4. Identify the microcontroller pin you want to use (eg. PB[3]), searching after the values in columns 'Module' and 'Function'. Scroll to the Excel row where the pin's name appear first in column 'Port'. On the column 'CR' there is a number which represents the numeric value of the Multiplexed Signal Configuration Register. Note down this number (eg. 19)
  - 5. Go to port container inside the Port plugin where you want to add the pin
  - 6. Add a new PortPin in the port container list then double click the newly added PortPin to open it's properties
  - 7. Go to the 'PortPin Mscr' attribute and type the number noted down at step A.4
  - 8. Go to the 'PortPin Mode' attribute and choose the functionality you want to use for the selected pin
  - 9. Look at the other attributes of the PortPin and set them to the desired values
  - 10. Go to PortPinEcucPartitionRef container inside the PortPin where you want to add a new partition
- B. Define pins that should not be touched by any Port driver functionality, including Port\_Init() function. This option allows the user to configure a list of pins for which the driver will not touch their MSCRs, leaving them containing the reset values. This list is named UnTouchedPortPin and is available in the PortConfigSet container and adding new entries in this list should follow the next steps:

- 1. Open the IOSignal description Excel file
- 2. Go to 'IO Signal Table' sheet
- 3. Identify the microcontroller pin you want the Port driver to not touch (eg. PB[3]), searching after the values in columns 'Module' and 'Function'. Scroll to the Excel row where the pin's name appear first in column 'Port'. On the column 'CR' there is a number which represents the numeric value of the Multiplexed Signal Configuration Register. Note down this number (eg. 19)
- 4. Go to UnTouchedPortPin list inside the PortConfigSet container
- 5. Add a new entry in the list and double click it to open it's properties
- 6. Go to the 'PortPin Mscr' attribute and type the number noted down at step A.3
- 7. Go to the 'PortPin Siu2 Instance' attribute and select the SIUL2 instance the pin belongs to
- C. Define the settings for all platform hardware pins that were not configured using mechanism described at point A and point B. This option allows the user to configure all platform pins that are not explicitly configured by the user (point A) or not left untouched (point B) as GPIOs, with some specific settings. These settings are available in the container NotUsedPortPin where the user can define the pin direction (in or out), pin level (high or low), pull up/down.

Every single platform hardware pin is configured by the Port driver, either by mechanism A, mechanism B or mechanism C.

For this reason, if the platform contains hardware pins that need to have certain non GPIO functionalities, these pins must be explicitly added in the Port configuration using mechanism A or B. Otherwise, they will be configured by Port\_Init() API as GPIOs.

#### Important note

In order to be able to use the debug capabilities, the JTAG pins need to be configured in the Port driver using mechanism B. This means that the following pins/functionalities need to be added in the UnTouchedPortPin list:

- JTAG TDI having PortPin Mscr set to 0 and SIUL2 Instance set to SIUL2 0
- JTAG\_TDO having PortPin Mscr set to 1 and SIUL2 Instance set to SIUL2\_0
- JTAG TCK having PortPin Mscr set to 4 and SIUL2 Instance set to SIUL2 0
- JTAG\_TMS having PortPin Mscr set to 5 and SIUL2 Instance set to SIUL2\_0

The Jtag pins can be automatically added in the Port driver configuration if when adding Port plugin in the Tresos project, the user selects the Default recommended configuration as: PortRecConfiguration\_JtagPins.

#### Driver

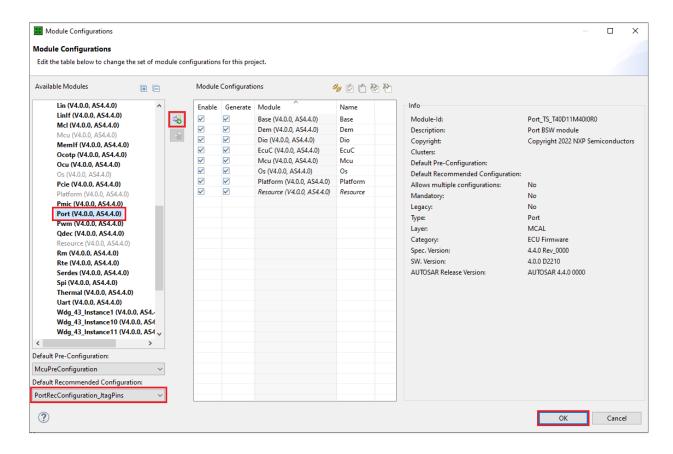


Figure 3.1 How to configure JTAG pins

#### Autosar extension functionality

- Support to run driver's code from User Mode. This option is configurable on/off per entire driver, using the checkbox 'Enable Port User Mode Support' in PortGeneral container. When this parameter is enabled, the Port module will adapt to run from user mode so that the registers under protection can be accessed from user mode. For more information, please see the IM chapter 'User Mode Support'.
- Port SetPinMode Does Not Touch GPIO Levels. This option is configurable on/off and it affects the functionality of the Port\_SetPinMode() API. When not checked, the function Port\_SetPinMode() will set the output level of the pin to the value configured in the PortPinLevelValue combo when called at run time to change mode of a pin from alternate function to GPIO. When checked, the function Port\_SetPinMode() will not touch the output level of the pin when called at run time to change mode of a pin from alternate function to GPIO.

#### 3.7 Runtime errors

This driver doesn't generate any runtime error.

# 3.8 Symbolic Names Disclaimer

All containers having symbolicNameValue set to TRUE in the AUTOSAR schema will generate defines like:

```
#define <Mip>Conf_<Container_ShortName>_<Container_ID>
```

For this reason it is forbidden to duplicate the names of such containers across the RTD configurations or to use names that may trigger other compile issues (e.g. match existing #ifdefs arguments).

# **Chapter 4**

# **Tresos Configuration Plug-in**

This chapter describes the Tresos configuration plug-in for the driver. All the parameters are described below.

- Module Port
  - Container PortConfigSet
    - \* Container NotUsedPortPin
      - · Parameter PortPinPue
      - · Parameter PortPinPus
      - · Parameter PortPinDirection
      - · Parameter PortPinLevelValue
    - \* Container PortContainer
      - · Parameter PortNumberOfPortPins
      - · Container PortPin
      - · Parameter PortPinPue
      - · Parameter PortPinPus
      - · Parameter PortPinSafeMode
      - · Parameter PortPinOde
      - · Parameter PortPinWithReadBack
      - · Parameter PortPinRcvr
      - $\cdot \ \ Parameter \ PortPinDirectionChangeable$
      - · Parameter PortPinModeChangeable
      - $\cdot \ \ Parameter \ PortPinSiul2Instance$
      - · Parameter PortPinId
      - · Parameter PortPinPcr
      - · Parameter PortPinDirection
      - · Parameter PortPinInitialMode
      - · Parameter PortPinMode
      - · Parameter PortPinLevelValue
      - · Parameter PortPinSlewRate
      - · Reference PortPinEcucPartitionRef
    - \* Container UnTouchedPortPin
      - · Parameter PortPinSiul2Instance
      - · Parameter PortPinPcr

- \* Container UntouchedIMCR
  - · Parameter IMCRSiul2Instance
  - · Parameter UntouchedPortPinImcr
- Container PortGeneral
  - \* Parameter PortDevErrorDetect
  - \* Parameter SIUL2PortIPDevErrorDetect
  - \* Parameter PortSetPinDirectionApi
  - \* Parameter PortSetPinModeApi
  - \* Parameter PortVersionInfoApi
  - $* \ Parameter \ PortSetPinModeDoesNotTouchGpioLevel \\$
  - \* Parameter PortSetAsUnusedPinApi
  - \* Parameter PortResetPinModeApi
  - \* Parameter PortEnableUserModeSupport
  - \* Parameter PortMulticoreSupport
  - \* Reference PortEcucPartitionRef
- Container CommonPublishedInformation
  - \* Parameter ArReleaseMajorVersion
  - \* Parameter ArReleaseMinorVersion
  - \* Parameter ArReleaseRevisionVersion
  - \* Parameter ModuleId
  - \* Parameter SwMajorVersion
  - \* Parameter SwMinorVersion
  - \* Parameter SwPatchVersion
  - \* Parameter VendorApiInfix
  - \* Parameter VendorId

#### 4.1 Module Port

Configuration of the Port module.

Included containers:

- PortConfigSet
- PortGeneral
- CommonPublishedInformation

	Property	Value
	type	ECUC-MODULE-DEF
	lowerMultiplicity	1
	upperMultiplicity	1
	postBuildVariantSupport	true
NXP Semicond	supportedConfigVariants uctors	VARIANT-POST-BUILD, VARIANT-PRE-COMPILE

# 4.2 Container PortConfigSet

This container contains a configuration of the PORT driver / SIUL2 module.

Included subcontainers:

- NotUsedPortPin
- PortContainer
- UnTouchedPortPin
- UntouchedIMCR

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

### 4.3 Container NotUsedPortPin

The init parameters values for the not used pins in the PORT configuration.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

### 4.4 Parameter PortPinPue

Enables the pull function. Used only when the associated destination is a chip pin.

Checked box means the Pull Up or Pull Down configuration selected by 'PortPin PUS' is enabled for the pin.

Unchecked box means the Pull Up or Pull Down configuration selected by 'PortPin PUS' is disabled for the pin.

This is an implementation specific parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

#### 4.5 Parameter PortPinPus

Determines whether the pull function is a pullup or pulldown when the pull function is enabled by the 'PortPin Pull Enable' field. Used only when the associated destination is a chip pin.

Checked box means the Pull Up configuration is set. Unchecked box means the Pull Down configuration is set.

This is an implementation specific parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

## 4.6 Parameter PortPinDirection

Selects the initial direction of the pin (IN or OUT). If the direction is not changeable, the value configured here is fixed.

#### Tresos Configuration Plug-in

The pin direction can be set only for the GPIO pins. For the Alternative Function modes the OUT pin direction is hw selected.

If the IN direction is needed too, it can be set at runtime.

NOTE: To set the IN direction take care, please, that all the possible module

inputs, possible as Alternative Functions for the pad mode,

are hw connected together, if IN direction is enabled, to the pad.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	PORT_PIN_IN
literals	['PORT_PIN_IN', 'PORT_PIN_OUT', 'PORT_PIN_DISABLED']

## 4.7 Parameter PortPinLevelValue

Port Pin Level value from Port pin list.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
varueConnigCrasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	PORT_PIN_LEVEL_LOW
literals	['PORT_PIN_LEVEL_HIGH', 'PORT_PIN_LEVEL_LOW']

# 4.8 Container PortContainer

Container collecting the PortPins.

Included subcontainers:

#### • PortPin

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE

## 4.9 Parameter PortNumberOfPortPins

The number of specified PortPins in this PortContainer.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	3
max	191
min	1

## 4.10 Container PortPin

Configuration of the individual port pins.

Included subcontainers:

• None

#### Tresos Configuration Plug-in

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE

## 4.11 Parameter PortPinPue

Enables the pull function. Used only when the associated destination is a chip pin.

Checked box means the Pull Up or Pull Down configuration selected by 'PortPin PUS' is enabled for the pin.

Unchecked box means the Pull Up or Pull Down configuration selected by 'PortPin PUS' is disabled for the pin.

This is an implementation specific parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

### 4.12 Parameter PortPinPus

Determines whether the pull function is a pullup or pulldown when the pull function is enabled by the 'PortPin Pull Enable' field. Used only when the associated destination is a chip pin.

Checked box means the Pull Up configuration is set. Unchecked box means the Pull Down configuration is set.

This is an implementation specific parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

## 4.13 Parameter PortPinSafeMode

Safe Mode Control

Used only when the associated destination is a chip pin. Specifies whether the chip disables the pin's output buffer when the chip enters Safe Mode.

Unchecked box means output is disabled in Safe Mode. The output buffer returns to its previous state when the chip leaves Safe Mode.

Checked box means that output is not disabled in Safe Mode.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

## 4.14 Parameter PortPinOde

Enable Open Drain Output for the configured Pin.

Checked box means the Open Drain configuration is set.

# Tresos Configuration Plug-in

This is an implementation specific parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

### 4.15 Parameter PortPinWithReadBack

Enables/Disables the read back possibility for this pin. Checked box means the Read Back is enabled.

When ReadBack is enabled, the Input Bufer of the pin gets enabled by setting the IBE bit in the MSCR (PCR) of the pin. Some alternate functions working as inputs might require having the IBE set to 1, so check this box in order to achieve this.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

#### 4.16 Parameter PortPinRcvr

Receiver Select

Checked box means that the single ended receiver is enabled.

Unchecked box means that the differential vref based receiver is enabled.

Note: In S32R or SIUL2\_0 of S32G platform, 1833 and GPIO33 pad types do not support this feature

#### Tresos Configuration Plug-in

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

# 4.17 Parameter PortPinDirectionChangeable

Enable/Disable the changeability for the configured Pin. Checked box means the Direction Changeability is enabled.

This is an implementation specific parameter. The changeable pin direction can be set only for the GPIO pins.

For a mode different than GPIO, pin direction changeability shall be disabled.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

# 4.18 Parameter PortPinModeChangeable

Parameter to indicate if the mode of a port pin is changeable during runtime.

Checked box: Port Pin mode changeable allowed.

Unchecked box: Port Pin mode changeable not permitted

The function for changing the pin modes is not supported by the safety implementation.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

## 4.19 Parameter PortPinSiul2Instance

Selects one of the SIULs instances available on the platform to configure the current pin from.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SIUL2_0
literals	['SIUL2_0', 'SIUL2_1']

# 4.20 Parameter PortPinId

Pin Id of the port pin.

This value will be assigned to the symbolic name derived from the port pin container short name.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	AUTOSAR_ECUC

#### Tresos Configuration Plug-in

Property	Value
symbolicNameValue	true
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	2
max	191
min	1

## 4.21 Parameter PortPinPcr

Used to specify port configuration register: SIUL I/O Pin Multiplexed Signal Configuration Registers (MSCR number).

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	0
max	190
min	0

#### 4.22 Parameter PortPinDirection

Selects the direction of the pin (IN, OUT , INOUT or HIGH\_Z) that will be configured by Port\_Init() function if the pin is configured as GPIO.

If the direction is not changeable, the value configured here is fixed. For the Alternative Function modes (PortPinMode is different than GPIO),

the setting in this enumeration control is kept in the port configuration structure and it is used when Port\_SetPinMode() is called at runtime to change the mode of the pin to GPIO.

If your Alternative Function is an input functionality that requires the IBE bit to be set in the MSCR, please select the checkbox 'PortPinWithReadback.

If direction is PORT\_PIN\_HIGH\_Z, there will be no initial direction setting.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	PORT_PIN_HIGH_Z
literals	['PORT_PIN_IN', 'PORT_PIN_OUT', 'PORT_PIN_INOUT', 'PORT_PIN← _HIGH_Z']

# 4.23 Parameter PortPinInitialMode

Port pin mode from mode list for use with Port\_Init() function.

NOTE: This parameter is not used in the current implementation and is retained as per std AUTOSAR\_EcucParamDef.arxml file.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	PORT_GPIO_MODE
literals	['PORT_GPIO_MODE', 'PORT_ALT1_FUNC_MODE', 'PORT_ALT2← _FUNC_MODE', 'PORT_ALT3_FUNC_MODE', 'PORT_ANALOG_← INPUT_MODE', 'PORT_ONLY_INPUT_MODE', 'PORT_EXTRA_← INPUT_MODE']

## Tresos Configuration Plug-in

# 4.24 Parameter PortPinMode

Selects the PORT pin mode from the modes list. One or more modes may be valid for a pin. This way it is possible to select between multiple modes. (e.g. DIO (GPIO option) or ICU (eTimer option)).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	GPIO

GPIO, 'ADCSAR 0, ADCSAR0, INJ. TRIC,' 'ADCSAR 0, ADCSAR0	Property	Value
TRIG. 'ADGSAR I ADGSAR INJ TRIG. 'ADGSAR I ADGSAR I TRIG.' BOOT BOOTMOD 0' BOOT BOOTMOD 1' BOOT RCONIO' BOOT	literals	['GPIO', 'ADCSAR 0 ADCSAR0 INJ TRIG', 'ADCSAR 0 ADCSAR0 $\leftarrow$
TRIG. 'BOOT_BOOTMOD_9', 'BOOT_BOOTMOD_1, 'BOOT_RCON12'  BOOT_RCON14', 'BOOT_RCON15', 'BOOT_RCON12', 'BOOT_RCON12', 'BOOT_RCON12', 'BOOT_RCON21', 'BOOT_RCON21', 'BOOT_RCON22', 'BOOT_RCON23', 'BOOT_RCON23', 'BOOT_RCON23', 'BOOT_RCON23', 'BOOT_RCON23', 'BOOT_RCON23', 'BOOT_RCON23', 'BOOT_RCON23', 'BOOT_RCON23', 'BOOT_RCON30', 'BOOT_RCON31', 'BOOT_RCON3		
BOOT RCON14, 'BOOT RCON15, 'BOOT RCON16, 'BOOT RCON27'   BOOT RCON21, 'BOOT RCON29, 'BOOT RCON23, 'BOOT RCON24, 'BOOT RCON23, 'BOOT RCON221, 'BOOT RCON221, 'BOOT RCON221, 'BOOT RCON221, 'BOOT RCON231, 'BOOT RCON231, 'BOOT RCON231, 'BOOT RCON231, 'BOOT RCON321, 'BOOT RCON322, 'BOOT RCON322		TRIG', 'BOOT BOOTMOD 0', 'BOOT BOOTMOD 1', 'BOOT RCON0',
BOOT RCONIS, 'BOOT RCON2,' 'BOOT RCON2)'   BOOT RCON25,' 'BOOT RCON22,' 'BOOT RCON26,' 'BOOT RCON26,' 'BOOT RCON27,' 'BOOT RCON27,' 'BOOT RCON27,' 'BOOT RCON27,' 'BOOT RCON27,' 'BOOT RCON27,' 'BOOT RCON28,' 'BOOT RCON27,' 'BOOT RCON31,' 'BOOT R		'BOOT_RCON10', 'BOOT_RCON11', 'BOOT_RCON12', 'BOOT_RCON13',
"BOOT_RCON2!, 'BOOT_RCON2!, 'BOOT_RCON2!, 'BOOT_RCON2!  "BOOT_RCON29!, 'BOOT_RCON2!, 'BOOT_RCON3!, 'BOOT_RCON3!  "BOOT_RCON3!, 'BOOT_RCON2!, 'BOOT_RCON3!, 'BOOT_RCON3!  "BOOT_RCON3!, 'BOOT_RCON3!, 'BOOT_RCON3!, 'BOOT_RCON3!  "BOOT_RCON3!, 'BOOT_RCON3!, 'BOOT_RCON9!, 'EOOT_RCON6!  "BOOT_RCON3!, 'BOOT_RCON8!, 'BOOT_RCON9!, 'CTU_CTU_EXT_TRIG!, 'DSPI_0_DSPI_DCON9!, 'CTU_CTU_EXT_TRIG!, 'DSPI_0_DSPI_DCON9!, 'CTU_CTU_EXT_TRIG!, 'DSPI_0_DSPI_DCON9!, 'CTU_CTU_EXT_TRIG!, 'DSPI_0_DSPI_DCON9!, 'DSPI_0_DSPI_0_PCS2!, 'DSPI_0_DSPI_DCS0!, 'DSPI_0_DSPI_0_PCS2!, 'DSPI_0_DSPI_DCON9!, 'DSPI_0_DSPI_0_PCS2!, 'DSPI_0_DSPI_0_PCS3', 'DSPI_0_DSPI_DCON9!, 'DSPI_0_DSPI_0_PCS2!, 'DSPI_0_DSPI_0_DSPI_0_PCS3', 'DSPI_0_DSPI_DCS0!, 'DSPI_0_DSPI_0_SCK_NOUT!, 'DSPI_1_DSPI_DCS0. 'NSPI_0_DSPI_DSPI_DCS0!, 'NSPI_0_DSPI_DCS0!, 'NSPI_1_DSPI_DCS0. 'NSPI_0_DSPI_DSPI_DCS0!, 'NSPI_1_DSPI_DCS0!, 'NSPI_1_DSPI_DSPI_DCS0!, 'NSPI_1_DSPI_DSPI_DCS0!, 'DSPI_1_DSPI_DSPI_DCS0!, 'NSPI_1_DSPI_DSPI_DSPI_DSPI_DSPI_DSPI_DSPI_DSPI		'BOOT_RCON14', 'BOOT_RCON15', 'BOOT_RCON16', 'BOOT_RCON17',
"BOOT_RCON25', 'BOOT_RCON26', 'BOOT_RCON27', 'BOOT_RCON31' "BOOT_RCON39', 'BOOT_RCON4', 'BOOT_RCON50', 'DOOT_RCON50', 'DOOT_ROOT_RCON50', 'DOOT_ROOT_RCON50', 'DOOT_ROOT_RCON50', 'DOOT_ROOT_ROOT_ROOT_ROOT_ROOT_ROOT_ROOT_		'BOOT_RCON18', 'BOOT_RCON19', 'BOOT_RCON1', 'BOOT_RCON20',
"BOOT_RCON29", BOOT_RCON2", BOOT_RCON30", BOOT_RCON51" "BOOT_RCON5", "BOOT_RCON4", "BOOT_RCON5", "BOOT_RCON5" "BOOT_RCON5", "BOOT_RCON9", "CTU_CTU_EXT_TRIG", "ISBI 0 DSPI0 PCS0 INVOIDED OSPI0 PCS0 OUT", "DSPI 0 DSPI0 PCS0 INVOIDED OSPI0 PCS9", "DSPI 0 DSPI0 PCS9", "DSPI 1 DSPI1 PCS0 UT", "DSPI 1 DSPI1 PCS1", "DSPI 1 DSPI1 PCS2", "DSPI 1 DSPI1 PCS2", "DSPI 1 DSPI1 PCS3", "DSPI 1 DSPI1 PCS1", "DSPI 1 DSPI1 PCS2", "DSPI 1 DSPI1 PCS4", "DSPI 1 DSPI1 PCS2", "DSPI 1 DSPI1 PCS4", "DSPI 1 DSPI1 PCS4", "DSPI 1 DSPI1 PCS1", "DSPI 2 DSPI2 PCS0 UOUT", "DSPI 2 DSPI2 PCS1", "DSPI 2 DSPI2 PCS0 UOUT", "DSPI 2 DSPI2 PCS1", "DSPI 3 DSPI3 PCS1", "DSPI 4 DSPI4 PCS1", "DSPI 5 DSPI5 PCS2", "DSPI 5 DSPI5 PCS2", "DSPI 5 DSPI5 PCS3", "DSPI5 PCS3", "D		'BOOT_RCON21', 'BOOT_RCON22', 'BOOT_RCON23', 'BOOT_RCON24',
"BOOT_RCON3", 'BOOT_RCON4", 'BOOT_RCON5", 'BOOT_RCON6"  BOOT_RCON7', 'BOOT_RCON8', 'BOOT_RCON9', 'CTU_CTU_EXT_TRIG', 'DSPI_0_DSPI0_PCS0_INOUT', 'DSPI_0_DSPI0_PCS0_INOUT', 'DSPI_0_DSPI0_PCS0_INOUT', 'DSPI_0_DSPI0_PCS0_INOUT', 'DSPI_0_DSPI0_PCS0_INOUT', 'DSPI_0_DSPI0_PCS0_INOUT', 'DSPI_0_DSPI0_PCS1', 'DSPI_0_DSPI0_PCS1', 'DSPI_0_DSPI0_PCS5', 'DSPI_0_DSPI0_PCS1', 'DSPI_0_DSPI0_PCS5', 'DSPI_0_DSPI0_PCS1', 'DSPI_0_DSPI0_PCS1', 'DSPI_0_DSPI0_PCS5', 'DSPI_0_DSPI0_PCS1', 'DSPI_0_DSPI0_SCK_INOUT', 'DSPI_0_DSPI0_SCK_OUT'  'DSPI_0_DSPI0_SIN', 'DSPI_0_DSPI0_SOUT', 'DSPI_1_DSPI1_PCS0_INOUT', 'DSPI_1_DSPI1_PCS0_INOUT', 'DSPI_1_DSPI1_PCS0_INOUT', 'DSPI_1_DSPI1_PCS0_INOUT', 'DSPI_1_DSPI1_PCS0_INOUT', 'DSPI_1_DSPI1_PCS0_INOUT', 'DSPI_1_DSPI1_SCK_INOUT', 'DSPI_1_DSPI1_SCK_INOUT', 'DSPI_1_DSPI1_SCK_INOUT', 'DSPI_1_DSPI1_SCK_INOUT', 'DSPI_1_DSPI1_SCK_INOUT', 'DSPI_1_DSPI1_SCK_INOUT', 'DSPI_1_DSPI1_SCK_INOUT', 'DSPI_2_DSPI2_PCS0_INOUT', 'DSPI_2_DSPI2_PCS0_INOUT', 'DSPI_2_DSPI2_PCS0_INOUT', 'DSPI_2_DSPI2_PCS1_INOUT', 'DSPI_2_DSPI2_PCS1_INOUT', 'DSPI_2_DSPI2_SCK_INOUT', 'DSPI_2_DSPI2_SCK_INOUT', 'DSPI_3_DSPI3_PCS0_IN'  "DSPI_3_DSPI3_PCS0_UT', 'DSPI_3_DSPI3_PCS1_IN', 'DSPI3_DSPI3_PCS0_IN'  "DSPI_3_DSPI3_PCS0_UT', 'DSPI_3_DSPI3_PCS1_IN', 'DSPI3_DSPI3_PCS0_IN'  "DSPI_3_DSPI3_PCS0_UT', 'DSPI_3_DSPI3_PCS1_IN', 'DSPI3_SCK_IN', 'DSPI3_SCK_IN', 'DSPI3_BSPI3_PCS0_IN'  "DSPI_3_DSPI3_PCS0_UT', 'DSPI_3_DSPI3_SCK_IN', 'DSPI3_SCK_IN', 'DSPI3_BSPI3_PCS0_IN'  "DSPI_3_DSPI3_PCS0_UT', 'DSPI_3_DSPI3_SCK_IN', 'DSPI3_SOUT'  "DSPI_3_DSPI3_PCS0_UT', 'DSPI_3_DSPI3_SCK_IN', 'DSPI3_BSPI3_PCS0_IN'  "DSPI_3_DSPI3_SCK_INOUT', 'DSPI_3_DSPI3_SCK_IN', 'DSPI3_DSPI3_SOUT'  "DSPI_4_DSPI4_PCS3', 'DSPI_4_DSPI4_PCS1', 'DSPI_4_DSPI4_PCS1'  "DSPI_4_DSPI4_PCS3', 'DSPI_4_DSPI4_PCS1', 'DSPI_5_DSPI5_PCS1_DSPI5_PCS1_N', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS0_IN'		'BOOT_RCON25', 'BOOT_RCON26', 'BOOT_RCON27', 'BOOT_RCON28',
"BOOT_RCONT, 'BOOT_RCONS, 'BOOT_RCONS, 'CTU_CTU_EXTATRIG', 'DSPI_0_DSPI_0_PCS0_INUT', 'DSPI_0_DSPI_0_PCS0_INUT', 'DSPI_0_DSPI_0_DSPI_0_PCS0_INUT', 'DSPI_0_DSPI_0_DSPI_0_PCS1,' 'DSPI_0_DSPI_0_DSPI_0_PCS2,' 'DSPI_0_DSPI_0_DSPI_0_DSPI_0_PCS2,' 'DSPI_0_DSPI_0_DSPI_0_DSPI_0_PCS3,' 'DSPI_0_DSPI_0_DSPI_0_SCK_INUT', 'DSPI_0_DSPI_0_SCK_INUT', 'DSPI_0_DSPI_0_SCK_INUT', 'DSPI_0_DSPI_0_SCK_INUT', 'DSPI_0_DSPI_0_SCK_INUT', 'DSPI_1_DSPI_1_PCS0_IN', 'DSPI_1_DSPI_1_PCS0_IN', 'DSPI_1_DSPI_1_PCS3,' 'DSPI_1_DSPI_1_PCS1,' 'DSPI_1_DSPI_2_PCS0_INOUT', 'DSP1_2_DSP1_2_PCS0_INOUT', 'DSP1_2_DSP1_2_PCS0_INOUT', 'DSP1_2_DSP1_2_PCS0_IN', 'DSP1_2_DSP1_2_PCS0_IN', 'DSP1_2_DSP1_2_PCS0_IN', 'DSP1_2_DSP1_2_PCS0_IN', 'DSP1_2_DSP1_2_PCS0_IN', 'DSP1_2_DSP1_2_PCS0_IN', 'DSP1_2_DSP1_2_PCS1_1, 'DSP1_3_DSP1_3_PCS0_IN', 'DSP1_3_DSP1_3_DSP1_3_PCS0_IN', 'DSP1_3_DSP1_3_PCS0_IN', 'DSP1_3_DSP1_3_DSP1_3_DSP1_3_PCS0_IN', 'DSP1_3_DSP1_3_PCS0_IN', 'DSP1_3_DSP1_3_PCS0_IN', 'DSP1_3_DSP1_3_DSP1_3_DSP1_3_PCS0_IN', 'DSP1_3_DSP1_3_PCS0_IN', 'DSP1_3_DSP1_3_DSP1_3_DSP1_3_PCS0_IN', 'DSP1_3_DSP1_3_DSP1_3_PCS0_IN', 'DSP1_3_DSP1_3_DSP1_3_PCS0_IN', 'DSP1_3_DSP1_3_DSP1_3_PCS0_IN', 'DSP1_3_DSP1_3_DSP1_3_PCS0_IN', 'DSP1_4_DSP1_5_DSP1_5_DSP1_5_DSP1_5_DSP1_5_DSP1_5_		
TRIC', 'DSPI_ DSPI0_PCS0_INOUT', 'DSPI_ DSPI0_ DSPI0_PCS0_N' 'DSPI_ DSPI0_DSPI0_PCS0_OUT', 'DSPI0_DSPI0_PCS1,' 'DSPI_ 0_DSPI0_PCS2,' 'DSPI_ 0_DSPI0_PCS3,' 'DSPI_ 0_DSPI0_PCS4,' 'DSPI_ 0_DSPI0_PCS5,' 'DSPI_ 0_DSPI0_PCS5,' 'DSPI_ 0_DSPI0_PCS5,' 'DSPI_ 0_DSPI0_PCS6,' 'DSPI_ 0_DSPI0_PCS6,' 'DSPI_ 0_DSPI0_SCK_UN' 'DSPI_ 0_DSPI0_SIN', 'DSPI_ 0_DSPI0_SCK_IN', 'DSPI_ 1_DSPI1_PCS0_OUT' 'DSPI_ 1_DSPI1_PCS1,' 'DSPI_ 1_DSPI_PCS2,' 'DSPI_ 1_DSPI1_PCS0_OUT' 'DSPI_ 1_DSPI1_PCS1,' 'DSPI_ 1_DSPI1_PCS2,' 'DSPI_ 1_DSPI1_PCS0_OUT' 'DSPI_ 1_DSPI1_PCS1,' 'DSPI_ 1_DSPI1_PCS2,' 'DSPI_ 1_DSPI1_PCS0_OUT' 'DSPI_ 1_DSPI1_PCS1,' 'DSPI_ 1_DSPI1_SCK_INOUT', 'DSPI_ 1_DSPI1_PCS0_OUT' 'DSPI_ 1_DSPI1_PCS1,' 'DSPI_ 2_DSPI1_DSPI1_DSPI1_PCS0_OUT' 'DSPI_ 0SPI1_SOUT', 'DSPI_ 2_DSPI2_PCS0_INOUT', 'DSPI_ 1_DSPI1_SCK_IN', 'DSPI_ 2_DSPI2_PCS0_IN', 'DSPI_ 2_DSPI2_SCK_IN', 'DSPI_ 2_DSPI2_SCK_IN', 'DSPI_ 3_DSPI3_PCS0_IN', 'DSPI_ 3_DSPI3_PCS0_IN', 'DSPI_ 3_DSPI3_PCS0_IN', 'DSPI_ 3_DSPI3_PCS0_IN', 'DSPI_ 3_DSPI3_PCS0_IN', 'DSPI_ 3_DSPI3_SCK_IN', 'DSPI_ 3_DSPI3_SC		
'DSPI_0_DSPI0_PCS0_OUT', 'DSPI_0_DSPI0_PCS1', 'DSPI_0_DSPI0_PCS2', 'DSPI_0_DSPI0_PCS3', 'DSPI_0_DSPI0_PCS1', 'DSPI_0_DSPI0_PCS3', 'DSPI_0_DSPI0_PCS1', 'DSPI_0_DSPI0_SCK_DUT'   'DSPI_0_DSPI0_SN', 'DSPI_0_DSPI0_SOUT', 'DSPI_1_DSPI1_PCS0_INOUT', 'DSPI_1_DSPI1_PCS0_INOUT', 'DSPI_1_DSPI1_PCS0_INOUT', 'DSPI_1_DSPI1_PCS0_UT'   'DSPI_1_DSPI1_PCS1', 'DSPI_1_DSPI1_PCS2', 'DSPI_1_DSPI1_PCS0_UT'   'DSPI_1_DSPI1_PCS1', 'DSPI_1_DSPI1_PCS2', 'DSPI_1_DSPI1_PCS3', 'DSPI_1_DSPI1_PCS1', 'DSPI_1_DSPI1_PCS1', 'DSPI_1_DSPI1_SOUT', 'DSPI_1_DSPI1_PCS3', 'DSPI_1_DSPI1_SOUT', 'DSPI_1_DSPI1_SOUT', 'DSPI_1_DSPI1_SOUT', 'DSPI_1_DSPI1_SOUT', 'DSPI_1_DSPI1_SOUT', 'DSPI_2_DSPI2_PCS0_INOUT', 'DSPI_2_DSPI2_PCS0_INOUT', 'DSPI_2_DSPI2_PCS0_INOUT', 'DSPI_2_DSPI2_PCS1', 'DSPI_2_CSC_INOUT', 'DSPI_2_DSPI2_PCS1', 'DSPI_2_SOUT', 'DSPI_2_DSPI2_SOUT', 'DSPI_2_DSPI2_SOUT', 'DSPI_2_DSPI2_SOUT', 'DSPI_2_DSPI2_SOUT', 'DSPI_2_DSPI2_SOUT', 'DSPI_2_DSPI2_SOUT', 'DSPI_3_DSPI3_DSPI3_SOUT', 'DSPI_3_DSPI3_DSPI3_SOUT', 'DSPI_3_DSPI3_DSPI3_SOUT', 'DSPI_3_DSPI3_DSPI3_SOUT', 'DSPI_3_DSPI3_SOUT', 'DSPI_3_DSPI3_SOUT', 'DSPI_3_DSPI3_SOUT', 'DSPI_3_DSPI3_SOUT', 'DSPI_3_DSPI3_SOUT', 'DSPI_4_DSPI4_PCS0_OUT', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS0_UT', 'DSPI_4_DSPI4_PCS1', 'DSPI_4_DSPI4_PCS0_UT', 'DSPI_4_DSPI4_SOUT', 'DSPI_5_DSPI5_SOUT',		
PCS2', 'DSPI_0_DSPI0_PCS3', 'DSPI_0_DSPI0_PCS5', 'DSPI_0_DSPI0_PCS6', 'DSPI_0_DSPI0_PCS6', 'DSPI_0_DSPI0_PCS6', 'DSPI_0_DSPI0_SCK_IN', 'DSPI_0_DSPI0_SCK_OUT'  'DSPI_0_DSPI0_SIN', 'DSPI_0_DSPI0_SCK_IN', 'DSPI_1_DSPI1_PCS0_UIT'  'DSPI_1_DSPI1_PCS1', 'DSPI_1_DSPI1_PCS0_UIT', 'DSPI_1_DSPI1_PCS0_UIT'  'DSPI_1_DSPI1_PCS1', 'DSPI_1_DSPI1_PCS2_'DSPI_1_DSPI1_PCS3'  'DSPI_1_DSPI1_PCS1', 'DSPI_1_DSPI1_SCK_OUT', 'DSPI_1_DSPI1_PCS3'  'DSPI_1_DSPI1_PCS1', 'DSPI_1_DSPI1_SCK_OUT', 'DSPI_1_DSPI1_PCS3'  'DSPI_1_DSPI1_PCS1', 'DSPI_2_DSPI2_SCK_OUT', 'DSPI_1_DSPI1_SCK_OUT', 'DSPI_2_DSPI2_PCS0_IN', 'DSPI_2_DSPI2_PCS0_IN', 'DSPI_2_DSPI2_PCS0_IN', 'DSPI_2_DSPI2_PCS0_IN', 'DSPI_2_DSPI2_PCS0_IN', 'DSPI_2_DSPI2_PCS0_IN', 'DSPI_2_DSPI2_PCS0_IN', 'DSPI_2_DSPI2_PCS0_IN', 'DSPI_2_DSPI2_PCS3', 'DSPI_2_DSPI2_PCS0_IN', 'DSPI_2_DSPI2_PCS0_IN', 'DSPI_2_DSPI2_SCK_IN'  'DSPI_2_DSPI2_SCK_OUT', 'DSPI_2_DSPI2_SIN', 'DSPI_2_DSPI2_SCK_IN'  'DSPI_3_DSPI3_PCS0_OUT', 'DSPI_3_DSPI3_PCS1', 'DSPI_3_DSPI3_PCS0_IN'  'DSPI_3_DSPI3_PCS0_OUT', 'DSPI_3_DSPI3_PCS1', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS0_OUT', 'DSPI_5_DSPI5_PCS1', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS0_OUT', 'DSPI_5_DSPI5_PCS1', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5_DSPI5_PCS0_IN',		
PCSS', 'DSPL_0_DSPlo_PCSG', 'DSPL_0_DSPlo_SCK_OUT'  'DSPL_0_DSPlo_SIN', 'DSPL_0_DSPlo_SCK_IN', 'DSPL_0_DSPlo_SCK_OUT'  'DSPL_0_DSPlo_SIN', 'DSPL_0_DSPlo_SOUT', 'DSPL_1_DSPLL_PCS0_UT'  'DSPL_1_DSPLL_PCS1', 'DSPL_1_DSPLL_PCS2', 'DSPL_1_DSPLL_PCS0_OUT'  'DSPL_1_DSPLL_PCS1', 'DSPL_1_DSPLL_PCS2', 'DSPL_1_DSPLL_PCS3'  'DSPL_1_DSPLL_PCS1', 'DSPL_1_DSPLL_PCS1', 'DSPL_1_DSPLL_PCS3'  'DSPL_1_DSPLL_PCS1', 'DSPL_1_DSPLL_SCK_INOUT', 'DSPL_1_DSPLL_PCS0_OUT', 'DSPL_2_DSPL2_PCS0_INOUT', 'DSPL_2_DSPL2_PCS0_INOUT', 'DSPL2_DSPL2_PCS0_IN', 'DSPL2_DSPL2_PCS0_IN', 'DSPL2_DSPL2_PCS0_IN', 'DSPL2_DSPL2_PCS0_IN', 'DSPL2_DSPL2_PCS0_IN', 'DSPL2_DSPL2_PCS0_IN', 'DSPL2_DSPL2_SCK_IN', 'DSPL2_DSPL2_SCK_IN', 'DSPL2_DSPL2_SCK_IN', 'DSPL2_DSPL2_SCK_IN', 'DSPL2_DSPL2_SCK_IN', 'DSPL2_DSPL2_SCK_IN', 'DSPL2_DSPL2_SCK_IN', 'DSPL2_DSPL2_SCK_IN', 'DSPL2_DSPL2_SCK_IN', 'DSPL3_DSPL3_PCS0_IN', 'DSPL3_DSPL3_SCK_IN', 'DSPL3_DSPL3_PCS0_IN', 'DSPL3_DSPL3_SCK_IN', 'DSPL3_DSPL3_SCK_IN', 'DSPL3_DSPL3_PCS0_IN', 'DSPL3_DSPL3_SCK_IN', 'DSPL3_DSPL3_SCK		
SCK INOUT, 'DSPI 0 DSPI0 SCK IN', 'DSPI 1 DSPI1 PCS0- INOUT, 'DSPI1 1 DSPI1 PCS0 IN', 'DSPI1 1 DSPI1 PCS0- INOUT, 'DSPI1 1 DSPI1 PCS0 IN', 'DSPI1 1 DSPI1 PCS0 OUT'  'DSPI 1 DSPI1 PCS1', 'DSPI 1 DSPI1 PCS2', 'DSPI 1 DSPI1 PCS3',  'DSPI 1 DSPI1 PCS1', 'DSPI 1 DSPI1 SCK INOUT', 'DSPI 1 DSPI1 PCS3',  'DSPI 1 DSPI1 PCS1', 'DSPI 1 DSPI1 SCK INOUT', 'DSPI 1 DSPI1 PCS1',  SCK IN', 'DSPI 2 DSPI2 PCS0 INOUT', 'DSPI 2 DSPI2 PCS0- IN', 'DSPI 2 DSPI2 PCS0 INOUT', 'DSPI 2 DSPI2 PCS0- IN', 'DSPI 2 DSPI2 PCS0 INOUT', 'DSPI 2 DSPI2 PCS1', 'DSPI 2 DSPI2 PCS2', 'DSPI 2 DSPI2 PCS2', 'DSPI 2 DSPI2 PCS1', 'DSPI 3 DSPI3 PCS0 INOUT', 'DSPI 3 DSPI3 SCK IN', 'DSPI 4 DSPI4 PCS2', 'DSPI 3 DSPI3 SCK IN', 'DSPI 4 DSPI4 PCS0 INOUT', 'DSPI 4 DSPI4 PCS0 INOUT', 'DSPI 4 DSPI4 PCS0 IN', 'DSPI 4 DSPI4 PCS1', 'DSPI 4 DSPI4 PCS0 INOUT', 'DSPI 4 DSPI4 PCS1', 'DSPI 4 DSPI4 SCK 'DSPI 5 DSPI5 PCS0 INOUT', 'DSPI 5 DSPI5 PCS0 IN', 'DSPI 5 DSPI5 SCK 'DSPI 5 DSPI5 SCK' 'DSPI 5 DSPI5 SCK' 'DSPI 5 DSPI5 SCK' 'DSPI 5 DSPI5 SCK' 'DSPI 5 DSPI5 SCK 'DSPI 5 DSPI5 SCK' 'DSPI 5 DSPI5 SCK 'DSPI 5 DSPI 5 DSPI 5 DSPI 5 D		
DSPI_O_DSPI_O_SNI_, 'DSPI_O_DSPI_O_SOUT', 'DSPI_I_DSPII_PCSO_UT'     DSPI_1 DSPII_PCSI_IN', 'DSPI_I_DSPII_PCSO_UT'     DSPI_1 DSPII_PCSI_IN', 'DSPI_I_DSPII_PCSO_UT'     DSPI_1 DSPII_PCSI_IN', 'DSPI_I_DSPII_PCSI_OUT'     DSPI_1 DSPII_PCSI_IN', 'DSPI_I_DSPII_PCSI_OSPII_PCSI_IN', 'DSPI_I_DSPII_SCK_INOUT', 'DSPI_I_DSPII_PCSI_IN', 'DSPI_I_DSPII_SCK_IN', 'DSPI_I_DSPII_SCK_INOUT', 'DSPI_I_DSPII_SCK_IN', 'DSPI_I_DSPII_SCK_IN', 'DSPI_I_DSPII_SCK_IN', 'DSPI_I_DSPII_SCK_IN', 'DSPI_I_DSPII_SCK_IN', 'DSPI_I_DSPII_SCK_IN', 'DSPI_I_DSPII_PCSI_IN', 'DSPI_I_DSPII_DSPII_DSPII_DSPII_DSPII_IN', 'DSPI_I_DSPII_IN', 'DSPI_I_DSPII_IN', 'DSPI_I_DSPII_IN', 'DSPI_I_DSPII_IN', 'DSPI_I_DSPII_IN', 'DSPI_I_IN', 'DSPI_I_IN', 'DSPI_I_IN', 'DSPI_I_IN', 'DSPI_I_IN', 'DSPI_I_IN', 'DSPI_I_IN', 'DSPI_I_IN', 'DSPI_I_IN', 'DSPI_I_I_IN', 'DSPI_I_IN', 'DSPI_IN', 'DSPI_IN		
INOUT', 'DSPI_1 DSPII_PCS0_IN', 'DSPI_1 DSPII_PCS0_UT'   'DSPI_1 DSPII_PCS1', 'DSPI_1 DSPII_PCS2', 'DSPI_1 DSPII_PCS3', 'DSPI_1 DSPII_PCS3', 'DSPI_1 DSPII_SCK_NOUT', 'DSPI_1 DSPII_SCK_NOUT', 'DSPI_1 DSPII_SCK_NOUT', 'DSPI_1 DSPII_SCK_NOUT', 'DSPI_1 DSPII_SCK_NOUT', 'DSPI_1 DSPII_SCK_NOUT', 'DSPI_2 DSPI2_PCS0_INV', 'DSPI_2 DSPI2_PCS0_INV', 'DSPI_2 DSPI2_PCS0_INV', 'DSPI_2 DSPI2_PCS0_INV', 'DSPI_2 DSPI2_PCS0_INV', 'DSPI_2 DSPI2_PCS0_INV', 'DSPI_2 DSPI2_PCS1', 'DSPI_2 DSPI2_PCS4', 'DSPI_2 DSPI2_PCS4', 'DSPI_2 DSPI2_PCS4', 'DSPI_2 DSPI2_PCS4', 'DSPI_2 DSPI2_SCK_INV', 'DSPI_2 DSPI2_SCK_INV', 'DSPI_2 DSPI2_SCK_INV', 'DSPI_2 DSPI2_SCK_INV', 'DSPI_3 DSPI3_PCS0_INV', 'DSPI_3 DSPI3_SCK_INV, 'DSPI_3 DSPI3_SCK_INV, 'DSPI_3 DSPI3_SCK_INV, 'DSPI_3 DSPI3_SCK_INV, 'DSPI_4 DSPI4_PCS0_INV, 'DSPI_5 DSPI5_PCS0_INV, 'DSPI_		
DSPL   DSPL   PCSL', 'DSPL   DSPL   PCSL', 'DSPL   DSPL   DSPL     SCK_IN', 'DSPL   DSPL   DSPL   SCK_INOUT', 'DSPL   LSPLL     SCK_IN', 'DSPL   DSPL   SCK_OUT', 'DSPL   DSPLS   DSPLS   DSPL     DSPL   SOUT', 'DSPL   DSPL   PCSO_INOUT', 'DSPL   DSPL   PCSO_IN', 'DSPL   DSPL   PCSO_IN', 'DSPL   DSPL   PCSO_IN', 'DSPL   DSPL   PCSL', 'DSPL   DSPL		
DSPI_   DSPI_   PCS4', 'DSPI_   DSPI_   SCK_   INOUT', 'DSPI_   DSPII_   SCK_   IN', 'DSPI_   DSPII_   SCK_   OUT', 'DSPI_   DSPII_   SDSPI_   SIN', 'DSPI_   DSPII_   SCK_   DSPII_   SOUT', 'DSPI_   DSPII_   DSPII_   SOUT', 'DSPI_   DSPII_   PCS0_   INOUT', 'DSPI_   DSPI2_ PCS0+   IN', 'DSPI_   DSPI2_ PCS1', 'DSPI_   DSPI2_ PCS2', 'DSPI_   DSPI2_ SCK_   INOUT', 'DSPI_   DSPI2_ PCS1', 'DSPI_   DSPI2_ SCK_   INOUT', 'DSPI_   DSPI2_ PCS1', 'DSPI_   DSPI2_ SOUT', 'DSPI_   DSPI3_ PCS0_   IN', 'DSPI_   DSPI3_ PCS1', 'DSPI_   DSPI3_ PCS0_   IN', 'DSPI_   DSPI3_ PCS1', 'DSPI_   DSPI3_ PCS0_   IN', 'DSPI_   DSPI3_ PCS1', 'DSPI_   DSPI3_ DSPI3_ PCS1		
SCK_IN', 'DSPI_1 DSPII_SCK_OUT', 'DSPI_1 DSPII_SIN', 'DSPI_1-DSPII_SOUT', 'DSPI_2 DSPI2_PCS0-INOUT', 'DSPI_2 DSPI2_PCS0-IN', 'DSPI_2 DSPI2_PCS0-IN', 'DSPI_2 DSPI2_PCS1', 'DSPI_2 DSPI2_PCS2', 'DSPI_2 DSPI2_PCS3', 'DSPI_2 DSPI2_PCS4', 'DSPI_2 DSPI2_SCK_INOUT', 'DSPI_2 DSPI2_SCK_IN', 'DSPI_2 DSPI2_SCK_INOUT', 'DSPI_2 DSPI2_SCK_IN', 'DSPI_2 DSPI2_SCK_INOUT', 'DSPI_2 DSPI2_SCK_IN', 'DSPI_2 DSPI2_SCK_INOUT', 'DSPI_3 DSPI3_PCS0_IN', 'DSPI_3 DSPI3_PCS0_IN', 'DSPI_3 DSPI3_PCS0_IN', 'DSPI_3 DSPI3_PCS1', 'DSPI_3 DSPI3_PCS2', 'DSPI_3 DSPI3_PCS3', 'DSPI_3 DSPI3_PCS1', 'DSPI_3 DSPI3_SCK_IN', 'DSPI_4 DSPI3_SCK_IN', 'DSPI_4 DSPI4_PCS0_IN', 'DSPI_4 DSPI4_SCK_IN', 'DSPI_4 DSPI4_SCK_IN', 'DSPI_4 DSPI4_SCK_IN', 'DSPI_5 DSPI5_PCS0_IN', 'DSPI_5 DSPI5_PCS0_IN', 'DSPI_5 DSPI5_PCS0_IN', 'DSPI_5 DSPI5_PCS0_IN', 'DSPI_5 DSPI5_PCS0_IN', 'DSPI_5 DSPI5_PCS0_IN', 'DSPI_5 DSPI5_SCK_IN', 'DSPI_5 DSPI5_SCK_IN'		
DSPI1_SOUT', 'DSPI_2_DSPI2_PCS0_INOUT', 'DSPI_2_DSPI2_PCS0_IN', 'DSPI_2_DSPI2_PCS0_OUT', 'DSPI_2_DSPI2_PCS1', 'DSPI_2_DSPI2_PCS2', 'DSPI_2_DSPI2_PCS3', 'DSPI_2_DSPI2_PCS3', 'DSPI_2_DSPI2_SCK_IN'  'DSPI_2_DSPI2_SCK', 'DSPI_2_DSPI2_SCK_INOUT', 'DSPI_2_DSPI2_SCK_IN'  'DSPI_2_DSPI2_SCK_OUT', 'DSPI_2_DSPI2_SIN', 'DSPI_2_DSPI2_SOUT', 'DSPI_3_DSPI3_PCS0_IN'  'DSPI_3_DSPI3_PCS0_OUT', 'DSPI_3_DSPI3_PCS1', 'DSPI_3_DSPI3_PCS0_IN'  'DSPI_3_DSPI3_PCS0_OUT', 'DSPI_3_DSPI3_PCS1', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_3_DSPI3_PCS0_IN'  'DSPI_3_DSPI3_SCK_INOUT', 'DSPI_3_DSPI3_PCS4', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_SCK_INOUT', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_SCK_INOUT', 'DSPI_5_DSPI5_SCK_IN', 'D		
IN', 'DSPI_2 DSPI2 PCS0_OUT', 'DSPI_2 DSPI2 PCS1', 'DSPI_2 ← DSPI2 PCS2', 'DSPI_2 DSPI2 PCS2', 'DSPI_2 DSPI2 SCK, 'DSPI_2 DSPI2 SCK IN' 'DSPI_2 DSPI2 SCK OUT', 'DSPI_2 DSPI2 SCK IN' 'DSPI_2 DSPI2 SCK OUT', 'DSPI_3 DSPI3 PCS0_IN' 'DSPI_4 DSPI3 DSPI3 SCK_IN', 'DSPI_4 DSPI3 DSPI3 SCK_IN', 'DSPI_4 DSPI3 DSPI3 SCK_IN', 'DSPI_4 DSPI4 PCS0_IN', 'DSPI_4 DSPI4 DSPI4 PCS0_IN', 'DSPI_4 DSPI4 PCS0_IN', 'DSPI_5 DSPI5 SCK_IN',		
DSPI2_PCS2', 'DSPI2_DSPI2_PCS3', 'DSPI2_DSPI2_PCS4', 'DSPI_2- DSPI2_SCK', 'DSPI_2_DSPI2_SCK_INOUT', 'DSPI_2_DSPI2_SCK_IN'  'DSPI2_DSPI2_SCK_OUT', 'DSPI2_DSPI2_SIN', 'DSPI_2_DSPI2_SOUT', 'DSPI_3_DSPI3_PCS0_INOUT', 'DSPI_3_DSPI3_PCS0_IN'  'DSPI_3_DSPI3_PCS0_OUT', 'DSPI_3_DSPI3_PCS1', 'DSPI_3_DSPI3_PCS2', 'DSPI_3_DSPI3_PCS3', 'DSPI_3_DSPI3_PCS4', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_4_DSPI3_SCK_IN', 'DSPI_5_DSPI3_DSPI3_SCK_IN', 'DSPI_5_DSPI3_DSPI3_SCK_IN', 'DSPI_5_DSPI3_DSPI3_SCK_IN', 'DSPI_5_DSPI3_DSPI3_SCK_IN', 'DSPI_5_DSPI3_DSPI3_DSPI3_SCK_IN', 'DSPI_5_DSPI3_SCK_IN', 'DSPI_5_		IN', 'DSPI_2_DSPI2_PCS0_OUT', 'DSPI_2_DSPI2_PCS1', 'DSPI_2_&
'DSPI_2 DSPI2_SCK_OUT', 'DSPI_2 DSPI2_SIN', 'DSPI_2 DSPI2_SOUT', 'DSPI_3 DSPI3_PCS0_IN'  'DSPI_3 DSPI3_PCS0_OUT', 'DSPI_3 DSPI3_PCS1_IN'  'DSPI_3 DSPI3_PCS0_OUT', 'DSPI_3 DSPI3_PCS1', 'DSPI_3 DSPI3_PCS2', 'DSPI_3 DSPI3_PCS4', 'DSPI_3 DSPI3_SCK_IN', 'DSPI_4 DSPI3_SCK_IN', 'DSPI_5 DSPI3_SCK_IN', 'DSPI_6 DSPI3_SCK_IN', 'DSPI_7 DSPI3_SCK_IN', 'DSPI_8 DSPI3_SCK_IN', 'DSPI_9 DSPI3_SCK_IN', 'DSPI_9 DSPI3_SCK_IN', 'DSPI_9 DSPI3_SCK_IN', 'DSPI_9 DSPI4_DSPI4_PCS0_IN', 'DSPI_9 DSPI4_PCS0_IN', 'DSPI_9 DSPI4_PCS0_IN', 'DSPI_9 DSPI4_PCS1', 'DSPI_9 DSPI4_PCS2', 'DSPI_9 DSPI4_PCS1', 'DSPI_9 DSPI4_PCS2', 'DSPI_9 DSPI4_PCS1', 'DSPI_9 DSPI4_PCS2', 'DSPI_9 DSPI4_PCS1', 'DSPI_9 DSPI4_PCS2', 'DSPI_9 DSPI4_PCS1', 'DSPI_9 DSPI5_PCS2', 'DSPI_9 DSPI5_PCS0_IN', 'DSPI_9 DSPI5_PCS1', 'DSPI_9 DSPI5_PCS2', 'DSPI_9 DSPI5_PCS0_IN', 'DSPI_9 DSPI5_PCS2', 'DSPI_9 DSPI5_PCS2', 'DSPI_9 DSPI5_PCS2', 'DSPI_9 DSPI5_PCS2', 'DSPI_9 DSPI5_PCS2', 'DSPI_9 DSPI5_PCS2', 'DSPI5_PCS3', 'DSPI_9 DSPI5_PCS4', 'DSPI_9 DSPI5_PCS2', 'DS		DSPI2_PCS2', 'DSPI_2_DSPI2_PCS3', 'DSPI_2_DSPI2_PCS4', 'DSPI_2 ~
_SOUT', 'DSPI_3_DSPI3_PCS0_INOUT', 'DSPI_3_DSPI3_PCS0_IN' 'DSPI_3_DSPI3_PCS0_OUT', 'DSPI_3_DSPI3_PCS1', 'DSPI_3_DSPI3_PCS2', 'DSPI_3_DSPI3_PCS2', 'DSPI_3_DSPI3_PCS3', 'DSPI_3_DSPI3_PCS4', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_3_DSPI3_SOUT' 'DSPI_4_DSPI4_PCS0_INOUT', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS1', 'DSPI_4_DSPI4_PCS2' 'DSPI_4_DSPI4_PCS3', 'DSPI_4_DSPI4_PCS4', 'DSPI_4_DSPI4_SCK' 'DSPI_4_DSPI4_SCK_INOUT', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_DS0_IN', 'DSPI_		_DSPI2_SCK', 'DSPI_2_DSPI2_SCK_INOUT', 'DSPI_2_DSPI2_SCK_IN',
'DSPI_3_DSPI3_PCS0_OUT', 'DSPI_3_DSPI3_PCS1', 'DSPI_3_DSPI3_← PCS2', 'DSPI_3_DSPI3_PCS3', 'DSPI_3_DSPI3_PCS4', 'DSPI_3_DSPI3_ECK_', 'DSPI_3_DSPI3_SCK_' INOUT', 'DSPI_3_DSPI3_SCK_' IN', 'DSPI_3_DSPI3_SCK_' DSPI_3_DSPI3_SCK_' DSPI_3_DSPI3_SCK_' DSPI_3_DSPI3_SCK_' DSPI_4_DSPI3_DSPI3_SOUT'   'DSPI_4_DSPI4_PCS0_INOUT', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_EDSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS1', 'DSPI_4_DSPI4_PCS2'   'DSPI_4_DSPI4_PCS4', 'DSPI_4_DSPI4_SCK_' DSPI_4_DSPI4_SCK_' DSPI_4_DSPI4_SCK_' DSPI_4_DSPI4_SCK_' DSPI_4_DSPI4_SCK_' DSPI_4_DSPI4_SCK_' DSPI_4_DSPI4_SCK_' DSPI_5_DSPI5_PCS0_INOUT', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS1'   'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS1'   'DSPI_5_DSPI5_PCS2' 'DSPI_5_DSPI5_SCK_' DSPI5_DSPI5_SCK_' DSPI5_SCK_' "DSPI_5_DSPI5_SCK_' DSPI5_SCK_'		'DSPI_2_DSPI2_SCK_OUT', 'DSPI_2_DSPI2_SIN', 'DSPI_2_DSPI2←
PCS2', 'DSPI_3_DSPI3_PCS3', 'DSPI_3_DSPI3_PCS4', 'DSPI_3_DSPI3_SCK, 'DSPI_3_DSPI3_SCK_IN', 'DSPI_4_SCK', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_4_SDSPI3_SCK_IN', 'DSPI_4_SDSPI3_SCK_IN', 'DSPI_4_SDSPI3_SCK_IN', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS2', 'DSPI_4_DSPI4_PCS2', 'DSPI_4_DSPI4_PCS2', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS2', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS2', 'DSPI_5_DSPI5_DSPI5_DSPI5_DSPI5_SCK_IN', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5_DSPI5_SOUT', 'FLEXCAN_0_CAN_0_TX', 'FLEXCAN_4_ICAN_1_TX', 'FLEXCAN_4_CAN_2_CAN_2_TX', 'FLEXCAN_3_CAN_3_TX', 'FLEXCAN_3_CAN_3_TX', 'FLEXCAN_3_CAN_3_TX', 'FLEXCAN_3_CAN_3_TX', 'FLEXCAN_3_CAN_3_TX', 'FLEXCAN_4_DSPI_5_DSPI_5_DSPI_5_SCR_IN', 'DSPI_5_DSPI_5_SCR_IN', 'DSPI_5_DSPI_5_SCR_IN', 'DSPI_5_DSPI_5_SCR_IN', 'DSPI_5_DSPI_5_SCR_IN', 'DSPI_5_DSPI_5_SCR_IN', 'DSPI_5_DSPI_5_SOUT', 'FLEXTAN_0_FR_DSG_1', 'FLEXTAN_0_FR_TXS_0_FR_TXD_B', 'FLEXTIMER_0_FTM0_CH0_OUT', 'FLEXTIMER_0_FTM0_CH0_OUT', 'FLEXTIMER_0_FTM0_CH1_INOUT', 'FLEXTIMER_0_FTM0_CH1_INOUT', 'FLEXTIMER_0_FTM0_CH1_IN', 'FLEXTIMER_0_FTM0_CH1_INOUT', 'FLEXTIMER_0_FTM0_CH1_IN', 'FLEXTIMER_0_FTM0_CH1_INOUT', 'FLEXTIMER_0_FTM0_CH1_IN', 'FLEXTIMER_0_FTM0_CH1_IN', 'FLEXTIMER_0_FTM0_CH1_IN', 'FLEXTIMER_0_FTM0_CH1_IN', 'FLEXTIMER_0_FTM0_CH1_IN', 'FLEXTIMER_0_FTM0_CH1_I		_SOUT', 'DSPI_3_DSPI3_PCS0_INOUT', 'DSPI_3_DSPI3_PCS0_IN',
SCK', 'DSPI_3_DSPI3_SCK_INOUT', 'DSPI_3_DSPI3_SCK_IN', 'DSPI_4_ 3_DSPI3_SCK_OUT', 'DSPI_3_DSPI3_SIN', 'DSPI_3_DSPI3_SOUT'  'DSPI_4_DSPI4_PCS0_INOUT', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_ DSPI4_PCS0_OUT', 'DSPI_4_DSPI4_PCS1', 'DSPI_4_DSPI4_PCS2'  'DSPI_4_DSPI4_PCS3', 'DSPI_4_DSPI4_PCS4', 'DSPI_4_DSPI4_PCS2'  'DSPI_4_DSPI4_SCK_INOUT', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS1', 'DSPI_5_DSPI5_PCS2'  'DSPI_5_DSPI5_PCS3', 'DSPI_5_DSPI5_PCS4', 'DSPI_5_DSPI5_SCK'  'DSPI_5_DSPI5_SCK_INOUT', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5_DSPI5_SOUT'  'FLEXCAN_0_CAN0_RX', 'FLEXCAN_0_CAN0_TX', 'FLEXCAN_4_I_CAN1_TX', 'FLEXCAN_4_I_CAN1_TX', 'FLEXCAN_3_CAN3_RX', 'FLEXCAN_3_CAN3_TX', 'FLEXCAN_5_CAN3_TX', 'FLEXCAN_5_CAN3_TX', 'FLEXCAN_5_CAN3_TX', 'FLEXCAN_5_CAN3_TX', 'FLEXCAN_5_CAN3_TX', 'FLEXCAN_5_CAN3_TX', 'FLEXCAN_5_CAN3_TX', 'FLEXCAN_5_CAN3_TX', 'FLEXRAY_0_FR_DBG_1'  'FLEXRAY_0_FR_DBG_2', 'FLEXRAY_0_FR_DBG_3', 'FLEXRAY_0_FR_DBG_1'  'FLEXRAY_0_FR_DBG_2', 'FLEXRAY_0_FR_DBG_3', 'FLEXRAY_0_FR_CAN3_TX', 'FLEXRAY_0_FR_TXD_B', 'FLEXRAY_0_FR_TXE_A_b'  'FLEXRAY_0_FR_TXD_B', 'FLEXRAY_0_FR_TXE_A_b'  'FLEXRAY_0_FR_TXD_B', 'FLEXRAY_0_FR_DSG_TXD_CH0_UN', 'FLEXTIMER_0_FTM0_CH0_UN', 'FLEXTIMER_0_FTM0_CH0_UN', 'FLEXTIMER_0_FTM0_CH1_INOUT',		
3_DSPI3_SCK_OUT', 'DSPI_3_DSPI3_SIN', 'DSPI_3_DSPI3_SOUT' 'DSPI_4_DSPI4_PCS0_INOUT', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS0_OUT', 'DSPI_4_DSPI4_PCS1', 'DSPI_4_DSPI4_PCS2' 'DSPI_4_DSPI4_PCS3', 'DSPI_4_DSPI4_PCS4', 'DSPI_4_DSPI4_SCK' 'DSPI_4_DSPI4_SCK_INOUT', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_5_DSPI5_DSPI5_DSSI5_PCS0_INOUT', 'DSPI_5_DSPI5_PCS0_INOUT', 'DSPI_5_DSPI5_PCS0_INOUT', 'DSPI_5_DSPI5_PCS0_INOUT', 'DSPI_5_DSPI5_PCS1', 'DSPI_5_DSPI5_PCS2' 'DSPI_5_DSPI5_PCS3', 'DSPI_5_DSPI5_PCS4', 'DSPI_5_DSPI5_PCS2' 'DSPI_5_DSPI5_SCK_INOUT', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5_CK' 'DSPI_5_DSPI5_SCK_INOUT', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5_SOUT' 'FLEXCAN_0_CAN0_RX', 'FLEXCAN_0_CAN0_TX', 'FLEXCAN_4- 1_CAN1_RX', 'FLEXCAN_1_CAN1_TX', 'FLEXCAN_2_CAN2_RX' 'FLEXCAN_2_CAN2_TX', 'FLEXCAN_3_CAN3_RX', 'FLEXCAN_4- CAN3_TX', 'FLEXRAY_0_FR_DBG_0', 'FLEXRAY_0_FR_DBG_1' 'FLEXRAY_0_FR_DBG_2', 'FLEXRAY_0_FR_DBG_3', 'FLEXRAY+ _0_FR_RXD_A', 'FLEXRAY_0_FR_RXD_B', 'FLEXRAY_0_FR_DBG_1' 'FLEXRAY_0_FR_TXE_B_b', 'FLEXRAY_0_FR_TXE_A_b' TXD_A', 'FLEXRAY_0_FR_TXD_B', 'FLEXRAY_0_FR_TXE_A_b' 'FLEXTIMER_0_FTM0_CH0_IN', 'FLEXTIMER_0_FTM0_CH0_OUT' 'FLEXTIMER_0_FTM0_CH0_IN', 'FLEXTIMER_0_FTM0_CH1IN', 'FLEXTIMER_0_FTM0_CH1_OUT', 'FLEXTIMER_0_FTM0_CH1IN', 'FLEXTIMER_0_FTM0_CH1_OUT', 'FLEXTIMER_0_FTM0_CH1IN', 'FLEXTIMER_0_FTM0_CH1_FINOUT', 'FLEXTIMER_0_FTM0_CH1CH2_INOUT', 'FLEXTIMER_0_FTM0_CH1CH2_INOUT', 'FLEXTIMER_0_FTM0_CH1CH2_INOUT', 'FLEXTIMER_0_FTM0_CH1-		
'DSPI_4_DSPI4_PCS0_INOUT', 'DSPI_4_DSPI4_PCS0_IN', 'DSPI_4_DSPI4_PCS0_OUT', 'DSPI_4_DSPI4_PCS1', 'DSPI_4_DSPI4_PCS2' 'DSPI_4_DSPI4_PCS3', 'DSPI_4_DSPI4_PCS4', 'DSPI_4_DSPI4_SCK' 'DSPI_4_DSPI4_SCK_INOUT', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_5_DSPI5_PCS0_INOUT', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_DSPI5_PCS1', 'DSPI_5_DSPI5_PCS2' 'DSPI_5_DSPI5_PCS3', 'DSPI_5_DSPI5_PCS4', 'DSPI_5_DSPI5_SCK' 'DSPI_5_DSPI5_SCK_INOUT', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5_DSPI5_SCK' 'DSPI_5_DSPI5_SCK_INOUT', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5_DSPI5_SCK' 'TSPI_5_DSPI5_SCK_INOUT', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5_DSPI5_SOUT' 'FLEXCAN_0_CAN0_RX', 'FLEXCAN_0_CAN0_TX', 'FLEXCAN_← 1_CAN1_RX', 'FLEXCAN_1_CAN1_TX', 'FLEXCAN_2_CAN2_RX' 'FLEXCAN_2_CAN2_TX', 'FLEXCAN_3_CAN3_RX', 'FLEXCAN_3← CAN3_TX', 'FLEXCAN_0_FR_DBG_0', 'FLEXRAY_0_FR_DBG_1' 'FLEXRAY_0_FR_DBG_2', 'FLEXRAY_0_FR_DBG_3', 'FLEXRAY+ 0_FR_RXD_A', 'FLEXRAY_0_FR_RXD_B', 'FLEXRAY_0_FR_← TXD_A', 'FLEXRAY_0_FR_TXD_B', 'FLEXRAY_0_FR_TXE_A_b' 'FLEXRAY_0_FR_TXE_B_b', 'FLEXTIMER_0_FTM0_CH0_INOUT' 'FLEXTIMER_0_FTM0_CH0_IN', 'FLEXTIMER_0_FTM0_CH0_OUT' 'FLEXTIMER_0_FTM0_CH1_INOUT', 'FLEXTIMER_0_FTM0_CH1- IN', 'FLEXTIMER_0_FTM0_CH1_OUT', 'FLEXTIMER_0_FTM0-CH1- IN', 'FLEXTIMER_0_FTM0_CH1-OUT', 'FLEXTIMER_0_FTM0-CH1- IN', 'FLEXTIMER_0_FTM0_CH1-OUT', 'FLEXTIMER_0_FTM0-CH1- IN', 'FLEXTIMER_0_FTM0_CH1-OUT', 'FLEXTIMER_0_FTM0-CH1- IN', 'FLEXTIMER_0_FTM0_CH1-INOUT', 'FLEXTIMER_0_FTM0-CH1-INOUT', 'FLEXTIMER_0_FTM0-CH1-INOUT', 'FLEXTIMER_0_FTM0-CH1-INOUT', 'FLEXTIMER_0_FTM0-CH1-INOUT', 'FLEXTIMER_0_FTM0-CH1-INOUT', 'FLEXTIMER_0_FTM0-CH1-INOUT', 'FLEXTIMER_0_FTM0-CH1-INOUT', 'FLEXTIMER_0_FTM		· · · · · · · · · · · · · · · · · · ·
DSPI4_PCS0_OUT', 'DSPI_4_DSPI4_PCS1', 'DSPI_4_DSPI4_PCS2'  'DSPI_4_DSPI4_PCS3', 'DSPI_4_DSPI4_PCS4', 'DSPI_4_DSPI4_SCK'  'DSPI_4_DSPI4_SCK_INOUT', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4← DSPI4_SCK_OUT', 'DSPI_4_DSPI4_SIN', 'DSPI_4_DSPI4_SOUT'  'DSPI_5_DSPI5_PCS0_INOUT', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5← DSPI5_PCS0_OUT', 'DSPI_5_DSPI5_PCS1', 'DSPI_5_DSPI5_PCS2'  'DSPI_5_DSPI5_PCS3', 'DSPI_5_DSPI5_PCS4', 'DSPI_5_DSPI5_SCK'  'DSPI_5_DSPI5_SCK_INOUT', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5_DSPI5_SCK'  'DSPI_5_DSPI5_SCK_OUT', 'DSPI_5_DSPI5_SIN', 'DSPI_5_DSPI5_SOUT'  'FLEXCAN_0_CAN0_RX', 'FLEXCAN_0_CAN0_TX', 'FLEXCAN_← 1_CAN1_RX', 'FLEXCAN_1_CAN1_TX', 'FLEXCAN_2_CAN2_RX'  'FLEXCAN_2_CAN2_TX', 'FLEXCAN_3_CAN3_RX', 'FLEXCAN_3← CAN3_TX', 'FLEXRAY_0_FR_DBG_0', 'FLEXRAY_0_FR_DBG_1'  'FLEXRAY_0_FR_DBG_2', 'FLEXRAY_0_FR_DBG_3', 'FLEXRAY— _0_FR_RXD_A', 'FLEXRAY_0_FR_RXD_B', 'FLEXRAY_0_FR_← TXD_A', 'FLEXRAY_0_FR_TXD_B', 'FLEXRAY_0_FR_TXE_A_b'  'FLEXRAY_0_FR_TXE_B_b', 'FLEXTIMER_0_FTM0_CH0_INOUT'  'FLEXTIMER_0_FTM0_CH1_INOUT', 'FLEXTIMER_0_FTM0_CH1—IN', 'FLEXTIMER_0_FTM0_CH1, 'IN', 'FLEXTIMER_0_FTM0_CH1, 'IN', 'FLEXTIMER_0_FTM0_CH1, 'IN', 'FLEXTIMER_0_FTM0_CH1, 'IN', 'FLEXTIMER_0_FTM0_CH1, 'IN', 'FLEXTIMER_0_FTM0_CH1, 'IN', 'IN', 'IN', 'IN', 'IN',		
'DSPI_4_DSPI4_PCS3', 'DSPI_4_DSPI4_PCS4', 'DSPI_4_DSPI4_SCK' 'DSPI_4_DSPI4_SCK_INOUT', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4=  _DSPI4_SCK_OUT', 'DSPI_4_DSPI4_SIN', 'DSPI_4_DSPI4_SOUT' 'DSPI_5_DSPI5_PCS0_INOUT', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5=  _DSPI5_PCS0_OUT', 'DSPI_5_DSPI5_PCS1', 'DSPI_5_DSPI5_PCS2' 'DSPI_5_DSPI5_PCS3', 'DSPI_5_DSPI5_PCS4', 'DSPI_5_DSPI5_SCK' 'DSPI_5_DSPI5_SCK_INOUT', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5=  _DSPI5_SCK_OUT', 'DSPI_5_DSPI5_SIN', 'DSPI_5_DSPI5_SOUT' 'FLEXCAN_0_CAN0_RX', 'FLEXCAN_0_CAN0_TX', 'FLEXCAN_4=  1_CAN1_RX', 'FLEXCAN_1_CAN1_TX', 'FLEXCAN_2_CAN2_RX' 'FLEXCAN_2_CAN2_TX', 'FLEXCAN_3_CAN3_RX', 'FLEXCAN_3=  _CAN3_TX', 'FLEXRAY_0_FR_DBG_0', 'FLEXRAY_0_FR_DBG_1' 'FLEXRAY_0_FR_DBG_2', 'FLEXRAY_0_FR_DBG_3', 'FLEXRAY=  0_FR_RXD_A', 'FLEXRAY_0_FR_RXD_B', 'FLEXRAY_0_FR_A=  TXD_A', 'FLEXRAY_0_FR_TXD_B', 'FLEXRAY_0_FR_TXE_A_b' 'FLEXRAY_0_FR_TXE_B_b', 'FLEXTIMER_0_FTM0_CH0_OUT' 'FLEXTIMER_0_FTM0_CH0_IN', 'FLEXTIMER_0_FTM0_CH1=  _IN', 'FLEXTIMER_0_FTM0_CH1_INOUT', 'FLEXTIMER_0_FTM0-CH1=  _IN', 'FLEXTIMER_0_FTM0_CH1_OUT', 'FLEXTIMER_0_FTM0-CH1=  _IN', 'FLEXTIMER_0_FTM0_CH1_OUT', 'FLEXTIMER_0_FTM0-CH1=  _IN', 'FLEXTIMER_0_FTM0_CH1_OUT', 'FLEXTIMER_0_FTM0-CH1=  _IN', 'FLEXTIMER_0_FTM0_CH1_OUT', 'FLEXTIMER_0_FTM0-CH1=  _CH2_INOUT', 'FLEXTIMER_0_FTM0_CH2_IN', 'FLEXTIMER=		
'DSPI_4_DSPI4_SCK_INOUT', 'DSPI_4_DSPI4_SCK_IN', 'DSPI_4← DSPI4_SCK_OUT', 'DSPI_4_DSPI4_SIN', 'DSPI_4_DSPI4_SOUT'  'DSPI_5_DSPI5_PCS0_INOUT', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5← DSPI5_PCS0_OUT', 'DSPI_5_DSPI5_PCS1', 'DSPI_5_DSPI5_PCS2'  'DSPI_5_DSPI5_PCS3', 'DSPI_5_DSPI5_PCS4', 'DSPI_5_DSPI5_SCK'  'DSPI_5_DSPI5_SCK_INOUT', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5← DSPI5_SCK_OUT', 'DSPI_5_DSPI5_SIN', 'DSPI_5_DSPI5_SOUT'  'FLEXCAN_0_CAN0_RX', 'FLEXCAN_0_CAN0_TX', 'FLEXCAN_← 1_CAN1_RX', 'FLEXCAN_1_CAN1_TX', 'FLEXCAN_2_CAN2_RX'  'FLEXCAN_2_CAN2_TX', 'FLEXCAN_3_CAN3_RX', 'FLEXCAN_3← CAN3_TX', 'FLEXRAY_0_FR_DBG_0', 'FLEXRAY_0_FR_DBG_1'  'FLEXRAY_0_FR_DBG_2', 'FLEXRAY_0_FR_DBG_3', 'FLEXRAY_0_FR_E DFR_RXD_A', 'FLEXRAY_0_FR_RXD_B', 'FLEXRAY_0_FR_E  TXD_A', 'FLEXRAY_0_FR_TXD_B', 'FLEXRAY_0_FR_TXE_A_b'  'FLEXRAY_0_FR_TXE_B_b', 'FLEXTIMER_0_FTM0_CH0_OUT'  'FLEXTIMER_0_FTM0_CH0_IN', 'FLEXTIMER_0_FTM0_CH1← IN', 'FLEXTIMER_0_FTM0_CH1_OUT', 'FLEXTIMER_0_FTM0_CH1← IN', 'FLEXTIMER_0_FTM0_CH1_OUT', 'FLEXTIMER_0_FTM0_CH1← IN', 'FLEXTIMER_0_FTM0_CH1_OUT', 'FLEXTIMER_0_FTM0—CH1← CH2_INOUT', 'FLEXTIMER_0_FTM0_CH2_IN', 'FLEXTIMER_0_FTM0—CH2_IN', 'FLEXTIMER_0_FTM0—CH1—INOUT', 'FLEXTIMER_0_FTM0—TNOUT', 'FLEXTIMER_0_FTM0—TNOUT'		
DSPI4_SCK_OUT', 'DSPI_4_DSPI4_SIN', 'DSPI_4_DSPI4_SOUT'  'DSPI_5_DSPI5_PCS0_INOUT', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5_E  DSPI5_PCS0_OUT', 'DSPI_5_DSPI5_PCS1', 'DSPI_5_DSPI5_PCS2'  'DSPI_5_DSPI5_PCS3', 'DSPI_5_DSPI5_PCS4', 'DSPI_5_DSPI5_SCK'  'DSPI_5_DSPI5_SCK_INOUT', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5_E  DSPI5_SCK_OUT', 'DSPI_5_DSPI5_SIN', 'DSPI_5_DSPI5_SOUT'  'FLEXCAN_0_CAN0_RX', 'FLEXCAN_0_CAN0_TX', 'FLEXCAN_E  1_CAN1_RX', 'FLEXCAN_1_CAN1_TX', 'FLEXCAN_2_CAN2_RX'  'FLEXCAN_2_CAN2_TX', 'FLEXCAN_3_CAN3_RX', 'FLEXCAN_3E  _CAN3_TX', 'FLEXRAY_0_FR_DBG_0', 'FLEXRAY_0_FR_DBG_1'  'FLEXRAY_0_FR_DBG_2', 'FLEXRAY_0_FR_DBG_3', 'FLEXRAYE  0_FR_RXD_A', 'FLEXRAY_0_FR_RXD_B', 'FLEXRAY_0_FR_EE  TXD_A', 'FLEXRAY_0_FR_TXD_B', 'FLEXRAY_0_FR_TXE_A_b'  'FLEXTIMER_0_FTM0_CH0_IN', 'FLEXTIMER_0_FTM0_CH0_OUT'  'FLEXTIMER_0_FTM0_CH1_INOUT', 'FLEXTIMER_0_FTM0_CH1=IN', 'FLEXTIMER_0_FTM0_CH1_INOUT', 'FLEXTIMER_0_FTM0=INEX_INCH1=IN', 'FLEXTIMER_0_FTM0_CH1=IN', 'FLEXTIMER_0_FTM0_CH1-IN', 'FLEXTIMER_0_FTM0_CH1-IN', 'FLEXTIMER_0_FTM0_CH1-IN', 'FLEXTIMER_0_FTM0_CH1-IN', 'FLEXTIMER_0_FTM0_CH1-IN', 'FLEXTIMER_0_FTM0_CH1-IN', 'FLEXTIMER_0_FTM0_CH1-IN', 'FLEXTIMER_0_FTM0_CH1-IN', 'FLEXTIMER_0_FTM0_CH1-IN',		
'DSPI_5_DSPI5_PCS0_INOUT', 'DSPI_5_DSPI5_PCS0_IN', 'DSPI_5← _DSPI5_PCS0_OUT', 'DSPI_5_DSPI5_PCS1', 'DSPI_5_DSPI5_PCS2' 'DSPI_5_DSPI5_PCS3', 'DSPI_5_DSPI5_PCS4', 'DSPI_5_DSPI5_SCK' 'DSPI_5_DSPI5_SCK_INOUT', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5← _DSPI5_SCK_OUT', 'DSPI_5_DSPI5_SIN', 'DSPI_5_DSPI5_SOUT' 'FLEXCAN_0_CAN0_RX', 'FLEXCAN_0_CAN0_TX', 'FLEXCAN_← 1_CAN1_RX', 'FLEXCAN_1_CAN1_TX', 'FLEXCAN_2_CAN2_RX' 'FLEXCAN_2_CAN2_TX', 'FLEXCAN_3_CAN3_RX', 'FLEXCAN_3← _CAN3_TX', 'FLEXRAY_0_FR_DBG_0', 'FLEXRAY_0_FR_DBG_1' 'FLEXRAY_0_FR_DBG_2', 'FLEXRAY_0_FR_DBG_3', 'FLEXRAY← _0_FR_RXD_A', 'FLEXRAY_0_FR_RXD_B', 'FLEXRAY_0_FR_← TXD_A', 'FLEXRAY_0_FR_TXD_B', 'FLEXRAY_0_FR_TXE_A_b' 'FLEXRAY_0_FR_TXE_B_b', 'FLEXTIMER_0_FTM0_CH0_INOUT' 'FLEXTIMER_0_FTM0_CH0_IN', 'FLEXTIMER_0_FTM0_CH1← _IN', 'FLEXTIMER_0_FTM0_CH1_OUT', 'FLEXTIMER_0_FTM0← _CH2_INOUT', 'FLEXTIMER_0_FTM0_CH2_IN', 'FLEXTIMER		
DSPI5_PCS0_OUT', 'DSPI_5_DSPI5_PCS1', 'DSPI_5_DSPI5_PCS2'  'DSPI_5_DSPI5_PCS3', 'DSPI_5_DSPI5_PCS4', 'DSPI_5_DSPI5_SCK'  'DSPI_5_DSPI5_SCK_INOUT', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5_C  _DSPI5_SCK_OUT', 'DSPI_5_DSPI5_SIN', 'DSPI_5_DSPI5_SOUT'  'FLEXCAN_0_CAN0_RX', 'FLEXCAN_0_CAN0_TX', 'FLEXCAN_4  1_CAN1_RX', 'FLEXCAN_1_CAN1_TX', 'FLEXCAN_2_CAN2_RX'  'FLEXCAN_2_CAN2_TX', 'FLEXCAN_3_CAN3_RX', 'FLEXCAN_3 \ _CAN3_TX', 'FLEXRAY_0_FR_DBG_0', 'FLEXRAY_0_FR_DBG_1'  'FLEXRAY_0_FR_DBG_2', 'FLEXRAY_0_FR_DBG_3', 'FLEXRAY \ _0_FR_RXD_A', 'FLEXRAY_0_FR_RXD_B', 'FLEXRAY_0_FR_\text{CAN}  TXD_A', 'FLEXRAY_0_FR_TXD_B', 'FLEXRAY_0_FR_TXE_A_b'  'FLEXTIMER_0_FTM0_CH0_IN', 'FLEXTIMER_0_FTM0_CH0_OUT'  'FLEXTIMER_0_FTM0_CH1_INOUT', 'FLEXTIMER_0_FTM0_CH1 \ _IN', 'FLEXTIMER_0_FTM0_CH1_OUT', 'FLEXTIMER_0_FTM0\ _CH2_INOUT', 'FLEXTIMER_0_FTM0_CH2_IN', 'FLEXTIMER_\ _CFTM0_CH1_DUT', 'FLEXTIMER_0_FTM0\ _CH2_INOUT', 'FLEXTIMER_0_FTM0_CH2_IN', 'FLEXTIMER_\ _OFTM0_CH1_OUT', 'FLEXTIMER_0_FTM0\ _CH2_INOUT', 'FLEXTIMER_0_FTM0_CH2_IN', 'FLEXTIMER_\ _OFTM0_CH1_INOUT', 'FLEXTIMER_O_FTM0\ _CH2_INOUT', 'FLEXTIMER_O_FTM0_CH2_IN', 'FLEXTIMER_\ _OFTM0_CH1_INOUT', 'FLEXTIMER_O_FTM0_CH2_IN', 'FLEXTIMER_\ _OFTM0_CH1_INOUT', 'FLEXTIMER_O_FTM0_CH1_INOUT', 'FLEXTIMER_\ _OFTM0_CH1_INOUT', 'FLEXTIMER_O_FTM0_CH1_INOUT', 'FLEXTIMER_\ _OFTM0_CH1_INOUT', 'FLEXTIMER_\ _OF		
'DSPI_5_DSPI5_SCK_INOUT', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5← _DSPI5_SCK_OUT', 'DSPI_5_DSPI5_SIN', 'DSPI_5_DSPI5_SOUT'  'FLEXCAN_0_CAN0_RX', 'FLEXCAN_0_CAN0_TX', 'FLEXCAN_← 1_CAN1_RX', 'FLEXCAN_1_CAN1_TX', 'FLEXCAN_2_CAN2_RX'  'FLEXCAN_2_CAN2_TX', 'FLEXCAN_3_CAN3_RX', 'FLEXCAN_3← _CAN3_TX', 'FLEXRAY_0_FR_DBG_0', 'FLEXRAY_0_FR_DBG_1'  'FLEXRAY_0_FR_DBG_2', 'FLEXRAY_0_FR_DBG_3', 'FLEXRAY← _0_FR_RXD_A', 'FLEXRAY_0_FR_RXD_B', 'FLEXRAY_0_FR_← TXD_A', 'FLEXRAY_0_FR_TXD_B', 'FLEXRAY_0_FR_TXE_A_b'  'FLEXRAY_0_FR_TXE_B_b', 'FLEXTIMER_0_FTM0_CH0_INOUT'  'FLEXTIMER_0_FTM0_CH0_IN', 'FLEXTIMER_0_FTM0_CH0_OUT'  'FLEXTIMER_0_FTM0_CH1_INOUT', 'FLEXTIMER_0_FTM0_CH1← _IN', 'FLEXTIMER_0_FTM0_CH1_OUT', 'FLEXTIMER_0_FTM0← _CH2_INOUT', 'FLEXTIMER_0_FTM0_CH2_IN', 'FLEXTIMER—		_DSPI5_PCS0_OUT', 'DSPI_5_DSPI5_PCS1', 'DSPI_5_DSPI5_PCS2',
DSPI5_SCK_OUT', 'DSPI_5_DSPI5_SIN', 'DSPI_5_DSPI5_SOUT'  'FLEXCAN_0_CAN0_RX', 'FLEXCAN_0_CAN0_TX', 'FLEXCAN_4  1_CAN1_RX', 'FLEXCAN_1_CAN1_TX', 'FLEXCAN_2_CAN2_RX'  'FLEXCAN_2_CAN2_TX', 'FLEXCAN_3_CAN3_RX', 'FLEXCAN_3_  _CAN3_TX', 'FLEXRAY_0_FR_DBG_0', 'FLEXRAY_0_FR_DBG_1'  'FLEXRAY_0_FR_DBG_2', 'FLEXRAY_0_FR_DBG_3', 'FLEXRAY_4  _0_FR_RXD_A', 'FLEXRAY_0_FR_RXD_B', 'FLEXRAY_0_FR_C  TXD_A', 'FLEXRAY_0_FR_TXD_B', 'FLEXRAY_0_FR_TXE_A_b'  'FLEXRAY_0_FR_TXE_B_b', 'FLEXTIMER_0_FTM0_CH0_INOUT'  'FLEXTIMER_0_FTM0_CH0_IN', 'FLEXTIMER_0_FTM0_CH0_OUT'  'FLEXTIMER_0_FTM0_CH1_INOUT', 'FLEXTIMER_0_FTM0_CH1_  _IN', 'FLEXTIMER_0_FTM0_CH1_OUT', 'FLEXTIMER_0_FTM0_CH1_  _CH2_INOUT', 'FLEXTIMER_0_FTM0_CH2_IN', 'FLEXTIMER_6_		'DSPI_5_DSPI5_PCS3', 'DSPI_5_DSPI5_PCS4', 'DSPI_5_DSPI5_SCK',
'FLEXCAN_0_CAN0_RX', 'FLEXCAN_0_CAN0_TX', 'FLEXCAN_← 1_CAN1_RX', 'FLEXCAN_1_CAN1_TX', 'FLEXCAN_2_CAN2_RX' 'FLEXCAN_2_CAN2_TX', 'FLEXCAN_3_CAN3_RX', 'FLEXCAN_3← CAN3_TX', 'FLEXRAY_0_FR_DBG_0', 'FLEXRAY_0_FR_DBG_1' 'FLEXRAY_0_FR_DBG_2', 'FLEXRAY_0_FR_DBG_3', 'FLEXRAY← _0_FR_RXD_A', 'FLEXRAY_0_FR_RXD_B', 'FLEXRAY_0_FR_← TXD_A', 'FLEXRAY_0_FR_TXD_B', 'FLEXRAY_0_FR_TXE_A_b' 'FLEXRAY_0_FR_TXE_B_b', 'FLEXTIMER_0_FTM0_CH0_INOUT' 'FLEXTIMER_0_FTM0_CH0_IN', 'FLEXTIMER_0_FTM0_CH0_OUT' 'FLEXTIMER_0_FTM0_CH1_INOUT', 'FLEXTIMER_0_FTM0_CH1← _IN', 'FLEXTIMER_0_FTM0_CH1_OUT', 'FLEXTIMER_0_FTM0← _CH2_INOUT', 'FLEXTIMER_0_FTM0_CH2_IN', 'FLEXTIMER—		'DSPI_5_DSPI5_SCK_INOUT', 'DSPI_5_DSPI5_SCK_IN', 'DSPI_5↔
1_CAN1_RX', 'FLEXCAN_1_CAN1_TX', 'FLEXCAN_2_CAN2_RX' 'FLEXCAN_2_CAN2_TX', 'FLEXCAN_3_CAN3_RX', 'FLEXCAN_3← _CAN3_TX', 'FLEXRAY_0_FR_DBG_0', 'FLEXRAY_0_FR_DBG_1' 'FLEXRAY_0_FR_DBG_2', 'FLEXRAY_0_FR_DBG_3', 'FLEXRAY← _0_FR_RXD_A', 'FLEXRAY_0_FR_RXD_B', 'FLEXRAY_0_FR_— TXD_A', 'FLEXRAY_0_FR_TXD_B', 'FLEXRAY_0_FR_TXE_A_b' 'FLEXRAY_0_FR_TXE_B_b', 'FLEXTIMER_0_FTM0_CH0_INOUT' 'FLEXTIMER_0_FTM0_CH0_IN', 'FLEXTIMER_0_FTM0_CH0_OUT' 'FLEXTIMER_0_FTM0_CH1_INOUT', 'FLEXTIMER_0_FTM0_CH1← _IN', 'FLEXTIMER_0_FTM0_CH1_OUT', 'FLEXTIMER_0_FTM0← _CH2_INOUT', 'FLEXTIMER_0_FTM0_CH2_IN', 'FLEXTIMER—		
$\label{eq:can2_TX'} \begin{tabular}{lllllllllllllllllllllllllllllllllll$		
$\begin{array}{cccccccccccccccccccccccccccccccccccc$		
$\label{eq:control_control_control} $$ \text{FLEXRAY}\_0\_FR\_DBG\_2', $$ \text{FLEXRAY}\_0\_FR\_DBG\_3', $$ \text{FLEXRAY}\_0\_FR\_RXD\_B', $$ \text{FLEXRAY}\_0\_FR\_C-CTXD\_A', $$ \text{FLEXRAY}\_0\_FR\_TXD\_B', $$ \text{FLEXRAY}\_0\_FR\_TXE\_A\_b', $$ \text{FLEXRAY}\_0\_FR\_TXE\_B\_b', $$ \text{FLEXTIMER}\_0\_FTM0\_CH0\_INOUT', $$ \text{FLEXTIMER}\_0\_FTM0\_CH0\_IN', $$ \text{FLEXTIMER}\_0\_FTM0\_CH0\_OUT', $$ \text{FLEXTIMER}\_0\_FTM0\_CH1\_INOUT', $$ \text{FLEXTIMER}\_0\_FTM0\_CH1\_IN', $$ \text{FLEXTIMER}\_0\_FTM0\_CH1\_OUT', $$ \text{FLEXTIMER}\_0\_FTM0-CH1\_IN', $$ \text{FLEXTIMER}\_0\_FTM0-CH1\_OUT', $$ \text{FLEXTIMER}\_0\_FTM0-CH1\_INOUT', $$ FLE$		
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		
$\label{eq:two_transform} TXD\_A',  'FLEXRAY\_0\_FR\_TXD\_B',  'FLEXRAY\_0\_FR\_TXE\_A\_b' \\  'FLEXRAY\_0\_FR\_TXE\_B\_b',  'FLEXTIMER\_0\_FTM0\_CH0\_INOUT' \\  'FLEXTIMER\_0\_FTM0\_CH0\_IN',  'FLEXTIMER\_0\_FTM0\_CH1\_INOUT',  'FLEXTIMER\_0\_FTM0\_CH1\_INOUT',  'FLEXTIMER\_0\_FTM0\_CH1\_IN',  'FLEXTIMER\_0\_FTM0\_CH1\_OUT',  'FLEXTIMER\_0\_FTM0\_CH2\_IN',  'FLEXTIMER\_0\_TM0\_CH2\_IN',  'FLEXTIMER\_0\_TM0\_TM0\_TM0\_TM0\_TM0\_TM0\_TM0\_TM0\_TM0\_T$		
$\label{eq:control_transform} \begin{array}{llllllllllllllllllllllllllllllllllll$		
$\label{eq:continuou} \begin{tabular}{lllllllllllllllllllllllllllllllllll$		
$\label{eq:control_transform} \begin{array}{lll} \text{'FLEXTIMER\_0\_FTM0\_CH1\_INOUT',} & \text{'FLEXTIMER\_0\_FTM0\_CH1} \\ \text{\_IN',} & \text{'FLEXTIMER\_0\_FTM0\_CH1\_OUT',} & \text{'FLEXTIMER\_0\_FTM0\_CH2\_IN',} & \text{'FLEXTIMER} \\ \text{\_CH2\_INOUT',} & \text{'FLEXTIMER\_0\_FTM0\_CH2\_IN',} & \text{'FLEXTIMER} \\ \end{array}$		
		'FLEXTIMER_0_FTM0_CH1_INOUT', 'FLEXTIMER_0_FTM0_CH1←
		_IN', 'FLEXTIMER_0_FTM0_CH1_OUT', 'FLEXTIMER_0_FTM0↔
		_CH2_INOUT', 'FLEXTIMER_0_FTM0_CH2_IN', 'FLEXTIMER←
		_0_FTM0_CH2_OUT', 'FLEXTIMER_0_FTM0_CH3_INOUT',
'FLEXTIMER 0 FTM0 CH3 IN', 'FLEXTIMER 0 FTM0 CH3 OUT'		'FLEXTIMER 0 FTM0 CH3 IN', 'FLEXTIMER 0 FTM0 CH3 OUT',
	NXP Semiconductors	'FLEXTIMER 32 FOND CHY STORY FLEXTIMER 0 FTM0 CH4
in, i bentimen_o_i i mo_oni_o o i , i bentimen_o_i i mo_ono	TVAT Semiconductors	IN', 'FLEXTIMER_0_FTM0_CH4_OUT', 'FLEXTIMER_0_FTM0_CH5\;\frac{31}{31}

Property	Value
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## 4.25 Parameter PortPinLevelValue

Port Pin Level value from Port pin list.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	PORT_PIN_LEVEL_LOW
literals	['PORT_PIN_LEVEL_HIGH', 'PORT_PIN_LEVEL_LOW', 'PORT_PIN_← LEVEL_NOTCHANGED']

#### 4.26 Parameter PortPinSlewRate

Configure Slew Rate for the configured Pin. This is an implementation specific parameter.

For SIUL2\_0, SIUL2\_1 signals of S32G and SIUL2\_0, SIUL2\_1 signals of S32R, the Slew Rate can be configured to one of the following values:

For "3.3 V/1.8 V" FAST pads:

Fmax=208 MHz (at 1.8V), 166 MHz (at 3.3V)

Fmax=166 MHz (at 1.8V), 150 MHz (at 3.3V)

Fmax=150 MHz (at 1.8V), 133 MHz (at 3.3V)

Fmax=133 MHz(at 1.8V), 100 MHz (at 3.3V)

Fmax=100 MHz (at 1.8V), 83 MHz (at 3.3V)

For "1.8 V" GPIO pads:

Fmax=208 MHz

Fmax=150 MHz

Fmax=133 MHz

Fmax=100 MHz

Fmax=50 MHz

For "3.3 V" GPIO pads:

Fmax=50 MHz

Fmax=1 MHz

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	N/A
literals	['SRE_3_3V_50MHZ_b100', 'SRE_3_3V_50MHZ_b101', 'SRE_3_3V_50\cup MHZ_b110', 'SRE_3_3V_1MHZ', 'SRE_208MHZ_1_8V_166MHZ_3_3V', 'SRE_166MHZ_1_8V_150MHZ_3_3V', 'SRE_150MHZ_1_8V_133MHZ_\cup 3_3V', 'SRE_133MHZ_1_8V_100MHZ_3_3V', 'SRE_100MHZ_1_8V_83\cup MHZ_3_3V', 'SRE_1_8V_208MHZ', 'SRE_1_8V_150MHZ', 'SRE_1_8V\cup 133MHZ', 'SRE_1_8V_100MHZ', 'SRE_1_8V_50MHZ', 'SRE_FASTEST\cup 208MHZ', 'SRE_150MHZ_LOWER', 'SRE_100MHZ_LOWER', 'SRE_50\cup MHZ_LOWER', 'SRE_SLOWEST_25MHZ']

# 4.27 Reference PortPinEcucPartitionRef

Maps the Port pin to zero a multiple ECUC partitions. The ECUC partitions referenced are a subset of the ECUC partitions where the Port driver is mapped to.

Property	Value
type	ECUC-REFERENCE-DEF
origin	AUTOSAR_ECUC
lowerMultiplicity	0
upperMultiplicity	Infinite
postBuildVariantMultiplicity	true

## Tresos Configuration Plug-in

Property	Value
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueConnigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
requires Symbolic Name Value	False
destination	/AUTOSAR/EcucDefs/EcuC/EcucPartitionCollection/EcucPartition

## 4.28 Container UnTouchedPortPin

List containing Pins that will not be touched by Port\_Init() function.

Included subcontainers:

### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE

## 4.29 Parameter PortPinSiul2Instance

Selects one of the SIULs instances available on the platform to configure the current pin from.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE

Property	Value
defaultValue	SIUL2_0
literals	['SIUL2_0', 'SIUL2_1']

## 4.30 Parameter PortPinPcr

Used to specify port configuration register: SIUL I/O Pin Multiplexed Signal Configuration Registers (MSCR number).

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	0
max	190
min	0

## 4.31 Container UntouchedIMCR

List containing IMCR of Pins that will not be touched by Port\_Init() function.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE

## 4.32 Parameter IMCRSiul2Instance

Selects one of the SIULs instances available on the platform to configure the current IMCR.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SIUL2_0
literals	['SIUL2_0', 'SIUL2_1']

## 4.33 Parameter UntouchedPortPinImcr

Selects one of the IMCR will be Untouched

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	0
max	496
min	0

## 4.34 Container PortGeneral

Module wide configuration parameters of the PORT driver.

Included subcontainers:

## • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

## 4.35 Parameter PortDevErrorDetect

Switches the Development Error Detection and Notification ON or OFF.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

## 4.36 Parameter SIUL2PortIPDevErrorDetect

Enables and Disables DevAssert checks in IP code.

True: Enabled.

 ${\bf False:\ Disabled.}$ 

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

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Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

## 4.37 Parameter PortSetPinDirectionApi

Pre-processor switch to enable/disable the use of the function Port\_SetPinDirection().

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

## ${\bf 4.38}\quad {\bf Parameter\ PortSetPinModeApi}$

The function for changing the pin modes is not supported by the safety implementation.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

## 4.39 Parameter PortVersionInfoApi

Pre-processor switch to enable/disable the API to read out the modules version information.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

## ${\bf 4.40} \quad {\bf Parameter~PortSetPinModeDoesNotTouchGpioLevel}$

Pre-processor switch. When not checked, the function Port\_SetPinMode() will set the output level of the pin to the value configured in the PortPinLevelValue combo when called at run time to change mode of a pin from alternate function to GPIO. When checked, the function Port\_SetPinMode() will not touch the output level of the pin when called at run time to change mode of a pin from alternate function to GPIO.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

## 4.41 Parameter PortSetAsUnusedPinApi

The function void Port\_SetAsUnusedPin shall configure the referenced pin with all the properties specified in the NotUsedPortPin container.

### Tresos Configuration Plug-in

The function void Port\_SetAsUsedPin shall configure the referenced pin with all the properties that where set during the Port\_Init operation.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

## 4.42 Parameter PortResetPinModeApi

The function Port\_ResetPinMode shall revert the port pin mode of the referenced pin to the value that was set by Port\_Init operation.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

## ${\bf 4.43} \quad {\bf Parameter\ PortEnable User Mode Support}$

When this parameter is enabled, the Port module will adapt to run from user mode, with the following measures:

- a) configuring REG\_PROT for SIUL2 IP so that the registers under protection can be accessed from user mode by setting UAA bit in REG\_PROT\_GCR to 1
- b) using 'call trusted function' stubs for all internal function calls that access registers requiring supervisor mode.

For more information, please see chapter 5.7 user mode Support in IM

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

## 4.44 Parameter PortMulticoreSupport

This parameter globally enables the possibility to support multicore. If this parameter is enabled, at least one EcucPartition needs to be defined (in all variants).

Note This is an Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

## 4.45 Reference PortEcucPartitionRef

Maps the Port driver to zero a multiple ECUC partitions to make the modules API available in this partition.

Tags: atp.Status=draft

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## Tresos Configuration Plug-in

Property	Value
type	ECUC-REFERENCE-DEF
origin	AUTOSAR_ECUC
lowerMultiplicity	0
upperMultiplicity	Infinite
postBuildVariantMultiplicity	true
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueConnigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
${\it requires Symbolic Name Value}$	False
destination	/AUTOSAR/EcucDefs/EcuC/EcucPartitionCollection/EcucPartition

## 4.46 Container CommonPublishedInformation

Common container, aggregated by all modules. It contains published information about vendor and versions.

Included subcontainers:

### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# ${\bf 4.47} \quad {\bf Parameter} \,\, {\bf ArRelease Major Version}$

Major version number of AUTOSAR specification on which the appropriate implementation is based on.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A

Property	Value
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	4
max	4
min	4

## 4.48 Parameter ArReleaseMinorVersion

Minor version number of AUTOSAR specification on which the appropriate implementation is based on.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	4
max	4
min	4

## 4.49 Parameter ArReleaseRevisionVersion

Revision version number of AUTOSAR specification on which the appropriate implementation is based on.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

## Tresos Configuration Plug-in

Property	Value
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	0
max	0
min	0

## 4.50 Parameter ModuleId

Module ID of this module from Module List.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	124
max	124
min	124

## 4.51 Parameter SwMajorVersion

Major version number of the vendor specific implementation of the module. The numbering is vendor specific.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION

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Property	Value
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	4
max	4
min	4

## 4.52 Parameter SwMinorVersion

Minor version number of the vendor specific implementation of the module. The numbering is vendor specific.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	0
max	0
min	0

## 4.53 Parameter SwPatchVersion

Patch level version number of the vendor specific implementation of the module. The numbering is vendor specific.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	0

### Tresos Configuration Plug-in

Property	Value
max	0
min	0

## 4.54 Parameter VendorApiInfix

In driver modules which can be instantiated several times on a single ECU, BSW00347 requires that the name of APIs is extended by the VendorId and a vendor specific name.

This parameter is used to specify the vendor specific name. In total, the implementation specific name is generated as follows:

E.g. assuming that the VendorId of the implementor is 123 and the implementer chose a VendorApiInfix of "v11r456" a api name Can\_Write defined in the SWS will translate to Can\_123\_v11r456Write.

This parameter is mandatory for all modules with upper multiplicity > 1. It shall not be used for modules with upper multiplicity =1.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	

## 4.55 Parameter VendorId

Vendor ID of the dedicated implementation of this module according to the AUTOSAR vendor list.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false

## Tresos Configuration Plug-in

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	43
max	43
min	43

# **Chapter 5**

## **Module Index**

# 5.1 Software Specification

Here is a list of all modules:

Port HLD	 40
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## **Chapter 6**

## **Module Documentation**

## 6.1 Port HLD

### 6.1.1 Detailed Description

#### Macros

• #define PORT VENDOR ID

Parameters that shall be published within the Port driver header file and also in the module's description file.

• #define PORT\_E\_PARAM\_CONFIG

The PORT module is not properly configured.

• #define PORT\_INSTANCE\_ID

Instance ID of port driver.

• #define PORT INIT ID

API service ID for PORT Init function.

• #define PORT\_SETPINDIRECTION\_ID

API service ID for PORT set pin direction function.

• #define PORT REFRESHPINDIRECTION ID

API service ID for PORT refresh pin direction function.

• #define PORT\_GETVERSIONINFO\_ID

API service ID for PORT get version info function.

• #define PORT\_SETPINMODE\_ID

API service ID for PORT set pin mode.

• #define PORT\_SETASUNUSEDPIN\_ID

API service ID for PORT set as unused pin.

• #define PORT\_SETASUSEDPIN\_ID

API service ID for PORT set as used pin.

• #define PORT\_RESETPINMODE\_ID

API service ID for PORT reset pin mode.

• #define PORT\_E\_PARAM\_PIN

Error ID of port driver.

• #define PORT\_E\_DIRECTION\_UNCHANGEABLE

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Port Pin Direction not configured as changeable.

• #define PORT E INIT FAILED

API Port\_Init() service called with wrong parameter.

• #define PORT\_E\_PARAM\_INVALID\_MODE

API Port\_SetPinMode() service called when mode is invalid.

• #define PORT E MODE UNCHANGEABLE

API Port\_SetPinMode() service called when mode is unchangeable.

• #define PORT\_E\_UNINIT

API service called without module initialization.

• #define PORT E PARAM POINTER

API service called with NULL Pointer Parameter.

### **Function Reference**

void Port\_Init (const Port\_ConfigType \*ConfigPtr)

Port driver initialization function.

• void Port\_SetPinDirection (Port\_PinType Pin, Port\_PinDirectionType Direction)

 $Port\_SetPinDirection.$ 

• void Port\_SetPinMode (Port\_PinType Pin, Port\_PinModeType Mode)

 $Port\_SetPinMode.$ 

• void Port GetVersionInfo (Std VersionInfoType \*versioninfo)

 $Port\_GetVersionInfo.$ 

• void Port\_RefreshPortDirection (void)

 $Port\_RefreshPortDirection.$ 

• void Port\_SetAsUnusedPin (Port\_PinType Pin)

 $Port\_SetAsUnusedPin.$ 

• void Port SetAsUsedPin (Port PinType Pin)

 $Port\_SetAsUsedPin.$ 

• void Port\_ResetPinMode (Port\_PinType Pin)

 $Port\_ResetPinMode.$ 

#### 6.1.2 Macro Definition Documentation

### 6.1.2.1 PORT\_VENDOR\_ID

#define PORT\_VENDOR\_ID

Parameters that shall be published within the Port driver header file and also in the module's description file.

Definition at line 60 of file Port.h.

## 6.1.2.2 PORT\_E\_PARAM\_CONFIG

#define PORT\_E\_PARAM\_CONFIG

The PORT module is not properly configured.

Definition at line 132 of file Port.h.

### 6.1.2.3 PORT\_INSTANCE\_ID

#define PORT\_INSTANCE\_ID

Instance ID of port driver.

Definition at line 139 of file Port.h.

## 6.1.2.4 PORT\_INIT\_ID

#define PORT\_INIT\_ID

API service ID for PORT Init function.

Parameters used when raising an error/exception.

Definition at line 153 of file Port.h.

## 6.1.2.5 PORT\_SETPINDIRECTION\_ID

#define PORT\_SETPINDIRECTION\_ID

API service ID for PORT set pin direction function.

Parameters used when raising an error/exception.

Definition at line 162 of file Port.h.

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S32 PORT Driver

## 6.1.2.6 PORT\_REFRESHPINDIRECTION\_ID

#define PORT\_REFRESHPINDIRECTION\_ID

API service ID for PORT refresh pin direction function.

Parameters used when raising an error/exception.

Definition at line 170 of file Port.h.

## 6.1.2.7 PORT\_GETVERSIONINFO\_ID

#define PORT\_GETVERSIONINFO\_ID

API service ID for PORT get version info function.

Parameters used when raising an error/exception.

Definition at line 179 of file Port.h.

### 6.1.2.8 PORT\_SETPINMODE\_ID

#define PORT\_SETPINMODE\_ID

API service ID for PORT set pin mode.

Parameters used when raising an error/exception.

Definition at line 188 of file Port.h.

### 6.1.2.9 PORT\_SETASUNUSEDPIN\_ID

#define PORT\_SETASUNUSEDPIN\_ID

API service ID for PORT set as unused pin.

Parameters used when raising an error/exception.

Definition at line 194 of file Port.h.

### 6.1.2.10 PORT\_SETASUSEDPIN\_ID

#define PORT\_SETASUSEDPIN\_ID

API service ID for PORT set as used pin.

Parameters used when raising an error/exception.

Definition at line 200 of file Port.h.

### 6.1.2.11 PORT\_RESETPINMODE\_ID

#define PORT\_RESETPINMODE\_ID

API service ID for PORT reset pin mode.

Parameters used when raising an error/exception.

Definition at line 209 of file Port.h.

#### 6.1.2.12 PORT\_E\_PARAM\_PIN

#define PORT\_E\_PARAM\_PIN

Error ID of port driver.

The following errors and exception are detectable by the PORT driver if development error detection is enabled.

Invalid Port Pin ID requested.

Det Error value, returned by Port SetPinDirection and Port PinMode if an wrong PortPin ID is passed.

Definition at line 239 of file Port.h.

### 6.1.2.13 PORT\_E\_DIRECTION\_UNCHANGEABLE

#define PORT\_E\_DIRECTION\_UNCHANGEABLE

Port Pin Direction not configured as changeable.

Det Error value, returned by Port\_SetPinDirection if the passed PortPin have unchangeable direction.

Definition at line 248 of file Port.h.

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### 6.1.2.14 PORT\_E\_INIT\_FAILED

#define PORT\_E\_INIT\_FAILED

API Port Init() service called with wrong parameter.

Det Error value, returned by Port\_Init function if Port\_Init is called with wrong parameter.

Definition at line 258 of file Port.h.

### 6.1.2.15 PORT\_E\_PARAM\_INVALID\_MODE

#define PORT\_E\_PARAM\_INVALID\_MODE

API Port\_SetPinMode() service called when mode is invalid.

Det Error value, returned by Port\_SetPinMode function if the passed PortPinMode is invalid.

Definition at line 267 of file Port.h.

### 6.1.2.16 PORT\_E\_MODE\_UNCHANGEABLE

#define PORT\_E\_MODE\_UNCHANGEABLE

API Port\_SetPinMode() service called when mode is unchangeable.

Det Error value, returned by Port SetPinMode function if the passed PortPin have a unchangeable Mode.

Definition at line 276 of file Port.h.

### 6.1.2.17 PORT\_E\_UNINIT

#define PORT\_E\_UNINIT

API service called without module initialization.

Det Error value, returned by a function if API service called prior to module initialization.

Definition at line 285 of file Port.h.

## 6.1.2.18 PORT\_E\_PARAM\_POINTER

```
#define PORT_E_PARAM_POINTER
```

API service called with NULL Pointer Parameter.

Det Error value, returned by Port\_GetVersionInfo function if API is called with NULL Pointer Parameter.

Definition at line 294 of file Port.h.

## 6.1.3 Function Reference

## 6.1.3.1 Port\_Init()

Port driver initialization function.

Function used for initializing the port driver and for initializing the configured pins.

#### Parameters

in   Port_ConfigType   * ConfigPtr Pointer to configuration (NULL_PTR if only one varian
--

Returns

void

### 6.1.3.2 Port\_SetPinDirection()

 ${\bf Port\_SetPinDirection}.$ 

Function used for changing the pin direction at runtime

Parameters

in

pin id of the pin that needs to change the direction

Parameters

new desired direction IN OUT IN\_OUT

Returns

void

## 6.1.3.3 Port\_SetPinMode()

 $Port\_SetPinMode.$ 

Function used to change the pin mode at runtime.

Parameters



pin id of the pin that needs to change the direction

Parameters



new mode

Returns

void

## 6.1.3.4 Port\_GetVersionInfo()

 ${\bf Port\_GetVersionInfo}.$ 

Function used to read the driver version information

### Parameters

	in	version in fo	pointer to structure that will contain the version information	]
--	----	---------------	--	---

Returns

void

## 6.1.3.5 Port\_RefreshPortDirection()

Port\_RefreshPortDirection.

function used to reset the direction of the pin

Returns

void

## 6.1.3.6 Port\_SetAsUnusedPin()

 ${\bf Port\_SetAsUnusedPin}.$ 

configures the referenced pin with all the properties specified in the NotUsedPortPin container.

Returns

void

#### 6.1.3.7 Port\_SetAsUsedPin()

Port SetAsUsedPin.

configures the referenced pin with all the properties that where set during the Port\_Init operation.

Returns

void

### 6.1.3.8 Port\_ResetPinMode()

Port ResetPinMode.

reverts the port pin mode of the referenced pin to the value that was set by Port\_Init operation.

Returns

void

## 6.2 Port IPL

## 6.2.1 Detailed Description

## **Data Structures**

- struct Siul2\_Port\_Ip\_PortType
- struct Siul2\_Port\_Ip\_PinSettingsConfig

Defines the converter configuration. More...

### Macros

- #define PORT\_PIN\_LEVEL\_NOTCHANGED\_U8

  Not changed port pin logic.

SIUL2 module maximum number of input signal on a pin.

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## Types Reference

 $\bullet \ \ typedef \ uint 8 \ Siul 2\_Port\_Ip\_PortPinsLevel Type$ 

 $\textit{Type of a port levels representation. Implements: } \textit{Siul2\_Port\_Ip\_PortPinsLevelType}.$ 

#### Enum Reference

• enum Siul2\_Port\_Ip\_PortPullConfig

Internal resistor pull feature selection Implements: Siul2\_Port\_Ip\_PortPullConfig.

• enum Siul2\_Port\_Ip\_PortMux

Configures the Pin output muxing selection Implements: Siul2\_Port\_Ip\_PortMux.

• enum Siul2\_Port\_Ip\_PortOutputBuffer

Configures the output buffer enable Implements: Siul2\_Port\_Ip\_PortOutputBuffer.

• enum Siul2\_Port\_Ip\_PortInputBuffer

 $Configures\ the\ Input\ Buffer\ Enable\ field.\ Implements: Siul2\_Port\_Ip\_PortInputBuffer.$ 

• enum Siul2\_Port\_Ip\_PortInputMux

Configures the Pin input muxing selection Implements : Siul2\_Port\_Ip\_PortInputMux.

• enum Siul2 Port Ip PortSafeMode

Configures the Safe Mode Control. Implements: Siul2\_Port\_Ip\_PortSafeMode.

• enum Siul2\_Port\_Ip\_PortSlewRateControl

 $Configures\ the\ slew\ rate\ control.\ Implements: Siul2\_Port\_Ip\_PortSlewRateControl.$ 

• enum Siul2\_Port\_Ip\_PortReceiverSelect

 $Configures\ the\ Receiver\ Select.\ Implements: Siul2\_Port\_Ip\_PortReceiverSelect.$ 

• enum Siul2\_Port\_Ip\_PortOpenDrain

Configures the Open Drain Enable field. Implements: Siul2\_Port\_Ip\_PortOpenDrain.

• enum Siul2\_Port\_Ip\_PortDirectionType

Configures port direction.

### **Function Reference**

• void Siul2\_Port\_Ip\_SetPullSel (Siul2\_Port\_Ip\_PortType \*const base, uint16 pin, Siul2\_Port\_Ip\_PortPullConfig pullConfig)

Configures the internal resistor.

• void Siul2\_Port\_Ip\_SetOutputBuffer (Siul2\_Port\_Ip\_PortType \*const base, uint16 pin, boolean enable, Siul2\_Port\_Ip\_PortMux mux)

Configures the output buffer and output signal.

• void Siul2\_Port\_Ip\_SetInputBuffer (Siul2\_Port\_Ip\_PortType \*const base, uint16 pin, boolean enable, uint32 inputMuxReg, Siul2\_Port\_Ip\_PortInputMux inputMux)

Configures the input buffer and input signal.

• Siul2\_Port\_Ip\_PortStatusType Siul2\_Port\_Ip\_Init (uint32 pinCount, const Siul2\_Port\_Ip\_PinSettingsConfig config[])

Initializes the pins with the given configuration structure.

• void Siul2\_Port\_Ip\_SetPinDirection (Siul2\_Port\_Ip\_PortType \*const base, uint16 pin, Siul2\_Port\_Ip\_PortDirectionType direction)

Configures the pin with the values form the configuration structure.

- uint32 Siul2\_Port\_Ip\_RevertPinConfiguration (const Siul2\_Port\_Ip\_PortType \*const base, uint16 pin)
  - This function configures the pin configuration with the values from the configuration structure.
- void Siul2\_Port\_Ip\_GetPinConfiguration (const Siul2\_Port\_Ip\_PortType \*const base, Siul2\_Port\_Ip\_PinSettingsConfig \*config, uint16 pin)

This function shall return the value of the pin configuration register.

## Variables

• const uint32 Port\_au32Siul2BaseAddr []

Base address array for Siul2 instances.

## 6.2.2 Data Structure Documentation

## 6.2.2.1 struct Siul2\_Port\_Ip\_PortType

PORT - Register Layout Typedef

Definition at line 387 of file Siul2\_Port\_Ip\_Types.h.

## $6.2.2.2 \quad struct \ Siul2\_Port\_Ip\_PinSettingsConfig$

Defines the converter configuration.

This structure is used to configure the pins Implements : Siul2\_Port\_Ip\_PinSettingsConfig

Definition at line 408 of file Siul2\_Port\_Ip\_Types.h.

#### Data Fields

Type	Name	Description
SIUL2_Type *	base	The main SIUL2 base pointer.
uint32	pinPortIdx	Port pin number.
Siul2_Port_Ip_PortPullConfig	pullConfig	Internal resistor pull feature selection.
Siul2_Port_Ip_PortMux	mux	Pin output muxing selection.
Siul2_Port_Ip_PortSafeMode	safeMode	Configures the Safe Mode Control, apply for SIUL2_0/1
Siul2_Port_Ip_PortSlewRateControl	slewRateCtrlSel	Configures the Slew Rate Control field.
$Siul2\_Port\_Ip\_PortReceiverSelect$	receiverSel	Configures the Receiver Select, apply for SIUL2_0/1
Siul2_Port_Ip_PortOpenDrain	openDrain	Configures open drain, apply for SIUL2_0/1
Siul2_Port_Ip_PortOutputBuffer	outputBuffer	Configures the Output Buffer Enable.
Siul2_Port_Ip_PortInputBuffer	inputBuffer	Configures the Input Buffer Enable.
Siul2_Port_Ip_PortInputMux	inputMux[(8U)]	Configures the input muxing
uint32	inputMuxReg[(8U)]	Configures the input muxing register. For the
	S32 PORT Dr	pins controlled by both SIUL2_0 and SIUL2_1 iver instances, refer the note for
NXP Semiconductors		PINS_DRV_SetInputBuffer function 6

## 6.2.3 Macro Definition Documentation

### 6.2.3.1 PORT\_PIN\_LEVEL\_NOTCHANGED\_U8

#define PORT\_PIN\_LEVEL\_NOTCHANGED\_U8

Not changed port pin logic.

Definition at line 166 of file Siul2\_Port\_Ip.h.

### 6.2.3.2 FEATURE\_SIUL2\_MAX\_NUMBER\_OF\_INPUT

#define FEATURE\_SIUL2\_MAX\_NUMBER\_OF\_INPUT

SIUL2 module maximum number of input signal on a pin.

Definition at line 102 of file Siul2 Port Ip Types.h.

## 6.2.4 Types Reference

### 6.2.4.1 Siul2\_Port\_Ip\_PortPinsLevelType

typedef uint8 Siul2\_Port\_Ip\_PortPinsLevelType

 $\label{type of a port levels representation. Implements: Siul2\_Port\_Ip\_PortPinsLevelType.$ 

Definition at line 115 of file Siul2\_Port\_Ip\_Types.h.

## 6.2.5 Enum Reference

## 6.2.5.1 Siul2\_Port\_Ip\_PortPullConfig

enum Siul2\_Port\_Ip\_PortPullConfig

Internal resistor pull feature selection Implements: Siul2\_Port\_Ip\_PortPullConfig.

#### Enumerator

PORT_INTERNAL_PULL_DOWN_ENABLED	internal pull-down resistor is enabled.
PORT_INTERNAL_PULL_UP_ENABLED	internal pull-up resistor is enabled.
PORT_INTERNAL_PULL_NOT_ENABLED	internal pull-down/up resistor is disabled.

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Definition at line 121 of file Siul2\_Port\_Ip\_Types.h.

## $6.2.5.2 \quad Siul2\_Port\_Ip\_PortMux$

enum Siul2\_Port\_Ip\_PortMux

Configures the Pin output muxing selection Implements : Siul2\_Port\_Ip\_PortMux.

#### Enumerator

PORT_MUX_AS_GPIO	corresponding pin is configured as GPIO
PORT_MUX_ALT1	chip-specific
PORT_MUX_ALT2	chip-specific
PORT_MUX_ALT3	chip-specific
PORT_MUX_ALT4	chip-specific
PORT_MUX_ALT5	chip-specific
PORT_MUX_ALT6	chip-specific
PORT_MUX_ALT7	chip-specific

Definition at line 132 of file Siul2\_Port\_Ip\_Types.h.

## $6.2.5.3 \quad Siul2\_Port\_Ip\_PortOutputBuffer$

enum Siul2\_Port\_Ip\_PortOutputBuffer

 $Configures \ the \ output \ buffer \ enable \ Implements: \ Siul2\_Port\_Ip\_PortOutput Buffer.$ 

### Enumerator

PORT_OUTPUT_BUFFER_DISABLED	Output buffer disabled
PORT_OUTPUT_BUFFER_ENABLED	Output buffer enabled

Definition at line 185 of file Siul2\_Port\_Ip\_Types.h.

## ${\bf 6.2.5.4 \quad Siul2\_Port\_Ip\_PortInputBuffer}$

enum Siul2\_Port\_Ip\_PortInputBuffer

 $Configures \ the \ Input \ Buffer \ Enable \ field. \ Implements: Siul2\_Port\_Ip\_PortInput Buffer.$ 

#### Enumerator

PORT_INPUT_BUFFER_DISABLED	Input buffer disabled
PORT_INPUT_BUFFER_ENABLED	Input buffer enabled

Definition at line 195 of file Siul2\_Port\_Ip\_Types.h.

## $6.2.5.5 \quad Siul2\_Port\_Ip\_PortInputMux$

enum Siul2\_Port\_Ip\_PortInputMux

Configures the Pin input muxing selection Implements : Siul2\_Port\_Ip\_PortInputMux.

#### Enumerator

PORT_INPUT_MUX_ALT0	Chip-specific
PORT_INPUT_MUX_ALT1	Chip-specific
PORT_INPUT_MUX_ALT2	Chip-specific
PORT_INPUT_MUX_ALT3	Chip-specific
PORT_INPUT_MUX_ALT4	Chip-specific
PORT_INPUT_MUX_ALT5	Chip-specific
PORT_INPUT_MUX_ALT6	Chip-specific
PORT_INPUT_MUX_ALT7	Chip-specific
PORT_INPUT_MUX_ALT8	Chip-specific
PORT_INPUT_MUX_ALT9	Chip-specific
PORT_INPUT_MUX_ALT10	Chip-specific
PORT_INPUT_MUX_ALT11	Chip-specific
PORT_INPUT_MUX_ALT12	Chip-specific

#### Enumerator

PORT_INPUT_MUX_ALT13	Chip-specific
PORT_INPUT_MUX_ALT14	Chip-specific
PORT_INPUT_MUX_ALT15	Chip-specific
PORT_INPUT_MUX_NO_INIT	No initialization

Definition at line 229 of file Siul2\_Port\_Ip\_Types.h.

## $\bf 6.2.5.6 \quad Siul2\_Port\_Ip\_PortSafeMode$

enum Siul2\_Port\_Ip\_PortSafeMode

 $Configures \ the \ Safe \ Mode \ Control. \ Implements: Siul2\_Port\_Ip\_PortSafe Mode.$ 

#### Enumerator

PORT_SAFE_MODE_DISABLED	To drive pad in hi-z state using $OBE = 0$ , when FCCU in fault state. The OBE will be driven by IP/SIUL when FCCU leaves the fault state.
PORT_SAFE_MODE_ENABLED	No effect on IP/SIUL driven OBE value

Definition at line 256 of file Siul2\_Port\_Ip\_Types.h.

## $6.2.5.7 \quad Siul2\_Port\_Ip\_PortSlewRateControl$

enum Siul2\_Port\_Ip\_PortSlewRateControl

 $Configures \ the \ slew \ rate \ control. \ Implements: Siul2\_Port\_Ip\_PortSlewRateControl.$ 

#### Enumerator

PORT_SLEW_RATE_CONTROL0	Fmax=208 MHz (at 1.8V), 166 MHz (at 3.3V), apply for SIUL2_0/1
PORT_SLEW_RATE_CONTROL4	Fmax=166 MHz (at 1.8V), 150 MHz (at 3.3V, apply for SIUL2_0/1
PORT_SLEW_RATE_CONTROL5	Fmax=150 MHz (at 1.8V), 133 MHz (at 3.3V), apply for SIUL2_0/1
PORT_SLEW_RATE_CONTROL6	Fmax=133 MHz(at 1.8V), 100 MHz (at 3.3V), apply for SIUL2_0/1
PORT_SLEW_RATE_CONTROL7	Fmax=83 MHz (at 1.8V), 63 MHz (at 3.3V), apply for SIUL2_0/1

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Definition at line 286 of file Siul2\_Port\_Ip\_Types.h.

## $6.2.5.8 \quad Siul2\_Port\_Ip\_PortReceiverSelect$

enum Siul2\_Port\_Ip\_PortReceiverSelect

 $Configures \ the \ Receiver \ Select. \ Implements: Siul2\_Port\_Ip\_PortReceiver Select.$ 

#### Enumerator

PORT_RECEIVER_ENABLE_DIFFERENTIAL_VREF	Enables the differential vref based receiver.
PORT_RECEIVER_ENABLE_SINGLE_ENDED	Enables the single ended receiver.

Definition at line 313 of file Siul2\_Port\_Ip\_Types.h.

## $6.2.5.9 \quad Siul2\_Port\_Ip\_PortOpenDrain$

enum Siul2\_Port\_Ip\_PortOpenDrain

Configures the Open Drain Enable field. Implements : Siul2\_Port\_Ip\_PortOpenDrain.

#### Enumerator

PORT_OPEN_DRAIN_DISABLED	Output is CMOS
PORT_OPEN_DRAIN_ENABLED	Output is open drain

Definition at line 373 of file Siul2\_Port\_Ip\_Types.h.

## $\bf 6.2.5.10 \quad Siul2\_Port\_Ip\_PortDirectionType$

enum Siul2\_Port\_Ip\_PortDirectionType

Configures port direction.

#### Enumerator

SIUL2_PORT_IN	Sets port pin as input.	
SIUL2_PORT_OUT	Sets port pin as output.	
SIUL2_PORT_IN_OUT	Sets port pin as bidirectional.	
SIUL2_PORT_HI_Z	Sets port pin as high_z.	river

Definition at line 394 of file Siul2\_Port\_Ip\_Types.h.

## 6.2.6 Function Reference

### 6.2.6.1 Siul2\_Port\_Ip\_SetPullSel()

Configures the internal resistor.

This function configures the internal resistor.

#### Parameters

in	base	Port base pointer (PORTA, PORTB, PORTA_AE, etc.)
in	pin	Port pin number
in	pullConfig	The pull configuration

### 6.2.6.2 Siul2\_Port\_Ip\_SetOutputBuffer()

Configures the output buffer and output signal.

This function configures the output buffer for the pin and the path for output signal from module to pin

#### Parameters

in	base	Port base pointer (PORTA, PORTB, PORTA_AE, etc.)	
in	pin	Port pin number	
in	enable	Enable output buffer	
in	mux	Pin muxing slot selection	

#### 6.2.6.3 Siul2\_Port\_Ip\_SetInputBuffer()

Configures the input buffer and input signal.

This function configures the input buffer for the pin and the path for input signal from pin to module

#### Parameters

in	base	Port base pointer (PORTA, PORTB, PORTA_AE, etc.), NULL if disabling inputMux only	
in	pin	Port pin number	
in	enable	Enable input buffer	
in	input Mux Reg	Pin muxing register slot selection	
in	inputMux	Pin muxing slot selection	

#### Note

: There are some pins controlled by both SIUL2\_0 and SIUL2\_1 instances In order to configure correctly and be consistent with other platforms, the inputMuxReg parameter of SIUL2\_1 instance must be added 512 units. For example: The actual inputMuxReg is 10 then the value there must be (10 + 512)

#### 6.2.6.4 Siul2\_Port\_Ip\_Init()

Initializes the pins with the given configuration structure.

This function configures the pins with the options provided in the provided structure.

#### Parameters

in	pinCount	The number of configured pins in structure
in	config	The configuration structure

#### Returns

The status of the operation

## 6.2.6.5 Siul2\_Port\_Ip\_SetPinDirection()

Configures the pin with the values form the configuration structure.

This function configures the pin configuration with the values form the configuration structure

#### Parameters

in	base	Port base pointer
in	pin	Port pin number
in	direction	The direction of pin

#### Returns

void

## 6.2.6.6 Siul2\_Port\_Ip\_RevertPinConfiguration()

This function configures the pin configuration with the values from the configuration structure.

This function configures the pin configuration with the values from the configuration structure

#### Parameters

in	base	Port base pointer
in	pin	Port pin number

#### Returns

MSCR register value

## 6.2.6.7 Siul2\_Port\_Ip\_GetPinConfiguration()

This function shall return the value of the pin configuration register.

This function shall return the value of the pin configuration register.

#### Parameters

in	base	Port base pointer
in	pin	Port pin number
out	config->pointer	to output configuration structure information

#### Returns

MSCR register value

## 6.2.7 Variable Documentation

### $6.2.7.1 \quad Port\_au32Siul2BaseAddr$

```
const uint32 Port_au32Siul2BaseAddr[] [extern]
```

Base address array for Siul2 instances.

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