# User Manual

for S32 PMIC Driver

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# **Revision History**

Revision	Date	Author	Description
1.0	31.10.2022	NXP AASW Team	Prepared for release S32 RTD AUTOSAR 4.4 Version 4.0.0 Re-
			lease

### Introduction

- Supported Derivatives
- Overview
- About This Manual
- Acronyms and Definitions
- Reference List

This User Manual describes NXP Semiconductor Non-AUTOSAR Pmic for S32CC platform. Non-AUTOSAR Pmic driver configuration parameters and deviations from the specification are described in Driver chapter of this document. Non-AUTOSAR Pmic driver requirements and APIs are described in the Non-AUTOSAR Pmic driver software specification document.

# 2.1 Supported Derivatives

The software described in this document is intended to be used with the following microcontroller devices of NXP Semiconductors:

- s32g274a\_bga525
- s32g254a\_bga525
- s32g233a\_bga525
- $s32g234m\_bga525$
- s32g378a\_bga525
- s32g379a\_bga525
- $s32g398a\_bga525$
- s32g399a\_bga525
- $s32g338m\_bga525$
- s32g339m\_bga525
- s32g358a\_bga525
- s32g359a\_bga525

All of the above microcontroller devices are collectively named as S32.

#### Introduction

### 2.2 Overview

AUTOSAR (AUTomotive Open System ARchitecture) is an industry partnership working to establish standards for software interfaces and software modules for automobile electronic control systems.

#### AUTOSAR:

- paves the way for innovative electronic systems that further improve performance, safety and environmental friendliness.
- is a strong global partnership that creates one common standard: "Cooperate on standards, compete on implementation".
- is a key enabling technology to manage the growing electrics/electronics complexity. It aims to be prepared for the upcoming technologies and to improve cost-efficiency without making any compromise with respect to quality.
- facilitates the exchange and update of software and hardware over the service life of the vehicle.

#### 2.3 About This Manual

This Technical Reference employs the following typographical conventions:

- Boldface style: Used for important terms, notes and warnings.
- *Italic* style: Used for code snippets in the text. Note that C language modifiers such "const" or "volatile" are sometimes omitted to improve readability of the presented code.

Notes and warnings are shown as below:

Note

This is a note.

Warning

This is a warning

# 2.4 Acronyms and Definitions

Term	Definition
API	Application Programming Interface
ASM	Assembler
BSMI	Basic Software Make file Interface
CAN	Controller Area Network
C/CPP	C and C++ Source Code
CS	Chip Select
CTU	Cross Trigger Unit
DEM	Diagnostic Event Manager
DET	Development Error Tracer
DMA	Direct Memory Access
ECU	Electronic Control Unit
FIFO First In First Out	
LSB Least Signifigant Bit	
MCU Micro Controller Unit	
MIDE Multi Integrated Development Environm	
MSB	Most Significant Bit
N/A Not Applicable	
RAM Random Access Memory	
SIU Systems Integration Unit	
SWS Software Specification	
VLE	Variable Length Encoding
XML Extensible Markup Language	

# 2.5 Reference List

#	Title	Version
1	S32G2 Reference Manual	Rev. 5, May 2022
2	S32G3 Reference Manual	Rev. 2 Draft C, June 2022
3	S32G2 Mask Set Errata for Mask 0P77B	Rev. 2.4
4	S32G3 Mask Set Errata for Mask 0P72B	Rev. 1.1
5	S32G2 Data Sheet	Rev. 5, May 2022
6	S32G3 Data Sheet	Rev. 2 Draft B, June 2022
7	VR5510 Data Sheet	Rev. 5, April 2022

## **Driver**

- Requirements
- Driver Design Summary
- Hardware Resources
- Deviations from Requirements
- Driver Limitations
- Driver usage and configuration tips
- Runtime errors
- Symbolic Names Disclaimer

# 3.1 Requirements

For CDD: PMIC is a Complex Device Driver (CDD), so there are no AUTOSAR requirements regarding this module.

It has vendor-specific requirements and implementation.

# 3.2 Driver Design Summary

- The PMIC driver is implemented as an Non-AUTOSAR Complex Device Driver. It provides support for implementing power management control.
- It uses the underlying hardware communication peripherals (e.g. I2C) to access the external registers on PMIC devices.
- The driver offers a hardware independent API to the upper layer that can be used to configure PMIC devices.
- Hardware and software settings can be configured using an AUTOSAR standard configuration tool.
- The driver reports errors to the Diagnostic Event Manager (DEM) and Default Error Tracer (DET) as defined in AUTOSAR.

### 3.3 Hardware Resources

The hardware configured by the PMIC driver is VR5510 revision B1 which is a NXP device power control management.

### 3.4 Deviations from Requirements

The driver deviates from the Non-AUTOSAR Pmic Driver software specification in some places. The table identifies the AUTOSAR requirements that are not fully implemented, implemented differently, not available, not testable or out of scope for the Pmic Driver.

Term	Definition	
N/S	Out of scope	
N/I	Not implemented	
N/F	Not fully implemented	

Below table identifies the AUTOSAR requirements that are not fully implemented, implemented differently, not available, not testable or out of scope for the driver.

Requirement	Status	Description	Notes
Req_Id	N/S	These requirements are not applicable to this specification.	Not a requirement.

### 3.5 Driver Limitations

- 1. Pmic driver does not have all MISRA violations resolved.
- 2. Pmic\_InitDevice function might not work with the Watchdog Window 1ms, 2ms... because the I2c command takes time and then Watchdog will not feed in the open duration. To avoid this problem, user should set Watchdog Window bigger and Watchdog Closed Window Duty Cycle minimum value (31,25%) or disable the Watchdog Window.
- 3. S32G2-RDB2 board does not support the emulation OTP feature.
- 4. Pmic driver does not support I2c asynchronous type because of the competition between I2c interrupt and timer(Gpt) interrupt. Then the watchdog will not trigger in the open state. To ensure safety, the driver just supports I2c synchronous transfer.
- 5. The watchdog is triggered via I2c command, it depends on the I2c speed. When I2c Speed has low speed, the watchdog might not trigger successfully in the watchdog's window open time. To avoid this problem, we recommend that the user should configure I2c with high speed, using a big window period when it is enabled.
- 6. Pmic driver does not support Ip configuration for Non-AUTOSAR applications. However, the user also uses the HLD configuration for Non-AUTOSAR applications by selecting the Non-AUTOSAR mode in the S32DS configuration.

#### Driver

- 7. Pmic driver may not initialize the device successfully in case the fault error counter limit is 2. The user avoids configuring the PmicFaultErrorCounterLimit as MAX 2 value in the configuration tool.
- 8. When a fault is triggered by the MCU via its FCCU pins, the device asserts the FS0B pin if the reaction is configured. Pmic\_ReleaseFs0b() is called, if the FCCU error is always reported in the "Error phase", Pmic\_ReleaseFs0b() will report E\_NOT\_OK without the error signal FS0B. The error signal FS0B might not report because the FS0B\_SNS bit in the FS\_SAFE\_IOS register did not report the state immediately. The process takes more time to update state.

## 3.6 Driver usage and configuration tips

#### Driver usage and configuration tips

This chapter is showcasing how certain features need to be configured/enabled.

- 1. Enable Watchdog by using Pmic to configure OTP fail-safe with device burn OTP without a watchdog.
- 2. If the device enables Watchdog, the user must enable watchdog monitoring in Pmic Configuration as the node PmicOtpConfiguration/PmicOtpConfiguration\_0/PmicOtpFailSafeUnitConfiguration/PmicOtpSafety← IOConfiguration/PmicWatchdogEnable and select the watchdog type according to watchdog OTP.
- 3. Pmic Init() function must be called before another function of the Pmic driver.
- 4. User can emulate OTP Pmic device by Pmic\_EmulateDeviceOTP() API. However, users must ensure the device is in OTP mode. Refer to Pmic VR5510 datasheet to understand this feature.
- 5. User can initialize device by Pmic\_InitDevice() function. This will configure user settings and switch the device to a Normal FS state. Pmic\_InitDevice() function shall not configure any Failsafe register if the device already was Initialized and moved to Normal\_FS state. Eg: If the device was initialized and switched to Normal\_FS in a boot phase, the Pmic\_InitDevice() function will return successfully without any failsafe configuration in the application phase. And if users want to re-configure the device in this case, users should use the Pmic\_GotoInitFS() function to switch the device back to InitFS mode. When Pmic\_GotoInitFS() is called, the watchdog service will be disabled until you call Pmic\_InitDevice(). This way makes sure that the driver can ignore trigger activity while the user is changing the user\_configuration (failsafe register value). To change the configuration, Pmic\_GotoInitFS() must be called and followed by Pmic\_InitDevice(). In case the DIE\_PROCESS feature is enabled, this function will configure SVS if the DIE\_PROCESS OTP of MCU is disabled. Refer to MCU S32G reference manual to check DIE PROCESS OTP bit.
- 6. Pmic\_ReadRegister(), Pmic\_WriteRegister() are used to reading, writing Pmic's register value.
- 7. Pmic\_InitClock will configure the clock of the Pmic device according to the configuration index. The Analog/
  F-out pin will show the frequency of the clock source. But users need to check the AMUX\_FOUT\_OTP bit
  before the calls function. AMUX\_FOUT\_OTP must be FOUT\_MODE.
- 8. Pmic SetMode() will switch the device to the mode according to a configuration index.

- 9. Pmic\_SetAnalogMux() will set analog mux assignment according to a channel configuration index. The Analog/F-out pin will show a voltage of channel mux. But users need to check the AMUX\_FOUT\_OTP bit before the calls function. AMUX\_FOUT\_OTP must be AMUX\_MODE.
- 10. Pmic\_SwitchSVS() will re-configure the static voltage scale (SVS) according to the SVS configuration index. Firstly, this function will switch the device back to InitFS, configure SVS and switch the device to Normal\_FS. In case the DIE\_PROCESS feature is enabled, this function will configure SVS if the DIE\_PROCESS OTP of MCU enables it. It will not configure SVS if the DIE\_PROCESS OTP of MCU is disabled. Refer to Mcu S32G reference manual to check DIE\_PROCESS bit.
- 11. The DIE\_PROCESS feature only supports on S32G2xx devices. S32G3xx will not be available.
- 12. Pmic\_ConfigureWatchdog() will configure the Watchdog Window according to the configuration index. Users must use watchdog\_notification\_task to trigger watchdog when notification is called. The Pmic\_TriggerWatchdog() needs to integrate into the notification task and switch to the new Watchdog Window.
- 13. Pmic\_TriggerWatchdog() should trigger the watchdog of the device. 2 options for watchdog type: Challenge or Simple, refer to Pmic datasheet. In case an external watchdog is used, trigger activity will occur if Pmic\_InitDevice() is already called before. If the Watchdog Window is enabled, this function should integrate into the watchdog notification task service. This way will make sure the synchronous when the driver changes the Watchdog Window setting. If the Watchdog Window is disabled, this trigger activity is controller by the driver.
- 14. Pmic\_DisableWatchdog() will disable watchdog in run time. This function also switches the device back to InitFS, configure the Watchdog Window disabling, and switch the device to Normal-FS. User should ignore the trigger watchdog by watchdog\_notification\_task of Pmic driver in case watchdog window already enabled before you call the Pmic\_DisableWatchdog().
- 15. Pmic\_ReleaseFs0b() is used to release the safety FS0B pin. The API only execute command if the PMIC device is not in the ASSERT\_FS0B state. This function has powerful in case PMIC reacted to assert the FS0B pin and is stuck in the ASSERT\_FS0B state. If users want PMIC to release FS0B and switch to the NORMAL\_FS state.
- 16. Pmic\_GetRawFaultEvents() will get raw fault events from main-unit and fail-safe-unit flag registers.
- 17. Pmic SetReactions() will set reactions when the system events occur.
- 18. Pmic GetDeviceInfo() will get device information.
- 19. Pmic driver supported both AUTOSAR and Non-AUTOSAR. This module has only a 'Pmic' component into S32DS IDE for configuration AUTOSAR and Non-AUTOSAR. Change 'AUTOSAR Mode' or 'Non-AUT← OSAR' on Pmic component according to the user's application type. When the user configures 'AUTOSAR Mode', Pmic component requires to import CDD\_I2c, CDD\_Ocotp, Port, Dio, Det, Dem component. When the user configures 'Non-AUTOSAR Mode', Pmic component requires to import ip component I2c, Ocotp\_Ip, Siul2\_Port, Siul2\_Dio, Det, Dem component. With Non-AUTOSAR case, the driver will call the I2c, Port, Dio and Ocotp Ip API. Users also need to fill data to some fields 'I2C IP Channel Reference, Siul2 instance, I2C SCL Pin reference, Siul2 I2c SCL Pin Mux for using. The project must add the macro definition for using Pmic Non-AUTOSAR.
  - Add the macro 'USE\_IPV\_IIC' to use I2c Ip in the example.
  - Add the macro 'USE\_IPV\_SIUL2' to use Port and Dio Ip in the example.

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- Add the macro 'USE\_IPV\_OCOTP' to use Ocotp Ip in the example. Refer to the Pmic\_Configuration 
   Non\_AUTOSAR\_Example\_S32G274A\_M7, Pmic\_Configuration\_Non\_AUTOSAR\_Example\_←
  S32G399A M7 example to understand how to use Pmic driver Non-AUTOSAR.
- 20. When User\_Mode is enabled in Non-AUTOSAR application, users should set the priority of any to interrupt more than 1. This way will avoid the hard fault handler by any module EXCLUSIVE AREA.
- 21. Recommendations on watchdog triggering and error checking:
  - Given that transfers are slow even at 1Mbit/s (>40us for a write, > 48us for a read), no API should be called from an interrupt context as it will make the system unresponsive for a good chunk of time.
  - Instead, the application software shall log the need for a watchdog trigger or the occurrence of an INTB event in their respective interrupt handlers and defer the "heavy" work to a non-interrupt context (i.e. task-context).
- The priorities of the tasks shall be set in such that the watchdog task could preempt every other task in the system.
- The exclusive areas within Pmic\_ReadRegister and Pmic\_WriteRegister shall be implemented such that the tasks calling any PMIC API will never preempt each other in the middle of a transfer (also applicable for the watchdog/INTB tasks). Interrupts do not necessarily have to be disabled if these are short enough to not interfere with the underlying synchronous communication activity.
- Given the extremely hardware-specific nature of PMICs and to keep the latencies of the communication channels at a minimum, there is no unified error handling interface available in the API. It is the responsibility of the application software to use the Pmic\_GetRawFaultEvents function judiciously.

#### 3.7 Runtime errors

The driver generates the following DEM errors at runtime.

Function	Error Code	Condition triggering the error
Pmic_InitDevice()	PMIC_E_ACESS_FAILURE	Issued when the PMIC device is not accessible.
Pmic_InitDevice()	PMIC_E_TIMEOUT_FAILURE	Issued when the uC/SoC/SiP time- outs while waiting for an event to occur in the PMIC device.
Pmic_InitDevice()	PMIC_E_INTEGRITY_CORR← UPTED	Issued when the PMIC device reports BIST (LBIST/ABIST) or $O \leftarrow$ TP failures.
Pmic_InitDevice()	PMIC_E_SIGNAL_SHORTED	Issued when the PMIC device does not successfully pass the safety signal/path checks.
Pmic_InitClock()	PMIC_E_CLOCK_FAILURE	Issued when the PMIC device reports clock failures (e.g. oscillator drifts, unlocked PLL, etc).
Pmic_SetMode()	PMIC_E_TIMEOUT_FAILURE	Issued when the uC/SoC/SiP time- outs while waiting for an event to occur in the PMIC device.

Function	Error Code	Condition triggering the error
Pmic_SwitchSVS()	PMIC_E_TIMEOUT_FAILURE	Issued when the uC/SoC/SiP time- outs while waiting for an event to occur in the PMIC device.
Pmic_SwitchSVS()	PMIC_E_INTEGRITY_CORR← UPTED	Issued when the PMIC device reports BIST (LBIST/ABIST) or O← TP failures.
Pmic_SwitchSVS()	PMIC_E_SIGNAL_SHORTED	Issued when the PMIC device does not successfully pass the safety signal/path checks.
Pmic_DisableWatchdog()	PMIC_E_TIMEOUT_FAILURE	Issued when the uC/SoC/SiP time- outs while waiting for an event to occur in the PMIC device.
Pmic_DisableWatchdog()	PMIC_E_INTEGRITY_CORR← UPTED	Issued when the PMIC device reports BIST (LBIST/ABIST) or O← TP failures.
Pmic_DisableWatchdog()	PMIC_E_SIGNAL_SHORTED	Issued when the PMIC device does not successfully pass the safety signal/path checks.
All Functions (Except Pmic_Init and Pmic_GetVersionInfo)	PMIC_E_COMM_FAILURE	Issued when the underlying communication fails, e.g. bus blocked or PMIC device not responding.
All Functions (Except Pmic_Init and Pmic_GetVersionInfo)	PMIC_E_INVALID_DATA	When the CRC verification fails on the master-side.

# 3.8 Symbolic Names Disclaimer

All containers having symbolicNameValue set to TRUE in the AUTOSAR schema will generate defines like:

```
\# define < Mip > Conf\_ < Container\_ShortName > \_ < Container\_ID >
```

For this reason it is forbidden to duplicate the names of such containers across the RTD configurations or to use names that may trigger other compile issues (e.g. match existing #ifdefs arguments).

## **Tresos Configuration Plug-in**

This chapter describes the Tresos configuration plug-in for the driver. All the parameters are described below.

- Module Pmic
  - Container PmicGeneralConfiguration
    - \* Parameter PmicDevErrorDetect
    - \* Parameter PmicDisableDemReportErrorStatus
    - \* Parameter PmicTimeoutMechanism
    - \* Parameter PmicTimeoutMethod
    - \* Parameter PmicTimeoutDuration
    - \* Parameter PmicVersionInfoApi
    - \* Parameter PmicDeviceInfoApi
    - \* Parameter PmicSetAnalogMuxApi
    - \* Parameter PmicWatchdogApi
    - \* Parameter PmicOtpEmulationModeApi
    - \* Parameter PmicSwitchSVSApi
    - \* Parameter PmicExternalWatchdog
    - \* Parameter PmicWatchdogTaskNotification
    - \* Parameter PmicDieProcessEnable
    - \* Parameter PmicEnableUserModeSupport
    - \* Reference PmicOcotplink
  - Container PmicGlobalConfig
    - \* Container PmicDevice
      - · Parameter PmicDeviceId
      - · Parameter PmicDeviceMainI2cAddress
      - · Parameter PmicDeviceSafetyI2cAddress
      - · Container PmicOtpConfiguration
      - · Container PmicOtpMainUnitConfiguration
      - · Container PmicOtpDeviceConfiguration
      - · Parameter PmicMainI2cAddress
      - · Parameter PmicVsupLockoutThreshold
      - · Parameter PmicAutoRetryEnable
      - · Parameter PmicAutoRetryTimeout

- · Parameter PmicAutoRetryLimit
- · Parameter PmicPllEnable
- · Parameter PmicClk1Divider
- · Parameter PmicClk2Divider
- · Parameter PmicCenterDieTempThreshold
- · Parameter PmicDeepSleepEnable
- · Container PmicOtpMainIOConfiguration
- · Parameter PmicPwron2GateEnable
- · Parameter PmicAmuxFoutPinMode
- · Parameter PmicPsyncEnable
- · Parameter PmicPsyncMode
- · Parameter PmicPsyncPowerDownControlEnable
- Parameter PmicStandbyTimerEnable
- · Parameter PmicStandbyDischargeThreshold
- · Parameter PmicStandbyPolarity
- · Parameter PmicStandbyPGoodEnable
- Parameter PmicVddioSupplySelect
- · Container PmicOtpPowerSequenceConfiguration
- · Parameter PmicSlotWidth
- · Container PmicVpreRegulator
- · Parameter PmicVpreEnableRegulator
- · Parameter PmicVprePowerupMode
- · Parameter PmicVprePhaseDelay
- · Parameter PmicVpreClockSelect
- · Container PmicBoostRegulator
- · Parameter PmicBoostEnableRegulator
- · Parameter PmicBoostSlotSelect
- · Parameter PmicBoostPhaseDelay
- · Parameter PmicBoostClockSelect
- · Parameter PmicBoostTsdBehavior
- · Container PmicHVLdoRegulator
- · Parameter PmicHVLdoEnableRegulator
- · Parameter PmicHVLdoSequenceControl
- · Parameter PmicHVLdoSlotSelect
- · Parameter PmicHVLdoTsdBehavior
- · Container PmicBuck1Regulator
- · Parameter PmicBuck1EnableRegulator
- · Parameter PmicBuck1SlotSelect
- · Parameter PmicBuck1PhaseDelay
- $\cdot \ \ Parameter \ PmicBuck1ClockSelect$
- · Parameter PmicBuck1TsdBehavior
- · Container PmicBuck2Regulator
- · Parameter PmicBuck2EnableRegulator
- · Parameter PmicBuck2SlotSelect
- · Parameter PmicBuck2PhaseDelay
- · Parameter PmicBuck2ClockSelect
- · Parameter PmicBuck2TsdBehavior

- · Container PmicBuck3Regulator
- · Parameter PmicBuck3EnableRegulator
- · Parameter PmicBuck3SlotSelect
- · Parameter PmicBuck3PhaseDelay
- · Parameter PmicBuck3ClockSelect
- · Parameter PmicBuck3TsdBehavior
- · Container PmicLdo1Regulator
- · Parameter PmicLdo1EnableRegulator
- Parameter PmicLdo1SlotSelect
- · Parameter PmicLdo1TsdBehavior
- · Container PmicLdo2Regulator
- · Parameter PmicLdo2EnableRegulator
- · Parameter PmicLdo2SlotSelect
- · Parameter PmicLdo2TsdBehavior
- · Container PmicLdo3Regulator
- · Parameter PmicLdo3EnableRegulator
- · Parameter PmicLdo3SlotSelect
- · Parameter PmicLdo3TsdBehavior
- · Container PmicOtpRegulatorsConfiguration
- · Container PmicVpreRegulator
- · Parameter PmicVpreOutputVoltage
- · Parameter PmicVpreSlopeCompensation
- · Parameter PmicVpreStdbyVoltageControlEnable
- · Parameter PmicVpreCsaThreshold
- · Parameter PmicVpreHsCurrentCapability
- · Parameter PmicVpreLsCurrentCapability
- · Parameter PmicVpreSoftStartRamp
- · Parameter PmicVpreHsOffTime
- · Parameter PmicVpreHsOnTime
- · Parameter PmicVpreShutdownDelay
- · Container PmicVBoostRegulator
- · Parameter PmicVBoostOutputVoltage
- · Parameter PmicVBoostSlopeCompensation
- · Parameter PmicVBoostLsOnTime
- · Parameter PmicVBoostCurrentLimit
- · Parameter PmicVBoostSlewRate
- · Parameter PmicVBoostCompensationCapacitor
- $\cdot \ \ Parameter \ Pmic VBoost Compensation Resistor$
- · Parameter PmicVBoostToVBos
- · Container PmicBuck1Regulator
- · Parameter PmicBuck1OutputVoltage
- · Parameter PmicBuck1CurrentLimit
- · Parameter PmicBuck1InductorSelect
- · Parameter PmicBuck1Transconductance
- · Parameter PmicBuck1DVSRamp
- · Parameter PmicBuck1PhaseMode
- · Container PmicBuck2Regulator

- · Parameter PmicBuck2OutputVoltage
- · Parameter PmicBuck2CurrentLimit
- · Parameter PmicBuck2InductorSelect
- · Parameter PmicBuck2Transconductance
- · Container PmicBuck3Regulator
- $\cdot \ \ Parameter \ PmicBuck3OutputVoltage$
- · Parameter PmicBuck3CurrentLimit
- · Parameter PmicBuck3InductorSelect
- · Parameter PmicBuck3Transconductance
- $\cdot \ \ Parameter \ Pmic Buck 3 Compensation Resistor$
- · Container PmicLdo1Regulator
- · Parameter PmicLdo1OutputVoltage
- · Parameter PmicLdo1CurrentLimit
- · Container PmicLdo2Regulator
- · Parameter PmicLdo2OutputVoltage
- · Parameter PmicLdo2OperatingMode
- · Container PmicLdo3Regulator
- $\cdot \ \ Parameter \ PmicLdo3OutputVoltage$
- · Parameter PmicLdo3OperatingMode
- · Container PmicHVLdoRegulator
- · Parameter PmicHVLdoOutputVoltage
- · Parameter PmicHVLdoTransitionMode
- · Container PmicOtpFailSafeUnitConfiguration
- · Container PmicOtpSafetyConfiguration
- · Parameter PmicSafetyI2cAddress
- · Parameter PmicRSTBTimerEnable
- · Parameter PmicFaultRecoveryEnable
- · Parameter PmicRstbDelay
- · Parameter PmicSVSLimit
- · Parameter PmicSVSOffsetType
- · Parameter PmicRSTBAssertPGOOD
- · Parameter PmicHVLDOMONMode
- · Parameter PmicLBISTEnable
- · Container PmicOtpSafetyIOConfiguration
- · Parameter PmicWatchdogEnable
- · Parameter PmicWatchdogType
- · Parameter PmicWdiPolarity
- · Parameter PmicFccu1OperatingMode
- · Parameter PmicFccuEnable
- · Parameter PmicStandbyModeEnable
- · Parameter PmicStandbyPolarity
- · Parameter PmicStandbyEntryControl
- · Parameter PmicSafetyStandbyWindowEnable
- · Parameter PmicSafetyWindowInitTimeout
- · Container PmicOtpVoltageMonitorConfiguration
- · Container PmicVcoreMonitor
- · Parameter PmicVcoreEnableMonitor

- · Parameter PmicVcoreMonitorVoltage
- · Parameter PmicVcoreMonitorUVThreshold
- · Parameter PmicVcoreMonitorOVThreshold
- · Parameter PmicVcoreMonitorUVDebounce
- · Parameter PmicVcoreMonitorOVDebounce
- · Parameter PmicVcoreMonitorPGOODAssert
- · Parameter PmicVcoreMonitorABIST1Enable
- · Container PmicVddioMonitor
- · Parameter PmicVddioEnableMonitor
- · Parameter PmicVddioMonitorVoltage
- · Parameter PmicVddioMonitorUVThreshold
- · Parameter PmicVddioMonitorOVThreshold
- · Parameter PmicVddioMonitorUVDebounce
- · Parameter PmicVddioMonitorOVDebounce
- · Parameter PmicVddioMonitorPGOODAssert
- · Parameter PmicVddioMonitorABIST1Enable
- · Container PmicHVLdoMonitor
- · Parameter PmicHVLdoEnableMonitor
- · Parameter PmicHVLdoMonitorVoltage
- · Parameter PmicHVLdoMonitorUVThreshold
- · Parameter PmicHVLdoMonitorOVThreshold
- · Parameter PmicHVLdoMonitorUVDebounce
- $\cdot \ \ Parameter \ PmicHVL do Monitor OV Debounce$
- · Parameter PmicHVLdoMonitorPGOODAssert
- · Parameter PmicHVLdoMonitorABIST1Enable
- · Container PmicVmon1Monitor
- · Parameter PmicVmon1EnableMonitor
- · Parameter PmicVmon1MonitorVoltage
- · Parameter PmicVmon1MonitorUVThreshold
- · Parameter PmicVmon1MonitorOVThreshold
- · Parameter PmicVmon1MonitorUVDebounce
- · Parameter PmicVmon1MonitorOVDebounce
- · Parameter PmicVmon1MonitorPGOODAssert
- · Parameter PmicVmon1MonitorABIST1Enable
- · Container PmicVmon2Monitor
- · Parameter PmicVmon2EnableMonitor
- · Parameter PmicVmon2MonitorVoltage
- · Parameter PmicVmon2MonitorUVThreshold
- · Parameter PmicVmon2MonitorOVThreshold
- $\cdot \ \ Parameter \ Pmic Vmon 2 Monitor UV Debounce$
- · Parameter PmicVmon2MonitorOVDebounce
- · Parameter PmicVmon2MonitorPGOODAssert
- $\cdot \ \ Parameter \ Pmic Vmon 2 Monitor ABIST 1 Enable$
- · Container PmicVmon3Monitor
- · Parameter PmicVmon3EnableMonitor
- · Parameter PmicVmon3MonitorVoltage
- $\cdot \ \ Parameter \ Pmic Vmon 3 Monitor UV Threshold$

- · Parameter PmicVmon3MonitorOVThreshold
- · Parameter PmicVmon3MonitorUVDebounce
- $\cdot \ \ Parameter \ Pmic Vmon 3 Monitor OV Debounce$
- · Parameter PmicVmon3MonitorPGOODAssert
- · Parameter PmicVmon3MonitorABIST1Enable
- · Container PmicVmon4Monitor
- · Parameter PmicVmon4EnableMonitor
- · Parameter PmicVmon4MonitorVoltage
- · Parameter PmicVmon4MonitorUVThreshold
- · Parameter PmicVmon4MonitorOVThreshold
- · Parameter PmicVmon4MonitorUVDebounce
- · Parameter PmicVmon4MonitorOVDebounce
- · Parameter PmicVmon4MonitorPGOODAssert
- $\cdot \ \ Parameter \ Pmic Vmon 4 Monitor ABIST 1 Enable$
- · Container PmicCommunicationConfiguration
- · Parameter PmicI2cCommunicationMethod
- · Reference PmicI2cChannelRef
- · Reference PmicI2CSCLPinRef
- · Reference PmicI2CSCLDioRef
- · Container PmicClockSettingConfig
- · Parameter PmicClockSettingId
- · Parameter PmicIrcoscFrequencyHz
- · Parameter PmicLowPowerOscFrequencyHz
- · Parameter PmicFinEnable
- · Parameter PmicExternalPIN Fin FrequencyHz
- · Parameter PmicPllClockSelection
- · Parameter PmicSpectrumModulationEnable
- · Parameter PmicTriangularCarrierFrequencyHz
- · Parameter PmicFoutMuxSelection
- · Parameter PmicFoutClockSelection
- · Parameter PmicFoutPhaseDelay
- · Parameter PmicClk1Frequency
- · Parameter PmicClk2Frequency
- · Container PmicClockReferencePoint
- · Parameter PmicClockFrequencySelect
- $\cdot \ \ Parameter \ PmicClockReferencePointFrequency$
- · Container PmicModeSettingConf
- · Parameter PmicModeID
- · Parameter PmicModeSelection
- · Parameter PmicPWRON2DeepSleepModeEnable
- · Parameter PmicPWRON1WakeUpEnable
- $\cdot \ \ Parameter \ Pmic PWRON 2 Wake Up Enable$
- · Parameter PmicStandbyTimerEnable
- · Parameter PmicStandbyTimerWindowDuration
- · Container PmicRegulatorsConfiguration
- · Container PmicVpreRegulator
- · Parameter PmicVpreEnableRegulator

- · Parameter PmicVpreStandbyOutputVoltage
- · Parameter PmicVpreHsCurrentCapability
- · Parameter PmicVpreLsCurrentCapability
- · Container PmicVBoostRegulator
- · Parameter PmicBoostEnableRegulator
- · Parameter PmicBoostSlewRate
- · Container PmicHVLdoRegulator
- · Parameter PmicHVLdoEnableRegulator
- · Parameter PmicHVLdoStandbyEnableRegulator
- · Container PmicBuck1Regulator
- · Parameter PmicBuck1EnableRegulator
- · Parameter PmicBuck1StandbyEnableRegulator
- · Parameter PmicBuck1StandbyOutputVoltage
- · Container PmicBuck2Regulator
- · Parameter PmicBuck2EnableRegulator
- · Parameter PmicBuck2StandbyEnableRegulator
- · Container PmicBuck3Regulator
- · Parameter PmicBuck3EnableRegulator
- $\cdot \ \ Parameter \ Pmic Buck 3 Standby Enable Regulator$
- · Container PmicLdo1Regulator
- · Parameter PmicLdo1EnableRegulator
- $\cdot$  Parameter PmicLdo1StandbyEnableRegulator
- · Container PmicLdo2Regulator
- · Parameter PmicLdo2EnableRegulator
- · Parameter PmicLdo2StandbyEnableRegulator
- · Container PmicLdo3Regulator
- · Parameter PmicLdo3EnableRegulator
- $\cdot \ \ Parameter \ PmicLdo 3 Standby Enable Regulator$
- · Container PmicVMONConfiguration
- · Parameter PmicVMON4RegulatorAssignment
- · Parameter PmicVMON3RegulatorAssignment
- · Parameter PmicVMON2RegulatorAssignment
- · Parameter PmicVMON1RegulatorAssignment
- · Container PmicReactionsSettingConf
- · Parameter PmicReactionsSettingId
- · Container PmicMainUnitReactionsConf
- · Container PmicMainInterruptMasks
- · Parameter PmicHvldoOverCurrentIntDisable
- $\cdot \ \ Parameter \ PmicBuck1OverCurrentIntDisable$
- $\cdot \ \ Parameter \ PmicBuck 2 Over Current Int Disable$
- · Parameter PmicBuck3OverCurrentIntDisable
- · Parameter PmicLdo1OverCurrentIntDisable
- $\cdot \ \ Parameter \ PmicLdo 2 Over Current Int Disable$
- · Parameter PmicLdo3OverCurrentIntDisable
- · Parameter PmicHvldoTempShutdownIntDisable
- $\cdot \ \ Parameter \ PmicBoostTempShutdownIntDisable$
- · Parameter PmicBuck1TempShutdownIntDisable

- · Parameter PmicBuck2TempShutdownIntDisable
- · Parameter PmicBuck3TempShutdownIntDisable
- · Parameter PmicLdo1TempShutdownIntDisable
- · Parameter PmicLdo2TempShutdownIntDisable
- · Parameter PmicLdo3TempShutdownIntDisable
- · Parameter PmicCenterDieTempIntDisable
- $\cdot \ \ Parameter \ Pmic Communication Error Int Disable$
- · Parameter PmicBosUndervoltageHighIntDisable
- · Parameter PmicBoostUndervoltageHighIntDisable
- · Parameter PmicBoostOvervoltageHighIntDisable
- · Parameter PmicBistTempShutdownIntDisable
- $\cdot \ \ Parameter \ PmicHvldoInputUndervoltageLowIntDisable$
- · Parameter PmicVpreOvervoltageIntDisable
- · Parameter PmicVpreOvercurrentIntDisable
- $\cdot \ \ Parameter \ Pmic Vpre Undervoltage Low Int Disable$
- $\cdot \ \ Parameter \ Pmic Vpre Undervoltage High Int Disable$
- $\cdot \ \ Parameter \ Pmic V sup Undervoltage 7 V Int Disable$
- $\cdot \ \ Parameter \ Pmic V sup Undervoltage Low Int Disable$
- $\cdot \ \ Parameter \ Pmic V sup Undervoltage High Int Disable$
- · Parameter PmicPwron2TransitionIntDisable
- · Parameter PmicPwron1TransitionIntDisable
- · Container PmicMainThermalShutdownBehaviors
- · Parameter PmicCenterDieTempThreshold
- · Parameter PmicBoostTsdBehavior
- · Parameter PmicBuck1TsdBehavior
- · Parameter PmicBuck2TsdBehavior
- · Parameter PmicBuck3TsdBehavior
- · Parameter PmicLdo1TsdBehavior
- · Parameter PmicLdo2TsdBehavior
- · Parameter PmicLdo3TsdBehavior
- · Parameter PmicLHVLdoTsdBehavior
- · Container PmicFailSafeUnitReactionsConf
- · Container PmicFailSafeInterruptMasks
- $\cdot \ \ Parameter \ Pmic Vmon 4 Over Under Voltage Int Disable$
- $\cdot \quad Parameter \ Pmic Vmon 3 Over Under Voltage Int Disable$
- $\cdot \quad Parameter \ Pmic Vmon 2 Over Under Voltage Int Disable$
- $\cdot \ \ Parameter \ Pmic Vmon 1 Over Under Voltage Int Disable$
- $\cdot \ \ Parameter \ Pmic Vddio Over Under Voltage Int Disable$
- $\cdot \quad Parameter \ Pmic V coremon Over Under Voltage Int Disable \\$
- $\cdot \ \ Parameter \ PmicWatchdogBadRefreshIntDisable$
- $\cdot \ \ Parameter \ PmicHvldoOverUnderVoltageIntDisable$
- · Parameter PmicFccu2EventIntDisable
- · Parameter PmicFccu1EventIntDisable
- · Container PmicAMUXConfiguration
- · Parameter PmicSetAnalogMuxApi
- · Container PmicAmuxChannel
- · Parameter PmicAmuxChannelId

- · Parameter PmicAmuxChannelSelect
- · Parameter PmicAmuxRatio
- · Container PmicFailSafeConfiguration
- · Container PmicSVSConfiguration
- · Parameter PmicSwitchSVSApi
- · Parameter PmicSVSOffset
- · Parameter PmicSVSOffsetSign
- · Parameter PmicBuck1SVSOutputVoltage
- · Container PmicSVSSettingConf
- · Parameter PmicSVSSettingId
- · Parameter PmicSVSOffsetSetting
- · Parameter PmicSVSOffsetSignSetting
- · Parameter PmicBuck1SVSOutputVoltageSetting
- · Container PmicFailSafePinReactions
- $\cdot \ \ Parameter \ Pmic V coremon Overvoltage Impact$
- · Parameter PmicVcoremonUndervoltageImpact
- · Parameter PmicHvldoOvervoltageImpact
- $\cdot \ \ Parameter \ PmicHvldoUndervoltageImpact$
- · Parameter PmicVddioOvervoltageImpact
- · Parameter PmicVddioUndervoltageImpact
- · Parameter PmicVmon4OvervoltageImpact
- · Parameter PmicVmon4UndervoltageImpact
- · Parameter PmicVmon3OvervoltageImpact
- · Parameter PmicVmon3UndervoltageImpact
- $\cdot \ \ Parameter \ Pmic Vmon 2 Overvoltage Impact$
- · Parameter PmicVmon2UndervoltageImpact
- $\cdot \ \ Parameter \ Pmic Vmon 1 Overvoltage Impact$
- · Parameter PmicVmon1UndervoltageImpact
- · Container PmicWatchdogConfiguration
- · Parameter PmicWatchdogApi
- · Parameter PmicWatchdogErrorCounterLimit
- · Parameter PmicWatchdogRefreshCounterLimit
- · Parameter PmicWatchdogErrorImpact
- $\cdot \ \ Parameter \ PmicWatchdogWindowPeriodEnable$
- $\cdot$  Parameter PmicWatchdogWindowPeriod\_Setting
- $\cdot \ \, {\bf Parameter} \, \, {\bf PmicWatchdogClosedWindowDutyCycle\_Setting} \, \,$
- $\cdot \ \ Parameter \ PmicWatchdogRecoveryWindowPeriod$
- · Parameter PmicWatchdogSeed
- · Container PmicWatchdogSettingConf
- · Parameter PmicWatchdogSettingId
- · Parameter PmicWatchdogWindowPeriod
- $\cdot \ \ Parameter \ PmicWatchdogClosedWindowDutyCycle$
- · Container PmicABIST2Configuration
- · Parameter PmicHVLdoMonitorABIST2Enable
- · Parameter PmicVcoreMonitorABIST2Enable
- · Parameter PmicVddioMonitorABIST2Enable
- · Parameter PmicVmon1MonitorABIST2Enable

- · Parameter PmicVmon2MonitorABIST2Enable
- · Parameter PmicVmon3MonitorABIST2Enable
- · Parameter PmicVmon4MonitorABIST2Enable
- · Container PmicSafeInputsConfiguration
- · Parameter PmicSafetyStandbyWindowDuration
- · Parameter PmicFccuMonitoringConfiguration
- · Parameter PmicFccu12FaultPolarity
- · Parameter PmicFccu12FaultImpact
- · Parameter PmicFccu1FaultPolarity
- · Parameter PmicFccu1FaultImpact
- · Parameter PmicFccu2FaultPolarity
- · Parameter PmicFccu2FaultImpact
- · Container PmicStateMachineConfiguration
- · Parameter PmicFaultErrorCounterLimit
- · Parameter PmicFaultErrorCounterImpact
- · Parameter PmicResetDuration
- · Parameter PmicBackupSafetyPath
- · Parameter PmicClockMonitoringEnable
- · Parameter PmicRSTBTimerEnable
- · Parameter PmicLowPowerClockMonitoringEnable
- \* Container PmicDemEventParameterRefs
  - · Reference PMIC E ACESS FAILURE
  - · Reference PMIC E INTEGRITY CORRUPTED
  - · Reference PMIC E SIGNAL SHORTED
  - · Reference PMIC E CLOCK FAILURE
  - · Reference PMIC\_E\_TIMEOUT\_FAILURE
- Container CommonPublishedInformation
  - \* Parameter ArReleaseMajorVersion
  - \* Parameter ArReleaseMinorVersion
  - \* Parameter ArReleaseRevisionVersion
  - \* Parameter ModuleId
  - \* Parameter SwMajorVersion
  - \* Parameter SwMinorVersion
  - \* Parameter SwPatchVersion
  - \* Parameter VendorApiInfix
  - \* Parameter VendorId

### 4.1 Module Pmic

Configuration of the Power Management Integrated Circuit (PMIC) module.

Included containers:

- PmicGeneralConfiguration
- PmicGlobalConfig
- CommonPublishedInformation

Property	Value
type	ECUC-MODULE-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantSupport	true
supportedConfigVariants	VARIANT-POST-BUILD, VARIANT-PRE-COMPILE

# 4.2 Container PmicGeneralConfiguration

This container contains the global configuration parameters of the Non-Autosar PMIC driver.

Note: Implementation Specific Parameter.

Included subcontainers:

### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

## 4.3 Parameter PmicDevErrorDetect

Pre-processor switch for enabling the default error detection and reporting to the DET.

This field shall switch the Default Error Tracer (DET) detection and notification ON or OFF.

The detection of default errors is configurable (ON/OFF) at precompile time.

#define PMIC\_DEV\_ERROR\_DETECT (STD\_ON)/(STD\_OFF) will be generated in Pmic\_Cfg.h file.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueCollingClasses	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	true

# 4.4 Parameter PmicDisableDemReportErrorStatus

Enable/Disable the API for reporting the Dem Error.

 $\# define\ PMIC\_DISABLE\_DEM\_REPORT\_ERROR\_STATUS\ (STD\_OFF)/(STD\_ON)\ will\ be\ generated\ in\ Pmic\_Cfg.h\ file.$ 

STD\_ON will be applied if PmicDisableDemReportErrorStatus is true or PmicDemEventParameterRefs is not enabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

## 4.5 Parameter PmicTimeoutMechanism

This parameter is used to select between two different timeout mechanisms.

When PmicTimeoutMechanism = LOOPS, the driver will use loop counting for timeouts

and the maximum number of iterations will be given by the PmicTimeoutDuration parameter.

 $\# define\ PMIC\_TIMEOUT\_MECHANISM\_LOOPS\ (STD\_OFF)/(STD\_ON)\ will\ be\ generated\ in\ Pmic\_Cfg.h$  file.

When PmicTimeoutMechanism = TICKS, the driver will use the Time Service module for deterministic

timeouts and the maximum number of microseconds will be given by the PmicTimeoutDuration parameter.

Internally, it is using the 1us32bit set of API services.

 $\# define\ PMIC\_TIMEOUT\_MECHANISM\_TICKS\ (STD\_OFF)/(STD\_ON)\ will\ be\ generated\ in\ Pmic\_Cfg.h$  file.

Note: The latter choice generates an additional dependency.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	LOOPS
literals	['LOOPS', 'TICKS']

#### 4.6 Parameter PmicTimeoutMethod

Vendor specific: Counter type used in timeout .

Based on selected counter type the timeout value will be interpreted as follows:

OSIF\_COUNTER\_SYSTEM - Use system counter.

 $\operatorname{OSIF} \_\operatorname{COUNTER} \_\operatorname{CUSTOM}$  - Use custom counter.

OSIF\_COUNTER\_DUMMY - Use dummy counter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
${\it symbolic} Name Value$	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	OSIF_COUNTER_SYSTEM
literals	['OSIF_COUNTER_SYSTEM', 'OSIF_COUNTER_CUSTOM', 'OSIF_CO← UNTER_DUMMY']

## 4.7 Parameter PmicTimeoutDuration

When PmicTimeoutMechanism = LOOPS, the unit of measurement is given in number of iterations.

When PmicTimeoutMechanism = TICKS, the unit of measurement is given in number of microseconds.

Please take the above into consideration when choosing the value for this parameter.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
${\it symbolic} Name Value$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
rolus ConferClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	50000
max	4294967295
min	1

# 4.8 Parameter PmicVersionInfoApi

Pre-processor switch to enable/disable the API to read out the modules version information (Pmic\_GetVersionInfo).

#define PMIC\_VERSION\_INFO\_API (STD\_ON)/(STD\_OFF) will be generated in Pmic\_Cfg.h file.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

# 4.9 Parameter PmicDeviceInfoApi

Pre-processor switch to enable/disable the API to read out the device information (Pmic\_GetDeviceInfo).

#define PMIC\_DEVICE\_INFO\_API (STD\_ON)/(STD\_OFF) will be generated in Pmic\_Cfg.h file.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

# 4.10 Parameter PmicSetAnalogMuxApi

Pre-processor switch to enable/disable the API to set the analog multiplexer (AMUX) pin.

#define PMIC\_SET\_ANALOG\_MUX\_API (STD\_ON)/(STD\_OFF) will be generated in Pmic\_Cfg.h file.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

# 4.11 Parameter PmicWatchdogApi

Pre-processor switch to enable/disable the Watchdog API.

#define PMIC\_WATCHDOG\_API (STD\_ON)/(STD\_OFF) will be generated in CDD\_Pmic\_Cfg.h file.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

# 4.12 Parameter PmicOtpEmulationModeApi

Pre-processor switch to enable/disable the OTP Emulation Mode API.

 $\# define\ PMIC\_OTP\_EMULATION\_MODE\_API\ (STD\_ON)/(STD\_OFF)\ will\ be\ generated\ in\ CDD\_Pmic\_Cfg.h$  file.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

# 4.13 Parameter PmicSwitchSVSApi

API shall re-configure static voltage scaler (SVS) after device was initialized.

In case DIE\_PROCESS feature is enable, this function will configure SVS if the DIE\_PROCESS otp of mcu enables.

It will not configure SVS if the DIE\_PROCESS otp of mcu disable. Refer Mcu reference manual to check DIE\_PROCESS bit.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

## 4.14 Parameter PmicExternalWatchdog

External watchdog - true if external watchdog is used (Wdg\_43\_VR5510), all other watchdog settings in this driver will be ignored.

The driver will assume that the application is using an external watchdog driver instead of directly calling the 'Pmic\_TriggerWatchdog' API.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

# 4.15 Parameter PmicWatchdogTaskNotification

Function name of callback. This function will be called when watchdog task is required and watchdog window is not DISABLE option.

If this notification is enabled, the driver will assume that the application will service the external watchdog

by directly calling the 'Pmic\_TriggerWatchdog' API.

Note: The notification can only be enabled if the Watchdog API is provided. (i.e. PmicGeneralConfiguration/PmicWatchdogAp = 'true').

Note: Implementation Specific Parameter.

NXP Semicondu

Property	Value
type	ECUC-FUNCTION-NAME-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
ectors S	32/ PRIAN TOPOST-BUILD: PRE-COMPILE
defaultValue	NULL PTR

## 4.16 Parameter PmicDieProcessEnable

This node allow to enable/disable the checking DIE\_PROCESS of MCU before setting static voltage scaler (SVS).

#define PMIC\_DIE\_PROCESS\_ENABLE (STD\_ON)/(STD\_OFF) will be generated in Pmic\_Cfg.h file.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolic} Name Value$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

# ${\bf 4.17} \quad {\bf Parameter} \ {\bf PmicEnableUserModeSupport}$

Enable/Disable user mode support.

True: Enabled

False: Disabled

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

# 4.18 Reference PmicOcotplink

Reference to the Ocotp channel configuration used to check the die\_process of MCU.

Ocotp Channel must be configured the eFuse word as OCOTP\_BANK0\_WORD6

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigCiasses	VARIANT-PRE-COMPILE: PRE-COMPILE
${\it requires Symbolic Name Value}$	true
destination	/AUTOSAR/EcucDefs/Ocotp/OcotpChannelList/OcotpChannel

## 4.19 Container PmicGlobalConfig

This container contains the global configuration parameter of the PMIC driver. This container is a MultipleConfigurationConta i.e. this container and its sub-containers exist once per configuration set.

Included subcontainers:

- PmicDevice
- PmicDemEventParameterRefs

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

## 4.20 Container PmicDevice

This container contains the configuration parameters of a particular PMIC device.

Note: "Users shall use unique names for naming the PMIC devices."

Included subcontainers:

- $\bullet \ \ PmicOtpConfiguration$
- $\bullet \ \ Pmic Communication Configuration$
- $\bullet \ \ PmicClockSettingConfig$
- $\bullet \ \ PmicModeSettingConf$
- $\bullet \ \ PmicReactionsSettingConf$
- $\bullet \ \ Pmic AMUX Configuration$
- $\bullet \ \ Pmic Fail Safe Configuration$

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE

## 4.21 Parameter PmicDeviceId

Identifies the PMIC device.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	true
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	1
max	255
min	0

# 4.22 Parameter PmicDeviceMainI2cAddress

The Main I2C address of the device.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	A_0x20
literals	['A_0x20', 'A_0x22', 'A_0x24', 'A_0x26', 'A_0x28', 'A_0x2A', 'A_0x2C', 'A \( \) _0x2E', 'A_0x30', 'A_0x32', 'A_0x34', 'A_0x36', 'A_0x38', 'A_0x3A', 'A_ \( \) _0x3C', 'A_0x3E']

# ${\bf 4.23}\quad {\bf Parameter\ PmicDeviceSafetyI2cAddress}$

The Fail-Safe Unit I2C address of the device.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	A_0x21
literals	

# 4.24 Container PmicOtpConfiguration

This container contains the configuration parameters for the OTP registers.

Note: Implementation Specific Parameter.

Included subcontainers:

- PmicOtpMainUnitConfiguration
- PmicOtpFailSafeUnitConfiguration

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE

# 4.25 Container PmicOtpMainUnitConfiguration

This container contains the configuration parameters for the OTP registers on the Main Unit.

Note: Implementation Specific Parameter.

Included subcontainers:

- $\bullet \ \ PmicOtpDeviceConfiguration$
- $\bullet \ \ PmicOtp Main IO Configuration$
- $\bullet \ \ PmicOtpPowerSequenceConfiguration$
- PmicOtpRegulatorsConfiguration

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# ${\bf 4.26}\quad {\bf Container\ PmicOtpDeviceConfiguration}$

This container contains the configuration parameters for the general device configuration of the Main Unit.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

## 4.27 Parameter PmicMainI2cAddress

Configures the I2C address of the Main Unit (I2CDEVADDR\_OTP[3:0]).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	A_0x20
literals	

### 4.28 Parameter PmicVsupLockoutThreshold

Configures the under-voltage low and high thresholds of the VSUP (VSUPCFG OTP).

It is imperative that VSUP > VSUP\_UVH for the device to start.

When VSUP < VSUP UVL, the device stops operation, disables HVLDO, and goes

directly to OFF mode without the proper power down sequence.

 $LOW_VOLTAGE_THRESHOLD - VSUP_UVL = 4.2V...4.4V$  and  $VSUP_UVH = 4.7V...5.1V$ 

HIGH\_VOLTAGE\_THRESHOLD - VSUP\_UVL = 5.3V...5.7V and VSUP\_UVH = 6.0V...6.4V.

Legend:

VSUP UVL - VSUP under-voltage threshold low (during power-up and VSUP falling)

VSUP\_UVH - VSUP under-voltage threshold high (during power-up and VSUP rising)

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	LOW_VOLTAGE_THRESHOLD
literals	['LOW_VOLTAGE_THRESHOLD', 'HIGH_VOLTAGE_THRESHOLD']

## 4.29 Parameter PmicAutoRetryEnable

This field is used to enable/disable the autoretry feature mechanism used to exit from the DEEP-FS (Deep Fail-Safe) mode (AUTORETRY\_EN\_OTP).

In case of VPRE\_FB\_OV detection, or TSD detection on a regulator (if configured), or DFS request from the FS (Fail-Safe) State Machine,

the device will stop and go directly to DEEP-FS mode without the proper power down sequence.

#### 0 - AUTORETRY is Disabled

### 1 - AUTORETRY is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

# ${\bf 4.30}\quad {\bf Parameter\ Pmic Auto Retry Time out}$

Configures the autoretry timeout (AUTORETRY\_TIMEOUT\_OTP).

Exit of DEEP-FS (Deep Fail-Safe) mode is only possible by PWRON1 = 0 or after either

4s or 100ms (the choice depending on the configuration of this field) if the autoretry

feature is activated.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TIME_4S
literals	['TIME_4S', 'TIME_100MS']

# 4.31 Parameter PmicAutoRetryLimit

Configures the autoretry limit (AUTORETRY\_INFINITE\_OTP).

The number of autoretries can be limited to 15 or infinite (the choice depending on the configuration of this field).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	NO_LIMIT
literals	['TIMES_15_LIMIT', 'NO_LIMIT']

## 4.32 Parameter PmicPllEnable

This field is used to enable/disable the PLL of the Main Unit (PLL\_SEL\_OTP).

0 - PLL is Disabled

1 - PLL is Enabled

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue S	32 PMIC Driver NX

# 4.33 Parameter PmicClk1Divider

Configures the CLK1 divider of the Main Unit (CLK\_DIV1\_OTP[1:0]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	DIV_9
literals	['DIV_9', 'DIV_8']

### 4.34 Parameter PmicClk2Divider

Configures the CLK2 divider of the Main Unit (CLK\_DIV2\_OTP[2:0]).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	DIV_44
literals	['DIV_8', 'DIV_10', 'DIV_44']

### 4.35 Parameter PmicCenterDieTempThreshold

Configures the center die temperature threshold (DIE CENTER TEMP OTP[2:0]).

A thermal sensor is placed on the center of the die (device) which is used to generate interrupts for the MCU whenever the temperature exceeds the configured threshold.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TEMP_105_oC
literals	['TEMP_75_oC', 'TEMP_90_oC', 'TEMP_105_oC', 'TEMP_120_oC', 'TEMP_135_oC', 'TEMP_150_oC']

# 4.36 Parameter PmicDeepSleepEnable

This field is used to enable/disable the Deep Sleep Mode of the Main Unit (DSM EN OTP).

- 0 DSM (Deep Sleep Mode) is Disabled
- 1 DSM (Deep Sleep Mode) is Enabled

When transitioning to DSM, the device goes through the proper power down sequence set by OTP to reach the deep sleep state where only the HVLDO is kept alive.

The DSM shuts down most of the device, except allows the HVLDO to be in the LDO mode if it is programmed to operate in Deep Sleep. The PWRON2 input detector is active in Deep Sleep and can trigger a turn-on event.

When DSM is enabled, the PWRON2 pin can be programmed to be used to transition to DSM from NORMAL\_M.

Warning: Only the PWRON2 input detector is alive during DSM, so only this pin can be used to exit from DSM.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

# 4.37 Container PmicOtpMainIOConfiguration

This container contains the configuration parameters for the I/O capabilities of the Main Unit.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

### 4.38 Parameter PmicPwron2GateEnable

Configures the impact of the PWRON2 on the logic that controls turning on and turning off the regulators (PWRON2\_GATE\_EN\_OTP).

- 0 PWRON2 Gate is Disabled (PWRON2 is NOT required for PWRUP)
- 1 PWRON2 Gate is Enabled (PWRON2 is required for PWRUP)

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

### 4.39 Parameter PmicAmuxFoutPinMode

Configures the internal function of the FOUT/AMUX pin (AMUX\_FOUT\_OTP).

The AMUX pin delivers 32 analog voltage channels outputs to the MCU ADC input.

The AMUX output is buffered out through the AMUX/FOUT pin. The voltage channels delivered to AMUX pin can be selected by I2C.

Maximum AMUX output vultage range is VDDIO.

The FOUT pin can be used to send different clocks to synchronize an external IC or for diagnostic.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	AMUX_MODE
literals	['AMUX_MODE', 'FOUT_MODE']

### 4.40 Parameter PmicPsyncEnable

This field is used to enable/disable the PSYNC mechanism used to synchronize multiple power management ICs (PSYNC EN OTP).

When disabled, the PSYNC pin shall be kept either open or short to GND.

- 0 PSYNC Mechanism is Disabled
- 1 PSYNC Mechanism is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

# 4.41 Parameter PmicPsyncMode

Configures the mode of the PSYNC mechanism (PSYNC\_CFG\_OTP).

The PSYNC mechanism allows to manage complex start-up sequence with multiple power management ICs like  $2x \ VR5510$  or  $1x \ VR5510 + 1x \ PF82$  (the choice depending on the configuration of this field).

When PSYNC is used to synchronize two VR5510, the PSYNC pin of each device must be connected and pulled up to VBOS pin of the VR5510 master device.

When PSYNC is used to synchronize one VR5510 and one PF82, the PSYNC pin of VR5510 must be connected to the PGOOD pin of PF82 and can be pulled up to

VBOS or VSNS pin.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SYNC_2X_VR5510
literals	['SYNC_2X_VR5510', 'SYNC_VR5510_AND_PF82']

# ${\bf 4.42} \quad {\bf Parameter\ PmicPsyncPowerDownControlEnable}$

When enabled, the VR5510 device will power down when PSYNC is low level.

- 0 PSYNC Power Down Control is Disabled
- 1 PSYNC PowerDown Control is Enabled

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

## 4.43 Parameter PmicStandbyTimerEnable

This field is used to enable/disable the standby transition timer (STBY\_TIMER\_EN\_OTP).

- 0 Standby Transition Timer is Disabled
- 1 Standby Transition Timer is Enabled

The Standby Timer is implemented in the Main-Unit logic to automatically transition

the device to Deep Fail-Safe (DFS) mode in case of timeout during Standby mode.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

# 4.44 Parameter PmicStandbyDischargeThreshold

Configures the standby discharge threshold (STBY\_DISCH\_OTP).

The device goes to standby mode after verifying that all the disabled

regulators have been discharged to less than  $75 \mathrm{mV}$  or  $150 \mathrm{mV}$  (the choice

depending on the configuration of this field).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	MAX_75_MV
literals	['MAX_75_MV', 'MAX_150_MV']

## 4.45 Parameter PmicStandbyPolarity

Configures the polarity of the standby signal (STBY\_POLARITY\_OTP).

STBY is an input signal that can be connected in the application to the MCU.

The standby mode is entered by toggling the STBY pin to either low or high

(the choice depending on the configuration of this field) or by a software

command from the MCU when conditions are programmed correctly with the

STBY\_EN\_OTP and STBY\_WINDOW\_EN\_OTP bits.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueConngClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	HIGH_IN_NORMAL_LOW_IN_STANDBY
literals	['HIGH_IN_NORMAL_LOW_IN_STANDBY', 'LOW_IN_NORMAL_HIG← H_IN_STANDBY']

# 4.46 Parameter PmicStandbyPGoodEnable

This field is used to enable/disable the standby PGOOD output signal (STBY\_PGOOD\_EN\_OTP).

0 - STBY\_PGOOD signal is Disabled

1 - STBY\_PGOOD signal is Enabled

STBY PGOOD is an output signal that can be connected in the application to the MCU.

The signal is high in normal mode and it will be asserted low in Standby mode to indicate a safe transition to the Standby mode when the regulators are discharged below the OTP configured threshold.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

# 4.47 Parameter PmicVddioSupplySelect

Configures the VDDIO supply selection (VDDIO\_REG\_ASSIGN\_OTP[2:0]).

The VDDIO input pin can be connected to VPRE, LDO1-3, BUCK2-3, or an external regulator (the choice depending on the configuration of this field).

The regulator connected to VDDIO MUST be at 1.8V or 3.3V

to be compatible with over-voltage and under-voltage monitoring thresholds.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	LDO3
literals	['EXTERNAL_REGULATOR', 'VPRE', 'LDO1', 'LDO2', 'BUCK2', 'BUCK3', 'LDO3']

### 4.48 Container PmicOtpPowerSequenceConfiguration

This container contains the configuration parameters for the power sequencing of the Main Unit.

Excepting VPRE, all the other regulator start according to the OTP power sequencing configuration.

Eight slots (SLOT\_0 to SLOT\_7) are available to program the start-up sequence of the regulators.

Additionally, HVLDO can be programmed to start up in a slot or not.

The power-up sequence starts at SLOT\_0 and ends at SLOT\_7, while the power-down sequence is executed in reverse order. If not all the available 7 slots are used, the state machine skips past the unused slots.

The regulators assigned to SLOT\_7 are not started during the power-up sequence. Instead, they can be started later in NORMAL mode through an I2C command.

Warning: For applications that require the HVLDO to track BUCK1,

BUCK1 and HVLDO must be separated by one slot, where HVLDO will start first followed by BUCK1.

Note: Implementation Specific Parameter.

Included subcontainers:

- PmicVpreRegulator
- PmicBoostRegulator
- PmicHVLdoRegulator
- PmicBuck1Regulator
- PmicBuck2Regulator
- PmicBuck3Regulator
- PmicLdo1Regulator
- PmicLdo2Regulator
- PmicLdo3Regulator

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

### 4.49 Parameter PmicSlotWidth

Controls the width of each slot (SLOT\_WIDTH\_OTP[1:0]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TIME_250US
literals	['TIME_250US', 'TIME_500US', 'TIME_1000US', 'TIME_2000US']

# 4.50 Container PmicVpreRegulator

This container contains the configuration parameters for the power sequencing of the VPRE (HVBUCK) regulator.

VPRE is the first regulator to start automatically, if enabled, before SLOT\_0.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# 4.51 Parameter PmicVpreEnableRegulator

This field is used to enable/disable the VPRE (HVBUCK) regulator (VPREDIS\_OTP).

0 - VPRE is Disabled

1 - VPRE is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

# 4.52 Parameter PmicVprePowerupMode

Controls the power-up behavior of the VPRE (HVBUCK) regulator (VPRE\_AUTO\_ON\_OTP).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	AUTO_ENABLED
literals	['AUTO_ENABLED', 'GATE_ENABLED']

# ${\bf 4.53}\quad {\bf Parameter\ PmicVprePhaseDelay}$

Controls the phase delay of the VPRE (HVBUCK) regulator (VPRE\_PH\_OTP[2:0]).

The clocks of all the switching regulators (VPRE, BOOST, and BUCK1-3) can be delayed to avoid all the regulators to turn ON at the same time to reduce peak current and

improve EMC performance.

VPRE has a peak current detection architecture. The PWM synchronizes the turn ON of the High-Side switch.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	0
max	7
min	0

# 4.54 Parameter PmicVpreClockSelect

Controls the clock selection of the VPRE (HVBUCK) regulator (VPRE\_CLK\_SEL\_OTP).

Warning: The VPRE operation at 2.2MHz is known to be unstable. Output ripple and PWM jitter may occur.

Consider using CLK2 for stability purposes.

There is a known bug when using the CLK1 for VPRE Clock, which results in buggy regulation

for high input voltages (VSUP over 30V).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	CLK2
literals	['CLK2', 'CLK1']

# ${\bf 4.55}\quad {\bf Container\ PmicBoostRegulator}$

This container contains the configuration parameters for the power sequencing of the BOOST regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

## 4.56 Parameter PmicBoostEnableRegulator

This field is used to enable/disable the BOOST regulator (BOOSTEN\_OTP).

0 - BOOST is Disabled

1 - BOOST is Enabled

Warning: When disabled, the VBOOST pin must be pulled up

to VPRE and the BOOST\_LS pin must be left open.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

### 4.57 Parameter PmicBoostSlotSelect

Controls the slot assignment of the BOOST regulator (BOOSTS\_OTP[2:0]).

The regulators assigned to SLOT\_7 are not started during the power-up sequence. Instead,

they can be started later in NORMAL mode through an I2C command.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SLOT_0
literals	['SLOT_0', 'SLOT_1', 'SLOT_2', 'SLOT_3', 'SLOT_4', 'SLOT_5', 'SLOT_6', 'SLOT_7']

# 4.58 Parameter PmicBoostPhaseDelay

Controls the phase delay of the BOOST regulator (VBST\_PH\_OTP[2:0]).

The clocks of all the switching regulators (VPRE, BOOST, and BUCK1-3) can be delayed to avoid all the regulators to turn ON at the same time to reduce peak current and improve EMC performance.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	0
max	7
min	0

### 4.59 Parameter PmicBoostClockSelect

Controls the clock selection of the BOOST regulator (VBST\_CLK\_SEL\_OTP).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	CLK1
literals	['CLK2', 'CLK1']

### 4.60 Parameter PmicBoostTsdBehavior

Controls the reaction/behavior of the BOOST regulator in case of a thermal shutdown event (BOOST\_TSDCFG\_OTP).

Can be configured to either shutdown only the regulator OR shutdown the regulator and transition the device into Deep Fail-State (DFS) mode when the thermal shutdown threshold is exceeded.

In case SHUTDOWN\_ONLY is selected, the regulator will startup automatically when the temperature goes down.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SHUTDOWN_AND_DFS
literals	['SHUTDOWN_ONLY', 'SHUTDOWN_AND_DFS']

# 4.61 Container PmicHVLdoRegulator

This container contains the configuration parameters for the power sequencing of the HVLDO regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# ${\bf 4.62} \quad {\bf Parameter} \,\, {\bf PmicHVLdoEnableRegulator}$

This field is used to enable/disable the HVLDO regulator (HVLDOEN\_OTP).

- 0 HVLDO is Disabled
- 1 HVLDO is Enabled

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

### 4.63 Parameter PmicHVLdoSequenceControl

Controls the power-up behavior of the HVLDO regulator (HVLDO\_SLOT\_EN\_OTP).

HVLDO can be configured to be the first (before VPRE) regulator to start automatically

before SLOT\_0 (HV\_HVLDO\_IN must be supplied by VSUP), or to start according to the assigned slot.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	START_IN_SLOT
literals	['START_FIRST', 'START_IN_SLOT']

#### 4.64 Parameter PmicHVLdoSlotSelect

Controls the slot assignment of the HVLDO regulator (HVLDOS\_OTP[2:0]).

The regulators assigned to SLOT\_7 are not started during the power-up sequence. Instead,

they can be started later in NORMAL mode through an I2C command.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE

Property	Value
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SLOT_0
literals	['SLOT_0', 'SLOT_1', 'SLOT_2', 'SLOT_3', 'SLOT_4', 'SLOT_5', 'SLOT_6', 'SLOT_7']

### 4.65 Parameter PmicHVLdoTsdBehavior

Controls the reaction/behavior of the HVLDO regulator in case of a thermal shutdown event (HVLDO\_TSDCFG\_OTP).

Can be configured to either shutdown only the regulator OR shutdown the regulator and transition the device into Deep Fail-State (DFS) mode when the thermal shutdown threshold is exceeded.

In case SHUTDOWN\_ONLY is selected, the regulator will startup automatically when the temperature goes down.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SHUTDOWN_AND_DFS
literals	['SHUTDOWN_ONLY', 'SHUTDOWN_AND_DFS']

## 4.66 Container PmicBuck1Regulator

This container contains the configuration parameters for the power sequencing of the BUCK1 regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

## 4.67 Parameter PmicBuck1EnableRegulator

This field is used to enable/disable the BUCK1 regulator.

0 - BUCK1 is Disabled

1 - BUCK1 is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

### 4.68 Parameter PmicBuck1SlotSelect

Controls the slot assignment of the BUCK1 regulator (BUCK1S\_OTP[2:0]).

The regulators assigned to SLOT\_7 are not started during the power-up sequence. Instead,

they can be started later in NORMAL mode through an I2C command.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF

Property	Value
origin	NXP
${\it symbolic} Name Value$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SLOT_0
literals	['SLOT_0', 'SLOT_1', 'SLOT_2', 'SLOT_3', 'SLOT_4', 'SLOT_5', 'SLOT_6', 'SLOT_7']

# 4.69 Parameter PmicBuck1PhaseDelay

Controls the phase delay of the BUCK1 regulator (BUCK1 PH OTP[2:0]).

The clocks of all the switching regulators (VPRE, BOOST, and BUCK1-3) can be delayed

to avoid all the regulators to turn ON at the same time to reduce peak current and

improve EMC performance.

BUCK1 has a valley current detection architecture. The PWM synchronizes the turn

ON of the Low-Side switch.

In dual-phase mode operation, the phase delay of the BUCK2 regulator is automatically

shifted an additional 180 degrees (i.e. BUCK2 Phase Delay (cycles) = PmicBuck1PhaseDelay + 1/2)

Property	Value	
type	ECUC-INTEGER-PARAM-DEF	
origin	NXP	
symbolicNameValue	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	false	
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE	
	VARIANT-PRE-COMPILE: PRE-COMPILE	
defaultValue	0	
max S	32 PMIC Driver	P Semiconductors
min	0	

#### 4.70 Parameter PmicBuck1ClockSelect

Controls the clock selection of the BUCK1 regulator (BUCK1\_CLK\_SEL\_OTP).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	CLK1
literals	['CLK2', 'CLK1']

#### 4.71 Parameter PmicBuck1TsdBehavior

Controls the reaction/behavior of the BUCK1 regulator in case of a thermal shutdown event (BUCK1\_TSDCFG\_OTP).

Can be configured to either shutdown only the regulator OR shutdown the regulator and transition the

device into Deep Fail-State (DFS) mode when the thermal shutdown threshold is exceeded.

In case SHUTDOWN\_ONLY is selected, the regulator will startup automatically when the temperature goes down.

	Property	Value
	type	ECUC-ENUMERATION-PARAM-DEF
	origin	NXP
	symbolicNameValue	false
	lowerMultiplicity	1
	upperMultiplicity	1
	postBuildVariantMultiplicity	N/A
	multiplicityConfigClasses	N/A
	postBuildVariantValue	false
	valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	varueConnigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
NXP Semico	defaultValue nductors	SHUTDOWN AND DFS S32 PMIC Driver
	literals	['SHUTDOWN_ONLY', 'SHUTDOWN_AND_DFS']

# 4.72 Container PmicBuck2Regulator

This container contains the configuration parameters for the power sequencing of the BUCK2 regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# 4.73 Parameter PmicBuck2EnableRegulator

This field is used to enable/disable the BUCK2 regulator (BUCK2EN\_OTP).

- 0 BUCK2 is Disabled
- 1 BUCK2 is Enabled

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

#### 4.74 Parameter PmicBuck2SlotSelect

Controls the slot assignment of the BUCK2 regulator (BUCK2S\_OTP[2:0]).

The regulators assigned to SLOT\_7 are not started during the power-up sequence. Instead,

they can be started later in NORMAL mode through an I2C command.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SLOT_0
literals	['SLOT_0', 'SLOT_1', 'SLOT_2', 'SLOT_3', 'SLOT_4', 'SLOT_5', 'SLOT_6', 'SLOT_7']

# 4.75 Parameter PmicBuck2PhaseDelay

Controls the phase delay of the BUCK2 regulator (BUCK2\_PH\_OTP[2:0]).

The clocks of all the switching regulators (VPRE, BOOST, and BUCK1-3) can be delayed

to avoid all the regulators to turn ON at the same time to reduce peak current and

improve EMC performance.

BUCK2 has a valley current detection architecture. The PWM synchronizes the turn

ON of the Low-Side switch.

In dual-phase mode operation, the phase delay of the BUCK2 regulator is automatically

shifted an additional 180 degrees (i.e. BUCK2 Phase Delay (cycles) = PmicBuck1PhaseDelay + 1/2)

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	0
max	7
min	0

#### 4.76 Parameter PmicBuck2ClockSelect

Controls the clock selection of the BUCK2 regulator (BUCK2\_CLK\_SEL\_OTP).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	CLK1
literals	['CLK2', 'CLK1']

### 4.77 Parameter PmicBuck2TsdBehavior

Controls the reaction/behavior of the BUCK2 regulator in case of a thermal shutdown event (BUCK2\_TSDCFG\_OTP).

Can be configured to either shutdown only the regulator OR shutdown the regulator and transition the

device into Deep Fail-State (DFS) mode when the thermal shutdown threshold is exceeded.

In case SHUTDOWN\_ONLY is selected, the regulator will startup automatically when the temperature goes down.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SHUTDOWN_AND_DFS
literals	['SHUTDOWN_ONLY', 'SHUTDOWN_AND_DFS']

# 4.78 Container PmicBuck3Regulator

This container contains the configuration parameters for the power sequencing of the BUCK3 regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# 4.79 Parameter PmicBuck3EnableRegulator

This field is used to enable/disable the BUCK3 regulator (BUCK3EN\_OTP).

#### 0 - BUCK3 is Disabled

#### 1 - BUCK3 is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

### 4.80 Parameter PmicBuck3SlotSelect

Controls the slot assignment of the BUCK3 regulator (BUCK3S\_OTP[2:0]).

The regulators assigned to SLOT\_7 are not started during the power-up sequence. Instead,

they can be started later in NORMAL mode through an I2C command.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SLOT_0
literals	['SLOT_0', 'SLOT_1', 'SLOT_2', 'SLOT_3', 'SLOT_4', 'SLOT_5', 'SLOT_6', 'SLOT_7']

# 4.81 Parameter PmicBuck3PhaseDelay

Controls the phase delay of the BUCK3 regulator (BUCK3\_PH\_OTP[2:0]).

The clocks of all the switching regulators (VPRE, BOOST, and BUCK1-3) can be delayed to avoid all the regulators to turn ON at the same time to reduce peak current and improve EMC performance.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
walno ConferClasses	VARIANT-POST-BUILD: PRE-COMPILE
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	0
max	7
min	0

### 4.82 Parameter PmicBuck3ClockSelect

Controls the clock selection of the BUCK3 regulator (BUCK3\_CLK\_SEL\_OTP).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	CLK1
literals S	['CLK2' 'CLK1'] 32 PMIC Driver

NXP Semiconductors S32 PMIC Driver 67

#### 4.83 Parameter PmicBuck3TsdBehavior

Controls the reaction/behavior of the BUCK3 regulator in case of a thermal shutdown event (BUCK3\_TSDCFG\_OTP).

Can be configured to either shutdown only the regulator OR shutdown the regulator and transition the device into Deep Fail-State (DFS) mode when the thermal shutdown threshold is exceeded.

In case SHUTDOWN\_ONLY is selected, the regulator will startup automatically when the temperature goes down.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SHUTDOWN_AND_DFS
literals	['SHUTDOWN_ONLY', 'SHUTDOWN_AND_DFS']

# 4.84 Container PmicLdo1Regulator

This container contains the configuration parameters for the power sequencing of the LDO1 regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# 4.85 Parameter PmicLdo1EnableRegulator

This field is used to enable/disable the LDO1 regulator (LDO1EN\_OTP).

0 - LDO1 is Disabled

1 - LDO1 is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

### 4.86 Parameter PmicLdo1SlotSelect

Controls the slot assignment of the LDO1 regulator (LDO1S\_OTP[2:0]).

The regulators assigned to SLOT $\_7$  are not started during the power-up sequence. Instead,

they can be started later in NORMAL mode through an I2C command.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SLOT_0
literals NXP Semiconductors	['SLOT_0', 'SLOT_1', 'SLOT_2', 'SLOT_3', 'SLOT_4', 'SLOT_5', 'SLOT_6', 'SLOT_7']

#### 4.87 Parameter PmicLdo1TsdBehavior

Controls the reaction/behavior of the LDO1 regulator in case of a thermal shutdown event (LDO1\_TSDCFG\_OTP).

Can be configured to either shutdown only the regulator OR shutdown the regulator and transition the device into Deep Fail-State (DFS) mode when the thermal shutdown threshold is exceeded.

In case SHUTDOWN\_ONLY is selected, the regulator will startup automatically when the temperature goes down.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SHUTDOWN_AND_DFS
literals	['SHUTDOWN_ONLY', 'SHUTDOWN_AND_DFS']

# 4.88 Container PmicLdo2Regulator

This container contains the configuration parameters for the power sequencing of the LDO2 regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# 4.89 Parameter PmicLdo2EnableRegulator

This field is used to enable/disable the LDO2 regulator (LDO2EN\_OTP).

0 - LDO2 is Disabled

1 - LDO2 is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigCiasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

### 4.90 Parameter PmicLdo2SlotSelect

Controls the slot assignment of the LDO2 regulator (LDO2S\_OTP[2:0]).

The regulators assigned to SLOT $\_7$  are not started during the power-up sequence. Instead,

they can be started later in NORMAL mode through an I2C command.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigCiasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SLOT_0
literals NXP Semiconductors	['SLOT_0', 'SLOT_1', 'SLOT_2', 'SLOT_3', 'SLOT_4', 'SLOT_5', 'SLOT_6', 'SLOT_7']

#### 4.91 Parameter PmicLdo2TsdBehavior

Controls the reaction/behavior of the LDO2 regulator in case of a thermal shutdown event (LDO2\_TSDCFG\_OTP).

Can be configured to either shutdown only the regulator OR shutdown the regulator and transition the device into Deep Fail-State (DFS) mode when the thermal shutdown threshold is exceeded.

In case SHUTDOWN\_ONLY is selected, the regulator will startup automatically when the temperature goes down.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SHUTDOWN_AND_DFS
literals	['SHUTDOWN_ONLY', 'SHUTDOWN_AND_DFS']

# 4.92 Container PmicLdo3Regulator

This container contains the configuration parameters for the power sequencing of the LDO3 regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# 4.93 Parameter PmicLdo3EnableRegulator

This field is used to enable/disable the LDO3 regulator (LDO3EN\_OTP).

0 - LDO3 is Disabled

1 - LDO3 is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

### 4.94 Parameter PmicLdo3SlotSelect

Controls the slot assignment of the LDO3 regulator (LDO3S\_OTP[2:0]).

The regulators assigned to SLOT\_7 are not started during the power-up sequence. Instead,

they can be started later in NORMAL mode through an I2C command.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SLOT_0
literals NXP Semiconductors	['SLOT_0', 'SLOT_1', 'SLOT_2', 'SLOT_3', 'SLOT_4', 'SLOT_5', 'SLOT_6', 'SLOT_7']

#### 4.95 Parameter PmicLdo3TsdBehavior

Controls the reaction/behavior of the LDO3 regulator in case of a thermal shutdown event (LDO3\_TSDCFG\_OTP).

Can be configured to either shutdown only the regulator OR shutdown the regulator and transition the device into Deep Fail-State (DFS) mode when the thermal shutdown threshold is exceeded.

In case SHUTDOWN\_ONLY is selected, the regulator will startup automatically when the temperature goes down.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SHUTDOWN_AND_DFS
literals	['SHUTDOWN_ONLY', 'SHUTDOWN_AND_DFS']

# ${\bf 4.96}\quad {\bf Container\ PmicOtpRegulatorsConfiguration}$

This container contains the configuration parameters for the OTP registers controlling the functionality of regulators.

Note: Implementation Specific Parameter.

Included subcontainers:

- PmicVpreRegulator
- $\bullet$  PmicVBoostRegulator
- PmicBuck1Regulator
- PmicBuck2Regulator
- PmicBuck3Regulator

- PmicLdo1Regulator
- PmicLdo2Regulator
- PmicLdo3Regulator
- PmicHVLdoRegulator

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# 4.97 Container PmicVpreRegulator

This container contains the configuration parameters of the VPRE (HVBUCK) regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# ${\bf 4.98}\quad {\bf Parameter\ PmicVpreOutputVoltage}$

Controls the output voltage of the VPRE (HVBUCK) regulator (VPREV\_OTP[5:0]).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	OUT_3V3
literals	['OUT_3V3', 'OUT_3V4', 'OUT_3V5', 'OUT_3V7', 'OUT_4V0', 'OUT_4V5', 'OUT_5V0', 'OUT_5V1', 'OUT_5V2']

# 4.99 Parameter PmicVpreSlopeCompensation

Controls the slope compensation of the VPRE (HVBUCK) regulator (VPRESC\_OTP[5:0]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SLOPE_60
literals	['SLOPE_60', 'SLOPE_70', 'SLOPE_140', 'SLOPE_200']

# ${\bf 4.100}\quad {\bf Parameter\ PmicVpreStdbyVoltageControlEnable}$

This field is used to enable/disable the 3V output voltage selection for VPRE in Standby Mode (VPREV\_STDY\_EN\_OTP).

0 - The output voltage of VPRE in Standby Mode is controlled by VPREV\_OTP[5:0]

(i.e. 'PmicVpreOutputVoltage').

1 - The output voltage of VPRE in Standby Mode is controlled according to the M\_REG\_CTRL3[VPREV\_STBY] selection

 $(i.e.\ 'PmicModeSettingConf/PmicRegulatorsConfiguration/PmicVpreRegulator/PmicVpreStandbyOutputVoltage').$ 

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

# 4.101 Parameter PmicVpreCsaThreshold

Controls the current sense amplifier peak detection threshold of the VPRE (HVBUCK) regulator (VPREILIM\_OTP[1:0]).

Warning: The 150mV setting is not available for 2.22MHz. (VPRE Clock Select must be set to CLK2).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	MAX_120_MV
literals	['MAX_50_MV', 'MAX_80_MV', 'MAX_120_MV', 'MAX_150_MV']

### 4.102 Parameter PmicVpreHsCurrentCapability

Controls the pull-up current capability of the HS (High-Side) gate driver of the VPRE (HVBUCK) regulator (VPRESRHS\_OTP[1:0]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	I_130_MA
literals	['I_130_MA', 'I_260_MA', 'I_520_MA', 'I_900_MA']

# ${\bf 4.103} \quad {\bf Parameter} \ {\bf PmicVpreLsCurrentCapability}$

Controls the pull-down current capability of the LS (Low-Side) gate driver of the VPRE (HVBUCK) regulator (VPRESRLS\_OTP[1:0]).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	I_130_MA
literals	['I_130_MA', 'I_260_MA', 'I_520_MA', 'I_900_MA']

# 4.104 Parameter PmicVpreSoftStartRamp

Controls the soft start ramp (from 0V to 1V) of the VPRE (HVBUCK) regulator (VPRE\_SSRAMP\_OTP).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	2
max	2
min	1

# ${\bf 4.105} \quad {\bf Parameter} \ {\bf PmicVpreHsOffTime}$

Controls the minimum OFF time of the HS (High-Side) gate driver of the VPRE (HVBUCK) regulator (VPRETOFF\_OTP[1:0])

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TIME_80NS
literals	['TIME_80NS', 'TIME_60NS', 'TIME_40NS', 'TIME_20NS']

#### 4.106 Parameter PmicVpreHsOnTime

Controls the minimum ON time of the HS (High-Side) gate driver of the VPRE (HVBUCK) regulator (VPRE\_PFM\_TON\_O

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TIME_120NS
literals	['TIME_120NS', 'TIME_210NS', 'TIME_300NS', 'TIME_560NS']

# 4.107 Parameter PmicVpreShutdownDelay

Controls the shutdown delay between VBOOST and VPRE (VPRE\_OFF\_DLY\_OTP).

When shutting down, the device follows the power down sequence to stop all the regulators in the reverse order of the power up sequence. The value of this field is an additional delay added to the Tslot time (PmicSlotWidth) between "SLOT\_0" and "VPRE\_OFF".

To be used in case VPRE is supplying an external PMIC to wait its power down sequence completion.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE 32 PMIC Driver
defaultValue	TIME_250US
literals	['TIME_250US', 'TIME_32MS']

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#### 4.108 Container PmicVBoostRegulator

This container contains the configuration parameters of the VBOOST regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# 4.109 Parameter PmicVBoostOutputVoltage

Controls the output voltage of the VBOOST regulator (VBSTV\_OTP[3:0]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	OUT_5V00
literals	['OUT_4V50', 'OUT_5V00', 'OUT_5V09', 'OUT_5V19', 'OUT_5V40', 'OUC T_5V74', 'OUT_6V00']

# ${\bf 4.110}\quad {\bf Parameter\ PmicVBoostSlopeCompensation}$

Controls the slope compensation of the VBOOST regulator (VBSTSC\_OTP[4:0]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SLOPE_67
literals	['SLOPE_160', 'SLOPE_125', 'SLOPE_79', 'SLOPE_67']

### 4.111 Parameter PmicVBoostLsOnTime

 $Controls \ the \ minimum \ ON \ time \ of \ the \ LS \ (Low-Side) \ gate \ driver \ of \ the \ VBOOST \ regulator \ (VBSTTONTIME\_OTP[1:0]).$ 

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TIME_60NS
literals	['TIME_60NS', 'TIME_50NS', 'TIME_70NS', 'TIME_80NS']

### 4.112 Parameter PmicVBoostCurrentLimit

Controls (limits) the output current of the VBOOST regulator (VBSTILIM\_OTP[1:0]).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	I_3_A
literals	['I_2_A', 'I_3_A']

#### 4.113 Parameter PmicVBoostSlewRate

Controls the slew rate of the VBOOST regulator (VBSTSR\_OTP[1:0]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	RATE_500
literals	['RATE_100', 'RATE_300', 'RATE_500']

# ${\bf 4.114} \quad {\bf Parameter} \ {\bf PmicVBoostCompensationCapacitor}$

Controls the compensation capacitor of the VBOOST regulator (VBSTCCOMP\_OTP[1:0]).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	C_125_PF
literals	['C_125_PF', 'C_75_PF', 'C_175_PF', 'C_225_PF']

### 4.115 Parameter PmicVBoostCompensationResistor

Controls the compensation resistor of the VBOOST regulator (VBSTRCOMP\_OTP[1:0]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	R_500_KOHM
literals	['R_750_KOHM', 'R_500_KOHM', 'R_1000_KOHM', 'R_250_KOHM']

### 4.116 Parameter PmicVBoostToVBos

This field is used to enable/disable the input path to VBOS of the VBOOST regulator (VBOS\_VBOOST\_OTP).

- 0 VBOOST Input Path to BOS is Disabled (BOS will regulate only from VSUP or VPRE)
- 1 VBOOST Input Path to BOS is Enabled (BOS will regulate from VBOOST or VSUP or VPRE)

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

# 4.117 Container PmicBuck1Regulator

This container contains the configuration parameters of the BUCK1 regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# 4.118 Parameter PmicBuck1OutputVoltage

Controls the output voltage of the BUCK1 regulator (BUCK1V\_OTP[7:0]).

 $\mathrm{BUCK1}$  (BUCK1/2 in dual-phase mode) is intended to supply the MCU core voltage.

The output voltage must have a resolution of  $6.25~\mathrm{mV}.$ 

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	0.8
max	1.8
min	0.4

#### 4.119 Parameter PmicBuck1CurrentLimit

Controls (limits) the output current of the BUCK1 regulator (BUCK1\_ILIM\_OTP[1:0]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	I_3_6_A
literals	['I_2_4_A', 'I_3_6_A']

### 4.120 Parameter PmicBuck1InductorSelect

Controls the inductance (LBuck1) for VBuck1\_SW of the BUCK1 regulator (BUCK1\_LSELECT\_OTP[1:0]).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	L_1_0_UH
literals	['L_1_0_UH', 'L_0_47_UH', 'L_1_5_UH']

#### 4.121 Parameter PmicBuck1Transconductance

Controls the transconductance of the BUCK1 regulator (BUCK1\_COMP\_OTP[2:0]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TRANS_65_uMho
literals	

# 4.122 Parameter PmicBuck1DVSRamp

Controls the DVS (Dynamic Voltage Scaling) ramp of the BUCK1 regulator (BUCK1DVS\_RAMP\_OTP).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	DVS_7_8
literals	['DVS_7_8', 'DVS_15_6']

#### 4.123 Parameter PmicBuck1PhaseMode

Controls the phase mode of the BUCK1 and BUCK2 regulators (VB12MULTIPH\_OTP).

BUCK1 and BUCK2 can work independently or in dual phase mode to double the output current capability.

When BUCK1 and BUCK2 are used in single phase, they have independent outputs, working independently.

When BUCK1 and BUCK2 are used in dual phase, they must have the same output voltage

configuration. Any action like TSD, OV, disable by I2C, on BUCK1 will affect BUCK2 and vice versa.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	DUAL_PHASE_MODE
literals	['SINGLE_PHASE_MODE', 'DUAL_PHASE_MODE']

#### 4.124 Container PmicBuck2Regulator

This container contains the configuration parameters of the BUCK2 regulator.

This container is configurable only when the BUCK1 and BUCK2 regulators are

not in double phase mode (i.e. PmicBuck1Regulator/PmicBuck1PhaseMode = 'SINGLE\_PHASE\_MODE').

Otherwise, BUCK2 will implicitly use the same configuration as BUCK1.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# 4.125 Parameter PmicBuck2OutputVoltage

Controls the output voltage of the BUCK2 regulator (BUCK2V\_OTP[7:0]).

The output voltage must have a resolution of 6.25 mV.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	0.8
max	1.8
min	0.4

### 4.126 Parameter PmicBuck2CurrentLimit

Controls (limits) the output current of the BUCK2 regulator (BUCK2\_ILIM\_OTP[1:0]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	I_3_6_A
literals	['I_2_4_A', 'I_3_6_A']

### 4.127 Parameter PmicBuck2InductorSelect

Controls the inductance (LBuck2) for VBuck2\_SW of the BUCK2 regulator (BUCK2\_LSELECT\_OTP[1:0]).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	L_1_0_UH
literals	['L_1_0_UH', 'L_0_47_UH', 'L_1_5_UH']

### 4.128 Parameter PmicBuck2Transconductance

Controls the transconductance of the BUCK2 regulator (BUCK2\_COMP\_OTP[2:0]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TRANS_65_uMho
literals	['TRANS_16_25_uMho', 'TRANS_32_5_uMho', 'TRANS_48_75_uMho', 'TRANS_65_uMho', 'TRANS_81_25_uMho', 'TRANS_97_5_uMho', 'TRANS_97_13_uMho', 'TRANS_97_5_uMho']

# ${\bf 4.129}\quad {\bf Container\ PmicBuck3Regulator}$

This container contains the configuration parameters of the BUCK3 regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# ${\bf 4.130}\quad {\bf Parameter\ PmicBuck 3 Output Voltage}$

Controls the output voltage of the BUCK3 regulator (BUCK3V\_OTP[4:0]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	OUT_1V1
literals	['OUT_1V0', 'OUT_1V1', 'OUT_1V2', 'OUT_1V25', 'OUT_1V3', 'OUT_1↔
	$ V35', 'OUT_1V5', 'OUT_1V6', 'OUT_1V8', 'OUT_1V85', 'OUT_2V0', 'O \leftarrow  V35', 'OUT_1V85', 'OUT_2V0', 'O \leftarrow  V35', 'OUT_1V8', 'OUT_1V8', 'OUT_1V85', 'OUT_2V0', 'O \leftarrow  V35', 'OUT_1V8', 'OUT_1V$
	UT_2V1', 'OUT_2V15', 'OUT_2V25', 'OUT_2V3', 'OUT_2V4', 'OUT_2V5',
	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$
	V35', 'OUT_3V4', 'OUT_3V5', 'OUT_3V8', 'OUT_4V0', 'OUT_4V1']

#### 4.131 Parameter PmicBuck3CurrentLimit

Controls (limits) the output current of the BUCK3 regulator (BUCK3\_ILIM\_OTP[1:0]).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	I_3_6_A
literals	['I_2_4_A', 'I_3_6_A']

### 4.132 Parameter PmicBuck3InductorSelect

Controls the inductance (LBuck3) for VBuck3\_SW of the BUCK3 regulator (BUCK3\_LSELECT\_OTP[1:0]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	L_1_0_UH
literals	['L_1_0_UH', 'L_0_47_UH', 'L_1_5_UH']

#### 4.133 Parameter PmicBuck3Transconductance

Controls the transconductance of the BUCK3 regulator (BUCK3 $\_$ GM $\_$ OTP).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TRANS_65_uMho
literals	['TRANS_65_uMho', 'TRANS_32_5_uMho']

### 4.134 Parameter PmicBuck3CompensationResistor

Controls the compensation resistor of the BUCK3 regulator (BUCK3\_RC\_OTP).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	R_56_KOHM
literals	['R_56_KOHM', 'R_106_KOHM']

# 4.135 Container PmicLdo1Regulator

This container contains the configuration parameters of the LDO1 regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# 4.136 Parameter PmicLdo1OutputVoltage

Controls the output voltage of the LDO1 regulator (LDO1V\_OTP[2:0]).

Property	Value	
type	ECUC-ENUMERATION-PARAM-DEF	
origin	NXP	
symbolicNameValue	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	false	
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE	
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE	
defaultValue	OUT_1V8	
literals	['OUT_1V1', 'OUT_1V2', 'OUT_1V6', 'OUT_1V8', 'OUT_2V5', 'OUT_2V8', 'OUT_3V3', 'OUT_5V0']	

### 4.137 Parameter PmicLdo1CurrentLimit

Controls (limits) the output current of the LDO1 regulator (LDO1ILIM\_OTP).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigCiasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	I_400_MA
literals	['I_400_MA', 'I_150_MA']

# 4.138 Container PmicLdo2Regulator

This container contains the configuration parameters of the LDO2 regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

## 4.139 Parameter PmicLdo2OutputVoltage

Controls the output voltage of the LDO2 regulator (LDO2V\_OTP[3:0]).

Note: Implementation Specific Parameter.

Property	Value	
type	ECUC-ENUMERATION-PARAM-DEF	
origin	NXP	
symbolicNameValue	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	false	
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE	
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE	
defaultValue	OUT_1V8	
literals	['OUT_1V5', 'OUT_1V6', 'OUT_1V8', 'OUT_1V85', 'OUT_2V15', 'OUT_ 2V5', 'OUT_2V8', 'OUT_3V0', 'OUT_3V1', 'OUT_3V15', 'OUT_3V2', 'OU← T_3V3', 'OUT_3V35', 'OUT_4V0', 'OUT_4V9', 'OUT_5V0']	

# 4.140 Parameter PmicLdo2OperatingMode

Controls the operating mode (Regulator / Load Switch) of the LDO2 regulator (LDO2\_LS\_OTP).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	REGULATOR_MODE
literals	['REGULATOR_MODE', 'LOAD_SWITCH_MODE']

## 4.141 Container PmicLdo3Regulator

This container contains the configuration parameters of the LDO3 regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

## ${\bf 4.142} \quad {\bf Parameter} \ {\bf PmicLdo3OutputVoltage}$

Controls the output voltage of the LDO3 regulator (LDO3V\_OTP[3:0]).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	OUT_1V8
literals	['OUT_1V5', 'OUT_1V6', 'OUT_1V8', 'OUT_1V85', 'OUT_2V15', 'OUT_ 2V5', 'OUT_2V8', 'OUT_3V0', 'OUT_3V1', 'OUT_3V15', 'OUT_3V2', 'OU← T_3V3', 'OUT_3V35', 'OUT_4V0', 'OUT_4V9', 'OUT_5V0']

## ${\bf 4.143} \quad {\bf Parameter} \ {\bf PmicLdo3OperatingMode}$

Controls the operating mode (Regulator / Load Switch) of the LDO3 regulator (LDO3\_LS\_OTP).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	LOAD_SWITCH_MODE
literals	['REGULATOR_MODE', 'LOAD_SWITCH_MODE']

## 4.144 Container PmicHVLdoRegulator

This container contains the configuration parameters of the HVLDO regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

## 4.145 Parameter PmicHVLdoOutputVoltage

Controls the output voltage of the HVLDO regulator (HVLDOV\_OTP[1:0]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigCiasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	OUT_0V8
literals	['OUT_0V8', 'OUT_3V3']

### 4.146 Parameter PmicHVLdoTransitionMode

Controls the transition mode (LDO in both NORMAL\_M and STBY\_M / LOAD\_SWITCH in NORMAL\_M and LDO in STBY\_M) of the HVLDO regulator (HVLDO\_TRANS\_MODE\_OTP).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SWITCH_NORMAL_LDO_STDBY
literals	['LDO_MODE_ONLY', 'SWITCH_NORMAL_LDO_STDBY']

## 4.147 Container PmicOtpFailSafeUnitConfiguration

This container contains the configuration parameters for the OTP registers on the Fail-Safe Unit.

Note: Implementation Specific Parameter.

Included subcontainers:

- PmicOtpSafetyConfiguration
- PmicOtpSafetyIOConfiguration
- $\bullet \ \ PmicOtpVoltageMonitorConfiguration$

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# 4.148 Container PmicOtpSafetyConfiguration

This container contains the configuration parameters for the general safety configuration of the Fail-Safe Unit.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

## 4.149 Parameter PmicSafetyI2cAddress

Configures the I2C address of the Fail-Safe Unit (I2CDEVID\_OTP[3:0]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	A_0x21
literals	

### 4.150 Parameter PmicRSTBTimerEnable

This field is used to enable/disable the 8s RSTB timer (DISSS\_OTP).

If enabled, the 8s RSTB timer starts each time the RSTB pin is asserted low.

When the LBIST is done, the 8s timer monitoring the RSTB pin starts and

the ABIST1 is automatically executed when all the regulators assigned to

ABIST1 have passed their UV and OV checks. When the ABIST1 is done,

RSTB and PGOOD pins are released, and the initialization of the device

is opened for 256ms. ABIST1 fail does not prevent RSTB and PGOOD release.

If RSTB is not released before the RSTB timer expires (i.e. within

8 seconds), the device will go into Deep Fail-Safe.

0 - RSTB Timer is Disabled

1 - RSTB Timer is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComingClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

## 4.151 Parameter PmicFaultRecoveryEnable

This field is used to enable/disable the fault recovery strategy (FLT\_RECOVERY\_EN\_OTP).

- 0 Fault Recovery Strategy is Disabled
- 1 Fault Recovery Strategy is Enabled

This function extends the watchdog window to allow the MCU to perform a fault recovery strategy. The goal is to not reset the MCU while it is trying to recover the application after a failure event. When a fault is triggered by the MCU via its FCCU pins, the FS0B is asserted by the device and the watchdog window duration becomes automatically an open window (no more duty cycle), whose duration is given by the WDW\_RECOVERY[3:0] bits.

The transition from the normal watchdog window duration to this new open window duration happens when the FCCU pin indicates an error and FS0B is asserted. If the MCU sends a good watchdog refresh before the end of the open window duration, the device switches bask to the normal watchdog window duration and associated duty cycle if the FCCU pins do not indicate an error anymore. Otherwise, a new open window period is started. If the MCU does not send a good watchdog refresh before the end of this second open window duration, then a reset pulse is generated and the Fail-Safe State Machine moves back to INIT\_FS.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigCiasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

## 4.152 Parameter PmicRstbDelay

Configures the delay between RSTB assertion and RSTB release (RSTB\_DELAY\_OTP).

This means that even if the MCU has released its RSTB signal, the VR5510 device

will still wait for this configured delay to expire before releasing

the RSTB signal.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	NO_DELAY
literals	['NO_DELAY', 'DELAY_5MS']

## 4.153 Parameter PmicSVSLimit

Configures the maximum number of SVS steps allowed (VCORE\_SVS\_CLAMP\_OTP[5:0]).

A SVS (Static Voltage Scaling) mechanism is implemented to allow the MCU to reduce the output voltage initially configured at start-up of BUCK1 (and BUCK2 if used in multiphase) by OTP, to optimize MCU voltage working points, and compensate part to part process variation.

The offset value is configurable with the SVS\_OFFSET[5:0] bits. The number of allowed SVS steps configured in this field effectively limits the applicable offset amount.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	MAX_STEP_16
literals	

## ${\bf 4.154} \quad {\bf Parameter \ Pmic SVSOffset Type}$

Configures the offset type applicable by the SVS mechanism (VCORE\_SVS\_FULL\_OFFSET\_OTP).

A SVS (Static Voltage Scaling) mechanism is implemented to allow the MCU to reduce the output voltage initially configured at start-up of BUCK1 (and BUCK2 if used in multiphase) by OTP, to optimize MCU voltage working points, and compensate part to part process variation.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF

Property	Value	
origin	NXP	
symbolicNameValue	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	false	
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE	
varueConngClasses	VARIANT-PRE-COMPILE: PRE-COMPILE	
defaultValue	NEGATIVE_OFFSET	
literals	['NEGATIVE_OFFSET', 'NEGATIVE_AND_POSITIVE_OFFSET']	

### 4.155 Parameter PmicRSTBAssertPGOOD

Configures whether the PGOOD output signal is also asserted low or not when the RSTB output signal is asserted (RSTB2PGOOD\_OTP).

RSTB is an open-drain output that can be connected in the application to the RESET of the MCU.

RSTB requires an external pull-up resistor to VDDIO and a filtering capacitor to GND for immunity.

When RSTB is asserted low, FS0B is also asserted low.

If the RSTB timer is enabled, when RSTB is stuck low for more than 8s, the device transition to DEEP-FS mode.

0 - PGOOD assertion is Disabled

1 - PGOOD assertion is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	35 THE MIC Driver

106 default Value S32 MIC Driver NXP Semiconductors

### 4.156 Parameter PmicHVLDOMONMode

Used to let the Fail-Safe Unit know whether the HVLDO regulator is operating in LOAD\_SWITCH mode or in LDO mode (HVLDO\_MODE\_OTP). In LOAD\_SWITCH mode, the reference will track internally the BUCK1 DVS DAC.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	LOAD_SWITCH_MODE
literals	['LOAD_SWITCH_MODE', 'LDO_MODE']

#### 4.157 Parameter PmicLBISTEnable

Configures whether LBIST is performed (LBIST\_DIS\_OTP[7:0]).

The Fail-Safe State Machine includes a LBIST to verify the correct functionality of the safety logic monitoring. The LBIST is performed after each POR, or after each wake-up from Standby.

In case of LBIST fail, RSTB and PGOOD are released, but FS0B remains stuck low and cannot be released.

The typical LBIST duration is 3ms and the maximum LBIST duration is 5ms.

0 - LBIST is Disabled

1 - LBIST is Enabled

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

## 4.158 Container PmicOtpSafetyIOConfiguration

This container contains the configuration parameters for the I/O capabilities of the Fail-Safe Unit.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# ${\bf 4.159 \quad Parameter \ PmicWatchdog Enable}$

This field is used to enable/disable the watchdog monitoring (WD\_DIS\_OTP).

- 0 Watchdog Monitoring is Disabled
- 1 Watchdog Monitoring is Enabled

The watchdog is a windowed watchdog. The first half of the windows is said to

be CLOSED, and the second half is said to be OPEN.

A good watchdog refresh is a good watchdog answer during the OPEN window.

A bad watchdog refresh is a bad watchdog answer during the OPEN window, no watchdog refresh during the OPEN window, or a good watchdog answer during the CLOSED window.

After a good or a bad watchdog refresh, a new window period starts immediately for the MCU to keep the synchronization with the windowed watchdog.

If enabled, the MCU must refresh the watchdog in the OPEN window of the watchdog window period.

The duration of the watchdog window is configurable from 1ms to 1024ms.

The duty cycle of the watchdog window is configurable from 31.25% to 68.75%.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

## 4.160 Parameter PmicWatchdogType

Configures the type of watchdog (WD SELECTION OTP).

The watchdog can be either a simple watchdog or a challenger watchdog.

The simple watchdog monitoring is based on a single configurable watchdog key.

The challenger watchdog monitoring is based on a 16-bits pseudo-random word generated by a LFSR, whose seed is configurable.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	CHALLENGER_WATCHDOG
literals	['SIMPLE_WATCHDOG', 'CHALLENGER_WATCHDOG']

## 4.161 Parameter PmicWdiPolarity

Configures the polarity of the WDI signal (WDI\_POL\_OTP).

This field is modifiable only when PmicFccu1OperatingMode = 'FCCU\_MODE'.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	FALLING_EDGE
literals	['FALLING_EDGE', 'RISING_EDGE']

### 4.162 Parameter PmicFccu1OperatingMode

Configures the operating mode of the FCCU1 pin (FCCU\_OR\_WDI\_OTP).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	FCCU_MODE
literals	['FCCU_MODE', 'WDI_MODE']

### 4.163 Parameter PmicFccuEnable

This field is used to enable/disable the FCCU monitoring (FCCU\_EN\_OTP).

0 - FCCU Monitoring is Disabled

1 - FCCU Monitoring is Enabled

The FCCU input pins are in charge of monitoring HW failure from the MCU.

The FCCU input pins can be configured by pair, or single independent inputs.

The FCCU monitoring is active as soon as the INIT\_FS state is closed by the

first good watchdog refresh.

The polarity of the FCCU fault signals as well as the fail-safe reaction on

RSTB and/or FS0B is configurable.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

## 4.164 Parameter PmicStandbyModeEnable

This field is used to enable/disable the Low-Power Standby Mode (STBY\_EN\_OTP).

0 - Standby Mode is Disabled

1 - Standby Mode is Enabled

The low current standby mode is used when the device is required to go into a minimal supply current mode while maintaining minimal preset output voltages.

The main regulators which are on during LP Standby mode are VPRE and the HVLDO.

The VPRE will be forced to operate in PFM mode, while the HVLDO will operate in

LDO mode. There is an option to operate other regulators (except BOOST) as well,

but the switching regulators will be forced to operate only in PFM.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

## 4.165 Parameter PmicStandbyPolarity

Configures the polarity of the standby signal (STBY POLARITY OTP).

STBY is an input signal that can be connected in the application to the MCU.

The standby mode is entered by toggling the STBY pin to either low or high

(the choice depending on the configuration of this field) or by a software

command from the MCU when conditions are programmed correctly with the

STBY\_EN\_OTP and STBY\_WINDOW\_EN\_OTP bits.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
${\it symbolic} Name Value$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	HIGH_IN_NORMAL_LOW_IN_STANDBY
literals	['HIGH_IN_NORMAL_LOW_IN_STANDBY', 'LOW_IN_NORMAL_HIG

## 4.166 Parameter PmicStandbyEntryControl

Configures the method of entering the LP Standby Mode (STBY\_SAFE\_DIS\_OTP).

The standby mode is entered by either toggling the STBY pin or by a software

command from the MCU (the choice depending on the configuration of this field)

when conditions are programmed correctly with the STBY\_EN\_OTP and

STBY\_WINDOW\_EN\_OTP bits.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	SW_AND_PIN_CONTROL
literals	['SW_AND_PIN_CONTROL', 'PIN_CONTROL_ONLY']

## 4.167 Parameter PmicSafetyStandbyWindowEnable

This field is used to enable/disable the Safety Standby Window (STBY\_WINDOW\_EN\_OTP).

- 0 Safety Standby Window is Disabled
- 1 Safety Standby Window is Enabled

When enabled, a maximum timeout can be configured between the I2C request and the STBY pin transition.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

### 4.168 Parameter PmicSafetyWindowInitTimeout

When the ABIST1 completes, the RSTB and PGOOD pins are released and the initialization of the device is opened via a programmable window based on the WD\_INIT\_TIMEOUT\_OTP[1:0] bit field (CFG\_ 2\_OTP register)

if WD\_INIT\_TIMEOUT\_OTP is expire timeout, PMIC device will reset.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TIME_1024MS
literals	['TIME_256MS', 'TIME_1024MS', 'TIME_32_5S', 'TIME_67S']

## 4.169 Container PmicOtpVoltageMonitorConfiguration

This container contains the configuration parameters for the OTP registers controlling the voltage monitoring aspect of the Fail-Safe Unit.

The voltage supervisor is in charge of over-voltage and under-voltage monitoring of VCOREMON, VDDIO, and VMONx input pins.

When an over-voltage occurs on a regulator monitored by one of these pins, the associated regulator is switched off until the fault is removed.

Note: Implementation Specific Parameter.

Included subcontainers:

- PmicVcoreMonitor
- PmicVddioMonitor
- PmicHVLdoMonitor
- PmicVmon1Monitor
- PmicVmon2Monitor
- PmicVmon3Monitor
- PmicVmon4Monitor

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

### 4.170 Container PmicVcoreMonitor

This container contains the configuration parameters for the voltage monitoring of the VCOREMON input pin.

VCOREMON input pin is dedicated to BUCK1 or BUCK1/2 in case of multiphase operation.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

### 4.171 Parameter PmicVcoreEnableMonitor

This field is used to enable/disable the voltage monitoring of the VCOREMON input pin.

- 0 VCOREMON is Disabled
- 1 VCOREMON is Enabled

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

## 4.172 Parameter PmicVcoreMonitorVoltage

Controls the nominal voltage of the VCOREMON input pin (VCORE\_V\_OTP[7:0]).

VCOREMON must be connected to the BUCK1 (BUCK1/2 in dual-phase mode) regulator output.

The nominal voltage must have a resolution of 6.25 mV.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	0.8
max	1.8
min	0.4

### 4.173 Parameter PmicVcoreMonitorUVThreshold

Controls the under-voltage threshold of the VCOREMON input pin (VCOREUVTH\_OTP[3:0]). The threshold is relative to the configured nominal voltage. For example, if this field is configured as 93.5% and VCOREMON Voltage = 0.8V, then the nominal under-voltage threshold will be equal to 0.8 \* (93.5 / 100) = 0.748 V.

Property	Value	
type	ECUC-ENUMERATION-PARAM-DEF	
origin	NXP	
${\it symbolic} Name Value$	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	false	
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE	
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE	
defaultValue	MIN_95_5	
literals	['MIN_95_5', 'MIN_95', 'MIN_94_5', 'MIN_94', 'MIN_93_5', 'MIN_93', 'M↔	
	IN_92_5', 'MIN_92', 'MIN_91_5', 'MIN_91', 'MIN_90_5', 'MIN_90', 'MIN←	
	_97_5', 'MIN_97', 'MIN_96_5', 'MIN_96']	

## 4.174 Parameter PmicVcoreMonitorOVThreshold

Controls the over-voltage threshold of the VCOREMON input pin (VCOREOVTH\_OTP[3:0]).

The threshold is relative to the configured nominal voltage. For example, if this field

is configured as 106.5% and VCOREMON Voltage = 0.8V, then the nominal over-voltage

threshold will be equal to 0.8 \* (106.5 / 100) = 0.852 V.

Property	Value	
type	ECUC-ENUMERATION-PARAM-DEF	
origin	NXP	
symbolicNameValue	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	false	
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE	
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE	
defaultValue	MAX_104_5	
literals		

### 4.175 Parameter PmicVcoreMonitorUVDebounce

Configures the under-voltage filtering time (debounce) of the VCOREMON input pin (UV\_MCU\_OTP[1:0]).

When the monitored voltage is below the nominal under-voltage threshold, this field represents the amount of time to wait until the under-voltage condition is asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TIME_25US
literals	['TIME_5US', 'TIME_15US', 'TIME_25US', 'TIME_40US']

#### 4.176 Parameter PmicVcoreMonitorOVDebounce

Configures the over-voltage filtering time (debounce) of the VCOREMON input pin (OV\_MCU\_OTP).

When the monitored voltage is above the nominal over-voltage threshold, this field represents the amount of time to wait until the over-voltage condition is asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue S	TIME 25US 32 PMIC Driver
literals	['TIME 25US', 'TIME 45US']

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### 4.177 Parameter PmicVcoreMonitorPGOODAssert

Configures whether the PGOOD output signal is asserted low or not by the FS\_LOGIC when the assigned regulator monitored by VCOREMON (i.e. BUCK1 or BUCK1/2) is in under-voltage or over-voltage (PGOOD\_VCORE\_OTP)

PGOOD is an open-drain output that can be connected in the application to the PORB of the MCU.

PGOOD requires an external pull-up resistor to VDDIO and a filtering capacitor to GND for immunity.

When PGOOD is asserted low, RSTB and FS0B are also asserted low.

- 0 PGOOD assertion is Disabled
- 1 PGOOD assertion is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

#### 4.178 Parameter PmicVcoreMonitorABIST1Enable

Configures whether VCOREMON is checked by ABIST1 or not (ABIST1 VCORE OTP).

The Fail-Safe State Machine includes two ABISTs to verify the correct functionality of the safety analog monitoring. ABIST1 is executed automatically after each POR or after each wake-up from Standby. In case of ABIST1 fail, RSTB and PGOOD are released, but FS0B remains stuck low and cannot be released.

It is recommended to verify latent faults on VCOREMON, HVLDOMON, and VDDIOMON during ABIST1, while the latent faults on VMONx can be verified either during ABIST1 or

#### ABIST2.

0 - VCOREMON check by ABIST1 is Disabled

1 - VCOREMON check by ABIST1 is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

#### Container PmicVddioMonitor 4.179

This container contains the configuration parameters for the voltage monitoring of the VDDIO input pin. VDDIO input pin can be connected to VPRE, LDO1-3, BUCK2-3, or an external regulator. The regulator connected to VDDIO must be at 1.8V or 3.3V to be compatible with over-voltage and undere-voltage monitoring thresholds.

If an external regulator is connected to VDDIO, then only a flag is reported to the MCU which then must decide the appropriate action to perform.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
tomultiplicityConfigClasses S3	2 <sup>N</sup> /MIC Driver

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## 4.180 Parameter PmicVddioEnableMonitor

This field is used to enable/disable the voltage monitoring of the VDDIOMON input pin (VDDIO\_VMON\_EN\_OTP).

- 0 VDDIOMON is Disabled
- 1 VDDIOMON is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

# ${\bf 4.181} \quad {\bf Parameter} \ {\bf PmicVddioMonitorVoltage}$

Controls the nominal voltage of the VDDIO input pin (VDDIO\_V\_OTP).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	OUT_3V3
literals	['OUT_1V8', 'OUT_3V3']

### 4.182 Parameter PmicVddioMonitorUVThreshold

Controls the under-voltage threshold of the VDDIO input pin (VDDIOUVTH\_OTP[3:0]).

The threshold is relative to the configured nominal voltage. For example, if this field

is configured as 93.5% and VDDIOMON Voltage = 1.8V, then the nominal under-voltage

threshold will be equal to 1.8 \* (93.5 / 100) = 1.683 V.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	MIN_95_5
literals	['MIN_95_5', 'MIN_95', 'MIN_94_5', 'MIN_94', 'MIN_93_5', 'MIN_93', 'M↔ IN_92_5', 'MIN_92', 'MIN_91_5', 'MIN_91', 'MIN_90_5', 'MIN_90', 'MIN← _97_5', 'MIN_97', 'MIN_96_5', 'MIN_96']

#### 4.183 Parameter PmicVddioMonitorOVThreshold

Controls the over-voltage threshold of the VDDIO input pin (VDDIOOVTH\_OTP[3:0]).

The threshold is relative to the configured nominal voltage. For example, if this field

is configured as 106.5% and VDDIOMON Voltage = 1.8V, then the nominal over-voltage

threshold will be equal to 1.8 \* (106.5 / 100) = 1.917 V.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	MAX_104_5
literals	

### 4.184 Parameter PmicVddioMonitorUVDebounce

 $Configures \ the \ under-voltage \ filtering \ time \ (debounce) \ of \ the \ VDDIO \ input \ pin \ (UV\_VDDIO\_OTP[1:0]).$ 

When the monitored voltage is below the nominal under-voltage threshold, this field represents the amount of time to wait until the under-voltage condition is asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TIME_25US
literals	['TIME_5US', 'TIME_15US', 'TIME_25US', 'TIME_40US']

## 4.185 Parameter PmicVddioMonitorOVDebounce

Configures the over-voltage filtering time (debounce) of the VDDIO input pin (OV\_VDDIO\_OTP).

When the monitored voltage is above the nominal over-voltage threshold, this field represents the

amount of time to wait until the over-voltage condition is asserted.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TIME_25US
literals	['TIME_25US', 'TIME_45US']

#### 4.186 Parameter PmicVddioMonitorPGOODAssert

Configures whether the PGOOD output signal is asserted low or not by the FS\_LOGIC when the assigned regulator monitored by VDDIOMON is in under-voltage or over-voltage (PGOOD\_VDDIO\_OTP).

PGOOD is an open-drain output that can be connected in the application to the PORB of the MCU.

PGOOD requires an external pull-up resistor to VDDIO and a filtering capacitor to GND for immunity.

When PGOOD is asserted low, RSTB and FS0B are also asserted low.

0 - PGOOD assertion is Disabled

1 - PGOOD assertion is Enabled

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

#### 4.187 Parameter PmicVddioMonitorABIST1Enable

Configures whether VDDIOMON is checked by ABIST1 or not (ABIST1\_VDDIO\_OTP).

The Fail-Safe State Machine includes two ABISTs to verify the correct functionality of the safety analog monitoring. ABIST1 is executed automatically after each POR or after each wake-up from Standby. In case of ABIST1 fail, RSTB and PGOOD are released, but FS0B remains stuck low and cannot be released.

It is recommended to verify latent faults on VCOREMON, HVLDOMON, and VDDIOMON during ABIST1, while the latent faults on VMONx can be verified either during ABIST1 or ABIST2.

- 0 VDDIOMON check by ABIST1 is Disabled
- 1 VDDIOMON check by ABIST1 is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

#### 4.188 Container PmicHVLdoMonitor

This container contains the configuration parameters for the voltage monitoring of the HVLDO regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

### 4.189 Parameter PmicHVLdoEnableMonitor

This field is used to enable/disable the voltage monitoring of the HVLDO regulator (HVLDO\_VMON\_EN\_OTP).

0 -  $\operatorname{HVLDOMON}$  is Disabled

1 -  $\operatorname{HVLDOMON}$  is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

## ${\bf 4.190 \quad Parameter \ PmicHVLdoMonitorVoltage}$

Controls the nominal voltage of the HVLDO regulator (HVLDO\_V\_OTP[1:0]).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	OUT_0V8
literals	['OUT_0V8', 'OUT_3V3']

### 4.191 Parameter PmicHVLdoMonitorUVThreshold

Controls the under-voltage threshold of the HVLDO regulator (HVLDO\_VMON\_UVTH\_OTP[3:0]).

The threshold is relative to the configured nominal voltage. For example, if this field

is configured as 93.5% and HVLDOMON Voltage = 0.8V, then the nominal under-voltage

threshold will be equal to 0.8 \* (93.5 / 100) = 0.748 V.

Note: Implementation Specific Parameter.

Property	Value	
type	ECUC-ENUMERATION-PARAM-DEF	
origin	NXP	
symbolicNameValue	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	false	
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE	
	VARIANT-PRE-COMPILE: PRE-COMPILE	
defaultValue	MIN_95_5	
literals	['MIN_95_5', 'MIN_95', 'MIN_94_5', 'MIN_94', 'MIN_93_5', 'MIN_93', 'M↔ IN_92_5', 'MIN_92', 'MIN_91_5', 'MIN_91', 'MIN_90_5', 'MIN_90', 'MIN← _97_5', 'MIN_97', 'MIN_96_5', 'MIN_96']	

### 4.192 Parameter PmicHVLdoMonitorOVThreshold

Controls the over-voltage threshold of the HVLDO regulator (HVLD\_VMON\_OVTH\_OTP[3:0]).

The threshold is relative to the configured nominal voltage. For example, if this field is configured as 106.5% and HVLDOMON Voltage = 0.8V, then the nominal over-voltage threshold will be equal to 0.8 \* (106.5 / 100) = 0.852 V.

Note: Implementation Specific Parameter.

Property	Value	
type	ECUC-ENUMERATION-PARAM-DEF	
origin	NXP	
${\it symbolic} Name Value$	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	false	
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE	
	VARIANT-PRE-COMPILE: PRE-COMPILE	
defaultValue	MAX_104_5	
literals	$['MAX\_104\_5', 'MAX\_105', 'MAX\_105\_5', 'MAX\_106', 'MAX\_106\_5', 'M \leftarrow]$	
	AX_107', 'MAX_107_5', 'MAX_108', 'MAX_108_5', 'MAX_109', 'MAX_	
	109_5', 'MAX_110', 'MAX_102_5', 'MAX_103', 'MAX_103_5', 'MAX_104']	

#### $Parameter\ PmicHVL do Monitor UV Debounce$ 4.193

Configures the under-voltage filtering time (debounce) of the HVLDO regulator (UV\_HVLDO\_OTP[1:0]). When the monitored voltage is below the nominal under-voltage threshold, this field represents the amount of time to wait until the under-voltage condition is asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TIME_25US
literals	['TIN <b>\$32</b> 5pint1CTintevel5US', 'TIME_25US', 'TIMEX140\$45hic

130 onductors

### 4.194 Parameter PmicHVLdoMonitorOVDebounce

Configures the over-voltage filtering time (debounce) of the HVLDO regulator (OV HVLDO OTP).

When the monitored voltage is above the nominal over-voltage threshold, this field represents the amount of time to wait until the over-voltage condition is asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TIME_25US
literals	['TIME_25US', 'TIME_45US']

#### 4.195 Parameter PmicHVLdoMonitorPGOODAssert

Configures whether the PGOOD output signal is asserted low or not by the FS\_LOGIC when the assigned regulator monitored by HVLDOMON is in under-voltage or over-voltage (PGOOD\_HVLDO\_VMON\_OTP).

PGOOD is an open-drain output that can be connected in the application to the PORB of the MCU.

PGOOD requires an external pull-up resistor to VDDIO and a filtering capacitor to GND for immunity.

When PGOOD is asserted low, RSTB and FS0B are also asserted low.

- 0 PGOOD assertion is Disabled
- 1 PGOOD assertion is Enabled

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

### 4.196 Parameter PmicHVLdoMonitorABIST1Enable

Configures whether HVLDOMON is checked by ABIST1 or not (ABIST1\_HVLDO\_VMON\_OTP).

The Fail-Safe State Machine includes two ABISTs to verify the correct functionality of the safety analog monitoring. ABIST1 is executed automatically after each POR or after each wake-up from Standby. In case of ABIST1 fail, RSTB and PGOOD are released, but FS0B remains stuck low and cannot be released.

It is recommended to verify latent faults on VCOREMON, HVLDOMON, and VDDIOMON during ABIST1, while the latent faults on VMONx can be verified either during ABIST1 or ABIST2.

- 0 HVLDOMON check by ABIST1 is Disabled
- 1 HVLDOMON check by ABIST1 is Enabled

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

### 4.197 Container PmicVmon1Monitor

This container contains the configuration parameters for the voltage monitoring of the VMON1 input pin.

VMON1 input pin can be be connected to VPRE, LDO1-3, BUCK2 (in case BUCK2 is not used in multiphase), BUCK3,

or an external regulator. The configuration of which regulator is connected to VMON1 is given in the M VMON REG register.

If an external regulator is connected to VMON1, then only a flag is reported to the MCU which then must decide the appropriate action to perform.

Warning: An external resistor bridge must be connected to VMON1 and it shall be calculated to deliver a middle point of 0.8V. It is recommended to use +/-1% or less resistor accuracy.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

#### 4.198 Parameter PmicVmon1EnableMonitor

This field is used to enable/disable the voltage monitoring of the VMON1 input pin (VMON1\_EN\_OTP).

- 0 VMON1 is Disabled
- 1 VMON1 is Enabled

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

# 4.199 Parameter PmicVmon1MonitorVoltage

Controls the nominal voltage of the VMON1 input pin.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	0.8

# 4.200 Parameter PmicVmon1MonitorUVThreshold

Controls the under-voltage threshold of the VMON1 input pin (VMON1UVTH\_OTP[3:0]).

The threshold is relative to the configured nominal voltage. For example, if this field is configured as 93.5% and VMON1 Voltage = 0.8V, then the nominal under-voltage threshold will be equal to 0.8 \* (93.5 / 100) = 0.748 V.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	MIN_95_5
literals	['MIN_95_5', 'MIN_95', 'MIN_94_5', 'MIN_94', 'MIN_93_5', 'MIN_93', 'M↔ IN_92_5', 'MIN_92', 'MIN_91_5', 'MIN_91', 'MIN_90_5', 'MIN_90', 'MIN← _97_5', 'MIN_97', 'MIN_96_5', 'MIN_96']

# 4.201 Parameter PmicVmon1MonitorOVThreshold

Controls the over-voltage threshold of the VMON1 input pin (VMON1OVTH\_OTP[3:0]).

The threshold is relative to the configured nominal voltage. For example, if this field

is configured as 106.5% and VMON1 Voltage = 0.8V, then the nominal over-voltage

threshold will be equal to 0.8 \* (106.5 / 100) = 0.852 V.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	MAX_104_5
literals	['MAX_104_5', 'MAX_105', 'MAX_105_5', 'MAX_106', 'MAX_106_5', 'M\Lefta AX_107', 'MAX_107_5', 'MAX_108', 'MAX_108_5', 'MAX_109', 'MAX_\Lefta AX_108_5', 'MAX_108_5', 'MAX_108_5
	109_5', 'MAX_110', 'MAX_102_5', 'MAX_103', 'MAX_103_5', 'MAX_104']

# 4.202 Parameter PmicVmon1MonitorUVDebounce

amount of time to wait until the under-voltage condition is asserted.

Configures the under-voltage filtering time (debounce) of the VMON1 input pin (UV\_VMON1\_OTP[1:0]). When the monitored voltage is below the nominal under-voltage threshold, this field represents the

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TIME_25US
literals	['TIME_5US', 'TIME_15US', 'TIME_25US', 'TIME_40US']

### 4.203 Parameter PmicVmon1MonitorOVDebounce

Configures the over-voltage filtering time (debounce) of the VMON1 input pin (OV\_VMON1\_OTP). When the monitored voltage is above the nominal over-voltage threshold, this field represents the amount of time to wait until the over-voltage condition is asserted.

Note: Implementation Specific Parameter.

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Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigCiasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue S	$71ME_{25}US_{12}$
literals	['TIME_25US', 'TIME_45US']

### 4.204 Parameter PmicVmon1MonitorPGOODAssert

Configures whether the PGOOD output signal is asserted low or not by the FS\_LOGIC when the assigned regulator monitored by VMON1 is in under-voltage or over-voltage (PGOOD\_VMON1\_OTP).

PGOOD is an open-drain output that can be connected in the application to the PORB of the MCU.

PGOOD requires an external pull-up resistor to VDDIO and a filtering capacitor to GND for immunity.

When PGOOD is asserted low, RSTB and FS0B are also asserted low.

- 0 PGOOD assertion is Disabled
- 1 PGOOD assertion is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

#### 4.205 Parameter PmicVmon1MonitorABIST1Enable

Configures whether VMON1 is checked by ABIST1 or not (ABIST1\_VMON1\_OTP).

The Fail-Safe State Machine includes two ABISTs to verify the correct functionality of the safety analog monitoring. ABIST1 is executed automatically after each POR or after each wake-up from Standby. In case of ABIST1 fail, RSTB and PGOOD are released, but FS0B remains stuck low and cannot be released.

It is recommended to verify latent faults on VCOREMON, HVLDOMON, and VDDIOMON during ABIST1, while the latent faults on VMONx can be verified either during ABIST1 or

#### ABIST2.

- 0 VMON1 check by ABIST1 is Disabled
- 1 VMON1 check by ABIST1 is Enabled

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

#### 4.206 Container PmicVmon2Monitor

This container contains the configuration parameters for the voltage monitoring of the VMON2 input pin.

VMON2 input pin can be be connected to VPRE, LDO1-3, BUCK2 (in case BUCK2 is not used in multiphase), BUCK3,

or an external regulator. The configuration of which regulator is connected to VMON2 is given in the M\_VMON\_REG register.

If an external regulator is connected to VMON2, then only a flag is reported to the MCU which then must decide the appropriate action to perform.

Warning: An external resistor bridge must be connected to VMON2 and it shall be calculated to deliver a middle point of 0.8V. It is recommended to use +/- 1% or less resistor accuracy.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# 4.207 Parameter PmicVmon2EnableMonitor

This field is used to enable/disable the voltage monitoring of the VMON2 input pin (VMON2\_EN\_OTP).

- 0 VMON2 is Disabled
- 1 VMON2 is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

# ${\bf 4.208} \quad {\bf Parameter} \ {\bf PmicVmon2MonitorVoltage}$

Controls the nominal voltage of the VMON2 input pin.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	0.8

### 4.209 Parameter PmicVmon2MonitorUVThreshold

Controls the under-voltage threshold of the VMON2 input pin (VMON2UVTH\_OTP[3:0]).

The threshold is relative to the configured nominal voltage. For example, if this field

is configured as 93.5% and VMON2 Voltage = 0.8V, then the nominal under-voltage

threshold will be equal to 0.8 \* (93.5 / 100) = 0.748 V.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	MIN_95_5
literals	['MIN_95_5', 'MIN_95', 'MIN_94_5', 'MIN_94', 'MIN_93_5', 'MIN_93', 'M↔ IN_92_5', 'MIN_92', 'MIN_91_5', 'MIN_91', 'MIN_90_5', 'MIN_90', 'MIN← _97_5', 'MIN_97', 'MIN_96_5', 'MIN_96']

#### 4.210 Parameter PmicVmon2MonitorOVThreshold

Controls the over-voltage threshold of the VMON2 input pin (VMON2OVTH\_OTP[3:0]).

The threshold is relative to the configured nominal voltage. For example, if this field

is configured as 106.5% and VMON2 Voltage = 0.8V, then the nominal over-voltage

threshold will be equal to 0.8 \* (106.5 / 100) = 0.852 V.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	MAX_104_5
literals	

# 4.211 Parameter PmicVmon2MonitorUVDebounce

Configures the under-voltage filtering time (debounce) of the VMON2 input pin (UV\_VMON2\_OTP[1:0]). When the monitored voltage is below the nominal under-voltage threshold, this field represents the

amount of time to wait until the under-voltage condition is asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TIME_25US
literals	['TIME_5US', 'TIME_15US', 'TIME_25US', 'TIME_40US']

# 4.212 Parameter PmicVmon2MonitorOVDebounce

Configures the over-voltage filtering time (debounce) of the VMON2 input pin (OV\_VMON2\_OTP).

When the monitored voltage is above the nominal over-voltage threshold, this field represents the

amount of time to wait until the over-voltage condition is asserted.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TIME_25US
literals	['TIME_25US', 'TIME_45US']

### 4.213 Parameter PmicVmon2MonitorPGOODAssert

Configures whether the PGOOD output signal is asserted low or not by the FS\_LOGIC when the assigned regulator monitored by VMON2 is in under-voltage or over-voltage (PGOOD\_VMON2\_OTP).

PGOOD is an open-drain output that can be connected in the application to the PORB of the MCU.

PGOOD requires an external pull-up resistor to VDDIO and a filtering capacitor to GND for immunity.

When PGOOD is asserted low, RSTB and FS0B are also asserted low.

- 0 PGOOD assertion is Disabled
- 1 PGOOD assertion is Enabled

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

### 4.214 Parameter PmicVmon2MonitorABIST1Enable

Configures whether VMON2 is checked by ABIST1 or not (ABIST1\_VMON2\_OTP).

The Fail-Safe State Machine includes two ABISTs to verify the correct functionality of the safety analog monitoring. ABIST1 is executed automatically after each POR or after each wake-up from Standby. In case of ABIST1 fail, RSTB and PGOOD are released, but FS0B remains stuck low and cannot be released.

It is recommended to verify latent faults on VCOREMON, HVLDOMON, and VDDIOMON during ABIST1, while the latent faults on VMONx can be verified either during ABIST1 or ABIST2.

- 0 VMON2 check by ABIST1 is Disabled
- 1 VMON2 check by ABIST1 is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

### 4.215 Container PmicVmon3Monitor

This container contains the configuration parameters for the voltage monitoring of the VMON3 input pin.

VMON3 input pin can be be connected to VPRE, LDO1-3, BUCK2 (in case BUCK2 is not used in multiphase), BUCK3,

or an external regulator. The configuration of which regulator is connected to VMON3 is given in the M\_VMON\_REG register.

If an external regulator is connected to VMON3, then only a flag is reported to the MCU which then must decide the appropriate action to perform.

Warning: An external resistor bridge must be connected to VMON3 and it shall be calculated to deliver a middle point of 0.8V. It is recommended to use +/- 1% or less resistor accuracy. Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

### 4.216 Parameter PmicVmon3EnableMonitor

This field is used to enable/disable the voltage monitoring of the VMON3 input pin (VMON3\_EN\_OTP).

- 0 VMON3 is Disabled
- 1 VMON3 is Enabled

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

# 4.217 Parameter PmicVmon3MonitorVoltage

Controls the nominal voltage of the VMON3 input pin.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	0.8

# 4.218 Parameter PmicVmon3MonitorUVThreshold

Controls the under-voltage threshold of the VMON3 input pin (VMON3UVTH\_OTP[3:0]).

The threshold is relative to the configured nominal voltage. For example, if this field

is configured as 93.5% and VMON3 Voltage = 0.8V, then the nominal under-voltage

threshold will be equal to 0.8 \* (93.5 / 100) = 0.748 V.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigCiasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	MIN_95_5
literals	['MIN_95_5', 'MIN_95', 'MIN_94_5', 'MIN_94', 'MIN_93_5', 'MIN_93', 'M↔
	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$
NXP Semiconductors	_97_5', 'MIN_97', 'MIN_96_5', 'MIN_96']   <b>S32 PMIC Driver</b> 147

### 4.219 Parameter PmicVmon3MonitorOVThreshold

Controls the over-voltage threshold of the VMON3 input pin (VMON3OVTH\_OTP[3:0]).

The threshold is relative to the configured nominal voltage. For example, if this field

is configured as 106.5% and VMON3 Voltage = 0.8V, then the nominal over-voltage

threshold will be equal to 0.8 \* (106.5 / 100) = 0.852 V.

Note: Implementation Specific Parameter.

Property	Value	
type	ECUC-ENUMERATION-PARAM-DEF	
origin	NXP	
symbolicNameValue	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	false	
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE	
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE	
defaultValue	MAX_104_5	
literals		

### 4.220 Parameter PmicVmon3MonitorUVDebounce

Configures the under-voltage filtering time (debounce) of the VMON3 input pin (UV\_VMON3\_OTP[1:0]).

When the monitored voltage is below the nominal under-voltage threshold, this field represents the amount of time to wait until the under-voltage condition is asserted.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A

Property	Value
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TIME_25US
literals	['TIME_5US', 'TIME_15US', 'TIME_25US', 'TIME_40US']

#### 4.221 Parameter PmicVmon3MonitorOVDebounce

Configures the over-voltage filtering time (debounce) of the VMON3 input pin (OV\_VMON3\_OTP). When the monitored voltage is above the nominal over-voltage threshold, this field represents the amount of time to wait until the over-voltage condition is asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TIME_25US
literals	['TIME_25US', 'TIME_45US']

#### 4.222 Parameter PmicVmon3MonitorPGOODAssert

Configures whether the PGOOD output signal is asserted low or not by the FS\_LOGIC when the assigned regulator monitored by VMON3 is in under-voltage or over-voltage (PGOOD\_VMON3\_OTP).

PGOOD is an open-drain output that can be connected in the application to the PORB of the MCU.

PGOOD requires an external pull-up resistor to VDDIO and a filtering capacitor to GND for immunity.

When PGOOD is asserted low, RSTB and FS0B are also asserted low.

0 - PGOOD assertion is Disabled

1 - PGOOD assertion is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

#### 4.223 Parameter PmicVmon3MonitorABIST1Enable

Configures whether VMON3 is checked by ABIST1 or not (ABIST1 VMON3 OTP).

The Fail-Safe State Machine includes two ABISTs to verify the correct functionality of the safety analog monitoring. ABIST1 is executed automatically after each POR or after each wake-up from Standby. In case of ABIST1 fail, RSTB and PGOOD are released, but FS0B remains stuck low and cannot be released.

It is recommended to verify latent faults on VCOREMON, HVLDOMON, and VDDIOMON during ABIST1, while the latent faults on VMONx can be verified either during ABIST1 or ABIST2.

- 0 VMON3 check by ABIST1 is Disabled
- 1 VMON3 check by ABIST1 is Enabled

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

#### 4.224 Container PmicVmon4Monitor

This container contains the configuration parameters for the voltage monitoring of the VMON4 input pin.

VMON4 input pin can be be connected to VPRE, LDO1-3, BUCK2 (in case BUCK2 is not used in multiphase), BUCK3,

or an external regulator. The configuration of which regulator is connected to VMON4 is given in the  $M_VMON_REG$  register.

If an external regulator is connected to VMON4, then only a flag is reported to the MCU which then must decide the appropriate action to perform.

Warning: An external resistor bridge must be connected to VMON4 and it shall be calculated to deliver a middle point of 0.8V. It is recommended to use +/-1% or less resistor accuracy.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# 4.225 Parameter PmicVmon4EnableMonitor

This field is used to enable/disable the voltage monitoring of the VMON4 input pin (VMON4\_EN\_OTP).

- 0 VMON4 is Disabled
- 1 VMON4 is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

# ${\bf 4.226} \quad {\bf Parameter} \ {\bf PmicVmon4MonitorVoltage}$

Controls the nominal voltage of the VMON4 input pin.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
${\it symbolic} Name Value$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	0.8

### 4.227 Parameter PmicVmon4MonitorUVThreshold

Controls the under-voltage threshold of the VMON4 input pin (VMON4UVTH\_OTP[3:0]).

The threshold is relative to the configured nominal voltage. For example, if this field

is configured as 93.5% and VMON4 Voltage = 0.8V, then the nominal under-voltage

threshold will be equal to 0.8 \* (93.5 / 100) = 0.748 V.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	MIN_95_5
literals	['MIN_95_5', 'MIN_95', 'MIN_94_5', 'MIN_94', 'MIN_93_5', 'MIN_93', 'M↔ IN_92_5', 'MIN_92', 'MIN_91_5', 'MIN_91', 'MIN_90_5', 'MIN_90', 'MIN← _97_5', 'MIN_97', 'MIN_96_5', 'MIN_96']

### 4.228 Parameter PmicVmon4MonitorOVThreshold

Controls the over-voltage threshold of the VMON4 input pin (VMON4OVTH\_OTP[3:0]).

The threshold is relative to the configured nominal voltage. For example, if this field

is configured as 106.5% and VMON4 Voltage = 0.8V, then the nominal over-voltage

threshold will be equal to 0.8 \* (106.5 / 100) = 0.852 V.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	MAX_104_5
literals	['MAX_104_5', 'MAX_105', 'MAX_105_5', 'MAX_106', 'MAX_106_5', 'M↔
	$AX_{107}', 'MAX_{107}_{5}', 'MAX_{108}', 'MAX_{108}_{5}', 'MAX_{109}', 'MAX_{\leftarrow}$
	109_5', 'MAX_110', 'MAX_102_5', 'MAX_103', 'MAX_103_5', 'MAX_104']

# 4.229 Parameter PmicVmon4MonitorUVDebounce

amount of time to wait until the under-voltage condition is asserted.

Configures the under-voltage filtering time (debounce) of the VMON4 input pin (UV\_VMON4\_OTP[1:0]). When the monitored voltage is below the nominal under-voltage threshold, this field represents the

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TIME_25US
literals	['TIME_5US', 'TIME_15US', 'TIME_25US', 'TIME_40US']

# 4.230 Parameter PmicVmon4MonitorOVDebounce

Configures the over-voltage filtering time (debounce) of the VMON4 input pin (OV\_VMON4\_OTP).

When the monitored voltage is above the nominal over-voltage threshold, this field represents the

amount of time to wait until the over-voltage condition is asserted.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TIME_25US
literals	['TIME_25US', 'TIME_45US']

### 4.231 Parameter PmicVmon4MonitorPGOODAssert

Configures whether the PGOOD output signal is asserted low or not by the FS\_LOGIC when the assigned regulator monitored by VMON4 is in under-voltage or over-voltage (PGOOD\_VMON4\_OTP).

PGOOD is an open-drain output that can be connected in the application to the PORB of the MCU.

PGOOD requires an external pull-up resistor to VDDIO and a filtering capacitor to GND for immunity.

When PGOOD is asserted low, RSTB and FS0B are also asserted low.

0 - PGOOD assertion is Disabled

1 - PGOOD assertion is Enabled

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

### 4.232 Parameter PmicVmon4MonitorABIST1Enable

Configures whether VMON4 is checked by ABIST1 or not (ABIST1\_VMON4\_OTP). The Fail-Safe State Machine includes two ABISTs to verify the correct functionality of the safety analog monitoring. ABIST1 is executed automatically after each POR or after each wake-up from Standby. In case of ABIST1 fail, RSTB and PGOOD are released, but FS0B remains stuck low and cannot be released.

It is recommended to verify latent faults on VCOREMON, HVLDOMON, and VDDIOMON during ABIST1, while the latent faults on VMONx can be verified either during ABIST1 or ABIST2.

- 0 VMON4 check by ABIST1 is Disabled
- 1 VMON4 check by ABIST1 is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

# 4.233 Container PmicCommunicationConfiguration

This container contains the configuration for the communication.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

#### 4.234 Parameter PmicI2cCommunicationMethod

Configures the mechanism used to communicate with the PMIC device (synchronous or asynchronous).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	SYNCHRONOUS
literals	['SYNCHRONOUS']

#### 4.235 Reference PmicI2cChannelRef

Reference to the I2C channel configuration used to communicate with the PMIC, which is set in the I2C driver configuration.

Warning: The driver will use the I2C addresses configured by OTP

 $(i.e.\ PmicOtpMainUnitConfiguration/PmicOtpDeviceConfiguration/PmicMainI2cAddress) and the property of the p$ 

for the Main Unit and PmicOtpFailSafeUnitConfiguration/PmicOtpSafetyConfiguration/

PmicSafetyI2cAddress for the Fail-Safe Unit).

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
${\it requires Symbolic Name Value}$	False
destination	/AUTOSAR/EcucDefs/I2c/I2cGlobalConfig/I2cChannel

# 4.236 Reference PmicI2CSCLPinRef

Reference to the SCL pin of the I2C channel used to communicate with the PMIC. This is pin will

be manually toggled in order to unlock the I2C bus should it get erroneously stuck.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
${\it requires Symbolic Name Value}$	False
destination	/ AUTOSAR/EcucDefs/Port/PortConfigSet/PortContainer/PortPin

# 4.237 Reference PmicI2CSCLDioRef

Reference to the Dio channel of the SCL pin of the I2C channel used to communicate with the PMIC. This Dio channel

will be used to toggle the pin repeatedly in order to unlock the I2C bus should it get erroneously stuck.

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
${\it requires Symbolic Name Value}$	False
destination	/AUTOSAR/EcucDefs/Dio/DioConfig/DioPort/DioChannel

# 4.238 Container PmicClockSettingConfig

This container contains the configuration for the Clock settings of the PMIC.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • PmicClockReferencePoint

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE

# 4.239 Parameter PmicClockSettingId

The ID of this PmicClockSettingConfig to be used as argument for the API call Pmic\_InitClock.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	true
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigCiasses	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	0
max	255
min	0

# ${\bf 4.240 \quad Parameter \ PmicIrcoscFrequencyHz}$

Internal Oscillator Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	F_20000000
literals	['F_16000000', 'F_17000000', 'F_18000000', 'F_19000000', 'F_20000000', 'F_21000000', 'F_22000000', 'F_23000000', 'F_24000000']

# 4.241 Parameter PmicLowPowerOscFrequencyHz

Low Power Oscillator Frequency [Hz] (LOW\_POWER\_CLOCK[1:0]).

This oscillator is used only in the low power standby mode

and has an accuracy of +/-10%.

The main purpose of this oscillator is to reduce the current

consumption of the device during the standby mode.

It is recommended to use the 600KHz setting for DDR self-refresh.

Warning: A frequency change of LPOSC needs

to be programmed at least 40us prior to transitioning the

VR5510 device into Standby Mode.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	F_100000
literals	['F_100000', 'F_300000', 'F_600000']

# 4.242 Parameter PmicFinEnable

This field is used to enable/disable the FIN pin (EXT\_FIN\_DIS) .

- 0 FIN Pin is Disabled
- 1 FIN Pin is Enabled

The PLL shall also be enabled by OTP in order to synchronize the switching regulators.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

# 4.243 Parameter PmicExternalPIN\_Fin\_FrequencyHz

FIN Reference Frequency [Hz] (CLK\_FIN\_DIV).

The input frequency range of FIN must be between 333KHz-500kHz or 2MHz-3MHz.

If the external frequency coming from the FIN pin at runtime is out of range,

CLK moves back to the internal oscillator and an error is reported through

the  $CLK_FIN_DIV_OK$  bit.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	333000.0
max	3000000.0
min	333000.0

# 4.244 Parameter PmicPllClockSelection

Configures the PLL Source Selection (EXT\_FIN\_SEL).

Warning: The PLL is enabled/disabled via the OTP settings.

This field is not editable unless the PLL is enabled

(PmicOtpMainUnitConfiguration/PmicOtpDeviceConfiguration/PmicPllEnable = 'true').

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	IRCOSC_CLK
literals	['IRCOSC_CLK', 'FIN_CLK']

# 4.245 Parameter PmicSpectrumModulationEnable

This field is used to enable/disable the spread spectrum modulation feature (MOD\_EN) .

- 0 Spread Spectrum Modulation is Disabled
- 1 Spread Spectrum Modulation is Enabled

The main purpose of the spread spectrum modulation is to improve the EMC performance

by spreading the energy of the internal oscillator and VPRE frequency on VBAT

frequency spectrum.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
S	32 ARIANT POST-BUILD: POST-BUILD NX
defaultValue	false

### 4.246 Parameter PmicTriangularCarrierFrequencyHz

Triangular Carrier Frequency [Hz] (MOD\_CONF).

The spread spectrum modulation has a  $\pm -5\%$  deviation range around

the center of the oscillator frequency.

It is recommended to select 23.15KHz carrier frequency when VPRE is

configured at 455KHz and 92.6KHz when VPRE is configured at 2.22MHz

for best performance.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	F_23150
literals	['F_23150', 'F_92600']

# 4.247 Parameter PmicFoutMuxSelection

Configures which clock to be sent to the FOUT pin (FOUT\_MUX\_SEL[3:0]).

The FOUT pin can be used to synchronize an external device with the VR5510.

Warning: The function of the AMUX/FOUT pin is selected via the OTP settings.

This field is not editable unless the AMUX/FOUT pin is configured as FOUT

 $(PmicOtpMainUnitConfiguration/PmicOtpMainIOConfiguration/PmicAmuxFoutPinMode = 'FOUT\_MODE'). \\$ 

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF

Property	Value
origin	NXP
${\it symbolic} Name Value$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	DISABLED
literals	['DISABLED', 'VPRE_CLK', 'BOOST_CLK', 'BUCK1_CLK', 'BUCK2_CLK', 'BUCK3_CLK', 'FOUT_CLK', 'CLK20M_MAIN_DIV48', 'CLK20M_FS_D← IV48', 'CLK_FIN_DIV']

# 4.248 Parameter PmicFoutClockSelection

Configures the FOUT Source Selection (FOUT\_CLK\_SEL).

This field is editable only when  $PmicFoutMuxSelection = FOUT\_CLK$ 

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigCiasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	CLK2
literals	['CLK1', 'CLK2']

# ${\bf 4.249} \quad {\bf Parameter\ PmicFoutPhaseDelay}$

Controls the phase delay of the FOUT\_CLK (FOUT\_PHASE[2:0]).

This field is editable only when PmicFoutMuxSelection = FOUT\_CLK

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	7
min	0

# 4.250 Parameter PmicClk1Frequency

CLK1 Reference Frequency [Hz].

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	2222000.0
max	2666666.0
min	1777777.0

# 4.251 Parameter PmicClk2Frequency

CLK2 Reference Frequency [Hz].

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	455000.0
max	545454.0
min	363636.0

### 4.252 Container PmicClockReferencePoint

This container defines a reference point for every possible frequency of the PMIC Clock Tree.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	6
upperMultiplicity	6
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# ${\bf 4.253 \quad Parameter \ PmicClockFrequencySelect}$

 $Select\ clock\ source\ for\ the\ specific\ instance\ of\ the\ PmicClockReference Point\ container.$ 

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
${\it symbolic} Name Value$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	VPRE_CLK
literals	['VPRE_CLK', 'BOOST_CLK', 'BUCK1_CLK', 'BUCK2_CLK', 'BUCK3_← CLK', 'FOUT_CLK']

# ${\bf 4.254} \quad {\bf Parameter\ PmicClockReferencePointFrequency}$

This is the frequency for the specific instance of the PmicClockReferencePoint container.

Calculated value.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	455000.0
max	3500000.0
min	0.0

# ${\bf 4.255} \quad {\bf Container\ PmicModeSettingConf}$

This container contains the configuration for the Mode setting of the PMIC.

Note: Implementation Specific Parameter.

Included subcontainers:

- PmicRegulatorsConfiguration
- $\bullet \ \ PmicVMONConfiguration$

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE

### 4.256 Parameter PmicModeID

This parameter shall represent the ID of the PMIC mode.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	true
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	0
max	255
min	0

### 4.257 Parameter PmicModeSelection

This parameter selects the Mode to be used.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	NORMAL
literals	['NORMAL', 'RESET', 'SHUTDOWN', 'STANDBY', 'DEEPSLEEP']

## 4.258 Parameter PmicPWRON2DeepSleepModeEnable

This field is used to enable/disable the entry to DeepSleep Mode by toggling the PWRON2 pin  $(M\_MODE[PWRON2\_DSM\_N])$ 

0 - PWRON2 (high-to-low) transition cannot trigger DSM

1 - PWRON2 (high-to-low) transition can trigger DSM

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

## ${\bf 4.259 \quad Parameter \ Pmic PWRON1Wake Up Enable}$

This field is used to enable/disable the wake-up functionality of the PWRON1 pin (M\_MODE[PWRON1DIS]).

0 - PWRON1 Wakeup Disable

#### 1 - PWRON1 Wakeup Enable

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

## 4.260 Parameter PmicPWRON2WakeUpEnable

This field is used to enable/disable the wake-up functionality of the PWRON2 pin  $(M\_MODE[PWRON2DIS])$ .

#### 0 - PWRON2 Wakeup Disable

#### 1 - PWRON2 Wakeup Enable

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

#### 4.261 Parameter PmicStandbyTimerEnable

This field is used to enable/disable the standby transition timer (M\_SM\_CTRL1[STBY\_TIMER\_EN]).

- 0 Standby Transition Timer is Disabled
- 1 Standby Transition Timer is Enabled

The Standby Timer is implemented in the Main-Unit logic to automatically transition

the device to Deep Fail-Safe (DFS) mode in case of timeout during Standby mode.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	False
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

## 4.262 Parameter PmicStandbyTimerWindowDuration

Configures the standby timer window duration (M\_SM\_CTRL1[TIMER\_STBY\_WINDOW]).

Represents the amount of time to wait in Standby mode until a timeout is triggered,

after which the device will automatically transition to Deep Fail-Safe (DFS) mode.

This field is editable only when the standby timer is enabled

(i.e. PmicStandbyTimerEnable = 'true').

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	TIME_1024MS
literals	['TIME_16MS', 'TIME_32MS', 'TIME_128MS', 'TIME_512MS', 'TIME_ $\leftarrow$
	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$
	65536MS', 'TIME_131072MS', 'TIME_262144MS', 'TIME_524288MS', 'TIM
	E_1048576MS', 'TIME_2097152MS', 'TIME_4194304MS', 'TIME_8388608MS']

## 4.263 Container PmicRegulatorsConfiguration

This container contains the configuration parameters for the registers controlling the functionality of regulators.

Note: Implementation Specific Parameter.

Included subcontainers:

- $\bullet \ \ PmicVpreRegulator$
- $\bullet \ \, {\rm PmicVBoostRegulator} \\$
- $\bullet \ \ PmicHVL do Regulator$
- PmicBuck1Regulator
- $\bullet \ \ PmicBuck 2 Regulator$
- $\bullet \quad PmicBuck3Regulator$
- PmicLdo1Regulator
- PmicLdo2Regulator
- $\bullet \ \ PmicLdo3Regulator$

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

## 4.264 Container PmicVpreRegulator

This container contains the configuration parameters of the VPRE (HVBUCK) regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

## 4.265 Parameter PmicVpreEnableRegulator

This field is used to control the power state the VPRE (HVBUCK) regulator (M\_REG\_CTRL1[VPREDIS/VPREEN]).

NO\_EFFECT - Keep previous power state of VPRE

DISABLE - VPRE is Disabled

ENABLE - VPRE is Enabled

This field is modifiable only when PmicModeSelection = 'NORMAL'.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	NO_EFFECT
literals	['NO_EFFECT', 'DISABLE', 'ENABLE']

# ${\bf 4.266} \quad {\bf Parameter} \ {\bf PmicVpreStandbyOutputVoltage}$

Controls the output voltage of the VPRE (HVBUCK) regulator in STANDBY mode (M\_REG\_CTRL3[VPREV\_STBY]).

This field is modifiable only when PmicModeSelection = 'STANDBY' and VPRE Standby Voltage is enabled by OTP (i.e. PmicOtpMainUnitConfiguration/PmicOtpRegulatorsConfiguration/PmicVpreRegulator/PmicVpreStdbyVoltageCont = 'true').

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	OUT_3V0
literals	['OUT_3V3', 'OUT_3V0']

# 4.267 Parameter PmicVpreHsCurrentCapability

Controls the pull-up current capability of the HS (High-Side) gate driver of the VPRE (HVBUCK) regulator (M\_REG\_CTRL2[VPRESRHS]).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	I_130_MA
literals	['I_130_MA', 'I_260_MA', 'I_520_MA', 'I_900_MA']

### 4.268 Parameter PmicVpreLsCurrentCapability

Controls the pull-down current capability of the LS (Low-Side) gate driver of the VPRE (HVBUCK) regulator (M\_REG\_CTRL2[VPRESRLS]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	I_130_MA
literals	['I_130_MA', 'I_260_MA', 'I_520_MA', 'I_900_MA']

## 4.269 Container PmicVBoostRegulator

This container contains the configuration parameters of the BOOST regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

## 4.270 Parameter PmicBoostEnableRegulator

This field is used to control the power state the BOOST regulator (M\_REG\_CTRL1[BOOSTDIS/BOOSTEN]).

 $\ensuremath{\mathsf{NO}}\xspace$  EFFECT - Keep previous power state of BOOST

 $\ \, DISABLE \ \ \, -BOOST \ \, is \ \, Disabled \\$ 

ENABLE - BOOST is Enabled

This field is modifiable only when PmicModeSelection = 'NORMAL'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	NO_EFFECT
literals	['NO_EFFECT', 'DISABLE', 'ENABLE']

### 4.271 Parameter PmicBoostSlewRate

Controls the slew rate of the BOOST regulator (M\_REG\_CTRL2[VBSTSR]).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	RATE_500
literals	['RATE_100', 'RATE_300', 'RATE_500']

## 4.272 Container PmicHVLdoRegulator

This container contains the configuration parameters of the HVLDO regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

## 4.273 Parameter PmicHVLdoEnableRegulator

This field is used to control the power state the HVLDO regulator (M\_REG\_CTRL2[HVLDOEN/HVLDODIS]).

NO\_EFFECT - Keep previous power state of HVLDO

DISABLE - HVLDO is Disabled

ENABLE - HVLDO is Enabled

This field is modifiable only when PmicModeSelection = 'NORMAL'.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	NO_EFFECT
literals	['NO_EFFECT', 'DISABLE', 'ENABLE']

### 4.274 Parameter PmicHVLdoStandbyEnableRegulator

This field is used to enable/disable the HVLDO regulator in STANDBY mode (M\_REG\_CTRL3[HVLDO\_STBY]).

- 0 HVLDO in Standby Mode is Disabled
- 1 HVLDO in Standby Mode is Enabled

This field is modifiable only when PmicModeSelection = 'STANDBY'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# 4.275 Container PmicBuck1Regulator

This container contains the configuration parameters of the BUCK1 regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

### 4.276 Parameter PmicBuck1EnableRegulator

This field is used to control the power state the BUCK1 regulator (M\_REG\_CTRL1[BUCK1DIS/BUCK1EN]).

NO\_EFFECT - Keep previous power state of BUCK1

DISABLE - BUCK1 is Disabled

ENABLE - BUCK1 is Enabled

This field is modifiable only when PmicModeSelection = 'NORMAL'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	NO_EFFECT
literals	['NO_EFFECT', 'DISABLE', 'ENABLE']

# ${\bf 4.277} \quad {\bf Parameter\ PmicBuck 1 Standby Enable Regulator}$

This field is used to enable/disable the BUCK1 regulator in STANDBY mode (M\_REG\_CTRL3[BUCK1\_STBY]).

- 0 BUCK1 in Standby Mode is Disabled
- 1 BUCK1 in Standby Mode is Enabled

This field is modifiable only when PmicModeSelection = 'STANDBY'.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

### 4.278 Parameter PmicBuck1StandbyOutputVoltage

Controls the output voltage of the BUCK1 (and BUCK1/2 in dual-phase mode) regulator(s)

in STANDBY Mode (M\_LVB1\_STDBY\_DVS[BUCK1\_STBY]).

BUCK1 (BUCK1/2 in dual-phase mode) is intended to supply the MCU core voltage.

The output voltage must have a resolution of 6.25 mV.

This field is modifiable only when PmicModeSelection = 'STANDBY'

and PmicBuck1StandbyEnableRegulator = 'true'.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.4
max	1.8
min	0.4

## 4.279 Container PmicBuck2Regulator

This container contains the configuration parameters of the BUCK2 regulator.

The container is modifiable only when the BUCK2 regulator is not configured

to operate in dual-phase mode.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# ${\bf 4.280 \quad Parameter \ Pmic Buck 2 Enable Regulator}$

This field is used to control the power state the BUCK2 regulator (M\_REG\_CTRL1[BUCK2DIS/BUCK2EN]).

 $NO\_EFFECT$  - Keep previous power state of BUCK2

DISABLE - BUCK2 is Disabled

ENABLE - BUCK2 is Enabled

This field is modifiable only when PmicModeSelection = 'NORMAL'.

Note: Implementation Specific Parameter.

literals

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
${\it symbolic} Name Value$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
S	32 PMTC Driver BUILD: POST-BUILD NX
defaultValue	NO_EFFECT

['NO\_EFFECT', 'DISABLE', 'ENABLE']

### 4.281 Parameter PmicBuck2StandbyEnableRegulator

This field is used to enable/disable the BUCK2 regulator in STANDBY mode (M\_REG\_CTRL3[BUCK2\_STBY]).

- 0 BUCK2 in Standby Mode is Disabled
- 1 BUCK2 in Standby Mode is Enabled

This field is modifiable only when PmicModeSelection = 'STANDBY'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# 4.282 Container PmicBuck3Regulator

This container contains the configuration parameters of the BUCK3 regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

### 4.283 Parameter PmicBuck3EnableRegulator

This field is used to control the power state the BUCK3 regulator (M\_REG\_CTRL1[BUCK3DIS/BUCK3EN]).

NO\_EFFECT - Keep previous power state of BUCK3

DISABLE - BUCK3 is Disabled

ENABLE - BUCK3 is Enabled

This field is modifiable only when PmicModeSelection = 'NORMAL'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	NO_EFFECT
literals	['NO_EFFECT', 'DISABLE', 'ENABLE']

# ${\bf 4.284} \quad {\bf Parameter\ PmicBuck 3 Standby Enable Regulator}$

This field is used to enable/disable the BUCK3 regulator in STANDBY mode (M\_REG\_CTRL3[BUCK3\_STBY]).

- 0 BUCK3 in Standby Mode is Disabled
- 1 BUCK3 in Standby Mode is Enabled

This field is modifiable only when PmicModeSelection = 'STANDBY'.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

### 4.285 Container PmicLdo1Regulator

This container contains the configuration parameters of the LDO1 regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# ${\bf 4.286} \quad {\bf Parameter} \ {\bf PmicLdo1EnableRegulator}$

This field is used to control the power state the LDO1 regulator (M\_REG\_CTRL1[LDO1DIS/LDO1EN]).

NO\_EFFECT - Keep previous power state of LDO1

DISABLE - LDO1 is Disabled

ENABLE - LDO1 is Enabled

This field is modifiable only when PmicModeSelection = 'NORMAL'.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	NO_EFFECT
literals	['NO_EFFECT', 'DISABLE', 'ENABLE']

### 4.287 Parameter PmicLdo1StandbyEnableRegulator

This field is used to enable/disable the LDO1 regulator in STANDBY mode (M\_REG\_CTRL3[LDO1\_STBY]).

- 0 LDO1 in Standby Mode is Disabled
- 1 LDO1 in Standby Mode is Enabled

This field is modifiable only when PmicModeSelection = 'STANDBY'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# ${\bf 4.288}\quad {\bf Container\ PmicLdo2Regulator}$

This container contains the configuration parameters of the LDO2 regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

### 4.289 Parameter PmicLdo2EnableRegulator

This field is used to control the power state the LDO2 regulator (M\_REG\_CTRL1[LDO2DIS/LDO2EN]).

NO\_EFFECT - Keep previous power state of LDO2  $\,$ 

 $\ \, {\rm DISABLE} \ \, \text{-} \ \, {\rm LDO2} \ \, {\rm is} \ \, {\rm Disabled}$ 

 ${\bf ENABLE} \quad \text{-} \ {\bf LDO2} \ {\bf is} \ {\bf Enabled}$ 

This field is modifiable only when PmicModeSelection = 'NORMAL'.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	NO_EFFECT
literals	['NO_EFFECT', 'DISABLE', 'ENABLE']

## ${\bf 4.290 \quad Parameter \ PmicLdo 2 Standby Enable Regulator}$

This field is used to enable/disable the LDO2 regulator in STANDBY mode (M\_REG\_CTRL3[LDO2\_STBY]).

- 0 LDO2 in Standby Mode is Disabled
- 1 LDO2 in Standby Mode is Enabled

This field is modifiable only when PmicModeSelection = 'STANDBY'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# 4.291 Container PmicLdo3Regulator

This container contains the configuration parameters of the LDO3 regulator.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

### 4.292 Parameter PmicLdo3EnableRegulator

This field is used to control the power state the LDO3 regulator (M\_REG\_CTRL1[LDO3DIS/LDO3EN]).

NO\_EFFECT - Keep previous power state of LDO3

DISABLE - LDO3 is Disabled

ENABLE - LDO3 is Enabled

This field is modifiable only when PmicModeSelection = 'NORMAL'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	NO_EFFECT
literals	['NO_EFFECT', 'DISABLE', 'ENABLE']

## ${\bf 4.293 \quad Parameter \ PmicLdo 3 Standby Enable Regulator}$

This field is used to enable/disable the LDO3 regulator in STANDBY mode (M\_REG\_CTRL3[LDO3\_STBY]).

- 0 LDO3 in Standby Mode is Disabled
- 1 LDO3 in Standby Mode is Enabled

This field is modifiable only when PmicModeSelection = 'STANDBY'.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

## 4.294 Container PmicVMONConfiguration

This container contains the configuration parameters for the registers controlling the regulator assignments of the VMONx input pins.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

## 4.295 Parameter PmicVMON4RegulatorAssignment

Configures which regulator will be monitored by VMON4 (M\_VMON\_REGx[VMON4\_REG\_ASSIGN]).

The VMON4 input pin can be connected to VPRE, BOOST, LDO1-3, BUCK3, or an

external regulator (the choice depending on the configuration of this field).

The regulator connected to VMON4 MUST use an external resistor bridge

delivering a middle point of 0.8V to be compatible with over-voltage and under-voltage

monitoring thresholds.

Note: This field is modifiable only if VMON4 is enabled by OTP (i.e. PmicOtpFailSafeUnitConfiguration/PmicOtpVoltageMoni = 'true')

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	EXTERNAL_REGULATOR
literals	['EXTERNAL_REGULATOR', 'VPRE', 'LDO1', 'LDO2', 'BUCK3', 'BOOST', 'LDO3']

## 4.296 Parameter PmicVMON3RegulatorAssignment

Configures which regulator will be monitored by VMON3 (M\_VMON\_REGx[VMON3\_REG\_ASSIGN]).

The VMON3 input pin can be connected to VPRE, BOOST, LDO1-3, BUCK3, or an

external regulator (the choice depending on the configuration of this field).

The regulator connected to VMON3 MUST use an external resistor bridge

delivering a middle point of 0.8V to be compatible with over-voltage and under-voltage

monitoring thresholds.

Note: This field is modifiable only if VMON3 is enabled by OTP (i.e. PmicOtpFailSafeUnitConfiguration/PmicOtpVoltageMoni = 'true')

Property	Value	
type	ECUC-ENUMERATION-PARAM-DEF	
origin	NXP	
symbolicNameValue	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	true	
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE	
varueComigCiasses	VARIANT-POST-BUILD: POST-BUILD	
defaultValue	EXTERNAL_REGULATOR	
NiXePaSemiconductors	['EXTERNAL <b>SREGMIACTOR</b> ivelyPRE', 'LDO1', 'LDO2', 'BUCK3', 'BOOSTI'93	
	'LDO3']	

#### 4.297 Parameter PmicVMON2RegulatorAssignment

Configures which regulator will be monitored by VMON2 (M\_VMON\_REGx[VMON2\_REG\_ASSIGN]).

The VMON2 input pin can be connected to VPRE, BOOST, LDO1-3, BUCK3, or an

external regulator (the choice depending on the configuration of this field).

The regulator connected to VMON2 MUST use an external resistor bridge

delivering a middle point of 0.8V to be compatible with over-voltage and under-voltage

monitoring thresholds.

Note: This field is modifiable only if VMON2 is enabled by OTP (i.e. PmicOtpFailSafeUnitConfiguration/PmicOtpVoltageMoni = 'true')

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
${\it symbolic} Name Value$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	EXTERNAL_REGULATOR
literals	['EXTERNAL_REGULATOR', 'VPRE', 'LDO1', 'LDO2', 'BUCK3', 'BOOST', 'LDO3']

# 4.298 Parameter PmicVMON1RegulatorAssignment

Configures which regulator will be monitored by VMON1 (M\_VMON\_REGx[VMON1\_REG\_ASSIGN]).

The VMON1 input pin can be connected to VPRE, BOOST, LDO1-3, BUCK3, or an

external regulator (the choice depending on the configuration of this field).

The regulator connected to VMON1 MUST use an external resistor bridge

delivering a middle point of 0.8V to be compatible with over-voltage and under-voltage

 $monitoring\ thresholds.$ 

Note: This field is modifiable only if VMON1 is enabled by OTP (i.e. PmicOtpFailSafeUnitConfiguration/PmicOtpVoltageMonit = 'true')

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	EXTERNAL_REGULATOR
literals	['EXTERNAL_REGULATOR', 'VPRE', 'LDO1', 'LDO2', 'BUCK3', 'BOOST', 'LDO3']

# 4.299 Container PmicReactionsSettingConf

This container contains the configuration for the reactions settings of the PMIC.

Note: Implementation Specific Parameter.

Included subcontainers:

- $\bullet \ \ PmicMainUnitReactionsConf$
- PmicFailSafeUnitReactionsConf

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE

# ${\bf 4.300 \quad Parameter \ Pmic Reactions Setting Id}$

The ID of this PmicReactionsSettingConf to be used as argument for the API calls Pmic\_SetReactions.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	true
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	0
max	255
min	0

### 4.301 Container PmicMainUnitReactionsConf

This container contains the configuration parameters for the reactions settings of the Main Unit.

Note: Implementation Specific Parameter.

Included subcontainers:

- $\bullet \ \ PmicMainInterruptMasks$
- PmicMainThermalShutdownBehaviors

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

## 4.302 Container PmicMainInterruptMasks

This container contains the configuration parameters for the interrupt masks settings of the Main Unit.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

#### 4.303 Parameter PmicHvldoOverCurrentIntDisable

This field is used to unmask/mask the interrupt for HVLDO Overcurrent event (M\_INT\_MASK1[HVLDOOC\_M]).

- 0 HVLDO Overcurrent Interrupt is Unmasked
- 1 HVLDO Overcurrent Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

### 4.304 Parameter PmicBuck1OverCurrentIntDisable

This field is used to unmask/mask the interrupt for BUCK1 Overcurrent event (M\_INT\_MASK1[BUCK1OC\_M]).

- 0 BUCK1 Overcurrent Interrupt is Unmasked
- 1 BUCK1 Overcurrent Interrupt is Masked

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

### 4.305 Parameter PmicBuck2OverCurrentIntDisable

This field is used to unmask/mask the interrupt for BUCK2 Overcurrent event (M\_INT\_MASK1[BUCK2OC\_M]).

0 - BUCK2 Overcurrent Interrupt is Unmasked

1 - BUCK2 Overcurrent Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

### 4.306 Parameter PmicBuck3OverCurrentIntDisable

This field is used to unmask/mask the interrupt for BUCK3 Overcurrent event (M\_INT\_MASK1[BUCK3OC\_M]).

0 - BUCK3 Overcurrent Interrupt is Unmasked

1 - BUCK3 Overcurrent Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

### 4.307 Parameter PmicLdo1OverCurrentIntDisable

This field is used to unmask/mask the interrupt for LDO1 Overcurrent event (M\_INT\_MASK1[LDO1OC\_M]).

0 - LDO1 Overcurrent Interrupt is Unmasked

1 - LDO1 Overcurrent Interrupt is Masked

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

### 4.308 Parameter PmicLdo2OverCurrentIntDisable

This field is used to unmask/mask the interrupt for LDO2 Overcurrent event (M\_INT\_MASK1[LDO2OC\_M]).

- 0 LDO2 Overcurrent Interrupt is Unmasked
- 1 LDO2 Overcurrent Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

### 4.309 Parameter PmicLdo3OverCurrentIntDisable

This field is used to unmask/mask the interrupt for LDO3 Overcurrent event (M\_INT\_MASK1[LDO3OC\_M]).

- 0 LDO3 Overcurrent Interrupt is Unmasked
- 1 LDO3 Overcurrent Interrupt is Masked

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# ${\bf 4.310}\quad {\bf Parameter}\ {\bf PmicHvldoTempShutdownIntDisable}$

This field is used to unmask/mask the interrupt for HVLDO Temperature Shutdown event (M\_INT\_MASK1[HVLDO\_TSDFI

- 0 HVLDO Temperature Shutdown Interrupt is Unmasked
- 1 HVLDO Temperature Shutdown Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# ${\bf 4.311} \quad {\bf Parameter\ PmicBoostTempShutdownIntDisable}$

This field is used to unmask/mask the interrupt for BOOST Temperature Shutdown event (M\_INT\_MASK1[BOOST\_TSDFL and the interrupt for BOOST Temperature Shutdown event (M\_INT\_MASK1[BOOST\_TSDFL and the interrupt for BOOST Temperature Shutdown event (M\_INT\_MASK1[BOOST\_TSDFL and the interrupt for BOOST Temperature Shutdown event (M\_INT\_MASK1[BOOST\_TSDFL and the interrupt for BOOST Temperature Shutdown event (M\_INT\_MASK1[BOOST\_TSDFL and the interrupt for BOOST Temperature Shutdown event (M\_INT\_MASK1[BOOST\_TSDFL and the interrupt for BOOST Temperature Shutdown event (M\_INT\_MASK1[BOOST\_TSDFL and the interrupt for BOOST Temperature Shutdown event (M\_INT\_MASK1[BOOST\_TSDFL and the interrupt for BOOST\_TSDFL and the interru

- 0 BOOST Temperature Shutdown Interrupt is Unmasked
- 1 BOOST Temperature Shutdown Interrupt is Masked

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigCiasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue S	$32$ $\sim$ N

## ${\bf 4.312} \quad {\bf Parameter} \ {\bf PmicBuck1TempShutdownIntDisable}$

 $This field is used to unmask/mask the interrupt for BUCK1\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK1\_TSDFLearner]) and the interrupt for BUCK1\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK1\_TSDFLearner]) and the interrupt for BUCK1\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK1\_TSDFLearner]) and the interrupt for BUCK1\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK1\_TSDFLearner]) and the interrupt for BUCK1\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK1\_TSDFLearner]) and the interrupt for BUCK1\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK1\_TSDFLearner]) and the interrupt for BUCK1\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK1\_TSDFLearner]) and the interrupt for BUCK1\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK1\_TSDFLearner]) and the interrupt for BUCK1\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK1\_TSDFLearner]) and the interrupt for BUCK1\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK1\_TSDFLearner]) and the interrupt for BUCK1\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK1\_TSDFLearner]) and the interrupt for BUCK1\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK1\_TSDFLearner]) and the interrupt for BUCK1\ Temperature\ event\ event\$ 

- 0 BUCK1 Temperature Shutdown Interrupt is Unmasked
- 1 BUCK1 Temperature Shutdown Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# ${\bf 4.313}\quad {\bf Parameter\ PmicBuck 2 Temp Shutdown Int Disable}$

 $This field is used to unmask/mask the interrupt for BUCK2\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK2\_TSDFLembers]) and the interrupt for BUCK2\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK2\_TSDFLembers]) and the interrupt for BUCK2\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK2\_TSDFLembers]) and the interrupt for BUCK2\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK2\_TSDFLembers]) and the interrupt for BUCK2\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK2\_TSDFLembers]) and the interrupt for BUCK2\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK2\_TSDFLembers]) and the interrupt for BUCK2\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK2\_TSDFLembers]) and the interrupt for BUCK2\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK2\_TSDFLembers]) and the interrupt for BUCK2\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK2\_TSDFLembers]) and the interrupt for BUCK2\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK2\_TSDFLembers]) and the interrupt for BUCK2\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK2\_TSDFLembers]) and the interrupt for BUCK2\ Temperature\ Shutdown\ event\ (M\_INT\_MASK1[BUCK2\_TSDFLembers]) and the interrupt for BUCK2\ Temperature\ event\ event\$ 

- 0 BUCK2 Temperature Shutdown Interrupt is Unmasked
- 1 BUCK2 Temperature Shutdown Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
ict@faultValue S	32aRMIC Driver

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## 4.314 Parameter PmicBuck3TempShutdownIntDisable

This field is used to unmask/mask the interrupt for BUCK3 Temperature Shutdown event (M\_INT\_MASK1[BUCK3\_TSDFL

- 0 BUCK3 Temperature Shutdown Interrupt is Unmasked
- 1 BUCK3 Temperature Shutdown Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# ${\bf 4.315}\quad {\bf Parameter}\ {\bf PmicLdo1TempShutdownIntDisable}$

This field is used to unmask/mask the interrupt for LDO1 Temperature Shutdown event (M\_INT\_MASK1[LDO1\_TSDFLG\_

- 0 LDO1 Temperature Shutdown Interrupt is Unmasked
- 1 LDO1 Temperature Shutdown Interrupt is Masked

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue S	32aRMIC Driver NX

# 4.316 Parameter PmicLdo2TempShutdownIntDisable

This field is used to unmask/mask the interrupt for LDO2 Temperature Shutdown event (M\_INT\_MASK1[LDO2\_TSDFLG\_I

- 0 LDO2 Temperature Shutdown Interrupt is Unmasked
- 1 LDO2 Temperature Shutdown Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# ${\bf 4.317} \quad {\bf Parameter} \ {\bf PmicLdo3TempShutdownIntDisable}$

This field is used to unmask/mask the interrupt for LDO3 Temperature Shutdown event (M\_INT\_MASK1[LDO3\_TSDFLG\_]

- 0 LDO3 Temperature Shutdown Interrupt is Unmasked
- 1 LDO3 Temperature Shutdown Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
ct@faultValue S	32 PMIC Driver

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## 4.318 Parameter PmicCenterDieTempIntDisable

This field is used to unmask/mask the interrupt for exceeding the Center Die Temperature Threshold (M\_INT\_MASK2[DIE\_e

- 0 Center Die Overheat Interrupt is Unmasked
- 1 Center Die Overheat Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# 4.319 Parameter PmicCommunicationErrorIntDisable

This field is used to unmask/mask the interrupt for any I2C communication error event (M\_INT\_MASK2[COM\_ERR\_M]).

- 0 Communication Error Interrupt is Unmasked
- 1 Communication Error Interrupt is Masked

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolic} Name Value$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue S	32 PMIC Driver NX

# 4.320 Parameter PmicBosUndervoltageHighIntDisable

This field is used to unmask/mask the interrupt for VBOS Undervoltage High event (M\_INT\_MASK2[VBOSUVH\_M]).

- 0 VBOS Undervoltage High Interrupt is Unmasked
- 1 VBOS Undervoltage High Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# ${\bf 4.321} \quad {\bf Parameter} \ {\bf PmicBoostUndervoltage High Int Disable}$

 $This field is used to unmask/mask the interrupt for VBOOST Undervoltage High event \\ (M\_INT\_MASK2[VBOOSTUVH\_M]) \\$ 

- 0 VBOOST Undervoltage High Interrupt is Unmasked
- 1 VBOOST Undervoltage High Interrupt is Masked

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
ict@FaultValue S	32aRMIC Driver

## 4.322 Parameter PmicBoostOvervoltageHighIntDisable

This field is used to unmask/mask the interrupt for VBOOST Overvoltage High event (M\_INT\_MASK2[VBOOSTOVH\_M]).

- 0 VBOOST Overvoltage High Interrupt is Unmasked
- 1 VBOOST Overvoltage High Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# ${\bf 4.323} \quad {\bf Parameter\ PmicBistTempShutdownIntDisable}$

- 0 Thermal Shutdown during BIST Interrupt is Unmasked
- 1 Thermal Shutdown during BIST Interrupt is Masked

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolic} Name Value$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue S	32 PMIC Driver NX

# ${\bf 4.324} \quad {\bf Parameter} \ {\bf PmicHvldoInputUndervoltageLowIntDisable}$

This field is used to unmask/mask the interrupt for both LV\_HVLDO\_IN and HV\_HVLDO\_IN Undervoltage Low event (M\_INT\_MASK2[HVLDO\_INPUT\_UVL\_M]).

- 0 LV/HV\_HVLDO\_IN Undervoltage Low Interrupt is Unmasked
- 1 LV/HV\_HVLDO\_IN Undervoltage Low Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# ${\bf 4.325} \quad {\bf Parameter\ Pmic Vpre Overvoltage Int Disable}$

This field is used to unmask/mask the interrupt for VPRE Overvoltage event (M\_INT\_MASK2[VPREOV2\_M]).

- 0 VPRE Overvoltage Interrupt is Unmasked
- 1 VPRE Overvoltage Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue ctors S	false 32 PMIC Driver

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## 4.326 Parameter PmicVpreOvercurrentIntDisable

This field is used to unmask/mask the interrupt for VPRE Overcurrent event (M\_INT\_MASK2[VPREOC\_M]).

- 0 VPRE Overcurrent Interrupt is Unmasked
- 1 VPRE Overcurrent Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# ${\bf 4.327} \quad {\bf Parameter} \ {\bf PmicVpreUndervoltageLowIntDisable}$

This field is used to unmask/mask the interrupt for VPRE Undervoltage Low event (M\_INT\_MASK2[VPREUVL\_M]).

- 0 VPRE Undervoltage Low Interrupt is Unmasked
- 1 VPRE Undervoltage Low Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

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## 4.328 Parameter PmicVpreUndervoltageHighIntDisable

This field is used to unmask/mask the interrupt for VPRE Undervoltage High event (M\_INT\_MASK2[VPREUVH\_M]).

- 0 VPRE Undervoltage High Interrupt is Unmasked
- 1 VPRE Undervoltage High Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# ${\bf 4.329 \quad Parameter \ Pmic V sup Under voltage 7 V Int Disable}$

This field is used to unmask/mask the interrupt for VSUP Undervoltage 7V event (M\_INT\_MASK2[VSUPUV7\_M]).

- 0 VSUP Undervoltage 7V Interrupt is Unmasked
- 1 VSUP Undervoltage 7V Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
ict@FaultValue S	32aRMIC Driver

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## 4.330 Parameter PmicVsupUndervoltageLowIntDisable

This field is used to unmask/mask the interrupt for VSUP Undervoltage Low event (M\_INT\_MASK2[VSUPUVL\_M]).

- 0 VSUP Undervoltage Low Interrupt is Unmasked
- 1 VSUP Undervoltage Low Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# ${\bf 4.331} \quad {\bf Parameter} \ {\bf PmicVsupUndervoltage High Int Disable}$

This field is used to unmask/mask the interrupt for VSUP Undervoltage High event (M\_INT\_MASK2[VSUPUVH\_M]).

- 0 VSUP Undervoltage High Interrupt is Unmasked
- 1 VSUP Undervoltage High Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue S	32 MIC Driver NX

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## 4.332 Parameter PmicPwron2TransitionIntDisable

This field is used to unmask/mask the interrupt for PWRON2 Transition (Toggling) event (M\_INT\_MASK2[PWRON2FLG\_N

- 0 PWRON2 Transition Interrupt is Unmasked
- 1 PWRON2 Transition Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# 4.333 Parameter PmicPwron1TransitionIntDisable

 $This field is used to unmask/mask the interrupt for PWRON1\ Transition\ (Toggling)\ event\ (M\_INT\_MASK2[PWRON1FLG\_MASK2]) and the interrupt for PWRON1\ Transition\ (Toggling)\ event\ (M\_INT\_MASK2[PWRON1FLG\_MASK2]) and the interrupt for PWRON1\ Transition\ (Toggling)\ event\ (M\_INT\_MASK2[PWRON1FLG\_MASK2]) and the interrupt for PWRON1\ Transition\ (Toggling)\ event\ (M\_INT\_MASK2[PWRON1FLG\_MASK2]) and the interrupt for PWRON1\ Transition\ (Toggling)\ event\ (M\_INT\_MASK2[PWRON1FLG\_MASK2]) and the interrupt for PWRON1\ Transition\ (Toggling)\ event\ (M\_INT\_MASK2[PWRON1FLG\_MASK2]) and the interrupt for PWRON1\ Transition\ (Toggling)\ event\ (M\_INT\_MASK2[PWRON1FLG\_MASK2]) and the interrupt for PWRON1\ Transition\ (Toggling)\ event\ (M\_INT\_MASK2[PWRON1FLG\_MASK2]) and the interrupt for PWRON1\ Transition\ (Toggling)\ event\ (M\_INT\_MASK2[PWRON1FLG\_MASK2]) and the interrupt for PWRON1\ Transition\ (Toggling)\ event\ (M\_INT\_MASK2[PWRON1FLG\_MASK2]) and the interrupt for PWRON1\ Transition\ (Toggling)\ event\ (M\_INT\_MASK2[PWRON1FLG\_MASK2]) and the interrupt for PWRON1\ Transition\ (Toggling)\ event\ (M\_INT\_MASK2[PWRON1FLG\_MASK2]) and the interrupt for PWRON1\ Transition\ (Toggling)\ event\ (M\_INT\_MASK2[PWRON1FLG\_MASK2]) and the interrupt for PWRON1\ Transition\ (Toggling)\ event\ (M\_INT\_MASK2[PWRON1FLG\_MASK2]) and the interrupt for PWRON1\ Transition\ (Toggling)\ event\ (M\_INT\_MASK2[PWRON1FLG\_MASK2]) and the interrupt for PWRON1\ Event\ (M\_INT\_MASK2[PWRON1FLG\_MASK2]) and the interrupt for$ 

- 0 PWRON1 Transition Interrupt is Unmasked
- 1 PWRON1 Transition Interrupt is Masked

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
ict@FaultValue S	32aRMIC Driver

### 4.334 Container PmicMainThermalShutdownBehaviors

This container contains the configuration parameters for the thermal shutdown behaviors of the Main Unit.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# 4.335 Parameter PmicCenterDieTempThreshold

Configures the center die temperature threshold (M\_TSD\_CFG[DIE\_CENTER\_TEMP]).

A thermal sensor is placed on the center of the die (device) which is used to generate interrupts for the MCU whenever the temperature exceeds the configured threshold.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	TEMP_105_oC
literals	['TEMP_75_oC', 'TEMP_90_oC', 'TEMP_105_oC', 'TEMP_120_oC', 'TEMP_135_oC', 'TEMP_150_oC']

#### 4.336 Parameter PmicBoostTsdBehavior

Controls the reaction/behavior of the BOOST regulator in case of a thermal shutdown event (M\_TSD\_CFG[BOOST\_TSDCF

Can be configured to either shutdown only the regulator OR shutdown the regulator and transition the device into Deep Fail-State (DFS) mode when the thermal shutdown threshold is exceeded.

In case SHUTDOWN\_ONLY is selected, the regulator will startup automatically when the temperature goes down.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	SHUTDOWN_AND_DFS
literals	['SHUTDOWN_ONLY', 'SHUTDOWN_AND_DFS']

#### 4.337 Parameter PmicBuck1TsdBehavior

Controls the reaction/behavior of the BUCK1 regulator in case of a thermal shutdown event (M\_TSD\_CFG[BUCK1\_TSDCFG

Can be configured to either shutdown only the regulator OR shutdown the regulator and transition the device into Deep Fail-State (DFS) mode when the thermal shutdown threshold is exceeded.

In case SHUTDOWN\_ONLY is selected, the regulator will startup automatically when the temperature goes down.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	SHUTDOWN_AND_DFS
literals	['SHUTDOWN_ONLY', 'SHUTDOWN_AND_DFS']

### 4.338 Parameter PmicBuck2TsdBehavior

Controls the reaction/behavior of the BUCK2 regulator in case of a thermal shutdown event (M\_TSD\_CFG[BUCK2\_TSDCFG

Can be configured to either shutdown only the regulator OR shutdown the regulator and transition the device into Deep Fail-State (DFS) mode when the thermal shutdown threshold is exceeded.

In case SHUTDOWN\_ONLY is selected, the regulator will startup automatically when the temperature goes down.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
${\it symbolic} Name Value$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	SHUTDOWN_AND_DFS
literals	['SHUTDOWN_ONLY', 'SHUTDOWN_AND_DFS']

### 4.339 Parameter PmicBuck3TsdBehavior

Controls the reaction/behavior of the BUCK3 regulator in case of a thermal shutdown event (M\_TSD\_CFG[BUCK3\_TSDCFG

Can be configured to either shutdown only the regulator OR shutdown the regulator and transition the device into Deep Fail-State (DFS) mode when the thermal shutdown threshold is exceeded.

In case SHUTDOWN\_ONLY is selected, the regulator will startup automatically when the temperature goes down.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	SHUTDOWN_AND_DFS
literals	['SHUTDOWN_ONLY', 'SHUTDOWN_AND_DFS']

#### 4.340 Parameter PmicLdo1TsdBehavior

Controls the reaction/behavior of the LDO1 regulator in case of a thermal shutdown event (M\_TSD\_CFG[LDO1\_TSDCFG]).

Can be configured to either shutdown only the regulator OR shutdown the regulator and transition the device into Deep Fail-State (DFS) mode when the thermal shutdown threshold is exceeded.

In case SHUTDOWN\_ONLY is selected, the regulator will startup automatically when the temperature goes down.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	SHUTDOWN_AND_DFS
literals	['SHUTDOWN_ONLY', 'SHUTDOWN_AND_DFS']

## 4.341 Parameter PmicLdo2TsdBehavior

Controls the reaction/behavior of the LDO2 regulator in case of a thermal shutdown event (M\_TSD\_CFG[LDO2\_TSDCFG]).

Can be configured to either shutdown only the regulator OR shutdown the regulator and transition the device into Deep Fail-State (DFS) mode when the thermal shutdown threshold is exceeded.

In case SHUTDOWN\_ONLY is selected, the regulator will startup automatically when the temperature goes down.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
${\it symbolic} Name Value$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	SHUTDOWN_AND_DFS
literals	['SHUTDOWN_ONLY', 'SHUTDOWN_AND_DFS']

#### 4.342 Parameter PmicLdo3TsdBehavior

Controls the reaction/behavior of the LDO3 regulator in case of a thermal shutdown event (M\_TSD\_CFG[LDO3\_TSDCFG]).

Can be configured to either shutdown only the regulator OR shutdown the regulator and transition the device into Deep Fail-State (DFS) mode when the thermal shutdown threshold is exceeded.

In case SHUTDOWN\_ONLY is selected, the regulator will startup automatically when the temperature goes down.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	SHUTDOWN_AND_DFS
literals	['SHUTDOWN_ONLY', 'SHUTDOWN_AND_DFS']

#### 4.343 Parameter PmicLHVLdoTsdBehavior

Controls the reaction/behavior of the HVLDO regulator in case of a thermal shutdown event (M\_TSD\_CFG[HVLDO\_TSDCFG]).

Can be configured to either shutdown only the regulator OR shutdown the regulator and transition the device into Deep Fail-State (DFS) mode when the thermal shutdown threshold is exceeded.

In case SHUTDOWN\_ONLY is selected, the regulator will startup automatically when the temperature goes down.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	SHUTDOWN_AND_DFS
literals	['SHUTDOWN_ONLY', 'SHUTDOWN_AND_DFS']

## 4.344 Container PmicFailSafeUnitReactionsConf

This container contains the configuration parameters for the reactions settings of the Fail-Safe Unit.

Note: Implementation Specific Parameter.

Included subcontainers:

#### $\bullet \ \ PmicFailSafeInterruptMasks$

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# ${\bf 4.345}\quad {\bf Container\ PmicFailSafeInterruptMasks}$

This container contains the configuration parameters for the interrupt masks settings of the Fail-Safe Unit.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

## 4.346 Parameter PmicVmon4OverUnderVoltageIntDisable

This field is used to unmask/mask the interrupt for VMON4 Overvoltage and Undervoltage events (FS\_INTB\_MASK[INT\_INT]).

- 0 VMON4 Overvoltage and Undervoltage Interrupt is Unmasked
- 1 VMON4 Overvoltage and Undervoltage Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# ${\bf 4.347} \quad {\bf Parameter} \ {\bf PmicVmon3OverUnderVoltageIntDisable}$

This field is used to unmask/mask the interrupt for VMON3 Overvoltage and Undervoltage events (FS\_INTB\_MASK[INT\_IN

- 0 VMON3 Overvoltage and Undervoltage Interrupt is Unmasked
- 1 VMON3 Overvoltage and Undervoltage Interrupt is Masked

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# ${\bf 4.348} \quad {\bf Parameter} \ {\bf PmicVmon2OverUnderVoltageIntDisable}$

This field is used to unmask/mask the interrupt for VMON2 Overvoltage and Undervoltage events (FS\_INTB\_MASK[INT\_INT]).

- 0 VMON2 Overvoltage and Undervoltage Interrupt is Unmasked
- 1 VMON2 Overvoltage and Undervoltage Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# ${\bf 4.349} \quad {\bf Parameter} \ {\bf PmicVmon1OverUnderVoltageIntDisable}$

This field is used to unmask/mask the interrupt for VMON1 Overvoltage and Undervoltage events (FS\_INTB\_MASK[INT\_IN

- 0 VMON1 Overvoltage and Undervoltage Interrupt is Unmasked
- 1 VMON1 Overvoltage and Undervoltage Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# ${\bf 4.350 \quad Parameter \ PmicVddio Over Under Voltage Int Disable}$

This field is used to unmask/mask the interrupt for VDDIO Overvoltage and Undervoltage events (FS\_INTB\_MASK[INT\_IN

- 0 VDDIO Overvoltage and Undervoltage Interrupt is Unmasked
- 1 VDDIO Overvoltage and Undervoltage Interrupt is Masked

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# ${\bf 4.351} \quad {\bf Parameter} \ {\bf PmicVcoremonOverUnderVoltageIntDisable}$

This field is used to unmask/mask the interrupt for VCOREMON Overvoltage and Undervoltage events (FS\_INTB\_MASK[IN

- 0 VCOREMON Overvoltage and Undervoltage Interrupt is Unmasked
- 1 VCOREMON Overvoltage and Undervoltage Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# ${\bf 4.352} \quad {\bf Parameter} \ {\bf PmicWatchdogBadRefreshIntDisable}$

 $This field is used to unmask/mask the interrupt for Bad Watchdog Refresh event (FS\_INTB\_MASK[INT\_INH\_BAD\_WD\_FRESH and FRESH and FRESH$ 

- 0 Bad Watchdog Refresh Interrupt is Unmasked
- 1 Bad Watchdog Refresh Interrupt is Masked

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue S	32aRMIC Driver N

## ${\bf 4.353} \quad {\bf Parameter} \ {\bf PmicHvldoOverUnderVoltageIntDisable}$

This field is used to unmask/mask the interrupt for HVLDO Overvoltage and Undervoltage events (FS\_INTB\_MASK[INT\_IN

- 0 HVLDO Overvoltage and Undervoltage Interrupt is Unmasked
- 1 HVLDO Overvoltage and Undervoltage Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

## 4.354 Parameter PmicFccu2EventIntDisable

This field is used to unmask/mask the interrupt for FCCU2 event (FS\_INTB\_MASK[INT\_INH\_FCCU2]).

- 0 FCCU2 Event Interrupt is Unmasked
- 1 FCCU2 Event Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

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## 4.355 Parameter PmicFccu1EventIntDisable

This field is used to unmask/mask the interrupt for FCCU1 event (FS\_INTB\_MASK[INT\_INH\_FCCU1]).

- 0 FCCU1 Event Interrupt is Unmasked
- 1 FCCU1 Event Interrupt is Masked

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

# 4.356 Container PmicAMUXConfiguration

This container contains the configuration for the AMUX pin.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • PmicAmuxChannel

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

### 4.357 Parameter PmicSetAnalogMuxApi

Pre-processor switch to enable/disable the API to set the analog multiplexer (AMUX) pin.

#define PMIC\_SET\_ANALOG\_MUX\_API (STD\_ON)/(STD\_OFF) will be generated in Pmic\_Cfg.h file.

This API cannot be enabled unless the AMUX/FOUT pin is configured as AMUX by OTP

 $(PmicOtpMainUnitConfiguration/PmicOtpMainIOConfiguration/PmicAmuxFoutPinMode = 'AMUX\_MODE'). \\$ 

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

## 4.358 Container PmicAmuxChannel

This container defines a symbolic name for every possible AMUX channel.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE

## 4.359 Parameter PmicAmuxChannelId

This parameter shall represent the ID of the AMUX channel.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	true
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	0
max	255
min	0

## 4.360 Parameter PmicAmuxChannelSelect

Select the AMUX channel for the specific instance of the PmicAmuxChannel container (M\_AMUX[AMUX]).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	GND
literals	['GND', 'VDDIO', 'TEMPERATURE', 'BANDGAP_MAIN', 'BANDGAP_F← AIL_SAFE', 'BUCK1', 'BUCK2', 'BUCK3', 'VPRE', 'VBOOST', 'LDO1', 'L← DO2', 'VBOS', 'VSUP1', 'PWRON1', 'PWRON2', 'HVLDO', 'LDO3']

#### 4.361 Parameter PmicAmuxRatio

Controls the divider ratio for VSUP, PWRON1, and PWRON2 (M\_AMUX[RATIO]).

This field is editable only when PmicAmuxChannelSelect is either VSUP, PWRON1 or PWRON2.

Warning: The input voltage range for VSUP, PWRON1, and PWRON2 must be

between 2.25V and 22.5V when RATIO = 20, and between 4.2V and 42V when RATIO = 34.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	RATIO_20
literals	['RATIO_20', 'RATIO_34']

# 4.362 Container PmicFailSafeConfiguration

This container contains the initial configuration parameters (set in the INIT\_FS state) for the overvoltage and undervoltage reactions.

Note: Implementation Specific Parameter.

Included subcontainers:

- PmicSVSConfiguration
- PmicFailSafePinReactions
- PmicWatchdogConfiguration
- PmicABIST2Configuration
- $\bullet \ \ Pmic Safe Inputs Configuration$
- PmicStateMachineConfiguration

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

## 4.363 Container PmicSVSConfiguration

This container contains the initial configuration parameters (set in the INIT\_FS state) for the SVS mechanism.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • PmicSVSSettingConf

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# 4.364 Parameter PmicSwitchSVSApi

Pre-processor allows to switch static voltage scaler value.

User need to configure SVS setting in tab PmicSVSSettingConf.

In case DIE\_PROCESS feature is enable, this function will configure SVS if the DIE\_PROCESS otp of mcu enables.

It will not configure SVS if the DIE\_PROCESS otp of mcu disable. Refer Mcu reference manual to check DIE\_PROCESS bit.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

#### 4.365 Parameter PmicSVSOffset

Statically scales the output voltage of BUCK1 (and BUCK2 if used in dual-phase mode)

by the configured amount in the direction specified by SVS\_OFFSET\_SIGN

in the INIT\_FS state (FS\_I\_SVS[SVS\_OFFSET]).

A SVS (Static Voltage Scaling) mechanism is implemented to allow the MCU to reduce

the output voltage initially configured at start-up of BUCK1 (and BUCK2 if

used in multiphase) by OTP, to optimize MCU voltage working points, and

compensate part to part process variation.

The offset amount is effectively limited by the allowed SVS steps configured

in VCORE\_SVS\_CLAMP\_OTP[5:0] by OTP (i.e. PmicFailSafeConfiguration/PmicOtpSafetyConfiguration/

PmicSVSLimit)

Depending on the offset, it may be needed to change the voltage in multiple steps

to not trigger an OV/UV event.

Value
ECUC-ENUMERATION-PARAM-DEF
NXP
false
1
1
N/A
N/A

Property	Value
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	OFFSET_0_0
literals	['OFFSET_0_0', 'OFFSET_6_25', 'OFFSET_12_5', 'OFFSET_18_75', 'OFFSET_25_0', 'OFFSET_31_25', 'OFFSET_37_5', 'OFFSET_43_75', 'OFFSET_50_0', 'OFFSET_56_25', 'OFFSET_62_5', 'OFFSET_68_75', 'OFFSET_50_0', 'OFFSET_81_25', 'OFFSET_87_5', 'OFFSET_93_75', 'OFFSET_100_0', 'OFFSET_106_25', 'OFFSET_112_5', 'OFFSET_118_75', 'OFFSET_125_0', 'OFFSET_131_25', 'OFFSET_137_5', 'OFFSET_143_75', 'OFFSET_150_0', 'OFFSET_156_25', 'OFFSET_162_5', 'OFFSET_168_75', 'OFFSET_175_0', 'OFFSET_181_25', 'OFFSET_187_5', 'OFFSET_193_75', 'OFFSET_200_0', 'OFFSET_206_25', 'OFFSET_212_5', 'OFFSET_218_75', 'OFFSET_225_0', 'OFFSET_231_25', 'OFFSET_237_5', 'OFFSET_243_75', 'OFFSET_250_0', 'OFFSET_256_25', 'OFFSET_262_5', 'OFFSET_268_75', 'OFFSET_275_0', 'OFFSET_281_25', 'OFFSET_287_5', 'OFFSET_293_75', 'OFFSET_300_0', 'OFFSET_306_25', 'OFFSET_312_5', 'OFFSET_318_75', 'OFFSET_325_0', 'OFFSET_331_25', 'OFFSET_337_5', 'OFFSET_343_75', 'OFFSET_350_0', 'OFFSET_356_25', 'OFFSET_362_5', 'OFFSET_368_75', 'OFFSET_375_0', 'OFFSET_381_25', 'OFFSET_387_5', 'OFFSET_393_75', 'OFFSET_375_0', 'OFFSET_381_25', 'OFFSET_387_5', 'OFFSET_393_75', 'OFFSET_375_0', 'OFFSET_381_25', 'OFFSET_387_5', 'OFFSET_393_75']

# 4.366 Parameter PmicSVSOffsetSign

Configures the offset type applicable by the SVS mechanism (FS\_I\_SVS[SVS\_OFFSET\_SIGN]).

The offset type is limited by the SVS offset type configured by OTP in VCORE\_SVS\_FULL\_OFFSET\_OTP

 $(i.e.\ PmicFailSafeConfiguration/PmicOtpSafetyConfiguration/PmicSVSOffsetType)$ 

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	NEGATIVE_OFFSET
literals	['NEGATIVE_OFFSET', 'POSITIVE_OFFSET']

### 4.367 Parameter PmicBuck1SVSOutputVoltage

Represents the output voltage of the BUCK1 (BUCK1/2 in dual-phase mode) regulator

after the SVS offset is applied. This output voltage will take effect at the

end of the INIT\_FS state.

The formula for calculating this field is:

1. If PmicSVSOffsetSign = NEGATIVE\_OFFSET:

 $\label{eq:pmicBuck1SVSOutputVoltage} PmicOtpMainUnitConfiguration/PmicOtpRegulatorsConfiguration/PmicBuck1Regulator/PmicOtpRegulatorsConfiguration/PmicBuck1Regulator/PmicOtpRegulatorsConfiguration/PmicBuck1Regulator/PmicOtpRegulatorsConfiguration/PmicBuck1Regulator/PmicOtpRegulatorsConfiguration/PmicOtpRegu$ 

2. If PmicSVSOffsetSign = POSITIVE\_OFFSET:

 $\label{eq:pmicBuck1SVSOutputVoltage} PmicOtpMainUnitConfiguration/PmicOtpRegulatorsConfiguration/PmicBuck1Regulator/PmicOtpRegulatorsConfiguration/PmicBuck1Regulator/PmicOtpRegulatorsConfiguration/PmicBuck1Regulator/PmicOtpRegulatorsConfiguration/PmicBuck1Regulator/PmicOtpRegulatorsConfiguration/PmicOtpRegu$ 

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.4
max	1.8
min	0.4

# 4.368 Container PmicSVSSettingConf

This container contains the configuration for the static voltage scaler settings of the PMIC.

If the PmicSwitchSVSApi is enabled, the list must have at least one element.

Otherwise, the list must be empty.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE

# 4.369 Parameter PmicSVSSettingId

This parameter shall represent the ID of the SVS configuration.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	true
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	0
max	255
min	0

## 4.370 Parameter PmicSVSOffsetSetting

Statically scales the output voltage of BUCK1 (and BUCK2 if used in dual-phase mode) by the configured amount in the direction specified by SVS\_OFFSET\_SIGN in the INIT\_FS state (FS\_I\_SVS[SVS\_OFFSET]).

A SVS (Static Voltage Scaling) mechanism is implemented to allow the MCU to reduce the output voltage initially configured at start-up of BUCK1 (and BUCK2 if used in multiphase) by OTP, to optimize MCU voltage working points, and compensate part to part process variation.

The offset amount is effectively limited by the allowed SVS steps configured

in VCORE\_SVS\_CLAMP\_OTP[5:0] by OTP (i.e. PmicFailSafeConfiguration/PmicOtpSafetyConfiguration/PmicSVSLimit)

Depending on the offset, it may be needed to change the voltage in multiple steps to not trigger an OV/UV event.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	OFFSET_0_0
literals	

### 4.371 Parameter PmicSVSOffsetSignSetting

Configures the offset type applicable by the SVS mechanism (FS\_I\_SVS[SVS\_OFFSET\_SIGN]).

The offset type is limited by the SVS offset type configured by OTP in VCORE\_SVS\_FULL\_OFFSET\_OTP

(i.e. PmicFailSafeConfiguration/PmicOtpSafetyConfiguration/PmicSVSOffsetType)

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	NEGATIVE_OFFSET
literals	['NEGATIVE_OFFSET', 'POSITIVE_OFFSET']

# 4.372 Parameter PmicBuck1SVSOutputVoltageSetting

Represents the output voltage of the BUCK1 (BUCK1/2 in dual-phase mode) regulator after the SVS offset is applied. This output voltage will take effect at the end of the INIT\_FS state.

The formula for calculating this field is:

1. If PmicSVSOffsetSign = NEGATIVE\_OFFSET:

 $\label{eq:pmicBuck1SVSOutputVoltage} PmicOtpMainUnitConfiguration/PmicOtpRegulatorsConfiguration/PmicBuck1Regulator/PmicOtpRegulatorsConfiguration/PmicBuck1Regulator/PmicOtpRegulatorsConfiguration/PmicBuck1Regulator/PmicOtpRegulatorsConfiguration/PmicBuck1Regulator/PmicOtpRegulatorsConfiguration/PmicOtpRegu$ 

2. If PmicSVSOffsetSign = POSITIVE OFFSET:

 $\label{eq:pmicBuck1SVSOutputVoltage} PmicOtpMainUnitConfiguration/PmicOtpRegulatorsConfiguration/PmicBuck1Regulator/PmicOtpRegulatorsConfiguration/PmicBuck1Regulator/PmicOtpRegulatorsConfiguration/PmicBuck1Regulator/PmicOtpRegulatorsConfiguration/PmicBuck1Regulator/PmicOtpRegulatorsConfiguration/PmicOtpRegu$ 

Note: This field must not be manually modified.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.4
max	1.8
min	0.4

### 4.373 Container PmicFailSafePinReactions

This container contains the configuration parameters for the pin reactions settings of the Fail-Safe Unit.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# 4.374 Parameter PmicVcoremonOvervoltageImpact

Configures the Fail-Safe reaction on RSTB and/or FS0B when an over-voltage fault is detected on VCOREMON (VCOREMON\_OV\_FS\_IMPACT[1:0]).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueConngClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FS0B_AND_RSTB_ASSERT
literals	['DISABLED', 'FS0B_ASSERT', 'FS0B_AND_RSTB_ASSERT']

# 4.375 Parameter PmicVcoremonUndervoltageImpact

Configures the Fail-Safe reaction on RSTB and/or FS0B when an under-voltage fault is detected on VCOREMON (VCOREMON\_UV\_FS\_IMPACT[1:0]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FS0B_ASSERT
literals	['DISABLED', 'FS0B_ASSERT', 'FS0B_AND_RSTB_ASSERT']

# ${\bf 4.376}\quad {\bf Parameter\ PmicHvldoOvervoltageImpact}$

Configures the Fail-Safe reaction on RSTB and/or FS0B when an over-voltage fault is detected on HVLDO (HVLDO\_OV\_FS\_

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FS0B_AND_RSTB_ASSERT
literals	['DISABLED', 'FS0B_ASSERT', 'FS0B_AND_RSTB_ASSERT']

# 4.377 Parameter PmicHvldoUndervoltageImpact

Configures the Fail-Safe reaction on RSTB and/or FS0B when an under-voltage fault is detected on HVLDO (HVLDO\_UV\_FS\_IMPACT[1:0]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FS0B_ASSERT
literals	['DISABLED', 'FS0B_ASSERT', 'FS0B_AND_RSTB_ASSERT']

# 4.378 Parameter PmicVddioOvervoltageImpact

Configures the Fail-Safe reaction on RSTB and/or FS0B when an over-voltage fault is detected on VDDIO (VDDIO\_OV\_FS\_

Property	Value	
type	ECUC-ENUMERATION-PARAM-DEF	
origin	NXP	
symbolicNameValue	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	true	
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE	
	VARIANT-POST-BUILD: POST-BUILD	
defaultValue	FS0B_AND_RSTB_ASSERT	
literals	['DISABLED', 'FS0B_ASSERT', 'FS0B_AND_RSTB_ASSERT']	

### 4.379 Parameter PmicVddioUndervoltageImpact

 $Configures \ the \ Fail-Safe \ reaction \ on \ RSTB \ and/or \ FS0B \ when \ an \ under-voltage \ fault \ is \ detected \ on \ VDDIO\_UV\_FSDE \ and/or \ FS0B \ when \ an \ under-voltage \ fault \ is \ detected \ on \ VDDIO\_UV\_FSDE \ and/or \ FS0B \ when \ an \ under-voltage \ fault \ is \ detected \ on \ VDDIO\_UV\_FSDE \ and/or \ FS0B \ when \ an \ under-voltage \ fault \ is \ detected \ on \ VDDIO\_UV\_FSDE \ and/or \ FS0B \ when \ an \ under-voltage \ fault \ is \ detected \ on \ VDDIO\_UV\_FSDE \ and/or \ FS0B \ when \ an \ under-voltage \ fault \ is \ detected \ on \ VDDIO\_UV\_FSDE \ and/or \ fault \ and/or \ and/or$ 

Note: Implementation Specific Parameter.

Property	Value	
type	ECUC-ENUMERATION-PARAM-DEF	
origin	NXP	
symbolicNameValue	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	true	
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE	
	VARIANT-POST-BUILD: POST-BUILD	
defaultValue	FS0B_ASSERT	
literals	['DISABLED', 'FS0B_ASSERT', 'FS0B_AND_RSTB_ASSERT']	

# 4.380 Parameter PmicVmon4OvervoltageImpact

Configures the Fail-Safe reaction on RSTB and/or FS0B when an over-voltage fault is detected on VMON4 (VMON4\_OV\_FS

Property	Value	
type	ECUC-ENUMERATION-PARAM-DEF	
origin	NXP	
symbolicNameValue	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	true	
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE	
	VARIANT-POST-BUILD: POST-BUILD	
defaultValue	FS0B_AND_RSTB_ASSERT	
literals	['DISABLED', 'FS0B_ASSERT', 'FS0B_AND_RSTB_ASSERT']	

### 4.381 Parameter PmicVmon4UndervoltageImpact

Configures the Fail-Safe reaction on RSTB and/or FS0B when an under-voltage fault is detected on VMON4 (VMON4\_UV\_FS\_IMPACT[1:0]).

Note: Implementation Specific Parameter.

Property	Value	
type	ECUC-ENUMERATION-PARAM-DEF	
origin	NXP	
symbolicNameValue	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	true	
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE	
	VARIANT-POST-BUILD: POST-BUILD	
defaultValue	FS0B_ASSERT	
literals	['DISABLED', 'FS0B_ASSERT', 'FS0B_AND_RSTB_ASSERT']	

## 4.382 Parameter PmicVmon3OvervoltageImpact

Configures the Fail-Safe reaction on RSTB and/or FS0B when an over-voltage fault is detected on VMON3\_OV\_FS\_

Property	Value	
type	ECUC-ENUMERATION-PARAM-DEF	
origin	NXP	
symbolicNameValue	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	true	
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE	
	VARIANT-POST-BUILD: POST-BUILD	
defaultValue	FS0B_AND_RSTB_ASSERT	
literals	['DISABLED', 'FS0B_ASSERT', 'FS0B_AND_RSTB_ASSERT']	

### 4.383 Parameter PmicVmon3UndervoltageImpact

Configures the Fail-Safe reaction on RSTB and/or FS0B when an under-voltage fault is detected on VMON3 (VMON3\_UV\_FS\_IMPACT[1:0]).

Note: Implementation Specific Parameter.

Property	Value	
type	ECUC-ENUMERATION-PARAM-DEF	
origin	NXP	
symbolicNameValue	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	true	
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE	
	VARIANT-POST-BUILD: POST-BUILD	
defaultValue	FS0B_ASSERT	
literals	['DISABLED', 'FS0B_ASSERT', 'FS0B_AND_RSTB_ASSERT']	

### 4.384 Parameter PmicVmon2OvervoltageImpact

Configures the Fail-Safe reaction on RSTB and/or FS0B when an over-voltage fault is detected on VMON2 (VMON2\_OV\_FS

Property	Value	
type	ECUC-ENUMERATION-PARAM-DEF	
origin	NXP	
symbolicNameValue	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	true	
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE	
	VARIANT-POST-BUILD: POST-BUILD	
defaultValue	FS0B_AND_RSTB_ASSERT	
literals	['DISABLED', 'FS0B_ASSERT', 'FS0B_AND_RSTB_ASSERT']	

# ${\bf 4.385 \quad Parameter \ Pmic Vmon 2 Undervoltage Impact}$

Configures the Fail-Safe reaction on RSTB and/or FS0B when an under-voltage fault is detected on VMON2 (VMON2\_UV\_FS\_IMPACT[1:0]).

Note: Implementation Specific Parameter.

Property	Value	
type	ECUC-ENUMERATION-PARAM-DEF	
origin	NXP	
symbolicNameValue	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	true	
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE	
	VARIANT-POST-BUILD: POST-BUILD	
defaultValue	FS0B_ASSERT	
literals	['DISABLED', 'FS0B_ASSERT', 'FS0B_AND_RSTB_ASSERT']	

## 4.386 Parameter PmicVmon1OvervoltageImpact

Configures the Fail-Safe reaction on RSTB and/or FS0B when an over-voltage fault is detected on VMON1 (VMON1\_OV\_FS

Property	Value	
type	ECUC-ENUMERATION-PARAM-DEF	
origin	NXP	
symbolicNameValue	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	true	
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE	
	VARIANT-POST-BUILD: POST-BUILD	
defaultValue	FS0B_AND_RSTB_ASSERT	
literals	['DISABLED', 'FS0B_ASSERT', 'FS0B_AND_RSTB_ASSERT']	

### 4.387 Parameter PmicVmon1UndervoltageImpact

Configures the Fail-Safe reaction on RSTB and/or FS0B when an under-voltage fault is detected on VMON1 (VMON1\_UV\_FS\_IMPACT[1:0]).

Note: Implementation Specific Parameter.

Property	Value	
type	ECUC-ENUMERATION-PARAM-DEF	
origin	NXP	
symbolicNameValue	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	true	
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE	
	VARIANT-POST-BUILD: POST-BUILD	
defaultValue	FS0B_ASSERT	
literals	['DISABLED', 'FS0B_ASSERT', 'FS0B_AND_RSTB_ASSERT']	

# 4.388 Container PmicWatchdogConfiguration

This container contains the initial configuration parameters (set in the INIT\_FS state) for the Watchdog. Included subcontainers:

• PmicWatchdogSettingConf

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

### 4.389 Parameter PmicWatchdogApi

Pre-processor switch to enable/disable the Watchdog API.

#define PMIC\_WATCHDOG\_API (STD\_ON)/(STD\_OFF) will be generated in Pmic\_Cfg.h file.

This API cannot be enabled unless the Watchdog Monitoring is enabled by OTP

(PmicOtpFailSafeUnitConfiguration/PmicOtpSafetyIOConfiguration/PmicWatchdogEnable = 'true').

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

### 4.390 Parameter PmicWatchdogErrorCounterLimit

Controls the Watchdog Error Counter Limit (FS\_I\_WD\_CFG[WD\_ERR\_LIMIT]).

The Watchdog Error Counter is incremented by 2 after each bad Watchdog

refresh and decremented by 1 after each good Watchdog refresh.

When the Watchdog Error Counter reaches this limit, the Fault Error

Counter will be incremented by 1 and will trigger a Fail-Safe reaction

configured by FS\_I\_WD\_CFG[WD\_FS\_IMPACT] (PmicWatchdogErrorImpact).

Note: This field is editable only when the Watchdog Monitoring is enabled

by OTP (i.e. PmicOtpFailSafeUnitConfiguration/PmicOtpSafetyIOConfiguration/

PmicWatchdogEnable = 'true')

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	MAX_6
literals	['MAX_8', 'MAX_6', 'MAX_4', 'MAX_2']

## ${\bf 4.391} \quad {\bf Parameter} \ {\bf PmicWatchdogRefreshCounterLimit}$

Controls the Watchdog Refresh Counter Limit (FS\_I\_WD\_CFG[WD\_RFR\_LIMIT]).

The Watchdog Refresh Counter is incremented by 1 after each good Watchdog

refresh, but is reset to 0 every time there is a bad Watchdog refresh.

When the Watchdog Refresh Counter reaches this limit, and if the next

Watchdog refresh is also good, the Fault Error Counter is decremented

by 1.

Note: This field is editable only when the Watchdog Monitoring is enabled

by OTP (i.e. PmicOtpFailSafeUnitConfiguration/PmicOtpSafetyIOConfigurati

PmicWatchdogEnable = 'true')

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	MAX_6
literals	['MAX_6', 'MAX_4', 'MAX_2', 'MAX_1']

### 4.392 Parameter PmicWatchdogErrorImpact

Configures the Fail-Safe reaction on RSTB and/or FS0B when the Watchdog

Error Counter reaches its maximum value (FS\_I\_WD\_CFG[WD\_FS\_IMPACT]).

Note: This field is editable only when the Watchdog Monitoring is enabled

by OTP (i.e. PmicOtpFailSafeUnitConfiguration/PmicOtpSafetyIOConfigurati

 ${\bf PmicWatchdogEnable = 'true')}$ 

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FS0B_AND_RSTB_ASSERT
literals	['DISABLED', 'FS0B_ASSERT', 'FS0B_AND_RSTB_ASSERT']

### 4.393 Parameter PmicWatchdogWindowPeriodEnable

This field is used to enable/disable the Watchdog Window Period (FS\_WD\_WINDOW\_DUR[WD\_WINDOW] = DISABLED).

The Watchdog Window Period is derived from the Fail-Safe oscillator with a  $\pm -5\%$  accuracy.

- 0 Watchdog Window Period is Disabled
- 1 Watchdog Window Period is Enabled

Note: This field is editable only when the Watchdog Monitoring is enabled

by OTP (i.e. PmicOtpFailSafeUnitConfiguration/PmicOtpSafetyIOConfiguration/

PmicWatchdogEnable = 'true')

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

# 4.394 Parameter PmicWatchdogWindowPeriod\_Setting

Controls the Watchdog Window Period (FS\_WD\_WINDOW\_DUR[WD\_WINDOW]).

This new watchdog window period is effective after the next

watchdog refresh.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	TIME_3MS
literals	['TIME_1MS', 'TIME_2MS', 'TIME_3MS', 'TIME_4MS', 'TIME_6MS', 'TI $\leftarrow$
	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$
	$\begin{array}{ c c c c c c c c c c c c c c c c c c c$
	MS']

### 4.395 Parameter PmicWatchdogClosedWindowDutyCycle\_Setting

 ${\bf Controls\ the\ Watchdog\ Window\ Duty\ Cycle\ (FS\_WD\_WINDOW\_DUR[WDW\_DC])}.$ 

This new duty cycle is effective after the next watchdog refresh.

The first half of the window is said CLOSED and the second half is

said OPEN. A good watchdog refresh is a good watchdog answer during

the OPEN window. A bad watchdog refresh is a bad watchdog answer

during the OPEN window, no watchdog refresh during the OPEN window

or a good watchdog answer during the CLOSED window. After a good

or bad watchdog refresh, a new window period starts immediately

for the MCU to keep the synchronization with the windowed watchdog.

Note: The OPEN window duty cycle is equal to (100 - PmicWatchdogClosedWindowDutyCycle)%.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
NXR Bend vanduatvasue	true S32 PMIC Driver 249
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueConngClasses	VARIANT POST RIIII D. POST RIIII D

#### 4.396 Parameter PmicWatchdogRecoveryWindowPeriod

Controls the Watchdog Window Duration when the device is in Fault Recovery Strategy (FS\_WD\_WINDOW\_DUR[WDW\_F

When a fault is triggered by the MCU via its FCCU pins, the FS0B is asserted by the device and the watchdog window duration becomes automatically an open window (no more duty cycle), whose duration is given by this field.

The transition from the normal watchdog window duration to this new open window duration happens when the FCCU pin indicates an error and FS0B is asserted. If the MCU sends a good watchdog refresh before the end of the open window duration, the device switches bask to the normal watchdog window duration and associated duty cycle if the FCCU pins do not indicate an error anymore. Otherwise, a new open window period is started. If the MCU does not send a good watchdog refresh before the end of this second open window duration, then a reset pulse is generated and the Fail-Safe State Machine moves back to INIT\_FS.

Note: This field is editable only when the Watchdog Monitoring is enabled by OTP (i.e. PmicOtpFailSafeUnitConfiguration/PmicOtpSafetyIOConfiguration/PmicWatchdogEnable = 'true')

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	TIME_64MS
literals	['DISABLE', 'TIME_1MS', 'TIME_2MS', 'TIME_3MS', 'TIME_4MS', 'TIM←
	E_6MS', 'TIME_8MS', 'TIME_12MS', 'TIME_16MS', 'TIME_24MS', 'TIME
	$32\text{MS'}$ , 'TIME_64MS', 'TIME_128MS', 'TIME_256MS', 'TIME_512MS', 'T $\leftarrow$
	IME_1024MS']

### 4.397 Parameter PmicWatchdogSeed

Configures the Watchdog Seed (FS\_WD\_SEED[WD\_SEED]).

This value is used to calculate the value to be written in the WD\_ANSWER

register during the OPEN watchdog window.

Note: This field is editable only when the Watchdog Monitoring is enabled

by OTP (i.e. PmicOtpFailSafeUnitConfiguration/PmicOtpSafetyIOConfiguration/

PmicWatchdogEnable = 'true')

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	23218
max	65534
min	1

## 4.398 Container PmicWatchdogSettingConf

This container contains the configuration for the Watchdog settings of the PMIC.

If the Watchdog Monitoring is enabled by OTP, the list must have at least one element.

Otherwise, the list must be empty.

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE

### 4.399 Parameter PmicWatchdogSettingId

This parameter shall represent the ID of the Watchdog configuration.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	true
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	0
max	255
min	0

# ${\bf 4.400} \quad {\bf Parameter} \ {\bf PmicWatchdogWindowPeriod}$

Controls the Watchdog Window Period (FS\_WD\_WINDOW\_DUR[WD\_WINDOW]).

This new watchdog window period is effective after the next

watchdog refresh.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	TIME_3MS
literals	['TIME_1MS', 'TIME_2MS', 'TIME_3MS', 'TIME_4MS', 'TIME_6MS', 'TI↔
	ME_8MS', 'TIME_12MS', 'TIME_16MS', 'TIME_24MS', 'TIME_32MS', 'T $\leftarrow$
	$\begin{array}{ c c c c c c c c c c c c c c c c c c c$
	MS']

### 4.401 Parameter PmicWatchdogClosedWindowDutyCycle

Controls the Watchdog Window Duty Cycle (FS\_WD\_WINDOW\_DUR[WDW\_DC]).

This new duty cycle is effective after the next watchdog refresh.

The first half of the window is said CLOSED and the second half is

said OPEN. A good watchdog refresh is a good watchdog answer during

the OPEN window. A bad watchdog refresh is a bad watchdog answer

during the OPEN window, no watchdog refresh during the OPEN window

or a good watchdog answer during the CLOSED window. After a good

or bad watchdog refresh, a new window period starts immediately

for the MCU to keep the synchronization with the windowed watchdog.

Note: The OPEN window duty cycle is equal to (100 - PmicWatchdogClosedWindowDutyCycle)%.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
NXR Benetvanduatvasue	true S32 PMIC Driver 253
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	WARIANT POST RIII D. POST RIII D

### 4.402 Container PmicABIST2Configuration

This container contains the initial configuration parameters (set in the INIT\_FS state) for the ABIST2 checks.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

#### 4.403 Parameter PmicHVLdoMonitorABIST2Enable

Configures whether HVLDOMON is checked by ABIST2 or not (FS\_I\_ABIST2\_CTRL[HVLDO\_VMON\_ABIST2]).

The Fail-Safe State Machine includes two ABISTs to verify the correct functionality

of the safety analog monitoring. ABIST2 is executed on demand by I2C request after

INIT\_FS closure and before releasing the FS0B pin.

It is recommended to verify latent faults on VCOREMON, HVLDOMON, and VDDIOMON during

ABIST1, while the latent faults on VMONx can be verified either during ABIST1 or

ABIST2.

In case of ABIST2 fail, the FS0B pin remains stuck low and cannot be released.

- 0 HVLDOMON check by ABIST2 is Disabled
- 1 HVLDOMON check by ABIST2 is Enabled

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

#### 4.404 Parameter PmicVcoreMonitorABIST2Enable

Configures whether VCOREMON is checked by ABIST2 or not (FS\_I\_ABIST2\_CTRL[VCORE\_ABIST2]).

The Fail-Safe State Machine includes two ABISTs to verify the correct functionality

of the safety analog monitoring. ABIST2 is executed on demand by I2C request after

INIT\_FS closure and before releasing the FS0B pin.

It is recommended to verify latent faults on VCOREMON, HVLDOMON, and VDDIOMON during

ABIST1, while the latent faults on VMONx can be verified either during ABIST1 or

ABIST2.

In case of ABIST2 fail, the FS0B pin remains stuck low and cannot be released.

- 0 VCOREMON check by ABIST2 is Disabled
- 1 VCOREMON check by ABIST2 is Enabled

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

#### 4.405 Parameter PmicVddioMonitorABIST2Enable

Configures whether VDDIOMON is checked by ABIST2 or not (FS I ABIST2 CTRL[VDDIO ABIST2]).

The Fail-Safe State Machine includes two ABISTs to verify the correct functionality

of the safety analog monitoring. ABIST2 is executed on demand by I2C request after

INIT\_FS closure and before releasing the FS0B pin.

It is recommended to verify latent faults on VCOREMON, HVLDOMON, and VDDIOMON during

ABIST1, while the latent faults on VMONx can be verified either during ABIST1 or

ABIST2.

In case of ABIST2 fail, the FS0B pin remains stuck low and cannot be released.

0 - VDDIOMON check by ABIST2 is Disabled

1 - VDDIOMON check by ABIST2 is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

#### 4.406 Parameter PmicVmon1MonitorABIST2Enable

Configures whether VMON1 is checked by ABIST2 or not (FS I ABIST2 CTRL[VMON1 ABIST2]).

The Fail-Safe State Machine includes two ABISTs to verify the correct functionality

of the safety analog monitoring. ABIST2 is executed on demand by I2C request after

INIT FS closure and before releasing the FS0B pin.

It is recommended to verify latent faults on VCOREMON, HVLDOMON, and VDDIOMON during

ABIST1, while the latent faults on VMONx can be verified either during ABIST1 or

ABIST2.

In case of ABIST2 fail, the FS0B pin remains stuck low and cannot be released.

- 0 VMON1 check by ABIST2 is Disabled
- 1 VMON1 check by ABIST2 is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

#### 4.407 Parameter PmicVmon2MonitorABIST2Enable

Configures whether VMON2 is checked by ABIST2 or not (FS\_I\_ABIST2\_CTRL[VMON2\_ABIST2]).

The Fail-Safe State Machine includes two ABISTs to verify the correct functionality

of the safety analog monitoring. ABIST2 is executed on demand by I2C request after

INIT FS closure and before releasing the FS0B pin.

It is recommended to verify latent faults on VCOREMON, HVLDOMON, and VDDIOMON during

ABIST1, while the latent faults on VMONx can be verified either during ABIST1 or

ABIST2.

In case of ABIST2 fail, the FS0B pin remains stuck low and cannot be released.

- 0 VMON2 check by ABIST2 is Disabled
- 1 VMON2 check by ABIST2 is Enabled

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComingClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

#### 4.408 Parameter PmicVmon3MonitorABIST2Enable

Configures whether VMON3 is checked by ABIST2 or not (FS\_I\_ABIST2\_CTRL[VMON3\_ABIST2]).

The Fail-Safe State Machine includes two ABISTs to verify the correct functionality

of the safety analog monitoring. ABIST2 is executed on demand by I2C request after

INIT FS closure and before releasing the FS0B pin.

It is recommended to verify latent faults on VCOREMON, HVLDOMON, and VDDIOMON during

ABIST1, while the latent faults on VMONx can be verified either during ABIST1 or

#### ABIST2.

In case of ABIST2 fail, the FS0B pin remains stuck low and cannot be released.

- 0 VMON3 check by ABIST2 is Disabled
- 1 VMON3 check by ABIST2 is Enabled

Property	Value	
type	ECUC-BOOLEAN-PARAM-DEF	
origin	NXP	
${\it symbolic} \\ {\it NameValue}$	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	true	
valueConfigClasses S	VARIANT-PRE-COMPILE: PRE-COMPILE 32 PMIC Driver NX: VARIANT-POST-BUILD: POST-BUILD	P Semiconducto
defaultValue	false	

#### 4.409 Parameter PmicVmon4MonitorABIST2Enable

Configures whether VMON4 is checked by ABIST2 or not (FS\_I\_ABIST2\_CTRL[VMON4\_ABIST2]).

The Fail-Safe State Machine includes two ABISTs to verify the correct functionality

of the safety analog monitoring. ABIST2 is executed on demand by I2C request after

INIT\_FS closure and before releasing the FS0B pin.

It is recommended to verify latent faults on VCOREMON, HVLDOMON, and VDDIOMON during

ABIST1, while the latent faults on VMONx can be verified either during ABIST1 or

ABIST2.

In case of ABIST2 fail, the FS0B pin remains stuck low and cannot be released.

0 - VMON4 check by ABIST2 is Disabled

1 - VMON4 check by ABIST2 is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

## 4.410 Container PmicSafeInputsConfiguration

This container contains the initial configuration parameters (set in the INIT\_FS state) for the safe inputs (FCCU + Standby Timing Window).

Note: Implementation Specific Parameter.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

### 4.411 Parameter PmicSafetyStandbyWindowDuration

Configures the safety standby window duration (FS\_I\_SAFE\_INPUTS[TIMING\_WINDOW\_STBY]).

There are two possible transitioning paths to Standby Mode (selected via OTP):

- Standard path using only STBY pin transition.
- Safety path using an I2C request + STBY pin transition.

If the safety path is used, this field defines the maximum timeout between the

I2C request and the STBY pin transition.

This field is editable only if the safety standby window is enabled by OTP

 $(i.e.\ PmicOtpFailSafeUnitConfiguration/PmicOtpSafetyIOConfiguration/PmicSafetyStandbyWindowEnable = 'true')$ 

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	TIME_1MS
literals	['DISABLED', 'TIME_60US', 'TIME_80US', 'TIME_100US', 'TIME_200US', 'TIME_300US', 'TIME_500US', 'TIME_1MS', 'TIME_2MS', 'TIME_3MS', 'TIME_5MS', 'TIME_8MS', 'TIME_10MS']

#### 4.412 Parameter PmicFccuMonitoringConfiguration

Configures the operating mode of the FCCU monitoring (FS\_I\_SAFE\_INPUTS[FCCU\_CFG]).

The FCCU input pins are in charge of monitoring the HW failure from MCU. The FCCU

monitoring is active as soon as the INIT\_FS is losed by the first good watchdog refresh.

The FCCU input pins can be configured by pair or as single independent inputs.

When FCCU1 and/or FCCU2 are used independently, the FCCU inputs can monitor 2 different and independent error signals.

Note: This field is editable only when the FCCU Monitoring is enabled by OTP

(i.e. PmicOtpFailSafeUnitConfiguration/PmicOtpSafetyIOConfiguration/PmicFccuEnable = 'true')

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FCCU1_AND_FCCU2_PAIR
literals	['DISABLED', 'FCCU1_AND_FCCU2_PAIR', 'FCCU1_OR_FCCU2_IND← EPENDENT', 'FCCU1_ONLY']

## 4.413 Parameter PmicFccu12FaultPolarity

Configures the fault polarity of the FCCU12 signal (FS\_I\_SAFE\_INPUTS[FCCU12\_FLT\_POL]).

When FCCU12 are used by pair, the bi-stable protocol is employed.

 $\label{eq:fccu1_low_or_fccu2} FCCU1\_LOW\_OR\_FCCU2\_HIGH\_IS\_FAULT - External pull-up resistor to VDDIO on FCCU2 and pull-down$ 

resistor to GND on FCCU1 are required to provide passive error state if the MCU does

not drive its FCCU output pins.

 $\label{eq:fccu1} FCCU1\_HIGH\_OR\_FCCU2\_LOW\_IS\_FAULT - External pull-up \ resistor \ to \ VDDIO \ on \ FCCU1 \ and \ pull-down$ 

resistor to GND on FCCU2 are required to provide passive error state if the MCU does not drive its FCCU output pins.

The pull-down resistor value must be at least 4 times bigger than the pull-up resistor in order

to detect FCCU1-short-to-FCCU2 failure mode, whatever the VDDIO voltage is (1.8V or 3.3V).

Note: This field is editable only when the FCCU Monitoring is enabled by OTP

(i.e. PmicOtpFailSafeUnitConfiguration/PmicOtpSafetyIOConfiguration/PmicFccuEnable = 'true')

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FCCU1_LOW_OR_FCCU2_HIGH_IS_FAULT
literals	['FCCU1_LOW_OR_FCCU2_HIGH_IS_FAULT', 'FCCU1_HIGH_OR_F $\leftarrow$ CCU2_LOW_IS_FAULT']

## 4.414 Parameter PmicFccu12FaultImpact

Configures the Fail-Safe reaction on RSTB and/or FS0B when a FCCU12

 $fault \ is \ detected \ (FS\_I\_SAFE\_INPUTS[FCCU12\_FS\_IMPACT]).$ 

Note: This field is editable only when the FCCU Monitoring is enabled by OTP

(i.e. PmicOtpFailSafeUnitConfiguration/PmicOtpSafetyIOConfiguration/PmicFccuEnable = 'true')

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FS0B_AND_RSTB_ASSERT
literals	['FS0B_ASSERT', 'FS0B_AND_RSTB_ASSERT']

### 4.415 Parameter PmicFccu1FaultPolarity

Configures the fault polarity of the FCCU1 signal (FS\_I\_SAFE\_INPUTS[FCCU1\_FLT\_POL]).

Note: This field is editable only when the FCCU Monitoring is enabled by OTP

 $(i.e.\ PmicOtpFailSafeUnitConfiguration/PmicOtpSafetyIOConfiguration/PmicFccuEnable = 'true')$ 

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	LOW_LEVEL_IS_FAULT
literals	['LOW_LEVEL_IS_FAULT', 'HIGH_LEVEL_IS_FAULT']

## 4.416 Parameter PmicFccu1FaultImpact

Configures the Fail-Safe reaction on RSTB and/or FS0B when a FCCU1

fault is detected (FS\_I\_SAFE\_INPUTS[FCCU1\_FS\_IMPACT]).

Note: This field is editable only when the FCCU Monitoring is enabled by OTP

 $(i.e.\ PmicOtpFailSafeUnitConfiguration/PmicOtpSafetyIOConfiguration/PmicFccuEnable = 'true')$ 

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FS0B_AND_RSTB_ASSERT
literals	['FS0B_ASSERT', 'FS0B_AND_RSTB_ASSERT']

## 4.417 Parameter PmicFccu2FaultPolarity

Configures the fault polarity of the FCCU2 signal (FS\_I\_SAFE\_INPUTS[FCCU2\_FLT\_POL]).

Note: This field is editable only when the FCCU Monitoring is enabled by OTP

 $(i.e.\ PmicOtpFailSafeUnitConfiguration/PmicOtpSafetyIOConfiguration/PmicFccuEnable = 'true')$ 

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	LOW_LEVEL_IS_FAULT
literals	['LOW_LEVEL_IS_FAULT', 'HIGH_LEVEL_IS_FAULT']

### 4.418 Parameter PmicFccu2FaultImpact

Configures the Fail-Safe reaction on RSTB and/or FS0B when a FCCU2

fault is detected (FS\_I\_SAFE\_INPUTS[FCCU2\_FS\_IMPACT]).

Note: This field is editable only when the FCCU Monitoring is enabled by OTP

 $(i.e.\ PmicOtpFailSafeUnitConfiguration/PmicOtpSafetyIOConfiguration/PmicFccuEnable = 'true')$ 

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FS0B_AND_RSTB_ASSERT
literals	['FS0B_ASSERT', 'FS0B_AND_RSTB_ASSERT']

## 4.419 Container PmicStateMachineConfiguration

This container contains the initial configuration parameters (set in the INIT\_FS state) for the state machine functionality of the Fail-Safe Unit.

Note: Implementation Specific Parameter.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

#### 4.420 Parameter PmicFaultErrorCounterLimit

Controls the Fault Error Counter Limit (FS\_I\_FSSM[FLT\_ERR\_CNT\_LIMIT]).

The Fault Error Counter counts the number of faults occuring in the system

(related to the device itself and also caused by external events).

The Fault Error Counter is incremented by 1 each time the RSTB and/or FS0B

pin is asserted and each time the Watchdog Error Counter Limit is reached.

It is decremented by 1 each time the Watchdog Refresh Counter Limit is reached.

The Fault Error Counter has two output values: Intermediate and Final. The

intermediate value is calculated as FEC\_Limit / 2 (i.e. the value of this

field divided by 2).

This maximum limit of the Fault Error Counter is used to transition in

Deep Fail-Safe mode.

After each power-up or wake-up from Standby mode, the Fault Error Counter

starts at level 1 to ensure the safe state. It is recommended to read

this counter and decrement it to an appropriate value by several

consecutive good Watchdog refreshes before a reset request by I2C.

The number of consecutive good Watchdog refreshes needed (N) to

decrement the Fault Error Counter to 0 is equal to:

$$N = FS I FSSM[FLT ERR CNT] * (FS I WD CFG[WD RFR LIMIT] + 1).$$

Note: Implementation Specific Parameter.

literals

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue S	32 <sup>M</sup> PMIC Driver NXI

['MAX\_2', 'MAX\_6', 'MAX\_8', 'MAX\_12']

P Semiconductors

### 4.421 Parameter PmicFaultErrorCounterImpact

Configures the Fail-Safe reaction on RSTB and/or FS0B when the Fault

Error Counter reaches its intermediate value (FS\_I\_FSSM[FLT\_ERR\_IMPACT]).

The intermediate value of the Fault Error Counter is equal to:

 $INTERMEDIATE\_VALUE = PmicFaultErrorCounterLimit \ / \ 2.$ 

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FS0B_AND_RSTB_ASSERT
literals	['DISABLED', 'FS0B_ASSERT', 'FS0B_AND_RSTB_ASSERT']

### 4.422 Parameter PmicResetDuration

Configures how long the RSTB signal is kept asserted (FS\_I\_FSSM[RSTB\_DUR]).

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	TIME_10MS
literals	['TIME_10MS', 'TIME_1MS']

### 4.423 Parameter PmicBackupSafetyPath

Configures whether the RSTB pin is asserted when a short-to-high failure is

detected on the FS0B pin (FS\_I\_FSSM[BACKUP\_SAFETY\_PATH]).

A FS0B short-to-high failure is detected after a duration of maximum 815us.

The RSTB pin assertion acts as a redundant path to reset the MCU and assert

its FCCU pin.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	RSTB_ASSERT
literals	['DISABLED', 'RSTB_ASSERT']

# 4.424 Parameter PmicClockMonitoringEnable

This field is used to enable/disable the IRCOSC/FIN Clock Monitoring (FS\_I\_FSSM[CLK\_MON\_DIS]).

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	ptrue III

#### 4.425 Parameter PmicRSTBTimerEnable

This field is used to enable/disable the 8s RSTB timer (FS\_I\_FSSM[DIS8S]).

If enabled, the 8s RSTB timer starts each time the RSTB pin is asserted low.

When the LBIST is done, the 8s timer monitoring the RSTB pin starts and

the ABIST1 is automatically executed when all the regulators assigned to

ABIST1 have passed their UV and OV checks. When the ABIST1 is done,

RSTB and PGOOD pins are released, and the initialization of the device

is opened for 256ms. ABIST1 fail does not prevent RSTB and PGOOD release.

If RSTB is not released before the RSTB timer expires (i.e. within

8 seconds), the device will go into Deep Fail-Safe Mode.

0 - RSTB Timer is Disabled

1 - RSTB Timer is Enabled

Note: This field is editable only when the 8s RSTB Timer is enabled

by OTP (i.e. PmicOtpFailSafeUnitConfiguration/PmicOtpSafetyConfiguration/

PmicRSTBTimerEnable = 'true')

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigCiasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

#### 4.426 Parameter PmicLowPowerClockMonitoringEnable

This field is used to enable/disable the Low Power OSC Clock Monitoring (FS\_I\_FSSM[LPCLK\_MON\_DIS]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

#### 4.427 Container PmicDemEventParameterRefs

Container for the references to DemEventParameter elements which shall be invoked using the API Dem\_ReportErrorStatus API in case the corresponding error occurs. The EventId is taken from the referenced DemEventParameter's DemEventId value. The standardized errors are provided in the container and can be extended by vendor specific error references.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE

## 4.428 Reference PMIC\_E\_ACESS\_FAILURE

Reference to the DemEventParameter which shall be issued when the device is not accesible.

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
${\it requires Symbolic Name Value}$	true
destination	/AUTOSAR/EcucDefs/Dem/DemConfigSet/DemEventParameter

# ${\bf 4.429} \quad {\bf Reference~PMIC\_E\_INTEGRITY\_CORRUPTED}$

Reference to the DemEventParameter which shall be issued when the device reports LBIST, ABIST or OTP failures.

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
requiresSymbolicNameValue	true
destination	/AUTOSAR/EcucDefs/Dem/DemConfigSet/DemEventParameter

## 4.430 Reference PMIC\_E\_SIGNAL\_SHORTED

Reference to the DemEventParameter which shall be issued when the device does not successfully pass the safety signals check.

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP

Property	Value
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
requiresSymbolicNameValue	true
destination	/AUTOSAR/EcucDefs/Dem/DemConfigSet/DemEventParameter

### 4.431 Reference PMIC\_E\_CLOCK\_FAILURE

Reference to the DemEventParameter which shall be issued when the device reports clock failures (e.g. oscillator drifts, unlocked PLLs, etc).

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
${\it requires Symbolic Name Value}$	true
destination	/AUTOSAR/EcucDefs/Dem/DemConfigSet/DemEventParameter

## 4.432 Reference PMIC\_E\_TIMEOUT\_FAILURE

Reference to the DemEventParameter which shall be issued when the error "Timeout caused by hardware error" has occurred.

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	0
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
${\it requires Symbolic Name Value}$	true
destination	/AUTOSAR/EcucDefs/Dem/DemConfigSet/DemEventParameter

# 4.433 Container CommonPublishedInformation

Common container, aggregated by all modules.

It contains published information about vendor and versions.

Included subcontainers:

#### • None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

# ${\bf 4.434} \quad {\bf Parameter} \,\, {\bf ArRelease Major Version}$

Major version number of AUTOSAR specification on which the appropriate implementation is based on.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false

Property	Value
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	4
max	4
min	4

### 4.435 Parameter ArReleaseMinorVersion

Minor version number of AUTOSAR specification on which the appropriate implementation is based on.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	4
max	4
min	4

### 4.436 Parameter ArReleaseRevisionVersion

Revision version number of AUTOSAR specification on which the appropriate implementation is based on.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION

Property	Value
defaultValue	0
max	0
min	0

### 4.437 Parameter ModuleId

Module ID of this module from Module List.

Note: Implementation Specific Parameter

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	255
max	255
min	255

# ${\bf 4.438}\quad {\bf Parameter~SwMajorVersion}$

Major version number of the vendor specific implementation of the module. The numbering is vendor specific.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false

### Tresos Configuration Plug-in

Property	Value
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
varueComigClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	4
max	4
min	4

# 4.439 Parameter SwMinorVersion

Minor version number of the vendor specific implementation of the module. The numbering is vendor specific.

Note: Implementation Specific Parameter

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
varueCollingClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	0
max	0
min	0

# 4.440 Parameter SwPatchVersion

Patch level version number of the vendor specific implementation of the module. The numbering is vendor specific.

Note: Implementation Specific Parameter

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A

Property	Value
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	0
max	0
min	0

# 4.441 Parameter VendorApiInfix

In driver modules which can be instantiated several times on a single ECU, BSW00347 requires that the name of APIs is extended by the VendorId and a vendor specific name.

This parameter is used to specify the vendor specific name. In total, the Implementation specific name is generated as follows:

E.g. assuming that the VendorId of the implementor is 123 and the implementer chose a VendorApiInfix of "v11r456" a api name

Can\_Write defined in the SWS will translate to Can\_123\_v11r456Write.

This parameter is mandatory for all modules with upper multiplicity >

1. It shall not be used for modules with upper multiplicity =1.

Note: Implementation Specific Parameter

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	

# 4.442 Parameter VendorId

Vendor ID of the dedicated implementation of this module according to the AUTOSAR vendor list.

Note: Implementation Specific Parameter

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
varueCollingClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	43
max	43
min	43

This chapter describes the Tresos configuration plug-in for the Pmic Driver. The most of the parameters are described below.

# **Chapter 5**

# **Module Index**

# 5.1 Software Specification

Here is a list of all modules:

Pmic HLD	280
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# **Chapter 6**

# **Module Documentation**

# 6.1 Pmic HLD

# 6.1.1 Detailed Description

### **Data Structures**

 $\bullet \ \ struct \ Pmic\_RawFaultType$ 

The structure containing the raw fault events for a PMIC device. More...

• struct Pmic\_DeviceInfoType

The device information structure for a PMIC device. More...

• struct Pmic\_InterfaceUnitConfigType

The interface configuration structure for a PMIC device. More...

• struct Pmic\_DeviceConfigType

Configuration structure for a PMIC device. More...

• struct Pmic\_DemConfigType

DEM error reporting configuration. More...

• struct Pmic\_ConfigType

Configuration structure of the driver. More...

### Macros

• #define PMIC\_E\_OK

Internal return codes.

### Types Reference

• typedef void(\* Pmic\_WdgTaskNotificationType) (const Pmic\_DeviceIndexType DeviceId, const uint8 u8↔ WdWindowValue, const uint8 u8WdDcValue)

This gives the call-out type for watchdog task notifications.

### **Enum Reference**

• enum Pmic\_ApiServiceIdType

API service IDs.

• enum Pmic\_ErrorIdType

Error IDs.

• enum Pmic\_InterfaceType

Interface selection.

• enum Pmic\_InterfaceDstType

Interface destination selection.

### **Function Reference**

• void Pmic\_Init (const Pmic\_ConfigType \*pConfigPtr)

Pmic Init.

• Std\_ReturnType Pmic\_InitDevice (const Pmic\_DeviceIndexType DeviceId)

 $Pmic\_InitDevice.$ 

• Std\_ReturnType Pmic\_EmulateDeviceOTP (const Pmic\_DeviceIndexType DeviceId)

Pmic EmulateDeviceOTP.

• Std\_ReturnType Pmic\_ReadRegister (const Pmic\_DeviceIndexType DeviceId, const Pmic\_InterfaceDstType eDestination, const uint8 u8RegAddr, uint16 \*pu16ValueOut)

 $Pmic\_ReadRegister.$ 

• Std\_ReturnType Pmic\_WriteRegister (const Pmic\_DeviceIndexType DeviceId, const Pmic\_InterfaceDstType eDestination, const uint8 u8RegAddr, const uint16 u16WriteValue)

 $Pmic\_WriteRegister.$ 

• Std\_ReturnType Pmic\_InitClock (const Pmic\_DeviceIndexType DeviceId, const Pmic\_ClockSettingIndex ← Type ClockSettingId)

 $Pmic\_InitClock.$ 

• Std\_ReturnType Pmic\_SetMode (const Pmic\_DeviceIndexType DeviceId, const Pmic\_ModeIndexType ModeSettingId)

 $Pmic\_SetMode.$ 

• Std\_ReturnType Pmic\_SetAnalogMux (const Pmic\_DeviceIndexType DeviceId, const Pmic\_Amux ChannelIndexType AmuxChannelId)

 $Pmic\_SetAnalogMux.$ 

• Std\_ReturnType Pmic\_SwitchSVS (const Pmic\_DeviceIndexType DeviceId, const Pmic\_SvsSettingIndex

Type SvsSettingID)

 $Pmic\_SwitchSVS.$ 

• Std\_ReturnType Pmic\_ConfigureWatchdog (const Pmic\_DeviceIndexType DeviceId, const Pmic\_ WatchdogSettingIndexType WatchdogSettingId)

Pmic\_Configure Watchdog.

• void Pmic TriggerWatchdog (const Pmic DeviceIndexType DeviceId)

 $Pmic\_TriggerWatchdog.$ 

• Std ReturnType Pmic DisableWatchdog (const Pmic DeviceIndexType DeviceId)

 $Pmic\_Disable Watchdog.$ 

• Std ReturnType Pmic ReleaseFs0b (const Pmic DeviceIndexType DeviceId)

PMIC executes the release safety FS0B pin.

• Std ReturnType Pmic GotoInitFS (const Pmic DeviceIndexType DeviceId)

 $Pmic\_GotoInitFS.$ 

• Std\_ReturnType Pmic\_GetRawFaultEvents (const Pmic\_DeviceIndexType DeviceId, Pmic\_RawFaultType \*pRawFaultEventsOut)

 $Pmic\_GetRawFaultEvents.$ 

• Std\_ReturnType Pmic\_SetReactions (const Pmic\_DeviceIndexType DeviceId, const Pmic\_ReactionSetting ← IndexType ReactionSettingId)

Pmic SetReactions.

• Std\_ReturnType Pmic\_GetDeviceInfo (const Pmic\_DeviceIndexType DeviceId, Pmic\_DeviceInfoType \*p↔ DeviceInfoOut)

Pmic GetDeviceInfo.

void Pmic\_GetVersionInfo (Std\_VersionInfoType \*pVersionInfoOut)

 $Pmic\_GetVersionInfo.$ 

• void Pmic Dem Check Device (const Pmic ReturnType eStatusCode)

API checks status and report the device run time error.

• Std ReturnType Pmic HLDChecksEntry (const Pmic ApiServiceIdType ePmicServiceID)

API checks the Pmic\_Init executed successfully before.

• void Pmic\_HLDChecksExit (const Std\_ReturnType eRetStatus, const Pmic\_ApiServiceIdType ePmic← ServiceID)

API checks the Pmic driver status in Pmic\_Init API.

• Std\_ReturnType Pmic\_HLDDeviceChecksEntry (const Pmic\_DeviceIndexType u32DeviceId, const Pmic\_ApiServiceIdType ePmicServiceID)

API checks the PMIC device already initialized before call another API.

• void Pmic\_HLDDeviceChecksExit (const Std\_ReturnType eRetStatus, const Pmic\_DeviceIndexType u32← DeviceId, const Pmic\_ApiServiceIdType ePmicServiceID)

API checks the Pmic driver status when user executes the Pmic\_InitDevice, Pmic\_EmulateDeviceOTP API.

• Std\_ReturnType Pmic\_Check\_Init (const Pmic\_ConfigType \*pConfigPtr)

API checks the Pmic\_Init parameter input valid.

• Std\_ReturnType Pmic\_Check\_ReadRegister (const Pmic\_DeviceIndexType u32DeviceId, const uint8 u8← RegAddr, const uint16 \*pu16ValueOut)

API checks the Pmic\_ReadRegister parameter input valid.

• Std\_ReturnType Pmic\_Check\_WriteRegister (const Pmic\_DeviceIndexType u32DeviceId, const uint8 u8← RegAddr)

API checks the Pmic\_WriteRegister parameter input valid.

• Std\_ReturnType Pmic\_Check\_SetMode (const Pmic\_DeviceIndexType u32DeviceId, const Pmic\_Mode ← IndexType u32ModeSettingId)

 $API\ checks\ the\ Pmic\_Setmode\ parameter\ input\ valid.$ 

• Std\_ReturnType Pmic\_Check\_InitClock (const Pmic\_DeviceIndexType u32DeviceId, const Pmic\_Clock← SettingIndexType u32ClockSettingID)

API checks the Pmic InitClock parameter input valid.

• Std\_ReturnType Pmic\_Check\_SetAnalogMux (const Pmic\_DeviceIndexType u32DeviceId, const Pmic\_← AmuxChannelIndexType u32AmuxChannelId)

API checks the Pmic\_SetAnalogMux parameter input valid.

• Std\_ReturnType Pmic\_Check\_SwitchSVS (const Pmic\_DeviceIndexType u32DeviceId, const Pmic\_Svs← SettingIndexType u32SvsSettingID)

API checks the Pmic\_SwitchSVS parameter input valid.

• Std\_ReturnType Pmic\_Check\_ConfigureWatchdog (const Pmic\_DeviceIndexType u32DeviceId, const Pmic WatchdogSettingIndexType u32WatchdogSettingId)

 $API\ checks\ the\ Pmic\_Configure\ Watchdog\ parameter\ input\ valid.$ 

• Std ReturnType Pmic Check TriggerWatchdog (const Pmic DeviceIndexType u32DeviceId)

API checks the Pmic\_TriggerWatchdog parameter input valid.

• Std\_ReturnType Pmic\_Check\_GotoInitFS (const Pmic\_DeviceIndexType u32DeviceId)

 $API\ checks\ the\ Pmic\_GotoInitFS\ parameter\ input\ valid.$ 

 $\bullet \ \ Std\_ReturnType\ Pmic\_Check\_GetRawFaultEvents\ (const\ Pmic\_RawFaultType\ *pRawFaultEventsOut)$ 

API checks the Pmic\_GetRawFaultEvents parameter input valid.

• Std\_ReturnType Pmic\_Check\_SetReactions (const Pmic\_DeviceIndexType u32DeviceId, const Pmic\_← ReactionSettingIndexType u32ReactionSettingId)

API checks the Pmic\_SetReactions parameter input valid.

 $\bullet \quad Std\_ReturnType \ Pmic\_Check\_GetDeviceInfo \ (const \ Pmic\_DeviceInfoType \ *pDeviceInfoOut)$ 

 $API\ checks\ the\ Pmic\_GetDeviceInfo\ parameter\ input\ valid.$ 

• Std\_ReturnType Pmic\_Check\_GetVersionInfo (const Std\_VersionInfoType \*pVersionInfo)

API checks the Pmic\_GetVersionInfo parameter input valid.

• void Pmic\_Det\_Check\_ReportErrors (const Pmic\_ReturnType eStatusCode, const Pmic\_ApiServiceIdType eServiceId)

API checks status and report the run time error.

#### Variables

• boolean Pmic\_abTestMode [PMIC\_MAX\_DEVICECONFIGS]

Array used to indicate whether the indexed device is in test mode.

• boolean Pmic abErrorDetected [PMIC MAX DEVICECONFIGS]

Array used to indicate whether the indexed device encountered an error.

• boolean Pmic\_abGateWdgTrigger [PMIC\_MAX\_DEVICECONFIGS]

Array used to indicate watchdog trigger will be forwarded to the device.

• boolean Pmic\_abIsWdgTrigger [PMIC\_MAX\_DEVICECONFIGS]

Array used to check watchdog trigger in progress or not. When Wdq\_trigger is in-progress, variable will set true.

### 6.1.2 Data Structure Documentation

### 6.1.2.1 struct Pmic\_RawFaultType

The structure containing the raw fault events for a PMIC device.

Contains various error flags of the Main-Unit and Fail-Safe Unit.

Definition at line 255 of file Pmic\_Types.h.

#### 6.1.2.2 struct Pmic\_DeviceInfoType

The device information structure for a PMIC device.

It contains the family id and the device id of the PMIC device.

Definition at line 267 of file Pmic Types.h.

# ${\bf 6.1.2.3 \quad struct \ Pmic\_Interface Unit Config Type}$

The interface configuration structure for a PMIC device.

It contains the type of the interface, of the communication, and the device address.

Definition at line 290 of file Pmic\_Types.h.

#### Data Fields

Type	Name	Description
Pmic_InterfaceType	eInterfaceType	The type of the interface.
uint8	u8ChannelId	The channel id of the interface.
uint8	u8MainUnitAddress	The address used to communicate with the Main Unit.
uint8	u8 Fail Safe Unit Address	The address used to communicate with the Fail-Safe Unit.
uint32	u32I2cSclPinIndex	The scl pin index.
uint8	u8I2cSclPinInitialMode	The device's i2c scl pin - initial mode.
uint8	u8I2cSclPinMode	The device's i2c scl pin - mode.
uint32	u32CPUFreq	The device's operating frequency.
uint32	u32I2cFreq	The device's i2c channel frequency.
uint16	u16I2cSclDioChannelId	The device's dio channel id.

### 6.1.2.4 struct Pmic\_DeviceConfigType

Configuration structure for a PMIC device.

It contains the configuration that a particular PMIC device is using.

Definition at line 312 of file Pmic\_Types.h.

#### **Data Fields**

• uint8 u8DeviceUnitId

Numeric instance value of the PMIC device.

• uint8 u8NrOfModeConfigs

Total number of mode configurations.

• uint8 u8NrOfClockConfigs

 $Total\ number\ of\ clock\ configurations.$ 

• uint8 u8NrOfReactionConfigs

Total number of reaction configurations.

• uint8 u8NrOfAmuxChannelConfigs

Total number of AMUX channel configurations.

uint8 u8NrOfSVSConfigs

Total number of SVS configurations.

• uint8 u8NrOfWatchdogConfigs

Total number of watchdog configurations.

• const Pmic\_Ipw\_ModeConfigType(\* paModeConfig )[]

Mode data configurations.

• const Pmic\_Ipw\_ClockConfigType(\* paClockConfig )[]

Clock data configurations.

• const Pmic\_Ipw\_ReactionConfigType(\* paReactionConfig )[]

Reaction data configurations.

• const Pmic\_Ipw\_AmuxChannelConfigType(\* paAmuxChannelConfig )[]

 $AMUX\ channel\ configurations.$ 

• const Pmic\_Ipw\_SVSConfigType(\* paSVSConfig )[]

 $SVS\ configurations.$ 

• const Pmic\_Ipw\_WatchdogConfigType(\* paWatchdogConfig )[]

Watchdog data configurations.

• Pmic\_InterfaceUnitConfigType \* pInterfaceConfig

The configuration of the interface used to communicate with the PMIC device.

• const Pmic\_Ipw\_HwDeviceConfigType \* pHwDeviceConfig

The hardware configuration of the PMIC device.

## 6.1.2.4.1 Field Documentation

#### 6.1.2.4.1.1 u8DeviceUnitId uint8 u8DeviceUnitId

Numeric instance value of the PMIC device.

Definition at line 314 of file Pmic Types.h.

#### 6.1.2.4.1.2 u8NrOfModeConfigs uint8 u8NrOfModeConfigs

Total number of mode configurations.

Definition at line 315 of file Pmic Types.h.

#### 6.1.2.4.1.3 u8NrOfClockConfigs uint8 u8NrOfClockConfigs

Total number of clock configurations.

Definition at line 316 of file Pmic\_Types.h.

### $6.1.2.4.1.4 \quad u8NrOfR eaction Configs \quad \verb"uint8 u8NrOfR eaction Configs"$

Total number of reaction configurations.

Definition at line 317 of file Pmic\_Types.h.

### $6.1.2.4.1.5 \quad u8NrOfAmuxChannelConfigs \quad \verb"uint8 u8NrOfAmuxChannelConfigs" \\$

Total number of AMUX channel configurations.

Definition at line 319 of file Pmic\_Types.h.

### $6.1.2.4.1.6 \quad u8NrOfSVSConfigs \quad \verb"uint8 u8NrOfSVSConfigs"$

Total number of SVS configurations.

Definition at line 322 of file Pmic\_Types.h.

### 6.1.2.4.1.7 u8NrOfWatchdogConfigs uint8 u8NrOfWatchdogConfigs

Total number of watchdog configurations.

Definition at line 325 of file Pmic\_Types.h.

### $6.1.2.4.1.8 \quad paModeConfig \quad \texttt{const Pmic_Ipw\_ModeConfigType} \ (* \ paModeConfig) \ [\ ]$

Mode data configurations.

Definition at line 327 of file Pmic\_Types.h.

### **6.1.2.4.1.9** paClockConfig const Pmic\_Ipw\_ClockConfigType(\* paClockConfig)[]

Clock data configurations.

Definition at line 328 of file Pmic\_Types.h.

6.1.2.4.1.10 paReactionConfig const Pmic\_Ipw\_ReactionConfigType(\* paReactionConfig)[]

Reaction data configurations.

Definition at line 329 of file Pmic\_Types.h.

 $\mathbf{6.1.2.4.1.11} \quad \mathbf{paAmuxChannelConfig} \quad \mathtt{const} \; \; \mathtt{Pmic\_Ipw\_AmuxChannelConfigType} \, (* \; \mathtt{paAmuxChannelConfig}) \; [ \; ]$ 

AMUX channel configurations.

Definition at line 331 of file Pmic\_Types.h.

6.1.2.4.1.12 paSVSConfig const Pmic\_Ipw\_SVSConfigType(\* paSVSConfig)[]

SVS configurations.

Definition at line 334 of file Pmic\_Types.h.

 $6.1.2.4.1.13 \quad paWatchdogConfig \quad \texttt{const Pmic\_Ipw\_WatchdogConfigType} \ (* \ paWatchdogConfig) \ [\ ]$ 

Watchdog data configurations.

Definition at line 337 of file Pmic\_Types.h.

 $\mathbf{6.1.2.4.1.14} \quad \mathbf{pInterfaceConfig} \quad \texttt{Pmic\_InterfaceUnitConfigType*} \quad \mathtt{pInterfaceConfig}$ 

The configuration of the interface used to communicate with the PMIC device.

Definition at line 339 of file Pmic\_Types.h.

6.1.2.4.1.15 pHwDeviceConfig const Pmic\_Ipw\_HwDeviceConfigType\* pHwDeviceConfig

The hardware configuration of the PMIC device.

Definition at line 340 of file Pmic Types.h.

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#### 6.1.2.5 struct Pmic\_DemConfigType

DEM error reporting configuration.

This structure contains information DEM error reporting.

Definition at line 351 of file Pmic\_Types.h.

#### 6.1.2.6 struct Pmic\_ConfigType

Configuration structure of the driver.

It contains the configuration used for initializing the driver.

Definition at line 368 of file Pmic\_Types.h.

### **Data Fields**

- uint32 Pmic\_u32DiePreocessOcotpIndex

  Index of Ocotp channel read OCOTP\_BANK0\_WORD6.
- uint8 Pmic\_u8NrOfDevices

Total number of configured PMIC devices.

- $\bullet \ \ const \ Pmic\_WdgTaskNotificationType \ Pmic\_pWdgTaskNotification \\$ 
  - Pointer to callout configured by user for watchdog task notifications.
- const Pmic\_DeviceConfigType(\* Pmic\_paDeviceConfig )[PMIC\_MAX\_DEVICECONFIGS] Pointer to list of PMIC device configurations.
- const Pmic\_DemConfigType \* Pmic\_pDemConfig

DEM error reporting configuration.

#### 6.1.2.6.1 Field Documentation

# $\mathbf{6.1.2.6.1.1} \quad Pmic\_u32DiePreocessOcotpIndex \quad \texttt{uint32} \; \texttt{Pmic}\_u32DiePreocessOcotpIndex$

Index of Ocotp channel read OCOTP BANKO WORD6.

Definition at line 371 of file Pmic\_Types.h.

### 6.1.2.6.1.2 Pmic\_u8NrOfDevices uint8 Pmic\_u8NrOfDevices

Total number of configured PMIC devices.

Definition at line 373 of file Pmic\_Types.h.

#### 6.1.2.6.1.3 Pmic\_pWdgTaskNotification const Pmic\_WdgTaskNotificationType Pmic\_pWdgTaskNotification

Pointer to callout configured by user for watchdog task notifications.

Definition at line 375 of file Pmic\_Types.h.

# 6.1.2.6.1.4 Pmic\_paDeviceConfig const Pmic\_DeviceConfigType(\* Pmic\_paDeviceConfig)[PMIC\_MAX\_DEVIC← ECONFIGS]

Pointer to list of PMIC device configurations.

Definition at line 377 of file Pmic\_Types.h.

### $6.1.2.6.1.5 \quad Pmic\_pDemConfig \quad \texttt{const} \; \\ \texttt{Pmic\_DemConfigType*} \; \\ \texttt{Pmic\_pDemConfig}$

DEM error reporting configuration.

Definition at line 379 of file Pmic\_Types.h.

### 6.1.3 Macro Definition Documentation

### 6.1.3.1 PMIC\_E\_OK

#define PMIC\_E\_OK

Internal return codes.

The enumeration with all the internal return codes interpreted by the driver

Definition at line 104 of file Pmic Internals.h.

### 6.1.4 Types Reference

### 6.1.4.1 Pmic\_WdgTaskNotificationType

typedef void(\* Pmic\_WdgTaskNotificationType) (const Pmic\_DeviceIndexType DeviceId, const uint8 u8Wd↔ WindowValue, const uint8 u8WdDcValue)

This gives the call-out type for watchdog task notifications.

Definition at line 247 of file Pmic\_Types.h.

### 6.1.5 Enum Reference

#### 6.1.5.1 Pmic\_ApiServiceIdType

enum Pmic\_ApiServiceIdType

API service IDs.

Service IDs of the PMIC API.

### Enumerator

PMIC_INIT_ID	Pmic_Init() ID.
PMIC_INIT_DEVICE_ID	Pmic_InitDevice() ID.
PMIC_EMULATE_DEVICE_OTP_ID	Pmic_EmulateDeviceOTP() ID.
PMIC_READ_REGISTER_ID	Pmic_ReadRegister() ID.
PMIC_WRITE_REGISTER_ID	Pmic_WriteRegister() ID.
PMIC_INIT_CLOCK_ID	Pmic_InitClock() ID.
PMIC_SET_MODE_ID	Pmic_SetMode() ID.
PMIC_SET_ANALOG_MUX_ID	Pmic_SetAnalogMux() ID.
PMIC_CONFIGURE_WATCHDOG_ID	Pmic_ConfigureWatchdog() ID.
PMIC_TRIGGER_WATCHDOG_ID	Pmic_TriggerWatchdog() ID.
PMIC_GET_RAW_FAULT_EVENTS_ID	Pmic_GetRawFaultEvents() ID.
PMIC_SET_REACTIONS_ID	Pmic_SetReactions() ID.
PMIC_GET_DEVICE_INFO_ID	Pmic_GetDeviceInfo() ID.
PMIC_GET_VERSION_INFO_ID	Pmic_GetVersionInfo() ID.
PMIC_DISABLE_WATCHDOG_ID	Pmic_DisableWatchdog() ID
PMIC_SWITCH_SVS_ID	Pmic_SwitchSVS() ID.
PMIC_GOTO_INITFS_ID	Pmic_GotoInitFS() ID.
PMIC_RELEASE_FS0B_ID	Pmic_ReleaseFs0b() ID.

Definition at line 144 of file Pmic\_Types.h.

# $\bf 6.1.5.2 \quad Pmic\_ErrorIdType$

enum Pmic\_ErrorIdType

Error IDs.

Error IDs of the PMIC API.

### Enumerator

PMIC_E_UNINIT	Driver uninitialized.
PMIC_E_INIT_FAILED	Invalid configuration pointer.
PMIC_E_DEVICE_UNINIT	Device uninitialized.
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PMIC_E_DEVICE_OTP_UNEMU	Un-emulated OTP on blank device.
PMIC_E_PARAM_POINTER	Invalid pointer argument.
PMIC_E_PARAM_DEVICE	Invalid device ID.
PMIC_E_PARAM_MODE	Invalid mode configuration ID.
PMIC_E_PARAM_CLOCK	Invalid clock configuration ID.
PMIC_E_PARAM_WDG	Invalid watchdog configuration ID.
PMIC_E_PARAM_AMUX	Invalid AMUX channel ID
PMIC_E_PARAM_REACTION	Invalid reaction configuration ID.
PMIC_E_PARAM_REG_ADDR	Invalid register address.
PMIC_E_COMM_FAILURE	Underlying communication failed
PMIC_E_INVALID_DATA	CRC Verification Failed
PMIC_E_PARAM_SVS	Invalid SVS ID

Definition at line 186 of file Pmic\_Types.h.

# ${\bf 6.1.5.3}\quad {\bf Pmic\_InterfaceType}$

enum Pmic\_InterfaceType

Interface selection.

The enumeration with interface possibilities

### Enumerator

PMIC_INTERFACE_I2C	Device communicates through I2C.
PMIC_INTERFACE_SPI	Device communicates through SPI.

Definition at line 221 of file Pmic\_Types.h.

### ${\bf 6.1.5.4 \quad Pmic\_InterfaceDstType}$

```
enum Pmic_InterfaceDstType
```

Interface destination selection.

The enumeration with interface destination possibilities.

#### Enumerator

PMIC_MAIN_UNIT	Interface with the Main Unit.
PMIC_FAIL_SAFE_UNIT	Interface with the Fail-Safe Unit.

Definition at line 232 of file Pmic\_Types.h.

# 6.1.6 Function Reference

### 6.1.6.1 Pmic\_Init()

Pmic\_Init.

Parameters

```
in pConfigPtr.
```

Returns

void.

### 6.1.6.2 Pmic\_InitDevice()

```
Std_ReturnType Pmic_InitDevice (

const Pmic_DeviceIndexType DeviceId )
```

 ${\bf Pmic\_InitDevice}.$ 

#### Parameters

in   Dev	$iceId. \mid$

### Returns

 $Std\_ReturnType.$ 

### 6.1.6.3 Pmic\_EmulateDeviceOTP()

### Pmic\_EmulateDeviceOTP.

### Parameters

in DeviceId.	
--------------	--

### Returns

 $Std\_ReturnType.$ 

# 6.1.6.4 Pmic\_ReadRegister()

### $Pmic\_ReadRegister.$

### Parameters

in	DeviceId.	
in	eDestination.	
in	u8RegAddr.	
in	pu16 Value Out.	

#### Returns

 $Std\_ReturnType.$ 

### 6.1.6.5 Pmic\_WriteRegister()

### Pmic\_WriteRegister.

#### Parameters

in	DeviceId.	
in	eDestination.	
in	u8RegAddr.	
in	$u16 {\it Write Value}.$	

### Returns

 $Std\_ReturnType.$ 

### 6.1.6.6 Pmic\_InitClock()

### ${\bf Pmic\_InitClock}.$

### Parameters

in	DeviceId.	
in	Clock Setting Id.	

### Returns

 $Std\_ReturnType.$ 

### 6.1.6.7 Pmic\_SetMode()

 $\operatorname{Pmic}_{\operatorname{SetMode}}$ .

#### Parameters

in	DeviceId.	
in	Mode Setting Id.	

#### Returns

 $Std\_ReturnType.$ 

# $6.1.6.8 \quad Pmic\_SetAnalogMux()$

 $Pmic\_SetAnalogMux.$ 

### Parameters

in	DeviceId.	
in	AmuxChannel Id.	

### Returns

 $Std\_ReturnType.$ 

### 6.1.6.9 Pmic\_SwitchSVS()

Pmic\_SwitchSVS.

### Parameters

in	DeviceId.	
in	SvsSetting ID.	

#### Returns

 $Std\_ReturnType.$ 

### 6.1.6.10 Pmic\_ConfigureWatchdog()

### $\label{pmicConfigureWatchdog.} Pmic\_ConfigureWatchdog.$

#### Parameters

in	DeviceId.	
in	Watch dog Setting Id.	

### Returns

 $Std\_ReturnType.$ 

# 6.1.6.11 Pmic\_TriggerWatchdog()

### Pmic\_TriggerWatchdog.

### Parameters

in	DeviceId.	

#### Returns

void.

### 6.1.6.12 Pmic\_DisableWatchdog()

Pmic\_DisableWatchdog.

Parameters

in	DeviceId.	
----	-----------	--

Returns

Std\_ReturnType.

### 6.1.6.13 Pmic\_ReleaseFs0b()

PMIC executes the release safety FS0B pin.

This function is used to release the safety FS0B pin. The API will not release the FS0B pin and return the  $E_{\leftarrow}$  NOT\_OK if the PMIC device is not in the ASSERT\_FS0B state. This API will report the E\_NOT\_OK if the Pmic\_Init and Pmic\_InitDevice APIs were not called successfully before. This function has powerful in case PMIC reacted to assert the FS0B pin and is stuck in the ASSERT\_FS0B state. If users want PMIC to release FS0B and switch to the NORMAL\_FS state.

#### Parameters

in	$Device \leftarrow$	The ID of device.
	Id	

Returns

 ${\rm E\_OK:}$  Release FS0B pin successfully  ${\rm E\_NOT\_OK:}$  Release FS0B pin unsuccessfully

### 6.1.6.14 Pmic\_GotoInitFS()

 $Pmic\_GotoInitFS.$ 

 ${\bf Parameters}$ 

in	Device Id.	
----	------------	--

Returns

 $Std\_ReturnType.$ 

# $6.1.6.15 \quad Pmic\_GetRawFaultEvents()$

 $\label{pmic_GetRawFaultEvents} Pmic\_GetRawFaultEvents.$ 

Parameters

in	DeviceId.	
out	pRawFaultEventsOut.	

Returns

 $Std\_ReturnType.$ 

### 6.1.6.16 Pmic\_SetReactions()

 ${\bf Pmic\_SetReactions}.$ 

Parameters

in	DeviceId.	
in	Reaction Setting Id.	

#### Returns

Std\_ReturnType.

### 6.1.6.17 Pmic\_GetDeviceInfo()

 $\operatorname{Pmic}_{\operatorname{GetDeviceInfo}}$ .

### Parameters

in	DeviceId.	
in	pDeviceInfoOut.	

#### Returns

 $Std\_ReturnType.$ 

## 6.1.6.18 Pmic\_GetVersionInfo()

 ${\bf Pmic\_GetVersionInfo}.$ 

Parameters

```
in pVersionInfoOut.
```

Returns

void.

# 6.1.6.19 Pmic\_Dem\_Check\_Device()

API checks status and report the device run time error.

The function will report when users cannot access the device, time out by hardware checking, the wrong hardware behavior, clock setting failure, safety pin cannot release.

#### Parameters

in $eSt$	atusCode   The status	of device need to	report runtime.
----------	-----------------------	-------------------	-----------------

### 6.1.6.20 Pmic\_HLDChecksEntry()

```
Std_ReturnType Pmic_HLDChecksEntry (

const Pmic_ApiServiceIdType ePmicServiceID )
```

API checks the Pmic\_Init executed successfully before.

The API will report the det error if Pmic\_Init did not execute successfully before.

#### Parameters

in $ePmicServiceID$	The ID of PMIC API service.
---------------------	-----------------------------

#### Returns

 ${\rm E\_OK:}$  Check is successful  ${\rm E\_NOT\_OK:}$  Check is unsuccessful

### 6.1.6.21 Pmic\_HLDChecksExit()

API checks the Pmic driver status in Pmic\_Init API.

#### Parameters

ſ	in	eRetStatus	the status of process before entrance this function. This will use to set the driver status.	
	in	ePmicServiceID	The ID of PMIC API service.	

### 6.1.6.22 Pmic\_HLDDeviceChecksEntry()

API checks the PMIC device already initialized before call another API.

The API will report the det error if u32DeviceId is out of range. The det error also reports if PMIC device uninitialized.

#### Parameters

in	u32 Device Id	The ID of PMIC device
in	ePmicServiceID	The ID of PMIC API service.

#### Returns

E\_OK: Check is successful E\_NOT\_OK: Check is unsuccessful

### 6.1.6.23 Pmic\_HLDDeviceChecksExit()

API checks the Pmic driver status when user executes the Pmic\_InitDevice, Pmic\_EmulateDeviceOTP API.

#### Parameters

in	eRetStatus	the status of process before entrance this function.
in	u32 Device Id	The ID of PMIC device
in	ePmicServiceID	The ID of PMIC API service.

### 6.1.6.24 Pmic\_Check\_Init()

API checks the Pmic\_Init parameter input valid.

#### Parameters

in $pConfigPtr$	The pointer driver configuration.
-----------------	-----------------------------------

### Returns

E\_OK: Check is successful E\_NOT\_OK: Check is unsuccessful

## 6.1.6.25 Pmic\_Check\_ReadRegister()

API checks the Pmic\_ReadRegister parameter input valid.

#### Parameters

in	u32 Device Id	The ID of PMIC device
in	u8RegAddr	The PMIC register address
in	pu16 Value Out	The pointer stores the reading value.

### Returns

E\_OK: Check is successful E\_NOT\_OK: Check is unsuccessful

### 6.1.6.26 Pmic\_Check\_WriteRegister()

API checks the Pmic\_WriteRegister parameter input valid.

#### Parameters

in	<i>u32</i> ←	The ID of PMIC device
	DeviceId	
in	u8RegAddr	The PMIC register address

#### Returns

E\_OK: Check is successful E\_NOT\_OK: Check is unsuccessful

### 6.1.6.27 Pmic\_Check\_SetMode()

API checks the Pmic\_Setmode parameter input valid.

### Parameters

	in	u32 Device Id	The ID of PMIC device
ĺ	in	$u32Mode \leftarrow$	The mode setting index
		SettingId	

#### Returns

E\_OK: Check is successful E\_NOT\_OK: Check is unsuccessful

### 6.1.6.28 Pmic\_Check\_InitClock()

API checks the Pmic\_InitClock parameter input valid.

### Parameters

in	u32 Device Id	The ID of PMIC device
in	$u32Clock \leftarrow$	The clock setting index
	SettingId	

#### Returns

 ${\rm E\_OK:}$  Check is successful  ${\rm E\_NOT\_OK:}$  Check is unsuccessful

### 6.1.6.29 Pmic\_Check\_SetAnalogMux()

API checks the Pmic\_SetAnalogMux parameter input valid.

#### Parameters

in	u32DeviceId	The ID of PMIC device
in	u32Amux⊷	The amux setting index
	Channel Id	

#### Returns

E\_OK: Check is successful E\_NOT\_OK: Check is unsuccessful

### 6.1.6.30 Pmic\_Check\_SwitchSVS()

API checks the  $\operatorname{Pmic}_{-}\operatorname{SwitchSVS}$  parameter input valid.

### Parameters

in	u32 Device Id	The ID of PMIC device	
in	u32 Svs Setting ID	The SVS setting index	

#### Returns

E\_OK: Check is successful E\_NOT\_OK: Check is unsuccessful

### 6.1.6.31 Pmic\_Check\_ConfigureWatchdog()

API checks the Pmic\_ConfigureWatchdog parameter input valid.

### Parameters

in	u32DeviceId	The ID of PMIC device
in	$u32Watchdog \leftarrow$	The watchdog setting index
	SettingId	

### Returns

E\_OK: Check is successful E\_NOT\_OK: Check is unsuccessful

### 6.1.6.32 Pmic\_Check\_TriggerWatchdog()

API checks the  $\operatorname{Pmic}$ \_TriggerWatchdog parameter input valid.

#### Parameters

in	<i>u32</i> ←	The ID of PMIC device
	DeviceId	

### Returns

E\_OK: Check is successful E\_NOT\_OK: Check is unsuccessful

### 6.1.6.33 Pmic\_Check\_GotoInitFS()

API checks the Pmic\_GotoInitFS parameter input valid.

### Parameters

in	<i>u32</i> ←	The ID of PMIC device
	DeviceId	

#### Returns

<code>E\_OK:</code> Check is successful <code>E\_NOT\_OK:</code> Check is unsuccessful

### 6.1.6.34 Pmic\_Check\_GetRawFaultEvents()

API checks the  $Pmic\_GetRawFaultEvents$  parameter input valid.

#### Parameters

in	pRawFaultEventsOut	The pointer stores the fault error counter.	
----	--------------------	---	--

### Returns

 ${\rm E\_OK:}$  Check is successful  ${\rm E\_NOT\_OK:}$  Check is unsuccessful

### 6.1.6.35 Pmic\_Check\_SetReactions()

API checks the Pmic\_SetReactions parameter input valid.

### Parameters

in	u32DeviceId	The ID of PMIC device
in	$u32Reaction \leftarrow$	The reaction setting index
	SettingId	

## Returns

<code>E\_OK:</code> Check is successful <code>E\_NOT\_OK:</code> Check is unsuccessful

### 6.1.6.36 Pmic\_Check\_GetDeviceInfo()

API checks the Pmic\_GetDeviceInfo parameter input valid.

#### Parameters

in	pDeviceInfoOut	The pointer gets the device information.
----	----------------	--

#### Returns

<code>E\_OK:</code> Check is successful <code>E\_NOT\_OK:</code> Check is unsuccessful

### 6.1.6.37 Pmic\_Check\_GetVersionInfo()

API checks the  $\operatorname{Pmic\_GetVersionInfo}$  parameter input valid.

#### Parameters

1	in	n Version Info	The pointer gets the driver version information.
	T11	p versioninjo	The pointer gets the driver version information.

### Returns

<code>E\_OK:</code> Check is successful <code>E\_NOT\_OK:</code> Check is unsuccessful

### 6.1.6.38 Pmic\_Det\_Check\_ReportErrors()

API checks status and report the run time error.

### Parameters

in	eStatusCode	The status of driver
in	eServiceId	The API service id

Returns

E\_OK: Check is successful E\_NOT\_OK: Check is unsuccessful

# 6.1.7 Variable Documentation

# $6.1.7.1 \quad Pmic\_abTestMode$

boolean Pmic\_abTestMode[PMIC\_MAX\_DEVICECONFIGS] [extern]

Array used to indicate whether the indexed device is in test mode.

#### 6.1.7.2 Pmic\_abErrorDetected

boolean Pmic\_abErrorDetected[PMIC\_MAX\_DEVICECONFIGS] [extern]

Array used to indicate whether the indexed device encountered an error.

### 6.1.7.3 Pmic\_abGateWdgTrigger

boolean Pmic\_abGateWdgTrigger[PMIC\_MAX\_DEVICECONFIGS] [extern]

Array used to indicate watchdog trigger will be forwarded to the device.

### 6.1.7.4 Pmic\_abIsWdgTrigger

boolean Pmic\_abIsWdgTrigger[PMIC\_MAX\_DEVICECONFIGS] [extern]

Array used to check watchdog trigger in progress or not. When Wdg\_trigger is in-progress, variable will set true.

# 6.2 Pmic Ipw driver

## 6.2.1 Detailed Description

### **Data Structures**

- struct Pmic\_Ipw\_ModeConfigType

  The structure contains the mode configuration type. More...
- struct Pmic\_Ipw\_ClockConfigType

The structure contains the clock configuration type. More...

 $\bullet \ \ struct \ Pmic\_Ipw\_ReactionConfigType$ 

The structure contains the reaction configuration type. More...

• struct Pmic\_Ipw\_HwDeviceConfigType

The structure contains the hardware configuration type. More...

### 6.2.2 Data Structure Documentation

### 6.2.2.1 struct Pmic\_Ipw\_ModeConfigType

The structure contains the mode configuration type.

Definition at line 115 of file Pmic\_Ipw\_Types.h.

### 6.2.2.2 struct Pmic\_Ipw\_ClockConfigType

The structure contains the clock configuration type.

Definition at line 125 of file Pmic\_Ipw\_Types.h.

#### 6.2.2.3 struct Pmic\_Ipw\_ReactionConfigType

The structure contains the reaction configuration type.

Definition at line 135 of file Pmic Ipw Types.h.

### 6.2.2.4 struct Pmic\_Ipw\_HwDeviceConfigType

The structure contains the hardware configuration type.

Definition at line 178 of file Pmic Ipw Types.h.

# 6.3 Pmic VR5510 driver

### 6.3.1 Detailed Description

### **Data Structures**

 $\bullet \ \ struct \ Pmic\_VR55XX\_ModeConfigType$ 

The structure contains the mode configuration type for VR55XX. More...

• struct Pmic\_VR55XX\_ClockConfigType

The structure contains the clock configuration type for VR55XX. More...

• struct Pmic\_VR55XX\_ReactionConfigType

The structure contains the reaction configuration type for VR55XX. More...

struct Pmic\_VR55XX\_AmuxChannelConfigType

The structure contains the AMUX channel configuration type for VR55XX. More...

• struct Pmic\_VR55XX\_SVSConfigType

The structure contains the SVS setting configuration type for VR55XX. More...

• struct Pmic\_VR55XX\_WatchdogConfigType

The structure contains the watchdog configuration type for VR55XX. More...

 $\bullet \ \ struct \ Pmic\_VR55XX\_DeviceInfoType$ 

The structure contains the device information type for VR55XX. More...

• struct Pmic\_VR55XX\_RawFaultType

The structure contains the raw fault events statuses for VR55XX. More...

#### Enum Reference

• enum Pmic VR55XX PowerModeType

Power Modes Encoding for VR55XX.

#### **Function Reference**

• Pmic\_ReturnType Pmic\_VR55XX\_I2C\_ReadRegister (const Pmic\_DeviceIndexType u32DeviceId, const Pmic\_InterfaceDstType eDestination, const uint8 u8RegAddr, uint16 \*pu16ValueOut)

 $Pmic\_VR55XX\_I2C\_ReadRegister.$ 

• Pmic\_ReturnType Pmic\_VR55XX\_I2C\_WriteRegister (const Pmic\_DeviceIndexType u32DeviceId, const Pmic\_InterfaceDstType eDestination, const uint8 u8RegAddr, const uint16 u16WriteValue)

Pmic VR55XX I2C WriteRegister.

- Pmic\_ReturnType Pmic\_VR55XX\_InitDevice (const Pmic\_DeviceIndexType u32DeviceId) Pmic\_VR55XX\_InitDevice.
- Pmic\_ReturnType Pmic\_VR55XX\_EmulateDeviceOTP (const Pmic\_DeviceIndexType u32DeviceId) Pmic\_VR55XX\_EmulateDeviceOTP.
- Pmic\_ReturnType Pmic\_VR55XX\_InitClock (const Pmic\_DeviceIndexType u32DeviceId, const Pmic\_  $\leftarrow$  ClockSettingIndexType u32ClockSettingID)

 $Pmic\_VR55XX\_InitClock.$ 

• Pmic\_ReturnType Pmic\_VR55XX\_SetMode (const Pmic\_DeviceIndexType u32DeviceId, const Pmic\_  $\hookleftarrow$  ModeIndexType u32ModeSettingID)

```
Pmic VR55XX SetMode.
```

• Pmic\_ReturnType Pmic\_VR55XX\_SetAnalogMux (const Pmic\_DeviceIndexType u32DeviceId, const Pmic\_AmuxChannelIndexType u32AmuxChannelID)

```
Pmic\_VR55XX\_SetAnalogMux.
```

• Pmic\_ReturnType Pmic\_VR55XX\_SwitchSVS (const Pmic\_DeviceIndexType u32DeviceId, const Pmic\_← SvsSettingIndexType u32SvsSettingID)

```
Pmic\_VR55XX\_SwitchSVS.
```

• Pmic\_ReturnType Pmic\_VR55XX\_ConfigureWatchdog (const Pmic\_DeviceIndexType u32DeviceId, const Pmic WatchdogSettingIndexType u32WatchdogSettingID)

```
Pmic\_VR55XX\_Configure Watchdog.
```

 $\bullet \ \ Pmic\_ReturnType \ \underline{Pmic\_VR55XX\_TriggerWatchdog} \ (const \ Pmic\_DeviceIndexType \ u32DeviceId)$ 

```
Pmic\_VR55XX\_TriggerWatchdog.
```

 $\bullet \ \ Pmic\_ReturnType \ Pmic\_VR55XX\_DisableWatchdog \ (const \ Pmic\_DeviceIndexType \ u32DeviceId)$ 

```
Pmic\_VR55XX\_Disable Watchdog.
```

- Pmic\_ReturnType Pmic\_VR55XX\_ReleaseFs0b (const Pmic\_DeviceIndexType u32DeviceId)

```
Pmic\_VR55XX\_ReleaseFs0b.
```

 Pmic\_ReturnType Pmic\_VR55XX\_GetRawFaultEvents (const Pmic\_DeviceIndexType u32DeviceId, Pmic\_VR55XX\_RawFaultType \*pRawFaultEventsOut\_VR55XX)

```
Pmic\_VR55XX\_GetRawFaultEvents.
```

• Pmic\_ReturnType Pmic\_VR55XX\_SetReactions (const Pmic\_DeviceIndexType u32DeviceId, const Pmic← ReactionSettingIndexType u32ReactionSettingID)

```
Pmic VR55XX SetReactions.
```

\*pDeviceInfoOut)

• Pmic\_ReturnType Pmic\_VR55XX\_GetDeviceInfo (const Pmic\_DeviceIndexType u32DeviceId, Pmic\_VR55XX\_DeviceInfo (const Pmic\_DeviceInfo (const Pmic\_DeviceIn

```
Pmic\_VR55XX\_GetDeviceInfo.
```

• Pmic ReturnType Pmic VR55XX GotoInitFS (const Pmic DeviceIndexType u32DeviceId)

```
Pmic\_VR55XX\_GotoInitFS.
```

### 6.3.2 Data Structure Documentation

### 6.3.2.1 struct Pmic\_VR55XX\_ModeConfigType

The structure contains the mode configuration type for VR55XX.

Definition at line 168 of file Pmic VR55XX Types.h.

#### 6.3.2.2 struct Pmic\_VR55XX\_ClockConfigType

The structure contains the clock configuration type for VR55XX.

Definition at line 185 of file Pmic VR55XX Types.h.

#### 6.3.2.3 struct Pmic\_VR55XX\_ReactionConfigType

The structure contains the reaction configuration type for VR55XX.

Definition at line 198 of file Pmic\_VR55XX\_Types.h.

# $6.3.2.4 \quad struct \ Pmic\_VR55XX\_AmuxChannelConfigType$

The structure contains the AMUX channel configuration type for VR55XX.

Definition at line 215 of file Pmic\_VR55XX\_Types.h.

## 6.3.2.5 struct Pmic\_VR55XX\_SVSConfigType

The structure contains the SVS setting configuration type for VR55XX.

Definition at line 227 of file  $Pmic\_VR55XX\_Types.h.$ 

#### $6.3.2.6 \quad struct \ Pmic\_VR55XX\_WatchdogConfigType$

The structure contains the watchdog configuration type for VR55XX.

Definition at line 238 of file Pmic\_VR55XX\_Types.h.

#### 6.3.2.7 struct Pmic\_VR55XX\_DeviceInfoType

The structure contains the device information type for VR55XX.

Definition at line 250 of file Pmic VR55XX Types.h.

#### 6.3.2.8 struct Pmic\_VR55XX\_RawFaultType

The structure contains the raw fault events statuses for VR55XX.

Definition at line 260 of file Pmic\_VR55XX\_Types.h.

# 6.3.3 Enum Reference

#### 6.3.3.1 Pmic\_VR55XX\_PowerModeType

enum Pmic\_VR55XX\_PowerModeType

Power Modes Encoding for VR55XX.

#### Enumerator

PMIC_NORMAL_MODE	Normal Mode.
PMIC_RESET_MODE	Reset Mode.
PMIC_SHUTDOWN_MODE	Shutdown Mode.
PMIC_STANDBY_MODE	Standby Mode.
PMIC_DEEPSLEEP_MODE	Deep Sleep Mode.

Definition at line 155 of file Pmic\_VR55XX\_Types.h.

## 6.3.4 Function Reference

## 6.3.4.1 Pmic\_VR55XX\_I2C\_ReadRegister()

 $\label{lem:pmic_VR55XX_I2C_ReadRegister} Pmic\_VR55XX\_I2C\_ReadRegister.$ 

#### Parameters

in	u32 Device Id.	
in	eDestination.	
in	u8RegAddr.	
in	pu16 Value Out.	

Returns

Pmic\_ReturnType.

#### 6.3.4.2 Pmic\_VR55XX\_I2C\_WriteRegister()

 $\label{lem:pmic_VR55XX_I2C_WriteRegister} Pmic\_VR55XX\_I2C\_WriteRegister.$ 

#### Parameters

in	u32 Device Id.	
in	eDestination.	
in	u8RegAddr.	
in	u16 Write Value.	

#### Returns

Pmic\_ReturnType.

# $6.3.4.3 \quad Pmic\_VR55XX\_InitDevice()$

 $Pmic\_VR55XX\_InitDevice.$ 

 ${\bf Parameters}$ 

in $u32DeviceId.$	
-------------------	--

# Returns

 ${\bf Pmic\_ReturnType}.$ 

# $\bf 6.3.4.4 \quad Pmic\_VR55XX\_EmulateDeviceOTP()$

 $\label{pmic_VR55XX} Pmic\_VR55XX\_EmulateDeviceOTP.$ 

Parameters

in	u32 Device Id.	

Returns

Pmic\_ReturnType.

# 6.3.4.5 Pmic\_VR55XX\_InitClock()

#### $Pmic\_VR55XX\_InitClock.$

#### Parameters

in	u32 Device Id.	
in	Clock Setting ID.	

#### Returns

Pmic\_ReturnType.

# 6.3.4.6 Pmic\_VR55XX\_SetMode()

#### $Pmic\_VR55XX\_SetMode.$

#### Parameters

in	u32 Device Id.	
in	u32 Mode Setting ID.	

#### Returns

 $Pmic\_ReturnType.$ 

## 6.3.4.7 Pmic\_VR55XX\_SetAnalogMux()

 $\label{pmic_VR55XX_SetAnalogMux} Pmic\_VR55XX\_SetAnalogMux.$ 

#### Parameters

in	u32 Device Id.	
in	u32 Amux Channel ID.	

#### Returns

 $Pmic\_ReturnType.$ 

## 6.3.4.8 Pmic\_VR55XX\_SwitchSVS()

```
Pmic_ReturnType Pmic_VR55XX_SwitchSVS (  {\tt const\ Pmic\_DeviceIndexType}\ u32DeviceId, \\ {\tt const\ Pmic\_SvsSettingIndexType}\ u32SvsSettingID\ )
```

#### $Pmic_VR55XX_SwitchSVS.$

#### Parameters

in	u32 Device Id.	
in	u32 Svs Setting ID.	

#### Returns

Pmic\_ReturnType.

## 6.3.4.9 Pmic\_VR55XX\_ConfigureWatchdog()

### Pmic\_VR55XX\_ConfigureWatchdog.

in	u32 Device Id.	
in	u32 Watch dog Setting ID.	

#### Returns

 $Pmic\_ReturnType.$ 

## 6.3.4.10 Pmic\_VR55XX\_TriggerWatchdog()

Pmic\_VR55XX\_TriggerWatchdog.

Parameters

in u32DeviceId.

#### Returns

 ${\bf Pmic\_ReturnType}.$ 

## 6.3.4.11 Pmic\_VR55XX\_DisableWatchdog()

 ${\it Pmic\_VR55XX\_DisableWatchdog}.$ 

Parameters

in u32DeviceId.

Returns

Pmic\_ReturnType.

## 6.3.4.12 Pmic\_VR55XX\_ReleaseFs0b()

 $Pmic_VR55XX_ReleaseFs0b.$ 

#### Parameters

#### Returns

 $Pmic\_ReturnType.$ 

## 6.3.4.13 Pmic\_VR55XX\_GetRawFaultEvents()

 $\label{pmic_VR55XX_GetRawFaultEvents} Pmic\_VR55XX\_GetRawFaultEvents.$ 

#### Parameters

in	u32 Device Id.	
in	$pRawFaultEventsOut\_VR55XX.$	

## Returns

Pmic\_ReturnType.

# 6.3.4.14 Pmic\_VR55XX\_SetReactions()

 ${\rm Pmic\_VR55XX\_SetReactions}.$ 

in	u32 Device Id.	
in	u32 Reaction Setting ID.	

#### Returns

 ${\bf Pmic\_ReturnType}.$ 

## 6.3.4.15 Pmic\_VR55XX\_GetDeviceInfo()

 ${\rm Pmic\_VR55XX\_GetDeviceInfo}.$ 

#### Parameters

in	u32 Device Id.	
in	pDeviceInfoOut.	

#### Returns

 ${\bf Pmic\_ReturnType}.$ 

# 6.3.4.16 Pmic\_VR55XX\_GotoInitFS()

 $Pmic\_VR55XX\_GotoInitFS.$ 

Parameters

```
in u32DeviceId.
```

#### Returns

 $Pmic\_ReturnType.$ 

# 6.4 I2c\_external\_access

# 6.4.1 Detailed Description

#### **Function Reference**

• Std\_ReturnType Pmic\_VR55XX\_I2cTransferExternal (const Pmic\_VR55XX\_I2cSetupType \*pI2cSetup← TypePtr, uint8 \*pTxBufferPtr, uint8 \*pRxBufferPtr)

I2c transfer.

## 6.4.2 Function Reference

## 6.4.2.1 Pmic\_VR55XX\_I2cTransferExternal()

I2c transfer.

This function transfers data via I2C.

in	I2cSetupTypePtr	pointer setup I2c interface
in	TxBufferPtr	I2C Tx buffer
	[in/out]	RxBufferPtr I2C Rx buffer

# 6.5 Ocotp\_external\_access

# 6.5.1 Detailed Description

#### **Function Reference**

• Std\_ReturnType Pmic\_VR55XX\_Ocotp\_ReadShadowRegister (const uint32 u32OcotpInstance, const uint32 u32OcotpIndex, uint32 \*u32Data)

Ocotp read shadow register.

## 6.5.2 Function Reference

## 6.5.2.1 Pmic\_VR55XX\_Ocotp\_ReadShadowRegister()

Ocotp read shadow register.

This function transfers data via OCOTP.

in	u32OcotpInstance	OCOTP instance
in	u32OcotpIndex	OCOTP register index
out	u32Data	OCOTP raw register data.

# 6.6 Pin external access

# 6.6.1 Detailed Description

#### **Function Reference**

• void Pmic\_VR55XX\_Port\_SetPinMode (const uint8 u8Siul2Instance, const uint32 u32Pin, const uint8 u8← Mode)

```
Pmic\_VR55XX\_Port\_SetPinMode\ sets\ Pin\ operation\ mode.
```

• void Pmic\_VR55XX\_Dio\_FlipChannel (const uint8 u8Siul2Instance, const uint16 u16ChannelId)

Pmic\_VR55XX\_Dio\_FlipChannel inverts the level of a pin.

#### 6.6.2 Function Reference

## 6.6.2.1 Pmic\_VR55XX\_Port\_SetPinMode()

Pmic VR55XX Port SetPinMode sets Pin operation mode.

This function controls the pin mode.

#### Parameters

in	u8 Siul 2 Instance	Instance SIUL (non-AUTOSAR) (not use with AUTOSAR)
in	u32Pin	Pin number (non-AUTOSAR) / Pin index setting (AUTOSAR)
in	u8Mode	Pin operation mode

# $6.6.2.2 \quad Pmic\_VR55XX\_Dio\_FlipChannel()$

Pmic\_VR55XX\_Dio\_FlipChannel inverts the level of a pin.

This function control the signal of pin

in	u8 Siul 2 Instance	Instance SIUL (non-AUTOSAR) (not use with AUTOSAR)
in	u16 Channel Id	channel number (non-AUTOSAR) / channel index setting (AUTOSAR)

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