User Manual

for S32 MCU Driver

Document Number: UM11MCUASR4.4 Rev0000R4.0.0 Rev. 1.0

Chapter 1

Revision History

Revision	Date	Author	Description
1.0	31.10.2022	NXP RTD Team	Prepared for release S32 RTD AUTOSAR 4.4 Version 4.0.0 Release

Chapter 2

Introduction

This User Manual describes NXP Semiconductors' AUTOSAR Mcu Driver for S32.

AUTOSAR Mcu Driver configuration parameters description can be found in the Tresos Configuration Plugin section. Deviations from the specification are described in the Deviations from Requirements section.

AUTOSAR Mcu driver requirements and APIs are described in the Mcu Driver Software Specification Document (version 4.4.0).

2.1 Supported Derivatives

The software described in this document is intended to be used with the following microcontroller devices of NXP Semiconductors:

- s32g274a_bga525
- s32g254a_bga525
- s32g233a_bga525
- s32g234m_bga525
- s32g378a_bga525
- s32g379a_bga525
- s32g398a_bga525
- s32g399a_bga525

- s32g338m_bga525
- s32g339m_bga525
- s32g358a_bga525
- s32g359a_bga525
- s32r45_bga780

All of the above microcontroller devices are collectively named as S32.

2.2 Overview

AUTOSAR (AUTomotive Open System ARchitecture) is an industry partnership working to establish standards for software interfaces and software modules for automobile electronic control systems.

AUTOSAR:

- paves the way for innovative electronic systems that further improve performance, safety and environmental friendliness.
- is a strong global partnership that creates one common standard: "Cooperate on standards, compete on implementation".
- is a key enabling technology to manage the growing electrics/electronics complexity. It aims to be prepared for the upcoming technologies and to improve cost-efficiency without making any compromise with respect to quality.
- facilitates the exchange and update of software and hardware over the service life of the vehicle.

2.3 About This Manual

This Technical Reference employs the following typographical conventions:

- **Boldface** style: Used for important terms, notes and warnings.
- *Italic* style: Used for code snippets in the text. Note that C language modifiers such "const" or "volatile" are sometimes omitted to improve readability of the presented code.

Notes and warnings are shown as below:

Note

This is a note.

Warning

This is a warning

2.4 Acronyms and Definitions

Term	Definition
API	Application Programming Interface
ASM	Assembler
BSMI	Basic Software Make file Interface
CAN	Controller Area Network
C/CPP	C and C++ Source Code
CS	Chip Select
CTU	Cross Trigger Unit
DEM	Diagnostic Event Manager
DET	Development Error Tracer
DMA	Direct Memory Access
ECU	Electronic Control Unit
FIFO	First In First Out
LSB	Least Signifigant Bit
MCU	Micro Controller Unit
MIDE	Multi Integrated Development Environment
MSB	Most Significant Bit
N/A	Not Applicable
RAM	Random Access Memory
SIU	Systems Integration Unit
SWS	Software Specification
VLE	Variable Length Encoding
XML	Extensible Markup Language

2.5 Reference List

#	Title	Version
1	Specification of Mcu Driver	AUTOSAR Release 4.4.0
2	S32G2 Reference Manual	Rev 5, May 2022
3	S32G3 Reference Manual	Rev.2 Draft C, June 2022
4	S32R45 Reference Manual	Rev. 3, 12/2021
5	S32G2 Errata Document	Mask Set Errata for Mask 0P77B, Rev. 2.4
6	S32G3 Errata Document	Mask Set Errata for Mask 0P72B, Rev. 1.1
7	S32R45 Errata Document	Mask Set Errata for Mask P57D, Rev. 2.0
8	S32G2 Data Sheet	Rev 5, May 2022
9	S32G3 Data Sheet	Rev 2, Draft B, June 2022
10	VR5510 Data Sheet	Rev 5, April 2022
11	S32R45 Data Sheet	Rev. 2 — 12/2021

Chapter 3

Driver

3.1 Requirements

Requirements for this driver are detailed in the AUTOSAR CP 4.4.0 Mcu Driver Software Specification document (See Table Reference List)

3.2 Driver Design Summary

The Mcu Driver controls the CLOCK, POWER and RAM modules of the S32 device. It provides the following features:

- Configuration and initialization of the CLOCK.
- Configuration and initialization of the POWER.
- Configuration and initialization of the RAM.

3.3 Hardware Resources

The Mcu Driver consists of:

1. Clock IPs (MC_CGM,FXOSC,SIRC,FIRC,CMU,DFS,PLLDIG,SRAMC)
2. Power IPs (MC_ME,PMC,MC_RGM)
3. Ram IPs (STCU2)

3.4 Deviations from Requirements

The driver deviates from the AUTOSAR MCU Driver software specification in some places. The table below identifies the AUTOSAR requirements that are not implemented or out of scope for the MCU Driver.

Term	Definition
N/S	Out of scope
N/I	Not implemented
N/F	Not fully implemented

Below table identifies the AUTOSAR requirements that are not fully implemented, implemented differently or out of scope for the MCU driver.

Requirement	Status	Description	Notes
SWS_Mcu_00053	N/S	If clock failure notification is enabled in the configuration set and a clock source failure error occurs, the error code MCU_↩ E_CLOCK_FAILURE shall be reported. (See also SWS_↩ Mcu_00051).	DEMs cannot be reported in ISR contexts. For the clock failure case the error MCU_E↩ _ISR_CLOCK_FAILURE was defined and if the error notification is configured by the application the CMU interrupt will report it.
SWS_Mcu_00257	N/S	Fail criteria for MCU_E_↩ CLOCK_FAILURE: a clock source failure occurs	For the clock failure case the error MCU_E_ISR_CLOCK_↩ FAILURE was defined and if the error notification is configured by the application the CMU interrupt will report it.
SWS_Mcu_00258	N/S	Pass criteria for MCU_E_↩ CLOCK_FAILURE: no clock source failure occurs	For the clock failure case the error MCU_E_ISR_CLOCK_↩ FAILURE was defined and if the error notification is configured by the application the CMU interrupt will report it.
SWS_Mcu_00245	N/S	If the register can affect several hardware modules and if it is not an I/O register, it shall be initialised by this MCU driver.	There is a separate plug-in that will cover shared ip's

Requirement	Status	Description	Notes
SWS_Mcu_00056	N/S	The function Mcu_Distribute↩ PllClock shall return without affecting the MCU hardware if the PLL clock has been automatically activated by the MCU hardware.	The function Mcu_Distribute↩ PllClock will change the Mcu hardware. The clock switching to PLL is not completed by Mcu_InitClock
SWS_Mcu_00259	N/S	: DRAFT: The MCU Driver module shall reject configurations with partition mappings which are not supported by the implementation.	Based on ticket AAI-462, this requirement is not applicable.
SWS_Mcu_CONSTR_00001	N/S	: DRAFT: The module will operate as an independent instance in each of the partitions, means the called API will only target the partition it is called in.	Based on ticket AAI-462, this requirement is not applicable.
CPR_RTD_00544.mcu	N/F	Driver shall support Autosar standard configuration format for the IP layer Note: EPD file for the IP shall be provided.	The Clock IP can't support this requirement.

3.5 Driver Limitations

The Mcu driver has the following limitations:

- The return value of Clock_Ip_GetClockFrequency() function is the frequency without the Gate.
- The CMU_FC_27 and CMU_FC_28 are monitoring A53_CORE_CLK and are accessible only by A53 core.
- The reset structure of partitions results in better device availability. If a fault is detected in a software reset domain, that domain can be reset separately without impacting the operation of the rest of the chip. (See the workaround in the sup-chapter "How to initialize partitions if a fault is detected in a software reset domain")

For S32R45 only:

- The CMU_FC_38 is monitoring ACCEL_3_CLK.
- The CMU_FC_39 is monitoring ACCEL_4_CLK (LAX_0).
- The CMU_FC_40 is monitoring ACCEL_4_CLK (LAX_1).
- And they are not accessible from the M7 core.
- Clock PERIPH_DFS3 in S32CT must be operating from 52MHz to 208MHz.

For S32G274A_Rev1 only:

- QuadSPI: DDR 200MHz and DDR 166MHz modes are not supported.

- uSDHC: DDR-HS400 is not supported.

For S32G3XX only: Selectors of PFE_MAC0_TX_CLK, PFE_MAC1_TX_CLK, PFE_MAC2_TX_CLK can not be configured individually.

- If PFEMAC0_TX_DIV_CLK is selected, GENCTRL1[CTRL0]/GENCTRL1[CTRL1]/GENCTRL1[CTRL2] registers are set to 0 (corresponding to PFE_MAC_0_TX_DIV_CLK, PFE_MAC_1_TX_DIV_CLK, PFE_MAC_2_TX_DIV_CLK are selected).

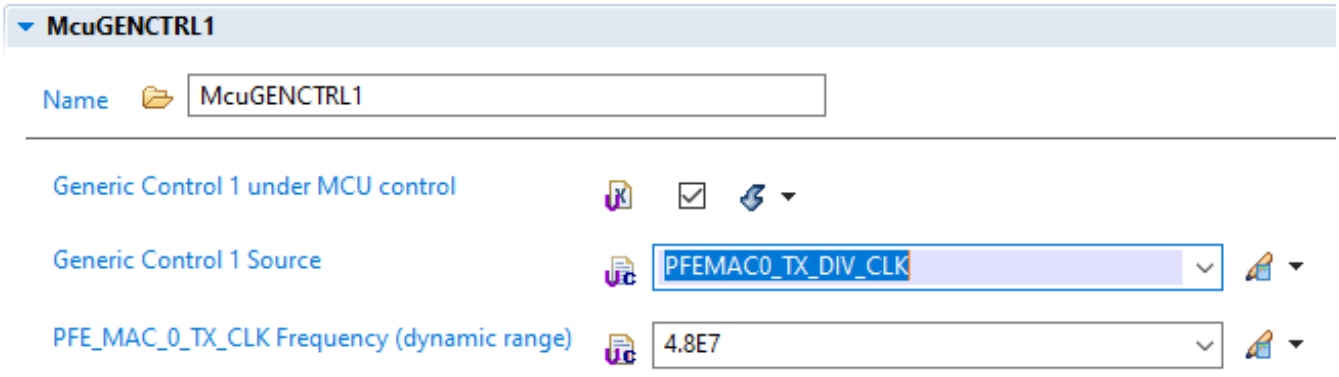

Figure 3.1 Tresos Plugin snapshot for McuGENCTRL1_PFEMAC0_TX_DIV_CLK form

- If SERDES_1_XPCS_0_TX is selected, GENCTRL1[CTRL0]/GENCTRL1[CTRL1]/GENCTRL1[CTRL2] registers are set to 1 (corresponding to SERDES_1_XPCS_0_TX_CLK, SERDES_1_XPCS_1_TX_CLK, SERDES_0_XPCS_1_TX_CLK are selected).

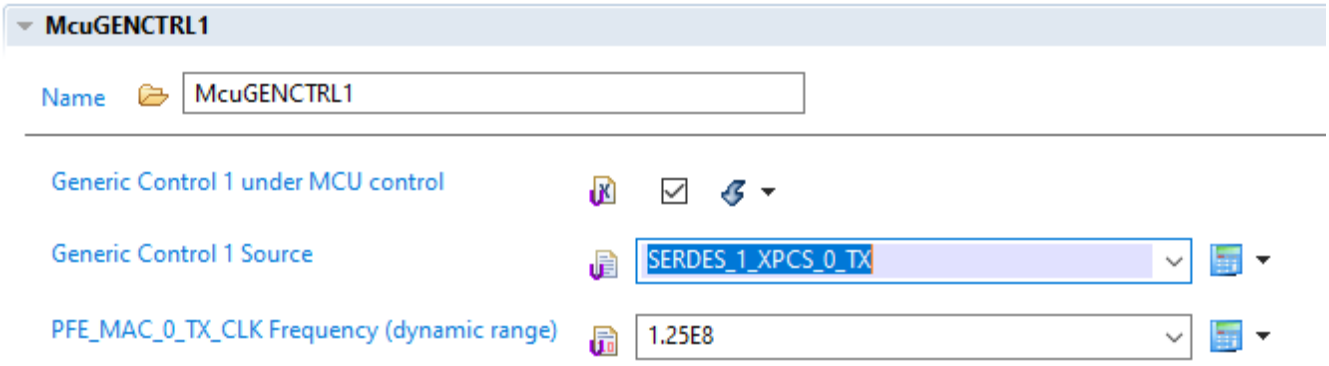

Figure 3.2 Tresos Plugin snapshot for McuGENCTRL1_SERDES_1_XPCS_0_TX form

Limitations of clock configuration on S32CT:

- Remove Mcu component from Peripheral tool and try to “Update code”, Clock IPL can work unexpectedly: the number of clock configuration be generated can be less than the number one you have in Clock tool. When a new project is created and only IPL is used (Mcu component was not added in Peripheral tool), everything is working fine.

  The workaround: Go to location of project and delete file ClockConfigurationMappings.txt then restart S32DS. After that everything will work as normal.

- When Functional Group from Peripherals Tool is updated by removing/renaming an existing entry(variant), a switching to Clock perspective is needed.

- When a project with a Functional Group different from “BOARD_InitPeripherals” is imported, a switching to Clock perspective is needed.

3.6 Driver usage and configuration tips

3.6.1 MCU Clock Management

- For bypassing the configuration of a clock source during Mcu_InitClock, the "[source] under MCU control" checkbox should be unchecked. This will generate smaller configurations that will be updated faster and more efficiently. In addition, if the application is configuring some clocks in advance, the UnderMcuControl should be unchecked so the MCU driver does not overwrite the initial settings.

- When the clock tree is initialized before the MCU driver is used. e.g The bootloader or user code initializes the clock tree. After that the control is passed to AUTOSAR software, the MCU is used to configured the ECU and clock again. The following sequence is required to successfully and safely re-configure the clock tree.

- System clock frequency selected must adhere to the same clock divider ratios shown in Clocking use case examples of Reference Manual.

1. Mcu_Init
2. Mcu_InitClock (to reinitialize the clock tree)
3. If the PLL is used as a clock source, call Mcu_GetPllStatus until it returns MCU_PLL_LOCKED and call Mcu_DistributePllClock.
4. Mcu_SetMode (to gate the peripheral clocks)

3.6.2 How to initialize FCCU module if using CMU interrupt over FCCU:

- The perform recover a software-recoverable non-critical fault: clear FCCU interrupt flag (FCCU_NCF_S_↩ NCFS28) to avoid hang on ISR function.

- Initialize interrupt FCCU: function handler, id, priority (corresponding to Mcu_Cmu_ClockFail_IRQHandler, FCCU_ALARM_IRQn, 7).

- Initialize FCCU module: Configure the non-critical fault channels.

- In user notification function, FCCU interrupt flag must be cleared to avoid hang on while loop interrupt (FCCU_NCF_S_NCFS28).

- Call functions of Mcu module to enable CMU interrupt.

3.6.3 MCU Mode Management

- For bypassing the configuration of a Partition, COFB set, or Core during Mcu_SetMode, the corresponding "[Block] Under MCU Control" checkbox should be unchecked. This will generate smaller configurations that will be updated faster and more efficiently. In addition, if the application is configuring a certain mode in advance, the UnderMcuControl should be unchecked so the MCU driver does not overwrite the initial settings.

- The clock sources that aren't used can be disabled in different run-modes to reduce power consumption.

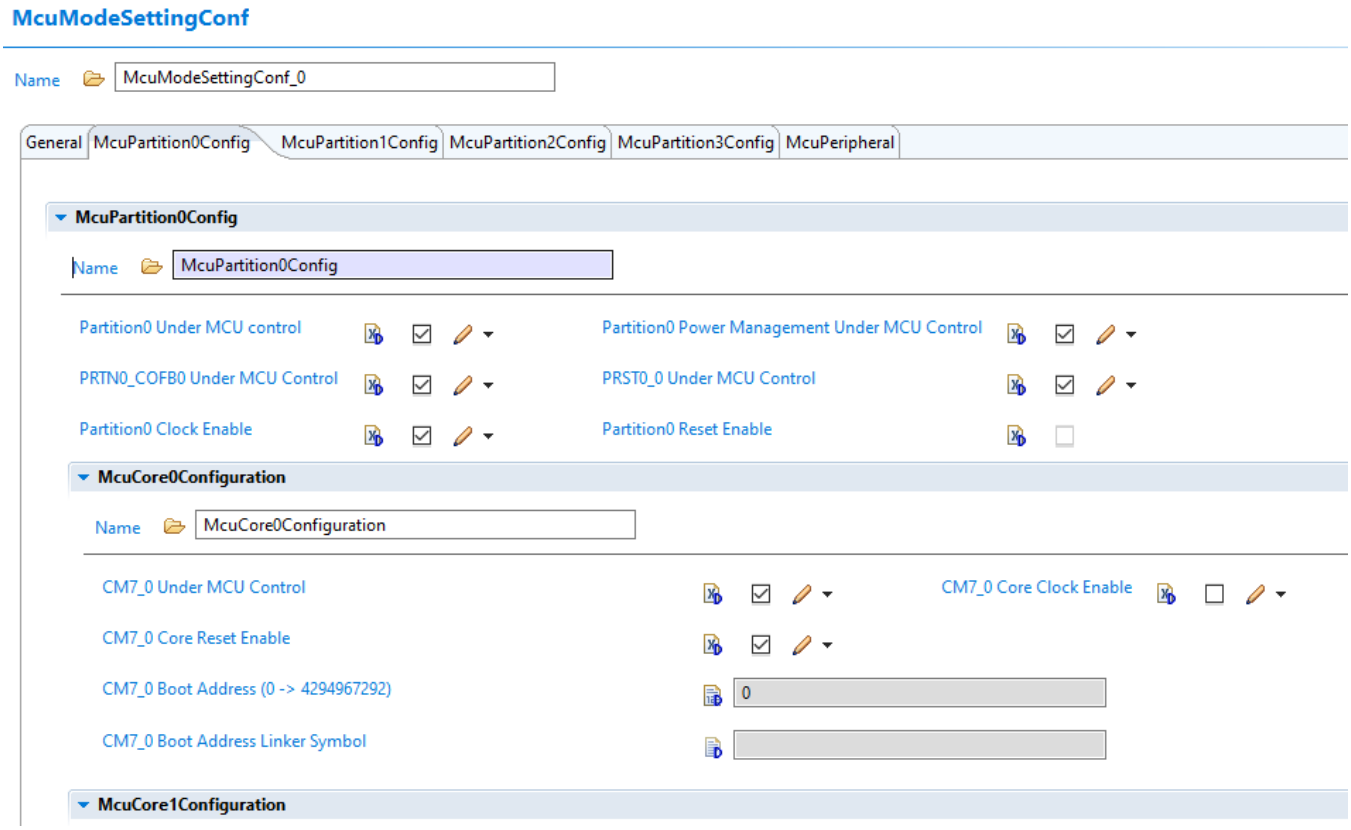

Figure 3.3 Tresos Plugin snapshot for McuPartition0Config form

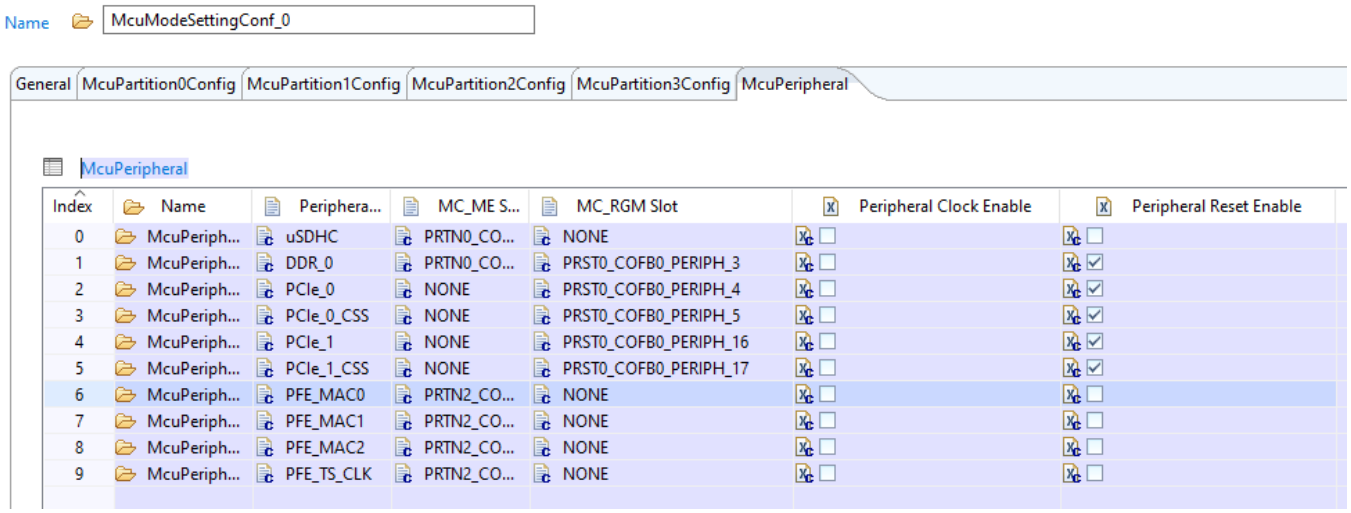

Figure 3.4 Tresos Plugin snapshot for McuPeripheral form

3.6.4 How to initialize partitions if a fault is detected in a software reset domain

If a fault is detected (FCCU NCF 48 - MTR Repair Error) in a software reset domain, that domain can be reset separately without impacting the operation of the rest of the chip. Call Mcu_SetMode() two times: Mcu_Set↩ Mode(McuModeSettingConf_0); /∗ partition 0,2 and 3

3.7 Runtime errors

The driver generates the following DET errors at runtime.

Table 3.3 Default Errors (reported by DET)

Function	Error Code	Condition triggering the error
Mcu_Init	MCU_E_INIT_FAILED	Invalid configuration pointer.
Mcu_InitClock	MCU_E_PARAM_CLOCK	Invalid input parameter.
Mcu_SetMode	MCU_E_PARAM_MODE	Invalid input parameter.
Mcu_InitRamSection	MCU_E_PARAM_↩ RAMSECTION	Invalid input parameter or invalid memory configuration.
Mcu_DistributePllClock	MCU_E_PLL_NOT_LOCKED	One of the used PLL's failed to achieve lock
All functions, except Mcu_Init and Mcu_GetVersionInfo	MCU_E_UNINIT	The driver is in an uninitialized state.
Mcu_GetMidrStructure	MCU_E_PARAM_POINTER	Invalid input parameter.
Mcu_GetVersionInfo	MCU_E_PARAM_POINTER	Invalid input parameter.
Mcu_Init	MCU_E_ALREADY_↩ INITIALIZED	The driver is already initialized.

Function	Error Code	Condition triggering the error
Mcu_DisableCmu	MCU_E_CMU_INDEX_OUT↩ _OF_RANGE	Invalid input parameter.

The driver generates the following DEM errors at runtime.

Table 3.5 Default Errors (reported by DEM)

Function	Error Code	Condition triggering the error
Mcu_GetResetReason	Mcu_E_TimeoutFailure	Reset flags could not be cleared.
Mcu_GetResetRawValue	Mcu_E_TimeoutFailure	Reset flags could not be cleared.
Mcu_SetMode	Mcu_E_TimeoutFailure	The MC_ME or LPU mode transition failed.
Mcu_Init	Mcu_E_TimeoutFailure	The MC_ME mode transition failed.
Mcu_InitClock	Mcu_E_TimeoutFailure	The MC_ME mode transition failed.
Mcu_DisableCmu	Mcu_E_TimeoutFailure	Disable CMU failed.
Mcu_GetRamState	Mcu_E_TimeoutFailure	Get RAM state failed.

3.8 Symbolic Names Disclaimer

All containers having symbolicNameValue set to TRUE in the AUTOSAR schema will generate defines like:

#define <Mip>Conf_<Container_ShortName>_<Container_ID>

For this reason it is forbidden to duplicate the names of such containers across the RTD configurations or to use names that may trigger other compile issues (e.g. match existing `#ifdefs` arguments).

Chapter 4

Tresos Configuration Plug-in

This chapter describes the Tresos configuration plug-in for the driver. All the parameters are described below.

- Module Mcu
  - Container McuGeneralConfiguration
    - Parameter McuDevErrorDetect
    - Parameter McuVersionInfoApi
    - Parameter McuGetRamStateApi
    - Parameter McuInitClock
    - Parameter McuNoPll
    - Parameter McuEnterLowPowerMode
    - Parameter McuTimeout
    - Parameter McuEnableUserModeSupport
    - Parameter McuPerformResetApi
    - Parameter McuCalloutBeforePerformReset
    - Parameter McuPerformResetCallout
    - Parameter McuCmuNotification
    - Parameter McuAlternateResetIsrUsed
    - Parameter McuCmuErrorIsrUsed
    - Parameter McuErrorIsrNotification
    - Parameter McuDisableRgmInit
    - Parameter McuDisablePmcInit
    - Parameter McuDisableRamWaitStatesConfig
    - Parameter McuPrepareMemoryConfig
    - Parameter McuTimeoutMethod
    - Parameter McuHardwareVersion
    - Parameter A53CoreFlavour
    - Reference McuEcucPartitionRef
    - Container McuControlledClocksConfiguration
      - Parameter McuFxoscUnderMcuControl
      - Parameter McuPll0UnderMcuControl
      - Parameter McuPll1UnderMcuControl
      - Parameter McuPll2UnderMcuControl

        - Parameter McuPll3UnderMcuControl
        - Parameter McuDfs0UnderMcuControl
        - Parameter McuDfs1UnderMcuControl
- Container McuDebugConfiguration
    - Parameter McuDisableDemReportErrorStatus
    - Parameter McuGetSystemStateApi
    - Parameter McuGetPowerModeStateApi
    - Parameter McuGetPowerDomainApi
    - Parameter McuSscmGetMemConfigApi
    - Parameter McuSscmGetStatusApi
    - Parameter McuSscmGetUoptApi
    - Parameter McuGetMidrStructureApi
    - Parameter McuDisableCmuApi
    - Parameter McuEmiosConfigureGprenApi
    - Parameter McuGetClockFrequencyApi
- Container McuCoreControlConfiguration
    - Parameter McuCoreBootAddressControl
- Container McuPublishedInformation
    - Container McuResetReasonConf
        - Parameter McuResetReason
- Container CommonPublishedInformation
    - Parameter ArReleaseMajorVersion
    - Parameter ArReleaseMinorVersion
    - Parameter ArReleaseRevisionVersion
    - Parameter ModuleId
    - Parameter SwMajorVersion
    - Parameter SwMinorVersion
    - Parameter SwPatchVersion
    - Parameter VendorApiInfix
    - Parameter VendorId
- Container McuModuleConfiguration
    - Parameter McuNumberOfMcuModes
    - Parameter McuRamSectors
    - Parameter McuResetSetting
    - Parameter McuCrystalFrequencyHz
    - Parameter McuExternalPAD_RTC_EXT_REF_CLK_FrequencyHz
    - Parameter McuExternalPAD_FTM_0_EXT_REF_CLK_FrequencyHz
    - Parameter McuExternalPAD_FTM_1_EXT_REF_CLK_FrequencyHz
    - Parameter McuExternalPAD_GMAC_EXT_TS_CLK_FrequencyHz
    - Parameter McuExternalPAD_GMAC_0_EXT_TX_CLK_FrequencyHz
    - Parameter McuExternalPAD_GMAC_0_EXT_RX_CLK_FrequencyHz
    - Parameter McuExternalPAD_GMAC_0_EXT_REF_CLK_FrequencyHz
    - Parameter McuExternalPAD_GMAC_1_EXT_TX_CLK_FrequencyHz
    - Parameter McuExternalPAD_GMAC_1_EXT_RX_CLK_FrequencyHz
    - Parameter McuExternalPAD_GMAC_1_EXT_REF_CLK_FrequencyHz

* Parameter McuExternalPAD_PFE_MAC_0_EXT_TX_CLK_FrequencyHz
* Parameter McuExternalPAD_PFE_MAC_0_EXT_RX_CLK_FrequencyHz
* Parameter McuExternalPAD_PFE_MAC_0_EXT_REF_CLK_FrequencyHz
* Parameter McuExternalPAD_PFE_MAC_1_EXT_TX_CLK_FrequencyHz
* Parameter McuExternalPAD_PFE_MAC_1_EXT_RX_CLK_FrequencyHz
* Parameter McuExternalPAD_PFE_MAC_1_EXT_REF_CLK_FrequencyHz
* Parameter McuExternalPAD_PFE_MAC_2_EXT_TX_CLK_FrequencyHz
* Parameter McuExternalPAD_PFE_MAC_2_EXT_RX_CLK_FrequencyHz
* Parameter McuExternalPAD_PFE_MAC_2_EXT_REF_CLK_FrequencyHz
* Parameter McuInternalPAD_SERDES_0_LANE_0_TX_FrequencyHz
* Parameter McuInternalPAD_SERDES_0_LANE_0_CDR_FrequencyHz
* Parameter McuInternalPAD_SERDES_0_LANE_1_TX_FrequencyHz
* Parameter McuInternalPAD_SERDES_0_LANE_1_CDR_FrequencyHz
* Parameter McuInternalPAD_SERDES_1_LANE_0_TX_FrequencyHz
* Parameter McuInternalPAD_SERDES_1_LANE_0_CDR_FrequencyHz
* Parameter McuInternalPAD_SERDES_1_LANE_1_TX_FrequencyHz
* Parameter McuInternalPAD_SERDES_1_LANE_1_CDR_FrequencyHz
* Parameter McuInternalPAD_SERDES_0_XPCS_0_TX_FrequencyHz
* Parameter McuInternalPAD_SERDES_0_XPCS_0_CDR_FrequencyHz
* Parameter McuInternalPAD_SERDES_0_XPCS_1_TX_FrequencyHz
* Parameter McuInternalPAD_SERDES_0_XPCS_1_CDR_FrequencyHz
* Parameter McuInternalPAD_SERDES_1_XPCS_0_TX_FrequencyHz
* Parameter McuInternalPAD_SERDES_1_XPCS_0_CDR_FrequencyHz
* Parameter McuInternalPAD_SERDES_1_XPCS_1_TX_FrequencyHz
* Parameter McuInternalPAD_SERDES_1_XPCS_1_CDR_FrequencyHz
* Parameter McuClockSrcFailureNotification
* Container McuClockSettingConfig
  - Parameter McuClockSettingId
  - Container McuFXOSC
  - Parameter McuFxoscUnderMcuControl
  - Parameter McuFxoscPowerDownCtr
  - Parameter McuFxoscByPass
  - Parameter McuFxoscMainComparator
  - Parameter McuFxoscCounter
  - Parameter McuFxoscOverdriveProtection
  - Parameter McuFXOSC_Frequency
  - Container McuCgm0SettingConfig
  - Parameter McuPCSStepDuration
  - Parameter McuPCSSwitchDuration
  - Container McuCgm0PcsConfig
  - Parameter McuClockPcfsUnderMcuControl
  - Parameter McuPCS_Name
  - Parameter McuPCS_SourceFrequency
  - Parameter McuPCS_MaxAllowableDynamicIDD
  - Container McuCgm0ClockMux0
  - Parameter McuClockMuxUnderMcuControl
  - Parameter McuClkMux0_Source

- Parameter McuClockMux0_Frequency
- Parameter McuClkMux0Div0_En
- Parameter McuClkMux0Div0_Divisor
- Parameter McuClockMux0Divider0_Frequency
- Parameter McuClkMux0Div1_En
- Parameter McuClkMux0Div1_Divisor
- Parameter McuClockMux0Divider1_Frequency
- Container McuCgm0ClockMux1
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux1_Source
- Parameter McuClkMux1Div0_En
- Parameter McuClkMux1Div0_Divisor
- Parameter McuClockMux1Divider0_Frequency
- Container McuCgm0ClockMux2
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux2_Source
- Parameter McuClkMux2Div0_En
- Parameter McuClkMux2Div0_Divisor
- Parameter McuClockMux2Divider0_Frequency
- Container McuCgm0ClockMux3
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux3_Source
- Parameter McuClkMux3Div0_En
- Parameter McuClkMux3Div0_Divisor
- Parameter McuClockMux3Divider0_Frequency
- Container McuCgm0ClockMux4
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux4_Source
- Parameter McuClkMux4Div0_En
- Parameter McuClkMux4Div0_Divisor
- Parameter McuClockMux4Divider0_Frequency
- Container McuCgm0ClockMux5
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux5_Source
- Parameter McuClkMux5Div0_En
- Parameter McuClkMux5Div0_Divisor
- Parameter McuClockMux5Divider0_Frequency
- Container McuCgm0ClockMux6
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux6_Source
- Parameter McuClkMux6Div0_En
- Parameter McuClkMux6Div0_Divisor
- Parameter McuClockMux6Divider0_Frequency
- Container McuCgm0ClockMux7
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux7_Source
- Parameter McuClockMux7_Frequency

- Container McuCgm0ClockMux8
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux8_Source
- Parameter McuClockMux8_Frequency
- Container McuCgm0ClockMux9
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux9_Source
- Parameter McuClkMux9Div0_En
- Parameter McuClkMux9Div0_Divisor
- Parameter McuClockMux9Divider0_Frequency
- Container McuCgm0ClockMux10
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux10_Source
- Parameter McuClkMux10Div0_En
- Parameter McuClkMux10Div0_Divisor
- Parameter McuClockMux10Divider0_Frequency
- Container McuCgm0ClockMux11
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux11_Source
- Parameter McuClockMux11_Frequency
- Container McuCgm0ClockMux12
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux12_Source
- Parameter McuClkMux12Div0_En
- Parameter McuClkMux12Div0_Divisor
- Parameter McuClockMux12Divider0_Frequency
- Container McuCgm0ClockMux14
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux14_Source
- Parameter McuClkMux14Div0_En
- Parameter McuClkMux14Div0_Divisor
- Parameter McuClockMux14Divider0_Frequency
- Container McuCgm0ClockMux15
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux15_Source
- Parameter McuClockMux15_Frequency
- Parameter McuClkMux15Div0_En
- Parameter McuClkMux15Div0_Divisor
- Parameter McuClockMux15Divider0_Frequency
- Container McuCgm0ClockMux16
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux16_Source
- Parameter McuClockMux16_Frequency
- Container McuCgm1SettingConfig
- Parameter McuPCSStepDuration
- Parameter McuPCSSwitchDuration
- Container McuCgm1PcsConfig

- Parameter McuClockPcfsUnderMcuControl
- Parameter McuPCS_Name
- Parameter McuPCS_SourceFrequency
- Parameter McuPCS_MaxAllowableDynamicIDD
- Container McuCgm1ClockMux0
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux0_Source
- Parameter McuClockMux0_Frequency
- Container McuCgm2SettingConfig
- Parameter McuPCSStepDuration
- Parameter McuPCSSwitchDuration
- Container McuCgm2PcsConfig
- Parameter McuClockPcfsUnderMcuControl
- Parameter McuPCS_Name
- Parameter McuPCS_SourceFrequency
- Parameter McuPCS_MaxAllowableDynamicIDD
- Container McuCgm2ClockMux0
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux0_Source
- Parameter McuClockMux0_Frequency
- Parameter McuClkMux0Div0_En
- Parameter McuClkMux0Div0_Divisor
- Parameter McuClockMux0Divider0_Frequency
- Container McuCgm2ClockMux1
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux1_Source
- Parameter McuClockMux1_Frequency
- Parameter McuClkMux1Div0_En
- Parameter McuClkMux1Div0_Divisor
- Parameter McuClockMux1Divider0_Frequency
- Container McuGENCTRL1_EMAC0
- Parameter McuClockMuxUnderMcuControl
- Parameter McuGENCTRL1_EMAC0_Source
- Parameter McuGENCTRL1_EMAC0_Frequency
- Container McuGENCTRL1_EMAC1
- Parameter McuClockMuxUnderMcuControl
- Parameter McuGENCTRL1_EMAC1_Source
- Parameter McuGENCTRL1_EMAC1_Frequency
- Container McuGENCTRL1_EMAC2
- Parameter McuClockMuxUnderMcuControl
- Parameter McuGENCTRL1_EMAC2_Source
- Parameter McuGENCTRL1_EMAC2_Frequency
- Container McuCgm2ClockMux2
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux2_Source
- Parameter McuClkMux2Div0_En
- Parameter McuClkMux2Div0_Divisor

- Parameter McuClockMux2Divider0_Frequency
- Container McuCgm2ClockMux3
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux3_Source
- Parameter McuClockMux3_Frequency
- Parameter McuClkMux3Div0_En
- Parameter McuClkMux3Div0_Divisor
- Parameter McuClockMux3Divider0_Frequency
- Container McuCgm2ClockMux4
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux4_Source
- Parameter McuClockMux4_Frequency
- Parameter McuClkMux4Div0_En
- Parameter McuClkMux4Div0_Divisor
- Parameter McuClockMux4Divider0_Frequency
- Container McuCgm2ClockMux5
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux5_Source
- Parameter McuClockMux5_Frequency
- Container McuCgm2ClockMux6
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux6_Source
- Parameter McuClockMux6_Frequency
- Container McuCgm2ClockMux7
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux7_Source
- Parameter McuClockMux7_Frequency
- Parameter McuClkMux7Div0_En
- Parameter McuClkMux7Div0_Divisor
- Parameter McuClockMux7Divider0_Frequency
- Container McuCgm2ClockMux8
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux8_Source
- Parameter McuClockMux8_Frequency
- Parameter McuClkMux8Div0_En
- Parameter McuClkMux8Div0_Divisor
- Parameter McuClockMux8Divider0_Frequency
- Container McuCgm2ClockMux9
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux9_Source
- Parameter McuClockMux9_Frequency
- Parameter McuClkMux9Div0_En
- Parameter McuClkMux9Div0_Divisor
- Parameter McuClockMux9Divider0_Frequency
- Container McuCgm5SettingConfig
- Container McuCgm5ClockMux0
- Parameter McuClockMuxUnderMcuControl

- Parameter McuClkMux0_Source
- Parameter McuClockMux0_Frequency
- Container McuCgm6SettingConfig
- Container McuCgm6ClockMux0
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux0_Source
- Parameter McuClkMux0Div0_En
- Parameter McuClkMux0Div0_Divisor
- Parameter McuClockMux0Divider0_Frequency
- Container McuCgm6ClockMux1
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux1_Source
- Parameter McuClkMux1Div0_En
- Parameter McuClkMux1Div0_Divisor
- Parameter McuClockMux1Divider0_Frequency
- Container McuCgm6ClockMux2
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux2_Source
- Parameter McuClockMux2_Frequency
- Container McuCgm6ClockMux3
- Parameter McuClockMuxUnderMcuControl
- Parameter McuClkMux3_Source
- Parameter McuClockMux3_Frequency
- Parameter McuClkMux3Div0_En
- Parameter McuClkMux3Div0_Divisor
- Parameter McuClockMux3Divider0_Frequency
- Container McuRtcClockSelect
- Parameter McuClockMuxUnderMcuControl
- Parameter McuRtc_Source
- Parameter McuRtc_Frequency
- Container McuPll_0
- Parameter McuPLLUnderMcuControl
- Parameter McuPLLEnabled
- Parameter McuPllClockSelection
- Container McuPll_Configuration
- Parameter McuPllDvRdiv
- Parameter McuPllDvMfi
- Parameter McuPllFmSscgbyp
- Parameter McuPllFmSpreadctl
- Parameter McuPllFmStepSize
- Parameter McuPllFmStepNo
- Parameter McuPllFdFmod
- Parameter McuPllFdMdp
- Parameter McuPllFdEmdp
- Parameter McuPllFdMfn
- Parameter McuPllFdSdmen
- Parameter McuPllOdiv0_En

- Parameter McuPllOdiv0_Div
- Parameter McuPllOdiv1_En
- Parameter McuPllOdiv1_Div
- Container McuPll_Parameter
- Parameter PLL_PHI0_Frequency
- Parameter PLL_PHI1_Frequency
- Parameter PLL_VCO_Frequency
- Container McuCoreDfs
- Container McuDfs_1
- Parameter McuDFSUnderMcuControl
- Parameter McuDFSPort_En
- Parameter McuDFSPortMfi
- Parameter McuDFSPortMfn
- Parameter DFS_CLK_Frequency
- Container McuDfs_2
- Parameter McuDFSUnderMcuControl
- Parameter McuDFSPort_En
- Parameter McuDFSPortMfi
- Parameter McuDFSPortMfn
- Parameter DFS_CLK_Frequency
- Container McuDfs_3
- Parameter McuDFSUnderMcuControl
- Parameter McuDFSPort_En
- Parameter McuDFSPortMfi
- Parameter McuDFSPortMfn
- Parameter DFS_CLK_Frequency
- Container McuDfs_4
- Parameter McuDFSUnderMcuControl
- Parameter McuDFSPort_En
- Parameter McuDFSPortMfi
- Parameter McuDFSPortMfn
- Parameter DFS_CLK_Frequency
- Container McuDfs_5
- Parameter McuDFSUnderMcuControl
- Parameter McuDFSPort_En
- Parameter McuDFSPortMfi
- Parameter McuDFSPortMfn
- Parameter DFS_CLK_Frequency
- Container McuDfs_6
- Parameter McuDFSUnderMcuControl
- Parameter McuDFSPort_En
- Parameter McuDFSPortMfi
- Parameter McuDFSPortMfn
- Parameter DFS_CLK_Frequency
- Container McuPll_1
- Parameter McuPLLUnderMcuControl
- Parameter McuPLLEnabled

- Parameter McuPllClockSelection
- Container McuPll_Configuration
- Parameter McuPllDvRdiv
- Parameter McuPllDvMfi
- Parameter McuPllFdMfn
- Parameter McuPllFdSdmen
- Parameter McuPllOdiv0_En
- Parameter McuPllOdiv0_Div
- Parameter McuPllOdiv1_En
- Parameter McuPllOdiv1_Div
- Parameter McuPllOdiv2_En
- Parameter McuPllOdiv2_Div
- Parameter McuPllOdiv3_En
- Parameter McuPllOdiv3_Div
- Parameter McuPllOdiv4_En
- Parameter McuPllOdiv4_Div
- Parameter McuPllOdiv5_En
- Parameter McuPllOdiv5_Div
- Parameter McuPllOdiv6_En
- Parameter McuPllOdiv6_Div
- Parameter McuPllOdiv7_En
- Parameter McuPllOdiv7_Div
- Container McuPll_Parameter
- Parameter PLL_PHI0_Frequency
- Parameter PLL_PHI1_Frequency
- Parameter PLL_PHI2_Frequency
- Parameter PLL_PHI3_Frequency
- Parameter PLL_PHI4_Frequency
- Parameter PLL_PHI5_Frequency
- Parameter PLL_PHI6_Frequency
- Parameter PLL_PHI7_Frequency
- Parameter PLL_VCO_Frequency
- Container McuPeriphDfs
- Container McuDfs_1
- Parameter McuDFSUnderMcuControl
- Parameter McuDFSPort_En
- Parameter McuDFSPortMfi
- Parameter McuDFSPortMfn
- Parameter DFS_CLK_Frequency
- Container McuDfs_2
- Parameter McuDFSUnderMcuControl
- Parameter McuDFSPort_En
- Parameter McuDFSPortMfi
- Parameter McuDFSPortMfn
- Parameter DFS_CLK_Frequency
- Container McuDfs_3
- Parameter McuDFSUnderMcuControl

- Parameter McuDFSPort_En
- Parameter McuDFSPortMfi
- Parameter McuDFSPortMfn
- Parameter DFS_CLK_Frequency
- Container McuDfs_4
- Parameter McuDFSUnderMcuControl
- Parameter McuDFSPort_En
- Parameter McuDFSPortMfi
- Parameter McuDFSPortMfn
- Parameter DFS_CLK_Frequency
- Container McuDfs_5
- Parameter McuDFSUnderMcuControl
- Parameter McuDFSPort_En
- Parameter McuDFSPortMfi
- Parameter McuDFSPortMfn
- Parameter DFS_CLK_Frequency
- Container McuDfs_6
- Parameter McuDFSUnderMcuControl
- Parameter McuDFSPort_En
- Parameter McuDFSPortMfi
- Parameter McuDFSPortMfn
- Parameter DFS_CLK_Frequency
- Container McuPll_2
- Parameter McuPLLUnderMcuControl
- Parameter McuPLLEnabled
- Parameter McuPllClockSelection
- Container McuPll_Configuration
- Parameter McuPllDvRdiv
- Parameter McuPllDvMfi
- Parameter McuPllFmSscgbyp
- Parameter McuPllFmSpreadctl
- Parameter McuPllFmStepSize
- Parameter McuPllFmStepNo
- Parameter McuPllFdFmod
- Parameter McuPllFdMdp
- Parameter McuPllFdEmdp
- Parameter McuPllFdMfn
- Parameter McuPllFdSdmen
- Parameter McuPllOdiv0_En
- Parameter McuPllOdiv0_Div
- Parameter McuPllOdiv1_En
- Parameter McuPllOdiv1_Div
- Container McuPll_Parameter
- Parameter PLL_PHI0_Frequency
- Parameter PLL_PHI1_Frequency
- Parameter PLL_VCO_Frequency
- Container McuPll_3

- Parameter McuPLLUnderMcuControl
- Parameter McuPLLEnabled
- Parameter McuPllClockSelection
- Container McuPll_Configuration
- Parameter McuPllDvRdiv
- Parameter McuPllDvMfi
- Parameter McuPllFmSscgbyp
- Parameter McuPllFmSpreadctl
- Parameter McuPllFmStepSize
- Parameter McuPllFmStepNo
- Parameter McuPllFdFmod
- Parameter McuPllFdMdp
- Parameter McuPllFdEmdp
- Parameter McuPllFdMfn
- Parameter McuPllFdSdmen
- Parameter McuPllOdiv0_En
- Parameter McuPllOdiv0_Div
- Container McuPll_Parameter
- Parameter PLL_PHI0_Frequency
- Parameter PLL_VCO_Frequency
- Container McuClkMonitor
- Parameter McuClockMonitorUnderMcuControl
- Parameter McuClkMonitorEn
- Parameter McuCmuName
- Parameter McuAsyncFHHInterruptEn
- Parameter McuAsyncFLLInterruptEn
- Parameter McuSyncFHHInterruptEn
- Parameter McuSyncFLLInterruptEn
- Container McuClockReferencePoint
- Parameter McuClockReferencePointFrequency
- Parameter McuClockFrequencySelect

* Container McuDemEventParameterRefs
  - Reference MCU_E_TIMEOUT_FAILURE
  - Reference MCU_E_INVALIDFXOSC_CONFIG
  - Reference MCU_E_CLOCKMUXSWITCH_FAILURE
  - Reference MCU_E_CLOCK_FAILURE
* Container McuModeSettingConf
  - Parameter McuMode
  - Parameter McuPowerMode
  - Parameter McuMainCoreSelect
  - Parameter McuEnableSleepOnExit
  - Container McuPartitionConfiguration
  - Container McuPartition0Config
  - Parameter McuPartitionUnderMcuControl
  - Parameter McuPartitionPowerUnderMcuControl
  - Parameter McuPrtnCofb0UnderMcuControl
  - Parameter McuPrstCofb0UnderMcuControl

- Parameter McuPartitionClockEnable
- Parameter McuPartitionResetEnable
- Container McuCore0Configuration
- Parameter McuCoreUnderMcuControl
- Parameter McuCoreClockEnable
- Parameter McuCoreResetEnable
- Parameter McuCoreBootAddress
- Parameter McuCoreBootAddressLinkerSym
- Container McuCore1Configuration
- Parameter McuCoreUnderMcuControl
- Parameter McuCoreClockEnable
- Parameter McuCoreResetEnable
- Parameter McuCoreBootAddress
- Parameter McuCoreBootAddressLinkerSym
- Container McuCore2Configuration
- Parameter McuCoreUnderMcuControl
- Parameter McuCoreClockEnable
- Parameter McuCoreResetEnable
- Parameter McuCoreBootAddress
- Parameter McuCoreBootAddressLinkerSym
- Container McuCore4Configuration
- Parameter McuCoreUnderMcuControl
- Parameter McuCoreClockEnable
- Parameter McuCoreResetEnable
- Parameter McuCoreBootAddress
- Parameter McuCoreBootAddressLinkerSym
- Container McuPartition1Config
- Parameter McuPartitionUnderMcuControl
- Parameter McuPartitionPowerUnderMcuControl
- Parameter McuPrtnCofb0UnderMcuControl
- Parameter McuPrstCofb0UnderMcuControl
- Parameter McuPartitionClockEnable
- Parameter McuPartitionResetEnable
- Container McuCore0Configuration
- Parameter McuCoreUnderMcuControl
- Parameter McuCoreClockEnable
- Parameter McuCoreResetEnable
- Parameter McuCoreBootAddress
- Parameter McuCoreBootAddressLinkerSym
- Container McuCore1Configuration
- Parameter McuCoreUnderMcuControl
- Parameter McuCoreClockEnable
- Parameter McuCoreResetEnable
- Parameter McuCoreBootAddress
- Parameter McuCoreBootAddressLinkerSym
- Container McuCore2Configuration
- Parameter McuCoreUnderMcuControl

- Parameter McuCoreClockEnable
- Parameter McuCoreResetEnable
- Parameter McuCoreBootAddress
- Parameter McuCoreBootAddressLinkerSym
- Container McuCore3Configuration
- Parameter McuCoreUnderMcuControl
- Parameter McuCoreClockEnable
- Parameter McuCoreResetEnable
- Parameter McuCoreBootAddress
- Parameter McuCoreBootAddressLinkerSym
- Container McuCore4Configuration
- Parameter McuCoreUnderMcuControl
- Parameter McuCoreClockEnable
- Parameter McuCoreResetEnable
- Parameter McuCoreBootAddress
- Parameter McuCoreBootAddressLinkerSym
- Container McuCore5Configuration
- Parameter McuCoreUnderMcuControl
- Parameter McuCoreClockEnable
- Parameter McuCoreResetEnable
- Parameter McuCoreBootAddress
- Parameter McuCoreBootAddressLinkerSym
- Container McuCore6Configuration
- Parameter McuCoreUnderMcuControl
- Parameter McuCoreClockEnable
- Parameter McuCoreResetEnable
- Parameter McuCoreBootAddress
- Parameter McuCoreBootAddressLinkerSym
- Container McuCore7Configuration
- Parameter McuCoreUnderMcuControl
- Parameter McuCoreClockEnable
- Parameter McuCoreResetEnable
- Parameter McuCoreBootAddress
- Parameter McuCoreBootAddressLinkerSym
- Container McuPartition2Config
- Parameter McuPartitionUnderMcuControl
- Parameter McuPartitionPowerUnderMcuControl
- Parameter McuPrtnCofb0UnderMcuControl
- Parameter McuPrstCofb0UnderMcuControl
- Parameter McuPartitionClockEnable
- Parameter McuPartitionResetEnable
- Container McuPartition3Config
- Parameter McuPartitionUnderMcuControl
- Parameter McuPartitionPowerUnderMcuControl
- Parameter McuPrtnCofb0UnderMcuControl
- Parameter McuPrstCofb0UnderMcuControl
- Parameter McuPartitionClockEnable

- Parameter McuPartitionResetEnable
- Container McuPartition4Config
- Parameter McuPartitionUnderMcuControl
- Parameter McuPartitionPowerUnderMcuControl
- Parameter McuPartitionClockEnable
- Parameter McuPartitionResetEnable
- Container McuPartition5Config
- Parameter McuPartitionUnderMcuControl
- Parameter McuPartitionPowerUnderMcuControl
- Parameter McuPartitionClockEnable
- Parameter McuPartitionResetEnable
- Container McuPartition6Config
- Parameter McuPartitionUnderMcuControl
- Parameter McuPartitionPowerUnderMcuControl
- Parameter McuPartitionClockEnable
- Parameter McuPartitionResetEnable
- Container McuPartition7Config
- Parameter McuPartitionUnderMcuControl
- Parameter McuPartitionPowerUnderMcuControl
- Parameter McuPartitionClockEnable
- Parameter McuPartitionResetEnable
- Container McuPeripheral
- Parameter McuPeripheralName
- Parameter McuModeEntrySlot
- Parameter McuResetGenerationSlot
- Parameter McuPeripheralClockEnable
- Parameter McuPeripheralResetEnable

* Container McuRamSectorSettingConf
  - Parameter McuRamSectorId
  - Parameter McuRamDefaultValue
  - Parameter McuRamSectionBaseAddress
  - Parameter McuRamSectionSize
  - Parameter McuRamSectionWriteSize
  - Parameter McuRamSectionBaseAddrLinkerSym
  - Parameter McuRamSectionSizeLinkerSym
* Container McuResetConfig
  - Parameter McuResetType
  - Parameter McuFuncResetEscThreshold
  - Parameter McuDestResetEscThreshold
  - Container McuResetSourcesConfig
  - Container McuEXR_ResetSource
  - Parameter McuDisableReset
  - Container McuF_FR_31_ResetSource
  - Parameter McuDisableReset
* Container McuPowerControl
  - Container McuPMC_Config
  - Parameter McuVDD_FXOSCNonCriticalFlag

- Parameter McuVDD_ADC0NonCriticalFlag
- Parameter McuVDD_ADC1NonCriticalFlag
- Parameter McuVDD_TMUNonCriticalFlag
- Parameter McuVDD_EFUSENonCriticalFlag
- Parameter McuVDD_HV_PLLNonCriticalFlag
- Parameter McuVDD_LV_PLLNonCriticalFlag
- Parameter McuVDD_HV_PLL_DDR0NonCriticalFlag
- Parameter McuVDD_LV_PLL_DDR0NonCriticalFlag
- Parameter McuVDD_HV_PLL_AURNonCriticalFlag
- Parameter McuVDD_LV_PLL_AURNonCriticalFlag
- Parameter McuVDD_IO_STBYNonCriticalFlag
- Parameter McuVDD_IO_ANonCriticalFlag
- Parameter McuVDD_IO_BNonCriticalFlag
- Parameter McuVDD_IO_USBNonCriticalFlag
- Parameter McuVDD_HV_PLL_ACCNonCriticalFlag
- Parameter McuVDD_LV_PLL_ACCNonCriticalFlag
- Parameter McuVDD_IO_SDHCNonCriticalFlag
- Parameter McuVDD_IO_C_GPIO4NonCriticalFlag
- Parameter McuVDD_IO_B_GPIO3NonCriticalFlag
- Parameter McuVDD_IO_B_GPIO2NonCriticalFlag
- Parameter McuVDD_IO_A_GPIO1NonCriticalFlag
- Parameter McuVDD_IO_GMAC1NonCriticalFlag
- Parameter McuVDD_IO_GMAC0NonCriticalFlag
- Parameter McuVDD_IO_CLKOUTNonCriticalFlag
- Parameter McuVDD_IO_QSPINonCriticalFlag

4.1 Module Mcu

Configuration of the MicroController Unit (MCU) module.

Included containers:

- McuGeneralConfiguration
- McuDebugConfiguration
- McuCoreControlConfiguration
- McuPublishedInformation
- CommonPublishedInformation
- McuModuleConfiguration

Property	Value
type	ECUC-MODULE-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantSupport	true
supportedConfigVariants	VARIANT-POST-BUILD, VARIANT-PRE-COMPILE

4.2 Container McuGeneralConfiguration

This container contains the general configuration for the MCU driver.

Included subcontainers:

- McuControlledClocksConfiguration

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.3 Parameter McuDevErrorDetect

Pre-processor switch for enabling the default error detection and reporting to the DET.

The switch McuDevErrorDetect shall switch the Default Error Tracer (Det) detection and notification ON or OFF.

The detection of default errors is configurable (ON/OFF) at precompile time.

#define MCU_DEV_ERROR_DETECT (STD_ON)/(STD_OFF) will be generated in Mcu_Cfg.h file.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.4 Parameter McuVersionInfoApi

Pre-processor switch to enable/disable the API to read out the modules version information.

#define MCU_VERSION_INFO_API (STD_ON)/(STD_OFF) will be generated in Mcu_Cfg.h file.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.5 Parameter McuGetRamStateApi

Pre-processor switch to enable/disable the API Mcu_GetRamState.

#define MCU_GET_RAM_STATE_API (STD_ON)/(STD_OFF) will be generated in Mcu_Cfg.h file.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

4.6 Parameter McuInitClock

If this parameter is set to FALSE, the clock initialization has to be disabled from the MCU driver. This concept applies when there are some write once clock registers and a bootloader is present. If this parameter is set to TRUE, the MCU driver is responsible with the clock initialization.

#define MCU_INIT_CLOCK (STD_ON)/(STD_OFF) will be generated in Mcu_Cfg.h file.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	true

4.7 Parameter McuNoPll

This parameter shall be set True, if the H/W does not have a PLL or the PLL circuitry is enabled after the power on without S/W intervention. In this case MCU_DistributePllClock has to be disabled and MCU_GetPllStatus has to return MCU_PLL_STATUS_UNDEFINED. Otherwise this parameters has to be set False.

#define MCU_NO_PLL (STD_ON)/(STD_OFF) will be generated in Mcu_Cfg.h file.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

4.8 Parameter McuEnterLowPowerMode

If this parameter has been configured to 'TRUE', the function 'Mcu_SetMode()' shall not be impacted and behave as specified.

If this parameter has been configured to 'FALSE', the function 'Mcu_SetMode()' shall not perform the transition to any low power modes as are 'STOP' or 'HALT' or any other mode, where the core stops execution.

#define MCU_ENTER_LOW_POWER_MODE (STD_ON)/(STD_OFF) will be generated in Mcu_Cfg.h file.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

4.9 Parameter McuTimeout

This parameter represents the maximum number of loops for blocking functionality.

The maximum time needed for a MC_ME transition from DRUN to DRUN with keeping PLL running is 3 ms.

Please take this into consideration when choosing the value for this parameter.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	50000
max	4294967295
min	1

4.10 Parameter McuEnableUserModeSupport

When this parameter is enabled, the MDL module will adapt to run from User Mode, with the following measures:

a) configuring REG_PROT for ABC1, ABC2 IPs so that the registers under protection can be accessed from user mode by setting UAA bit in REG_PROT_GCR to 1

b) using 'call trusted function' stubs for all internal function calls that access registers requiring supervisor mode.

c) other module specific measures

for more information, please see chapter 5.7 User Mode Support in IM

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.11 Parameter McuPerformResetApi

Pre-processor switch to enable/disable the use the Mcu_PerformReset() API.

OFF - Mcu_PerformReset() API is not used.

ON - Mcu_PerformReset() API is used.

#define MCU_PERFORM_RESET_API (STD_ON)/(STD_OFF) will be generated in Mcu_Cfg.h file.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.12 Parameter McuCalloutBeforePerformReset

Check this if you want a callout function, called by MCU right before Mcu_PerformReset().

This parameter is available for configuration only if "McuPerformResetApi" is ON.

#define MCU_RESET_CALLOUT_USED (STD_ON)/(STD_OFF) will be generated in Mcu_Cfg.h file.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.13 Parameter McuPerformResetCallout

Function name of callout.

The field is editable only if "McuCalloutBeforePerformReset" is ON.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FUNCTION-NAME-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	NULL_PTR

4.14 Parameter McuCmuNotification

Function pointer to callback function.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FUNCTION-NAME-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	NULL_PTR

4.15 Parameter McuAlternateResetIsrUsed

Check this if you have any reset source demoted to IRQ (i.e. at least one McuModuleConfiguration/McuResetConfig/*/McuDisableReset = 'true').

#define POWER_IP_RESET_ALTERNATE_ISR_USED (STD_ON)/(STD_OFF) will be generated in Power_Ip_Cfg_Defines.h file.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.16 Parameter McuCmuErrorIsrUsed

Check this if clock source failure notifications are enabled (i.e. McuModuleConfiguration/McuClockSrcFailureNotification = 'ENABLED').

#define MCU_CMU_ERROR_ISR_USED (STD_ON)/(STD_OFF) will be generated in Mcu_Cfg.h file.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.17 Parameter McuErrorIsrNotification

Function name of callout. This function will be called by the error ISR.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FUNCTION-NAME-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	NULL_PTR

4.18 Parameter McuDisableRgmInit

If this parameter is set to TRUE, the Reset Generation Module (MC_RGM) initialization will be disabled in the MCU driver.

If this parameter is set to FALSE, the MCU driver is responsible for the Reset Generation Module (MC_RGM) initialization.

#define MCU_DISABLE_RGM_INIT (STD_ON)/(STD_OFF) will be generated in Mcu_Cfg.h file.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

4.19 Parameter McuDisablePmcInit

If this parameter is set to TRUE, the Power Management Controller (PMC) initialization will be disabled in the MCU driver.

If this parameter is set to FALSE, the MCU driver is responsible for the Power Management Controller (PMC) initialization.

#define MCU_DISABLE_PMC_INIT (STD_ON)/(STD_OFF) will be generated in Mcu_Cfg.h file.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

4.20 Parameter McuDisableRamWaitStatesConfig

Check this if you want the SRAMC configuration to be bypassed.

If this is checked, the settings configured in McuRam(from McuClockSettingConfig) will not be used.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.21 Parameter McuPrepareMemoryConfig

Function name of a callout that will be called before and after configuring

the SRAM controller. It will have a parameter that will specify if it is

the entry or the exit point of the controllers configuration.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FUNCTION-NAME-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	NULL_PTR

4.22 Parameter McuTimeoutMethod

McuTimeoutMethod

Configures the timeout method.

Based on this selection a certain timeout method from OsIf will be used in the driver.

Note: If OSIF_COUNTER_SYSTEM or OSIF_COUNTER_CUSTOM are selected make sure the corresponding timer is enabled in OsIf General configuration.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	OSIF_COUNTER_DUMMY
literals	['OSIF_COUNTER_DUMMY', 'OSIF_COUNTER_SYSTEM', 'OSIF_↩ COUNTER_CUSTOM']

4.23 Parameter McuHardwareVersion

McuHardwareVersion

Configures the hardware version.

For S32G274:

Cut 1.0: PS32G274ABVUC 0N92V SBAB 1937C

Cut 2.0: PS32G274ABVUC 0P77B SBAA 2030A

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	Rev2
literals	['Rev1', 'Rev2']

4.24 Parameter A53CoreFlavour

A53CoreFlavour

Configures the A53 CORE FLAVOUR.

1.0GHZ Core frequency

1.1GHZ Core frequency

1.3GHZ Core frequency

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	f1300MHz
literals	['f1000MHz', 'f1100MHz', 'f1300MHz']

4.25 Reference McuEcucPartitionRef

Maps the MCU driver to zero or multiple ECUC partitions to make the

modules API available in this partition.

Tags: atp.Status=draft

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-REFERENCE-DEF
origin	AUTOSAR_ECUC
lowerMultiplicity	0
upperMultiplicity	Infinite
postBuildVariantMultiplicity	true
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
requiresSymbolicNameValue	False
destination	/AUTOSAR/EcucDefs/EcuC/EcucPartitionCollection/EcucPartition

4.26 Container McuControlledClocksConfiguration

This container contains pre-compile options for all the clock sources under MCU control.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.27 Parameter McuFxoscUnderMcuControl

Check this if FXOSC is under MCU control in any of the Mcu Clock Setting Configurations

(i.e. at least one McuClockSettingConfig/*/McuFXOSC/McuFxoscUnderMcuControl = 'true').

#define MCU_FXOSC_UNDER_MCU_CONTROL (STD_ON)/(STD_OFF) will be generated in Mcu_Cfg.h file.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	true

4.28 Parameter McuPll0UnderMcuControl

Check this if CorePLL is under MCU control in any of the Mcu Clock Setting Configurations

(i.e. at least one McuClockSettingConfig/*/McuPll_0/McuPLLUnderMcuControl = 'true').

#define MCU_PLL0_UNDER_MCU_CONTROL (STD_ON)/(STD_OFF) will be generated in Mcu_Cfg.h file.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	true

4.29 Parameter McuPll1UnderMcuControl

Check this if PeriphPLL is under MCU control in any of the Mcu Clock Setting Configurations

(i.e. at least one McuClockSettingConfig/*/McuPll_1/McuPLLUnderMcuControl = 'true').

#define MCU_PLL1_UNDER_MCU_CONTROL (STD_ON)/(STD_OFF) will be generated in Mcu_Cfg.h file.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	true

4.30 Parameter McuPll2UnderMcuControl

Check this if PeriphPLL is under MCU control in any of the Mcu Clock Setting Configurations

(i.e. at least one McuClockSettingConfig/*/McuPll_2/McuPLLUnderMcuControl = 'true').

#define MCU_PLL2_UNDER_MCU_CONTROL (STD_ON)/(STD_OFF) will be generated in Mcu_Cfg.h file.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	true

4.31 Parameter McuPll3UnderMcuControl

Check this if PeriphPLL is under MCU control in any of the Mcu Clock Setting Configurations

(i.e. at least one McuClockSettingConfig/*/McuPll_3/McuPLLUnderMcuControl = 'true').

#define MCU_PLL3_UNDER_MCU_CONTROL (STD_ON)/(STD_OFF) will be generated in Mcu_Cfg.h file.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	true

4.32 Parameter McuDfs0UnderMcuControl

Check this if CoreDFS is under MCU control in any of the Mcu Clock Setting Configurations

(i.e. at least one McuClockSettingConfig/*/McuCoreDfs/McuDfs_x/McuDFSUnderMcuControl = 'true').

#define MCU_DFS0_UNDER_MCU_CONTROL (STD_ON)/(STD_OFF) will be generated in Mcu_Cfg.h file.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	true

4.33 Parameter McuDfs1UnderMcuControl

Check this if PeriphDFS is under MCU control in any of the Mcu Clock Setting Configurations

(i.e. at least one McuClockSettingConfig/*/McuPeriphDfs/McuDfs_x/McuDFSUnderMcuControl = 'true').

#define MCU_DFS1_UNDER_MCU_CONTROL (STD_ON)/(STD_OFF) will be generated in Mcu_Cfg.h file.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	true

4.34 Container McuDebugConfiguration

This container contains option for non-ASR APIs used for debug or extra-implementation.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.35 Parameter McuDisableDemReportErrorStatus

Enable/Disable the API for reporting the Dem Error.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.36 Parameter McuGetSystemStateApi

Enable/Disable the API for System state information: Mcu_GetSystem_State().

Information extracted from SSCM hw IP.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.37 Parameter McuGetPowerModeStateApi

Enable/Disable the API for MC_ME state: Mcu_GetPowerMode_State().

Get information regarding current power mode, enabled clocks, etc (content of ME_GS register).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.38 Parameter McuGetPowerDomainApi

Enable/Disable the API for MC_PCU state: Mcu_GetPowerDomain_Status().

Get information from PCU_STAT register.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.39 Parameter McuSscmGetMemConfigApi

Enable/Disable the API for Mcu_SscmGetMemConfig().

Get information from SSCM_MEMCONFIG register.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.40 Parameter McuSscmGetStatusApi

Enable/Disable the API for Mcu_SscmGetStatus().

Get information from SSCM_STATUS register.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.41 Parameter McuSscmGetUoptApi

Enable/Disable the API for Mcu_SscmGetUopt().

Get information from SSCM_UOPT register.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.42 Parameter McuGetMidrStructureApi

Enable/Disable the API for Mcu_GetMidrStructure().

Get information from SIUL2 MIDRn registers.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.43 Parameter McuDisableCmuApi

Enable/Disable the API for disabling the clock monitoring unit.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.44 Parameter McuEmiosConfigureGprenApi

Enable/Disable the API for Mcu_EmiosConfigureGpren().

Changes the GPREN bit of the EMIOS_MCR register of an addressed eMIOS instance.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.45 Parameter McuGetClockFrequencyApi

Enable/Disable the API for Mcu_GetClockFrequency().

Return the frequency of a given clock.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.46 Container McuCoreControlConfiguration

This configuration holds global control over the partition specific core control features.

This container is implementation specific.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.47 Parameter McuCoreBootAddressControl

Global ENABLE / DISABLE of the code that writes the PRTNm_COREn_ADDR registers.

These registers give the boot addresses for the cores in their corresponding partitions.

If this check box is ON, the registers will be written during each Mcu_SetMode() call.

#define MCU_CONFIGURE_CADDRN (STD_ON)/(STD_OFF) will be generated in Mcu_Cfg.h file.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.48 Container McuPublishedInformation

Container holding all MCU specific published information parameters.

Included subcontainers:

- McuResetReasonConf

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.49 Container McuResetReasonConf

This container contains the configuration for the different type of reset reason that can be retrieved from Mcu_GetResetReason Api.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE

4.50 Parameter McuResetReason

The parameter represents the different type of reset that a Micro supports. This parameter is referenced by the parameter EcuMResetReason in the ECU State manager module.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	true
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	0
max	255
min	0

4.51 Container CommonPublishedInformation

Common container, aggregated by all modules.

It contains published information about vendor and versions.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.52 Parameter ArReleaseMajorVersion

Major version number of AUTOSAR specification on which the appropriate implementation is based on.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	4
max	4
min	4

4.53 Parameter ArReleaseMinorVersion

Minor version number of AUTOSAR specification on which the appropriate implementation is based on.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION

Property	Value
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	4
max	4
min	4

4.54 Parameter ArReleaseRevisionVersion

Revision version number of AUTOSAR specification on which the appropriate implementation is based on.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	0
max	0
min	0

4.55 Parameter ModuleId

Module ID of this module from Module List.

Note: Implementation Specific Parameter

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION

Property	Value
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	101
max	101
min	101

4.56 Parameter SwMajorVersion

Major version number of the vendor specific implementation of the module. The numbering is vendor specific.

Note: Implementation Specific Parameter

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	4
max	4
min	4

4.57 Parameter SwMinorVersion

Minor version number of the vendor specific implementation of the module. The numbering is vendor specific.

Note: Implementation Specific Parameter

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	0
max	0
min	0

4.58 Parameter SwPatchVersion

Patch level version number of the vendor specific implementation of the module. The numbering is vendor specific.

Note: Implementation Specific Parameter

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	0
max	0
min	0

4.59 Parameter VendorApiInfix

In driver modules which can be instantiated several times on a single ECU, BSW00347 requires that the name of APIs is extended by the VendorId and a vendor specific name.

This parameter is used to specify the vendor specific name. In total, the Implementation specific name is generated as follows:

<ModuleName>_<VendorId>_<VendorApiInfix>.

E.g. assuming that the VendorId of the implementor is 123 and the implementer chose a VendorApiInfix of "v11r456" a api name

Can_Write defined in the SWS will translate to Can_123_v11r456Write.

This parameter is mandatory for all modules with upper multiplicity >

1. It shall not be used for modules with upper multiplicity =1.

Note: Implementation Specific Parameter

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	

4.60 Parameter VendorId

Vendor ID of the dedicated implementation of this module according to the AUTOSAR vendor list.

Note: Implementation Specific Parameter

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
defaultValue	43
max	43
min	43

4.61 Container McuModuleConfiguration

This container contains the configuration for the MCU driver.

Included subcontainers:

- McuClockSettingConfig

- McuDemEventParameterRefs
- McuModeSettingConf
- McuRamSectorSettingConf
- McuResetConfig
- McuPowerControl

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.62 Parameter McuNumberOfMcuModes

This parameter shall represent the number of Modes available for the MCU (from "McuModeSettingConf" list).

CalculationFormula = Number of configured "McuModeSettingConf".

This parameter is not used.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1
max	255
min	1

4.63 Parameter McuRamSectors

This parameter shall represent the number of RAM sectors available for the MCU (from "McuRamSectorSettingConf" list).

CalculationFormula = Number of configured "McuRamSectorSettingConf".

This parameter is not used.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1
max	4294967295
min	0

4.64 Parameter McuResetSetting

This parameters applies to the function Mcu_PerformReset(), which performs a microcontroller reset using the hardware feature of the microcontroller.

Note: This parameter is not used by the current Implementation.

Software Reset occurs when Mcu_PerformReset() function is called.

This parameter is not used.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	1
max	255
min	1

4.65 Parameter McuCrystalFrequencyHz

Crystal Frequency or External Reference Frequency [Hz].

For S32G2XX, the valid range is [20 ... 40] MHz.

For S32R45, the valid value is 40 MHz.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	4.0E7
max	4.0E7
min	2.0E7

4.66 Parameter McuExternalPAD_RTC_EXT_REF_CLK_FrequencyHz

RTC external reference clock (RTC_EXT_REF_CLK) [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	4.8E7
max	2.0E8
min	2.0E7

4.67 Parameter McuExternalPAD_FTM_0_EXT_REF_CLK_FrequencyHz

FTM0 external reference clock (FTM_0_EXT_REF_CLK) [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	2.0E7
max	2.0E7
min	0.0

4.68 Parameter McuExternalPAD_FTM_1_EXT_REF_CLK_FrequencyHz

FTM1 external reference clock (FTM_1_EXT_REF_CLK) [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	2.0E7
max	2.0E7
min	0.0

4.69 Parameter McuExternalPAD_GMAC_EXT_TS_CLK_FrequencyHz

Ethernet timestamp clock (GMAC_EXT_TS_CLK) Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	2.0E8
max	2.0E8
min	5000000.0

4.70 Parameter McuExternalPAD_GMAC_0_EXT_TX_CLK_FrequencyHz

Ethernet TX clock (GMAC_0_EXT_TX_CLK) Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	2500000.0

4.71 Parameter McuExternalPAD_GMAC_0_EXT_RX_CLK_FrequencyHz

Ethernet RX clock (GMAC_0_EXT_RX_CLK) Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	2500000.0

4.72 Parameter McuExternalPAD_GMAC_0_EXT_REF_CLK_FrequencyHz

Ethernet RMII REF Clock (GMAC_0_EXT_REF_CLK) Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	5.0E7
max	5.0E7
min	0.0

4.73 Parameter McuExternalPAD_GMAC_1_EXT_TX_CLK_FrequencyHz

Ethernet TX clock (GMAC_1_EXT_TX_CLK) Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	2500000.0

4.74 Parameter McuExternalPAD_GMAC_1_EXT_RX_CLK_FrequencyHz

Ethernet RX clock (GMAC_1_EXT_RX_CLK) Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	2500000.0

4.75 Parameter McuExternalPAD_GMAC_1_EXT_REF_CLK_FrequencyHz

Ethernet RMII REF Clock (GMAC_1_EXT_REF_CLK) Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	5.0E7
max	5.0E7
min	0.0

4.76 Parameter McuExternalPAD_PFE_MAC_0_EXT_TX_CLK_FrequencyHz

Packet Forwarding Engine Ethernet Port 0 TX clock (PFE_MAC_0_EXT_TX_CLK) Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	3.12E8
max	3.12E8
min	2500000.0

4.77 Parameter McuExternalPAD_PFE_MAC_0_EXT_RX_CLK↩ _FrequencyHz

Packet Forwarding Engine Ethernet Port 0 RX clock (PFE_MAC_0_EXT_RX_CLK) Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	3.12E8
max	3.12E8
min	2500000.0

4.78 Parameter McuExternalPAD_PFE_MAC_0_EXT_REF_↩ CLK_FrequencyHz

Packet Forwarding Engine Ethernet Port 0 RMII REF Clock (PFE_MAC_0_EXT_REF_CLK) Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	5.0E7
max	5.0E7
min	0.0

4.79 Parameter McuExternalPAD_PFE_MAC_1_EXT_TX_CLK_FrequencyHz

Packet Forwarding Engine Ethernet Port 1 TX clock (PFE_MAC_1_EXT_TX_CLK) Reference Frequency [Hz].

Note: This field is not used on S32R45 platforms.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	2500000.0

4.80 Parameter McuExternalPAD_PFE_MAC_1_EXT_RX_CLK_FrequencyHz

Packet Forwarding Engine Ethernet Port 1 RX clock (PFE_MAC_1_EXT_RX_CLK) Reference Frequency [Hz].

Note: This field is not used on S32R45 platforms.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD

Property	Value
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	2500000.0

4.81 Parameter McuExternalPAD_PFE_MAC_1_EXT_REF_↩ CLK_FrequencyHz

Packet Forwarding Engine Ethernet Port 1 RMII REF Clock (PFE_MAC_1_EXT_REF_CLK) Reference Frequency [Hz].

Note: This field is not used on S32R45 platforms.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	5.0E7
max	5.0E7
min	0.0

4.82 Parameter McuExternalPAD_PFE_MAC_2_EXT_TX_CLK↩ _FrequencyHz

Packet Forwarding Engine Ethernet Port 2 TX clock (PFE_MAC_2_EXT_TX_CLK) Reference Frequency [Hz].

Note: This field is not used on S32R45 platforms.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	2500000.0

4.83 Parameter McuExternalPAD_PFE_MAC_2_EXT_RX_CLK_FrequencyHz

Packet Forwarding Engine Ethernet Port 2 RX clock (PFE_MAC_2_EXT_RX_CLK) Reference Frequency [Hz].

Note: This field is not used on S32R45 platforms.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	2500000.0

4.84 Parameter McuExternalPAD_PFE_MAC_2_EXT_REF_↩ CLK_FrequencyHz

Packet Forwarding Engine Ethernet Port 2 RMII REF Clock (PFE_MAC_2_EXT_REF_CLK) Reference Frequency [Hz].

Note: This field is not used on S32R45 platforms.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	5.0E7
max	5.0E7
min	0.0

4.85 Parameter McuInternalPAD_SERDES_0_LANE_0_TX_FrequencyHz

SerDes 0 Lane 0 TX Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE

Property	Value
defaultValue	1.25E8
max	1.25E8
min	1.0E8

4.86 Parameter McuInternalPAD_SERDES_0_LANE_0_CDR_FrequencyHz

SerDes 0 Lane 0 CDR (Clock and Data Recovery) Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	1.0E8

4.87 Parameter McuInternalPAD_SERDES_0_LANE_1_TX_FrequencyHz

SerDes 0 Lane 1 TX Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A

Property	Value
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	1.0E8

4.88 Parameter McuInternalPAD_SERDES_0_LANE_1_CDR_FrequencyHz

SerDes 0 Lane 1 CDR (Clock and Data Recovery) Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	1.0E8

4.89 Parameter McuInternalPAD_SERDES_1_LANE_0_TX_FrequencyHz

SerDes 1 Lane 0 TX Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	1.0E8

4.90 Parameter McuInternalPAD_SERDES_1_LANE_0_CDR_FrequencyHz

SerDes 1 Lane 0 CDR (Clock and Data Recovery) Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	1.0E8

4.91 Parameter McuInternalPAD_SERDES_1_LANE_1_TX_FrequencyHz

SerDes 1 Lane 1 TX Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	1.0E8

4.92 Parameter McuInternalPAD_SERDES_1_LANE_1_CDR_FrequencyHz

SerDes 1 Lane 1 CDR (Clock and Data Recovery) Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	1.0E8

4.93 Parameter McuInternalPAD_SERDES_0_XPCS_0_TX_FrequencyHz

SerDes 0 Xpcs 0 TX Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	1.0E8

4.94 Parameter McuInternalPAD_SERDES_0_XPCS_0_CDR_FrequencyHz

SerDes 0 Xpcs 0 CDR (Clock and Data Recovery) Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	1.0E8

4.95 Parameter McuInternalPAD_SERDES_0_XPCS_1_TX_FrequencyHz

SerDes 0 Xpcs 1 TX Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	1.0E8

4.96 Parameter McuInternalPAD_SERDES_0_XPCS_1_CDR_FrequencyHz

SerDes 0 Xpcs 1 CDR (Clock and Data Recovery) Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	1.0E8

4.97 Parameter McuInternalPAD_SERDES_1_XPCS_0_TX_FrequencyHz

SerDes 1 Xpcs 0 TX Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	1.0E8

4.98 Parameter McuInternalPAD_SERDES_1_XPCS_0_CDR_FrequencyHz

SerDes 1 Xpcs 0 CDR (Clock and Data Recovery) Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	1.0E8

4.99 Parameter McuInternalPAD_SERDES_1_XPCS_1_TX_FrequencyHz

SerDes 1 Xpcs 1 TX Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	1.0E8

4.100 Parameter McuInternalPAD_SERDES_1_XPCS_1_CDR_FrequencyHz

SerDes 1 Xpcs 1 CDR (Clock and Data Recovery) Reference Frequency [Hz].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	1.25E8
max	1.25E8
min	1.0E8

4.101 Parameter McuClockSrcFailureNotification

Enables/Disables clock failure notification.

In case this feature is not supported by HW the setting should be disabled.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	DISABLED
literals	['ENABLED', 'DISABLED']

4.102 Container McuClockSettingConfig

This container contains the configuration for the Clock settings of the MCU.

Included subcontainers:

- McuFXOSC
- McuCgm0SettingConfig
- McuCgm1SettingConfig
- McuCgm2SettingConfig
- McuCgm5SettingConfig
- McuCgm6SettingConfig
- McuRtcClockSelect
- McuPll_0
- McuCoreDfs
- McuPll_1
- McuPeriphDfs
- McuPll_2
- McuPll_3
- McuClkMonitor
- McuClockReferencePoint

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE

4.103 Parameter McuClockSettingId

The Id of this McuClockSettingConfig to be used as argument for the API call Mcu_InitClock().

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	true
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	0
max	255
min	0

4.104 Container McuFXOSC

This container contains the specific configuration of the MCU FXOSC (External Oscillator) configuration.

Note: Implementation Specific Container.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.105 Parameter McuFxoscUnderMcuControl

Set this to TRUE if FXOSC is under MCU control

If it is FALSE then the MCU driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.106 Parameter McuFxoscPowerDownCtr

Crystal oscillator power-down control:

Checked - Crystal oscillator is switched ON.

Unchecked - Crystal oscillator is switched OFF.

Configure the FXOSC_CTRL[OSCON] field.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.107 Parameter McuFxoscByPass

Crystal Oscillator Bypass.

This bit specifies whether the oscillator should be bypassed or not.

0 - Internal oscillator not bypassed.

1 - Internal oscillator bypassed.

Configure the FXOSC_CTRL[OSC_BYP] field.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.108 Parameter McuFxoscMainComparator

Power down signal for main comparator.

This field should be 1 when external crystal is used, and 0 when FXOSC is in Single-Input Bypass Mode (i.e. FXOSC_CTRL[OSC_BYP] = 1).

0 - Comparator disabled.

1 - Comparator enabled.

Configure the FXOSC_CTRL[COMP_EN] field.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.109 Parameter McuFxoscCounter

When the internal counter reaches this value, the oscillator is stable.

These bits specify the "end of count value" to be used for comparison by the

oscillator stabilization counter after reset or whenever it is switched on.

The counter is kept under reset if operating in Single-Input Bypass Mode (i.e. FXOSC_CTRL[OSC_BYP] = 1).

EOCV value is always 1ms in Differential Bypass mode.

Note: Please ensure that the internal counter is running for at least the stabilization

time of the crystal as given in the Data Sheet.

To calculate EOCV from startup time (of crystal), use the following formula:

EOCV (in decimal) = (Stabilization time in ns) / (4 * 128 * Time period of clock in ns)

Configure the FXOSC_CTRL[EOCV] field.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	157
max	255
min	0

4.110 Parameter McuFxoscOverdriveProtection

Crystal overdrive protection.

This value decides the trans-conductance applied by the FXOSC amplifier,

and it will depend on crystal specification.

FXOSC will not function when this field is 0 (0 trans-conductance).

In Differential Bypass Mode, this field must be set to 1.

Configure the FXOSC_CTRL[GM_SEL] field.

Note: FXOSC will not function when this field is set to 0 (0 trans-conductance).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	12
max	15
min	0

4.111 Parameter McuFXOSC_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	4.0E7
min	0.0

4.112 Container McuCgm0SettingConfig

This container contains the configuration for the CGM_0 settings of the MCU.

Included subcontainers:

- McuCgm0PcsConfig
- McuCgm0ClockMux0
- McuCgm0ClockMux1
- McuCgm0ClockMux2
- McuCgm0ClockMux3
- McuCgm0ClockMux4
- McuCgm0ClockMux5
- McuCgm0ClockMux6
- McuCgm0ClockMux7
- McuCgm0ClockMux8
- McuCgm0ClockMux9
- McuCgm0ClockMux10
- McuCgm0ClockMux11
- McuCgm0ClockMux12
- McuCgm0ClockMux14
- McuCgm0ClockMux15
- McuCgm0ClockMux16

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.113 Parameter McuPCSStepDuration

The value provided specifies the number of microseconds per step (i.e. the duration of a step, given in microseconds).

If more time is needed for the power supply to come to full load, this value should be increased.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	100
min	1

4.114 Parameter McuPCSSwitchDuration

MC_CGM_PCFS_SDUR register configuration.

The value provided defines the duration of one PCS clock switch step in terms of 48MHz FIRC cycles.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	48
max	65535
min	0

4.115 Container McuCgm0PcsConfig

This register defines the rate of frequency change and initial change value for the

progressive system clock switching when switching the system clock source to or from

the FXOSC_CLK on ramp-up and ramp-down, respectively.

Note: Implementation Specific Container.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE

4.116 Parameter McuClockPcfsUnderMcuControl

Set this to TRUE if this clock PCFS is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.117 Parameter McuPCS_Name

This is the name of the PCFS module.

PCFS_x corresponds to clock_src_x.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	PCFS_12
literals	['PCFS_12']

4.118 Parameter McuPCS_SourceFrequency

This is the frequency of the input clock source (i.e. the frequency of clk_src_x).

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	2.0E9
min	0.0

4.119 Parameter McuPCS_MaxAllowableDynamicIDD

This value defines the maximum allowable change in current (IDD) per microsecond.

It depends on the application and on the power supply (how much current can it deliver rapidly).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	50.0
max	150.0
min	0.0

4.120 Container McuCgm0ClockMux0

This container enables and selects the configuration clocks for

XBAR_2X_CLK,

XBAR_CLK (always equal to XBAR_2X_CLK / 2),

XBAR_DIV2_CLK (always equal XBAR_2X_CLK / 4),

XBAR_DIV4_CLK (always equal XBAR_2X_CLK / 8),

XBAR_DIV3_CLK (always equal XBAR_2X_CLK / 6),

XBAR_DIV6_CLK (always equal XBAR_2X_CLK / 12),

LBIST_CLK,

DAPB_CLK.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.121 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.122 Parameter McuClkMux0_Source

Clock Mux 0 Source Selection.

Sets the MC_CGM_0_MUX_0_CSC[SELCTL] field register.

MC_CGM_0_MUX_0_CSC[SELCTL] - This field selects the source clock for Clock Mux 0.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'CORE_PLL_DFS1_CLK']

4.123 Parameter McuClockMux0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	8.0E8
min	4.8E7

4.124 Parameter McuClkMux0Div0_En

Clock Mux 0 Divider enable.

This field enables the Clock Divider for LBIST_CLK.

Sets the MC_CGM_0_MUX_0_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_0_MUX_0_DC_0[DIV] and MC_CGM_0_MUX_0_DC_0[PHASE] fields is ignored and the LBIST_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.125 Parameter McuClkMux0Div0_Divisor

Clock Mux 0 Division value.

Sets the MC_CGM_0_MUX_0_DC_0[DIV] field register.

MC_CGM_0_MUX_0_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux0Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.126 Parameter McuClockMux0Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	5.0E7
min	0.0

4.127 Parameter McuClkMux0Div1_En

Clock Mux 0 Divider enable.

This field enables the Clock Divider for DAPB_CLK.

Sets the MC_CGM_0_MUX_0_DC_1[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_0_MUX_0_DC_1[DIV] fields is ignored and the DAPB_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD

4.128 Parameter McuClkMux0Div1_Divisor

Clock Mux 0 Division value.

Sets the MC_CGM_0_MUX_0_DC_1[DIV] field register.

MC_CGM_0_MUX_0_DC_1[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux0Div1_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	5
max	255
min	0

4.129 Parameter McuClockMux0Divider1_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	8000000.0
max	1.334E8
min	0.0

4.130 Container McuCgm0ClockMux1

This container enables and selects the configuration clocks

for CLKOUT0.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.131 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.132 Parameter McuClkMux1_Source

Clock Mux 1 Source Selection.

Sets the MC_CGM_0_MUX_1_CSC[SELCTL] field register.

MC_CGM_0_MUX_1_CSC[SELCTL] - This field selects the source clock for Clock Mux 1.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FXOSC_CLK
literals	['FXOSC_CLK', 'PERIPH_PLL_PHI0_CLK', 'PERIPH_PLL_DFS2_CLK', 'PERIPH_PLL_DFS5_CLK']

4.133 Parameter McuClkMux1Div0_En

Clock Mux 1 Divider enable.

This field enables the Clock Divider for CLKOUT0.

Sets the MC_CGM_0_MUX_1_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_0_MUX_1_DC_0[DIV] field is ignored and the CLKOUT0 clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.134 Parameter McuClkMux1Div0_Divisor

Clock Mux 1 Division value.

Sets the MC_CGM_0_MUX_1_DC_0[DIV] field register.

MC_CGM_0_MUX_1_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux1Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true

Property	Value
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.135 Parameter McuClockMux1Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	2.08E8
min	0.0

4.136 Container McuCgm0ClockMux2

This container enables and selects the configuration clocks

for CLKOUT1.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.137 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.138 Parameter McuClkMux2_Source

Clock Mux 2 Source Selection.

Sets the MC_CGM_0_MUX_2_CSC[SELCTL] field register.

MC_CGM_0_MUX_2_CSC[SELCTL] - This field selects the source clock for Clock Mux 2.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FXOSC_CLK
literals	['FXOSC_CLK', 'PERIPH_PLL_PHI0_CLK', 'PERIPH_PLL_DFS2_CLK', 'PERIPH_PLL_DFS5_CLK']

4.139 Parameter McuClkMux2Div0_En

Clock Mux 2 Divider enable.

This field enables the Clock Divider for CLKOUT1.

Sets the MC_CGM_0_MUX_2_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_0_MUX_2_DC_0[DIV] field is ignored and the CLKOUT1 clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.140 Parameter McuClkMux2Div0_Divisor

Clock Mux 2 Division value.

Sets the MC_CGM_0_MUX_2_DC_0[DIV] field register.

MC_CGM_0_MUX_2_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux2Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.141 Parameter McuClockMux2Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	2.08E8
min	0.0

4.142 Container McuCgm0ClockMux3

This container enables and selects the configuration clocks

for PER_CLK.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.143 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.144 Parameter McuClkMux3_Source

Clock Mux 3 Source Selection.

Sets the MC_CGM_0_MUX_3_CSC[SELCTL] field register.

MC_CGM_0_MUX_3_CSC[SELCTL] - This field selects the source clock for Clock Mux 3.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'PERIPH_PLL_PHI1_CLK']

4.145 Parameter McuClkMux3Div0_En

Clock Mux 3 Divider enable.

This field enables the Clock Divider for PER_CLK.

Sets the MC_CGM_0_MUX_3_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_0_MUX_3_DC_0[DIV] field is ignored and the PER_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.146 Parameter McuClkMux3Div0_Divisor

Clock Mux 3 Division value.

Sets the MC_CGM_0_MUX_3_DC_0[DIV] field register.

MC_CGM_0_MUX_3_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux3Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true

Property	Value
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.147 Parameter McuClockMux3Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	8.0E7
min	0.0

4.148 Container McuCgm0ClockMux4

This container enables and selects the configuration clocks

for FTM_0_REF_CLK.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.149 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.150 Parameter McuClkMux4_Source

Clock Mux 4 Source Selection.

Sets the MC_CGM_0_MUX_4_CSC[SELCTL] field register.

MC_CGM_0_MUX_4_CSC[SELCTL] - This field selects the source clock for Clock Mux 4.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'PERIPH_PLL_PHI1_CLK', 'FTM_0_EXT_REF_CLK']

4.151 Parameter McuClkMux4Div0_En

Clock Mux 4 Divider enable.

This field enables the Clock Divider for FTM_0_REF_CLK.

Sets the MC_CGM_0_MUX_4_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_0_MUX_4_DC_0[DIV] field is ignored and the FTM_0_REF_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.152 Parameter McuClkMux4Div0_Divisor

Clock Mux 4 Division value.

Sets the MC_CGM_0_MUX_4_DC_0[DIV] field register.

MC_CGM_0_MUX_4_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux4Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.153 Parameter McuClockMux4Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1.2E7
max	8.0E7
min	0.0

4.154 Container McuCgm0ClockMux5

This container enables and selects the configuration clocks

for FTM_1_REF_CLK.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.155 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.156 Parameter McuClkMux5_Source

Clock Mux 5 Source Selection.

Sets the MC_CGM_0_MUX_5_CSC[SELCTL] field register.

MC_CGM_0_MUX_5_CSC[SELCTL] - This field selects the source clock for Clock Mux 5.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'PERIPH_PLL_PHI1_CLK', 'FTM_1_EXT_REF_CLK']

4.157 Parameter McuClkMux5Div0_En

Clock Mux 5 Divider enable.

This field enables the Clock Divider for FTM_1_REF_CLK.

Sets the MC_CGM_0_MUX_5_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_0_MUX_5_DC_0[DIV] field is ignored and the FTM_1_REF_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.158 Parameter McuClkMux5Div0_Divisor

Clock Mux 5 Division value.

Sets the MC_CGM_0_MUX_5_DC_0[DIV] field register.

MC_CGM_0_MUX_5_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux5Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true

Property	Value
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.159 Parameter McuClockMux5Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1.2E7
max	8.0E7
min	0.0

4.160 Container McuCgm0ClockMux6

This container enables and selects the configuration clocks

for FLEXRAY_PE_CLK.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.161 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.162 Parameter McuClkMux6_Source

Clock Mux 6 Source Selection.

Sets the MC_CGM_0_MUX_6_CSC[SELCTL] field register.

MC_CGM_0_MUX_6_CSC[SELCTL] - This field selects the source clock for Clock Mux 6.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'FXOSC_CLK', 'PERIPH_PLL_PHI1_CLK']

4.163 Parameter McuClkMux6Div0_En

Clock Mux 6 Divider enable.

This field enables the Clock Divider for FLEXRAY_PE_CLK.

Sets the MC_CGM_0_MUX_6_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_0_MUX_6_DC_0[DIV] field is ignored and the FLEXRAY_PE_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.164 Parameter McuClkMux6Div0_Divisor

Clock Mux 6 Division value.

Sets the MC_CGM_0_MUX_6_DC_0[DIV] field register.

MC_CGM_0_MUX_6_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux6Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.165 Parameter McuClockMux6Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	2.4E7
max	4.0E7
min	0.0

4.166 Container McuCgm0ClockMux7

This container enables and selects the configuration clocks

for CAN_PE_CLK.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.167 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.168 Parameter McuClkMux7_Source

Clock Mux 7 Source Selection.

Sets the MC_CGM_0_MUX_7_CSC[SELCTL] field register.

MC_CGM_0_MUX_7_CSC[SELCTL] - This field selects the source clock for Clock Mux 7.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'FXOSC_CLK', 'PERIPH_PLL_PHI2_CLK']

4.169 Parameter McuClockMux7_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	8.0E7
min	4.0E7

4.170 Container McuCgm0ClockMux8

This container enables and selects the configuration clocks

for LIN_BAUD_CLK and LINFLEXD_CLK (always equal to LIN_BAUD_CLK / 2).

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.171 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.172 Parameter McuClkMux8_Source

Clock Mux 8 Source Selection.

Sets the MC_CGM_0_MUX_8_CSC[SELCTL] field register.

MC_CGM_0_MUX_8_CSC[SELCTL] - This field selects the source clock for Clock Mux 8.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'FXOSC_CLK', 'PERIPH_PLL_PHI3_CLK']

4.173 Parameter McuClockMux8_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	1.33E8
min	0.0

4.174 Container McuCgm0ClockMux9

This container enables and selects the configuration clocks

for GMAC_TS_CLK.

This container is not supported on S32G3XX derivatives.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.175 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.176 Parameter McuClkMux9_Source

Clock Mux 9 Source Selection.

Sets the MC_CGM_0_MUX_9_CSC[SELCTL] field register.

MC_CGM_0_MUX_9_CSC[SELCTL] - This field selects the source clock for Clock Mux 9.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'PERIPH_PLL_PHI4_CLK', 'GMAC_EXT_TS_CLK']

4.177 Parameter McuClkMux9Div0_En

Clock Mux 9 Divider enable.

This field enables the Clock Divider for GMAC_TS_CLK.

Sets the MC_CGM_0_MUX_9_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_0_MUX_9_DC_0[DIV] field is ignored and the GMAC_TS_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.178 Parameter McuClkMux9Div0_Divisor

Clock Mux 9 Division value.

Sets the MC_CGM_0_MUX_9_DC_0[DIV] field register.

MC_CGM_0_MUX_9_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux9Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.179 Parameter McuClockMux9Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	2.0E8
min	0.0

4.180 Container McuCgm0ClockMux10

This container enables and selects the configuration clocks

for GMAC_0_TX_CLK.

This container is not supported on S32G3XX derivatives.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.181 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.182 Parameter McuClkMux10_Source

Clock Mux 10 Source Selection.

Sets the MC_CGM_0_MUX_10_CSC[SELCTL] field register.

MC_CGM_0_MUX_10_CSC[SELCTL] - This field selects the source clock for Clock Mux 10.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'PERIPH_PLL_PHI5_CLK', 'GMAC_0_EXT_TX_CLK', 'GMAC_0_EXT_REF_CLK', 'SERDES_0_XPCS_0_TX']

4.183 Parameter McuClkMux10Div0_En

Clock Mux 10 Divider enable.

This field enables the Clock Divider for GMAC_0_TX_CLK.

Sets the MC_CGM_0_MUX_10_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_0_MUX_10_DC_0[DIV] field is ignored and the GMAC_0_TX_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD

4.184 Parameter McuClkMux10Div0_Divisor

Clock Mux 10 Division value.

Sets the MC_CGM_0_MUX_10_DC_0[DIV] field register.

MC_CGM_0_MUX_10_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux10Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.185 Parameter McuClockMux10Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	1.25E8
min	0.0

4.186 Container McuCgm0ClockMux11

This container enables and selects the configuration clocks

for GMAC_0_RX_CLK.

This container is not supported on S32G3XX derivatives.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.187 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.188 Parameter McuClkMux11_Source

Clock Mux 11 Source Selection.

Sets the MC_CGM_0_MUX_11_CSC[SELCTL] field register.

MC_CGM_0_MUX_11_CSC[SELCTL] - This field selects the source clock for Clock Mux 11.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'GMAC_0_EXT_RX_CLK', 'SERDES_0_XPCS_0_CDR', 'GMAC0_REF_DIV_CLK']

4.189 Parameter McuClockMux11_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	1.25E8
min	2500000.0

4.190 Container McuCgm0ClockMux12

This container enables and selects the configuration clocks

for QSPI_2X_CLK and QSPI_1X_CLK (always equal to QSPI_2X_CLK / 2).

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.191 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.192 Parameter McuClkMux12_Source

Clock Mux 12 Source Selection.

Sets the MC_CGM_0_MUX_12_CSC[SELCTL] field register.

MC_CGM_0_MUX_12_CSC[SELCTL] - This field selects the source clock for Clock Mux 12.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'PERIPH_PLL_DFS1_CLK']

4.193 Parameter McuClkMux12Div0_En

Clock Mux 12 Divider enable.

This field enables the Clock Divider for QSPI_2X_CLK.

Sets the MC_CGM_0_MUX_12_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_0_MUX_12_DC_0[DIV] field is ignored and the QSPI_2X_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.194 Parameter McuClkMux12Div0_Divisor

Clock Mux 12 Division value.

Sets the MC_CGM_0_MUX_12_DC_0[DIV] field register.

MC_CGM_0_MUX_12_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux12Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.195 Parameter McuClockMux12Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

For S32G274A_Rev1 only:

QSPI: QuadSPI DDR 200MHz and DDR 166MHz modes are not supported.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	6.66666667E8
min	0.0

4.196 Container McuCgm0ClockMux14

This container enables and selects the configuration clocks

for SDHC_CLK.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.197 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.198 Parameter McuClkMux14_Source

Clock Mux 14 Source Selection.

Sets the MC_CGM_0_MUX_14_CSC[SELCTL] field register.

MC_CGM_0_MUX_14_CSC[SELCTL] - This field selects the source clock for Clock Mux 14.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'PERIPH_PLL_DFS3_CLK']

4.199 Parameter McuClkMux14Div0_En

Clock Mux 14 Divider enable.

This field enables the Clock Divider for SDHC_CLK.

Sets the MC_CGM_0_MUX_14_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_0_MUX_14_DC_0[DIV] field is ignored and the SDHC_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.200 Parameter McuClkMux14Div0_Divisor

Clock Mux 14 Division value.

Sets the MC_CGM_0_MUX_14_DC_0[DIV] field register.

MC_CGM_0_MUX_14_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux14Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.201 Parameter McuClockMux14Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

For S32G274A_Rev1 only:

uSDHC: DDR-HS400 is not supported.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	2.0E8
min	0.0

4.202 Container McuCgm0ClockMux15

This container enables and selects the configuration clocks

for GMAC0_REF_DIV_CLK.

This container is not supported on S32G3XX derivatives.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.203 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.204 Parameter McuClkMux15_Source

Clock Mux 15 Source Selection.

Sets the MC_CGM_0_MUX_15_CSC[SELCTL] field register.

MC_CGM_0_MUX_15_CSC[SELCTL] - This field selects the source clock for Clock Mux 15.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'GMAC_0_EXT_REF_CLK']

4.205 Parameter McuClockMux15_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	5.0E7
min	0.0

4.206 Parameter McuClkMux15Div0_En

Clock Mux 15 Divider enable.

This field enables the Clock Divider for GMAC0_REF_DIV_CLK.

Sets the MC_CGM_0_MUX_15_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_0_MUX_15_DC_0[DIV] field is ignored and the GMAC0_REF_DIV_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.207 Parameter McuClkMux15Div0_Divisor

Clock Mux 15 Division value.

Sets the MC_CGM_0_MUX_15_DC_0[DIV] field register.

MC_CGM_0_MUX_15_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux15Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.208 Parameter McuClockMux15Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	5.0E7
min	0.0

4.209 Container McuCgm0ClockMux16

This container enables and selects the configuration clocks

for SPI_CLK.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.210 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.211 Parameter McuClkMux16_Source

Clock Mux 16 Source Selection.

Sets the MC_CGM_0_MUX_16_CSC[SELCTL] field register.

MC_CGM_0_MUX_16_CSC[SELCTL] - This field selects the source clock for Clock Mux 16.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'PERIPH_PLL_PHI7_CLK']

4.212 Parameter McuClockMux16_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	1.0E8
min	1.0E7

4.213 Container McuCgm1SettingConfig

This container contains the configuration for the CGM_1 settings of the MCU.

Included subcontainers:

- McuCgm1PcsConfig
- McuCgm1ClockMux0

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.214 Parameter McuPCSStepDuration

The value provided specifies the number of microseconds per step (i.e. the duration of a step, given in microseconds).

If more time is needed for the power supply to come to full load, this value should be increased.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	100
min	1

4.215 Parameter McuPCSSwitchDuration

MC_CGM_PCFS_SDUR register configuration.

The value provided defines the duration of one PCS clock switch step in terms of 48MHz FIRC cycles.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	48
max	65535
min	0

4.216 Container McuCgm1PcsConfig

This register defines the rate of frequency change and initial change value for the

progressive system clock switching when switching the system clock source to or from

the FXOSC_CLK on ramp-up and ramp-down, respectively.

Note: Implementation Specific Container.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE

4.217 Parameter McuClockPcfsUnderMcuControl

Set this to TRUE if this clock PCFS is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.218 Parameter McuPCS_Name

This is the name of the PCFS module.

PCFS_x corresponds to clock_src_x.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	PCFS_4
literals	['PCFS_4']

4.219 Parameter McuPCS_SourceFrequency

This is the frequency of the input clock source (i.e. the frequency of clk_src_x).

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.0E7
max	2.0E9
min	0.0

4.220 Parameter McuPCS_MaxAllowableDynamicIDD

This value defines the maximum allowable change in current (IDD) per microsecond.

It depends on the application and on the power supply (how much current can it deliver rapidly).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	50.0
max	150.0
min	0.0

4.221 Container McuCgm1ClockMux0

This container enables and selects the configuration clocks for

A53_CORE_CLK,

A53_CORE_DIV2_CLK (always equal A53_CORE_CLK / 2),

A53_CORE_DIV10_CLK(always equal A53_CORE_CLK / 10).

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.222 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock refference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.223 Parameter McuClkMux0_Source

Select the Clock Mux 0 Source Selection.

Configure the MC_CGM_1_MUX_0_CSC[SELCTL] field register.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'CORE_PLL_PHI0_CLK']

4.224 Parameter McuClockMux0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	1.0E9
min	0.0

4.225 Container McuCgm2SettingConfig

This container contains the configuration for the CGM_2 settings of the MCU.

Included subcontainers:

- McuCgm2PcsConfig
- McuCgm2ClockMux0
- McuCgm2ClockMux1
- McuGENCTRL1_EMAC0
- McuGENCTRL1_EMAC1
- McuGENCTRL1_EMAC2
- McuCgm2ClockMux2
- McuCgm2ClockMux3
- McuCgm2ClockMux4
- McuCgm2ClockMux5
- McuCgm2ClockMux6
- McuCgm2ClockMux7
- McuCgm2ClockMux8
- McuCgm2ClockMux9

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.226 Parameter McuPCSStepDuration

The value provided specifies the number of microseconds per step (i.e. the duration of a step, given in microseconds).

If more time is needed for the power supply to come to full load, this value should be increased.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	100
min	1

4.227 Parameter McuPCSSwitchDuration

MC_CGM_PCFS_SDUR register configuration.

The value provided defines the duration of one PCS clock switch step in terms of 48MHz FIRC cycles.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	48
max	65535
min	0

4.228 Container McuCgm2PcsConfig

This register defines the rate of frequency change and initial change value for the

progressive system clock switching when switching the system clock source to or from

the FXOSC_CLK on ramp-up and ramp-down, respectively.

Note: Implementation Specific Container.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE

4.229 Parameter McuClockPcfsUnderMcuControl

Set this to TRUE if this clock PCFS is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.230 Parameter McuPCS_Name

This is the name of the PCFS module.

PCFS_x corresponds to clock_src_x.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	PCFS_33
literals	['PCFS_33']

4.231 Parameter McuPCS_SourceFrequency

This is the frequency of the input clock source (i.e. the frequency of clk_src_x).

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.0E7
max	2.0E9
min	0.0

4.232 Parameter McuPCS_MaxAllowableDynamicIDD

This value defines the maximum allowable change in current (IDD) per microsecond.

It depends on the application and on the power supply (how much current can it deliver rapidly).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	50.0
max	150.0
min	0.0

4.233 Container McuCgm2ClockMux0

On S32G2XX, this container enables and selects the configuration clocks for PFE_PE_CLK and PFE_SYS_CLK (always equal to PFE_PE_CLK / 2)

On S32R45, this container enables and selects the configuration clocks for ACCEL_3_CLK and ACCEL_3_DIV3_CLK (always equal to ACCEL_3_CLK / 3).

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.234 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.235 Parameter McuClkMux0_Source

Clock Mux 0 Source Selection.

Sets the MC_CGM_2_MUX_0_CSC[SELCTL] field register.

MC_CGM_2_MUX_0_CSC[SELCTL] - This field selects the source clock for Clock Mux 0.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'ACCEL_PLL_PHI1_CLK']

4.236 Parameter McuClockMux0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	6.0E8
min	0.0

4.237 Parameter McuClkMux0Div0_En

Clock Mux 0 Divider enable.

This field enables the Clock Divider for:

S32G2XX - PFE_PE_CLK, PFE_SYS_CLK

S32R45 - ACCEL_3_CLK, ACCEL_3_DIV3_CLK

Sets the MC_CGM_2_MUX_0_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_2_MUX_0_DC_0[DIV] field is ignored and the PFE_PE_CLK, ACCEL_3_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.238 Parameter McuClkMux0Div0_Divisor

Clock Mux 0 Division value.

Sets the MC_CGM_2_MUX_0_DC_0[DIV] field register.

MC_CGM_2_MUX_0_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux0Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	15
min	0

4.239 Parameter McuClockMux0Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	2.4E7
max	6.0E8
min	0.0

4.240 Container McuCgm2ClockMux1

On S32G2XX, this container enables and selects the configuration clocks for PFE_MAC_0_TX_DIV_CLK.

On S32R45, this container enables and selects the configuration clocks for ACCEL_4_CLK.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.241 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.242 Parameter McuClkMux1_Source

Clock Mux 1 Source Selection.

Sets the MC_CGM_2_MUX_1_CSC[SELCTL] field register.

MC_CGM_2_MUX_1_CSC[SELCTL] - This field selects the source clock for Clock Mux 1.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'SERDES_1_XPCS_0_TX', 'PERIPH_PLL_PHI5_CLK', 'PFE_MAC_0_EXT_TX_CLK', 'PFE_MAC_0_EXT_REF_CLK']

4.243 Parameter McuClockMux1_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	3.125E8
min	2500000.0

4.244 Parameter McuClkMux1Div0_En

Clock Mux 1 Divider enable.

This field enables the Clock Divider for:

S32G2XX - PFE_MAC_0_TX_DIV_CLK

S32R45 - ACCEL_4_CLK

Sets the MC_CGM_2_MUX_1_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_2_MUX_1_DC_0[DIV] field is ignored and the PFE_MAC_0_TX_DIV_CLK, ACCEL_4_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.245 Parameter McuClkMux1Div0_Divisor

Clock Mux 1 Division value.

Sets the MC_CGM_2_MUX_1_DC_0[DIV] field register.

MC_CGM_2_MUX_1_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux1Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.246 Parameter McuClockMux1Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	3.125E8
min	0.0

4.247 Container McuGENCTRL1_EMAC0

On S32GXXX, this container enables and selects the configuration clocks for PFE_MAC_0_TX_CLK.

This container is not supported on S32R45 platform.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.248 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.249 Parameter McuGENCTRL1_EMAC0_Source

PFE_MAC_0_TX_CLK Source Selection.

Sets the GENCTRL1[CTRL] field register.

Sets the GENCTRL1[CTRL] - This field selects the source clock for PFE_MAC_0_TX_CLK.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	SERDES_1_XPCS_0_TX
literals	['PFEMAC0_TX_DIV_CLK', 'SERDES_1_XPCS_0_TX']

4.250 Parameter McuGENCTRL1_EMAC0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	3.125E8
max	3.125E8
min	2500000.0

4.251 Container McuGENCTRL1_EMAC1

On S32G3XX, this container enables and selects the configuration clocks for PFE_MAC_1_TX_CLK.

This container is not supported on S32R45 and S32G2XX platforms.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.252 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.253 Parameter McuGENCTRL1_EMAC1_Source

PFE_MAC_0_TX_CLK Source Selection.

Sets the GENCTRL1[CTRL] field register.

Sets the GENCTRL1[CTRL] - This field selects the source clock for PFE_MAC_1_TX_CLK.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	SERDES_1_XPCS_1_TX
literals	['PFEMAC1_TX_DIV_CLK', 'SERDES_1_XPCS_1_TX']

4.254 Parameter McuGENCTRL1_EMAC1_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1.25E8
max	3.125E8
min	2500000.0

4.255 Container McuGENCTRL1_EMAC2

On S32G3XX, this container enables and selects the configuration clocks for PFE_MAC_2_TX_CLK.

This container is not supported on S32R45 and S32G2XX platforms.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.256 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.257 Parameter McuGENCTRL1_EMAC2_Source

PFE_MAC_0_TX_CLK Source Selection.

Sets the GENCTRL1[CTRL] field register.

Sets the GENCTRL1[CTRL] - This field selects the source clock for PFE_MAC_2_TX_CLK.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	SERDES_0_XPCS_1_TX
literals	['PFEMAC2_TX_DIV_CLK', 'SERDES_0_XPCS_1_TX']

4.258 Parameter McuGENCTRL1_EMAC2_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1.25E8
max	3.125E8
min	2500000.0

4.259 Container McuCgm2ClockMux2

On S32G3XX, this container enables and selects the configuration clocks for PFE_MAC_1_TX_DIV_CLK.

On S32R45, this container enables and selects the configuration clocks for GMAC_1_TX_CLK.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.260 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.261 Parameter McuClkMux2_Source

Clock Mux 2 Source Selection.

Sets the MC_CGM_2_MUX_2_CSC[SELCTL] field register.

MC_CGM_2_MUX_2_CSC[SELCTL] - This field selects the source clock for Clock Mux 2.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'SERDES_1_XPCS_1_TX', 'PERIPH_PLL_PHI5_CLK', 'PFE_MAC_1_EXT_TX_CLK', 'PFE_MAC_1_EXT_REF_CLK']

4.262 Parameter McuClkMux2Div0_En

Clock Mux 2 Divider enable.

This field enables the Clock Divider for:

S32G2XX - PFE_MAC_1_TX_CLK

S32G3XX - PFE_MAC_1_TX_DIV_CLK

S32R45 - GMAC_1_TX_CLK

S32V344 - REC_CLK

Sets the MC_CGM_2_MUX_2_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_2_MUX_2_DC_0[DIV] field is ignored and the PFE_MAC_1_TX_CLK, GMAC_1_TX_CLK, PFE_MAC_1_TX_DIV_CLK or REC_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.263 Parameter McuClkMux2Div0_Divisor

Clock Mux 2 Division value.

Sets the MC_CGM_2_MUX_2_DC_0[DIV] field register.

MC_CGM_2_MUX_2_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux2Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.264 Parameter McuClockMux2Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	3.125E8
min	0.0

4.265 Container McuCgm2ClockMux3

On S32G2XX, this container enables and selects the configuration clocks for PFE_MAC_2_TX_CLK.

On S32G2XX, this container enables and selects the configuration clocks for PFE_MAC_2_TX_DIV_CLK.

On S32R45, this container enables and selects the configuration clocks for GMAC_1_REF_DIV_CLK.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.266 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.267 Parameter McuClkMux3_Source

Clock Mux 3 Source Selection.

Sets the MC_CGM_2_MUX_3_CSC[SELCTL] field register.

MC_CGM_2_MUX_3_CSC[SELCTL] - This field selects the source clock for Clock Mux 3.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'SERDES_0_XPCS_1_TX', 'PERIPH_PLL_PHI5_CLK', 'PFE_MAC_2_EXT_TX_CLK', 'PFE_MAC_2_EXT_REF_CLK']

4.268 Parameter McuClockMux3_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	3.125E8
min	2500000.0

4.269 Parameter McuClkMux3Div0_En

Clock Mux 3 Divider enable.

This field enables the Clock Divider for:

S32G2XX - PFE_MAC_2_TX_CLK

S32G3XX - PFE_MAC_2_TX_DIV_CLK

S32R45 - GMAC_1_REF_DIV_CLK

Sets the MC_CGM_2_MUX_3_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_2_MUX_3_DC_0[DIV] field is ignored and the PFE_MAC_2_TX_CLK or GMAC_1_REF_DIV_CLK, PFE_MAC_2_TX_DIV_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.270 Parameter McuClkMux3Div0_Divisor

Clock Mux 3 Division value.

Sets the MC_CGM_2_MUX_3_DC_0[DIV] field register.

MC_CGM_2_MUX_3_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux3Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.271 Parameter McuClockMux3Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	3.125E8
min	0.0

4.272 Container McuCgm2ClockMux4

On S32G2XX, this container enables and selects the configuration clocks for PFE_MAC_0_RX_CLK.

On S32R45, this container enables and selects the configuration clocks for GMAC_1_RX_CLK.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.273 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.274 Parameter McuClkMux4_Source

Clock Mux 4 Source Selection.

Sets the MC_CGM_2_MUX_4_CSC[SELCTL] field register.

MC_CGM_2_MUX_4_CSC[SELCTL] - This field selects the source clock for Clock Mux 4.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'PFEMAC0_REF_DIV_CLK', 'PFE_MAC_0_EXT_RX_CLK', 'SERDES_1_XPCS_0_CDR']

4.275 Parameter McuClockMux4_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	3.125E8
min	2500000.0

4.276 Parameter McuClkMux4Div0_En

Clock Mux 4 Divider enable.

This field enables the Clock Divider for:

S32V344 - PFEMAC0_REF_DIV_CLK (represented by the name PFEMAC0_REF_DIV_CLK_2)

Sets the MC_CGM_2_MUX_4_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_2_MUX_4_DC_0[DIV] field is ignored and the PFEMAC0_REF_DIV_CLK_2 clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.277 Parameter McuClkMux4Div0_Divisor

Clock Mux 4 Division value.

Sets the MC_CGM_2_MUX_4_DC_0[DIV] field register.

MC_CGM_2_MUX_4_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux4Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	0
min	0

4.278 Parameter McuClockMux4Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	3.125E8
min	0.0

4.279 Container McuCgm2ClockMux5

On S32G2XX, this container enables and selects the configuration clocks for PFE_MAC_1_RX_CLK.

This container is not supported on S32R45 platform.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.280 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.281 Parameter McuClkMux5_Source

Clock Mux 5 Source Selection.

Sets the MC_CGM_2_MUX_5_CSC[SELCTL] field register.

MC_CGM_2_MUX_5_CSC[SELCTL] - This field selects the source clock for Clock Mux 5.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'PFEMAC1_REF_DIV_CLK', 'PFE_MAC_1_EXT_RX_↩ CLK', 'SERDES_1_XPCS_1_CDR']

4.282 Parameter McuClockMux5_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	3.125E8
min	2500000.0

4.283 Container McuCgm2ClockMux6

On S32G2XX, this container enables and selects the configuration clocks for PFE_MAC_2_RX_CLK.

This container is not supported on S32R45 platform.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.284 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.285 Parameter McuClkMux6_Source

Clock Mux 6 Source Selection.

Sets the MC_CGM_2_MUX_6_CSC[SELCTL] field register.

MC_CGM_2_MUX_6_CSC[SELCTL] - This field selects the source clock for Clock Mux 6.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'PFEMAC2_REF_DIV_CLK', 'PFE_MAC_2_EXT_RX_↩ CLK', 'SERDES_0_XPCS_1_CDR']

4.286 Parameter McuClockMux6_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	3.125E8
min	2500000.0

4.287 Container McuCgm2ClockMux7

On S32G2XX, this container enables and selects the configuration clocks for PFEMAC0_REF_DIV_CLK.

This container is not supported on S32R45 platform.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.288 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.289 Parameter McuClkMux7_Source

Clock Mux 7 Source Selection.

Sets the MC_CGM_2_MUX_7_CSC[SELCTL] field register.

MC_CGM_2_MUX_7_CSC[SELCTL] - This field selects the source clock for Clock Mux 7.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'PFE_MAC_0_EXT_REF_CLK']

4.290 Parameter McuClockMux7_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	5.0E7
min	0.0

4.291 Parameter McuClkMux7Div0_En

Clock Mux 7 Divider enable.

This field enables the Clock Divider for:

S32G2XX - PFEMAC0_REF_DIV_CLK

Sets the MC_CGM_2_MUX_7_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_2_MUX_7_DC_0[DIV] field is ignored and the PFEMAC0_REF_DIV_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.292 Parameter McuClkMux7Div0_Divisor

Clock Mux 7 Division value.

Sets the MC_CGM_2_MUX_7_DC_0[DIV] field register.

MC_CGM_2_MUX_7_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux7Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	63
min	0

4.293 Parameter McuClockMux7Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	5.0E7
min	0.0

4.294 Container McuCgm2ClockMux8

On S32G2XX, this container enables and selects the configuration clocks for PFEMAC1_REF_DIV_CLK.

This container is not supported on S32R45 platform.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.295 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.296 Parameter McuClkMux8_Source

Clock Mux 8 Source Selection.

Sets the MC_CGM_2_MUX_8_CSC[SELCTL] field register.

MC_CGM_2_MUX_8_CSC[SELCTL] - This field selects the source clock for Clock Mux 8.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'PFE_MAC_1_EXT_REF_CLK']

4.297 Parameter McuClockMux8_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	5.0E7
min	0.0

4.298 Parameter McuClkMux8Div0_En

Clock Mux 8 Divider enable.

This field enables the Clock Divider for:

S32G2XX - PFEMAC1_REF_DIV_CLK

Sets the MC_CGM_2_MUX_8_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_2_MUX_8_DC_0[DIV] field is ignored and the PFEMAC1_REF_DIV_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.299 Parameter McuClkMux8Div0_Divisor

Clock Mux 8 Division value.

Sets the MC_CGM_2_MUX_8_DC_0[DIV] field register.

MC_CGM_2_MUX_8_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux8Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	63
min	0

4.300 Parameter McuClockMux8Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	5.0E7
min	0.0

4.301 Container McuCgm2ClockMux9

On S32G2XX, this container enables and selects the configuration clocks for PFEMAC2_REF_DIV_CLK.

This container is not supported on S32R45 platform.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.302 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.303 Parameter McuClkMux9_Source

Clock Mux 9 Source Selection.

Sets the MC_CGM_2_MUX_9_CSC[SELCTL] field register.

MC_CGM_2_MUX_9_CSC[SELCTL] - This field selects the source clock for Clock Mux 9.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'PFE_MAC_2_EXT_REF_CLK']

4.304 Parameter McuClockMux9_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	5.0E7
min	0.0

4.305 Parameter McuClkMux9Div0_En

Clock Mux 9 Divider enable.

This field enables the Clock Divider for:

S32G2XX - PFEMAC2_REF_DIV_CLK

Sets the MC_CGM_2_MUX_9_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_2_MUX_9_DC_0[DIV] field is ignored and the PFEMAC2_REF_DIV_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.306 Parameter McuClkMux9Div0_Divisor

Clock Mux 9 Division value.

Sets the MC_CGM_2_MUX_9_DC_0[DIV] field register.

MC_CGM_2_MUX_9_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux9Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	63
min	0

4.307 Parameter McuClockMux9Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	5.0E7
min	0.0

4.308 Container McuCgm5SettingConfig

This container contains the configuration for the CGM_5 settings of the MCU.

Included subcontainers:

- McuCgm5ClockMux0

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.309 Container McuCgm5ClockMux0

This container enables and selects the configuration clocks

for DDR_CLK.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.310 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock refference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.311 Parameter McuClkMux0_Source

Select the Clock Mux 0 Source Selection.

Configure the MC_CGM_5_MUX_0_CSC[SELCTL] field register.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'DDR_PLL_PHI0_CLK']

4.312 Parameter McuClockMux0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	8.0E8
min	0.0

4.313 Container McuCgm6SettingConfig

This container contains the configuration for the CGM_6 settings of the MCU.

Included subcontainers:

- McuCgm6ClockMux0
- McuCgm6ClockMux1
- McuCgm6ClockMux2
- McuCgm6ClockMux3

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.314 Container McuCgm6ClockMux0

This container enables and selects the configuration clocks

for GMAC_TS_CLK.

This container is supported on S32G3XX derivatives only.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.315 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.316 Parameter McuClkMux0_Source

Clock Mux 0 Source Selection.

Sets the MC_CGM_6_MUX_0_CSC[SELCTL] field register.

MC_CGM_6_MUX_0_CSC[SELCTL] - This field selects the source clock for Clock Mux 0.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'PERIPH_PLL_PHI4_CLK', 'GMAC_EXT_TS_CLK']

4.317 Parameter McuClkMux0Div0_En

Clock Mux 0 Divider enable.

This field enables the Clock Divider for GMAC_TS_CLK.

Sets the MC_CGM_6_MUX_0_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_6_MUX_0_DC_0[DIV] field is ignored and the GMAC_TS_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.318 Parameter McuClkMux0Div0_Divisor

Clock Mux 0 Division value.

Sets the MC_CGM_6_MUX_0_DC_0[DIV] field register.

MC_CGM_6_MUX_0_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux9Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.319 Parameter McuClockMux0Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	2.0E8
min	0.0

4.320 Container McuCgm6ClockMux1

This container enables and selects the configuration clocks

for GMAC_0_TX_CLK.

This container is supported on S32G3XX derivatives only.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.321 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.322 Parameter McuClkMux1_Source

Clock Mux 1 Source Selection.

Sets the MC_CGM_6_MUX_1_CSC[SELCTL] field register.

MC_CGM_6_MUX_1_CSC[SELCTL] - This field selects the source clock for Clock Mux 1.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'PERIPH_PLL_PHI5_CLK', 'GMAC_0_EXT_TX_CLK', 'GMAC_0_EXT_REF_CLK', 'SERDES_0_XPCS_0_TX']

4.323 Parameter McuClkMux1Div0_En

Clock Mux 1 Divider enable.

This field enables the Clock Divider for GMAC_0_TX_CLK.

Sets the MC_CGM_6_MUX_1_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_6_MUX_1_DC_0[DIV] field is ignored and the GMAC_0_TX_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.324 Parameter McuClkMux1Div0_Divisor

Clock Mux 1 Division value.

Sets the MC_CGM_6_MUX_1_DC_0[DIV] field register.

MC_CGM_6_MUX_1_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux1Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.325 Parameter McuClockMux1Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	1.25E8
min	0.0

4.326 Container McuCgm6ClockMux2

This container enables and selects the configuration clocks

for GMAC_0_RX_CLK.

This container is supported on S32G3XX derivatives only.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.327 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.328 Parameter McuClkMux2_Source

Clock Mux 2 Source Selection.

Sets the MC_CGM_6_MUX_2_CSC[SELCTL] field register.

MC_CGM_6_MUX_2_CSC[SELCTL] - This field selects the source clock for Clock Mux 2.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'GMAC_0_EXT_RX_CLK', 'SERDES_0_XPCS_0_CDR', 'GMAC0_REF_DIV_CLK']

4.329 Parameter McuClockMux2_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	1.25E8
min	2500000.0

4.330 Container McuCgm6ClockMux3

This container enables and selects the configuration clocks

for GMAC0_REF_DIV_CLK.

This container is supported on S32G3XX derivatives only.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.331 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.332 Parameter McuClkMux3_Source

Clock Mux 3 Source Selection.

Sets the MC_CGM_6_MUX_3_CSC[SELCTL] field register.

MC_CGM_6_MUX_3_CSC[SELCTL] - This field selects the source clock for Clock Mux 3.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'GMAC_0_EXT_REF_CLK']

4.333 Parameter McuClockMux3_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	5.0E7
min	0.0

4.334 Parameter McuClkMux3Div0_En

Clock Mux 3 Divider enable.

This field enables the Clock Divider for GMAC0_REF_DIV_CLK.

Sets the MC_CGM_6_MUX_3_DC_0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

If it is set to 0 (Divider 0 is disabled), any write access to the MC_CGM_6_MUX_3_DC_0[DIV] field is ignored and the GMAC0_REF_DIV_CLK clock remains disabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.335 Parameter McuClkMux3Div0_Divisor

Clock Mux 6 Division value.

Sets the MC_CGM_6_MUX_3_DC_0[DIV] field register.

MC_CGM_6_MUX_3_DC_0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider.

This parameter is enabled only if McuClkMux15Div0_En is true.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.336 Parameter McuClockMux3Divider0_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	4.8E7
max	5.0E7
min	0.0

4.337 Container McuRtcClockSelect

This container selects the configuration clocks for RTC_CLK.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.338 Parameter McuClockMuxUnderMcuControl

Set this to TRUE if this clock mux is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.339 Parameter McuRtc_Source

RTC_CLK Source Selection.

Sets the RTCC[CLKSEL] field register.

Sets the RTCC[CLKSEL] - This field selects the source clock for RTC_CLK.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'RTC_EXT_REF_CLK', 'SIRC_CLK']

4.340 Parameter McuRtc_Frequency

This is the frequency for the specific instance of the "McuClockReferencePoint" container.

Value calculated for user info. It is given in Hz.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	4.8E7
min	0.0

4.341 Container McuPll_0

This container provides the specific configuration for the CORE PLL.

Note: Implementation Specific Container.

Included subcontainers:

- McuPll_Configuration
- McuPll_Parameter

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.342 Parameter McuPLLUnderMcuControl

Set this to TRUE if this PLL is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.343 Parameter McuPLLEnabled

0 - CorePLL is disabled.

1 - CorePLL is enabled (and can be used as a clock source).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.344 Parameter McuPllClockSelection

PLL Source Selection - PLLDIG_PLLCLKMUX[REFCLKSEL].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'FXOSC_CLK']

4.345 Container McuPll_Configuration

Configuration values for PLL.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.346 Parameter McuPllDvRdiv

Input clock predivider.

Sets the PLL: PLLDIG_PLLDV[RDIV] field register.

This field controls the value of the divider on the input clock. The output of the predivider circuit generates the reference clock to the PLL analog loop.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	2
max	7
min	1

4.347 Parameter McuPllDvMfi

Loop multiplication factor divider.
Sets the PLL: PLLDIG_PLLDV[MFI] field register.
This field controls the value of the divider in the feedback loop. The value specified by the MFD bits establishes the multiplication factor applied to the reference frequency. Divider value = MFD, where MFD should be choosen such that it does not violate VCO frequency specifications.
Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	60
max	255
min	1

4.348 Parameter McuPllFmSscgbyp

Modulation enable.

This bit enables spectrum modulation.

Set the PLL: PLLDIG_PLLFM[SSCGBYP] field.

0 - Spread spectrum modulation is not bypassed.

1 - Spread spectrum modulation is bypassed.

Note: PLLFM[SSCGBYP] must be cleared and PLLFD[SDMEN] must be set for the frequency modulation mechanism to be enabled.

Note: Frequency Modulation is only possible if PLLDIG_PLLFM[STEPSIZE] * PLLDIG_PLLFM[STEPNO] less than 18432.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.349 Parameter McuPllFmSpreadctl

Modulation type selection:

- Center around nominal frequency.

- Spread below nominal frequency.

Configure the PLLDIG_PLLFM[SPREADCTL] field register.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	Center_Spread
literals	['Center_Spread']

4.350 Parameter McuPllFmStepSize

Modulation period.

Sets the PLL: PLLDIG_PLLFM[STEPSIZE] field register.

STEPSIZE is the binary equivalent of the modulation period variable.

It is calculated as: StepSize = [McuPllFdMdp * (McuPllDvMfi + McuPllFdMfn / 18432) * 18432] / (100 * McuPllFmStepNo).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	1023
min	0

4.351 Parameter McuPllFmStepNo

Increment step.

Sets the PLL: PLLDIG_PLLFM[STEPNO] field register.

This field is the binary equivalent of the STEPNO variable.

It is calculated as: StepNo = McuClockReferencePointFrequency(McuPllClockSelection) / (2 * McuPllFdFmod * McuPllDvRdiv).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	2047
min	1

4.352 Parameter McuPllFdFmod

The modulation frequency. This should be set to the highest frequency component present in the modulating signal.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	64000.0
min	0.0

4.353 Parameter McuPllFdMdp

The modulation depth percentage. This value indicates by how much the modulated variable varies around its unmodulated level.

It is calculated as the FrequencyDeviation (deviation from the carrier/nominal frequency) divided by the ModulatingSignalFrequency(Fmod).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	3.0
min	0.0

4.354 Parameter McuPllFdEmdp

The effective modulation depth percentage. Because of the rounding operations applied to StepSize and StepNo, the effective MDP may differ from the intended MDP (i.e. the value of 'McuPllFdMdp').

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	3
min	0

4.355 Parameter McuPllFdMfn

Numerator for fractional loop division factor - PLLDIG_PLLFD[MFN].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	32767
min	0

4.356 Parameter McuPllFdSdmen

Sigma Delta Modulation Enable.

Set the PLL: PLLDIG_PLLFD[SDMEN] field register.

0 - Sigma delta modulation disabled.

1 - Sigma delta modulation enabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.357 Parameter McuPllOdiv0_En

PHI0 Divider enable.

Set the PLL: PLLDIG_PLLODIV0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.358 Parameter McuPllOdiv0_Div

PHI0 Division value.

PLLDIG_PLLODIV0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	255
min	0

4.359 Parameter McuPllOdiv1_En

PHI1 Divider enable.

Set the PLL: PLLDIG_PLLODIV1[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.360 Parameter McuPllOdiv1_Div

PHI1 Division value.

PLLDIG_PLLODIV1[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.361 Container McuPll_Parameter

Calculated values for PLL.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.362 Parameter PLL_PHI0_Frequency

Output value for CORE_PLL_PHI0_CLK frequency.

For S32G2XX, the valid range is [0 ... 1000] MHz.

For S32R45, the valid range is [0 ... 800] MHz.

For S32G3XX, the valid range is [0 ... 1311] MHz.

The valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	1.311E9
min	0.0

4.363 Parameter PLL_PHI1_Frequency

Output value for CORE_PLL_PHI1_CLK frequency.

The valid range is [2.54 ... 400] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	1.0
min	0.0

4.364 Parameter PLL_VCO_Frequency

Output value for CORE_VCO frequency.

For S32G2XX, the valid range is [1300 ... 2000] MHz.

For S32R45, the valid range is [1300 ... 1600] MHz.

For S32G3XX, the valid range is [1300 ... 2622] MHz.

The valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	2.622E9
min	0.0

4.365 Container McuCoreDfs

This container provides the specific configuration for the CORE DFS.

Note: Implementation Specific Container.

Included subcontainers:

- McuDfs_1
- McuDfs_2
- McuDfs_3
- McuDfs_4
- McuDfs_5
- McuDfs_6

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.366 Container McuDfs_1

Configuration values for DFS_1.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.367 Parameter McuDFSUnderMcuControl

Set this to TRUE if this DFS is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.368 Parameter McuDFSPort_En

DFS1 Output Port Enable.

This field specifies whether MCU will control the configuration and functionality of CORE_DFS1_CLK inside the driver.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.369 Parameter McuDFSPortMfi

This field provides the integer part of division factor for portn. - DFS_DVPORT0[MFI].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	255
min	1

4.370 Parameter McuDFSPortMfn

This field provides the fractional part of division factor for portn. - DFS_DVPORT0[MFN].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	35
min	0

4.371 Parameter DFS_CLK_Frequency

Output value for CORE_DFS1_CLK frequency.

The valid range is [40 ... 800] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	8.0E8
min	0.0

4.372 Container McuDfs_2

Configuration values for DFS_2.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.373 Parameter McuDFSUnderMcuControl

Set this to TRUE if this DFS is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.374 Parameter McuDFSPort_En

DFS2 Output Port Enable.

This field specifies whether MCU will control the configuration and functionality of CORE_DFS2_CLK inside the driver.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.375 Parameter McuDFSPortMfi

This field provides the integer part of division factor for portn. - DFS_DVPORT1[MFI].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	255
min	1

4.376 Parameter McuDFSPortMfn

This field provides the fractional part of division factor for portn. - DFS_DVPORT1[MFN].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	35
min	0

4.377 Parameter DFS_CLK_Frequency

Output value for CORE_DFS2_CLK frequency.

The valid range is [40 ... 800] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	8.0E8
min	0.0

4.378 Container McuDfs_3

Configuration values for DFS_3.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.379 Parameter McuDFSUnderMcuControl

Set this to TRUE if this DFS is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.380 Parameter McuDFSPort_En

DFS3 Output Port Enable.

This field specifies whether MCU will control the configuration and functionality of CORE_DFS3_CLK inside the driver.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.381 Parameter McuDFSPortMfi

This field provides the integer part of division factor for portn. - DFS_DVPORT2[MFI].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	255
min	1

4.382 Parameter McuDFSPortMfn

This field provides the fractional part of division factor for portn. - DFS_DVPORT2[MFN].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	35
min	0

4.383 Parameter DFS_CLK_Frequency

Output value for CORE_DFS3_CLK frequency.

The valid range is [40 ... 500] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	2.622E9
min	0.0

4.384 Container McuDfs_4

Configuration values for DFS_4.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.385 Parameter McuDFSUnderMcuControl

Set this to TRUE if this DFS is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.386 Parameter McuDFSPort_En

DFS4 Output Port Enable.

This field specifies whether MCU will control the configuration and functionality of CORE_DFS4_CLK inside the driver.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.387 Parameter McuDFSPortMfi

This field provides the integer part of division factor for portn. - DFS_DVPORT3[MFI].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	255
min	1

4.388 Parameter McuDFSPortMfn

This field provides the fractional part of division factor for portn. - DFS_DVPORT3[MFN].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	35
min	0

4.389 Parameter DFS_CLK_Frequency

Output value for CORE_DFS4_CLK frequency.

For S32R45, the valid range is [40 ... 400] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	1.0
min	0.0

4.390 Container McuDfs_5

Configuration values for DFS_5.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.391 Parameter McuDFSUnderMcuControl

Set this to TRUE if this DFS is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.392 Parameter McuDFSPort_En

DFS5 Output Port Enable.

This field specifies whether MCU will control the configuration and functionality of CORE_DFS5_CLK inside the driver.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.393 Parameter McuDFSPortMfi

This field provides the integer part of division factor for portn. - DFS_DVPORT4[MFI].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	255
min	1

4.394 Parameter McuDFSPortMfn

This field provides the fractional part of division factor for portn. - DFS_DVPORT4[MFN].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	35
min	0

4.395 Parameter DFS_CLK_Frequency

Output value for CORE_DFS5_CLK frequency.

The valid range is [2.54 ... 600] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	1.0
min	0.0

4.396 Container McuDfs_6

Configuration values for DFS_6.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.397 Parameter McuDFSUnderMcuControl

Set this to TRUE if this DFS is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.398 Parameter McuDFSPort_En

DFS6 Output Port Enable.

This field specifies whether MCU will control the configuration and functionality of CORE_DFS6_CLK inside the driver.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.399 Parameter McuDFSPortMfi

This field provides the integer part of division factor for portn. - DFS_DVPORT5[MFI].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	255
min	1

4.400 Parameter McuDFSPortMfn

This field provides the fractional part of division factor for portn. - DFS_DVPORT5[MFN].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	35
min	0

4.401 Parameter DFS_CLK_Frequency

Output value for CORE_DFS6_CLK frequency.

The valid range is [2.54 ... 600] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	1.0
min	0.0

4.402 Container McuPll_1

This container provides the specific configuration for the PERIPH PLL.

Note: Implementation Specific Container.

Included subcontainers:

- McuPll_Configuration
- McuPll_Parameter

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.403 Parameter McuPLLUnderMcuControl

Set this to TRUE if this PLL is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.404 Parameter McuPLLEnabled

0 - PeriphPLL is disabled.

1 - PeriphPLL is enabled (and can be used as a clock source).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.405 Parameter McuPllClockSelection

PLL Source Selection - PLLDIG_PLLCLKMUX[REFCLKSEL].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'FXOSC_CLK']

4.406 Container McuPll_Configuration

Configuration values for PLL.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.407 Parameter McuPllDvRdiv

Input clock predivider.

Sets the PLL: PLLDIG_PLLDV[RDIV] field register.

This field controls the value of the divider on the input clock. The output of the predivider circuit generates the reference clock to the PLL analog loop.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	2
max	7
min	1

4.408 Parameter McuPllDvMfi

Loop multiplication factor divider.

Sets the PLL: PLLDIG_PLLDV[MFI] field register.

This field controls the value of the divider in the feedback loop. The value specified by the MFD bits establishes the multiplication factor applied to the reference frequency. Divider value = MFD, where MFD should be choosen such that it does not violate VCO frequency specifications.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	60
max	255
min	1

4.409 Parameter McuPllFdMfn

Numerator for fractional loop division factor - PLLDIG_PLLFD[MFN].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true

Property	Value
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	32767
min	0

4.410 Parameter McuPllFdSdmen

Sigma Delta Modulation Enable.

Set the PLL: PLLDIG_PLLFD[SDMEN] field register.

0 - Sigma delta modulation disabled.

1 - Sigma delta modulation enabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.411 Parameter McuPllOdiv0_En

PHI0 Divider enable.

Set the PLL: PLLDIG_PLLODIV0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.412 Parameter McuPllOdiv0_Div

PHI0 Division value.

PLLDIG_PLLODIV0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.413 Parameter McuPllOdiv1_En

PHI1 Divider enable.

Set the PLL: PLLDIG_PLLODIV1[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.414 Parameter McuPllOdiv1_Div

PHI1 Division value.

PLLDIG_PLLODIV1[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.415 Parameter McuPllOdiv2_En

PHI2 Divider enable.

Set the PLL: PLLDIG_PLLODIV2[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.416 Parameter McuPllOdiv2_Div

PHI2 Division value.

PLLDIG_PLLODIV2[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.417 Parameter McuPllOdiv3_En

PHI3 Divider enable.

Set the PLL: PLLDIG_PLLODIV3[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.418 Parameter McuPllOdiv3_Div

PHI3 Division value.

PLLDIG_PLLODIV3[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.419 Parameter McuPllOdiv4_En

PHI4 Divider enable.

Set the PLL: PLLDIG_PLLODIV4[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.420 Parameter McuPllOdiv4_Div

PHI4 Division value.

PLLDIG_PLLODIV4[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.421 Parameter McuPllOdiv5_En

PHI5 Divider enable.

Set the PLL: PLLDIG_PLLODIV5[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A

Property	Value
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.422 Parameter McuPllOdiv5_Div

PHI5 Division value.

PLLDIG_PLLODIV5[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.423 Parameter McuPllOdiv6_En

PHI6 Divider enable.

Set the PLL: PLLDIG_PLLODIV6[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.424 Parameter McuPllOdiv6_Div

PHI6 Division value.

PLLDIG_PLLODIV6[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.425 Parameter McuPllOdiv7_En

PHI7 Divider enable.

Set the PLL: PLLDIG_PLLODIV7[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.426 Parameter McuPllOdiv7_Div

PHI7 Division value.

PLLDIG_PLLODIV7[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.427 Container McuPll_Parameter

Calculated values for PLL.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.428 Parameter PLL_PHI0_Frequency

Output value for PERIPH_PLL_PHI0_CLK frequency.

For S32G2XX, the valid range is [100 ... 125] MHz.

For S32R45, the valid range is [0 ... 125] MHz.

The valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	1.25E8
min	0.0

4.429 Parameter PLL_PHI1_Frequency

Output value for PERIPH_PLL_PHI1_CLK frequency.

The valid range is [0 ... 80] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	8.0E7
min	0.0

4.430 Parameter PLL_PHI2_Frequency

Output value for PERIPH_PLL_PHI2_CLK frequency.

For S32G2XX, the valid range is [40 ... 80] MHz.

For S32R45, the valid range is [0 ... 80] MHz.

The valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	8.0E7
min	0.0

4.431 Parameter PLL_PHI3_Frequency

Output value for PERIPH_PLL_PHI3_CLK frequency.

The valid range is [0 ... 133] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	1.33E8
min	0.0

4.432 Parameter PLL_PHI4_Frequency

Output value for PERIPH_PLL_PHI4_CLK frequency.

The valid range is [0 ... 200] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	2.0E8
min	0.0

4.433 Parameter PLL_PHI5_Frequency

Output value for PERIPH_PLL_PHI5_CLK frequency.

The valid range is [0 ... 500] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	1.25E8
min	0.0

4.434 Parameter PLL_PHI6_Frequency

Output value for PERIPH_PLL_PHI6_CLK frequency.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	2.0E9
min	0.0

4.435 Parameter PLL_PHI7_Frequency

Output value for PERIPH_PLL_PHI7_CLK frequency.

The valid range is [0 ... 100] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	1.0E8
min	0.0

4.436 Parameter PLL_VCO_Frequency

Output value for PERIPH_VCO frequency.

The valid range is [1300 ... 2000] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	2.0E9
min	0.0

4.437 Container McuPeriphDfs

This container provides the specific configuration for the PERIPH DFS.

Note: Implementation Specific Container.

Included subcontainers:

- McuDfs_1
- McuDfs_2
- McuDfs_3
- McuDfs_4
- McuDfs_5
- McuDfs_6

Property	Value

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.438 Container McuDfs_1

Configuration values for DFS_1.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.439 Parameter McuDFSUnderMcuControl

Set this to TRUE if this DFS is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.440 Parameter McuDFSPort_En

DFS1 Output Port Enable.

This field specifies whether MCU will control the configuration and functionality of PERIPH_DFS1_CLK inside the driver.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.441 Parameter McuDFSPortMfi

This field provides the integer part of division factor for portn. - DFS_DVPORT0[MFI].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	255
min	1

4.442 Parameter McuDFSPortMfn

This field provides the fractional part of division factor for portn. - DFS_DVPORT0[MFN].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	35
min	0

4.443 Parameter DFS_CLK_Frequency

Output value for PERIPH_DFS1_CLK frequency.

For S32R45, the valid range is [133... 532] MHz,

For S32GXXX, the valid range is [532 ... 800] MHz,

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	8.0E8
min	0.0

4.444 Container McuDfs_2

Configuration values for DFS_2.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.445 Parameter McuDFSUnderMcuControl

Set this to TRUE if this DFS is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.446 Parameter McuDFSPort_En

DFS2 Output Port Enable.

This field specifies whether MCU will control the configuration and functionality of PERIPH_DFS2_CLK inside the driver.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.447 Parameter McuDFSPortMfi

This field provides the integer part of division factor for portn. - DFS_DVPORT1[MFI].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	255
min	1

4.448 Parameter McuDFSPortMfn

This field provides the fractional part of division factor for portn. - DFS_DVPORT1[MFN].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	6
max	35
min	0

4.449 Parameter DFS_CLK_Frequency

Output value for PERIPH_DFS2_CLK frequency.

The valid range is [40 ... 628] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	6.28E8
min	0.0

4.450 Container McuDfs_3

Configuration values for DFS_3.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.451 Parameter McuDFSUnderMcuControl

Set this to TRUE if this DFS is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.452 Parameter McuDFSPort_En

DFS3 Output Port Enable.

This field specifies whether MCU will control the configuration and functionality of PERIPH_DFS3_CLK inside the driver.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.453 Parameter McuDFSPortMfi

This field provides the integer part of division factor for portn. - DFS_DVPORT2[MFI].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	255
min	1

4.454 Parameter McuDFSPortMfn

This field provides the fractional part of division factor for portn. - DFS_DVPORT2[MFN].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	35
min	0

4.455 Parameter DFS_CLK_Frequency

Output value for PERIPH_DFS3_CLK frequency.

For S32R45, the valid range is [52 ... 208] MHz,

For S32GXXX, the valid range is [416 ... 800] MHz,

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	8.0E8
min	0.0

4.456 Container McuDfs_4

Configuration values for DFS_4.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.457 Parameter McuDFSUnderMcuControl

Set this to TRUE if this DFS is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.458 Parameter McuDFSPort_En

DFS4 Output Port Enable.

This field specifies whether MCU will control the configuration and functionality of PERIPH_DFS4_CLK inside the driver.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.459 Parameter McuDFSPortMfi

This field provides the integer part of division factor for portn. - DFS_DVPORT3[MFI].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	255
min	1

4.460 Parameter McuDFSPortMfn

This field provides the fractional part of division factor for portn. - DFS_DVPORT3[MFN].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	35
min	0

4.461 Parameter DFS_CLK_Frequency

Output value for PERIPH_DFS4_CLK frequency.

The valid range is [2.54 ... 600] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	1.0
min	0.0

4.462 Container McuDfs_5

Configuration values for DFS_5.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.463 Parameter McuDFSUnderMcuControl

Set this to TRUE if this DFS is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.464 Parameter McuDFSPort_En

DFS5 Output Port Enable.

This field specifies whether MCU will control the configuration and functionality of PERIPH_DFS5_CLK inside the driver.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.465 Parameter McuDFSPortMfi

This field provides the integer part of division factor for portn. - DFS_DVPORT4[MFI].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	255
min	1

4.466 Parameter McuDFSPortMfn

This field provides the fractional part of division factor for portn. - DFS_DVPORT4[MFN].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	35
min	0

4.467 Parameter DFS_CLK_Frequency

Output value for PERIPH_DFS5_CLK frequency.

The valid range is [2.54 ... 80] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	8.0E7
min	0.0

4.468 Container McuDfs_6

Configuration values for DFS_6.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.469 Parameter McuDFSUnderMcuControl

Set this to TRUE if this DFS is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.470 Parameter McuDFSPort_En

DFS6 Output Port Enable.

This field specifies whether MCU will control the configuration and functionality of PERIPH_DFS6_CLK inside the driver.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.471 Parameter McuDFSPortMfi

This field provides the integer part of division factor for portn. - DFS_DVPORT5[MFI].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	255
min	1

4.472 Parameter McuDFSPortMfn

This field provides the fractional part of division factor for portn. - DFS_DVPORT5[MFN].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	35
min	0

4.473 Parameter DFS_CLK_Frequency

Output value for PERIPH_DFS6_CLK frequency.

The valid range is [2.54 ... 300] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	1.0
min	0.0

4.474 Container McuPll_2

This container provides the specific configuration for the ACCEL_PLL.

Note: Implementation Specific Container.

Included subcontainers:

- McuPll_Configuration
- McuPll_Parameter

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.475 Parameter McuPLLUnderMcuControl

Set this to TRUE if this PLL is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.476 Parameter McuPLLEnabled

0 - ACCEL_PLL is disabled.

1 - ACCEL_PLL is enabled (and can be used as a clock source).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.477 Parameter McuPllClockSelection

PLL Source Selection - PLLDIG_PLLCLKMUX[REFCLKSEL].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'FXOSC_CLK']

4.478 Container McuPll_Configuration

Configuration values for PLL.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.479 Parameter McuPllDvRdiv

Input clock predivider.

Sets the PLL: PLLDIG_PLLDV[RDIV] field register.

This field controls the value of the divider on the input clock. The output of the predivider circuit generates the reference clock to the PLL analog loop.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	2
max	7
min	1

4.480 Parameter McuPllDvMfi

Loop multiplication factor divider.

Sets the PLL: PLLDIG_PLLDV[MFI] field register.

This field controls the value of the divider in the feedback loop. The value specified by the MFD bits establishes the multiplication factor applied to the reference frequency. Divider value = MFD, where MFD should be choosen such that it does not violate VCO frequency specifications.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	60
max	255
min	1

4.481 Parameter McuPllFmSscgbyp

Modulation enable.

This bit enables spectrum modulation.

Set the PLL: PLLDIG_PLLFM[SSCGBYP] field.

0 - Spread spectrum modulation is not bypassed.

1 - Spread spectrum modulation is bypassed.

Note: PLLFM[SSCGBYP] must be cleared and PLLFD[SDMEN] must be set for the frequency modulation mechanism to be enabled.

Note: Frequency Modulation is only possible if PLLDIG_PLLFM[STEPSIZE] * PLLDIG_PLLFM[STEPNO] less than 18432.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.482 Parameter McuPllFmSpreadctl

Modulation type selection:

- Center around nominal frequency.

- Spread below nominal frequency.

Configure the PLLDIG_PLLFM[SPREADCTL] field register.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	Center_Spread
literals	['Center_Spread']

4.483 Parameter McuPllFmStepSize

Modulation period.

Sets the PLL: PLLDIG_PLLFM[STEPSIZE] field register.

STEPSIZE is the binary equivalent of the modulation period variable.

It is calculated as: StepSize = [McuPllFdMdp * (McuPllDvMfi + McuPllFdMfn / 18432) * 18432] / (100 * McuPllFmStepNo).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	1023
min	0

4.484 Parameter McuPllFmStepNo

Increment step.

Sets the PLL: PLLDIG_PLLFM[STEPNO] field register.

This field is the binary equivalent of the STEPNO variable.

It is calculated as: StepNo = McuClockReferencePointFrequency(McuPllClockSelection) / (2 * McuPllFdFmod * McuPllDvRdiv).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	2047
min	1

4.485 Parameter McuPllFdFmod

The modulation frequency. This should be set to the highest frequency component present in the modulating signal.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE

Property	Value
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	64000.0
min	0.0

4.486 Parameter McuPllFdMdp

The modulation depth percentage. This value indicates by how much the modulated variable varies around its unmodulated level.

It is calculated as the FrequencyDeviation (deviation from the carrier/nominal frequency) divided by the ModulatingSignalFrequency(Fmod).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	3.0
min	0.0

4.487 Parameter McuPllFdEmdp

The effective modulation depth percentage. Because of the rounding operations applied to StepSize and StepNo,

the effective MDP may differ from the intended MDP (i.e. the value of 'McuPllFdMdp').

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	3
min	0

4.488 Parameter McuPllFdMfn

Numerator for fractional loop division factor - PLLDIG_PLLFD[MFN].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	32767
min	0

4.489 Parameter McuPllFdSdmen

Sigma Delta Modulation Enable.

Set the PLL: PLLDIG_PLLFD[SDMEN] field register.

0 - Sigma delta modulation disabled.

1 - Sigma delta modulation enabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.490 Parameter McuPllOdiv0_En

PHI0 Divider enable.

Set the PLL: PLLDIG_PLLODIV0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.491 Parameter McuPllOdiv0_Div

PHI0 Division value.

PLLDIG_PLLODIV0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.492 Parameter McuPllOdiv1_En

PHI1 Divider enable.

Set the PLL: PLLDIG_PLLODIV1[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.493 Parameter McuPllOdiv1_Div

PHI1 Division value.

PLLDIG_PLLODIV1[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.494 Container McuPll_Parameter

Calculated values for PLL.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.495 Parameter PLL_PHI0_Frequency

Output value for ACCEL_PLL_PHI0_CLK frequency.

The valid range is [0 ... 600] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	6.0E8
min	0.0

4.496 Parameter PLL_PHI1_Frequency

Output value for ACCEL_PLL_PHI1_CLK frequency.

The valid range is [0 ... 600] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true

Property	Value
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	6.0E8
min	0.0

4.497 Parameter PLL_VCO_Frequency

Output value for ACCEL_VCO frequency.

The valid range is [1300 ... 2400] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	2.4E9
min	0.0

4.498 Container McuPll_3

This container provides the specific configuration for the DDR_PLL.

Note: Implementation Specific Container.

Included subcontainers:

- McuPll_Configuration
- McuPll_Parameter

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.499 Parameter McuPLLUnderMcuControl

Set this to TRUE if this PLL is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.500 Parameter McuPLLEnabled

0 - DDR_PLL is disabled.

1 - DDR_PLL is enabled (and can be used as a clock source).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.501 Parameter McuPllClockSelection

PLL Source Selection - PLLDIG_PLLCLKMUX[REFCLKSEL].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	FIRC_CLK
literals	['FIRC_CLK', 'FXOSC_CLK']

4.502 Container McuPll_Configuration

Configuration values for PLL.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.503 Parameter McuPllDvRdiv

Input clock predivider.

Sets the PLL: PLLDIG_PLLDV[RDIV] field register.

This field controls the value of the divider on the input clock. The output of the predivider circuit generates the reference clock to the PLL analog loop.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	2
max	7
min	1

4.504 Parameter McuPllDvMfi

Loop multiplication factor divider.
Sets the PLL: PLLDIG_PLLDV[MFI] field register.
This field controls the value of the divider in the feedback loop. The value specified by the MFD bits establishes the multiplication factor applied to the reference frequency. Divider value = MFD, where MFD should be choosen such that it does not violate VCO frequency specifications.
Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	60
max	255
min	1

4.505 Parameter McuPllFmSscgbyp

Modulation enable.

This bit enables spectrum modulation.

Set the PLL: PLLDIG_PLLFM[SSCGBYP] field.

0 - Spread spectrum modulation is not bypassed.

1 - Spread spectrum modulation is bypassed.

Note: PLLFM[SSCGBYP] must be cleared and PLLFD[SDMEN] must be set for the frequency modulation mechanism to be enabled.

Note: Frequency Modulation is only possible if PLLDIG_PLLFM[STEPSIZE] * PLLDIG_PLLFM[STEPNO] less than 18432.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.506 Parameter McuPllFmSpreadctl

Modulation type selection:

- Center around nominal frequency.

- Spread below nominal frequency.

Configure the PLLDIG_PLLFM[SPREADCTL] field register.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	Center_Spread
literals	['Center_Spread']

4.507 Parameter McuPllFmStepSize

Modulation period.

Sets the PLL: PLLDIG_PLLFM[STEPSIZE] field register.

STEPSIZE is the binary equivalent of the modulation period variable.

It is calculated as: StepSize = [McuPllFdMdp * (McuPllDvMfi + McuPllFdMfn / 18432) * 18432] / (100 * McuPllFmStepNo).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	1023
min	0

4.508 Parameter McuPllFmStepNo

Increment step.

Sets the PLL: PLLDIG_PLLFM[STEPNO] field register.

This field is the binary equivalent of the STEPNO variable.

It is calculated as: StepNo = McuClockReferencePointFrequency(McuPllClockSelection) / (2 * McuPllFdFmod * McuPllDvRdiv).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	2047
min	1

4.509 Parameter McuPllFdFmod

The modulation frequency. This should be set to the highest frequency component present in the modulating signal.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	64000.0
min	0.0

4.510 Parameter McuPllFdMdp

The modulation depth percentage. This value indicates by how much the modulated variable varies around its unmodulated level.

It is calculated as the FrequencyDeviation (deviation from the carrier/nominal frequency) divided by the ModulatingSignalFrequency(Fmod).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	3.0
min	0.0

4.511 Parameter McuPllFdEmdp

The effective modulation depth percentage. Because of the rounding operations applied to StepSize and StepNo, the effective MDP may differ from the intended MDP (i.e. the value of 'McuPllFdMdp').

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	3
min	0

4.512 Parameter McuPllFdMfn

Numerator for fractional loop division factor - PLLDIG_PLLFD[MFN].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	32767
min	0

4.513 Parameter McuPllFdSdmen

Sigma Delta Modulation Enable.

Set the PLL: PLLDIG_PLLFD[SDMEN] field register.

0 - Sigma delta modulation enabled.

1 - Sigma delta modulation disabled.

Note: PLLFM[SSCGBYP] must be cleared and PLLFD[SDMEN] must be set for the frequency modulation mechanism to be enabled.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.514 Parameter McuPllOdiv0_En

PHI0 Divider enable.

Set the PLL: PLLDIG_PLLODIV0[DE] field register.

0 - Divider is disabled

1 - Divider is enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.515 Parameter McuPllOdiv0_Div

PHI0 Division value.

PLLDIG_PLLODIV0[DIV] - This field provides the division value for the clock divider. The clock period of the clock after division

would be 'DIV+1' times the time period of the current input clock to the divider

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.516 Container McuPll_Parameter

Calculated values for PLL.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.517 Parameter PLL_PHI0_Frequency

Output value for DDR_PLL_PHI0_CLK frequency.

The valid range is [0 ... 800] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	8.0E8
min	0.0

4.518 Parameter PLL_VCO_Frequency

Output value for DDR_PLL_VCO frequency.

The valid range is [1300 ... 1600] MHz, the valid value is 0 when disabled.

Note: This field must not be manually modified.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0.0
max	1.6E9
min	0.0

4.519 Container McuClkMonitor

This container contains the specific configuration (parameters) of the Clock Monitor Unit.

Each CMU is independently programmed. FIRC and FXOSC are used as the clock monitor references.

Detailed information on the CMUs can be found in the Clock Monitor Unit chapter.

This parameter is enabled only if "McuClockSrcFailureNotification" is enabled.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	28
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE

4.520 Parameter McuClockMonitorUnderMcuControl

Set this to TRUE if this clock monitor is under mcu control

If it is FALSE then the mcu driver will not write the corresponding registers.

The user must still set the values - they are used by the clock reference points

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.521 Parameter McuClkMonitorEn

Enables/Disables the clock monitor (CMU_FC_GCR[FCE]).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.522 Parameter McuCmuName

This is the name of the CMU.

With name convention: CMU_FC_[Number Of CMU Unit]_[Name of Monitored clock].

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	CMU_FC_0_FXOSC_CLK
literals	['CMU_FC_0_FXOSC_CLK', 'CMU_FC_5_XBAR_DIV3_FAIL_CLK', 'CMU_FC_6_CORE_M7_0_CLK', 'CMU_FC_7_XBAR_DIV3_CLK', 'CMU_FC_8_CORE_M7_1_CLK', 'CMU_FC_9_CORE_M7_2_CLK', 'CMU_FC_10_PER_CLK', 'CMU_FC_11_SERDES_REF_CLK', 'CMU_FC_12_FLEXRAY_CLK', 'CMU_FC_13_FLEXCAN_CLK', 'CMU_FC_14_GMAC0_TX_CLK', 'CMU_FC_15_GMAC_TS_CLK', 'CMU_FC_16_LINFLEXD_CLK', 'CMU_FC_17_QSPI_1X_CLK', 'CMU_FC_18_SDHC_CLK', 'CMU_FC_20_DDR_CLK', 'CMU_FC_21_GMAC0_RX_CLK', 'CMU_FC_22_SPI_CLK', 'CMU_FC_24_CORE_M7_3_CLK', 'CMU_FC_27_CORE_A53_CLUSTER_0_CLK', 'CMU_FC_28_CORE_A53_CLUSTER_1_CLK', 'CMU_FC_39_PFE_SYS_CLK', 'CMU_FC_46_PFEMAC0_TX_DIV_CLK', 'CMU_FC_47_PFEMAC0_RX_CLK', 'CMU_FC_48_PFEMAC1_TX_DIV_CLK', 'CMU_FC_49_PFEMAC1_RX_CLK', 'CMU_FC_50_PFEMAC2_TX_DIV_CLK', 'CMU_FC_51_PFEMAC2_RX_CLK']

4.523 Parameter McuAsyncFHHInterruptEn

This field is used to enable/disable FHH asynchronous interrupt at the module boundary. (CMU_FC_IER[FHHAIE]).

0 - Asynchronous FHH Interrupt is Disabled

1 - Asynchronous FHH Interrupt is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.524 Parameter McuAsyncFLLInterruptEn

This field is used to enable/disable FLL asynchronous interrupt at the module boundary. (CMU_FC_IER[FLLAIE]).

0 - Asynchronous FLL Interrupt is Disabled

1 - Asynchronous FLL Interrupt is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.525 Parameter McuSyncFHHInterruptEn

This field is used to enable/disable FHH synchronous interrupt at the module boundary. (CMU_FC_IER[FHHIE]).

0 - Synchronous FHH Interrupt is Disabled

1 - Synchronous FHH Interrupt is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.526 Parameter McuSyncFLLInterruptEn

This field is used to enable/disable FLL synchronous interrupt at the module boundary. (CMU_FC_IER[FLLIE]).

0 - Synchronous FLL Interrupt is Disabled

1 - Synchronous FLL Interrupt is Enabled

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.527 Container McuClockReferencePoint

This container defines a reference point in the Mcu Clock tree. It defines the frequency which then can be used by other modules as an input value. Lower multiplictiy is 1, as even in the simpliest case (only one frequency is used), there is one frequency to be defined.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE

4.528 Parameter McuClockReferencePointFrequency

This is the frequency for the specific instance of the McuClockReferencePoint container.

It shall be given in Hz.

Calculated value.

Property	Value
type	ECUC-FLOAT-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	2.4E7
max	5.0E9
min	0.0

4.529 Parameter McuClockFrequencySelect

Select clock source for the specific instance of the McuClockReferencePoint container.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	XBAR_CLK
literals	['CUSTOM', 'XBAR_CLK', 'XBAR_DIV2_CLK', 'XBAR_DIV3_CLK', 'XBAR_DIV4_CLK', 'XBAR_DIV6_CLK', 'LBIST_CLK', 'DAPB_CLK', 'CLKOUT0', 'CLKOUT1', 'PER_CLK', 'FTM_0_REF_CLK', 'FTM_1_↩ REF_CLK', 'FLEXRAY_PE_CLK', 'CAN_PE_CLK', 'LIN_BAUD_CLK', 'LINFLEXD_CLK', 'GMAC_TS_CLK', 'GMAC0_TX_CLK', 'GMAC0_↩ RX_CLK', 'QSPI_2X_CLK', 'QSPI_1X_CLK', 'SDHC_CLK', 'GMAC0↩ _REF_CLK', 'GMAC0_REF_DIV_CLK', 'SPI_CLK', 'A53_CORE_CLK', 'A53_CORE_DIV2_CLK', 'A53_CORE_DIV10_CLK', 'PFEMAC0_↩ TX_DIV_CLK', 'PFEMAC0_REF_DIV_CLK', 'PFEMAC0_RX_CLK', 'PFEMAC1_TX_DIV_CLK', 'PFEMAC1_REF_DIV_CLK', 'PFEMAC1↩ _RX_CLK', 'PFEMAC2_TX_DIV_CLK', 'PFEMAC2_REF_DIV_CLK', 'PFEMAC2_RX_CLK', 'PFE_PE_CLK', 'PFE_SYS_CLK', 'DDR_CLK', 'SERDES_REF_CLK', 'FXOSC_CLK', 'FIRC_CLK', 'SIRC_CLK', 'SNVS↩ _CLK', 'RTC_CLK']

4.530 Container McuDemEventParameterRefs

Container for the references to DemEventParameter elements which shall be invoked using the API Dem_SetEventStatus API in case the corresponding error occurs.

The EventId is taken from the referenced DemEventParameter's DemEventId value.

The standardized errors are provided in the container and can be extended by vendor specific error references.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE

4.531 Reference MCU_E_TIMEOUT_FAILURE

Reference to configured DEM event to report Timeout failure.

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
requiresSymbolicNameValue	true
destination	/AUTOSAR/EcucDefs/Dem/DemConfigSet/DemEventParameter

4.532 Reference MCU_E_INVALIDFXOSC_CONFIG

Reference to configured DEM event to report a FXOSC invalid configuration event.

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
requiresSymbolicNameValue	true
destination	/AUTOSAR/EcucDefs/Dem/DemConfigSet/DemEventParameter

4.533 Reference MCU_E_CLOCKMUXSWITCH_FAILURE

Reference to configured DEM event to report a failed clock switch request.

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
requiresSymbolicNameValue	true
destination	/AUTOSAR/EcucDefs/Dem/DemConfigSet/DemEventParameter

4.534 Reference MCU_E_CLOCK_FAILURE

Reference to configured DEM event to report Clock source failure.

Property	Value
type	ECUC-REFERENCE-DEF
origin	AUTOSAR_ECUC
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
requiresSymbolicNameValue	False
destination	/AUTOSAR/EcucDefs/Dem/DemConfigSet/DemEventParameter

4.535 Container McuModeSettingConf

This container contains the configuration for the Mode setting of the MCU.

Note: Implementation Specific Parameter.

Included subcontainers:

- McuPartitionConfiguration

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE

4.536 Parameter McuMode

This parameter shall represent the ID of the MCU mode.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	true
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	0
max	255
min	0

4.537 Parameter McuPowerMode

This parameter selects the Power Mode to be used.

For valid Mode transitions refers to "MC_ME Mode Diagram" from Reference Manual.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	RUN
literals	['RUN', 'CORE_STANDBY', 'SOC_STANDBY', 'FUNC_RESET', 'DEST_↩ RESET', 'CORE_WARM_RESET']

4.538 Parameter McuMainCoreSelect

This field is used to select which core will be designated as the Main Core.

The driver will configure the MC_ME_MAIN_COREID[PIDX] and MC_ME_MAIN_COREID[CIDX]

register fields based on this parameter.

This field is modifiable only when McuPowerMode = 'SOC_STANDBY'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	HSE_CM7
literals	['CM7_0', 'CM7_1', 'CM7_2', 'CM7_3', 'HSE_CM7', 'A53_0', 'A53_1', 'A53↩ _2', 'A53_3', 'A53_4', 'A53_5', 'A53_6', 'A53_7']

4.539 Parameter McuEnableSleepOnExit

Indicates sleep-on-exit when returning from Handler mode to Thread mode:

0 - Do not sleep when returning to Thread mode.

1 - Enter sleep, or deep sleep, on return from an ISR.

Setting this bit to 1 enables an interrupt driven application to avoid returning to an empty main application.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.540 Container McuPartitionConfiguration

This section generates control signals based on the logic partitions

implemented inside it. The logic partition refers to SoC blocks controlled by single

partition of MC_ME. Each of the MC_ME partition implements or control a set of logic

functionality using the MC_ME partition processes hardware.

Note: Implementation Specific Parameter.

Included subcontainers:

- McuPartition0Config
- McuPartition1Config
- McuPartition2Config
- McuPartition3Config
- McuPartition4Config
- McuPartition5Config
- McuPartition6Config
- McuPartition7Config
- McuPeripheral

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.541 Container McuPartition0Config

This container contains the configuration for Partition 0.

Included subcontainers:

- McuCore0Configuration
- McuCore1Configuration
- McuCore2Configuration
- McuCore4Configuration

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.542 Parameter McuPartitionUnderMcuControl

Set this to TRUE if Partition 0 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN0 or PRST0).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.543 Parameter McuPartitionPowerUnderMcuControl

Set this to TRUE if Partition 0 Power Management is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN0_PCONF).

This means that the setting configured by node "McuPartitionClockEnable" will be left untouched

(i.e. the configuration will not have any effect in hardware).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.544 Parameter McuPrtnCofb0UnderMcuControl

Set this to TRUE if PRTN0_COFB0 is under MCU control.
If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN0_COFB0).
This means that all the peripherals under the 'McuPeripheral' list prefixed by 'PRTN0_COFB0'
will be left untouched (i.e. the configuration will not have any effect in hardware).
Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.545 Parameter McuPrstCofb0UnderMcuControl

Set this to TRUE if PRST0_0 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRST0_0).

This means that all the peripherals under the 'McuPeripheral' list prefixed by 'PRST0_COFB0'

will be left untouched (i.e. the configuration will not have any effect in hardware).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.546 Parameter McuPartitionClockEnable

Configures the MC_ME_PRTN0_PCONF[PCE] register field.

This bit controls whether the clock to IPs (other than core(s)) in the partition are enabled or disabled.

0b - Disable the clock to IPs.

1b - Enable the clock to IPs.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.547 Parameter McuPartitionResetEnable

Partition 0 corresponds to the Main Reset Partition which is automatically released from reset after POR, destructive or functional reset.

This bit controls whether the reset signal to IPs (other than core(s)) in the partition is asserted or deasserted.

0b - Deassert the reset signal to IPs.

1b - Assert the reset signal to IPs.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.548 Container McuCore0Configuration

This container contains the configuration for the CM7_0 core within Partition 0.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.549 Parameter McuCoreUnderMcuControl

Set this to TRUE if CM7_0 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN0_CORE0 and PRST0_0).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.550 Parameter McuCoreClockEnable

Configures the MC_ME_PRTN0_CORE0_PCONF[CCE] register field.

This bit controls whether the clock to CM7_0 is enabled or disabled.

0 - CM7_0 Core Clock is Disabled.

1 - CM7_0 Core Clock is Enabled.

Warning: When disabling the core clock, the driver

will busy-wait until the corresponding MC_ME_PRTN0_CORE0_STAT[WFI]

flag is set. This means that the core to be shutdown must always

execute an WFI as its last instruction.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.551 Parameter McuCoreResetEnable

Configures the MC_RGM_PRST0_0[PERIPH_0_RST] register field.

This bit controls whether the CM7_0 reset is asserted or deasserted.

0 - CM7_0 Core Reset is Deasserted.

1 - CM7_0 Core Reset is Asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.552 Parameter McuCoreBootAddress

Configures the MC_ME_PRTN0_CORE0_ADDR[ADDR] register field.

This register controls the boot address of the CM7_0 core.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding CM7_0 core

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	4294967292
min	0

4.553 Parameter McuCoreBootAddressLinkerSym

Configures the MC_ME_PRTN0_CORE0_ADDR[ADDR] register field.

This register controls the boot address of the CM7_0 core.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding CM7_0 core

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: If this parameter is empty, then the boot address

(integer value) defined by 'McuCoreBootAddress' will be used.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	

4.554 Container McuCore1Configuration

This container contains the configuration for the CM7_1 core within Partition 0.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.555 Parameter McuCoreUnderMcuControl

Set this to TRUE if CM7_1 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN0_CORE1 and PRST0_0).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.556 Parameter McuCoreClockEnable

Configures the MC_ME_PRTN0_CORE1_PCONF[CCE] register field.

This bit controls whether the clock to CM7_1 is enabled or disabled.

0 - CM7_1 Core Clock is Disabled.

1 - CM7_1 Core Clock is Enabled.

Warning: When disabling the core clock, the driver

will busy-wait until the corresponding MC_ME_PRTN0_CORE1_STAT[WFI]

flag is set. This means that the core to be shutdown must always

execute an WFI as its last instruction.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.557 Parameter McuCoreResetEnable

Configures the MC_RGM_PRST0_0[PERIPH_1_RST] register field.

This bit controls whether the CM7_1 reset is asserted or deasserted.

0 - CM7_1 Core Reset is Deasserted.

1 - CM7_1 Core Reset is Asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.558 Parameter McuCoreBootAddress

Configures the MC_ME_PRTN0_CORE1_ADDR[ADDR] register field.

This register controls the boot address of the CM7_1 core.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding CM7_1 core

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	4294967292
min	0

4.559 Parameter McuCoreBootAddressLinkerSym

Configures the MC_ME_PRTN0_CORE1_ADDR[ADDR] register field.

This register controls the boot address of the CM7_1 core.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding CM7_1 core

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: If this parameter is empty, then the boot address

(integer value) defined by 'McuCoreBootAddress' will be used.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	

4.560 Container McuCore2Configuration

This container contains the configuration for the CM7_2 core within Partition 0.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.561 Parameter McuCoreUnderMcuControl

Set this to TRUE if CM7_2 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN0_CORE2 and PRST0_0).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.562 Parameter McuCoreClockEnable

Configures the MC_ME_PRTN0_CORE2_PCONF[CCE] register field.

This bit controls whether the clock to CM7_2 is enabled or disabled.

0 - CM7_2 Core Clock is Disabled.

1 - CM7_2 Core Clock is Enabled.

Warning: When disabling the core clock, the driver

will busy-wait until the corresponding MC_ME_PRTN0_CORE2_STAT[WFI]

flag is set. This means that the core to be shutdown must always

execute an WFI as its last instruction.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.563 Parameter McuCoreResetEnable

Configures the MC_RGM_PRST0_0[PERIPH_2_RST] register field.

This bit controls whether the CM7_2 reset is asserted or deasserted.

0 - CM7_2 Core Reset is Deasserted.

1 - CM7_2 Core Reset is Asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.564 Parameter McuCoreBootAddress

Configures the MC_ME_PRTN0_CORE2_ADDR[ADDR] register field.

This register controls the boot address of the CM7_2 core.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding CM7_2 core

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	4294967292
min	0

4.565 Parameter McuCoreBootAddressLinkerSym

Configures the MC_ME_PRTN0_CORE2_ADDR[ADDR] register field.

This register controls the boot address of the CM7_2 core.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding CM7_2 core

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: If this parameter is empty, then the boot address

(integer value) defined by 'McuCoreBootAddress' will be used.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	

4.566 Container McuCore4Configuration

This container contains the configuration for the CM7_3 core within Partition 0.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.567 Parameter McuCoreUnderMcuControl

Set this to TRUE if CM7_3 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN0_CORE4 and PRST0_0).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.568 Parameter McuCoreClockEnable

Configures the MC_ME_PRTN0_CORE4_PCONF[CCE] register field.

This bit controls whether the clock to CM7_3 is enabled or disabled.

0 - CM7_3 Core Clock is Disabled.

1 - CM7_3 Core Clock is Enabled.

Warning: When disabling the core clock, the driver

will busy-wait until the corresponding MC_ME_PRTN0_CORE4_STAT[WFI]

flag is set. This means that the core to be shutdown must always

execute an WFI as its last instruction.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.569 Parameter McuCoreResetEnable

Configures the MC_RGM_PRST0_0[PERIPH_6_RST] register field.

This bit controls whether the CM7_3 reset is asserted or deasserted.

0 - CM7_3 Core Reset is Deasserted.

1 - CM7_3 Core Reset is Asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.570 Parameter McuCoreBootAddress

Configures the MC_ME_PRTN0_CORE4_ADDR[ADDR] register field.

This register controls the boot address of the CM7_3 core.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding CM7_3 core

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	4294967292
min	0

4.571 Parameter McuCoreBootAddressLinkerSym

Configures the MC_ME_PRTN0_CORE4_ADDR[ADDR] register field.

This register controls the boot address of the CM7_3 core.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding CM7_3 core

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: If this parameter is empty, then the boot address

(integer value) defined by 'McuCoreBootAddress' will be used.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	

4.572 Container McuPartition1Config

This container contains the configuration for Partition 1.

Included subcontainers:

- McuCore0Configuration
- McuCore1Configuration
- McuCore2Configuration

- McuCore3Configuration
- McuCore4Configuration
- McuCore5Configuration
- McuCore6Configuration
- McuCore7Configuration

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.573 Parameter McuPartitionUnderMcuControl

Set this to TRUE if Partition 1 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN1 or PRST1).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.574 Parameter McuPartitionPowerUnderMcuControl

Set this to TRUE if Partition 1 Power Management is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN1_PCONF or

PRST1_0[PERIPH_64_RST] or RDC1).

This means that the settings configured by nodes "McuPartitionClockEnable" and "McuPartitionResetEnable"

will be left untouched (i.e. the configuration will not have any effect in hardware).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.575 Parameter McuPrtnCofb0UnderMcuControl

Set this to TRUE if PRTN1_COFB0 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN1_COFB0).

This means that all the peripherals under the 'McuPeripheral' list prefixed by 'PRTN1_COFB0'

will be left untouched (i.e. the configuration will not have any effect in hardware).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.576 Parameter McuPrstCofb0UnderMcuControl

Set this to TRUE if PRST1_0 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRST1_0).

This means that all the peripherals under the 'McuPeripheral' list prefixed by 'PRST1_COFB0'

will be left untouched (i.e. the configuration will not have any effect in hardware).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.577 Parameter McuPartitionClockEnable

Configures the MC_ME_PRTN1_PCONF[PCE] register field.

This bit controls whether the clock to IPs (other than core(s)) in the partition are enabled or disabled.

0b - Disable the clock to IPs.

1b - Enable the clock to IPs.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.578 Parameter McuPartitionResetEnable

Configures the MC_RGM_PRST1_0[PERIPH_64_RST] and RDC1_CTRL_REG[INTERCONNECT_INTERFACE_DISABL register fields.

This bit controls whether the reset signal to IPs (other than core(s)) in the partition is asserted or deasserted.

0b - Deassert the reset signal to IPs.

1b - Assert the reset signal to IPs.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.579 Container McuCore0Configuration

This container contains the configuration for the Cortex-A53 CORE 0 cluster 0 within Partition 1.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.580 Parameter McuCoreUnderMcuControl

Set this to TRUE if Cortex-A53 CORE 0 cluster 0 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN1_CORE0 and PRST1_0).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.581 Parameter McuCoreClockEnable

Configures the MC_ME_PRTN1_CORE0_PCONF[CCE] register field.
Lockstep mode: These registers control CA53 cluster0?1.
Performance mode: These registers control CA53 cluster0.
0 - CA53 cluster0 Core Clock is Disabled.
1 - CA53 cluster0 Core Clock is Enabled.
Warning: When disabling the core clock, the driver
will busy-wait until the corresponding MC_ME_PRTN1_CORE0_STAT[WFI]
flag is set. This means that the core to be shutdown must always
execute an WFI as its last instruction.
Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.582 Parameter McuCoreResetEnable

Configures the MC_RGM_PRST1_0[PERIPH_65_RST] register field.

This bit controls whether the A53_0 reset is asserted or deasserted.

0 - Cortex-A53 CORE 0 cluster 0 Reset is Deasserted.

1 - Cortex-A53 CORE 0 cluster 0 Reset is Asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.583 Parameter McuCoreBootAddress

Configures the MC_ME_PRTN1_CORE0_ADDR[ADDR] register field.

This register controls the boot address of the Cortex-A53 CORE 0 cluster 0.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding Cortex-A53 CORE 0 cluster 0

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	4294967292
min	0

4.584 Parameter McuCoreBootAddressLinkerSym

Configures the MC_ME_PRTN1_CORE0_ADDR[ADDR] register field.

This register controls the boot address of the Cortex-A53 CORE 0 cluster 0.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding Cortex-A53 CORE 0 cluster 0

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: If this parameter is empty, then the boot address

(integer value) defined by 'McuCoreBootAddress' will be used.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	

4.585 Container McuCore1Configuration

This container contains the configuration for the Cortex-A53 CORE 1 cluster 0 within Partition 1.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.586 Parameter McuCoreUnderMcuControl

Set this to TRUE if Cortex-A53 CORE 1 cluster 0 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN1_CORE1 and PRST1_0).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.587 Parameter McuCoreClockEnable

Configures the MC_ME_PRTN1_CORE1_PCONF[CCE] register field.

This bit is reserved. To enable Cortex-A53 CORE 1 cluster 0 please configure McuCore0Configuration/McuCoreClockEnable.

Warning: When disabling the core clock, the driver

will busy-wait until the corresponding MC_ME_PRTN1_CORE1_STAT[WFI]

flag is set. This means that the core to be shutdown must always

execute an WFI as its last instruction.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.588 Parameter McuCoreResetEnable

Configures the MC_RGM_PRST1_0[PERIPH_66_RST] register field.

This bit controls whether the Cortex-A53 CORE 1 cluster 0 reset is asserted or deasserted.

0 - Cortex-A53 CORE 1 cluster 0 Core Reset is Deasserted.

1 - Cortex-A53 CORE 1 cluster 0 Core Reset is Asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.589 Parameter McuCoreBootAddress

Configures the MC_ME_PRTN1_CORE1_ADDR[ADDR] register field.

This register controls the boot address of the Cortex-A53 CORE 1 cluster 0.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding Cortex-A53 CORE 1 cluster 0

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	4294967292
min	0

4.590 Parameter McuCoreBootAddressLinkerSym

Configures the MC_ME_PRTN1_CORE1_ADDR[ADDR] register field.

This register controls the boot address of the Cortex-A53 CORE 1 cluster 0.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding Cortex-A53 CORE 1 cluster 0

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: If this parameter is empty, then the boot address

(integer value) defined by 'McuCoreBootAddress' will be used.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	

4.591 Container McuCore2Configuration

This container contains the configuration for the Cortex-A53 CORE 0 cluster 1 within Partition 1.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.592 Parameter McuCoreUnderMcuControl

Set this to TRUE if Cortex-A53 CORE 0 cluster 1 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN1_CORE2 and PRST1_0).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.593 Parameter McuCoreClockEnable

Configures the MC_ME_PRTN1_CORE2_PCONF[CCE] register field.

Lockstep mode: These registers are reserved.

Performance mode: These registers control CA53 cluster1.

0 - Cortex-A53 CORE 0 cluster 1 Core Clock is Disabled.

1 - Cortex-A53 CORE 0 cluster 1 Core Clock is Enabled.

Warning: When disabling the core clock, the driver

will busy-wait until the corresponding MC_ME_PRTN1_CORE2_STAT[WFI]

flag is set. This means that the core to be shutdown must always

execute an WFI as its last instruction.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.594 Parameter McuCoreResetEnable

Configures the MC_RGM_PRST1_0[PERIPH_67_RST] register field.

This bit controls whether the Cortex-A53 CORE 0 cluster 1 reset is asserted or deasserted.

0 - Cortex-A53 CORE 0 cluster 1 Core Reset is Deasserted.

1 - Cortex-A53 CORE 0 cluster 1 Core Reset is Asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.595 Parameter McuCoreBootAddress

Configures the MC_ME_PRTN1_CORE2_ADDR[ADDR] register field.

This register controls the boot address of the Cortex-A53 CORE 0 cluster 1.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding Cortex-A53 CORE 0 cluster 1

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	4294967292
min	0

4.596 Parameter McuCoreBootAddressLinkerSym

Configures the MC_ME_PRTN1_CORE2_ADDR[ADDR] register field.

This register controls the boot address of the Cortex-A53 CORE 0 cluster 1.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding Cortex-A53 CORE 0 cluster 1

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: If this parameter is empty, then the boot address

(integer value) defined by 'McuCoreBootAddress' will be used.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	

4.597 Container McuCore3Configuration

This container contains the configuration for the Cortex-A53 CORE 1 cluster 1 within Partition 1.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.598 Parameter McuCoreUnderMcuControl

Set this to TRUE if Cortex-A53 CORE 1 cluster 1 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN1_CORE3 and PRST1_0).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.599 Parameter McuCoreClockEnable

Configures the MC_ME_PRTN1_CORE3_PCONF[CCE] register field.

This bit is reserved. To enable Cortex-A53 CORE 1 cluster 1 please configure McuCore2Configuration/McuCoreClockEnable.

Warning: When disabling the core clock, the driver

will busy-wait until the corresponding MC_ME_PRTN1_CORE3_STAT[WFI]

flag is set. This means that the core to be shutdown must always

execute an WFI as its last instruction.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.600 Parameter McuCoreResetEnable

Configures the MC_RGM_PRST1_0[PERIPH_68_RST] register field.

This bit controls whether the Cortex-A53 CORE 1 cluster 1 reset is asserted or deasserted.

0 - Cortex-A53 CORE 1 cluster 1 Core Reset is Deasserted.

1 - Cortex-A53 CORE 1 cluster 1 Core Reset is Asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.601 Parameter McuCoreBootAddress

Configures the MC_ME_PRTN1_CORE3_ADDR[ADDR] register field.

This register controls the boot address of the Cortex-A53 CORE 1 cluster 1.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding Cortex-A53 CORE 1 cluster 1

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	4294967292
min	0

4.602 Parameter McuCoreBootAddressLinkerSym

Configures the MC_ME_PRTN1_CORE3_ADDR[ADDR] register field.

This register controls the boot address of the Cortex-A53 CORE 1 cluster 1.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding Cortex-A53 CORE 1 cluster 1

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: If this parameter is empty, then the boot address

(integer value) defined by 'McuCoreBootAddress' will be used.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	

4.603 Container McuCore4Configuration

This container contains the configuration for the Cortex-A53 CORE 2 cluster 0 core within Partition 1.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.604 Parameter McuCoreUnderMcuControl

Set this to TRUE if Cortex-A53 CORE 2 cluster 0 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN1_CORE4 and PRST1_0).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.605 Parameter McuCoreClockEnable

Configures the MC_ME_PRTN1_CORE4_PCONF[CCE] register field.

This bit is reserved. To enable Cortex-A53 CORE 2 cluster 0 please configure McuCore0Configuration/McuCoreClockEnable.

Warning: When disabling the core clock, the driver

will busy-wait until the corresponding MC_ME_PRTN1_CORE0_STAT[WFI]

flag is set. This means that the core to be shutdown must always

execute an WFI as its last instruction.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.606 Parameter McuCoreResetEnable

Configures the MC_RGM_PRST1_0[PERIPH_69_RST] register field.

This bit controls whether the Cortex-A53 CORE 2 cluster 0 reset is asserted or deasserted.

0 - Cortex-A53 CORE 2 cluster 0 Core Reset is Deasserted.

1 - Cortex-A53 CORE 2 cluster 0 Core Reset is Asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.607 Parameter McuCoreBootAddress

Configures the MC_ME_PRTN1_CORE4_ADDR[ADDR] register field.

This register controls the boot address of the Cortex-A53 CORE 2 cluster 0 core.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding A53_0 core

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	4294967292
min	0

4.608 Parameter McuCoreBootAddressLinkerSym

Configures the MC_ME_PRTN1_CORE4_ADDR[ADDR] register field.

This register controls the boot address of the Cortex-A53 CORE 2 cluster 0 core.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding Cortex-A53 CORE 2 cluster 0 core

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: If this parameter is empty, then the boot address

(integer value) defined by 'McuCoreBootAddress' will be used.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	

4.609 Container McuCore5Configuration

This container contains the configuration for the Cortex-A53 CORE 3 cluster 0 within Partition 1.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.610 Parameter McuCoreUnderMcuControl

Set this to TRUE if Cortex-A53 CORE 3 cluster 0 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN1_CORE1 and PRST1_0).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.611 Parameter McuCoreClockEnable

Configures the MC_ME_PRTN1_CORE1_PCONF[CCE] register field.

This bit is reserved. To enable Cortex-A53 CORE 3 cluster 0 please configure McuCore0Configuration/McuCoreClockEnable.

Warning: When disabling the core clock, the driver

will busy-wait until the corresponding MC_ME_PRTN1_CORE1_STAT[WFI]

flag is set. This means that the core to be shutdown must always

execute an WFI as its last instruction.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.612 Parameter McuCoreResetEnable

Configures the MC_RGM_PRST1_0[PERIPH_70_RST] register field.

This bit controls whether the Cortex-A53 CORE 3 cluster 0 reset is asserted or deasserted.

0 - Cortex-A53 CORE 3 cluster 0 Core Reset is Deasserted.

1 - Cortex-A53 CORE 3 cluster 0 Core Reset is Asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.613 Parameter McuCoreBootAddress

Configures the MC_ME_PRTN1_CORE1_ADDR[ADDR] register field.

This register controls the boot address of the Cortex-A53 CORE 3 cluster 0.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding Cortex-A53 CORE 3 cluster 0

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	4294967292
min	0

4.614 Parameter McuCoreBootAddressLinkerSym

Configures the MC_ME_PRTN1_CORE1_ADDR[ADDR] register field.

This register controls the boot address of the Cortex-A53 CORE 3 cluster 0.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding Cortex-A53 CORE 3 cluster 0

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: If this parameter is empty, then the boot address

(integer value) defined by 'McuCoreBootAddress' will be used.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	

4.615 Container McuCore6Configuration

This container contains the configuration for the Cortex-A53 CORE 2 cluster 1 within Partition 1.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.616 Parameter McuCoreUnderMcuControl

Set this to TRUE if Cortex-A53 CORE 2 cluster 1 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN1_CORE2 and PRST1_0).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.617 Parameter McuCoreClockEnable

Configures the MC_ME_PRTN1_CORE2_PCONF[CCE] register field.

This bit is reserved. To enable Cortex-A53 CORE 2 cluster 1 please configure McuCore2Configuration/McuCoreClockEnable.

Warning: When disabling the core clock, the driver

will busy-wait until the corresponding MC_ME_PRTN1_CORE2_STAT[WFI]

flag is set. This means that the core to be shutdown must always

execute an WFI as its last instruction.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.618 Parameter McuCoreResetEnable

Configures the MC_RGM_PRST1_0[PERIPH_71_RST] register field.

This bit controls whether the Cortex-A53 CORE 2 cluster 1 reset is asserted or deasserted.

0 - Cortex-A53 CORE 2 cluster 1 Core Reset is Deasserted.

1 - Cortex-A53 CORE 2 cluster 1 Core Reset is Asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.619 Parameter McuCoreBootAddress

Configures the MC_ME_PRTN1_CORE2_ADDR[ADDR] register field.

This register controls the boot address of the Cortex-A53 CORE 2 cluster 1.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding Cortex-A53 CORE 2 cluster 1

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	4294967292
min	0

4.620 Parameter McuCoreBootAddressLinkerSym

Configures the MC_ME_PRTN1_CORE2_ADDR[ADDR] register field.

This register controls the boot address of the Cortex-A53 CORE 2 cluster 1.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding Cortex-A53 CORE 2 cluster 1

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: If this parameter is empty, then the boot address

(integer value) defined by 'McuCoreBootAddress' will be used.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	

4.621 Container McuCore7Configuration

This container contains the configuration for the Cortex-A53 CORE 3 cluster 1 within Partition 1.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.622 Parameter McuCoreUnderMcuControl

Set this to TRUE if Cortex-A53 CORE 3 cluster 1 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN1_CORE3 and PRST1_0).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.623 Parameter McuCoreClockEnable

Configures the MC_ME_PRTN1_CORE3_PCONF[CCE] register field.

This bit is reserved. To enable Cortex-A53 CORE 3 cluster 1 please configure McuCore1Configuration/McuCoreClockEnable.

Warning: When disabling the core clock, the driver

will busy-wait until the corresponding MC_ME_PRTN1_CORE3_STAT[WFI]

flag is set. This means that the core to be shutdown must always

execute an WFI as its last instruction.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.624 Parameter McuCoreResetEnable

Configures the MC_RGM_PRST1_0[PERIPH_72_RST] register field.

This bit controls whether the Cortex-A53 CORE 3 cluster 1 reset is asserted or deasserted.

0 - Cortex-A53 CORE 3 cluster 1 Core Reset is Deasserted.

1 - Cortex-A53 CORE 3 cluster 1 Core Reset is Asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.625 Parameter McuCoreBootAddress

Configures the MC_ME_PRTN1_CORE3_ADDR[ADDR] register field.

This register controls the boot address of the Cortex-A53 CORE 3 cluster 1.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding Cortex-A53 CORE 3 cluster 1

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	4294967292
min	0

4.626 Parameter McuCoreBootAddressLinkerSym

Configures the MC_ME_PRTN1_CORE3_ADDR[ADDR] register field.

This register controls the boot address of the Cortex-A53 CORE 3 cluster 1.

The value from this field will be masked with 0xFFFFFFFC (i.e.

the boot address must be aligned on a 4-byte boundary).

This field is modifiable only when the corresponding Cortex-A53 CORE 3 cluster 1

clock is enabled and McuCoreControlConfiguration/McuCoreBootAddressControl

is 'true'.

Note: If this parameter is empty, then the boot address

(integer value) defined by 'McuCoreBootAddress' will be used.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	

4.627 Container McuPartition2Config

This container contains the configuration for Partition 2.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.628 Parameter McuPartitionUnderMcuControl

Set this to TRUE if Partition 2 is under MCU control.
If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN2 or PRST2).
Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.629 Parameter McuPartitionPowerUnderMcuControl

Set this to TRUE if Partition 2 Power Management is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN2_PCONF or PRST2_0[PERIPH_128_RST] or RDC2).

This means that the settings configured by nodes "McuPartitionClockEnable" and "McuPartitionResetEnable" will be left untouched (i.e. the configuration will not have any effect in hardware).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.630 Parameter McuPrtnCofb0UnderMcuControl

Set this to TRUE if PRTN2_COFB0 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN2_COFB0).

This means that all the peripherals under the 'McuPeripheral' list prefixed by 'PRTN2_COFB0'

will be left untouched (i.e. the configuration will not have any effect in hardware).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.631 Parameter McuPrstCofb0UnderMcuControl

Set this to TRUE if PRST2_0 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRST2_0).

This means that all the peripherals under the 'McuPeripheral' list prefixed by 'PRST2_COFB0'

will be left untouched (i.e. the configuration will not have any effect in hardware).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.632 Parameter McuPartitionClockEnable

Configures the MC_ME_PRTN2_PCONF[PCE] register field.

This bit controls whether the clock to IPs (other than core(s)) in the partition are enabled or disabled.

0b - Disable the clock to IPs.

1b - Enable the clock to IPs.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.633 Parameter McuPartitionResetEnable

Configures the MC_RGM_PRST2_0[PERIPH_128_RST] and RDC2_CTRL_REG[INTERCONNECT_INTERFACE_DISAB
register fields.

This bit controls whether the reset signal to IPs (other than core(s)) in the partition is asserted or deasserted.

0b - Deassert the reset signal to IPs.

1b - Assert the reset signal to IPs.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.634 Container McuPartition3Config

This container contains the configuration for Partition 3.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.635 Parameter McuPartitionUnderMcuControl

Set this to TRUE if Partition 3 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN3 or PRST3).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.636 Parameter McuPartitionPowerUnderMcuControl

Set this to TRUE if Partition 3 Power Management is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN3_PCONF or PRST3_0[PERIPH_192_RST] or RDC3).

This means that the settings configured by nodes "McuPartitionClockEnable" and "McuPartitionResetEnable" will be left untouched (i.e. the configuration will not have any effect in hardware).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.637 Parameter McuPrtnCofb0UnderMcuControl

Set this to TRUE if PRTN3_COFB0 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN3_COFB0).

This means that all the peripherals under the 'McuPeripheral' list prefixed by 'PRTN3_COFB0' will be left untouched (i.e. the configuration will not have any effect in hardware).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.638 Parameter McuPrstCofb0UnderMcuControl

Set this to TRUE if PRST3_0 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRST3_0).

This means that all the peripherals under the 'McuPeripheral' list prefixed by 'PRST3_COFB0' will be left untouched (i.e. the configuration will not have any effect in hardware).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.639 Parameter McuPartitionClockEnable

Configures the MC_ME_PRTN3_PCONF[PCE] register field.

This bit controls whether the clock to IPs (other than core(s)) in the partition are enabled or disabled.

0b - Disable the clock to IPs.

1b - Enable the clock to IPs.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.640 Parameter McuPartitionResetEnable

Configures the MC_RGM_PRST3_0[PERIPH_192_RST] and RDC3_CTRL_REG[INTERCONNECT_INTERFACE_DISAB
register fields.

This bit controls whether the reset signal to IPs (other than core(s)) in the partition is asserted or deasserted.

0b - Deassert the reset signal to IPs.

1b - Assert the reset signal to IPs.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A

Property	Value
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.641 Container McuPartition4Config

This container contains the configuration for Partition 4.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.642 Parameter McuPartitionUnderMcuControl

Set this to TRUE if Partition 4 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN4 or PRST4).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.643 Parameter McuPartitionPowerUnderMcuControl

Set this to TRUE if Partition 4 Power Management is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN4_PCONF or PRST4_0[PERIPH_256_RST] or RDC4).

This means that the settings configured by nodes "McuPartitionClockEnable" and "McuPartitionResetEnable" will be left untouched (i.e. the configuration will not have any effect in hardware).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.644 Parameter McuPartitionClockEnable

Configures the MC_ME_PRTN4_PCONF[PCE] register field.

This bit controls whether the clock to IPs (other than core(s)) in the partition are enabled or disabled.

0b - Disable the clock to IPs.

1b - Enable the clock to IPs.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.645 Parameter McuPartitionResetEnable

Configures the MC_RGM_PRST4_0[PERIPH_256_RST] and RDC4_CTRL_REG[INTERCONNECT_INTERFACE_DISAB register fields.

This bit controls whether the reset signal to IPs (other than core(s)) in the partition is asserted or deasserted.

0b - Deassert the reset signal to IPs.

1b - Assert the reset signal to IPs.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.646 Container McuPartition5Config

This container contains the configuration for Partition 5.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.647 Parameter McuPartitionUnderMcuControl

Set this to TRUE if Partition 5 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN5 or PRST5).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.648 Parameter McuPartitionPowerUnderMcuControl

Set this to TRUE if Partition 5 Power Management is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN5_PCONF or PRST5_0[PERIPH_320_RST] or RDC5).

This means that the settings configured by nodes "McuPartitionClockEnable" and "McuPartitionResetEnable" will be left untouched (i.e. the configuration will not have any effect in hardware).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.649 Parameter McuPartitionClockEnable

Configures the MC_ME_PRTN5_PCONF[PCE] register field.

This bit controls whether the clock to IPs (other than core(s)) in the partition are enabled or disabled.

0b - Disable the clock to IPs.

1b - Enable the clock to IPs.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.650 Parameter McuPartitionResetEnable

Configures the MC_RGM_PRST5_0[PERIPH_320_RST] and RDC5_CTRL_REG[INTERCONNECT_INTERFACE_DISAB
register fields.

This bit controls whether the reset signal to IPs (other than core(s)) in the partition is asserted or deasserted.

0b - Deassert the reset signal to IPs.

1b - Assert the reset signal to IPs.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.651 Container McuPartition6Config

This container contains the configuration for Partition 6.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.652 Parameter McuPartitionUnderMcuControl

Set this to TRUE if Partition 6 is under MCU control.
If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN6 or PRST6).
Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.653 Parameter McuPartitionPowerUnderMcuControl

Set this to TRUE if Partition 6 Power Management is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN6_PCONF or PRST6_0[PERIPH_384_RST] or RDC6).

This means that the settings configured by nodes "McuPartitionClockEnable" and "McuPartitionResetEnable" will be left untouched (i.e. the configuration will not have any effect in hardware).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.654 Parameter McuPartitionClockEnable

Configures the MC_ME_PRTN6_PCONF[PCE] register field.

This bit controls whether the clock to IPs (other than core(s)) in the partition should be enabled or disabled.

0b - Disable the clock to IPs.

1b - Enable the clock to IPs.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.655 Parameter McuPartitionResetEnable

Configures the MC_RGM_PRST6_0[PERIPH_384_RST] and RDC6_CTRL_REG[INTERCONNECT_INTERFACE_DISAB
register fields.

This bit controls whether the reset signal to IPs (other than core(s)) in the partition is asserted or deasserted.

0b - Deassert the reset signal to IPs.

1b - Assert the reset signal to IPs.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A

Property	Value
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.656 Container McuPartition7Config

This container contains the configuration for Partition 7.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.657 Parameter McuPartitionUnderMcuControl

Set this to TRUE if Partition 7 is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN7 or PRST7).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.658 Parameter McuPartitionPowerUnderMcuControl

Set this to TRUE if Partition 7 Power Management is under MCU control.

If it is FALSE, then the MCU driver will not write the corresponding registers (PRTN7_PCONF or PRST7_0[PERIPH_448_RST] or RDC7).

This means that the settings configured by nodes "McuPartitionClockEnable" and "McuPartitionResetEnable" will be left untouched (i.e. the configuration will not have any effect in hardware).

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.659 Parameter McuPartitionClockEnable

Configures the MC_ME_PRTN7_PCONF[PCE] register field.

This bit controls whether the clock to IPs (other than core(s)) in the partition are enabled or disabled.

0b - Disable the clock to IPs.

1b - Enable the clock to IPs.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.660 Parameter McuPartitionResetEnable

Configures the MC_RGM_PRST7_0[PERIPH_448_RST] and RDC7_CTRL_REG[INTERCONNECT_INTERFACE_DISAB register fields.

This bit controls whether the reset signal to IPs (other than core(s)) in the partition is asserted or deasserted.

0b - Deassert the reset signal to IPs.

1b - Assert the reset signal to IPs.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	true

4.661 Container McuPeripheral

This contains the power state configuration for the current peripheral.

Note: Implementation Specific Container.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	10
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE

4.662 Parameter McuPeripheralName

This is the name of the peripheral.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	uSDHC
literals	['uSDHC', 'DDR_0', 'PCIe_0', 'PCIe_0_CSS', 'PCIe_1', 'PCIe_1_CSS', 'PFE_MAC0', 'PFE_MAC1', 'PFE_MAC2', 'PFE_TS_CLK']

4.663 Parameter McuModeEntrySlot

This is the MC_ME slot corresponding to the peripheral.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	PRTN0_COFB0_REQ0
literals	['PRTN0_COFB0_REQ0', 'PRTN0_COFB0_REQ1', 'PRTN2_COFB0_REQ0', 'PRTN2_COFB0_REQ1', 'PRTN2_COFB0_REQ2', 'PRTN2_COFB0_REQ3', 'NONE']

4.664 Parameter McuResetGenerationSlot

This is the MC_RGM slot corresponding to the peripheral.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	NONE
literals	['PRST0_COFB0_PERIPH_3', 'PRST0_COFB0_PERIPH_4', 'PRST0_COFB0_PERIPH_5', 'PRST0_COFB0_PERIPH_16', 'PRST0_COFB0_PERIPH_17', 'NONE']

4.665 Parameter McuPeripheralClockEnable

Configures the MC_ME_PRTNx_COFBx_CLKEN[REQx] register field.

0 - Peripheral Clock is Gated.

1 - Peripheral Clock is Running.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.666 Parameter McuPeripheralResetEnable

Configures the MC_RGM_PRSTx_x[PERIPH_x_RST] register field.

0 - Peripheral Reset is Deasserted.

1 - Peripheral Reset is Asserted.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.667 Container McuRamSectorSettingConf

This container contains the configuration for the RAM Sector setting.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE

4.668 Parameter McuRamSectorId

This parameter shall represent the ID of the MCU RAM Sector configuration.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	true
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	0
max	4294967295
min	0

4.669 Parameter McuRamDefaultValue

This parameter shall represent the Data pre-setting to be initialized.

Default value is 0.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	255
min	0

4.670 Parameter McuRamSectionBaseAddress

This parameter represents the RAM section base address.

The address must be aligned to 4 bytes.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	872415232
max	893386743
min	872415232

4.671 Parameter McuRamSectionSize

This parameter represents the RAM section size in bytes.

The size must be a multiple of 4.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1024
max	20971520
min	0

4.672 Parameter McuRamSectionWriteSize

This parameter shall define the size in bytes of data which can be written into RAM at once.

The ram write size is currently restricted to {1, 2, 4, 8} bytes.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	AUTOSAR_ECUC
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	8
max	4294967295
min	0

4.673 Parameter McuRamSectionBaseAddrLinkerSym

This parameter represents the RAM section base address.

The address must be aligned to 4 bytes.

If this parameter is empty, then the integer values from "McuRamSectionBaseAddress" will be used.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	

4.674 Parameter McuRamSectionSizeLinkerSym

This parameter represents the RAM section size in bytes.

The size must be multiple of 4.

If this parameter is empty, then the integer values from "McuRamSectionSize" will be used.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	

4.675 Container McuResetConfig

The reset generation module (MC_RGM) centralizes the different reset sources and manages the reset sequence of the device.

Note: Implementation Specific Parameter.

Included subcontainers:

- McuResetSourcesConfig

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.676 Parameter McuResetType

This parameter selects the type of the reset to be performed through the McuPerformReset API.

A 'destructive' reset source is associated with an event related to a critical - usually hardware - error or dysfunction. When a 'destructive' reset event occurs, the full reset sequence is applied to the chip. This resets the full chip ensuring a safe start-up state for both digital and analog modules, and the memory content must be considered to be unknown.

A 'functional' reset source is associated with an event related to a less-critical - usually non-hardware - error or dysfunction. When a 'functional' reset event occurs, a partial reset sequence is applied to the chip. In this case, most digital modules are reset normally, while the state of analog modules or specific digital modules (e.g., debug modules, flash modules) as well as the system memory content is preserved.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE VARIANT-POST-BUILD: POST-BUILD
defaultValue	FunctionalReset
literals	['FunctionalReset', 'DestructiveReset']

4.677 Parameter McuFuncResetEscThreshold

RGM_FRET[FRET] field configuration.

If the value of this field is 0, the functional reset escalation function is disabled.

Any other value is the number of 'functional' resets which will cause a 'destructive' reset.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	15
max	15
min	0

4.678 Parameter McuDestResetEscThreshold

RGM_DRET[DRET] field configuration.

If the value of this field is 0, the destructive reset escalation function is disabled.

Any other value is the number of 'destructive' resets which will keep the chip in the reset state

until the next power-on reset.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	15
min	0

4.679 Container McuResetSourcesConfig

Configuration of reset sources.

Note: Implementation Specific Parameter.

Included subcontainers:

- McuEXR_ResetSource
- McuF_FR_31_ResetSource

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.680 Container McuEXR_ResetSource

'RESET_B pin assertion' reset source configuration.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.681 Parameter McuDisableReset

RGM_FERD[D_EXR] field configuration.

0 - Functional reset event 'RESET_B pin assertion' triggers a reset sequence.

1 - Functional reset event 'RESET_B pin assertion' generates an interrupt request.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.682 Container McuF_FR_31_ResetSource

'Debug Functional Reset' reset source configuration.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.683 Parameter McuDisableReset

RGM_FERD[D_F_FR_31] field configuration.

0 - Functional reset event 'Debug Functional Reset' triggers a reset sequence.

1 - Functional reset event 'Debug Functional Reset' generates an interrupt request.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.684 Container McuPowerControl

Note: Implementation Specific Parameter.

Included subcontainers:

- McuPMC_Config

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.685 Container McuPMC_Config

This PMC Control Register contains the various control settings of the PMC block, see table "PMC NCSPD mapping"

in RM.

Note: Implementation Specific Parameter.

Included subcontainers:

- None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.686 Parameter McuVDD_FXOSCNonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL0] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on VDD_FXOSC able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.687 Parameter McuVDD_ADC0NonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL1] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on VDD_ADC0 able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.688 Parameter McuVDD_ADC1NonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL2] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on VDD_ADC1 able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.689 Parameter McuVDD_TMUNonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL3] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on VDD_TMU able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.690 Parameter McuVDD_EFUSENonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL4] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on VDD_EFUSE able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.691 Parameter McuVDD_HV_PLLNonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL5] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on VDD_HV_PLL able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.692 Parameter McuVDD_LV_PLLNonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL6] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on VDD_LV_PLL able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.693 Parameter McuVDD_HV_PLL_DDR0NonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL7] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on VDD_HV_PLL_DDR0 able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.694 Parameter McuVDD_LV_PLL_DDR0NonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL8] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on VDD_LV_PLL_DDR0 able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.695 Parameter McuVDD_HV_PLL_AURNonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL9] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on VDD_HV_PLL_AUR able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.696 Parameter McuVDD_LV_PLL_AURNonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL10] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on VDD_LV_PLL_AUR able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.697 Parameter McuVDD_IO_STBYNonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL11] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on VDD_IO_STBY able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.698 Parameter McuVDD_IO_ANonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL17] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on VDD_IO_A able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.699 Parameter McuVDD_IO_BNonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL18] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on VDD_IO_B able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.700 Parameter McuVDD_IO_USBNonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL21] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on VDD_IO_USB able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.701 Parameter McuVDD_HV_PLL_ACCNonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL11] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on VDD_HV_PLL_ACC able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.702 Parameter McuVDD_LV_PLL_ACCNonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL12] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on VDD_LV_PLL_ACC able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.703 Parameter McuVDD_IO_SDHCNonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL23] field configuration for S32R45 derivative.

PMC_NCPSD_CTL[NCSPD_CTL22] field configuration for S32GXXX derivative.

Non-critical supply presence detector control

The non-critical SPD input on VDD_IO_SDHC I/O segment able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.704 Parameter McuVDD_IO_C_GPIO4NonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL24] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on GPIO_4 I/O segment supply SPD monitor (VDD_IO_C) able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.705 Parameter McuVDD_IO_B_GPIO3NonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL25] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on GPIO_3 I/O segment supply SPD monitor (VDD_IO_B) able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.706 Parameter McuVDD_IO_B_GPIO2NonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL26] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on GPIO_2 I/O segment supply SPD monitor (VDD_IO_B) able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A

Property	Value
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.707 Parameter McuVDD_IO_A_GPIO1NonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL27] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on GPIO_1 I/O segment supply SPD monitor (VDD_IO_A) able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.708 Parameter McuVDD_IO_GMAC1NonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL28] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on GMAC_1 I/O segment supply SPD monitor (VDD_IO_GMAC1) able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.709 Parameter McuVDD_IO_GMAC0NonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL29] field configuration.

Non-critical supply presence detector control

The non-critical SPD input on GMAC_0 I/O segment supply SPD monitor (VDD_IO_GMAC0) able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.710 Parameter McuVDD_IO_CLKOUTNonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL30] field configuration for S32R45.

PMC_NCPSD_CTL[NCSPD_CTL28] field configuration for S32GXXX.

Non-critical supply presence detector control

The non-critical SPD input on CLKOUT I/O segment supply SPD monitor (VDD_IO_CLKOUT) able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.711 Parameter McuVDD_IO_QSPINonCriticalFlag

PMC_NCPSD_CTL[NCSPD_CTL31] field configuration for S32R45.

PMC_NCPSD_CTL[NCSPD_CTL23] field configuration for S32GXXX.

Non-critical supply presence detector control

The non-critical SPD input on QuadSPI_A I/O segment supply SPD monitor (VDD_IO_QSPI) able to set the non-critical output flag.

0 - The NCSPD cannot set the non-critical flag.

1 - An NCSPD event will set the non-critical flag.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

This chapter describes the Tresos configuration plug-in for the *driver* Driver. The most of the parameters are described below.

Chapter 5

Module Index

5.1 Software Specification

Here is a list of all modules:

Chapter 6

Module Documentation

6.1 Clock Ip Driver

6.1.1 Detailed Description

Data Structures

- struct Clock_Ip_ExtOSCType
- struct Clock_Ip_ClockMonitorType
- struct Clock_Ip_IrcoscConfigType

  Clock Source IRCOSC configuration structure. Implements Clock_Ip_IrcoscConfigType_Class. More...
- struct Clock_Ip_XoscConfigType

  CGM Clock Source XOSC configuration structure. Implements Clock_Ip_XoscConfigType_Class. More...
- struct Clock_Ip_PllConfigType

  CGM Clock Source PLLDIG configuration structure. Implements Clock_Ip_PllConfigType_Class. More...
- struct Clock_Ip_SelectorConfigType

  Clock selector configuration structure. Implements Clock_Ip_SelectorConfigType_Class. More...
- struct Clock_Ip_DividerConfigType

  Clock divider configuration structure. Implements Clock_Ip_DividerConfigType_Class. More...
- struct Clock_Ip_DividerTriggerConfigType

  Clock divider trigger configuration structure. Implements Clock_Ip_DividerTriggerConfigType_Class. More...
- struct Clock_Ip_FracDivConfigType

  Clock fractional divider configuration structure. Implements Clock_Ip_FracDivConfigType_Class. More...
- struct Clock_Ip_ExtClkConfigType

  Clock external clock configuration structure. Implements Clock_Ip_ExtClkConfigType_Class. More...
- struct Clock_Ip_PcfsConfigType

  Clock Source PCFS configuration structure. Implements Clock_Ip_PcfsConfigType_Class. More...
- struct Clock_Ip_GateConfigType

  Clock gate clock configuration structure. Implements Clock_Ip_GateConfigType_Class. More...
- struct Clock_Ip_CmuConfigType

  Clock cmu configuration structure. Implements Clock_Ip_CmuConfigType_Class. More...
- struct Clock_Ip_ConfiguredFrequencyType

Configured frequency structure. Implements Clock_Ip_ConfiguredFrequencyType_Class. More...

- struct Clock_Ip_SpecificPerpihParamType

  Clock Specific peripheral configure. Implements Clock_Ip_SpecificPerpihParamType_Class. More...
- struct Clock_IP_SpecificPeriphConfigType

  Clock Specific peripheral structure. Implements Clock_IP_SpecificPeriphConfigType_Class. More...
- struct Clock_Ip_ClockConfigType

  Clock configuration structure. Implements Clock_Ip_ClockConfigType_Class. More...

Macros

- #define CLOCK_IP_NO_PLL

  This parameter shall be set True, if the H/W does not have a PLL.

Types Reference

- typedef void(∗ Clock_Ip_NotificationsCallbackType) (Clock_Ip_NotificationType Error, Clock_Ip_NameType ClockName)

  Clock notifications callback type. Implements ClockNotificationsCallbackType_Class.

Enum Reference

- enum Clock_Ip_ClockNameSourceType

  Clock ip source type.
- enum Clock_Ip_PllStatusReturnType

  Clock pll status return codes.
- enum Clock_Ip_DfsStatusType

  Clock dfs status return codes.
- enum Clock_Ip_PowerModesType

  Power modes.
- enum Clock_Ip_PowerNotificationType

  Power mode notification.
- enum Clock_Ip_NameType

  Clock names.
- enum Clock_Ip_StatusType

  Clock ip status return codes.
- enum Clock_Ip_PllStatusType

  Clock ip pll status return codes.
- enum Clock_Ip_CmuStatusType

  Clock ip cmu status return codes.
- enum Clock_Ip_NotificationType

  Clock ip report error types.
- enum Clock_Ip_TriggerDividerType

  Clock ip trigger divider type.
- enum Clock_Ip_SpecificPeriphParamType

  specific peripheral.

Function Reference

- uint32 Clock_Ip_GetClockFrequency (Clock_Ip_NameType ClockName)

  Gets the clock frequency for a specific clock name.
- Clock_Ip_StatusType Clock_Ip_Init (Clock_Ip_ClockConfigType const *Config)

  Set clock configuration according to pre-defined structure.
- void Clock_Ip_InitClock (Clock_Ip_ClockConfigType const *Config)

  Set the PLL and other MCU specific clock options.
- Clock_Ip_PllStatusType Clock_Ip_GetPllStatus (void)

  Returns the lock status of the PLL.
- void Clock_Ip_DistributePll (void)

  Activates the PLL in MCU clock distribution.
- void Clock_Ip_InstallNotificationsCallback (Clock_Ip_NotificationsCallbackType Callback)

  Install a clock notifications callback.
- void Clock_Ip_ClearClockMonitorStatus (Clock_Ip_NameType ClockName)

  Clears status flags for a monitor clock.
- Clock_Ip_CmuStatusType Clock_Ip_GetClockMonitorStatus (Clock_Ip_NameType ClockName)

  Returns the clock monitor status.
- void Clock_Ip_DisableClockMonitor (Clock_Ip_NameType ClockName)

  Disables a clock monitor.
- void Clock_Ip_DisableModuleClock (Clock_Ip_NameType ClockName)

  Disables clock for a peripheral.
- void Clock_Ip_EnableModuleClock (Clock_Ip_NameType ClockName)

  Enables clock for a peripheral.
- void Clock_Ip_StartTimeout (uint32 *StartTimeOut, uint32 *ElapsedTimeOut, uint32 *TimeoutTicksOut, uint32 TimeoutUs)

  Initializes a starting reference point for timeout.
- boolean Clock_Ip_TimeoutExpired (uint32 *StartTimeInOut, uint32 *ElapsedTimeInOut, uint32 Timeout↩ Ticks)

  Checks for timeout condition.
- void Power_Ip_CM7_EnableSleepOnExit (void)

  The function enables SLEEPONEXIT bit.
- void Power_Ip_CM7_DisableSleepOnExit (void)

  The function disables SLEEPONEXIT bit.
- void Power_Ip_CortexM_WarmReset (void)

  The function request a Warm reset.
- void Power_Ip_CM7_DisableDeepSleep (void)

  The function disable SLEEPDEEP bit.
- void Power_Ip_CM7_EnableDeepSleep (void)

  The function enable SLEEPDEEP bit.
- void Power_Ip_MC_RGM_ResetInit (const Power_Ip_MC_RGM_ConfigType *ConfigPtr)

  This function initializes the Reset parameters.
- void Power_Ip_MC_RGM_PerformReset (const Power_Ip_MC_RGM_ConfigType *ConfigPtr)

  This function performs a microcontroller reset.
- Power_Ip_ResetType Power_Ip_MC_RGM_GetResetReason (void)

  This function returns the Reset reason.
- Power_Ip_RawResetType Power_Ip_MC_RGM_GetResetRawValue (void)

This function returns the Raw Reset value.

- void Power_Ip_MC_RGM_ModeConfig (const Power_Ip_MC_RGM_ModeConfigType *ModeConfigPtr)

  Request mode configuration from MC_RGM.
- void Power_Ip_MC_RGM_CheckModeConfig (const Power_Ip_MC_RGM_ModeConfigType *Mode↩ ConfigPtr)

  Check mode configuration from MC_RGM.
- void Power_Ip_MC_RGM_EnableResetDomain (const Power_Ip_MC_RGM_ModeConfigType *Mode↩ ConfigPtr)

  Enable interconnect interface of Software Reset Domain base on configuration of McuPartitionResetEnable.
- void Power_Ip_MC_RGM_DisableResetDomain (const Power_Ip_MC_RGM_ModeConfigType *Mode↩ ConfigPtr)

  Disable interconnect interface of Software Reset Domain base on configuration of McuPartitionResetEnable.
- void Power_Ip_PMC_PowerInit (const Power_Ip_PMC_ConfigType *ConfigPtr)

  This function configure the Power Management Controller.

6.1.2 Data Structure Documentation

6.1.2.1 struct Clock_Ip_ExtOSCType

XOSC - Register Layout Typedef

Definition at line 236 of file Clock_Ip_Specific.h.

Data Fields

Type	Name	Description
uint32	CTRL	XOSC Control Register, offset: 0x0
const uint32	STAT	Oscillator Status Register, offset: 0x4

6.1.2.2 struct Clock_Ip_ClockMonitorType

CMU - Register Layout Typedef

Definition at line 242 of file Clock_Ip_Specific.h.

Data Fields

Type	Name	Description
uint32	GCR	Global Configuration Register, offset: 0x0
uint32	RCCR	Reference Count Configuration Register, offset: 0x4
uint32	HTCR	High Threshold Configuration Register, offset: 0x8
uint32	LTCR	Low Threshold Configuration Register, offset: 0xC
volatile uint32	SR	Status Register, offset: 0x10
uint32	IER	Interrupt Enable Register, offset: 0x14

6.1.2.3 struct Clock_Ip_IrcoscConfigType

Clock Source IRCOSC configuration structure. Implements Clock_Ip_IrcoscConfigType_Class.

Definition at line 2641 of file Clock_Ip_Types.h.

Data Fields

Type	Name	Description
Clock_Ip_NameType	Name	Clock name associated to ircosc
uint16	Enable	Enable ircosc.
uint8	Regulator	Enable regulator.
uint8	Range	Ircosc range.
uint8	LowPowerModeEnable	Ircosc enable in VLP mode
uint8	StopModeEnable	Ircosc enable in STOP mode

6.1.2.4 struct Clock_Ip_XoscConfigType

CGM Clock Source XOSC configuration structure. Implements Clock_Ip_XoscConfigType_Class.

Definition at line 2657 of file Clock_Ip_Types.h.

Data Fields

Type	Name	Description
Clock_Ip_NameType	Name	Clock name associated to xosc
uint32	Freq	External oscillator frequency.
uint16	Enable	Enable xosc.
uint16	StartupDelay	Startup stabilization time.
uint8	BypassOption	XOSC bypass option
uint8	CompEn	Comparator enable
uint8	TransConductance	Crystal overdrive protection
uint8	Gain	Gain value
uint8	Monitor	Monitor type

6.1.2.5 struct Clock_Ip_PllConfigType

CGM Clock Source PLLDIG configuration structure. Implements Clock_Ip_PllConfigType_Class.

Definition at line 2680 of file Clock_Ip_Types.h.

Data Fields

Type	Name	Description
Clock_Ip_NameType	Name	Clock name associated to pll
uint16	Enable	Enable pll.
Clock_Ip_NameType	InputReference	Input reference.
uint8	Bypass	Bypass pll.
uint8	Predivider	Input clock predivider. (PREDIV)
uint16	NumeratorFracLoopDiv	Numerator of fractional loop division factor (MFN)
uint8	MulFactorDiv	Multiplication factor divider (MFD)
uint8	ModulationFrequency	Enable/disable modulation
uint8	ModulationType	Modulation type
uint16	ModulationPeriod	Stepsize - modulation period
uint16	IncrementStep	Stepno - step no
uint8	SigmaDelta	Sigma Delta Modulation Enable
uint8	DitherControl	Dither control enable
uint8	DitherControlValue	Dither control value
uint8	Monitor	Monitor type
uint16	Dividers[3U]	Dividers values

6.1.2.6 struct Clock_Ip_SelectorConfigType

Clock selector configuration structure. Implements Clock_Ip_SelectorConfigType_Class.

Definition at line 2714 of file Clock_Ip_Types.h.

Data Fields

Type	Name	Description
Clock_Ip_NameType	Name	Clock name associated to selector
Clock_Ip_NameType	Value	Name of the selected input source

6.1.2.7 struct Clock_Ip_DividerConfigType

Clock divider configuration structure. Implements Clock_Ip_DividerConfigType_Class.

Definition at line 2725 of file Clock_Ip_Types.h.

Data Fields

Type	Name	Description
Clock_Ip_NameType	Name	Clock name associated to divider.
uint32	Value	Divider value - if value is zero then divider is disabled.
uint8	Options[1U]	

6.1.2.8 struct Clock_Ip_DividerTriggerConfigType

Clock divider trigger configuration structure. Implements Clock_Ip_DividerTriggerConfigType_Class.

Definition at line 2736 of file Clock_Ip_Types.h.

Data Fields

Type	Name	Description
Clock_Ip_NameType	Name	Clock name associated to divider for which trigger is configured.
Clock_Ip_TriggerDividerType	TriggerType	Trigger value - if value is zero then divider is updated immediately, divider is not triggered.
Clock_Ip_NameType	Source	Clock name of the common input source of all dividers from the same group that support a common update

6.1.2.9 struct Clock_Ip_FracDivConfigType

Clock fractional divider configuration structure. Implements Clock_Ip_FracDivConfigType_Class.

Definition at line 2750 of file Clock_Ip_Types.h.

Data Fields

Type	Name	Description
Clock_Ip_NameType	Name	Clock name associated to fractional divider.
uint8	Enable	Enable control for port n
uint32	Value[2U]	Fractional dividers

6.1.2.10 struct Clock_Ip_ExtClkConfigType

Clock external clock configuration structure. Implements Clock_Ip_ExtClkConfigType_Class.

Definition at line 2762 of file Clock_Ip_Types.h.

Data Fields

Type	Name	Description
Clock_Ip_NameType	Name	Clock name of the external clock.
uint32	Value	Enable value - if value is zero then clock is gated, otherwise is enabled in different modes.

6.1.2.11 struct Clock_Ip_PcfsConfigType

Clock Source PCFS configuration structure. Implements Clock_Ip_PcfsConfigType_Class.

Definition at line 2773 of file Clock_Ip_Types.h.

Data Fields

Type	Name	Description
Clock_Ip_NameType	Name	Clock source from which ramp-down and to which ramp-up are processed.
uint32	MaxAllowableIDDchange	Maximum variation of current per time (mA/microsec) - max allowable IDD change is determined by the user's power supply design.
uint32	StepDuration	Step duration of each PCFS step
Clock_Ip_NameType	SelectorName	Name of the selector that supports PCFS and name is one the inputs that can be selected
uint32	ClockSourceFrequency	Frequency of the clock source from which ramp-down and to which ramp-up are processed.

6.1.2.12 struct Clock_Ip_GateConfigType

Clock gate clock configuration structure. Implements Clock_Ip_GateConfigType_Class.

Definition at line 2787 of file Clock_Ip_Types.h.

Data Fields

Type	Name	Description
Clock_Ip_NameType	Name	Clock name associated to clock gate.
uint16	Enable	Enable or disable clock

6.1.2.13 struct Clock_Ip_CmuConfigType

Clock cmu configuration structure. Implements Clock_Ip_CmuConfigType_Class.

Definition at line 2798 of file Clock_Ip_Types.h.

Data Fields

Type	Name	Description
Clock_Ip_NameType	Name	Clock name associated to clock monitor.
uint8	Enable	Enable/disable clock monitor
uint32	Interrupt	Enable/disable interrupt
uint32	MonitoredClockFrequency	Frequency of the clock source from which ramp-down and to which ramp-up are processed.

6.1.2.14 struct Clock_Ip_ConfiguredFrequencyType

Configured frequency structure. Implements Clock_Ip_ConfiguredFrequencyType_Class.

Definition at line 2810 of file Clock_Ip_Types.h.

Data Fields

Type	Name	Description
Clock_Ip_NameType	Name	Clock name of the configured frequency value
uint32	ConfiguredFrequencyValue	Configured frequency value

6.1.2.15 struct Clock_Ip_SpecificPerpihParamType

Clock Specific peripheral configure. Implements Clock_Ip_SpecificPerpihParamType_Class.

Definition at line 2820 of file Clock_Ip_Types.h.

6.1.2.16 struct Clock_IP_SpecificPeriphConfigType

Clock Specific peripheral structure. Implements Clock_IP_SpecificPeriphConfigType_Class.

Definition at line 2830 of file Clock_Ip_Types.h.

6.1.2.17 struct Clock_Ip_ClockConfigType

Clock configuration structure. Implements Clock_Ip_ClockConfigType_Class.

Definition at line 2840 of file Clock_Ip_Types.h.

Data Fields

Type	Name	Description
uint32	ClkConfigId	The ID for Clock configuration
uint8	IrcoscsCount	IRCOSCs count
uint8	XoscsCount	XOSCs count
uint8	PllsCount	PLLs count
uint8	SelectorsCount	Selectors count
uint8	DividersCount	Dividers count
uint8	DividerTriggersCount	Divider triggers count
uint8	FracDivsCount	Fractional dividers count
uint8	ExtClksCount	External clocks count
uint8	GatesCount	Clock gates count
uint8	PcfsCount	Clock pcfs count
uint8	CmusCount	Clock cmus count

Data Fields

Type	Name	Description
uint8	ConfigureFrequenciesCount	Configured frequencies count
Clock_Ip_IrcoscConfigType	Ircoscs[(2U)]	IRCOSCs
Clock_Ip_XoscConfigType	Xoscs[(1U)]	XOSCs
Clock_Ip_PllConfigType	Plls[(4U)]	PLLs
Clock_Ip_SelectorConfigType	Selectors[(32U)]	Selectors
Clock_Ip_DividerConfigType	Dividers[(33U)]	Dividers
Clock_Ip_DividerTriggerConfigType	DividerTriggers[1U]	Divider triggers
Clock_Ip_FracDivConfigType	FracDivs[(12U)]	Fractional dividers
Clock_Ip_ExtClkConfigType	ExtClks[(24U)]	External clocks
Clock_Ip_GateConfigType	Gates[(9U)]	Clock gates
Clock_Ip_PcfsConfigType	Pcfs[(3U)]	Progressive clock switching
Clock_Ip_CmuConfigType	Cmus[(28U)]	Clock cmus
Clock_IP_SpecificPeriphConfigType	SpecificPeriphalConfiguration	Clock specific peripheral configuration
Clock_Ip_ConfiguredFrequencyType	ConfiguredFrequencies[(4U)]	Configured frequency values

6.1.3 Macro Definition Documentation

6.1.3.1 CLOCK_IP_NO_PLL

```
#define CLOCK_IP_NO_PLL
```

This parameter shall be set True, if the H/W does not have a PLL.

Definition at line 196 of file Clock_Ip_Types.h.

6.1.4 Types Reference

6.1.4.1 Clock_Ip_NotificationsCallbackType

```
typedef void(* Clock_Ip_NotificationsCallbackType) (Clock_Ip_NotificationType Error, Clock_Ip_NameType
ClockName)
```

Clock notifications callback type. Implements ClockNotificationsCallbackType_Class.

Definition at line 2635 of file Clock_Ip_Types.h.

6.1.5 Enum Reference

6.1.5.1 Clock_Ip_ClockNameSourceType

```
enum Clock_Ip_ClockNameSourceType
```

Clock ip source type.

Enumerator

UKNOWN_TYPE	Clock path from source to this clock name has at least one selector.
IRCOSC_TYPE	Source is an internal oscillator.
XOSC_TYPE	Source is an external oscillator.
PLL_TYPE	Source is a pll.
EXT_CLK_TYPE	Source is an external clock.
SERDES_TYPE	Source is a SERDES.

Definition at line 237 of file Clock_Ip_Private.h.

6.1.5.2 Clock_Ip_PllStatusReturnType

enum Clock_Ip_PllStatusReturnType

Clock pll status return codes.

Enumerator

STATUS_PLL_NOT_ENABLED	Not enabled
STATUS_PLL_UNLOCKED	Unlocked
STATUS_PLL_LOCKED	Locked

Definition at line 251 of file Clock_Ip_Private.h.

6.1.5.3 Clock_Ip_DfsStatusType

enum Clock_Ip_DfsStatusType

Clock dfs status return codes.

Enumerator

STATUS_DFS_NOT_ENABLED	Not enabled
STATUS_DFS_UNLOCKED	Unlocked
STATUS_DFS_LOCKED	Locked

Definition at line 261 of file Clock_Ip_Private.h.

6.1.5.4 Clock_Ip_PowerModesType

enum Clock_Ip_PowerModesType

Power modes.

Definition at line 205 of file Clock_Ip_Types.h.

6.1.5.5 Clock_Ip_PowerNotificationType

enum Clock_Ip_PowerNotificationType

Power mode notification.

Definition at line 216 of file Clock_Ip_Types.h.

6.1.5.6 Clock_Ip_NameType

enum Clock_Ip_NameType

Clock names.

Definition at line 226 of file Clock_Ip_Types.h.

6.1.5.7 Clock_Ip_StatusType

enum Clock_Ip_StatusType

Clock ip status return codes.

Enumerator

CLOCK_IP_SUCCESS	Clock tree was initialized successfully.
CLOCK_IP_ERROR	One of the elements timeout, clock tree couldn't be initialized.

Definition at line 2574 of file Clock_Ip_Types.h.

6.1.5.8 Clock_Ip_PllStatusType

enum Clock_Ip_PllStatusType

Clock ip pll status return codes.

Enumerator

CLOCK_IP_PLL_LOCKED	PLL is locked
CLOCK_IP_PLL_UNLOCKED	PLL is unlocked
CLOCK_IP_PLL_STATUS_UNDEFINED	PLL Status is unknown

Definition at line 2582 of file Clock_Ip_Types.h.

6.1.5.9 Clock_Ip_CmuStatusType

enum Clock_Ip_CmuStatusType

Clock ip cmu status return codes.

Enumerator

CLOCK_IP_CMU_IN_RANGE	Frequency is in range
CLOCK_IP_CMU_HIGH_FREQ	Frequency is higher than high limit
CLOCK_IP_CMU_LOW_FREQ	Frequency is lower than low limit
CLOCK_IP_CMU_STATUS_UNDEFINED	CMU status is unknown

Definition at line 2591 of file Clock_Ip_Types.h.

6.1.5.10 Clock_Ip_NotificationType

enum Clock_Ip_NotificationType

Clock ip report error types.

Enumerator

CLOCK_IP_CMU_ERROR	Cmu Fccu notification.
CLOCK_IP_REPORT_TIMEOUT_ERROR	Report Timeout Error.
CLOCK_IP_REPORT_FXOSC_CONFIGURATION_ERROR	Report Fxosc Configuration Error.
CLOCK_IP_REPORT_CLOCK_MUX_SWITCH_ERROR	Report Clock Mux Switch Error.

Enumerator

CLOCK_IP_RAM_MEMORY_CONFIG_ENTRY	Ram config entry point.
CLOCK_IP_RAM_MEMORY_CONFIG_EXIT	Ram config exit point.
CLOCK_IP_FLASH_MEMORY_CONFIG_ENTRY	Flash config entry point.
CLOCK_IP_FLASH_MEMORY_CONFIG_EXIT	Flash config exit point.
CLOCK_IP_ACTIVE	Report Clock Active.
CLOCK_IP_INACTIVE	Report Clock Inactive.

Definition at line 2600 of file Clock_Ip_Types.h.

6.1.5.11 Clock_Ip_TriggerDividerType

```
enum Clock_Ip_TriggerDividerType
```

Clock ip trigger divider type.

Enumerator

IMMEDIATE_DIVIDER_UPDATE	Immediate divider update.
COMMON_TRIGGER_DIVIDER_UPDATE	Common trigger divider update.

Definition at line 2615 of file Clock_Ip_Types.h.

6.1.5.12 Clock_Ip_SpecificPeriphParamType

```
enum Clock_Ip_SpecificPeriphParamType
```

specific peripheral.

Definition at line 2623 of file Clock_Ip_Types.h.

6.1.6 Function Reference

6.1.6.1 Clock_Ip_GetClockFrequency()

```
uint32 Clock_Ip_GetClockFrequency (
            Clock_Ip_NameType ClockName )
```

Gets the clock frequency for a specific clock name.

This function checks the current clock configurations and then calculates the clock frequency for a specific clock name defined in Clock_Ip_NameType. Clock modules must be properly configured before using this function. See features.h for supported clock names for different chip families. The returned value is in Hertz. If frequency is required for a peripheral and the module is not clocked, then 0 Hz frequency is returned.

Parameters

in	*ClockName*	Clock names defined in Clock_Ip_NameType

Returns

frequency Returned clock frequency value in Hertz

6.1.6.2 Clock_Ip_Init()

```
Clock_Ip_StatusType Clock_Ip_Init (
            Clock_Ip_ClockConfigType const * Config )
```

Set clock configuration according to pre-defined structure.

This function sets system to target clock configuration; It sets the clock modules registers for clock mode change.

Parameters

in	*Config*	Pointer to configuration structure.

Returns

void

Note

If external clock is used in the target mode, please make sure it is enabled, for example, if the external oscillator is used, please setup correctly.

6.1.6.3 Clock_Ip_InitClock()

```
void Clock_Ip_InitClock (
            Clock_Ip_ClockConfigType const * Config )
```

Set the PLL and other MCU specific clock options.

This function initializes the PLL and other MCU specific clock options. The clock configuration parameters are provided via the configuration structure.

This function shall start the PLL lock procedure (if PLL shall be initialized) and shall return without waiting until the PLL is locked.

Parameters

in	*Config*	Pointer to configuration structure.

Returns

void

6.1.6.4 Clock_Ip_GetPllStatus()

```
Clock_Ip_PllStatusType Clock_Ip_GetPllStatus (
            void  )
```

Returns the lock status of the PLL.

This function returns status of the PLL: undefined, unlocked or locked. This function returns undefined status if this function is called prior to calling of the function Clock_Ip_InitClock

Returns

Status. Pll lock status

6.1.6.5 Clock_Ip_DistributePll()

```
void Clock_Ip_DistributePll (
            void  )
```

Activates the PLL in MCU clock distribution.

This function activates the PLL clock to the MCU clock distribution.

This function removes the current clock source (for example internal oscillator clock) from MCU clock distribution.

Application layer calls this function after the status of the PLL has been detected as locked by the function Clock↩_Ip_GetPllStatus.

The function Clock_Ip_DistributePll shall return without affecting the MCU hardware if the PLL clock has been automatically activated by the MCU hardware.

Returns

void

6.1.6.6 Clock_Ip_InstallNotificationsCallback()

```
void Clock_Ip_InstallNotificationsCallback (
            Clock_Ip_NotificationsCallbackType Callback )
```

Install a clock notifications callback.

This function installs a callback for reporting notifications from clock driver

Parameters

in	*Clock_Ip_NotificationsCallbackType*	notifications callback

Returns

void

6.1.6.7 Clock_Ip_ClearClockMonitorStatus()

```
void Clock_Ip_ClearClockMonitorStatus (
            Clock_Ip_NameType ClockName )
```

Clears status flags for a monitor clock.

This function clears status flags for a monitor clock.

Parameters

in	*ClockName*	Clock Name.

Returns

void

6.1.6.8 Clock_Ip_GetClockMonitorStatus()

```
Clock_Ip_CmuStatusType Clock_Ip_GetClockMonitorStatus (
            Clock_Ip_NameType ClockName )
```

Returns the clock monitor status.

This function returns status of the clock monitor: undefined, lower, higher, in range. This function returns undefined status if this function is called when corresponding cmu is not enabled.

Returns

Status. Cmu status

6.1.6.9 Clock_Ip_DisableClockMonitor()

```
void Clock_Ip_DisableClockMonitor (
             Clock_Ip_NameType ClockName )
```

Disables a clock monitor.

This function disables a clock monitor.

Parameters

in	*ClockName*	Clock Name.

Returns

void

6.1.6.10 Clock_Ip_DisableModuleClock()

```
void Clock_Ip_DisableModuleClock (
            Clock_Ip_NameType ClockName )
```

Disables clock for a peripheral.

This function disables clock for a peripheral.

Parameters

in	*ClockName*	Clock Name.

Returns

void

6.1.6.11 Clock_Ip_EnableModuleClock()

```
void Clock_Ip_EnableModuleClock (
            Clock_Ip_NameType ClockName )
```

Enables clock for a peripheral.

This function enables clock for a peripheral.

Parameters

in	*ClockName*	Clock Name.

Returns

void

6.1.6.12 Clock_Ip_StartTimeout()

```
void Clock_Ip_StartTimeout (
            uint32 * StartTimeOut,
            uint32 * ElapsedTimeOut,
            uint32 * TimeoutTicksOut,
            uint32 TimeoutUs )
```

Initializes a starting reference point for timeout.

Parameters

out	*StartTimeOut*	The starting time from which elapsed time is measured
out	*ElapsedTimeOut*	The elapsed time to be passed to Clock_Ip_TimeoutExpired
out	*TimeoutTicksOut*	The timeout value (in ticks) to be passed to Clock_Ip_TimeoutExpired
in	*TimeoutUs*	The timeout value (in microseconds)

6.1.6.13 Clock_Ip_TimeoutExpired()

```
boolean Clock_Ip_TimeoutExpired (
            uint32 * StartTimeInOut,
            uint32 * ElapsedTimeInOut,
            uint32 TimeoutTicks )
```

Checks for timeout condition.

Parameters

in,out	*StartTimeInOut*	The starting time from which elapsed time is measured
in,out	*ElapsedTimeInOut*	The accumulated elapsed time from the starting time reference
in	*TimeoutTicks*	The timeout limit (in ticks)

6.1.6.14 Power_Ip_CM7_EnableSleepOnExit()

```
void Power_Ip_CM7_EnableSleepOnExit (
            void  )
```

The function enables SLEEPONEXIT bit.

Parameters

None	

Returns

None

6.1.6.15 Power_Ip_CM7_DisableSleepOnExit()

```
void Power_Ip_CM7_DisableSleepOnExit (
             void  )
```

The function disables SLEEPONEXIT bit.

Parameters

None	

Returns

None

6.1.6.16 Power_Ip_CortexM_WarmReset()

```
void Power_Ip_CortexM_WarmReset (
             void  )
```

The function request a Warm reset.

Parameters

None	

Returns

None

6.1.6.17 Power_Ip_CM7_DisableDeepSleep()

```
void Power_Ip_CM7_DisableDeepSleep (
            void  )
```

The function disable SLEEPDEEP bit.

Parameters

in	*none*	

Returns

void

6.1.6.18 Power_Ip_CM7_EnableDeepSleep()

```
void Power_Ip_CM7_EnableDeepSleep (
            void  )
```

The function enable SLEEPDEEP bit.

Parameters

in	*none*	

Returns

void

6.1.6.19 Power_Ip_MC_RGM_ResetInit()

```
void Power_Ip_MC_RGM_ResetInit (
            const Power_Ip_MC_RGM_ConfigType * ConfigPtr )
```

This function initializes the Reset parameters.

Parameters

ConfigPtr	Pointer to the MC_RGM configuration structure.

Returns

None

6.1.6.20 Power_Ip_MC_RGM_PerformReset()

```
void Power_Ip_MC_RGM_PerformReset (
            const Power_Ip_MC_RGM_ConfigType * ConfigPtr )
```

This function performs a microcontroller reset.

Parameters

ConfigPtr	Pointer to the MC_RGM configuration structure.

Returns

None

6.1.6.21 Power_Ip_MC_RGM_GetResetReason()

```
Power_Ip_ResetType Power_Ip_MC_RGM_GetResetReason (
            void  )
```

This function returns the Reset reason.

Parameters

None	

Returns

Reason of the Reset event.

6.1.6.22 Power_Ip_MC_RGM_GetResetRawValue()

```
Power_Ip_RawResetType Power_Ip_MC_RGM_GetResetRawValue (
            void  )
```

This function returns the Raw Reset value.

Parameters

None	

Returns

Implementation-specific value with the Reset status.

6.1.6.23 Power_Ip_MC_RGM_ModeConfig()

```
void Power_Ip_MC_RGM_ModeConfig (
            const Power_Ip_MC_RGM_ModeConfigType * ModeConfigPtr )
```

Request mode configuration from MC_RGM.

Parameters

MC_RGM	Mode Domain Settings.

Returns

None

6.1.6.24 Power_Ip_MC_RGM_CheckModeConfig()

```
void Power_Ip_MC_RGM_CheckModeConfig (
            const Power_Ip_MC_RGM_ModeConfigType * ModeConfigPtr )
```

Check mode configuration from MC_RGM.

Parameters

MC_RGM	Mode Domain Settings.

Returns

None

6.1.6.25 Power_Ip_MC_RGM_EnableResetDomain()

```
void Power_Ip_MC_RGM_EnableResetDomain (
            const Power_Ip_MC_RGM_ModeConfigType * ModeConfigPtr )
```

Enable interconnect interface of Software Reset Domain base on configuration of McuPartitionResetEnable.

Parameters

MC_RGM	Mode Domain Settings.

Returns

None

6.1.6.26 Power_Ip_MC_RGM_DisableResetDomain()

```
void Power_Ip_MC_RGM_DisableResetDomain (
            const Power_Ip_MC_RGM_ModeConfigType * ModeConfigPtr )
```

Disable interconnect interface of Software Reset Domain base on configuration of McuPartitionResetEnable.

Parameters

MC_RGM	Mode Domain Settings.

Returns

None

6.1.6.27 Power_Ip_PMC_PowerInit()

```
void Power_Ip_PMC_PowerInit (
            const Power_Ip_PMC_ConfigType * ConfigPtr )
```

This function configure the Power Management Controller.

Parameters

ConfigPtr	Pointer to PMC configuration structure.

Returns

None

6.2 Mcu Driver

6.2.1 Detailed Description

Data Structures

- struct Mcu_ConfigType

  Initialization data for the MCU driver. More...
- struct Mcu_MidrReturnType

  MIDR configuration. More...

Macros

- #define MCU_VENDOR_ID

  Import all data types from lower layers that should be exported. Mcu.h shall include Mcu_Cfg.h for the API pre-compiler switches.

Types Reference

- typedef Power_Ip_HwIPsConfigType Mcu_HwIPsConfigType

  Mcu driver configuration structure.
- typedef Clock_Ip_ClockConfigType Mcu_ClockConfigType

  Definition of a Clock configuration.
- typedef Ram_Ip_RamConfigType Mcu_RamConfigType

  Definition of a Clock configuration.
- typedef Power_Ip_ModeConfigType Mcu_ModeConfigType

  Definition of a Mode configuration.

Enum Reference

- enum Mcu_ClockNotificationType

  Mcu_ClockNotificationType.

Function Reference

- void Mcu_Init (const Mcu_ConfigType *ConfigPtr)
  MCU driver initialization function.
- Std_ReturnType Mcu_InitRamSection (Mcu_RamSectionType RamSection)
  MCU driver initialization of Ram sections.
- Std_ReturnType Mcu_InitClock (Mcu_ClockType ClockSetting)
  MCU driver clock initialization function.
- void Mcu_SetMode (Mcu_ModeType McuMode)
  This function sets the MCU power mode.
- Std_ReturnType Mcu_DistributePllClock (void)
  This function activates the PLL clock to the MCU clock distribution.
- Mcu_PllStatusType Mcu_GetPllStatus (void)
  This function returns the lock status of the PLL.
- Mcu_ResetType Mcu_GetResetReason (void)
  This function returns the Reset reason.
- Mcu_RawResetType Mcu_GetResetRawValue (void)
  This function returns the Raw Reset value.
- void Mcu_PerformReset (void)
  This function performs a microcontroller reset.
- void Mcu_GetVersionInfo (Std_VersionInfoType *versioninfo)
  This function returns the Version Information for the MCU module.
- Mcu_RamStateType Mcu_GetRamState (void)
  This function returns the actual state of the RAM.
- void Mcu_GetMidrStructure (Mcu_MidrReturnType MidrPtr[((uint8) 2U)])
  This function returns the value of the MIDR registers.
- void Mcu_DisableCmu (Clock_Ip_NameType ClockName)
  Disable clock monitoring unit.
- uint32 Mcu_GetClockFrequency (Clock_Ip_NameType ClockName)
  Return the frequency of a given clock.
- void Mcu_SleepOnExit (Mcu_SleepOnExitType SleepOnExit)
  This function disable/enable SleepOnExit.

Variables

- const Mcu_ConfigType * Mcu_pConfigPtr
  Local copy of the pointer to the configuration data.

6.2.2 Data Structure Documentation

6.2.2.1 struct Mcu_ConfigType

Initialization data for the MCU driver.

A pointer to such a structure is provided to the MCU initialization routines for configuration.

Definition at line 170 of file Mcu.h.

Data Fields

- Mcu_ClockNotificationType ClkSrcFailureNotification
  Clock source failure notification enable configuration.
- Mcu_RamSectionType NoRamConfigs
  Total number of MCU modes.
- Mcu_ModeType NoModeConfigs
  Total number of MCU clock configurations.
- const Mcu_RamConfigType(* RamConfigArrayPtr)[((uint32) 1U)]
  RAM data configuration.
- const Mcu_ModeConfigType(* ModeConfigArrayPtr)[((uint32) 9U)]
  Clock data configuration.
- const Mcu_HwIPsConfigType * HwIPsConfigPtr
  IPs data generic configuration.

6.2.2.1.1 Field Documentation

6.2.2.1.1.1 ClkSrcFailureNotification `Mcu_ClockNotificationType ClkSrcFailureNotification`

Clock source failure notification enable configuration.

<

Total number of RAM sections.

Definition at line 174 of file Mcu.h.

6.2.2.1.1.2 NoRamConfigs `Mcu_RamSectionType NoRamConfigs`

Total number of MCU modes.

Definition at line 182 of file Mcu.h.

6.2.2.1.1.3 NoModeConfigs `Mcu_ModeType NoModeConfigs`

Total number of MCU clock configurations.

Definition at line 185 of file Mcu.h.

6.2.2.1.1.4 RamConfigArrayPtr `const Mcu_RamConfigType(* RamConfigArrayPtr)[((uint32) 1U)]`

RAM data configuration.

<

Power Modes data configuration.

Definition at line 193 of file Mcu.h.

6.2.2.1.1.5 ModeConfigArrayPtr `const Mcu_ModeConfigType(* ModeConfigArrayPtr)[((uint32) 9U)]`

Clock data configuration.

Definition at line 197 of file Mcu.h.

6.2.2.1.1.6 HwIPsConfigPtr `const Mcu_HwIPsConfigType* HwIPsConfigPtr`

IPs data generic configuration.

<

Definition at line 204 of file Mcu.h.

6.2.2.2 struct Mcu_MidrReturnType

MIDR configuration.

Definition at line 237 of file Mcu_Ipw_Types.h.

Data Fields

Type	Name	Description
uint32	Midr1	SIUL2_MIDR1 Configuration register.
uint32	Midr2	SIUL2_MIDR2 Configuration register.

6.2.3 Macro Definition Documentation

6.2.3.1 MCU_VENDOR_ID

```
#define MCU_VENDOR_ID
```

Import all data types from lower layers that should be exported. Mcu.h shall include Mcu_Cfg.h for the API pre-compiler switches.

Definition at line 64 of file Mcu.h.

6.2.4 Types Reference

6.2.4.1 Mcu_HwIPsConfigType

```
typedef Power_Ip_HwIPsConfigType Mcu_HwIPsConfigType
```

Mcu driver configuration structure.

Configuration for SIU reset configuration module. Configuration for power management and SSCM. Configuration for FLASH controller. Used by "Mcu_ConfigType" structure.

Definition at line 194 of file Mcu_Ipw_Types.h.

6.2.4.2 Mcu_ClockConfigType

```
typedef Clock_Ip_ClockConfigType Mcu_ClockConfigType
```

Definition of a Clock configuration.

This configuration is transmitted as parameter to Mcu_Ipw_InitClock() API. Used by "Mcu_ConfigType" structure.

Note

The structure Mcu_ConfigType shall provide a configurable (enable/ disable) clock failure notification if the MCU provides an interrupt for such detection.

Definition at line 207 of file Mcu_Ipw_Types.h.

6.2.4.3 Mcu_RamConfigType

```
typedef Ram_Ip_RamConfigType Mcu_RamConfigType
```

Definition of a Clock configuration.

This configuration is transmitted as parameter to Mcu_Ipw_InitClock() API. Used by "Mcu_ConfigType" structure.

Note

The structure Mcu_ConfigType shall provide a configurable (enable/ disable) clock failure notification if the MCU provides an interrupt for such detection.

Definition at line 220 of file Mcu_Ipw_Types.h.

6.2.4.4 Mcu_ModeConfigType

```
typedef Power_Ip_ModeConfigType Mcu_ModeConfigType
```

Definition of a Mode configuration.

This configuration is transmitted as parameter to Mcu_Ipw_SetMode() API. Used by "Mcu_ConfigType" structure.

Definition at line 229 of file Mcu_Ipw_Types.h.

6.2.5 Enum Reference

6.2.5.1 Mcu_ClockNotificationType

```
enum Mcu_ClockNotificationType
```

Mcu_ClockNotificationType.

Clock failure notification. Enable/disable clock failure interrupt generated by the MCU.

Enumerator

MCU_CLK_NOTIF_DIS	Disable clock notification.
MCU_CLK_NOTIF_EN	Enable clock notification.

Definition at line 173 of file Mcu_Ipw_Types.h.

6.2.6 Function Reference

6.2.6.1 Mcu_Init()

```
void Mcu_Init (
            const Mcu_ConfigType * ConfigPtr )
```

MCU driver initialization function.

This routine initializes the MCU Driver. The intention of this function is to make the configuration setting for power down, clock and Ram sections visible within the MCU Driver.

Parameters

in	*ConfigPtr*	Pointer to configuration structure.

Returns

void

6.2.6.2 Mcu_InitRamSection()

```
Std_ReturnType Mcu_InitRamSection (
            Mcu_RamSectionType RamSection )
```

MCU driver initialization of Ram sections.

Function initializes the ram section selected by RamSection parameter. The section base address, size and value to be written are provided from the configuration structure. The function will write the value specified in the configuration structure indexed by RamSection. After the write it will read back the RAM to verify that the requested value was written.

Parameters

in	*RamSection*	Index of ram section from configuration structure to be initialized.

Returns

Command has or has not been accepted.

Return values

E_OK	Valid parameter, the driver state allowed execution and the RAM check was successful
E_NOT_OK	Invalid parameter, the driver state did not allowed execution or the RAM check was not successful

6.2.6.3 Mcu_InitClock()

```
Std_ReturnType Mcu_InitClock (
            Mcu_ClockType ClockSetting )
```

MCU driver clock initialization function.

This function intializes the PLL and MCU specific clock options. The clock setting is provided from the configuration structure.

Parameters

in	*ClockSetting*	Clock setting ID from config structure to be used.

Returns

Command has or has not been accepted.

Return values

E_OK	The driver state allowed the execution of the function and the provided parameter was in range
E_NOT_OK	The driver state did not allowed execution or the parameter was invalid

6.2.6.4 Mcu_SetMode()

```
void Mcu_SetMode (
            Mcu_ModeType McuMode )
```

This function sets the MCU power mode.

This function activates MCU power mode from config structure selected by McuMode parameter. If the driver state is invalid or McuMode is not in range the function will skip changing the mcu mode.

Parameters

in	*McuMode*	MCU mode setting ID from config structure to be set.

Returns

void

6.2.6.5 Mcu_DistributePllClock()

```
Std_ReturnType Mcu_DistributePllClock (
            void  )
```

This function activates the PLL clock to the MCU clock distribution.

Function completes the PLL configuration and then activates the PLL clock to MCU. If the MCU_NO_PLL is TRUE the Mcu_DistributePllClock has to be disabled. The function will not distribute the PLL clock if the driver state does not allow it, or the PLL is not stable.

Returns

Std_ReturnType

Return values

E_OK	Command has been accepted.
E_NOT_OK	Command has not been accepted.

6.2.6.6 Mcu_GetPllStatus()

```
Mcu_PllStatusType Mcu_GetPllStatus (
            void  )
```

This function returns the lock status of the PLL.

The user takes care that the PLL is locked by executing Mcu_GetPllStatus. If the MCU_NO_PLL is TRUE the MCU_GetPllStatus has to return MCU_PLL_STATUS_UNDEFINED. It will also return MCU_PLL_STATUS↩ _UNDEFINED if the driver state was invalid

Returns

Mcu_PllStatusType Provides the lock status of the PLL.

Return values

MCU_PLL_STATUS_UNDEFINED	PLL Status is unknown.
MCU_PLL_LOCKED	PLL is locked.
MCU_PLL_UNLOCKED	PLL is unlocked.

6.2.6.7 Mcu_GetResetReason()

```
Mcu_ResetType Mcu_GetResetReason (
            void  )
```

This function returns the Reset reason.

This routine returns the Reset reason that is read from the hardware.

Returns

Mcu_ResetType Reason of the Reset event.

6.2.6.8 Mcu_GetResetRawValue()

```
Mcu_RawResetType Mcu_GetResetRawValue (
            void  )
```

This function returns the Raw Reset value.

This routine returns the Raw Reset value that is read from the hardware.

Returns

Mcu_RawResetType Description of the returned value.

Return values

uint32	Code of the Raw reset value.

6.2.6.9 Mcu_PerformReset()

```
void Mcu_PerformReset (
            void  )
```

This function performs a microcontroller reset.

This function performs a microcontroller reset by using the hardware feature of the microcontroller. In case the function returns, the user must reset the platform using an alternate reset mechanism

Returns

void

6.2.6.10 Mcu_GetVersionInfo()

```
void Mcu_GetVersionInfo (
            Std_VersionInfoType * versioninfo )
```

This function returns the Version Information for the MCU module.

This function returns the vendor id, module id, major, minor and patch version.

Parameters

in,out	*versioninfo*	A pointer to a variable to store version info.

Returns

void

6.2.6.11 Mcu_GetRamState()

```
Mcu_RamStateType Mcu_GetRamState (
            void  )
```

This function returns the actual state of the RAM.

This function returns if the Ram Status is valid after a reset. The report is get from STCU as a result of MBIST (Memory Built-In Self Tests).

Returns

Mcu_RamStateType Status of the Ram Content.

Return values

MCU_RAMSTATE_INVALID	Ram state is not valid or unknown (default), or the driver state does not allow this call.
MCU_RAMSTATE_VALID	Ram state is valid.

6.2.6.12 Mcu_GetMidrStructure()

```
void Mcu_GetMidrStructure (
            Mcu_MidrReturnType MidrPtr[((uint8) 2U)] )
```

This function returns the value of the MIDR registers.

This function returns the platform dependent Mcu_MidrReturnType structure witch contains the MIDRn registers.

Parameters

in,out	*MidrPtr*	A pointer to a variable to store the Mcu_MidrReturnType structure.

Returns

void

6.2.6.13 Mcu_DisableCmu()

```
void Mcu_DisableCmu (
            Clock_Ip_NameType ClockName )
```

Disable clock monitoring unit.

This function disables the selected clock monitoring unit.

Precondition

Function requires an execution of Mcu_Init() before it can be used.

Parameters

in	*ClockName*	Name of the monitor clock for which CMU must be disabled.

Returns

void

6.2.6.14 Mcu_GetClockFrequency()

```
uint32 Mcu_GetClockFrequency (
            Clock_Ip_NameType ClockName )
```

Return the frequency of a given clock.

This function returns the frequency of a given clock which is request by user.

Precondition

Function requires an execution of Mcu_Init() before it can be used,

Parameters

in	*ClockName*	Name of the monitor clock for which CMU must be disabled.

Returns

uint32

6.2.6.15 Mcu_SleepOnExit()

```
void Mcu_SleepOnExit (
            Mcu_SleepOnExitType SleepOnExit )
```

This function disable/enable SleepOnExit.

Disable/enable Sleep on exit when returning from Handler mode to Thread mode.

Parameters

in	*Mcu_SleepOnExitType*	The value will be configured to SLEEPONEXIT bits. MCU_SLEEP_ON_EXIT_DISABLED - Disable SLEEPONEXIT bit. MCU_SLEEP_ON_EXIT_ENABLED - Enable SLEEPONEXIT bit.

Returns

void

6.2.7 Variable Documentation

6.2.7.1 Mcu_pConfigPtr

```
const Mcu_ConfigType* Mcu_pConfigPtr  [extern]
```

Local copy of the pointer to the configuration data.

6.3 Power Ip Driver

6.3.1 Detailed Description

Data Structures

- struct Power_Ip_MC_ME_CoreConfigType
  MC_ME Core Configuration. *More...*
- struct Power_Ip_MC_ME_CofbConfigType
  MC_ME COFB Configuration. *More...*
- struct Power_Ip_MC_ME_PartitionConfigType
  MC_ME Partition Configuration. *More...*
- struct Power_Ip_MC_ME_ModeConfigType
  MC_ME IP Configuration. *More...*
- struct Power_Ip_MC_RGM_ConfigType
  Configuration of MC_RGM hardware IP. *More...*
- struct Power_Ip_MC_RGM_CoreConfigType

MC_RGM Core Reset Configuration. More...

- struct Power_Ip_MC_RGM_CofbConfigType

  MC_RGM COFB Configuration. More...
- struct Power_Ip_MC_RGM_DomainConfigType

  MC_RGM Domain Configuration. More...
- struct Power_Ip_MC_RGM_ModeConfigType

  MC_RGM IP Mode Configuration. More...
- struct Power_Ip_PMC_ConfigType

  Configuration for PMC. More...
- struct Power_Ip_MC_RGM_Type

Macros

- #define IP_CM_AIRCR
- #define CM_AIRCR_VECTKEY(x)
- #define MCU_RAW_RESET_DEFAULT

  The function Mcu_GetResetRawValue shall return an implementation specific value which does not correspond to a valid value of the reset status register and is not equal to 0 if this function is called prior to calling of the function Mcu_Init, and if supported by the hardware.
- #define POWER_IP_FIRST_RESET_REASON_POS

  This macro is used to define the position of the first reset reason.
- #define POWER_IP_RESET_DOMAIN_COUNT
- #define POWER_IP_RESET_INSTANCE_COUNT
- #define POWER_IP_MC_RGM_PRST_COUNT

Types Reference

- typedef uint32 Power_Ip_RawResetType

  The type Mcu_RawResetType specifies the reset reason in raw register format, read from a reset status register.
- typedef uint32 Power_Ip_ModeType

  The Mcu_ModeType specifies the identification (ID) for a MCU mode, configured via configuration structure.
- typedef void(∗ Power_Ip_ReportErrorsCallbackType) (Power_Ip_ReportErrorType Error, uint8 ErrorCode)

  Power report error callback structure. Implements PowerReportErrorCallbackType_Class.

Enum Reference

- enum Power_Ip_MC_RGM_ResetType

  Reset type to be performed through the Mcu_PerformReset() API.
- enum Power_MC_RGM_StatusType
- enum Power_Ip_MSCM_CpxType

  Type of the return value of the function Mcu_GetCpxType.
- enum Power_Ip_PowerModeType

  Power Modes encoding.
- enum Power_Ip_ReportErrorType

  Power ip report error types.

Function Reference

- void Power_Ip_Init (const Power_Ip_HwIPsConfigType *HwIPsConfigPtr)
  Power initialization.
- void Power_Ip_SetMode (const Power_Ip_ModeConfigType *ModeConfigPtr)
  Sets mode.
- Power_Ip_PowerModeType Power_Ip_GetPreviousMode (void)
  This function returns the previous mode.
- void Power_Ip_PerformReset (const Power_Ip_HwIPsConfigType *HwIPsConfigPtr)
  Performs reset.
- Power_Ip_ResetType Power_Ip_GetResetReason (void)
  Returns reset type.
- Power_Ip_RawResetType Power_Ip_GetResetRawValue (void)
  Returns raw reset type.
- void Power_Ip_InstallNotificationsCallback (Power_Ip_ReportErrorsCallbackType ReportErrorsCallback)
  Install report error callback.
- void Power_Ip_StartTimeout (uint32 *StartTimeOut, uint32 *ElapsedTimeOut, uint32 *TimeoutTicksOut, uint32 TimeoutUs)
  Initializes a starting reference point for timeout.
- boolean Power_Ip_TimeoutExpired (uint32 *StartTimeInOut, uint32 *ElapsedTimeInOut, uint32 Timeout↩ Ticks)
  Checks for timeout condition.

6.3.2 Data Structure Documentation

6.3.2.1 struct Power_Ip_MC_ME_CoreConfigType

MC_ME Core Configuration.

This structure contains information for configuring the cores. The definitions for each Core setting within the structure Power_Ip_MC_ME_CoreConfigType shall contain:

- The index of the Core (within its partition).
- The boot address of the Core.
- Power management information (i.e. start or shutdown the Core).

Definition at line 183 of file Power_Ip_MC_ME_Types.h.

Data Fields

Type	Name	Description
boolean	CoreUnderMcuControl	Specifies whether the given core is under MCU control. The index of the core within the partition.
uint8	CoreIndex	The boot address of the core.
uint32 *	CoreBootAddress	
464uint32	CorePconfRegValue	The process configuration register value of the core.

6.3.2.2 struct Power_Ip_MC_ME_CofbConfigType

MC_ME COFB Configuration.

This structure contains information for configuring the COFBs (Collection of Functional Blocks). The definitions for each COFB setting within the structure Power_Ip_MC_ME_CofbConfigType shall contain:

- The index of the COFB (within its partition).
- The list of peripherals enable/disable (i.e. the value of the PRTNx_COFBx_CLKEN register).

Definition at line 206 of file Power_Ip_MC_ME_Types.h.

Data Fields

Type	Name	Description
boolean	CofbUnderMcuControl	Specifies whether the given COFB set is under MCU control. < The index of the COFB set within the partition.
uint8	CofbIndex	
uint32	CofbClkenRegValue	The clock enable register value of the COFB set.
uint32	CofbBlocksToUpdateMask	Mask containing the COFB blocks to be updated.

6.3.2.3 struct Power_Ip_MC_ME_PartitionConfigType

MC_ME Partition Configuration.

This structure contains information for configuring the Partitions. The definitions for each Partition setting within the structure Power_Ip_MC_ME_PartitionConfigType shall contain:

- The index of the Partition.
- The configuration settings for the COFBs contained within the Partition.
- The configuration settings for the Cores contained within the Partition.

Definition at line 230 of file Power_Ip_MC_ME_Types.h.

Data Fields

Type	Name	Description
boolean	PartitionUnderMcuControl	Specifies whether the given partition is under MCU control. < Specifies whether the given partition's power management is under MCU control
boolean	PartitionPowerUnderMcuControl	The index of the partition.

Data Fields

Type	Name	Description
uint8	PartitionIndex	
uint32	PartitionPconfRegValue	The process configuration register value of the partition.
uint32	PartitionTriggerMask	Mask containing the Partition triggers (PCE/OSSE/etc) to be updated. Number of COFBs within the partition.
uint8	NumberOfCofbs	The configuration of the COFBs.
const Power_Ip_MC_ME_CofbConfigType(∗	ArrayPartitionCofbConfigPtr)[]	Number of cores within the partition.
uint8	NumberOfCores	The configuration of the cores.
const Power_Ip_MC_ME_CoreConfigType(∗	ArrayPartitionCoreConfigPtr)[]	

6.3.2.4 struct Power_Ip_MC_ME_ModeConfigType

MC_ME IP Configuration.

This structure contains information for configuring the entire MC_ME IP.

Definition at line 263 of file Power_Ip_MC_ME_Types.h.

Data Fields

Type	Name	Description
uint32	MainCoreIdRegValue	MC_ME Main Core ID register. < MC_ME Mode Partition Settings.
const Power_Ip_MC_ME_PartitionConfigType(∗	ArrayPartitionConfigPtr)[((uint8) -1U)]	

6.3.2.5 struct Power_Ip_MC_RGM_ConfigType

Configuration of MC_RGM hardware IP.

This data configuration is set at module initialization phase.

Definition at line 132 of file Power_Ip_MC_RGM_Types.h.

Data Fields

Type	Name	Description
Power_Ip_MC_RGM_ResetType	ResetType	RESET type: Functional vs Destructive. <
uint32	FuncResetOpt	Enable/Disable functional reset sources (RGM_FERD register). <
uint32	FesThresholdReset	Functional Reset Escalation Threshold (RGM_FRET register). < Destructive Reset Escalation Threshold (RGM_DRET register).
uint32	DesThresholdReset	

6.3.2.6 struct Power_Ip_MC_RGM_CoreConfigType

MC_RGM Core Reset Configuration.

This structure contains information for configuring the cores. The definitions for each Core setting within the structure Mcu_Power_Ip_MC_RGM_CoreConfigType shall contain:

- The index of the Core (within its domain).
- Power management information (i.e. assert or deassert the reset signal of the Core).

Definition at line 170 of file Power_Ip_MC_RGM_Types.h.

Data Fields

Type	Name	Description
boolean	CoreUnderMcuControl	Specifies whether the given core is under MCU control. < The index of the core within the domain.
uint8	CoreIndex	
uint32	CorePrstRegValue	The reset enable register value of the core.
uint32	CoreBlocksToUpdateMask	Mask containing the Core blocks to be updated.

6.3.2.7 struct Power_Ip_MC_RGM_CofbConfigType

MC_RGM COFB Configuration.

This structure contains information for configuring the COFBs (Collection of Functional Blocks). The definitions for each COFB setting within the structure Mcu_Power_Ip_MC_RGM_CofbConfigType shall contain:

- The index of the COFB (within its domain).
- The list of peripherals enable/disable (i.e. the value of the PRSTx_COFBy register).

Definition at line 193 of file Power_Ip_MC_RGM_Types.h.

Data Fields

Type	Name	Description
boolean	CofbUnderMcuControl	Specifies whether the given COFB set is under MCU control. < The index of the COFB set within the domain.
uint8	CofbIndex	
uint32	CofbRstRegValue	The reset enable register value of the COFB set.
uint32	CofbBlocksToUpdateMask	Mask containing the COFB blocks to be updated.

6.3.2.8 struct Power_Ip_MC_RGM_DomainConfigType

MC_RGM Domain Configuration.

This structure contains information for configuring the Domains. The definitions for each Domain setting within the structure Mcu_Power_Ip_MC_RGM_DomainConfigType shall contain:

- The index of the Domain.
- The configuration settings for the COFBs contained within the Domain.

Definition at line 216 of file Power_Ip_MC_RGM_Types.h.

Data Fields

Type	Name	Description
boolean	DomainUnderMcuControl	Specifies whether the given domain is under MCU control. < Specifies whether the given domain's power management is under MCU control
boolean	DomainPowerUnderMcuControl	The index of the domain.
uint8	DomainIndex	
uint32	DomainRdcRegValue	The process configuration register value of the domain. Number of COFBs within the domain.
uint8	NumberOfCofbs	The configuration of the COFBs.
const Power_Ip_MC_RGM_CofbConfigType(*	ArrayDomainCofbConfigPtr)[]	Number of cores within the domain.
uint8	NumberOfCores	The configuration of the cores.
const Power_Ip_MC_RGM_CoreConfigType(*	ArrayDomainCoreConfigPtr)[]	

6.3.2.9 struct Power_Ip_MC_RGM_ModeConfigType

MC_RGM IP Mode Configuration.

This structure contains information for configuring the entire MC_RGM IP.

Definition at line 248 of file Power_Ip_MC_RGM_Types.h.

Data Fields

Type	Name	Description
const Power_Ip_MC_RGM_DomainConfigType(*	ArrayDomainConfigPtr)[((uint8) 1U)]	MC_RGM Mode Domain Settings. <

6.3.2.10 struct Power_Ip_PMC_ConfigType

Configuration for PMC.

The power control unit (PMC) acts as a bridge for mapping the PMC peripheral to the PMC address space.

Definition at line 108 of file Power_Ip_PMC_Types.h.

Data Fields

Type	Name	Description
uint32	NcspdCtrl	Non-Critical Supply Presence Detector Control Register (NCSPD_CTL)

6.3.2.11 struct Power_Ip_MC_RGM_Type

MC_RGM - Register Layout Typedef

Definition at line 313 of file Power_Ip_Specific.h.

Data Fields

Type	Name	Description
volatile uint32	DES	Destructive Event Status Register, offset: 0x0
uint8	RESERVED_0[4]	
volatile uint32	FES	Functional /External Reset Status Register, offset: 0x8
volatile uint32	FERD	Functional Event Reset Disable Register, offset: 0xC
uint8	RESERVED_1[4]	

Data Fields

Type	Name	Description
volatile uint32	FREC	Functional Reset Escalation Counter Register, offset: 0x14
volatile uint32	FRET	Functional Reset Escalation Threshold Register, offset: 0x18
volatile uint32	DRET	Destructive Reset Escalation Threshold Register, offset: 0x1C
volatile uint32	ERCTRL	External Reset Control Register, offset: 0x20
volatile uint32	RDSS	Reset During Standby Status Register, offset: 0x24
uint8	RESERVED_2[24]	
struct Power_Ip_MC_RGM_Type.PRST	PRST[(8U)]	
uint8	RESERVED_3[192]	
struct Power_Ip_MC_RGM_Type.PSTAT	PSTAT[(8U)]	

6.3.3 Macro Definition Documentation

6.3.3.1 IP_CM_AIRCR

```
#define IP_CM_AIRCR
```

CM7 AIRCR base pointer

Definition at line 123 of file Power_Ip_CortexM7.h.

6.3.3.2 CM_AIRCR_VECTKEY

```
#define CM_AIRCR_VECTKEY(
              x )
```

Reg_eSys_CortexM_H_REF_1 A function should be used in preference to a function-like macro where they are interchangeable.

Definition at line 133 of file Power_Ip_CortexM7.h.

6.3.3.3 MCU_RAW_RESET_DEFAULT

```
#define MCU_RAW_RESET_DEFAULT
```

The function Mcu_GetResetRawValue shall return an implementation specific value which does not correspond to a valid value of the reset status register and is not equal to 0 if this function is called prior to calling of the function Mcu_Init, and if supported by the hardware.

Definition at line 103 of file Power_Ip_Specific.h.

6.3.3.4 POWER_IP_FIRST_RESET_REASON_POS

```
#define POWER_IP_FIRST_RESET_REASON_POS
```

This macro is used to define the position of the first reset reason.

Definition at line 249 of file Power_Ip_Specific.h.

6.3.3.5 POWER_IP_RESET_DOMAIN_COUNT

```
#define POWER_IP_RESET_DOMAIN_COUNT
```

Number of domains of the RESET module.

Definition at line 255 of file Power_Ip_Specific.h.

6.3.3.6 POWER_IP_RESET_INSTANCE_COUNT

```
#define POWER_IP_RESET_INSTANCE_COUNT
```

Number of instances of the RESET module.

Definition at line 257 of file Power_Ip_Specific.h.

6.3.3.7 POWER_IP_MC_RGM_PRST_COUNT

```
#define POWER_IP_MC_RGM_PRST_COUNT
```

MC_RGM - Size of Registers Arrays

Definition at line 264 of file Power_Ip_Specific.h.

6.3.4 Types Reference

6.3.4.1 Power_Ip_RawResetType

```
typedef uint32 Power_Ip_RawResetType
```

The type Mcu_RawResetType specifies the reset reason in raw register format, read from a reset status register.

The type shall be uint8, uint16 or uint32 based on best performance.

Destructive and Functional Reset Events Log.

Definition at line 192 of file Power_Ip_Types.h.

6.3.4.2 Power_Ip_ModeType

```
typedef uint32 Power_Ip_ModeType
```

The Mcu_ModeType specifies the identification (ID) for a MCU mode, configured via configuration structure.

The type shall be uint8, uint16 or uint32.

Definition at line 201 of file Power_Ip_Types.h.

6.3.4.3 Power_Ip_ReportErrorsCallbackType

```
typedef void(* Power_Ip_ReportErrorsCallbackType) (Power_Ip_ReportErrorType Error, uint8 ErrorCode)
```

Power report error callback structure. Implements PowerReportErrorCallbackType_Class.

Definition at line 243 of file Power_Ip_Types.h.

6.3.5 Enum Reference

6.3.5.1 Power_Ip_MC_RGM_ResetType

```
enum Power_Ip_MC_RGM_ResetType
```

Reset type to be performed through the Mcu_PerformReset() API.

Destructive Reset:

- Flash is always reset, so an updated value of the option bits is reloaded in volatile registers outside of the Flash array.
- Trimming is lost.
- STCU is reset and configured BISTs are executed Functional Reset:
- Starts the reset sequence from PHASE1 or from PHASE3.
- The volatile registers are not reset; in case of a reset event, the trimming is maintained.
- No BISTs shall be executed after functional resets.

Enumerator

MCU_FUNC_RESET	Functional Reset type.
MCU_DEST_RESET	Destructive Reset type.

Definition at line 115 of file Power_Ip_MC_RGM_Types.h.

6.3.5.2 Power_MC_RGM_StatusType

enum Power_MC_RGM_StatusType

Enumerator

POWER_MC_RGM_UNINIT	The MC_RGM driver is uninitialized.
POWER_MC_RGM_INIT	The MC_RGM driver is initialized.

Definition at line 259 of file Power_Ip_MC_RGM_Types.h.

6.3.5.3 Power_Ip_MSCM_CpxType

enum Power_Ip_MSCM_CpxType

Type of the return value of the function Mcu_GetCpxType.

The type of Mcu_CpxType is an enumeration with the following values: POWER_IP_CORE_A53, POWER_↩ IP_CORE_CM7.

Enumerator

POWER_IP_CORE_UNDEFINED	Undefined core.
POWER_IP_CORE_A53	Cortex A53 core.
POWER_IP_CORE_CM7	Cortex M7 core.

Definition at line 106 of file Power_Ip_MSCM.h.

6.3.5.4 Power_Ip_PowerModeType

enum Power_Ip_PowerModeType

Power Modes encoding.

Supported power modes for the MCU.

Enumerator

POWER_IP_DEST_RESET_MODE	Destructive Reset Mode.
POWER_IP_FUNC_RESET_MODE	Functional Reset Mode.
POWER_IP_RESET_MODE	Any reset mode. Used when the particular type of reset doesn't matter.
POWER_IP_CORE_WARM_RESET_MODE	Core Warm Reset Mode.
POWER_IP_CORE_STANDBY_MODE	Core Standby Mode.
POWER_IP_SOC_PREPARE_STANDBY_MODE	Prepare Standby Mode.
POWER_IP_SOC_STANDBY_MODE	StandBy Mode.
POWER_IP_STANDBY_MODE	Prepare Standby and StandBy Mode.
POWER_IP_RUN_MODE	Run Mode.

Definition at line 167 of file Power_Ip_Types.h.

6.3.5.5 Power_Ip_ReportErrorType

```
enum Power_Ip_ReportErrorType
```

Power ip report error types.

Enumerator

POWER_IP_REPORT_TIMEOUT_ERROR	Report Timeout Error.
POWER_IP_ISR_ERROR	Notification Error.
POWER_IP_PMC_ERROR	Notification PMC.

Definition at line 232 of file Power_Ip_Types.h.

6.3.6 Function Reference

6.3.6.1 Power_Ip_Init()

```
void Power_Ip_Init (
            const Power_Ip_HwIPsConfigType * HwIPsConfigPtr )
```

Power initialization.

This function power initialization

Parameters

in	*HwIPsConfigPtr*	power initialization configuration.

Returns

void

6.3.6.2 Power_Ip_SetMode()

```
void Power_Ip_SetMode (
            const Power_Ip_ModeConfigType * ModeConfigPtr )
```

Sets mode.

This function sets mode.

Parameters

in	*ModeConfigPtr*	power set mote configuration.

Returns

void

6.3.6.3 Power_Ip_GetPreviousMode()

```
Power_Ip_PowerModeType Power_Ip_GetPreviousMode (
            void  )
```

This function returns the previous mode.

This function returns the previous mode.

Returns

Status of the previous mode.

6.3.6.4 Power_Ip_PerformReset()

```
void Power_Ip_PerformReset (
            const Power_Ip_HwIPsConfigType * HwIPsConfigPtr )
```

Performs reset.

This function performs reset.

Parameters

in	*HwIPsConfigPtr*	reset initialization configuration.

Returns

void

6.3.6.5 Power_Ip_GetResetReason()

```
Power_Ip_ResetType Power_Ip_GetResetReason (
            void  )
```

Returns reset type.

This function returns reset type.

Returns

Power_Ip_ResetType Reset type

6.3.6.6 Power_Ip_GetResetRawValue()

```
Power_Ip_RawResetType Power_Ip_GetResetRawValue (
            void  )
```

Returns raw reset type.

This function returns raw reset type.

Returns

Power_Ip_RawResetType Raw reset type

6.3.6.7 Power_Ip_InstallNotificationsCallback()

```
void Power_Ip_InstallNotificationsCallback (
            Power_Ip_ReportErrorsCallbackType ReportErrorsCallback )
```

Install report error callback.

This function installs a callback for reporting errors from power driver

Parameters

in	*ReportErrorsCallback*	Callback to be installed.

Returns

void

6.3.6.8 Power_Ip_StartTimeout()

```
void Power_Ip_StartTimeout (
            uint32 * StartTimeOut,
            uint32 * ElapsedTimeOut,
            uint32 * TimeoutTicksOut,
            uint32 TimeoutUs )
```

Initializes a starting reference point for timeout.

Parameters

out	*StartTimeOut*	The starting time from which elapsed time is measured
out	*ElapsedTimeOut*	The elapsed time to be passed to PowerTimeoutExpired
out	*TimeoutTicksOut*	The timeout value (in ticks) to be passed to PowerTimeoutExpired
in	*TimeoutUs*	The timeout value (in microseconds)

6.3.6.9 Power_Ip_TimeoutExpired()

```
boolean Power_Ip_TimeoutExpired (
            uint32 * StartTimeInOut,
            uint32 * ElapsedTimeInOut,
            uint32 TimeoutTicks )
```

Checks for timeout condition.

Parameters

in,out	*StartTimeInOut*	The starting time from which elapsed time is measured
in,out	*ElapsedTimeInOut*	The accumulated elapsed time from the starting time reference
in	*TimeoutTicks*	The timeout limit (in ticks)

6.4 Ram Ip Driver

6.4.1 Detailed Description

Data Structures

- struct Ram_Ip_RamConfigType

  Definition of a RAM section within the configuration structure. The definitions for each RAM section within the structure Ram_Ip_ConfigType shall contain: More...

Types Reference

- typedef void(* Ram_Ip_ReportErrorsCallbackType) (Ram_Ip_RamReportErrorType Error, uint8 Error↩ Code)

  Ram report error callback structure. Implements RamReportErrorCallbackType_Class.
- typedef uint32 Ram_Ip_RamSectionType

  The Ram_Ip_RamSectionType specifies the identification (ID) for a RAM section, configured via the configuration structure. The type shall be uint8, uint16 or uint32, based on best performance.
- typedef uint32 Ram_Ip_RamIndexType

  The Ram_Ip_RamIndexType specifies the variable for indexing RAM sections. The type shall be uint8, uint16 or uint32, based on best performance.
- typedef uint32 Ram_Ip_RamSizeType

  The Ram_Ip_RamSizeType specifies the RAM section size. The type shall be uint8, uint16 or uint32, based on best performance.
- typedef uint32 Ram_Ip_RamWriteSizeType

  The Ram_Ip_RamWriteSizeType specifies the RAM section write size. The type shall be uint8, uint16 or uint32, based on best performance.

Enum Reference

- enum Ram_Ip_RamReportErrorType

  Ram ip report error types.
- enum Ram_Ip_RamStateType

  Ram State of the microcontroller.
- enum Ram_Ip_StatusType

  Ram ip status return codes.

Function Reference

- Ram_Ip_StatusType Ram_Ip_InitRamSection (const Ram_Ip_RamConfigType *RamConfigPtr)

  Initializes RAM section.
- Ram_Ip_RamStateType Ram_Ip_GetRamState (void)

  Returns RAM state.
- void Ram_Ip_InstallNotificationsCallback (Ram_Ip_ReportErrorsCallbackType ReportErrorsCallback)

  Install report error callback. This function installs a callback for reporting errors from Ram driver.

6.4.2 Data Structure Documentation

6.4.2.1 struct Ram_Ip_RamConfigType

Definition of a RAM section within the configuration structure. The definitions for each RAM section within the structure Ram_Ip_ConfigType shall contain:

- RAM section base address
- Section size
- Data pre-setting to be initialized
- RAM write size

Definition at line 191 of file Ram_Ip_Types.h.

Data Fields

Type	Name	Description
Ram_Ip_RamSectionType	RamSectorId	The ID for Ram Sector configuration.
uint8(*	RamBaseAddrPtr)[1U]	RAM section base address.
Ram_Ip_RamSizeType *	RamSize	RAM section size.
uint64	RamDefaultValue	RAM default value for initialization.
Ram_Ip_RamWriteSizeType	RamWriteSize	RAM section write size.

6.4.3 Types Reference

6.4.3.1 Ram_Ip_ReportErrorsCallbackType

```
typedef void(* Ram_Ip_ReportErrorsCallbackType) (Ram_Ip_RamReportErrorType Error, uint8 ErrorCode)
```

Ram report error callback structure. Implements RamReportErrorCallbackType_Class.

Definition at line 125 of file Ram_Ip_Types.h.

6.4.3.2 Ram_Ip_RamSectionType

```
typedef uint32 Ram_Ip_RamSectionType
```

The Ram_Ip_RamSectionType specifies the identification (ID) for a RAM section, configured via the configuration structure. The type shall be uint8, uint16 or uint32, based on best performance.

Definition at line 133 of file Ram_Ip_Types.h.

6.4.3.3 Ram_Ip_RamIndexType

```
typedef uint32 Ram_Ip_RamIndexType
```

The Ram_Ip_RamIndexType specifies the variable for indexing RAM sections. The type shall be uint8, uint16 or uint32, based on best performance.

Definition at line 140 of file Ram_Ip_Types.h.

6.4.3.4 Ram_Ip_RamSizeType

```
typedef uint32 Ram_Ip_RamSizeType
```

The Ram_Ip_RamSizeType specifies the RAM section size. The type shall be uint8, uint16 or uint32, based on best performance.

Definition at line 147 of file Ram_Ip_Types.h.

6.4.3.5 Ram_Ip_RamWriteSizeType

```
typedef uint32 Ram_Ip_RamWriteSizeType
```

The Ram_Ip_RamWriteSizeType specifies the RAM section write size. The type shall be uint8, uint16 or uint32, based on best performance.

Definition at line 154 of file Ram_Ip_Types.h.

6.4.4 Enum Reference

6.4.4.1 Ram_Ip_RamReportErrorType

```
enum Ram_Ip_RamReportErrorType
```

Ram ip report error types.

Enumerator

RAM_IP_REPORT_TIMEOUT_ERROR	Report Timeout Error.

Definition at line 110 of file Ram_Ip_Types.h.

6.4.4.2 Ram_Ip_RamStateType

```
enum Ram_Ip_RamStateType
```

Ram State of the microcontroller.

This is the Ram State data type returned by the function Mcu_GetRamState() of the Mcu module.

Enumerator

RAM_IP_RAMSTATE_INVALID	RAM content is not valid or unknown (default).
RAM_IP_RAMSTATE_VALID	RAM content is valid.

Definition at line 161 of file Ram_Ip_Types.h.

6.4.4.3 Ram_Ip_StatusType

```
enum Ram_Ip_StatusType
```

Ram ip status return codes.

This is the Ram State data type returned by the function Mcu_GetRamState() of the Mcu module.

Enumerator

RAM_IP_STATUS_OK	RAM_IP Ok status
RAM_IP_STATUS_NOT_OK	RAM_IP Not ok status
RAM_IP_STATUS_UNDEFINED	RAM_IP Status is unknown

Definition at line 174 of file Ram_Ip_Types.h.

6.4.5 Function Reference

6.4.5.1 Ram_Ip_InitRamSection()

```
Ram_Ip_StatusType Ram_Ip_InitRamSection (
            const Ram_Ip_RamConfigType * RamConfigPtr )
```

Initializes RAM section.

This function initializes RAM section.

Parameters

in	*RamConfigPtr*	Ram section configuration.

Returns

Ram_Ip_StatusType Ram status

6.4.5.2 Ram_Ip_GetRamState()

```
Ram_Ip_RamStateType Ram_Ip_GetRamState (
            void  )
```

Returns RAM state.

This function returns RAM section.

Returns

Ram_Ip_RamStateType Ram state

6.4.5.3 Ram_Ip_InstallNotificationsCallback()

```
void Ram_Ip_InstallNotificationsCallback (
            Ram_Ip_ReportErrorsCallbackType ReportErrorsCallback )
```

Install report error callback. This function installs a callback for reporting errors from Ram driver.

Parameters

in	*ReportErrorsCallback*	Callback to be installed.

Returns

void

How to Reach Us:

Home Page:
nxp.com

Web Support:
nxp.com/support