Computer Project: Transients on Transmission Lines

B EE 361 A: Spring 2020

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Total Score: _____

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1. Introduction

With the objective of implementing a Transmission Line representation of a CMOS circuit using the circuit simulator program, LTSpice, this final class project instructed students to answer many different questions in the analysis of created schematics. Integrating a myriad of transmission line techniques from the course textbook, Ulaby's *Fundamentals of Applied Electronics, 7th Edition*, each problem became a relevant step in solving for the overall best Transmission Line representation circuit.

2. Transmission Line Representation of a CMOS Circuit

Problem 1

Discussions

Problem 1 uses Transient Analysis for the FR-4 PCB Microstrip Lossless Line. This lossless line has a CMOS circuit laid out on this PCB. The example is given in **Figure 2-1**.

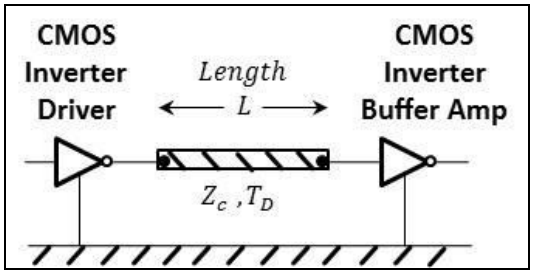


Figure 2-1: CMOS Circuit on a PCB

This CMOS Circuit consists of CMOS inverters with an interconnect between them. This CMOS Circuit can also be modeled as a Transmission Line Circuit as shown in **Figure 2-2**.

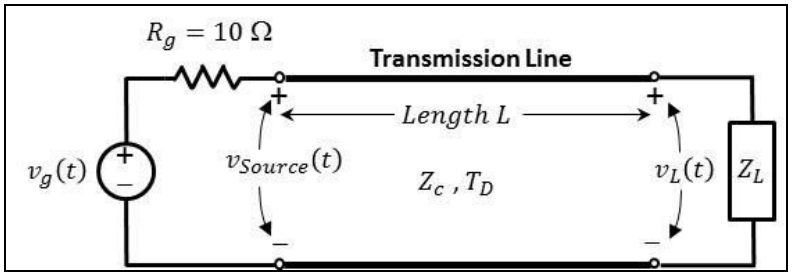


Figure 2-2: Transmission Line Circuit representation of CMOS Circuit

The load impedance Z_L is representative of the CMOS Inverter Buffer Amp and the Transmission Line is representative of the interconnect between the source and the load impedance. This circuit in **Figure 2-2** is what is inside of the microstrip landline shown in **Figure 2-3**.

This microstrip landline will be the main focus for this project and is where all the analysis in problem #1 will be based on. Problem #1 is broken up into four parts (A - D): identifying the type of two-conductor transmission line, calculating the characteristic impedance Z_o of the microstrip line, calculating the delay time for the microstrip line, and finally calculating the maximum distance if the microstrip landline time delay is 0.5 ns. All of these calculations are crucial for what is to come in the next problems (#2 - #10). This is because these values will be entered into LTspice for this microstrip line to be analyzed. All calculations and a description of the calculations for parts A - D are given under *Calculations*.

Given

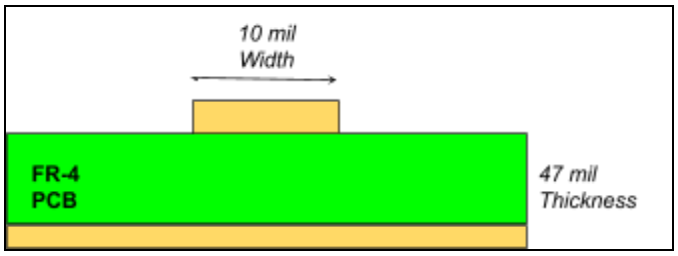


Figure 2-3: FR-4 Microstrip Land-Line

The permittivity of an FR-4 Circuit Board Material = 4.7 max (ε_r)

Calculations

A. What type of two-conductor transmission line in Ulaby Chapter 2, does this land-line most resemble?

This land-line most resembles a lossless microstrip line.

B. Calculate the characteristic impedance of this lossless line.

The characteristic impedance equation for a lossless line is given below:

$$Z_o = \frac{60}{\sqrt{\varepsilon_{eff}}}\left[ln\left(\frac{6 + (2\pi - 6)\, e^{-t}}{s}\right) + \sqrt{1 + \frac{4}{s^2}} \right]$$

In order to find this characteristic impedance (Z_o), we have to find the effective coefficient (ε_{eff}). The equation is given below:

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + (\frac{\varepsilon_r + 1}{2})(1 + \frac{10}{s})^{-xy}$$

The effective coefficient (ε_r) equation requires an x value and a y value. Since ε_r is given (4.7) we can plug it in to solve for x:

$$x = 0.56\,[\,\frac{\varepsilon_r - 0.9}{\varepsilon_r + 3}\,]^{0.05} = 0.56\,[\,\frac{(4.7) - 0.9}{(4.7) + 3}\,]^{0.05} = 0.5057$$

The equation y is solved by first solving for s , which is the width - to - thickness ratio:

$$s = \frac{w}{h} = \frac{10\,mil}{47\,mil} = 0.2128$$

Plugging in s into equation y gives the following:

$$\begin{aligned} y &= 1 + 0.02\,[\,ln(\frac{s^4 + (3.7{*}10^{-4})s^2}{s^4 + 0.43})\,] + 0.05\,[\,ln(1 + (1.7 * 10^{-4})s^3] \\ &= 1 + 0.02\,[\,ln(\frac{(0.2128)^4 + (3.7{*}10^{-4})(0.2128)^2}{(0.2128)^4 + 0.43})\,] + 0.05[\,ln(1 + (1.7 * 10^{-4})(0.2128)^3\,] \\ &= 1 + 0.02\,[\,ln(\frac{0.002067}{0.43205})\,] + 0.05\,[ln(1)\,] \\ &= 1 - 0.106849 + 0 = 1.10685 \end{aligned}$$

Once x and y are found, their values along with ε_r = 4.7 can be plugged into the ε_{eff} equation:

$$\begin{aligned} \varepsilon_{eff} &= \frac{(4.7) + 1}{2} + [\frac{(4.7) - 1}{2}][1 + \frac{10}{(0.2128)}]^{-(0.54057)(1.10685)} \\ &= 2.85 + (1.85)(47.992)^{-(0.59833)} = 3.0325 \end{aligned}$$

Finally, the characteristic impedance can be found with the known value of ε_r that was calculated above:

$$Z_o = \frac{60}{\sqrt{\varepsilon_{eff}}}[\,ln(\frac{6 + (2\pi - 6)\,e^{-t}}{s}) + \sqrt{1 + \frac{4}{s^2}}\,]$$

$$t = (\frac{30.67}{s})^{0.75} = [\frac{30.67}{(0.2128)}]^{0.75} = 41.596$$

$$\begin{aligned} Z_o &= \frac{60}{\sqrt{(3.0325)}}\,[\,ln(\frac{6 + (2\pi - 6)\,e^{-(41.596)}}{(0.2128)}) + \sqrt{1 + \frac{4}{(0.2128)^2}}\,] \\ &= (34.4549)[\,ln(\frac{(6)}{(0.2128)}) + (9.4515)\,] \\ &= (34.4549)[\,ln((28.1955) + (9.4515)\,] \\ &= (34.4549)(3.6283) = 125.011 \end{aligned}$$

$$Z_0 = 125.011\ \Omega$$

C. What is the delay time for the pulse to travel from CMOS Inverter # 1 to CMOS Inverter #2 for a land-line that is 10 cm long?

We know the distance d to be $10\ cm\ or\ 0.1\ m$

$$d = 10\ cm = 0.1\ m$$

The equation for a round trip delay time for the land-line is:

$$round\ trip\ delay \rightarrow \Delta t = \frac{2d}{u_p}$$

Solving for u_p with the known value of the speed of light c and the coefficient ε_r gives us:

$$u_p = \frac{c}{\sqrt{\varepsilon_r}} = \frac{3*10^8}{\sqrt{4.7}} = 1.3838 * 10^8\ m/s$$

Finally, plugging everything in to solve for the delay time Δt gives:

$$\Delta t = \frac{2(0.1\ m)}{(1.3838*10^8\ m/s)} = 1.445 * 10^{-9} = 1.445\ ns$$

$$delay\ time = 1.445\ ns$$

D. **If we wanted to limit time delay to less than 0.5 ns, what would the maximum length be?**

To solve for the maximum length, we use the same equation as in part C:

$$round\ trip\ delay \rightarrow \Delta t = \frac{2d}{u_p}$$

We can rearrange the equation for d since Δt is given for us and we solved u_p above in part C:

$$\Delta t = 0.5 * 10^{-9} s$$
$$u_p = 1.3838 * 10^8\ m/s$$
$$d = \frac{\Delta t * u_p}{2} = \frac{(0.5*10^{-9})(1.3838*10^8)}{2} = 0.0346\ m = 3.46\ cm$$

$$maximum\ length = 3.46\ cm$$

3. Purely Resistive Terminations

Problem 2

Discussions

LTSpice Results

The purpose of this LTspice problem is to analyze a transmission line of a calculated value 125.011 Ω. With this Tx-line, we see how it can affect a circuit with a 5U(t) step function pulse source, a resistive source impedance Z_g of 10 Ω, and a resistive load impedance Z_L of 200 Ω.

Problem two starts off with building a transmission line circuit in LTspice as shown in **Figure 3-1**. First, the circuit is excited with a 5U(t) pulse voltage source. For this voltage source, T_{rise} and T_{fall} have been set to 0.1 ps. This is because even though there is no rise or fall time for this circuit, LTspice will default to a value of 0s to get the desired step function without any rise or fall time effects. Finally, since the T_initial is 0V, the pulse source must start at 1s instead of 0s.

In the LTspice circuit schematic in **Figure 3-1**, Z_g is the resistive source impedance and has a value of 10 Ω. This perfects the pulse source and balances out any imperfections of electric potential. According to the graph shown in **Figure 3-2**, this resistive source impedance maintains a steady input voltage value of 5 V for the step function. This can be shown in the red line labeled V(n001).

The transmission line is the main focus of our analysis. The time delay (Td) is 0.5 ns and the calculated characteristic impedance is 125.011 Ω. The time delay is the time it takes for the signal or current to get from one end of the transmission line to the other. A transmission line is a pair of wires that will continue to draw current from the source so long as a continuous wave propagation is flowing, behaving as a constant load.

Finally, Z_L is the resistive load impedance has a value of 200 Ω. This is the measure of the opposition of the current that is external to the electrical source, which is in this case the pulse source. The load voltage (Vn003) as labeled in **Figure 3-2**. At first, the voltage of the load is high, around 5.7 V. However, over time the voltage starts to level out and eventually stays around 4.76 V. The reason for this high voltage is because of the electric potential of the pulse source. The electric potential is really high as the electrons leave the pulse source once the source is turned on. However, once the electrons flow throughout the whole circuit, Tx-line and the load impedance start to take effect and eventually cause the voltage to level off to a base voltage of about 4.76 V.

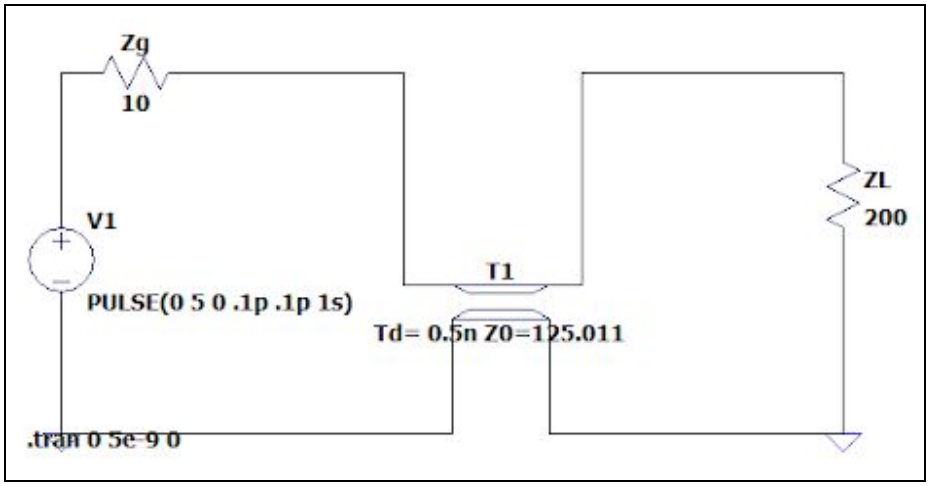


Figure 3-1: Transmission Line Circuit *5u(t) V Source, Zg (10 Ω), ZL (200 Ω), & Transmission Line T1 with Td = 0.5 ns & Z0 = 125.011 Ω*

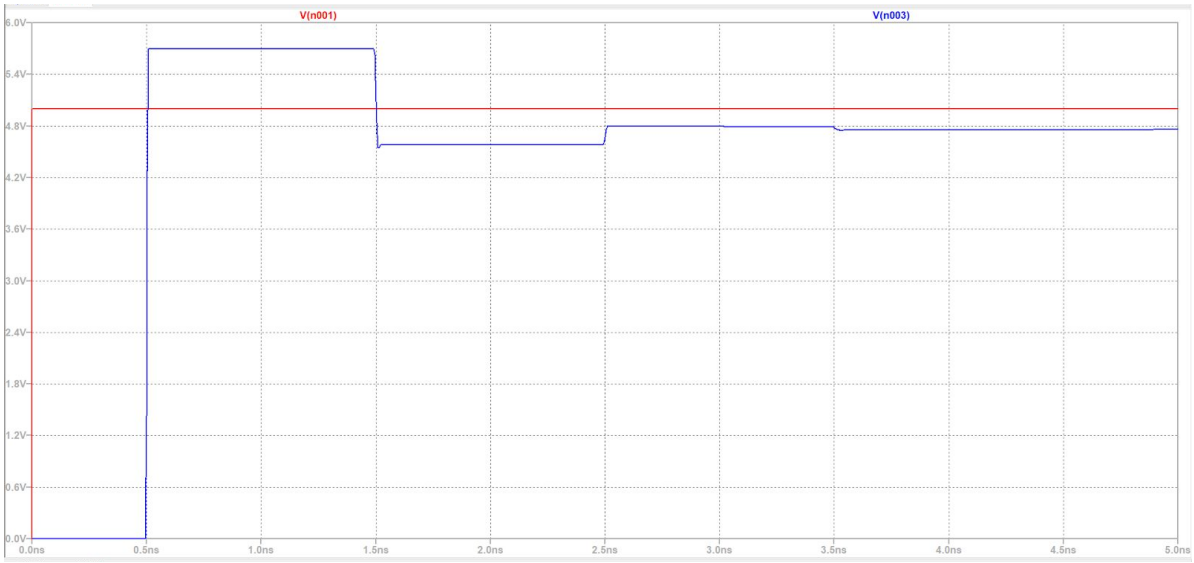


Figure 3-2: Voltage Plot of Figure 3-1 *V(n001) = V_{source} & V(n003) = V_L*

Results of Calculations and Graphs

The purpose of these calculations and graphs is to prove the accuracy of the data that was collected for the above figures that were modeled in LTspice in this problem: **Figure 3-1** and **Figure 3-2.** In order to compare the data modeled in LTspice, calculations were done to draw a bounce diagram. A graph to represent the bounce diagram was drawn to model the bounce diagram results. They are shown as **Figure 3-3** and **Figure 3-4** respectively.

The solution below in the *Calculations* section compares with the exact solution derived in section 2-12 of *Fundamentals of Applied Electrodynamics* by *Ulaby* because the technique of bounce diagrams and graphing the input and load voltage changes are the same.

To compare the input and load voltage changes (V(n001) and V(n003)), a few calculations must be done. First, the source and load reflection coefficient were calculated. An expression for the incident voltage ($t = 0^+$) was calculated as well. These three values were used to calculate several voltage differences that bounced back and forth down the bounce diagram. Note that these are not the values of the input and load voltages, but only the differences between them. Once these voltage differences were calculated a bounce diagram was drawn. This diagram is shown in **Figure 3-3** along with the input and load voltages themselves. Finally, a graph showing the step function of the calculated $V_s(t)$ and $V_L(t)$ on the bounce diagram is shown in **Figure 3-4.**

The purpose of creating a bounce diagram and graphing the results is to analyze the transmission line effects by trying to match what LTspice has shown. According to the graphs shown in **Figure 3-4,** the analysis comparison was effective. Both the LTspice and bounce diagram graphs match exactly.

Calculations

Below are the calculations to compare the LTspice results given in **Figure 3-1** and **Figure 3-2** under the *Discussions* section. They are accompanied with a bounce diagram to display the calculation results (**Figure 3-3**) along with a graph to display the bounce diagram results (**Figure 3-4**).

Source Reflection Coefficient:

$$R_s = Z_g = 10\ \Omega$$
$$Z_0 = 125.011\ \Omega$$
$$\Gamma_s = \frac{R_s - Z_o}{R_s + Z_o} = \frac{(10) - (125.011)}{(10) + (125.011)} = -0.8519$$

Load Reflection Coefficient:

$$R_L = Z_L = 200\ \Omega$$
$$Z_o = 125.011\ \Omega$$
$$\Gamma_L = \frac{R_L - Z_o}{R_L + Z_o} = \frac{(200) - (125.011)}{(200) + (125.011)} = 0.23072$$

Expression for the Incident Voltage ($t = 0^+$):

$$V_1^+ = \frac{Z_o}{R_s + Z_o}(V_o) = \frac{(125.011)}{(10) + (125.011)}(5\ V) = 4.6297\ V$$

Voltage Calculations for Bounce Diagram (**Figure 3-3):**

$$V_1^+ = 4.6297\ V$$
$$V_1^- = \Gamma_L V_1^+ = (0.2307)(4.6297) = 1.0681\ V$$

$$V_2^+ = \Gamma_s V_1^- = (-0.8519)(1.0681) = -0.9099\ V$$
$$V_2^- = \Gamma_L V_2^+ = (0.2307)(-0.9099) = -0.2099\ V$$
$$V_3^+ = \Gamma_s V_2^- = (-0.8519)(-0.2099) = 0.1788238\ V$$
$$V_3^- = \Gamma_L V_3^+ = (0.2307)(0.77514) = 0.0412546\ V$$
$$V_4^+ = \Gamma_s V_3^- = (-0.8519)(0.178825) = -0.0351448\ V$$
$$V_4^- = \Gamma_L V_4^+ = (0.2307)(-0.15234) = -0.0081079\ V$$
$$V_5^+ = \Gamma_s V_4^- = (-0.8519)(-0.351) = 0.006907\ V$$
$$V_5^- = \Gamma_L V_5^+ = (0.2307)(0.02990) = 0.001593\ V$$
$$V_6^+ = \Gamma_s V_5^- = (-0.8519)(0.006898) = -0.001357\ V$$

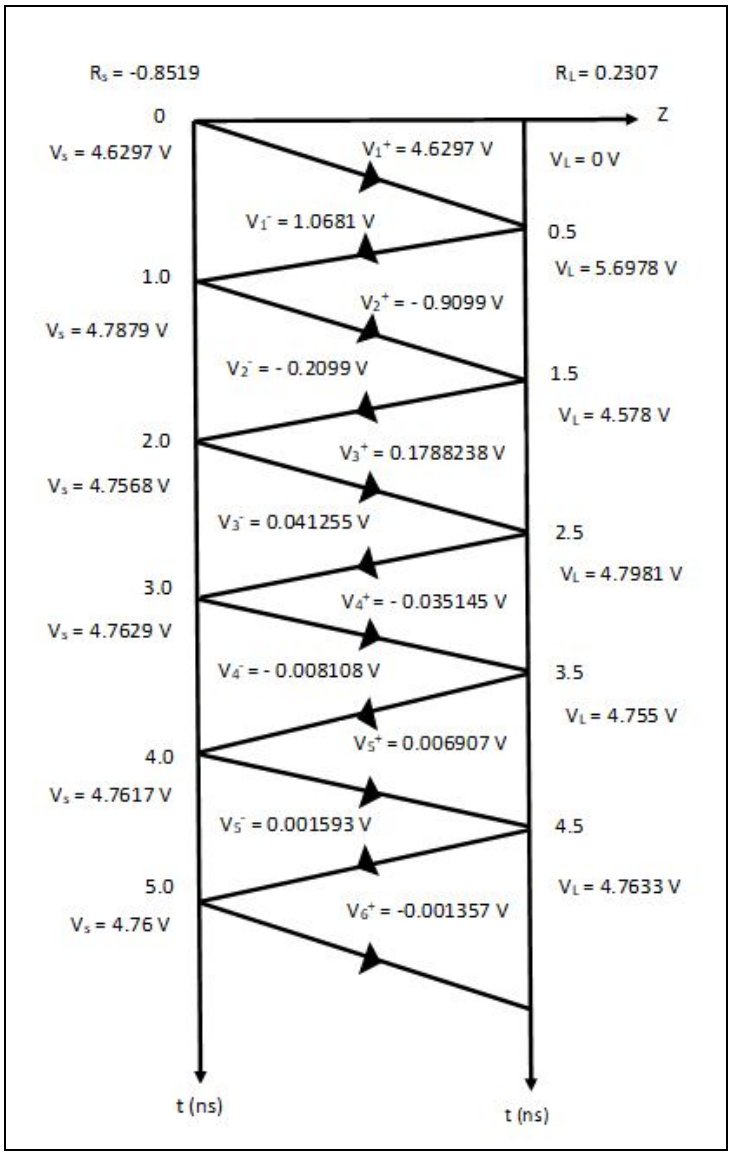


Figure 3-3: Bounce Diagram for Problem 2 Calculations section

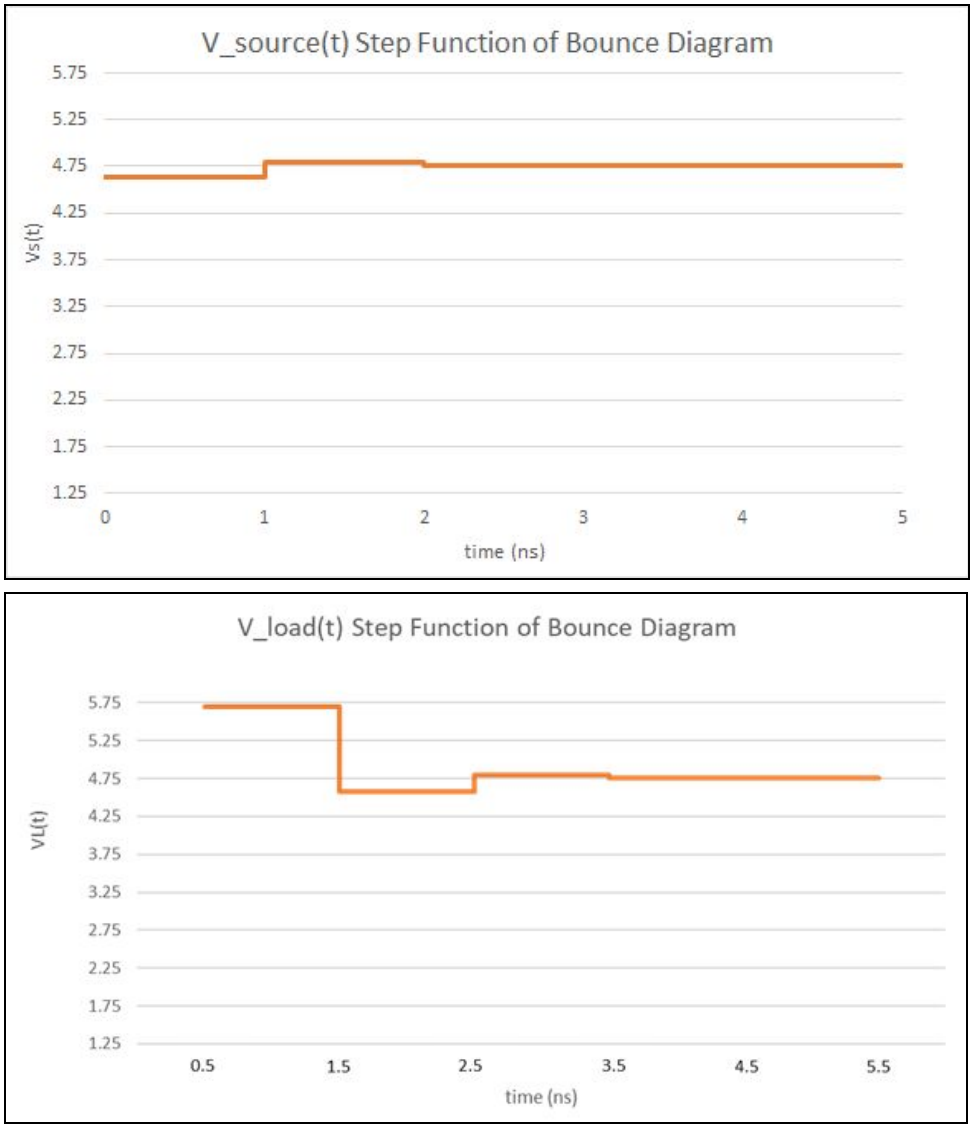


Figure 3-4: Vsource(t) and VLoad(t) graphs for Problem 2 Bounce Diagram Results

Conclusions

The goal of problem #2 is to analyze a simple 125.011Ω transmission line with a 5U(t) step function pulse source and understand how this transmission line and its values can affect a circuit. By connecting a resistive source impedance of 10Ω and resistive source load of 200Ω, an analysis of how Tx-line theory impacts elements in a circuit can be better understood. Calculating and graphing results and matching those results to the LTspice results proved to be effective because all results match almost exactly. Comparing the calculations to the LTspice results is important because it gives a greater understanding of how Tx-line theory relates to what we have learned in class. These calculations matched what we have learned and what has been observed during this problem.

Problem 3

Discussions

LTSpice Results

The goal of problem #3 is to change the characteristic impedance Z_0 to 50Ω instead of 125.011Ω to see how a lower characteristic impedance value would change the circuit. All values are the same as in problem #2. The resistive source impedance Z_g is 10Ω, the time delay (Td) for the transmission line is 0.5 ns, the characteristic impedance Z_0 is 50Ω and finally the resistive load impedance Z_L is 200 Ω.

Compared to problem #2, the blue line (V(n003)) that symbolized the load impedance Z_L was different for this problem. In this case, the starting voltage was higher. The starting voltage in the graph shown below in **Figure 3-5** is 6.6667 V for this problem, compared to 5.67 V in problem #2. The variation of the changes between voltages before they leveled out to one voltage was a lot different and larger. This is the result of lowering the characteristic impedance Z_0 to 50Ω. Because of a smaller characteristic impedance in the transmission line, the electrons due to the electric potential force (voltage) couldn't level out fast enough and the electric potential difference was larger compared to problem #2. See **Figure 3-5** and **Figure 3-6** for the schematic and graph below.

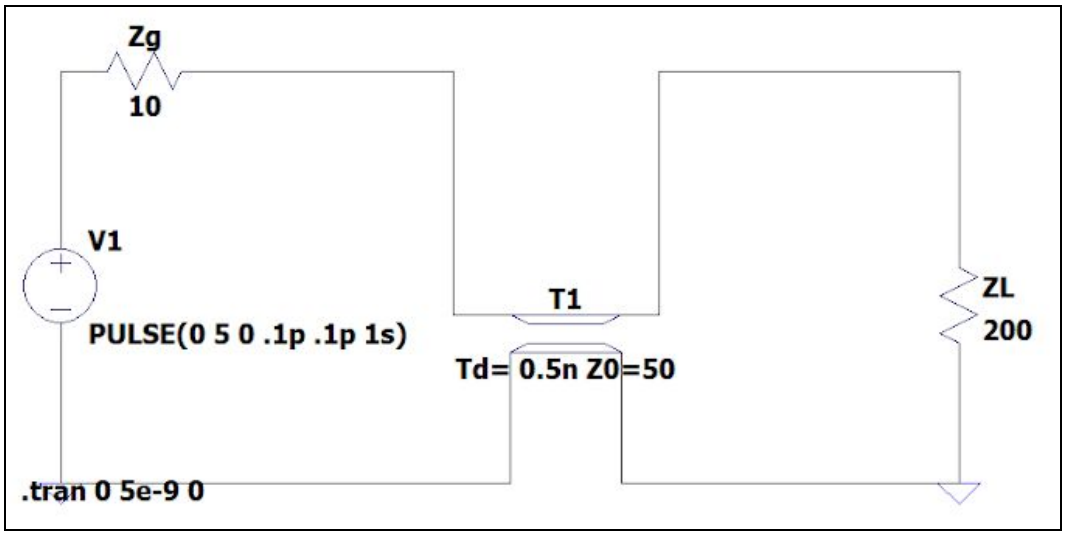


Figure 3-5: Transmission Line Circuit with 50 Ω Characteristic Impedance

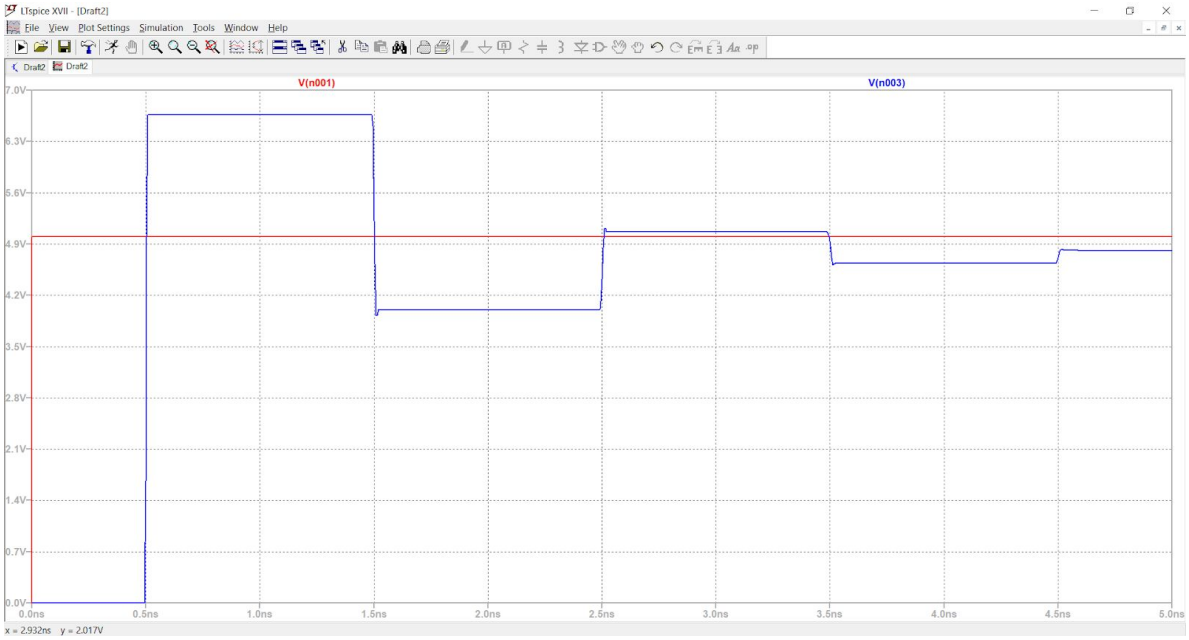


Figure 3-6: Voltage Plot of Figure 3-3 *V(n001) = V_{source} & V(n003) = V_L*

Results of Calculations and Graphs

The purpose of these calculations and graphs is to prove the accuracy of the data that was collected for the above figures that were modeled in LTspice in this problem: **Figure 3-5** and **Figure 3-6.** In order to compare the data modeled in LTspice, calculations were done to draw a bounce diagram. A graph to represent the bounce diagram was drawn to model the bounce diagram results. They are shown in **Figures 3-7** and **3-8** respectively for the bounce diagram and graph.

The *Calculations* section below is smaller compared to the calculations sections shown in previous problems. This is because of the smaller characteristic impedance value of 50Ω. Due to its small value, the source reflection coefficient and the load reflection coefficient each have smaller values, but the same sign as shown below, compared to the values in problem #2. The voltage expression for the incident voltage ($t = 0^+$) is also smaller in this problem. This results in a larger voltage difference for the voltage difference calculations, shown below. The bounce diagram with all the voltage difference values and the $V_s(t)$ and $V_L(t)$ values are shown in **Figure 3-7**. The graph of the calculations and bounce diagram (**Figure 3-8**) both show the $V_s(t)$ and $V_L(t)$ values, each with their own graph. These values are similar to what is shown in the LTspice graph in **Figure 3-6**, which indicates that the LTspice and calculated results match and are accurate. Because the characteristic impedance value Z_0 is lower, the electric potential (voltage) has time to level out to 4.76 V on the graph, and therefore, the changes between voltages on the graph also happen more often. The reason why the load voltage of 4.76 V is the same as problem #2 is that the load impedance Z_L is still 200 Ω.

Calculations

Below are the calculations to compare the LTspice results given in **Figure 3-5** and **Figure 3-6** under the *Discussions* section above. They are accompanied with a bounce diagram to display the calculation results (**Figure 3-7**) along with a graph to display the bounce diagram results (**Figure 3-8**).

Source Reflection Coefficient:

$R_s = Z_g = 10\ \Omega$
$Z_o = 50\ \Omega$

$$\Gamma_s = \frac{\Gamma_s - Z_o}{\Gamma_s + Z_o} = \frac{(10) - (50)}{(10) + (50)} = -0.6667$$

Load Reflection Coefficient:

$R_L = Z_L = 200\ \Omega$
$Z_o = 50\ \Omega$

$$\Gamma_L = \frac{\Gamma_L - Z_o}{\Gamma_L + Z_o} = \frac{(200) - (50)}{(200) - (50)} = 0.6$$

Expression for the Incident Voltage ($t = 0^+$):

$$V_1^+ = \frac{Z_o}{R_s + Z_o}(V_o) = \frac{(50)}{(200) + (50)}(5V) = 4.1667\ V$$

Voltage Calculations for Bounce Diagram (**Figure 3-7**):

$$V_1^+ = 4.1667\ V$$
$$V_1^- = \Gamma_L V_1^+ = (0.6)(4.1667) = 2.50002\ V$$
$$V_2^+ = \Gamma_s V_1^- = (-0.667)(2.50002) = -1.6675\ V$$
$$V_2^- = \Gamma_L V_2^+ = (0.6)(-1.6675) = -1.0005\ V$$
$$V_3^+ = \Gamma_s V_2^- = (-0.667)(-1.0005) = 0.6670\ V$$
$$V_3^- = \Gamma_L V_3^+ = (0.6)(0.6670) = 0.4002\ V$$
$$V_4^+ = \Gamma_s V_3^- = (-0.667)(0.4002) = -0.2668\ V$$
$$V_4^- = \Gamma_L V_4^+ = (0.6)(-0.2668) = -0.16008\ V$$
$$V_5^+ = \Gamma_s V_4^- = (-0.667)(-0.16008) = 0.10673\ V$$
$$V_5^- = \Gamma_L V_5^+ = (0.6)(0.10673) = 0.064\ V$$
$$V_6^+ = \Gamma_s V_5^- = (-0.667)(0.064) = -0.04269\ V$$

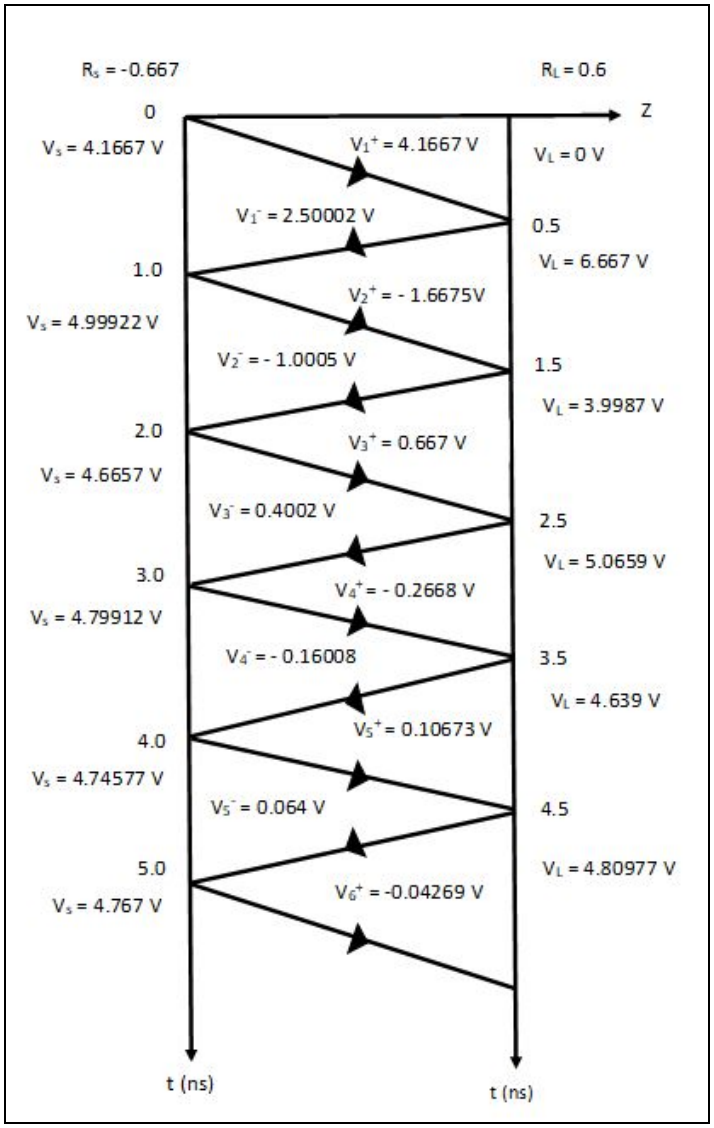


Figure 3-7: Bounce Diagram for Problem #3 Calculations Section

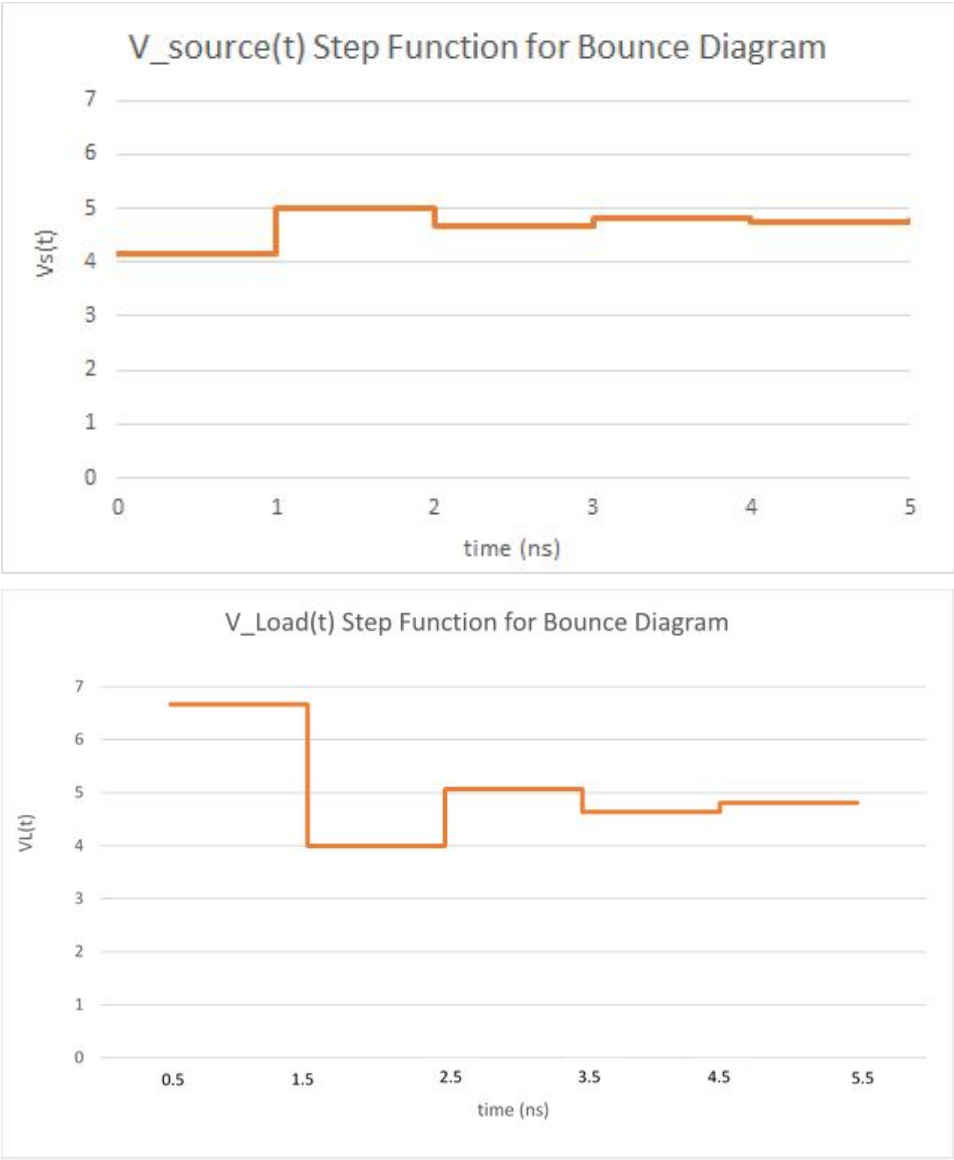


Figure 3-8: Vsource(t) and VLoad(t) Graphs for Bounce Diagram Results

Conclusions

To conclude, the goal of problem #3 is to lower the calculated characteristic impedance value of 125.011Ω to 50Ω to analyze the same circuit in problem #2 in a different way. By comparing the circuit in problem #2 to the circuit in problem #3, a few things were noticed. First, the load voltage graph on LTspice shown in **Figure 3-6** displayed a much-varied voltage graph with voltages with much greater and larger differences before getting to a voltage value of 4.76 V. Second, the calculations in problem #3 were different compared to the calculations done in problem #2. Because the impedance value was smaller this time, values such as the source reflection coefficient, the load reflection coefficient, and the expression for the incident voltage ($t = 0^+$) were also smaller. This resulted in the voltage difference calculations for the bounce diagram to be larger.

Problem 4

Discussions

LTSpice Results

In problem #4, the step function was replaced with a pulse function, such that the pulse function is equal to 5[U(t) - U(t - 0.5 ns)] Volts. Therefore, the starting voltage is 5 volts and the delay time is 0.5 ns, which is equivalent to 5e-10 according to **Figure 3-9** below. The rise and fall times (T_{rise} and T_{fall}) are 1% of the pulse width. Since the pulse width is 5e-10, multiplying that number by 0.1 results in the rise and fall times of 5e-12. Everything else in the figure is the same as problem #3. The source impedance is 10 Ω, the characteristic impedance is 50 Ω, and the load impedance is 200 Ω.

According to the equation given in problem #4 and #5: 5[U(t) - U(t - 0.5 ns)] Volts, there are two U(t) step functions with a 5 V amplitude. The graph in **Figure 3-10** clearly shows results with a pulse function. This is shown by the smaller peaks in **Figure 3-10** compared to the step graph shown in problem #2 and problem #3 LTSpice graphs with no peaks. The results of this equation can be seen in V(n001) and V(n002).

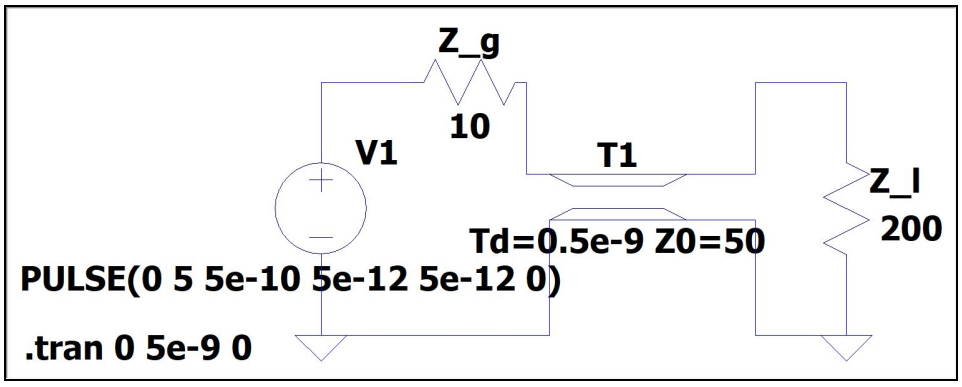


Figure 3-9: Transmission Line Circuit with Short Pulse of 0.5 ns

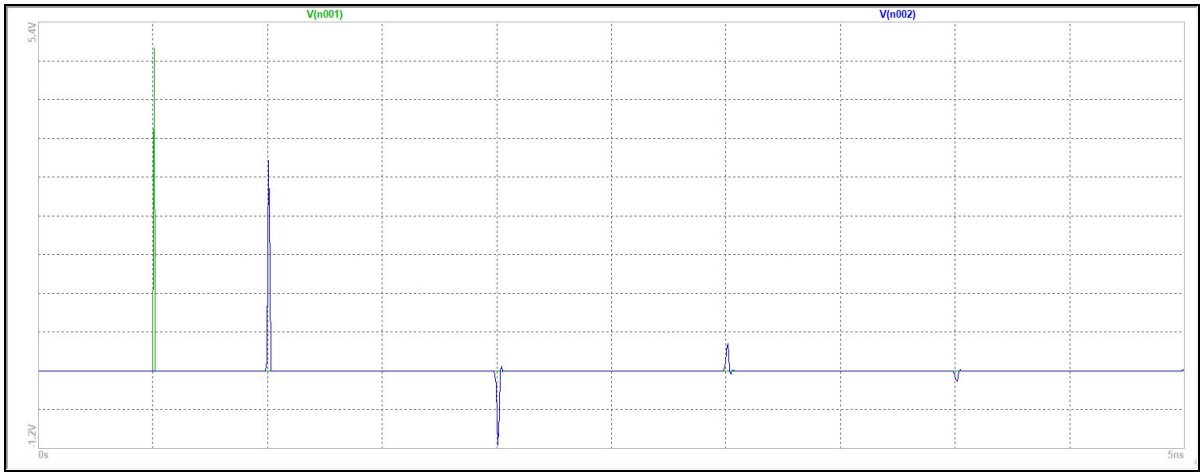


Figure 3-10: Voltage Plot of Figure 3-5 *V(n001) = V_{source} & V(n002) = V_L*

Results of Calculations and Graphs

The calculations used to solve for the source and load reflection coefficients, as well as the expression for the incident voltage, are the same as problem #3. The only difference is that the delay time is at 0.5 ns as shown in the equation: 5[$U(t)-U(t-0.5\ ns)$] Volts. Also, a subtraction operation was done to create the **Figure 3-12** graphs. This subtraction operation was taken from **Figure 3-8** since all values are the same.

In **Figure 3-11**, the original line is in black and is the same as problem #3. There is a second line in blue that shows the second step function that is delayed by 0.5 ns. As seen in the equation: 5[$U(t)-U(t-0.5\ ns)$] Volts, the 0.5 ns delay time is negative, which makes the voltage in the blue line have a negative value.

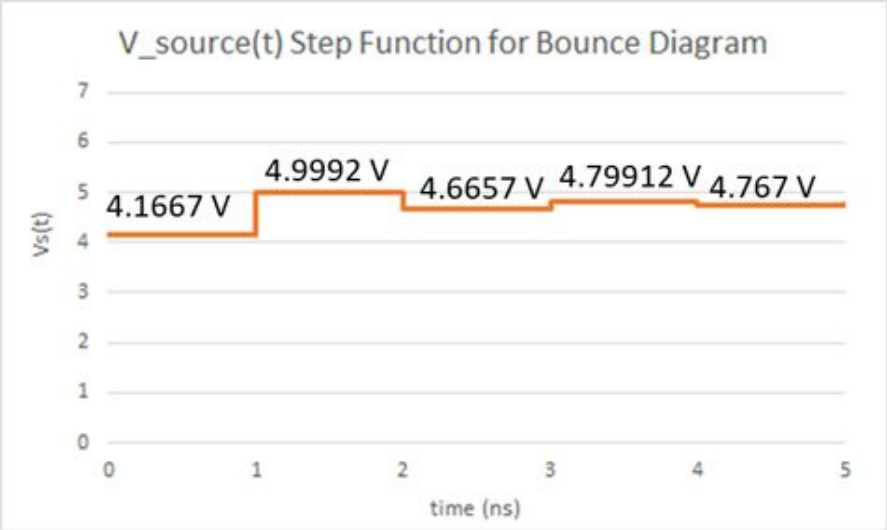
According to the first graph that shows the Vsource(t) shown in **Figure 3-12,** the source is shown to start at around 4.3 V. This starting point represents a dc voltage of amplitude 4.3 V that is switched on at t = 0 and stays at that value indefinitely. Problem #2 and #3 had a source that stayed indefinitely in this way. Refer to **Figures 3-2, 3-4, 3-6** and **3-8.** From there the voltages vary until eventually going to zero. This is because of the second component of the equation to create this phenomenon. When subtracting the second voltage to the previous voltage of the graph in **Figure 3-8,** the voltages for the graph **Figure 3-12** are created and as shown will eventually go to zero.

For the load graph in **Figure 3-12**, the graph continues to decrease to zero. The load voltages in problem #3 will also subtract each other until they go to zero. Calculations for how problem #4 **Figure 3-12** graphs were created is given below.

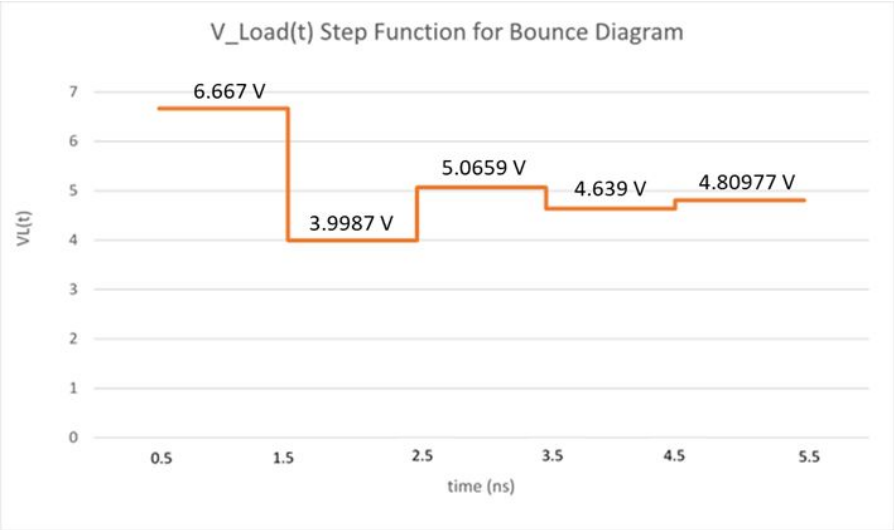
Calculations

These calculations describe how the graphs in **Figure 3-12** were calculated. The reason why they're calculated in this way is because the graphs in problem #3 can be used to create the pulse function in **Figure 3-12** by subtracting two step functions. Refer to Graphs in **Figure 3-12** for calculation results.

4.1667 - 0 = 4.1667
4.9992 - 4.1667 = - 0.8325
4.6657 - 4.9992 = - 0.3335
4.79912 - 4.6657 = 0.13342
4.767 - 4.79912 = - 0.03212



6.667 - 0 = 6.667
3.9987 - 6.667 = - 2.6683
5.0659 - 3.9987 = 1.0672
4.639 - 5.0659 = - 0.4269
4.80977 - 4.639 = 0.17077



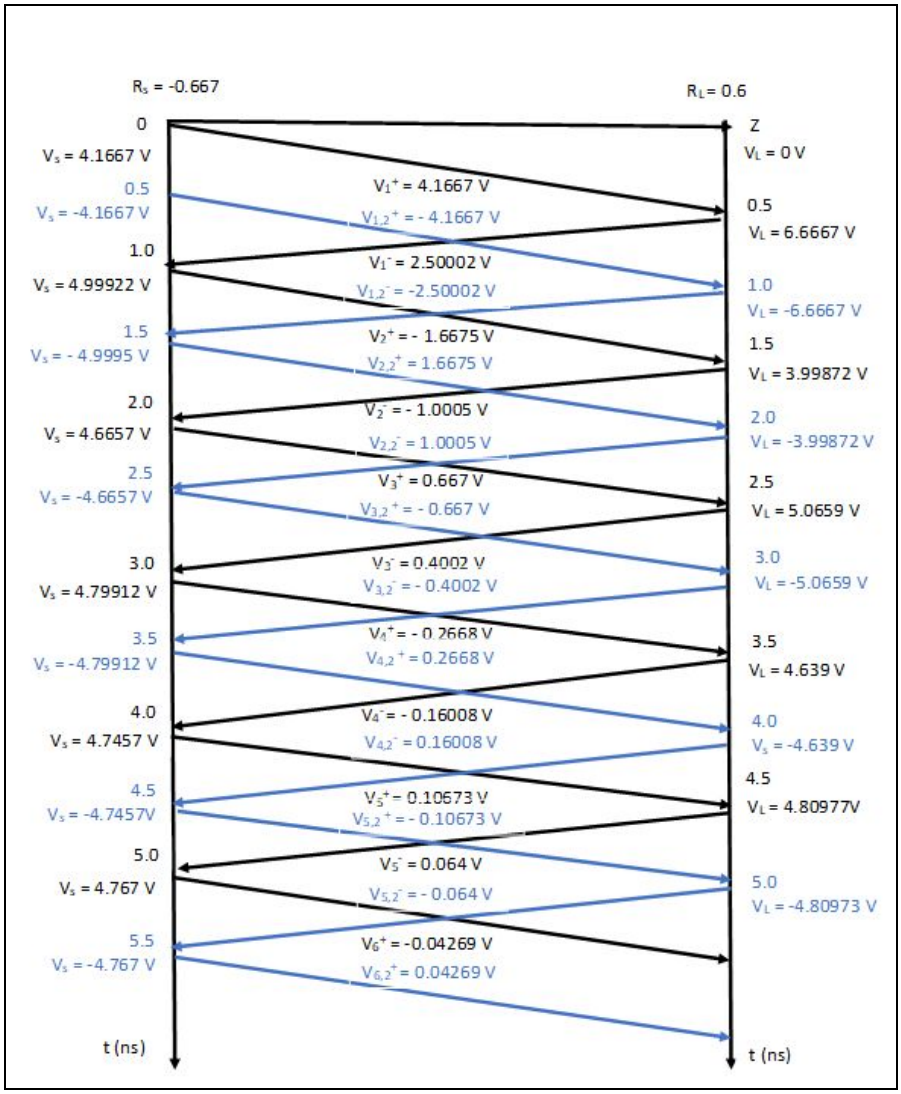


Figure 3-11: Bounce Diagram for Problem #4 Calculations Section

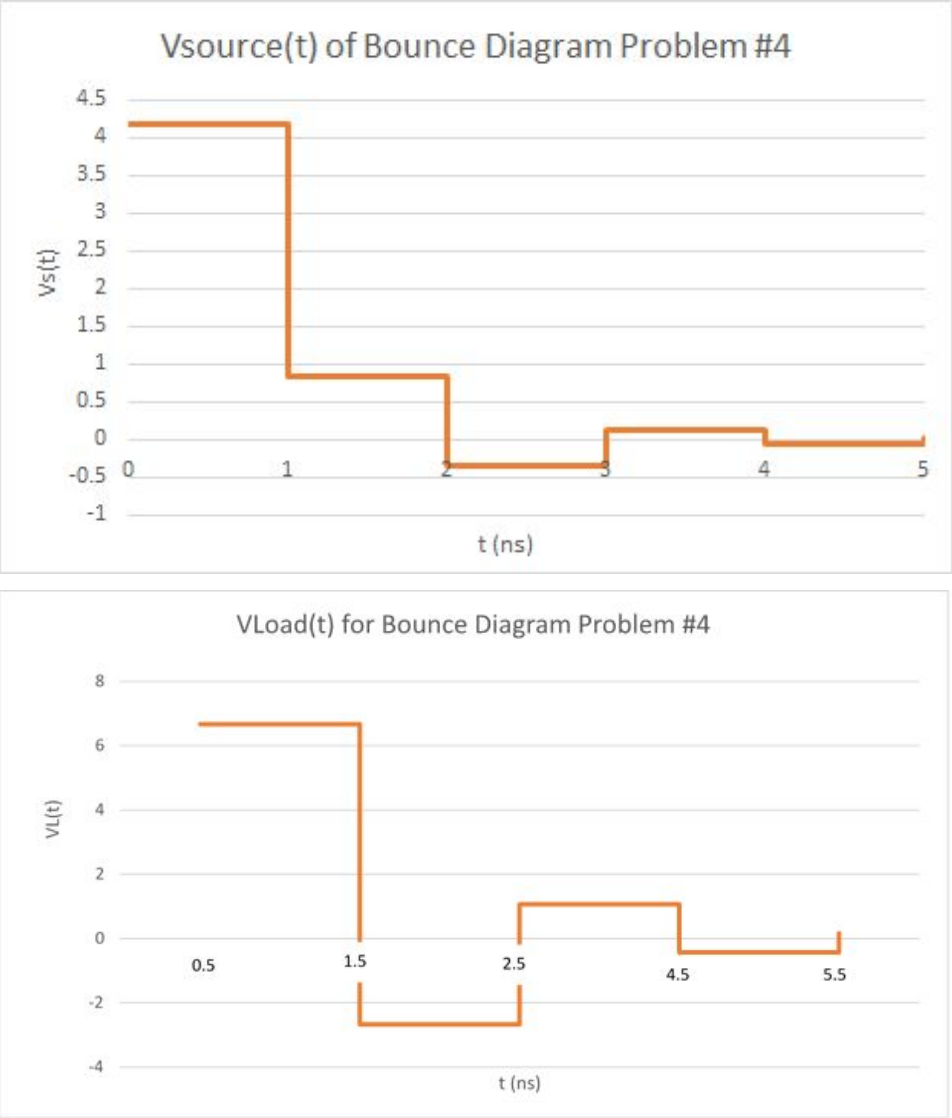


Figure 3-12: Vsource(t) and Vload(t) graphs for Problem #4

Conclusions

In conclusion, problem #4 analyzes a circuit with a pulse source. This pulse source creates an added step function. According to problem #3, this will allow the second voltage to be subtracted by the first voltage in **Figure 3-8** to create the pulse function in problem #4 **Figure 3-12**. The LTspice circuit and graph is changed compared to problem #3 by changing the delay time and the transient time to stop saving data to 5e-10. The T_{rse} and T_{fall} values were also changed to account for 1% of the delay time, which resulted in a value of 5e-12. This is because the delay time isn't zero anymore, it has a value. According to the LTspice graph, the subtraction of the 0.5 ns in the equation: $5[U(t)-U(t-0.5\ ns)]$ Volts created a different graph. One that resulted in a pulse and a decrease in voltage rather than a consistency in voltage that is shown in problem #3.

Problem 5

Discussions

LTSpice Results

Problem #5 describes what would happen if the pulse function graph was placed at 1.5e-9 (1.5 ns) instead of 0.5 ns. According to **Figure 3-13**, the time delay (Td) in the transmission line is the same (0.5 ns), but the T_{rise} and T_{fall} are different according to the time delay of the pulse source (1.5 ns). The pulse source is 5 V, source resistive impedance is 10 Ω, characteristic impedance is 50 Ω, and the load resistive impedance is 200 Ω.

Figure 3-14 shows the graph of the circuit in **Figure 3-13**. The graph is shifted over by 1.5 ns as expected. Also, it's noticed that the source in green (V(n001)) is smaller than the problem #4 LTSpice source in green (V(n001)) shown in **Figure 3-10**. This is because of the delay change to 1.5 ns. Due to the delay and the change in T_{rise} and T_{fall}, the voltages change values as shown in the LTSpice graph below. The V(n001) is smaller than before in problem #4, **Figure 3-10** and the V(n002) is larger than before in problem #4 in the same figure. Results for circuit and graph is shown below.

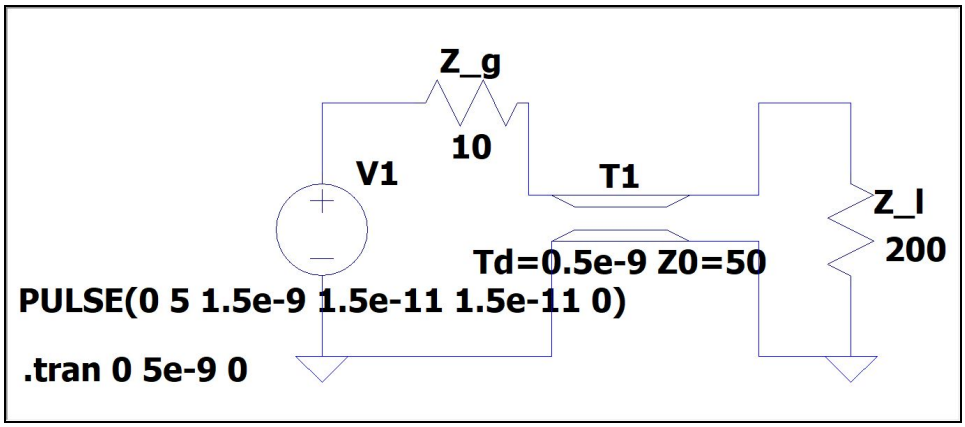


Figure 3-13: Transmission Line Circuit with Short Pulse of 1.5 ns

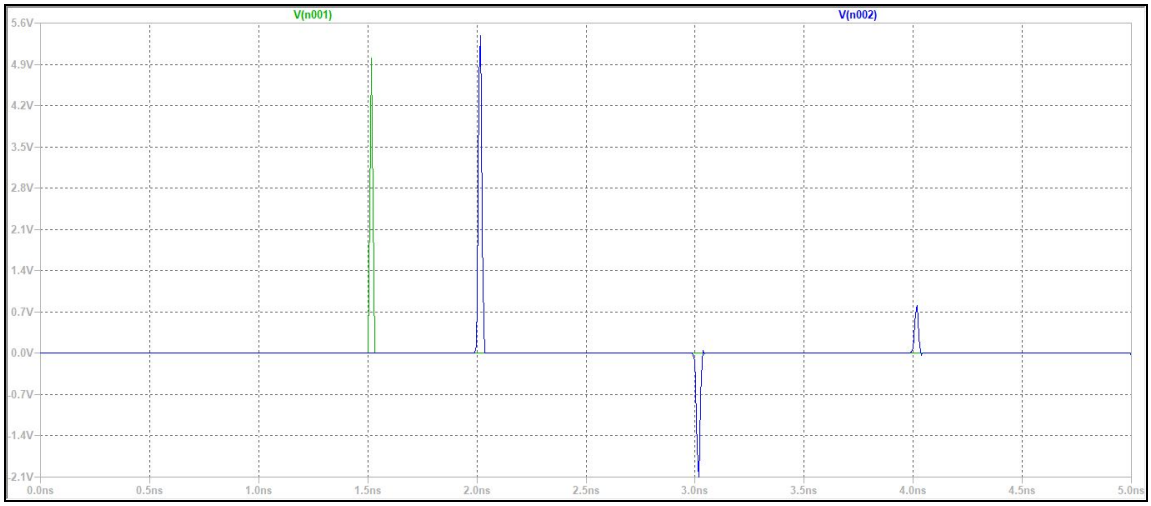


Figure 3-14: Voltage Plot of Figure 3-7 *V(n001) = V_{source} & V(n002) = V_L*

Results of Calculations and Graphs

For problem #5, the calculations are the same as in problem #3, but the delay time is increased to 1.5 ns. This would make the pulse longer and therefore start at a later time, according to **Figure 3-14**. The bounce diagram is shown below under **Figure 3-15** and the graph of the Vsource(t) and VLoad(t) graphs of the bounce diagram is also shown below under **Figure 3-16**. To see detailed calculations of this problem's bounce diagram and graphs, see problem #3 under Calculations.

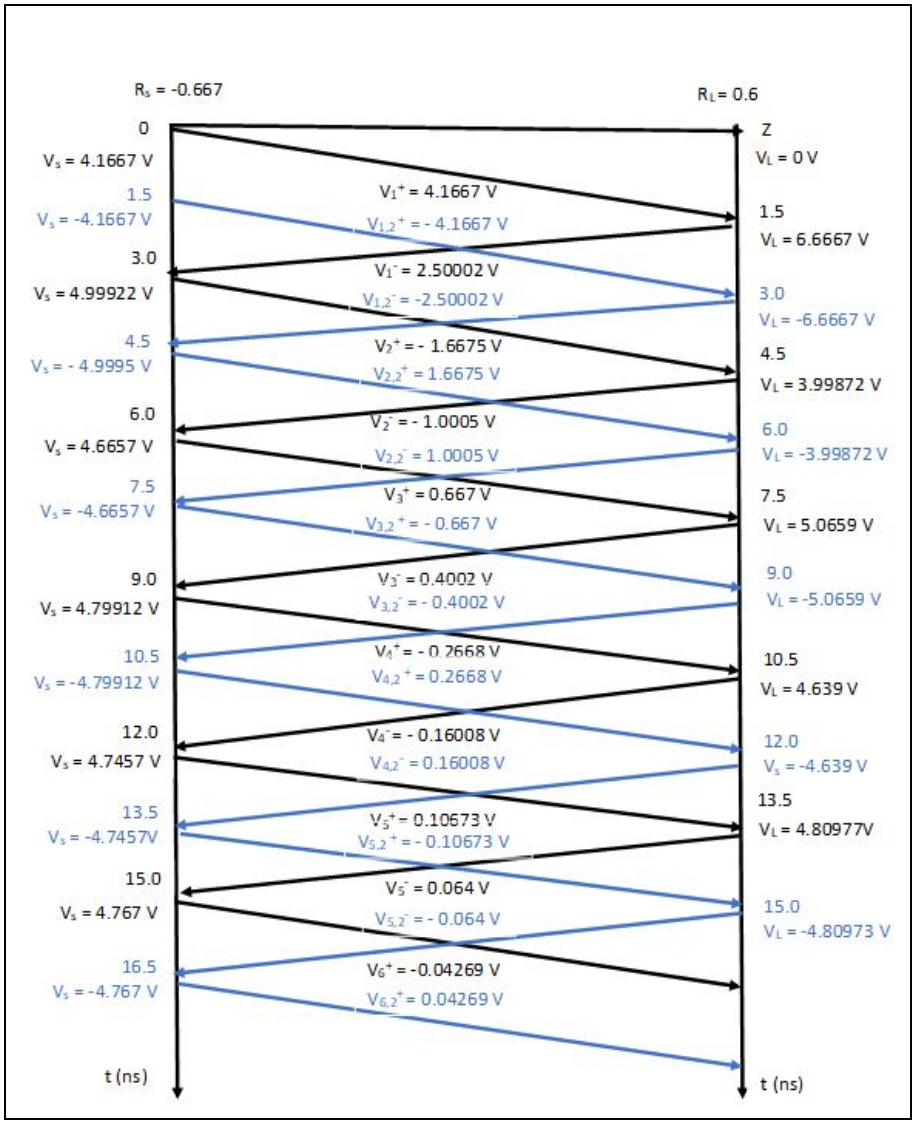
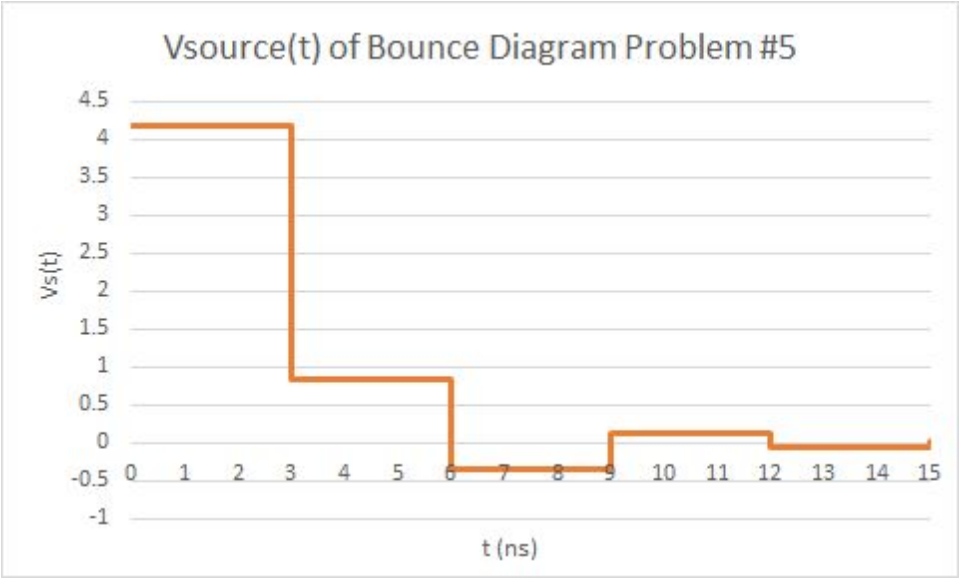


Figure 3-15: Bounce Diagram for problem #5



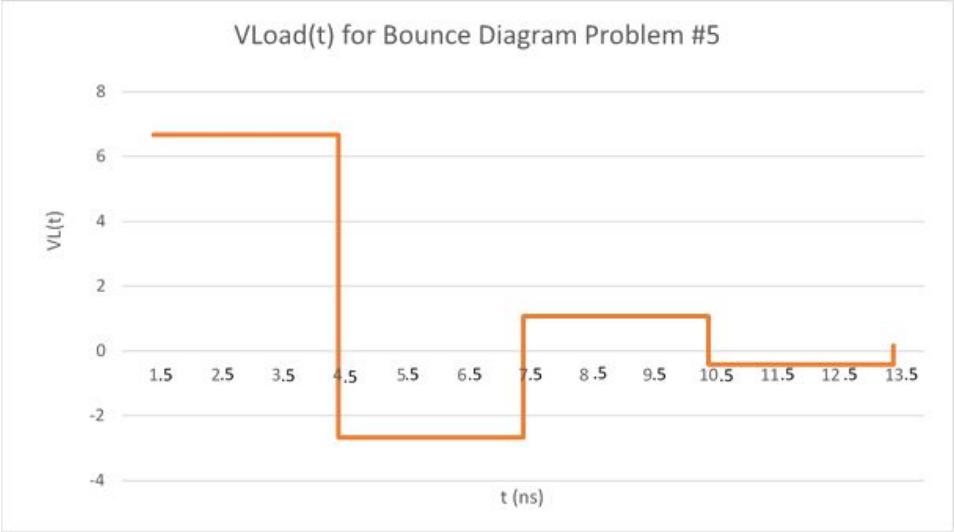


Figure 3-16: Vsource(t) and VLoad(t) Graph's for problem #5

Conclusions

In conclusion, the goal of problem #5 was to move the time delay from 0.5 ns in problem #4, to a time delay of 1.5 ns. This is to see how this could change the LTSpice graph. In general, with the exception of the time delay of 1.5 ns, the LTSpice circuit and graph as well as the calculations with the bounce diagram and excel graphs are all the same as in problem #4. Excel graphs match what the LTSpice graphs show for this problem which indicates that both graphs were accurately calculated and analyzed.

4. Reactive Terminations

Problem 6

Discussions

After appending a capacitor in place of the original load resistor in Problem 5, our team manipulated the pulse function to output a clock signal with a 50% duty cycle, 12.5 ns pulse width, and 0.2 s rise and fall times, as per the given instructions. **Figure 4-1** shows the circuit schematic that represents these changes while **Figure 4-2** shows the LTSpice-simulated output of this circuit schematic. In order to do this, we created a new pulse function that included a period value of:

$$T = 2 * pulse\ width + rise\ time + fall\ time$$
$$2 * 12.5ns + 0.2 + 0.2$$
$$T = 25.4ns$$

LTSpice Analysis

When our circuit simulation is first run, the output in **Figure 4-2** shows the source voltage increasing to 5 V over 0.2 s, staying constant at 5 V for 12.5 s, and then dropping off to 0 V over 0.2 s; this is exactly what we wanted. However, the response of the load voltage was unexpected, as it wavers drastically anywhere between about 9 V and -4 V.

Explain what is Happening at the Load

Because the load is now a CMOS inverter-equivalent capacitor, its voltage still sees reflections, but processes them differently. Voltage builds within a capacitor following the expression:

$$V_C(t) = V_{Source}(1 - e^{-\frac{t}{RC}})$$

Just like in previous problems, this unmatched load creates multiple reflections, resulting in an oscillating pulse that becomes damped over time (due to generator and line resistance). However, due to the above expression, the voltage output is far more curved than the resistor-type loads of previous problems, matching the logarithmic function $V_C(t)$.

Logic Threshold Problem

If the logic threshold for this CMOS circuit is approximately 2.5 V, false logic triggering will be produced, specifically about 3 ns following the source's change in logic (0 -> 1 or 1 -> 0). Looking at **Figure 4-2**, at this point in time, the load voltage reads a value of about 2.1 V or logic

value 0 while the source voltage reads a value of 5 V or logic value 1. This will produce some false logic triggering at this point in time.

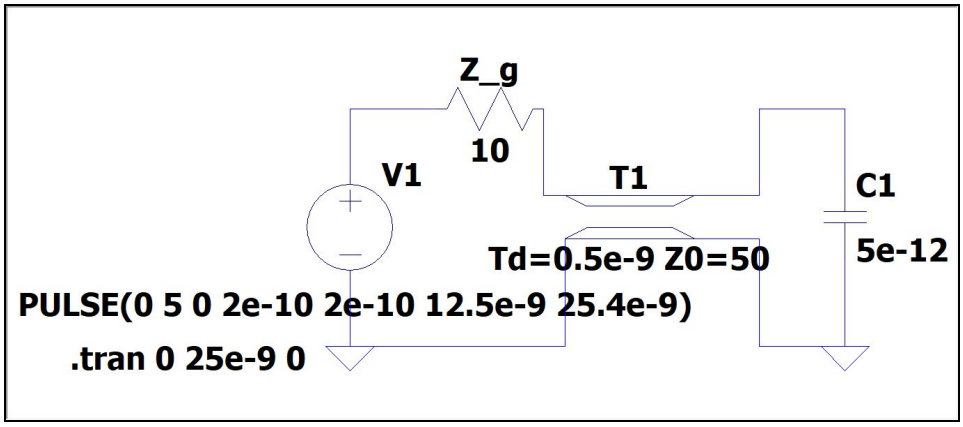


Figure 4-1: Transmission Line Circuit with CMOS-Equivalent 5 pF Capacitor & 12.5 ns Pulse Width

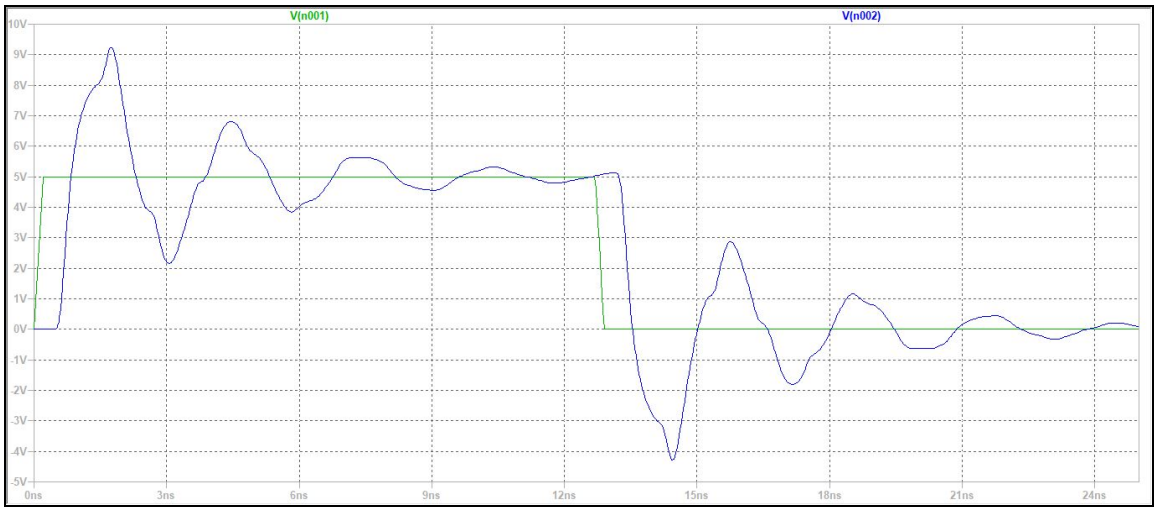


Figure 4-2: Voltage Plot of Figure 4-1 *V(n001) = V_{source} & V(n002) = V_L*

Conclusions

Problem 6 very closely represents the responses of our previous resistor-type problems. However, the curved output and clock source signals bring a new perspective to this problem, bringing up new questions in the comparison of capacitors to resistors.

Problem 7

Discussions

Repeating Problem 6 with longer rise times gives us the circuit as shown in **Figure 4-3** and the LTSpice simulation output of **Figure 4-4**.

LTSpice Analysis

Analysing our circuit and response, the output in **Figure 4-4** shows the source voltage increasing and decreasing over 2.5 ns intervals rather than 0.2. This response was also unexpected, showing a similar response to that of Problem 6, but with much less noise.

Explain what is Happening at the Load

After increasing the rise and fall times of the identical circuit to that of Problem 6, the load sees some reflections, but at much smaller amplitudes. After doing some research, our team thinks this is because longer rise and fall times are attributed to lower capacitive feedthrough and increased decoupling. This decoupling decreased the noise and voltage spikes that were in the voltage response of the previous problem. Our theory on the reasoning for this is that the source voltage signal becomes somewhat of a bypass capacitor where the slopes of the rise and fall times increase, becoming more similar to the sloped charging and discharging times characteristic of a capacitor.

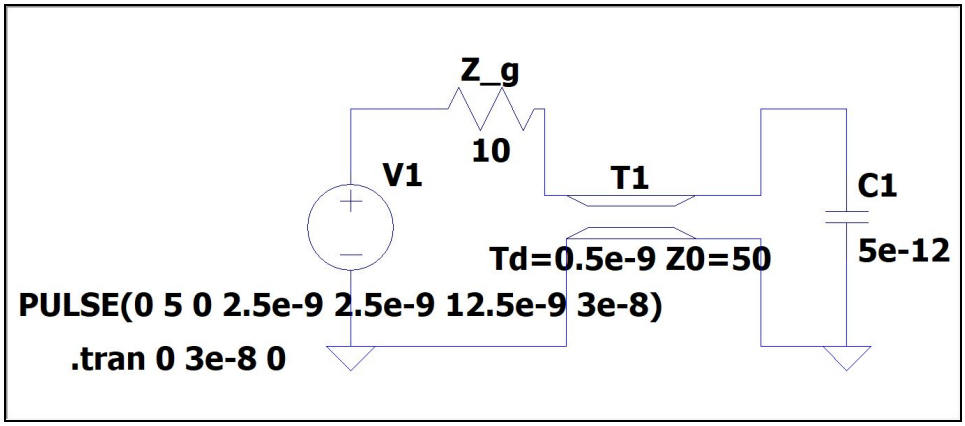


Figure 4-3: Transmission Line CMOS-Equivalent Circuit with 2.5 ns Rise/Fall Times

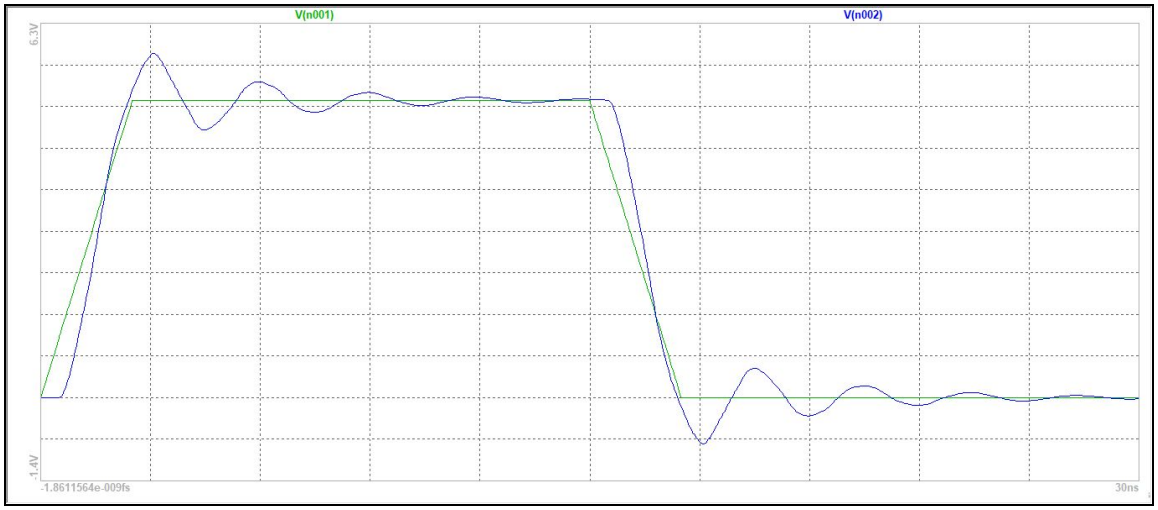


Figure 4-4: Voltage Plot of Figure 4-3 *V(n001) = V_{source} & V(n002) = V_L*

Conclusions

Although our team has no way of proving how the increased rise and fall times increase decoupling in the transmission line, we feel we learned a lot about the transient response of circuits during this problem. Helping us decipher and design more efficient circuits in the next few problems, this increase in rise and fall times leads to a better voltage response with extremely reduced noise, producing almost no false logic triggering whatsoever. Therefore, increasing rise and fall times serves to better the response of CMOS circuits.

5. Matching Techniques for Signal Integrity

Problem 8

5.1. Matching at the Source

Discussions

Impedance matching at the source required us to change Z_g to 50 Ω such that $Z_g = Z_0$. In doing so, our circuit (**Figure 5-1**) was run through the LTSpice Simulator to output an extremely matched signal with no obvious reflections (**Figure 5-2**).

LTSpice Analysis

Looking over **Figure 5-2**, our team noticed that the only difference between the input source voltage and output voltage response were the small curves created by the capacitor as it charges and discharges at a logarithmic rate. Basically, we observe almost no reflections.

Results of Calculations

From our calculations, the reflection coefficient at the source is very close to zero. This means that there is no reflected signal for the case of the series match at the source.

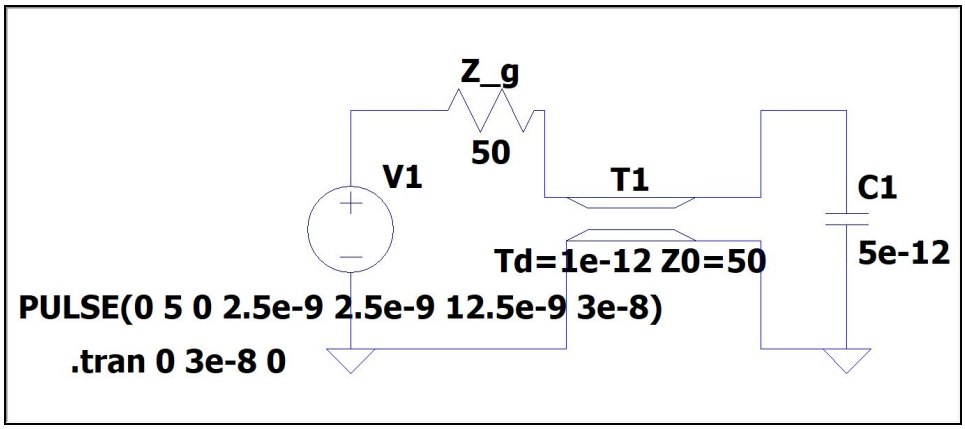


Figure 5-1: Source-Matched CMOS-Equivalent Transmission Line Circuit

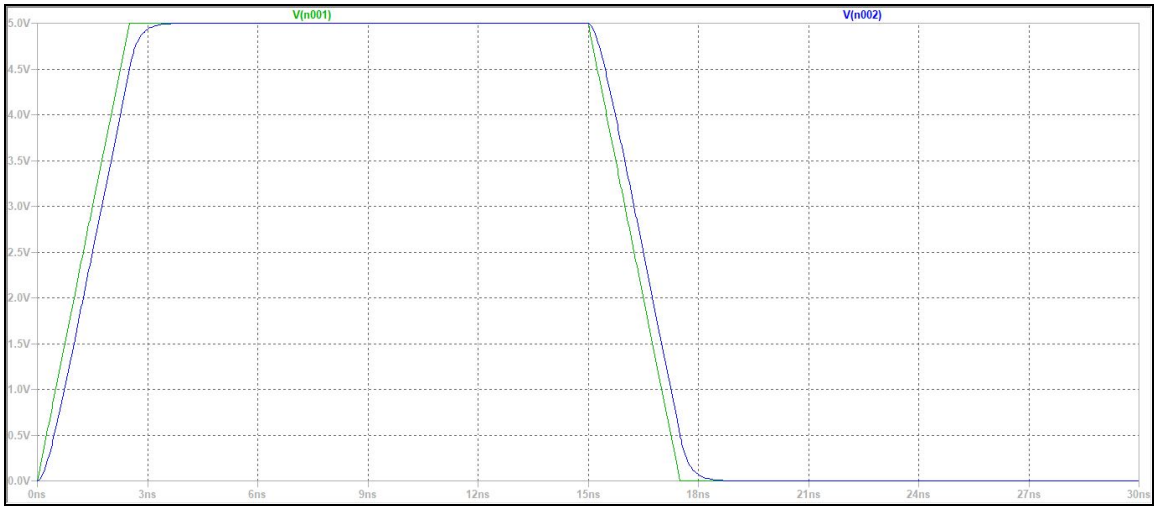


Figure 5-2: Voltage Plot of Figure 5-1 *V(n001) = V_{source} & V(n002) = V_L*

Calculations

The expression for the reflection coefficient at the source:

$$\Gamma_s = \frac{Z_g - Z_0}{Z_g + Z_0} = \frac{(50) - (50)}{(50) + (50)} = 0$$

$$\Gamma_s = 0$$

Since the source reflection coefficient depends only on real values, it can easily be converted between the phasor and time domain; therefore:

$$\Gamma_s(t) = 0$$

Conclusions

Overall, we observed no reflections and calculated almost none.

Problem 9

5.2. Matching at the Load

Discussions

Impedance matching at the load required us to add another resistor in parallel prior to the load of the transmission line. Our circuit is shown in **Figure 5-3** and our voltage response is shown in **Figure 5-4**.

LTSpice Analysis

Following the loading of the response in **Figure 5-4**, we observe again nearly no reflection in the response voltage signal. However, we do observe that the response voltage signal's amplitude is decreased by a small factor. We attribute this to the fact that the load now acts like a voltage divider.

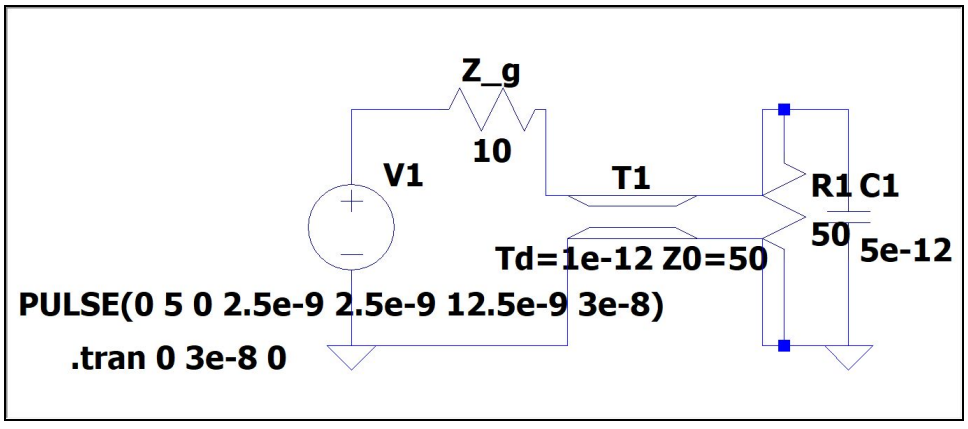


Figure 5-3: Load-Matched CMOS-Equivalent Transmission Line Circuit

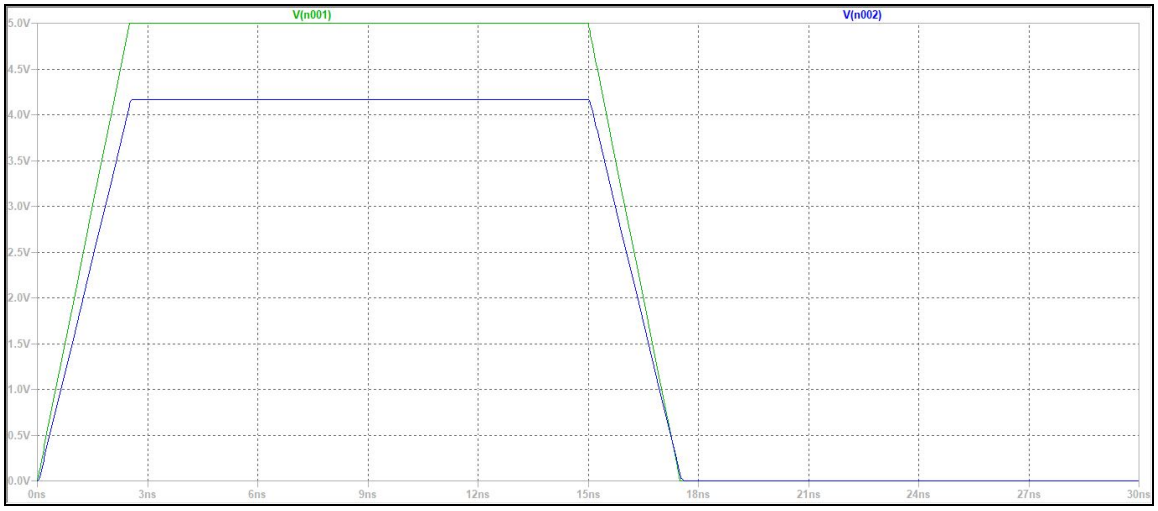


Figure 5-4: Voltage Plot of Figure 5-3 *V(n001) = V_{source} & V(n002) = V_L*

Calculations

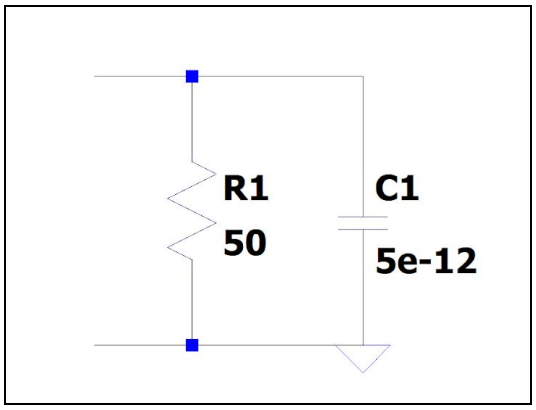


Figure 5-5: Zoomed-In Schematic of the Load

Expression for Reflective Coefficient at the load:

$$\Gamma_L(s) = \frac{Z_L - Z_0}{Z_L + Z_0}$$

$$= \frac{-sRC}{2 + RC} = -1 + \frac{2}{RC} * \frac{1}{s + \frac{1}{RC}}$$

Take the Laplace Transform:

$$\Gamma_L(t) = -\delta(t) + \frac{2}{RC} e^{\frac{-t}{RC}}$$

Conclusions

Overall, this portion of the lab was relatively complicated, but very educational. Again, we saw almost no reflections and calculated almost no reflections other than the slight curvature found at the edges of the response voltage. When compared to the previous problem, the voltage response seems to have less of a defined curvature, which is mainly due to the fact that the

effect from the capacitor's voltage is diminished due to being incorporated into a voltage divider (**Figure 5-5**).

Problem 10

5.3. Series Matching at the Source End & Parallel Matching at the Load End

Discussions

Problem 10 combined both matching the source and the load. Our circuit is shown in **Figure 5-6** while the subsequent voltage response is shown in **Figure 5-7**. Simultaneously matching the source and load results in an output signal that is half the amplitude of the original voltage signal. Although both resistors are impedance matched, the resistor and capacitor in parallel divide the voltage such that both sides are unmatched. This is much like Problem 9, which we also attributed to the voltage divider having a mismatch with the opposite side of the circuit.

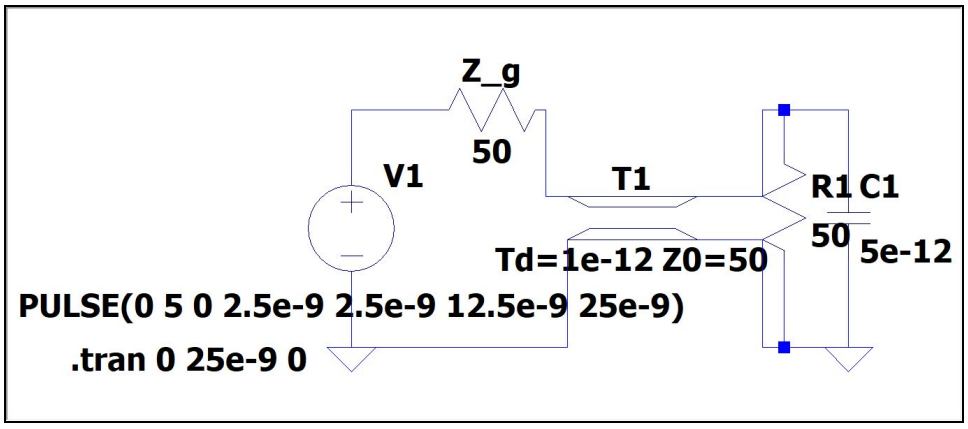


Figure 5-6: Source-Matched & Load-Matched CMOS-Equivalent Transmission Line Circuit

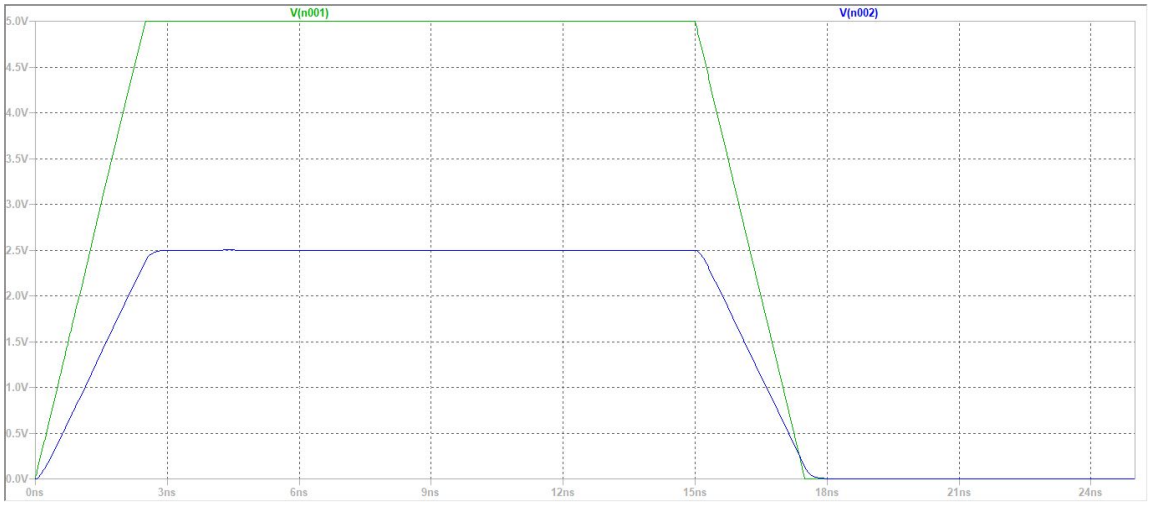


Figure 5-7: Voltage Plot of Figure 5-3 *V(n001) =* V_{source} *& V(n002) =* V_L

Conclusions

After analyzing all of our results, we concluded that the voltage divider was evenly spit, decreasing the voltage by half. This result is understandable because the characteristic impedance attempts to match with the source and the load at the same time. Because of this, only half of the signal is reflected, leaving about half the signal in our voltage response.

Conclusion

After completing all of the problems of this project, we propose the best combination of techniques that one could use to maintain Signal Integrity for CMOS circuits as a circuit purely parallel matched at the load with Z_g=0 like shown in **Figure C-1**. The resulting voltage response is also shown in **Figure C-2**.

From this graph, we can see that the source voltage lines up almost perfectly with the voltage response, proving that this is the best circuit design for maximum power transfer. We theorize this is because there is no resistance for the source to depend on, so the transmission line becomes purely based on the load.

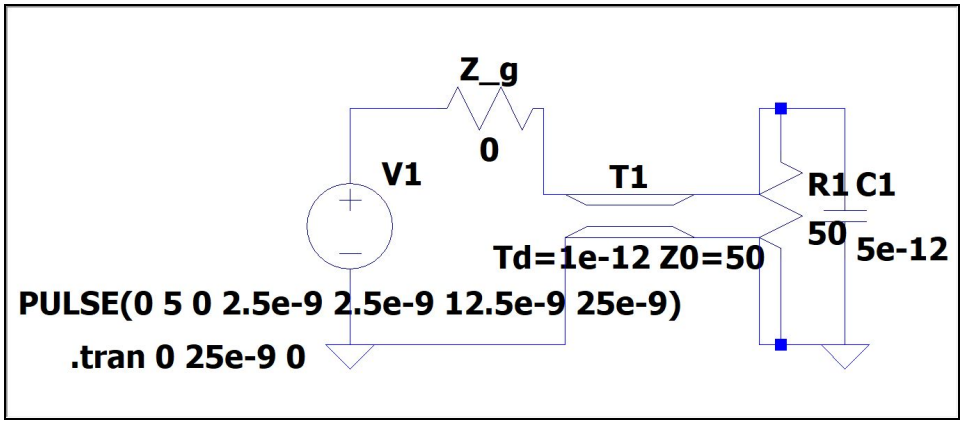


Figure C-1: Proposed High Signal Integrity CMOS-Equivalent Circuit

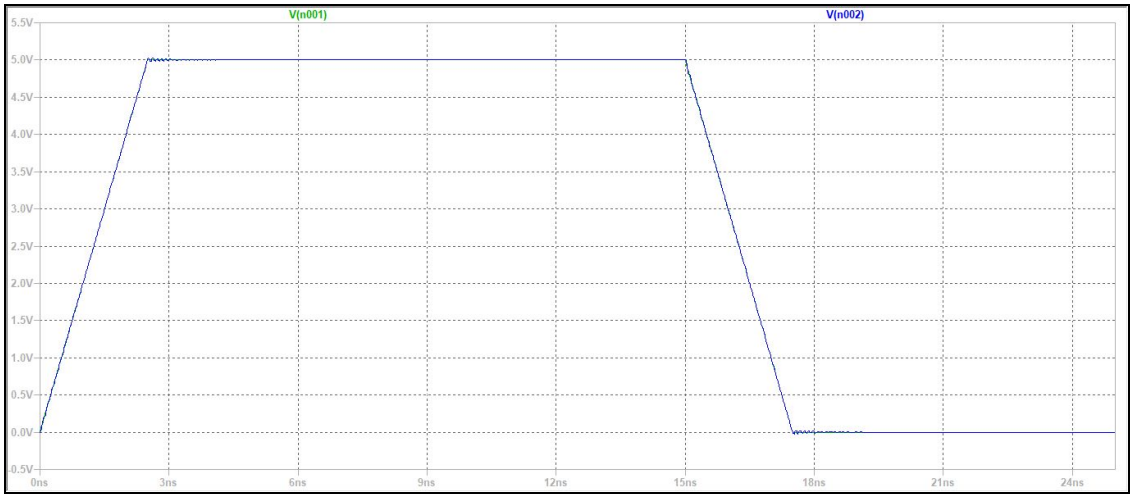


Figure C-2: Voltage Plot of Figure 6-1 *V(n001) = V_{source}* **=** *V(n002) = V_L*