B EE 361 Spring 2020

Computer Project: Transients on Transmission Lines

Instructor: Dr. Walter Charczenko
Due: Tuesday, May 30, 2020

Team Name: _____
Student Names: _____
Student ID's: _____
Total Score: _____

This computer project will be completed in teams of two people. Each team will choose a team name of their choice. When the project is completed, each team will submit a single report in a Word format (printed). Each member of the team will be responsible for their representative portion of the presentation and the report. However, (as in life when working on group projects) the team will receive a single grade.

This project will require access to a SPICE circuit simulator. PSpice AD Lite and LTSpice are available as freeware downloads on the internet. There will also be a version of LTSpice available on the computers in the EE laboratory. All circuits, equations, and results in this project should be copied and pasted into a full **Word** format report (**no** handwritten equations, plots, or diagrams). **Discussions should be written with great detail in the report, including a couple of paragraphs for each part of the report using clear and concise terms.** Plots of simulations should be used to support your conclusions. **All plots and their scales, axis, and labels need to very clear!** All reports will be printed out and handed in. Let the fun begin!

The coversheet for the report should include all of the information given at the top of this page.

1. Introduction

In class we will be studying *Transients on Transmission Lines* (Ulaby section 2-12). Transient analysis is useful in dealing with digital and wideband signals that exist in digital chips, circuits and computer networks. In class, we derived equations and presented a closed form analysis of single-frequency, time-harmonic signals under steady-state (SS) conditions. In general, transients are more difficult to analyze and to obtain closed form solutions. This is especially true when performing transient analysis of reactive loads. It is for this reason that a circuit simulator such as SPICE is very useful in gaining insight into digital circuit behavior. In this computer lab, we will analyze a CMOS circuit that is laid out on a printed circuit board (PCB).

2. Transmission Line Representation of a CMOS Circuit

A CMOS circuit shown in figure 2-1 below consists of two CMOS inverters (buffers) with a conductive interconnect (land line on a printed circuit board-PCB) between them.

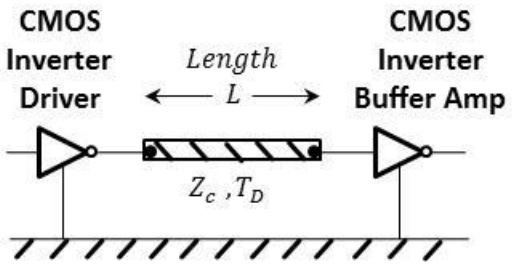

Figure 2-1. CMOS data line circuit on a PCB.

A transmission line representation of the circuit in figure 2-1 is shown below in figure 2-2. In this circuit, the output of the CMOS inverter number 1 is represented by a Thevenin equivalent voltage source with a Thevenin equivalent generator resistance $R_g = 10\ \Omega$. The input of the CMOS buffer number 2, is represented by a load impedance Z_L. The land trace interconnect between the inverters is modeled as a transmission line.

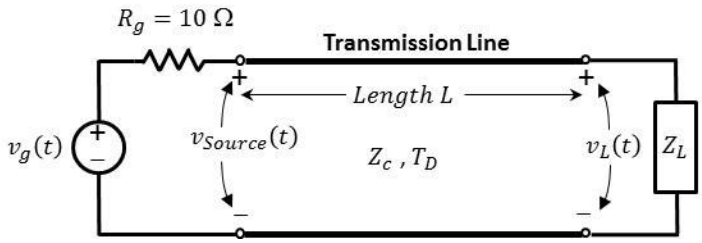

Figure 2-2. Transmission Line representation of the circuit I figure 2-1.

A cross section of the land line on the circuit board is shown in figure 2-3. The width of the top conductor is 10 mils. The thickness of the FR-4 (glass-epoxy) circuit board is 47 mils. To calculate problem 1, look up the permittivity of the FR-4 circuit board material on the Internet.

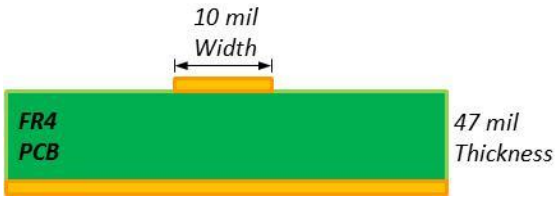

Figure 2-3. Cross-section of the land on the FR-4 PCB.

Problem #1: What type of two conductor transmission line in chapter 2 of Ulaby, does this land line most resemble? Show all of your work and calculate the characteristic impedance of this *lossless* line. What is the delay time for pulse to travel from CMOS Inverter #1 to CMOS Inverter #2 for a land line that is 10 cm long? If we wanted to limit the delay time to less than 0.5 ns, what would the maximum length of this line be?

Now we are ready to analyze this circuit with the SPICE simulator.

3. Purely Resistive Terminations

Construct and a SPICE model consisting of a VPWL source with a resistive source impedance of $Z_g = R_g = 10\,\Omega$; a lossless transmission line with a characteristic impedance of Z_c that was calculated in problem #1, and delay time of 0.5 ns. In problems #2 through #6, treat the load impedance as purely resistive and in problem #2 use $Z_L = R_L = 200\,\Omega$.

Problem #2: Excite this circuit with a 5 Volt step function $(5U(t)\ Volts)$. Plot the voltage at the source, $v_{Source}(t)$, and load ends, $v_L(t)$, over a time span of 0 to 5 ns. Using the technique of bounce diagrams explain how your solution compares with the exact solution derived using the technique given in Ulaby section 2-12.

Problem #3: In this problem you have re-designed the circuit board trace such that its' characteristic is now $Z_c = 50\,\Omega$. All other parameters and circuit elements are the same as before. Repeat problem #2. Describe what is different in this case as opposed to the results that you simulated in problem #2.

Problem #4: Given the same circuit as in problem #3, set up a single short pulse on generator VPWL such that a single pulse at time $t = 0$ is generated with a pulse width (duration of pulse) equals the length of the delay line time delay of 0.5 ns $(5[U(t) - U(t - 0.5\ ns)]\ Volts)$. The pulse rise and fall times should each be 1% of the pulse width. Run your simulation, plot the results, and explain what is happening. Adjust

Problem #5: Repeat problem #4 with a long (as compared to the transmission delay time) pulse of 1.5 ns. Program the same rise and fall times as you did in problem #4. Again, adjust the time span of your plots so that you can see everything that is happening.

4. Reactive Terminations

In the previous section we have modeled purely resistive loads. The input to a CMOS inverter is reactive. The input to a CMOS inverter can be represented as a $C = 5\ pF$ shunt capacitor. Insert this shunt capacitor into your circuit model instead of the load resistor R_L.

Problem #6: Repeat problem #5 with the new capacitive load and use a new SPICE pulse generator VPULSE that simulates a digital clock signal. The new clock signal will have a repetitive pulse that will have a 50% duty cycle, a pulse width of 25x the delay time of the transmission line (12.5 ns), and rise/fall times of 0.2 ns. Plot what is happening at the load and the generator (clock) signal for 1 duty cycle of the clock. Explain what is happening at the load. If the threshold for the CMOS circuit is halfway between logic level 1 and logic level 0, (i.e. approximately 2.5 Volts), could this produce false logic triggering in this circuit?

Problem #7: Repeat problem #6, however now change the rise and fall times to 2.5 ns. Run the simulation, plot the clock and load signals for one clock duty cycle. Explain in detail what you think is going on at the load.

5. Matching Techniques for Signal Integrity

As was seen in the previous section, impedance mismatches at the generator (Thevenin source) and at a reactive load can spoil the signal integrity of digital signals, thus resulting in high Bit Error Rates (BER). We will try a number of techniques to see if we can correct some of these problems in the *Integrity of the Signals* (**Signal Integrity**).

5.1. Matching at the Source

Problem #8: In your SPICE model, place a 40 Ω resistor in series prior to the input to the transmission line. Derive an expression for the reflection coefficient Γ_{Source} at the source and explain what the reflected signal is for the case of this series match at the source? Use the same clock signal that you used in problem #6 and run the simulator. Plot the clock and load signals for one duty cycle. What do you observe?

5.2. Matching at the Load

Problem #9: Now, in your SPICE model, place a 50 Ω resistor in parallel (shunt) prior to the load of the transmission line. Derive an expression for the reflection coefficient Γ_L at the capacitive load, and explain what the reflected signal is for the case of this parallel match at the load? Use the same clock signal that you used in problem #6 and run the simulator. Plot the clock and load signals for one duty cycle. What do you observe?

5.3. Series Matching at the Source End and Parallel Matching at the Load End

Problem #10: One would think that the best one could do, would be a simultaneous combination of the two matching techniques (series matching at the source and parallel matching at the load) that we have simulated. Set up this SPICE model and run your simulation as before. What do you observe at the load? What happened? Can you explain this in terms of your previous models? **Conclusion:** Propose what you think would be the best combination of techniques that one could use to maintain *Signal Integrity* for these CMOS circuits.