NanoVNA & WiFi Antenna Z-Match Project

B EE 454 A: RF & Microwave Engineering (Spring 2021)

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Problem 1

Data Files & Topologies

Circuit I - *Austin*

Using AWR Microwave Office DE, I plotted out *S11 Circuit I.s1p* on the smith chart in *Figure 1*.

Based on this data, I chose **topology B**, which is a series LC circuit with a Parallel resistor. After testing many different topologies, I found this circuit gave the closest response to the plotted data when plotting each topology on a smith chart. Additionally, I was led to believe that this topology was more likely because the plotted data denoted a series LC portion of the circuit since the response was both in the upper and lower portions of the smith chart. Since the response did not touch the left edge of the smith chart, this led me to believe that there was a resistor involved in the circuit as well. Moreover, a similar image of a smith chart response was given on circuit #2 of the RF Demo Kit, leading me to this topology.

A schematic diagram of topology B without component values is shown in *Figure 2*.

Figure 1: Circuit 1 Smith Chart

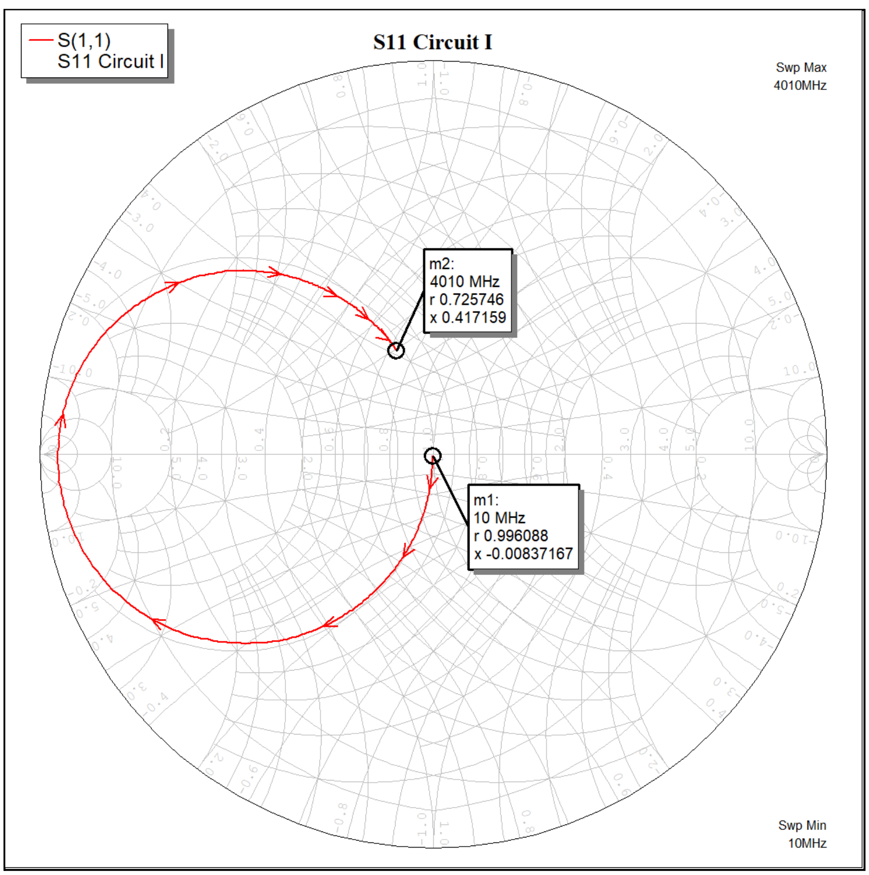
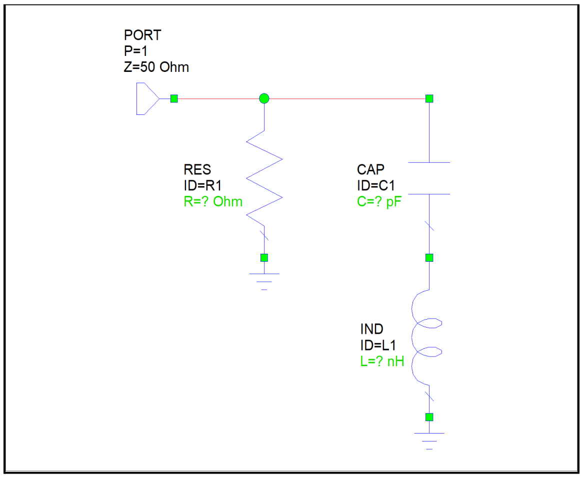


Figure 2: Topology B without Component Values



Circuit II - *Huy*

Using AWR DE to plot the S11 Circuit 2.s1p file we get the smith chart shown in Figure 3. Based on the Smith chart the topology used was topology F, the parallel RLC circuit. What led me to believe this was in order for the smith chart move from the center to the right side of the smith chart in the inductive region was for an inductor to be in parallel to the ports. Afterwards we see that the plots move in a clockwise motion in the capacitive region that means the circuit must also have a capacitor in parallel as well. Finally to make this smith chart not all imaginary values and not touch the right edge of the smith chart, we needed a resistor in parallel. That is how I was able to find what topology to use.

A schematic diagram of topology F without component values is shown in *Figure 4*.

Figure 3: Circuit 2 Smith Chart

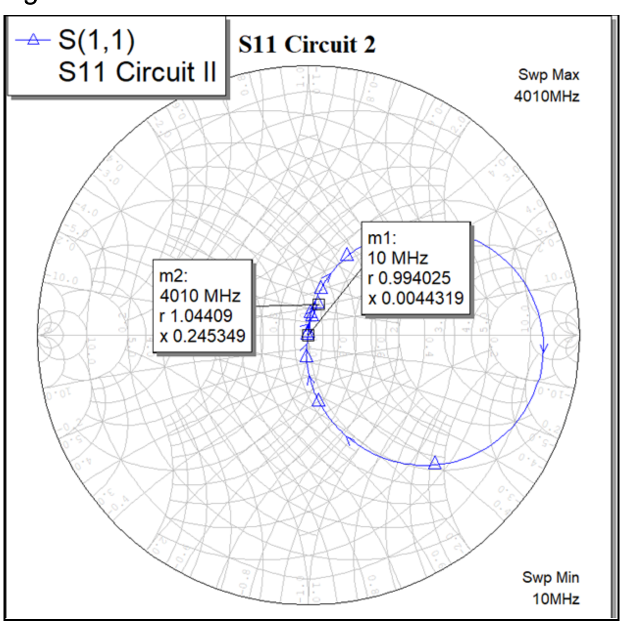
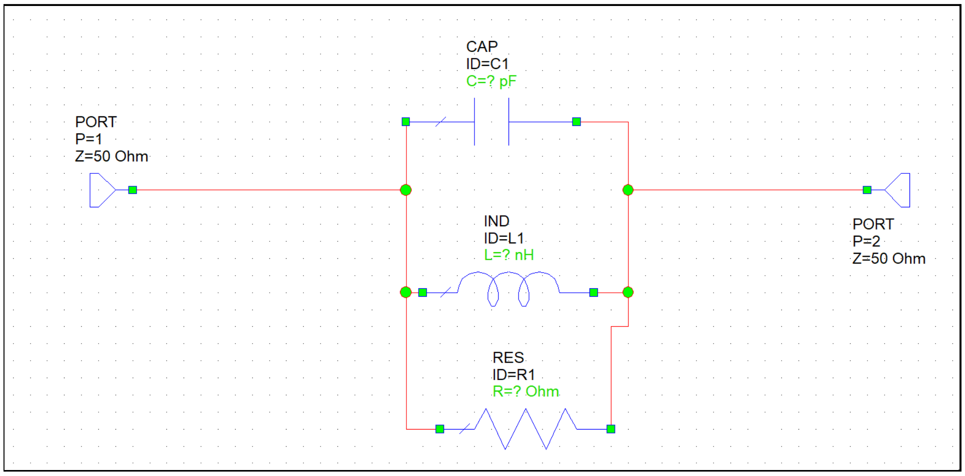


Figure 4: Topology F without Component values



Problem 2

Finding Component Values

Circuit I - *Austin*

Using AWR Microwave Office DE, I tried and simulated many different combinations of component values until I found one that was closest to fitting the curve of Circuit I. I found that having the parallel resistor value at 50 Ω completed the overall shape of the smith chart curve while editing the Capacitor and Inductor values completed the circumference of the curve.

The circuit schematic with component values is shown in *Figure 5* and its smith chart response is shown in *Figure 6*.

Figure 5: Topology B with Component Values

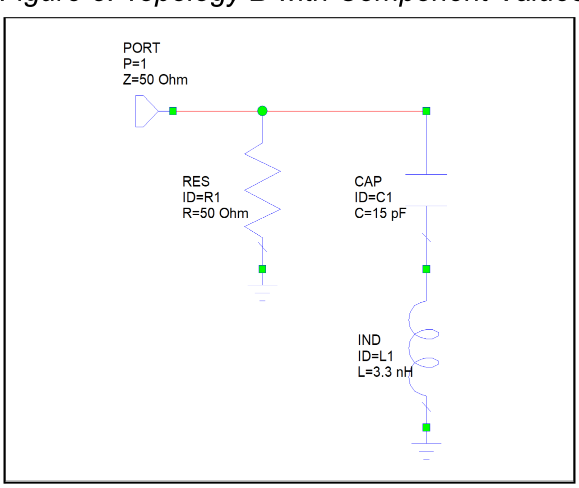
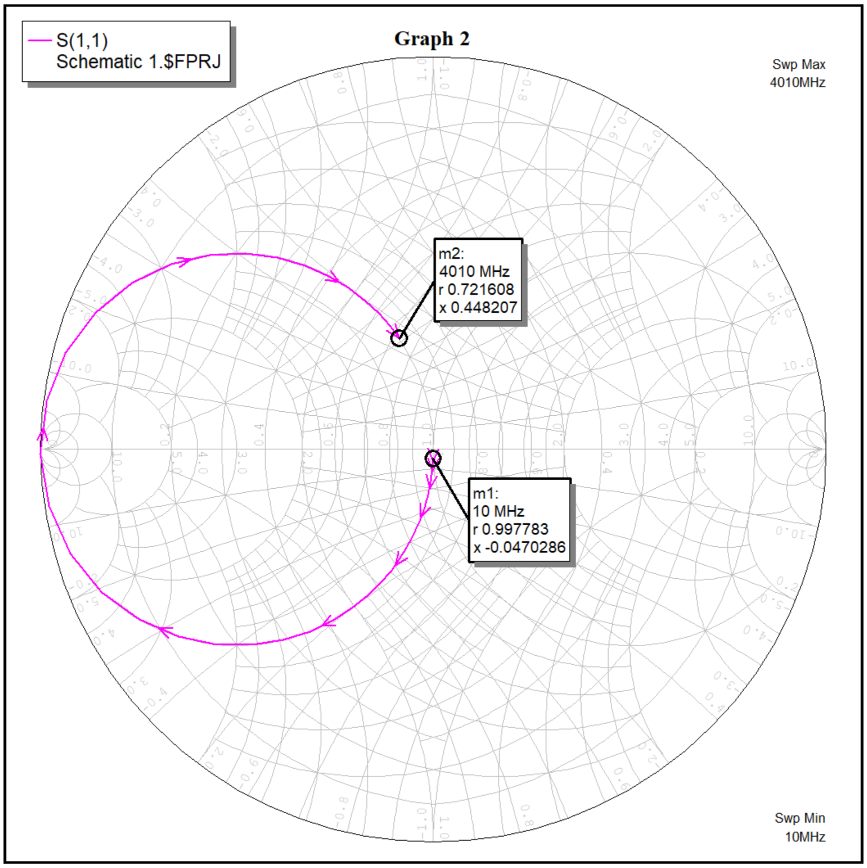


Figure 6: Topology B Smith Chart Response



Circuit II - *Huy*

Using AWR DE after finding what topology the smith chart was, I started testing different components values to have my smith chart match closely to the S11 Circuit 2.s1p file. I found that having an 800Ω resistor in parallel was able to pull the circle from the right edge, while having a 5 nH inductor in parallel was able to complete the half circle in the inductive region, finally having a 10 pF capacitor in parallel it was able to go all the way around the capacitive region creating a full circle.

The circuit schematic with component values is shown in *Figure 7* and its smith chart response is shown in *Figure 8*.

Figure 7: Topology F with Component Values

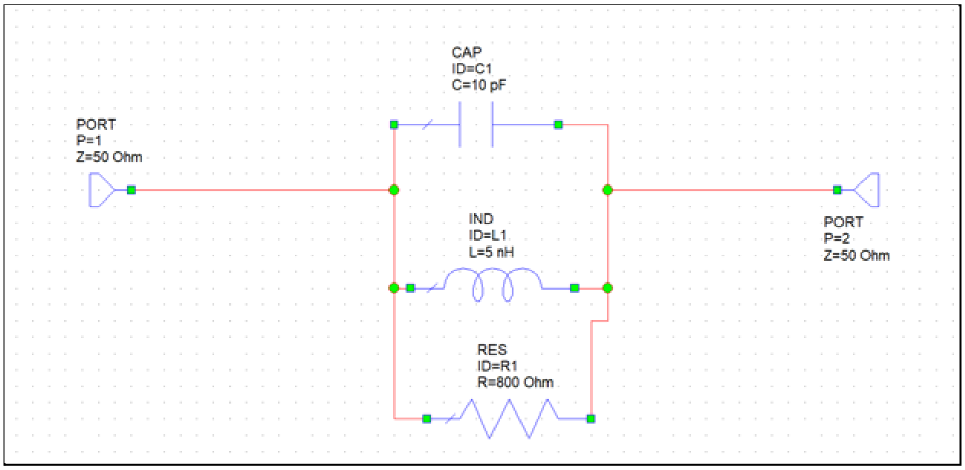
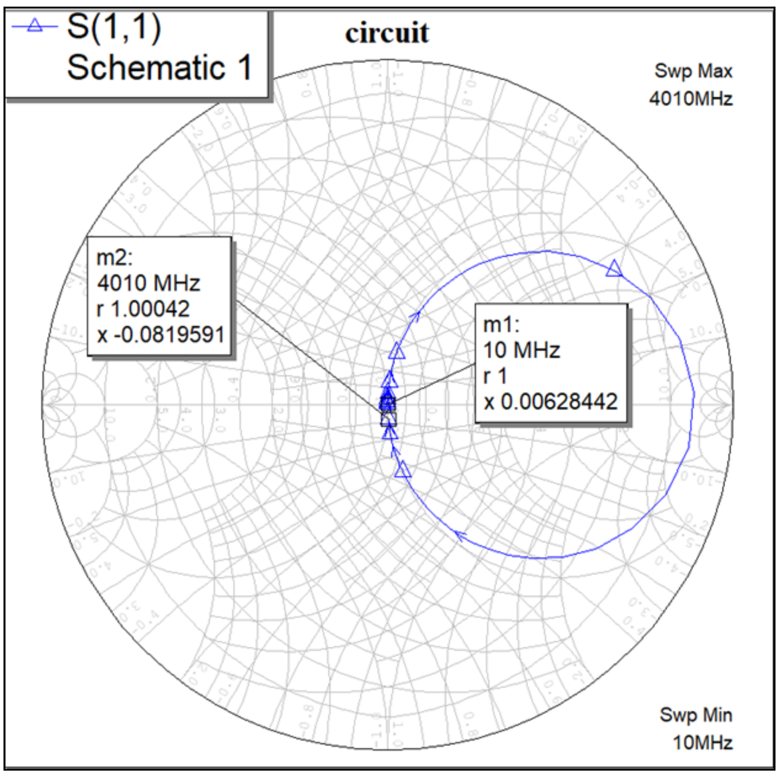


Figure 8: Topology F Smith Chart Response



Problem 3

RF Demo Kit RLC & LC Frequency Sweeps

Circuit #1 RLC - *Austin*

After calibrating the NanoVNA with the RF Demo Kit, I attached the SMA connector probe to the CH0 port of the NanoVNA and began sweeping over the specified frequency range. After some trial and error, I was able to successfully plot S_{11} on the NanoVNA's smith chart (*Figure 9*) as well as from an AWR DE Schematic file I created based on the measured topology (*Figure 11*). The topology was given as **topology D**, which is a series LC circuit with a resistor in parallel with the inductor. From this topology, I was able to create a schematic file (*Figure 10*) and find the following RLC values:

R = 50 Ω
L = 100 nH
C = 100 pF

Figure 9: NanoVNA Results

Figure 10: Topology D Schematic

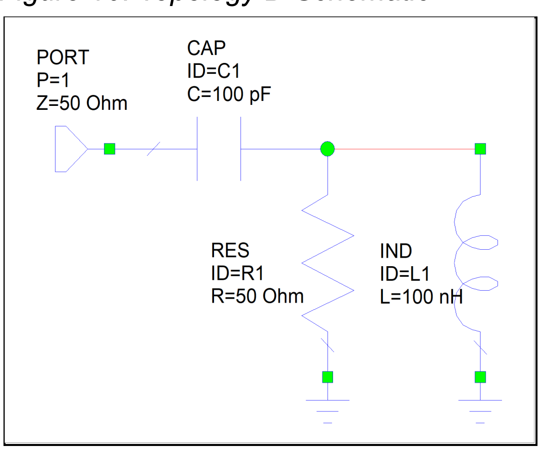
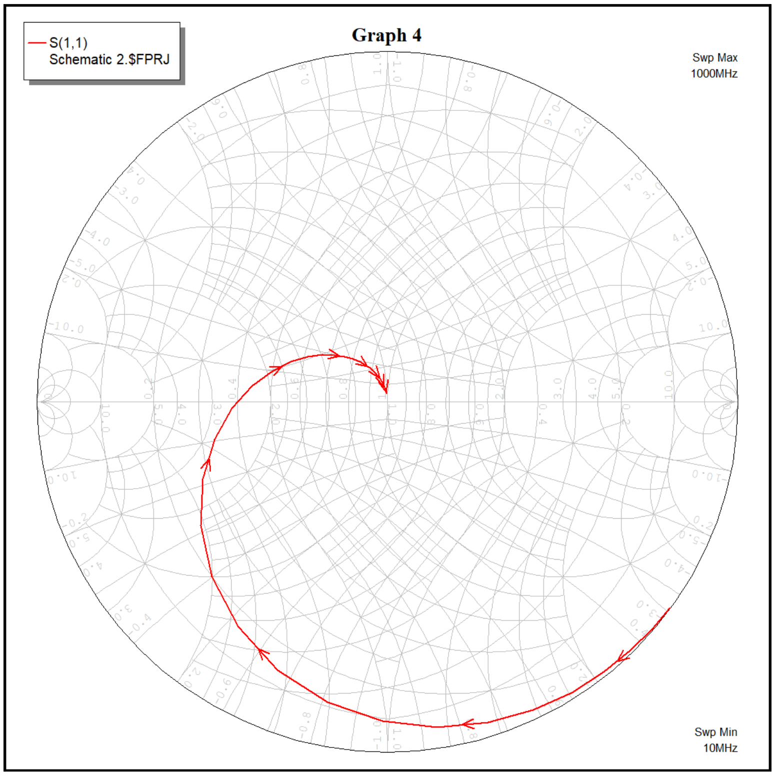


Figure 11: Topology D Smith Chart



Circuit #8 LC - *Huy*

After calibrating the NanoVNA using the RF demokit, I attached the SMA connector to CH0 and the other end to the RF demokit and swept from 10MHz to 1GHz and got the smith chart shown in Figure 12. Afterwards I was able to identify the topology of this was topology A and was able to recreate the smith chart in AWRD shown in Figure 13 using the schematic shown in Figure 14. Since the NanoVNA results showed that the smith chart was around the edges it means that the circuit must be purely imaginary so no resistors are included. The reason why the NanoVNA is not completely imaginary is because of the little resistance in the SMA connecter since they are not perfect. After some trial and error I was able to find the values of the circuit to get my smith chart to closely match the NanoVNA result.

Figure 12: NanoVNA Results

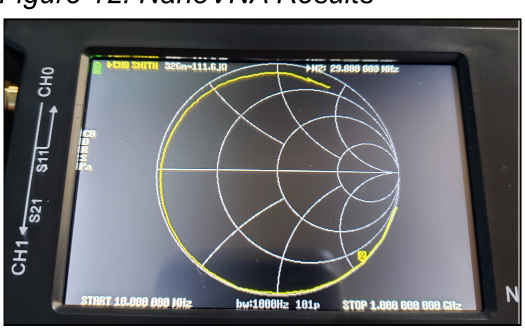


Figure 13: Topology A Smith Chart

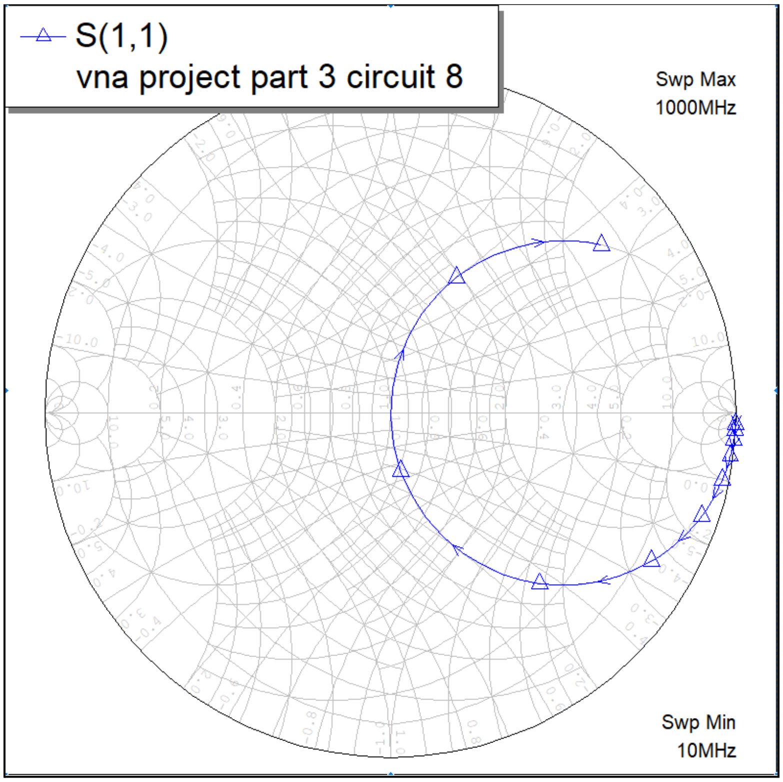
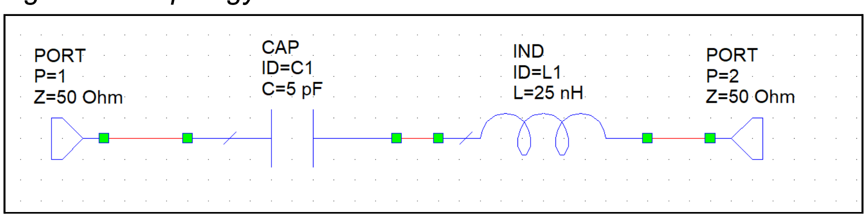


Figure 14: Topology A Schematic



Problem 4

Antenna Project

4A. Touchstone File Plots

After downloading the provided *Antenna_2450.s1p* file for the antenna, we plotted $|S_{11}|$, $<S_{11}$, and S_{11} on a smith chart. However, we noticed that the provided frequency range in the *.s1p* file (2 - 3 GHz) was completely different from the frequency range requested in the problem statement (0.1 - 1.5 GHz). Since the smith chart could only be plotted in the former of these ranges, Figures 15-16 show $|S_{11}|$ and $<S_{11}$ in the 0.1 - 1.5 GHz range respectively and Figures 17-19 show $|S_{11}|$, $<S_{11}$, and S_{11} on a smith chart in the 2 - 3 GHz range.

Figure 15: $|S_{11}|$ 0.1 - 1.5 GHz

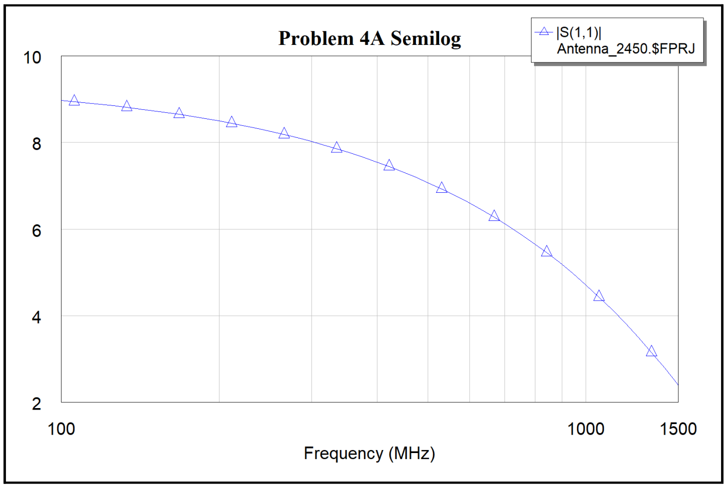


Figure 16: $<S_{11}$ 0.1 - 1.5 GHz

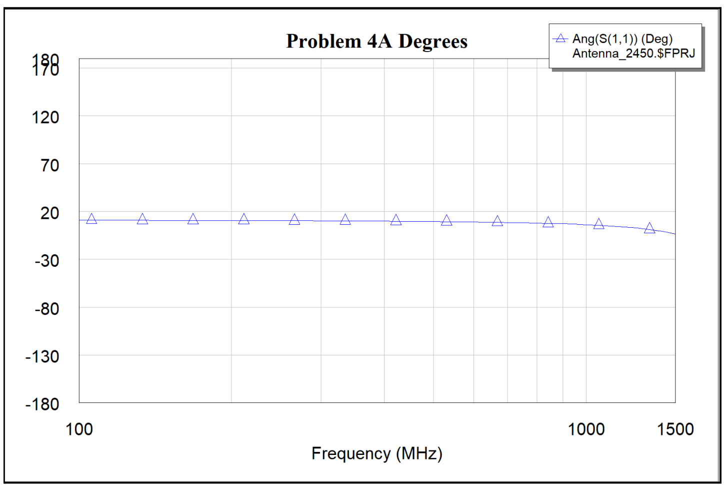


Figure 17: $|S_{11}|$ 2 - 3 GHz

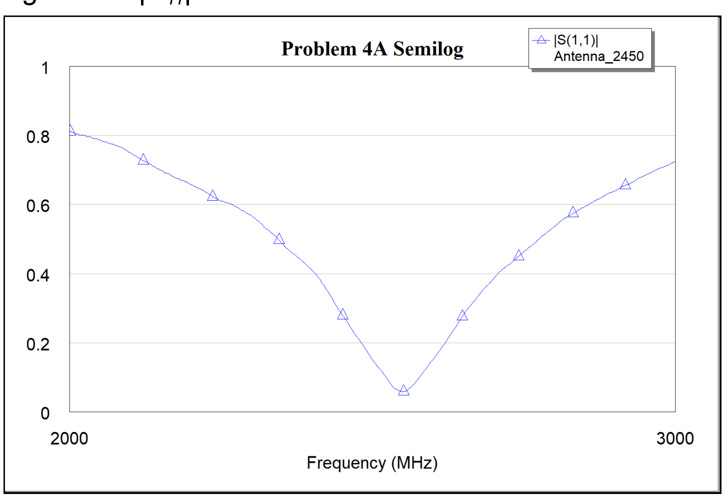


Figure 18: <S_{11} 2 - 3 GHz

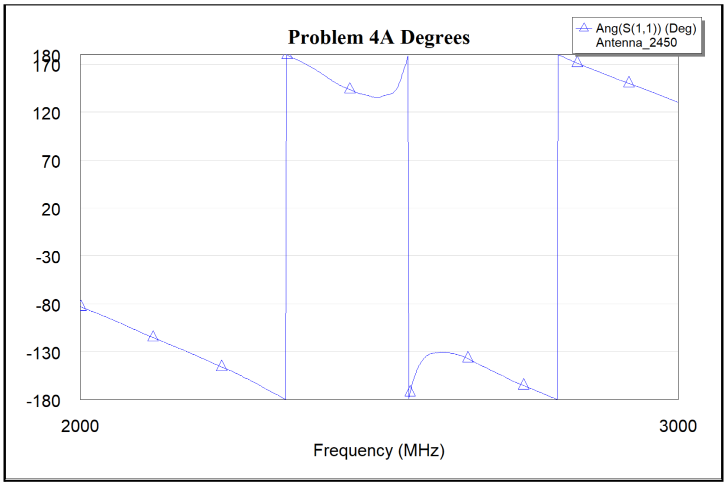
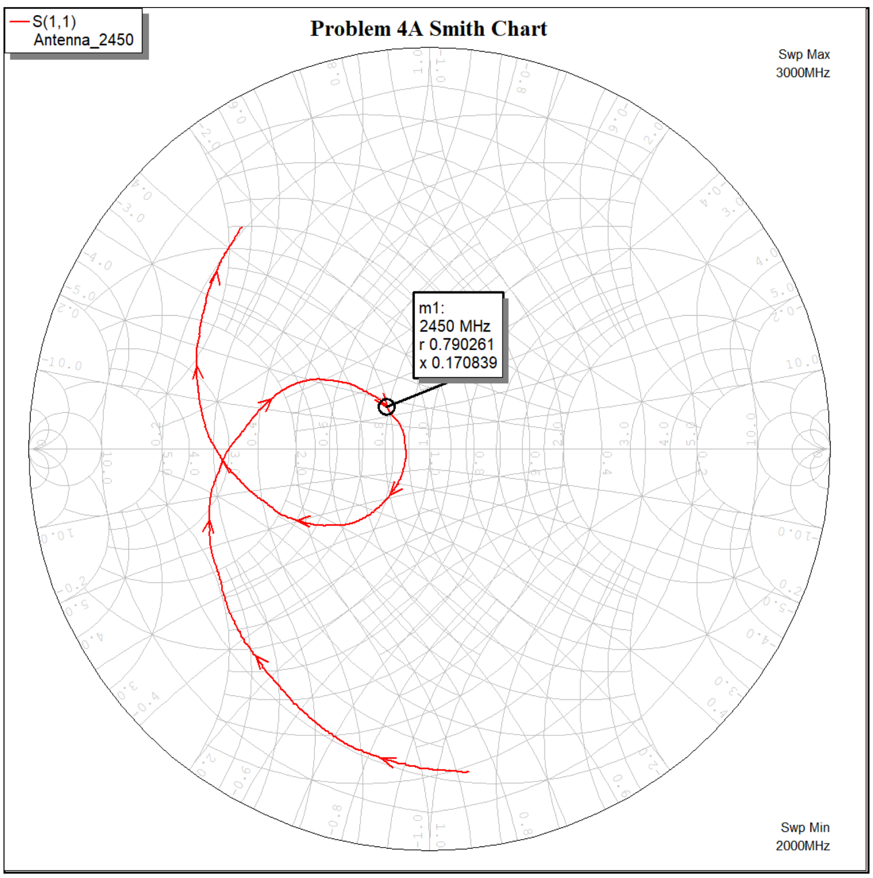


Figure 19: |S_{11}| on a Smith Chart



4B. Antenna Circuit Model

We started this problem by looking to curve fit the antenna smith chart response with a parallel RL circuit. Since the curve at 2.45 GHz most fit to a g_L circle, this circuit served both as a precursor to the eventual RLC circuit we would need to create and as a proof of concept to curve-fitting this response. Using the impedance value denoted by marker m1 in *Figure 19*, we were able to use some simple impedance and admittance calculations to determine the component values for L and R. These calculations can be found in the appendix section of this report. After creating the schematic (*Figure 20*) and simulating, we obtained the smith chart response in *Figure 21* including marker m1 which gives approximately the same impedance value as the antenna data. All component values in the following sections can be found in each circuit's schematic (*Figure 20, 22, 24*).

Figure 20: RL Circuit Schematic

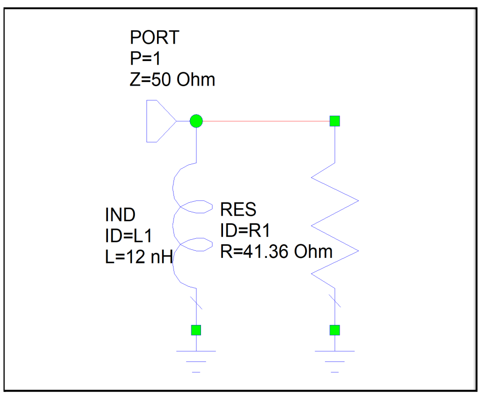
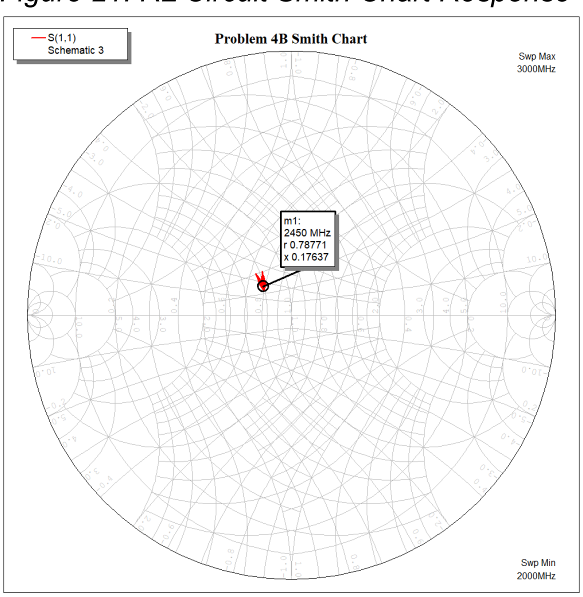


Figure 21: RL Circuit Smith Chart Response



Using the RL circuit as a proof of concept, we began creating an RLC circuit to have the same response as the RL by minimizing the effect of the capacitor. We did this by choosing a large parallel capacitor such that the smith chart response would travel from the center of the smith chart to the left edge via a g_L circle. From here, we added a series resistor to travel to the correct g_L circle that the antenna impedance resided on and added a small inductor to travel up that g_L circle to the correct susceptance value. Putting this circuit together in reverse order, we get the schematic in *Figure 22* and the subsequent smith chart response in *Figure 23*. Marker m1 on *Figure 23* also gives approximately the same impedance value as the RL Circuit and antenna data.

Figure 22: RLC Circuit Schematic

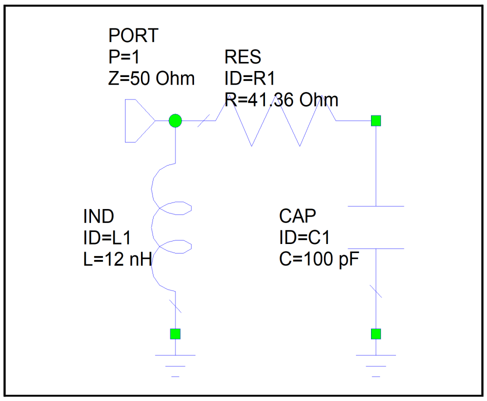
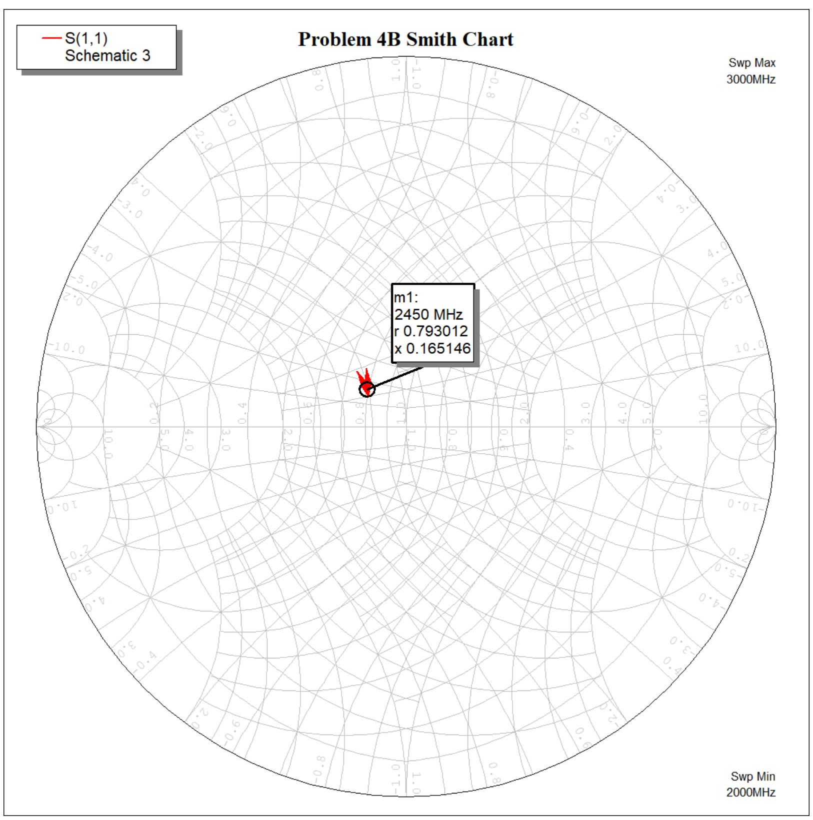


Figure 23: RLC Circuit Smith Chart Response



Using similar component values, we calculated an added parallel inductance of 587.57 nH was necessary to travel down the g_L circle to the closest pure real impedance value. *Figure 24 and 25* show the schematic of this circuit after adding the parallel inductor and its smith chart response from 0.1 to 1.5 GHz respectively. Marker m1 on *Figure 25* shows that the response at 850 GHz is very close to pure real.

Figure 24: RLC Pure Real Resistance Circuit Schematic

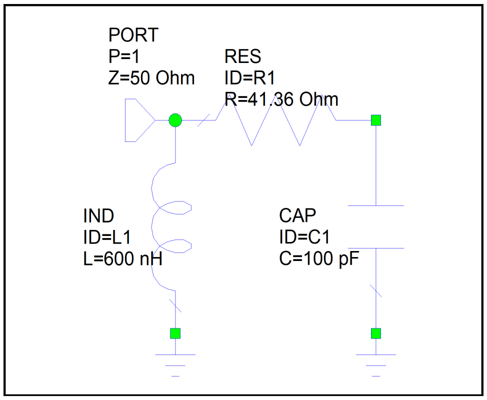
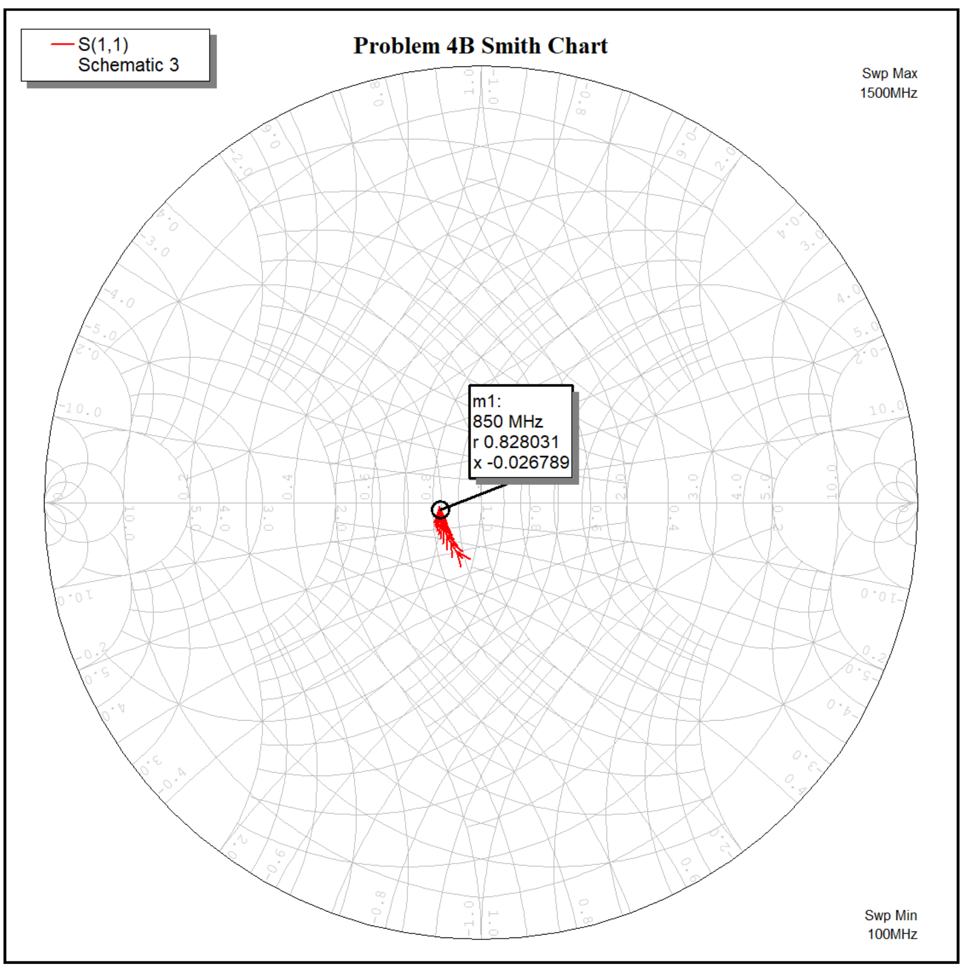


Figure 25: RLC Pure Real Resistance Smith Chart Response



4C. Matching Circuit Design

We designed a band-pass L network to impedance match the antenna circuit from *Figure 24* at a frequency of 2.45 GHz by first choosing a low pass series-inductor/parallel-capacitor matching circuit. This circuit was chosen because our parallel resistor had a greater resistance than our series resistor and because we wanted to travel along the upper-half of the smith chart. Using Q-Matching equations, we chose Q based upon these two resistor values and settled on L and C values given in the schematic shown in *Figure 26*.

Then, using the listed capacitors and inductors available in the lab, we chose L and C values that were closest to our calculated values which are shown in *Figure 27*. *Figures 28 and 29* show the smith chart responses for these circuits. In the first these smith charts, two markers at 850 MHz and 2.45 GHz show that the network is matched at 2.45 GHz while also having a pure real impedance value at 850 MHz. *Figures 30 and 31* show Semilog plots of $|S_{11}|$, the former plot proving that the matching circuit is indeed a band-pass circuit. Although the lab component values are only slightly off from the original values, the responses show that it is enough to completely unmatch the circuit.

Figure 26: Matching Network Schematic

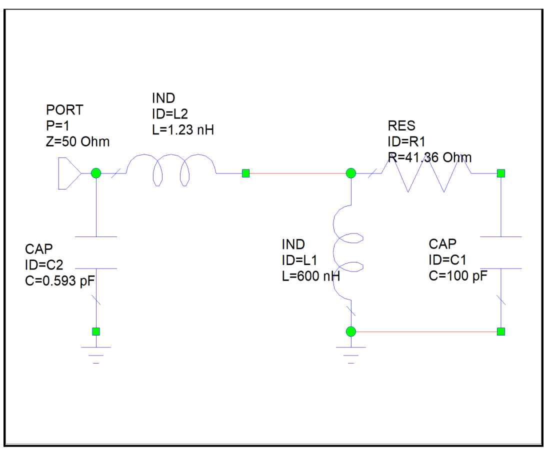


Figure 27: Matching Network with Lab Components Schematic

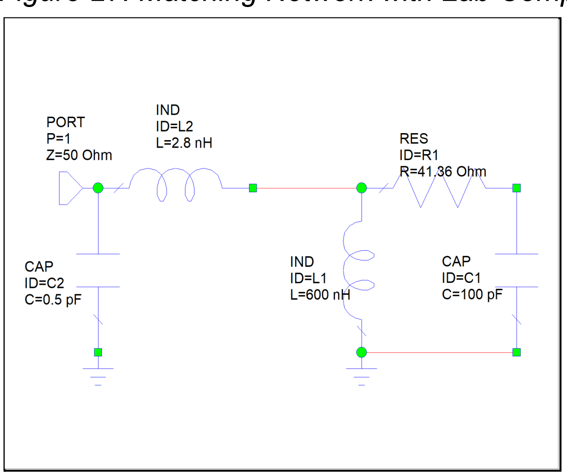


Figure 28: Matching Network Smith Chart Response

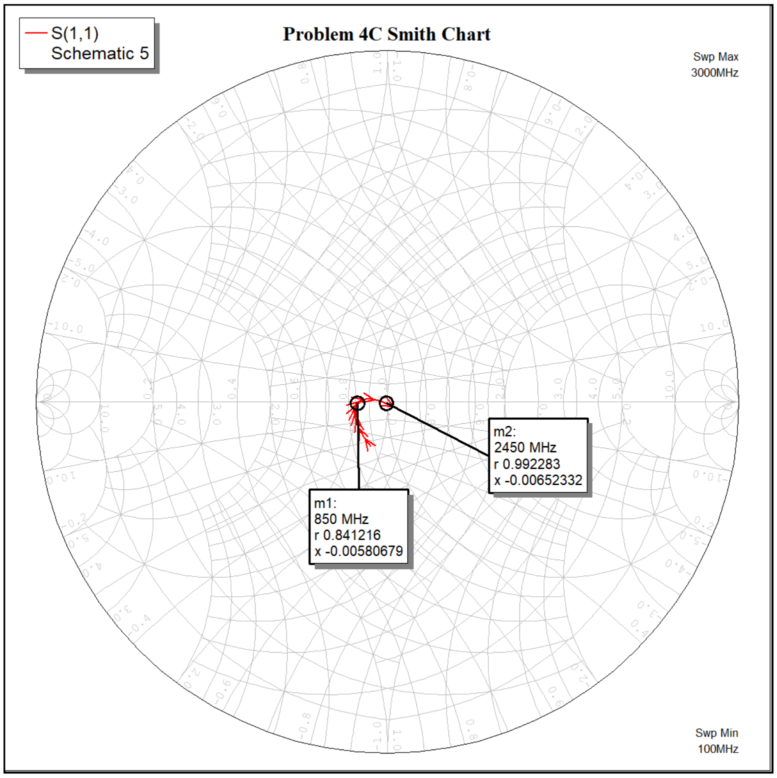


Figure 29: Matching Network with Lab Components Smith Chart Response

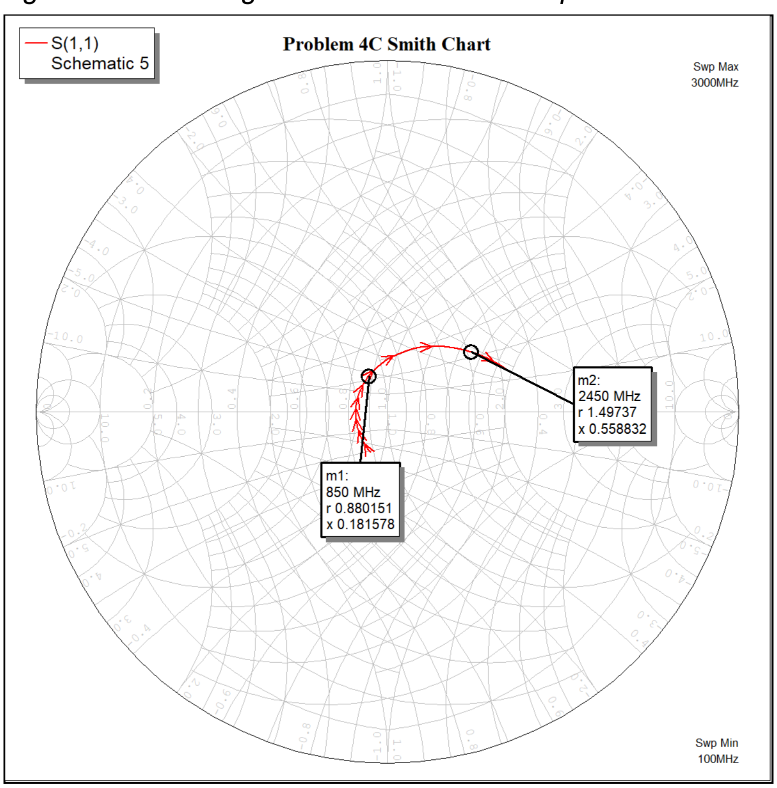


Figure 30: Matching Network $|S_{11}|$ Plot

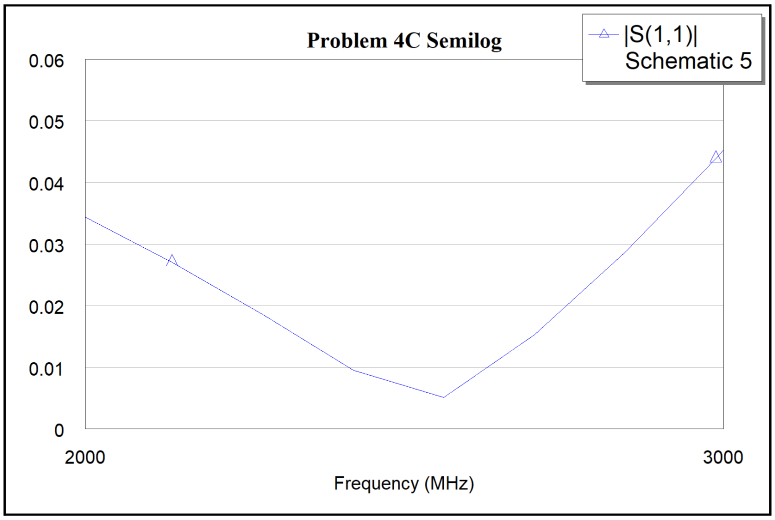
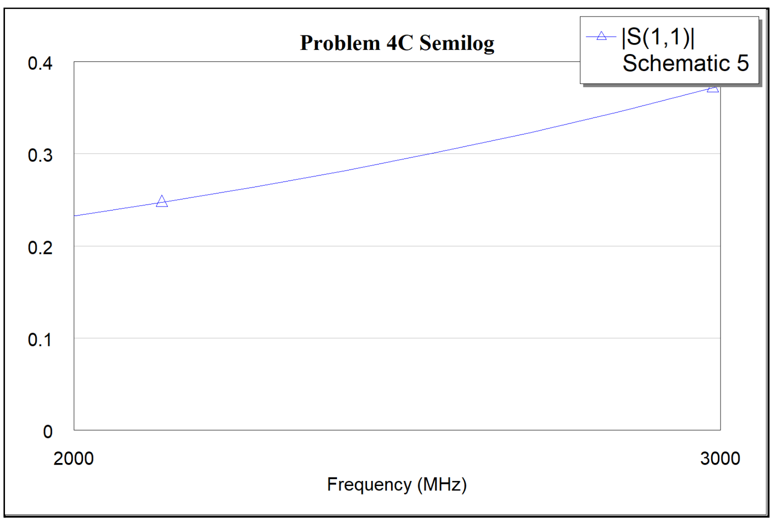


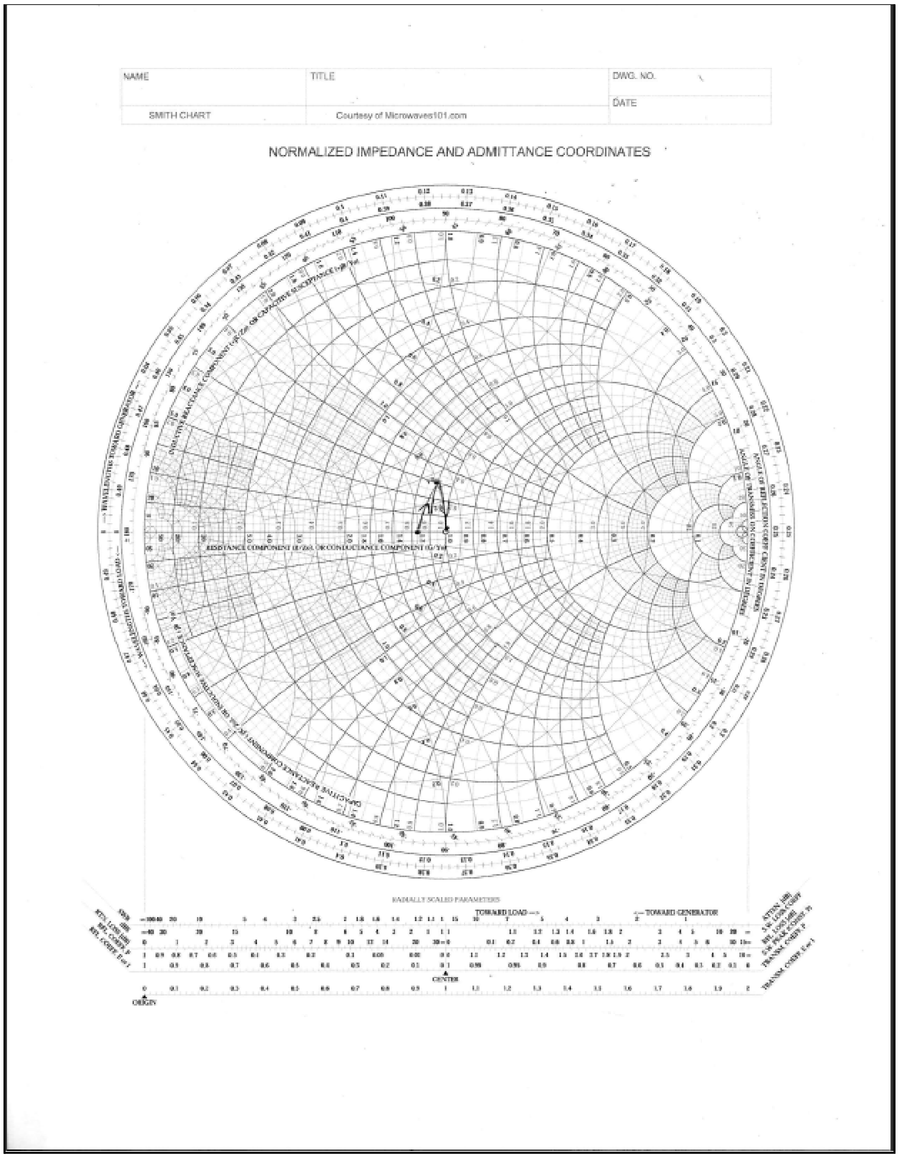
Figure 31: Matching Network with Lab Components $|S_{11}|$ Plot



4D. Smith Chart Matching Plot

Using the circuit model from *Figure 26* left of the antenna circuit, we drew the response of the series inductor and parallel capacitor as they each travel toward the center of the smith chart. Following the calculations in Appendix D, we move along a constant reactance circle from the series inductor and along a constant conductance circle from the parallel capacitor. We then end up nearly in the exact center of the chart, matching our antenna circuit (*Figure 32*).

Figure 32: S11 matching from LC port to antenna resistance



4E. Matching Circuit Plots

We now can simulate the circuit shown in *Figure 26*. After plotting the S_{11} smith chart we get an impedance of 8.841-j 0.0058 shown in *Figure 33*. Plotting the S_{11} semilog we get a magnitude of 0.0863 at 850MHz shown in *Figure 34*. Finally plotting the S_{11} from -180 to 180 degrees, we can see from *Figure 35* that there is a phase of -177.7 degrees. To find the dB difference between our matching network and antenna from **4A** we will compare the magnitude from our matching network circuit and our antenna circuit to find how much more power our matching circuit is outputting. We did the calculation in Appendix problem **4E**. With our RLC matching circuit the dB output went up a total of .8523 dB. Not a huge amount of change in dB output.

Figure 33: S11 Matching Network Smith Chart

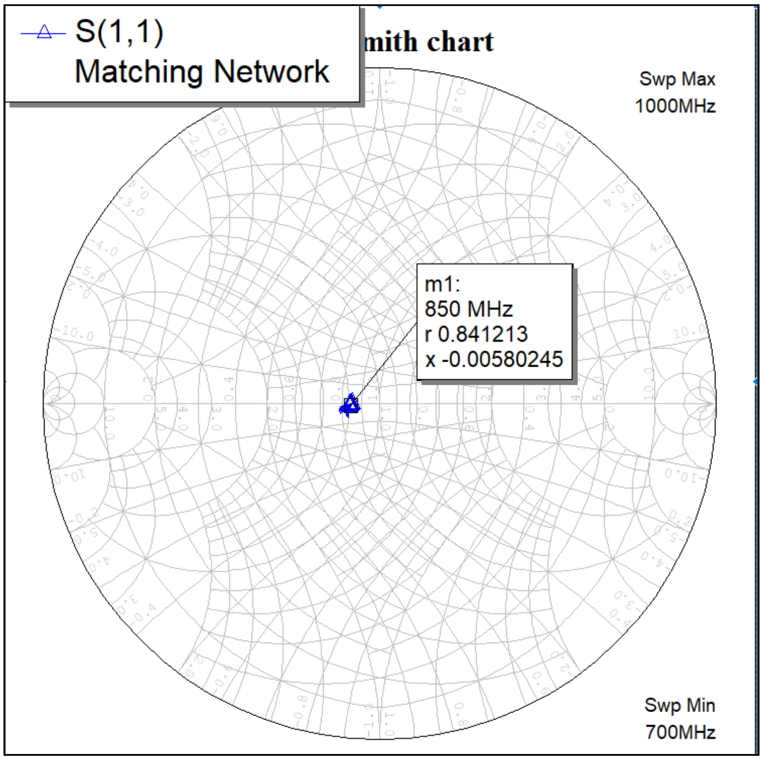


Figure 34: S11 Matching Network Semilog plot

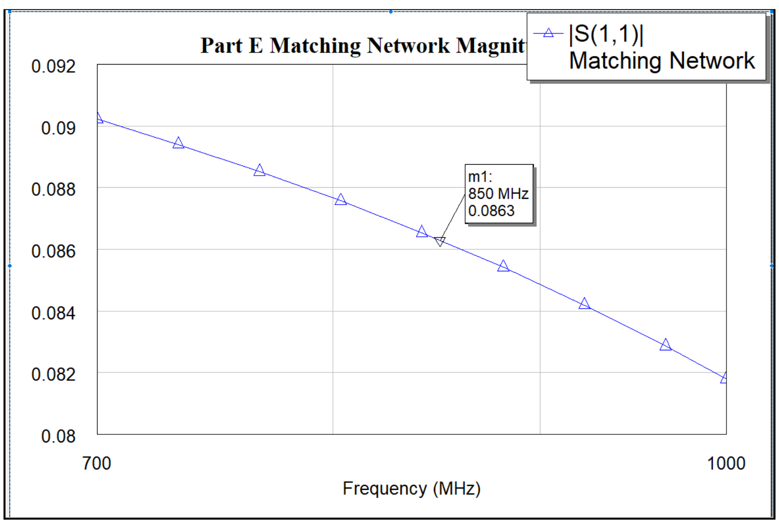
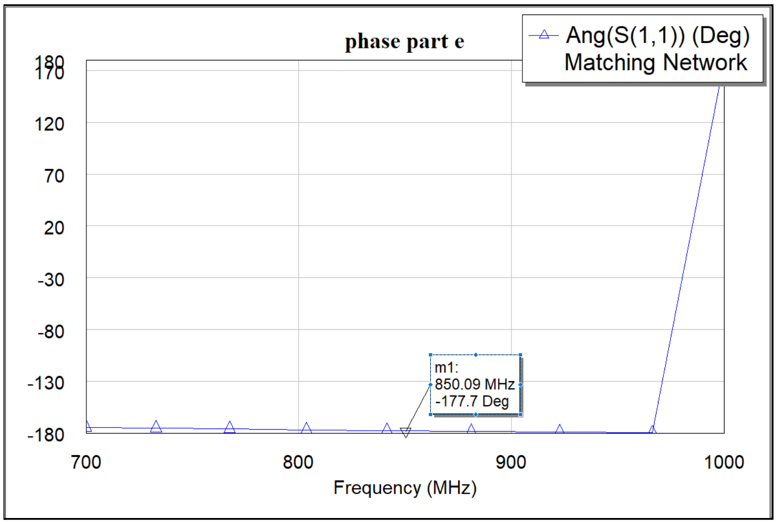


Figure 35: S11 Matching Network degrees plot From 180 to -180



Appendix

Written Work for Problems

Problem 4B

RL Circuit:

Problem 4B

$m1 \Rightarrow (0.790261 + 0.170839j)\, 50\Omega$

$$Y_{m1} = \frac{1}{(0.790261 + 0.170839j)50} = 0.0241779 - 0.005227402j\, S = \frac{1}{R} - \frac{j}{\omega L}$$

$$\therefore \quad R = \frac{1}{0.0241779\ S} \Rightarrow \boxed{R = 41.36\ \Omega}$$

$$\therefore \quad L = \frac{1}{(2\pi)(2.45E9)(0.005227402)} \Rightarrow \boxed{L = 12\,nH}$$

RLC Pure Real Resistance Circuit:

No.

Date.

$f = 850\,MHz$

$$Y_{RL} = \frac{41.293}{41.293^2 + (2\pi \cdot 850\times10^6 \cdot 100\times10^{-12})^2} + j\frac{2\pi \cdot 850\times10^6 \cdot 100\times10^{-12}}{41.293^2 + 2\pi \cdot 850\times10^6 \cdot 100\times10^{-12}}$$

$= 0.242 + j\,0.000313$

$$Y_{LL} = -j\frac{1}{2\pi \cdot 850\times10^6 \cdot (L_2 \cdot 10.64\,nH}$$

$Y_{LL} = Y_{RC}$

$$\frac{1}{2\pi \cdot 850\times10^6 \cdot L_2 \cdot 10.64\,nH} = 0.000313 \rightarrow L_2 = \frac{1}{2\pi \cdot 850 \cdot 10^6 \cdot .000313} - 10.64\,nH$$

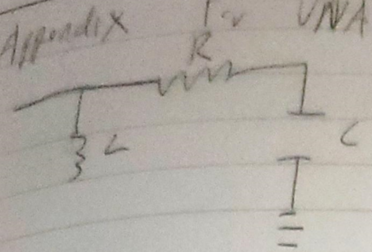
$L_2 = 587.57\,nH$

RLC Circuit:

No.

Date.

Appendix for VNA project



$Z_{ant} = 0.79 + j\,.171$ $\quad f_0 = 2.45\ \text{GHz}$

$Z_{ant} = 0.79 + j\,.171 \cdot 50 = 39.5 + j\,8.55$

$$Z_{rc} = R - \frac{j}{\omega C} = Y_{rc} = \frac{R}{R^2 + \omega c^2} + \frac{j\omega C}{R^2 + \omega c^2} \qquad Y = \frac{-j}{\omega L}$$

$$Y_{in} = Y_{rc} + Y_L = \frac{R}{R^2 + \omega c^2} + j\left(\frac{\omega c}{R^2 + \omega c^2} - \frac{1}{\omega L}\right)$$

$$Y_{ant} = \frac{39.5}{39.5^2 + 8.55^2} - j\,\frac{8.55}{39.5^2 + 8.55^2} = 0.024218 - j\,.00523$$

$C = 100\,pF$, $Re\{Y_0\} = Re\{Y_{ant}\}$

$$\frac{R}{R^2 + (2\pi \cdot 2.45 \cdot 10^9 \cdot 100\times10^{-12})^2} = 0.024 \rightarrow \frac{R}{R^2 + 2.369} = 0.0242$$

$$R = 0.0242 \cdot (R^2 + 2.369) \rightarrow R = .0242R^2 + .0573 \rightarrow$$

$$-.0242R^2 + R - .0573 = \frac{-1 \pm \sqrt{(1)^2 - 4(-.0242)(-.0573)}}{2(-.0242)} \rightarrow$$

$$\frac{-1 \pm .997}{-.0483} \neq \frac{-1 + .997}{-.0483} = -.057\Omega = R \text{ too small}$$

$$\frac{-1 - .997}{-.0483} = 41.293\Omega$$

$$\frac{2\pi \cdot 2.45 \cdot 10^9 \cdot 100^{-12}}{41.293^2 + (2\pi \cdot 2.45\times10^9 \cdot 100\times10^{-12})} - \frac{1}{2\pi \cdot 2.45\times10^9 \cdot L} = -j\,0.0052$$

$$= 9.019\times10^{-4} - \frac{1}{2\pi \cdot 2.45\times10^9 \cdot L} = -0.0052 = -$$

$$\frac{-1}{2\pi \cdot 2.45\times10^9 \cdot L} = -.00610 \rightarrow L = \frac{1}{2\pi \cdot 2.45\times10^9 \cdot .00610}$$

$L = 10.64\,nH$

Problem 4C

Circuit Design:

Problem 4C

$$Q = \sqrt{\frac{R_{large}}{R_{small}} - 1} = \sqrt{\frac{50}{41.36} - 1} \Rightarrow \underline{Q = 0.4571}$$

$$L_{nH} = \frac{0.159\, Q_s\, R_{small}}{f_{GHz}} = \frac{(0.159)(0.4571)(41.36)}{2.45} \Rightarrow \boxed{L = 1.23\,nH}$$

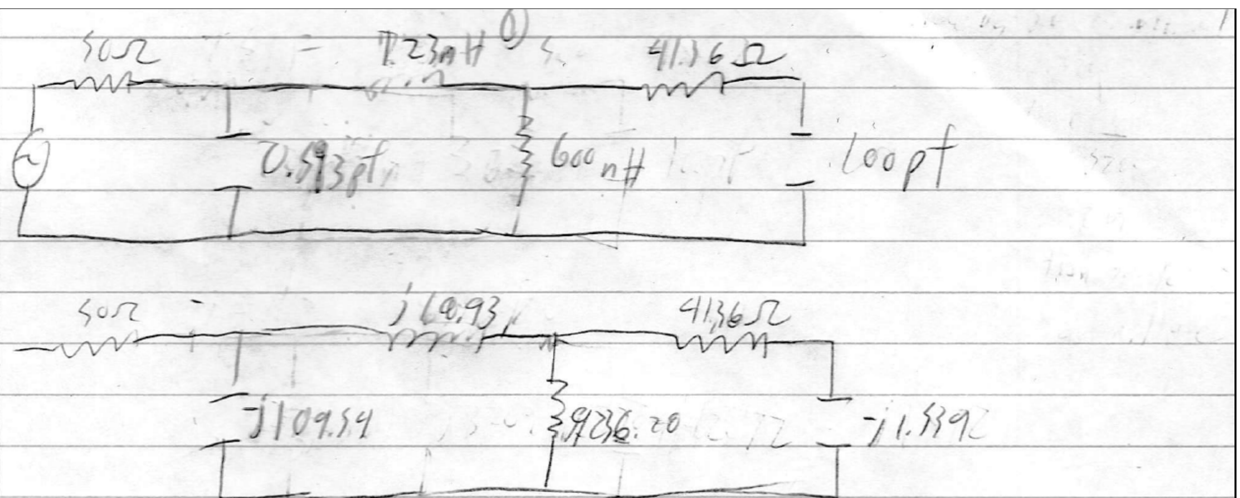
$$C_{pF} = \frac{159\, Q_p}{f_{GHz}\, R_{large}} = \frac{(159)(0.4571)}{(2.45)(50)} \Rightarrow \boxed{C = 0.593\ pF}$$

Using Lab capacitors & Inductors...

$$\boxed{L_{lab} = 2.8\,nH \quad C_{lab} = 0.5\,pF}$$

Problem 4D

Matching Circuit:



$\frac{41.36}{50} = .8272$ $j\omega L = 1.23nH \cdot 2\pi \cdot 2.45GHz = j18.93$

$j\frac{18.93}{50} = j.3786 \rightarrow .8272 + j.3786$

$0.593pF \cdot 2\pi \cdot 2.45GHz = -j109.54 \div 50\Omega = -j2.1909$

$y = .8272 + j.3786 - j2.1909 = .8272 - j1.8122$

Problem 4E

Power Calculation

$-20\log(0.095198) = 20.427\,dB$ nonmatching circuit
$-20\log(0.08637) = 21.279\,dB$ matching circuit
$21.279 - 20.47 = \boxed{.8523\,dB}$