	PC->Addr 11	IR[8:6]->A1 11	IR[11:9]->A3 11	T3->D3 111	T3->DPC 11	PC->ALU 11	T2->ALU 111
	T3 ->Addr 10	IR[11:9] ->A1 10	PE->A3 10	SE9 ->D3 110	T1->DPC 10	T1->ALU 10	SE_9->ALU 110
		PE ->A1 01		T5->D3 101	T5->DPC 01	T3->ALU 01	SE6->ALU 101
				T4->D3 100			1->ALU 100
	Mem Addr	**A1**	**A3**	**D3**	**DPC**	**ALU_IN_0**	**ALU_IN_1**
State	**MUX_1_Sel**	**MUX_2_Sel**	**MUX_3_Sel**	**MUX_4_Sel**	**MUX_5_Sel**	**MUX_6_Sel**	**MUX_7_Sel**
S_init	11	11				11	100
S_reg_read							
S_alu_op						10	111
S_reg_write			11	111			
S_right_pad_reg_write			11	110			
S_mem_read	10						
S_reg_write_2			11	101			
S_reg_write_from_T4			11	100			
S_reg_write_from_PE			10	100			
S_reg_read_1		10					
S_alu_op_imm6						10	101
S_mem_write	10					11	101
S_T3_to_PC					11		
S_alu_pad_6						11	101
S_write_PC					10		
S_PC_loop							
S_T3_inc						_01	100
S_alu_pad_9						11	110
S_reg_read_write		10					
S_reg_read_from_PE		_01					
S_update_PC					_01		