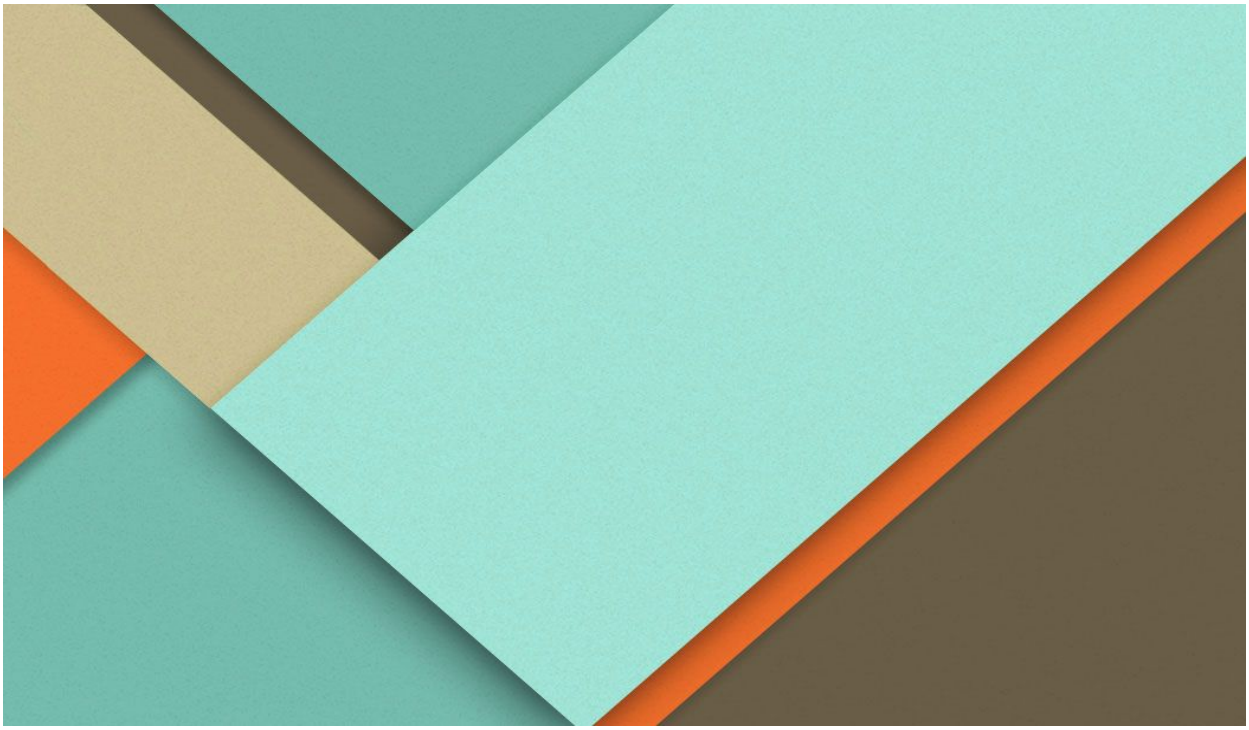

EE 677 COURSE PROJECT

LUT MAPPING

2016
MID-REVIEW REPORT

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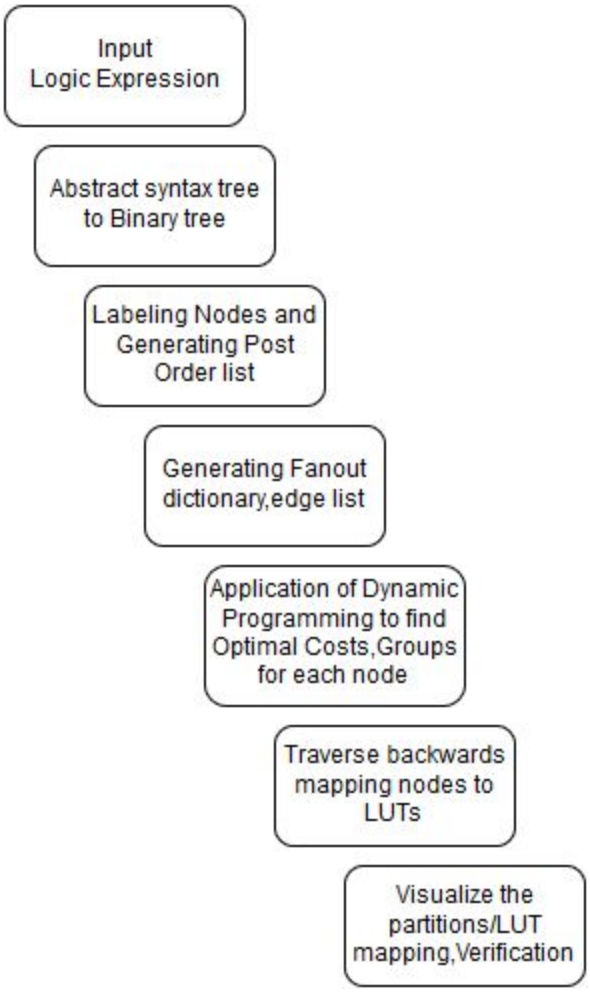
OBJECTIVE:

To transform a given logic circuit into its equivalent realization using several 6-LUTs

FLOW CHART:



INPUT/OUTPUT SPECIFICATIONS:

Input:

Logic expression(Representation of logic circuit) to implemented using 6-LUTs with following constraints:

1.Accepted literals in expressions ‘a’, ‘b’, … ‘z’ , ‘A’, … ‘Z’ (not ‘a’ denoted as ‘~a’ …)

2.Supported operators ‘and’ , ‘or’ , ‘xor’ , ‘not’

3.Not operator should be at the leaf nodes

Output:

1.Mappings of binary gates to 6-LUTs --(developed)

2.Graphical visualization of obtained partitions of the network (in png format) --(developed)

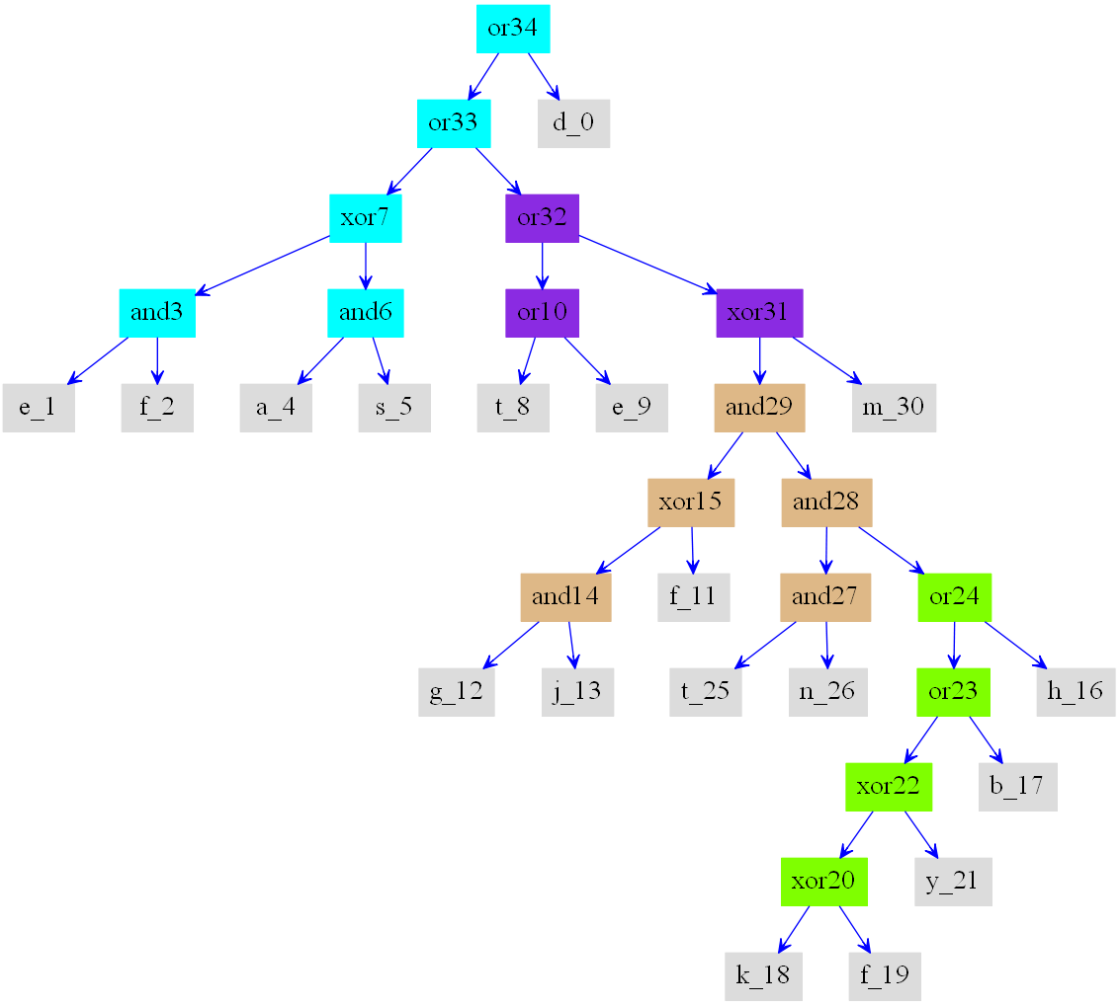
3.Bits to be filled in the 6-LUTs --(developed)

4.Verification of Logical Equivalence of final LUT network --(under progress)

RESULTS: (Test Cases)

1. Input Expression:

'd|(e&f)^(a&s)|(t|e)|(f^g&j)&(h|b|(k^f)^y)&(t&n)^m'



OUTPUT:

Total Cost : 4

LUT Mappings:

LUT1: ['or34', 'or33', 'xor7', 'and3', 'and6']

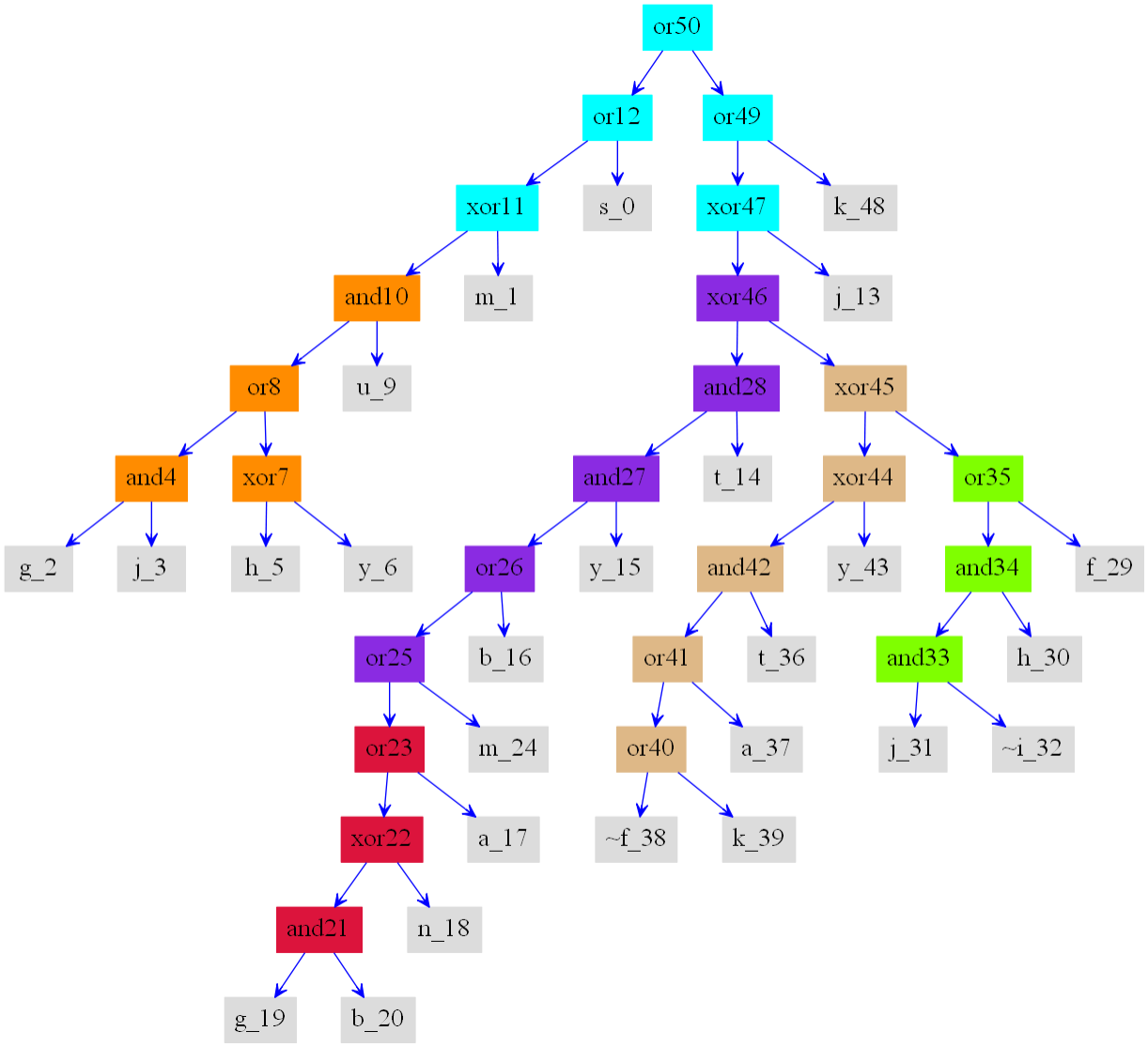
LUT2: ['or32', 'or10', 'xor31']

LUT3: ['and29', 'xor15', 'and28', 'and14', 'and27']

LUT4: ['or24', 'or23', 'xor22', 'xor20']

2. Input Expression:

'(s|m^(g&j|h^y)&u)|j^t&y&(b|(a|n^g&b)|m)^(f|h&j&~i)^t&(a|~f|k)^y|k'



OUTPUT:

Total Cost : 6

LUT Mappings :

LUT1: ['or50', 'or12', 'or49', 'xor11', 'xor47'] **LUT2: ['xor46', 'and28', 'and27', 'or26', 'or25']**

LUT3: ['xor45', 'xor44', 'and42', 'or41', 'or40'] **LUT4: ['or35', 'and34', 'and33']**

LUT5: ['or23', 'xor22', 'and21'] **LUT6: ['and10', 'or8', 'and4', 'xor7']**

REFERENCES:

1. Hactel & Somenzi :Logic Synthesis and Verification Algorithms

2. http://interactivepython.org/runestone/static/pythonds/index.html