CM65xxB USB Audio

Application Notes

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Release Note

Revision	Date	Description
0.10	2012/1/14	First release
0.20	2012/1/19	Update
0.91	2012/8/15	Modify EEPROM setup memo.
1.00	2012/1/08	Release
1.01	2013/2/7	Modify CM65XX -> CM65XXB
1.02	2013/05/27	Add Microphone Bias Voltage & GPIO control notice
1.03	2014/06/04	Modify EEPROM requirement.

1 About This Document

The Purpose of this document is to summarize the common application notes for customers who are designing their products with Cmedia CM65xxB USB audio Processor series or who are evaluating the solutions. It will contain the following contents about the typical system block diagram; schematics design notes, layout guide, applicable PC OS, and exception notes. It's recommended to read this document before you start to plan and design your products with CM65xxB USB Audio solution.

2 CM65xxB USB Audio Solutions Introduction

Cmedia's CM65xxB is a highly integrated USB audio single chip optimized for consumer headset solutions. CM65xxB supports standard HID compliant volume control pins and playback control pins. CM65xxB also offers playback operation and playback/record mute LED indicators in order to show the current status.

All necessary analog and digital modules are embedded in CM65xxB, including stereo DAC, headphone driver, stereo ADC, microphone pre-amp booster, PLL, regulator, and USB transceiver. Moreover, CM65xxB integrates 5-band hardware equalizer (EQ) with 4 default preset modes (Music/flat, Communication, Gaming, and Movie). The EQ preset gain parameters can also be customized for compensating the headphone SPL performance or to be complaint with TIA-920 standard.

In addition, embedded microphone Auto Gain-Control (AGC) function can adjust inputs that are out of the preset volume range to a proper volume. Also, the AGC avoids large signal clipping during voice communication. Optional clipping detection LED also gives users an alert when the excess volume input happens.

3 Typical System Block Diagram

The typical system design is as the following block diagram:

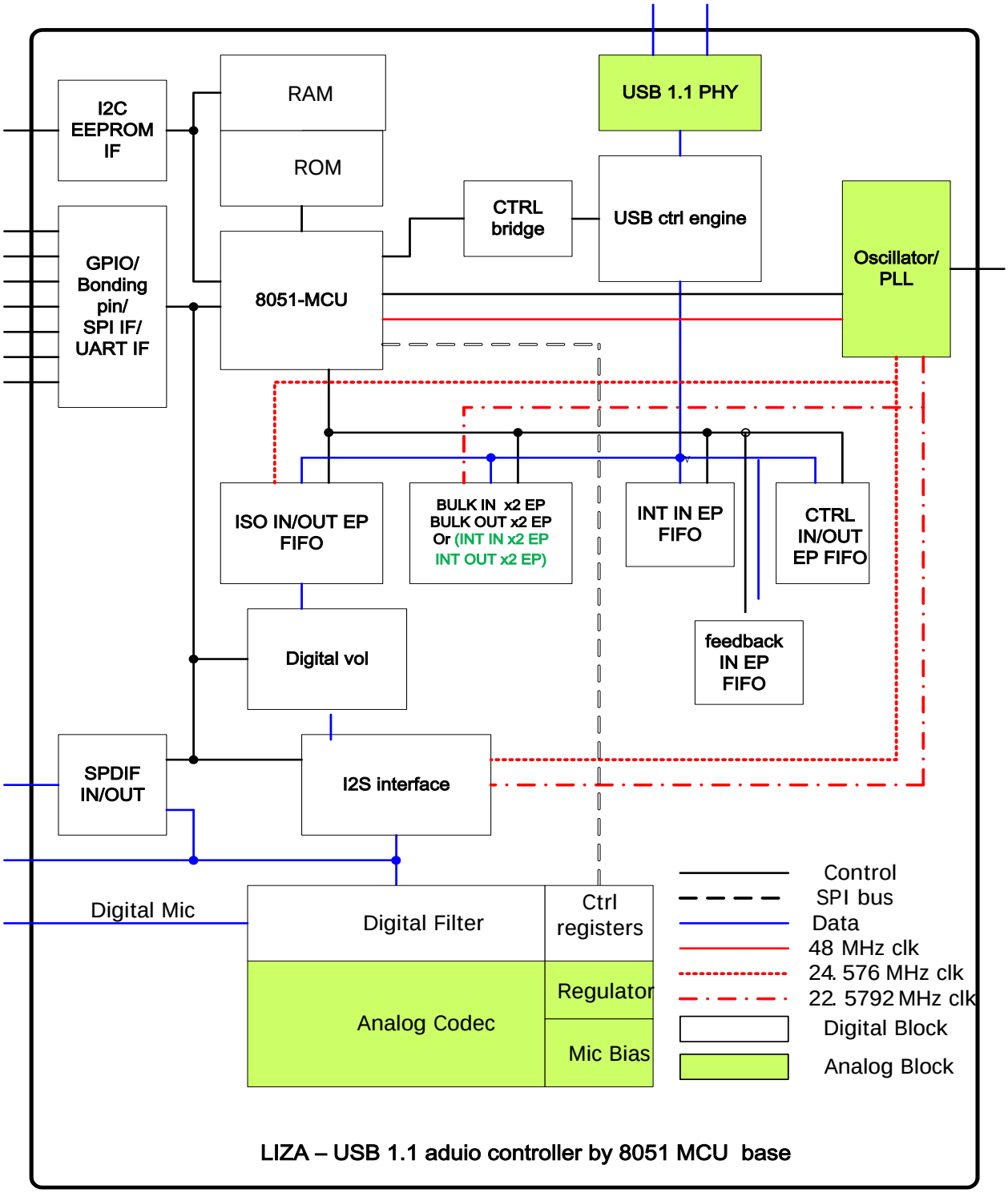
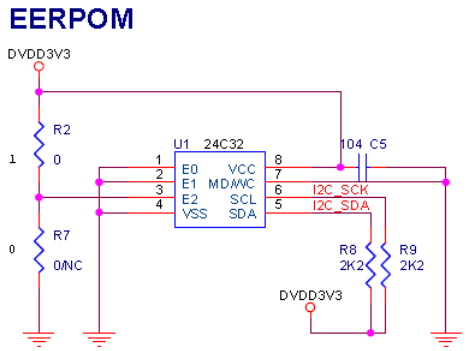


Figure1. Typical CM65xxB USB Audio Processor System Block Diagram

4 Schematics Design Notes

4.1 EEPROM

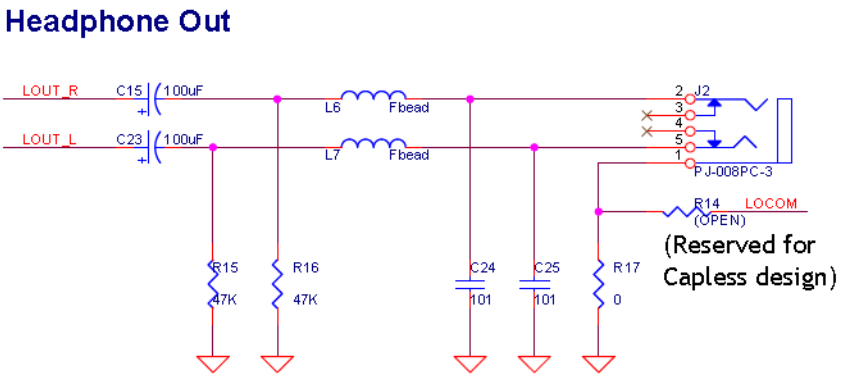


CM65xxB support serial EEPROM 24C02 ~ 24C512.
24C02 ~ 24C16 R7 = short, R2 = open

EEPROM Type	R7	R2
24C01/02/04/08/16	Short (Pull Low)	Open
24C32/64/128	Open	Short (Pull High)

- EEPROM must support A2(Address 2) Pin.
- The CM65xxB default I2C speed is 400KHz, and the customized firmware is loaded from external EEPROM. To load the firmware successfully, please select the EEPROM supports 400KHz.

4.2 Headphone Out for Cap-less Design

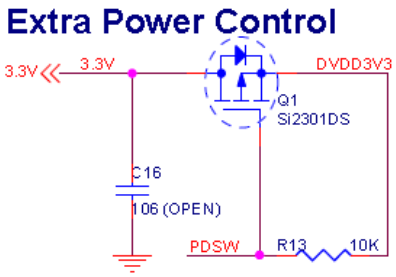


CM65xxB support Cap-less Output.
Line out used to cut off capacitor to separate DC. For frequency response and cost,

C15 and C23 can be removed (short-circuited) and use cap-less line out as the schematics above. When using cap-less mode, the crosstalk will be slightly worse can't pass DTM tests. LOCOM output DC same line out, then earphone receive same DC.

Output Type	R17	R14	C15	C23
Normal	Short	Open	100uF	100uF
Cap-less	Open	Short	Short	Short

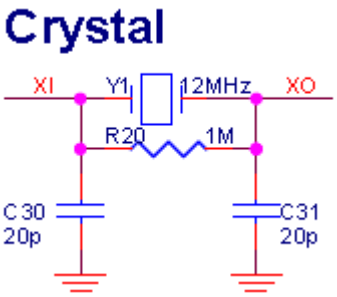
4.3 Power Control Design



PDSW pin support DC 1.8V ~ 5V

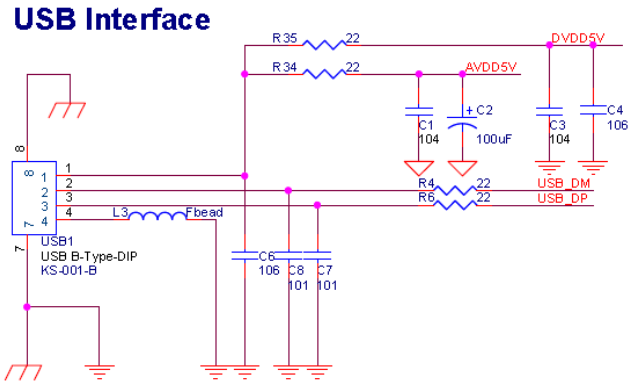
OS Mode	PDSW
Operation	Drive Low
Suspend	Open

4.4 Crystal Design



CM65xxB need a 12MHz Crystal

4.5 USB Interface Design

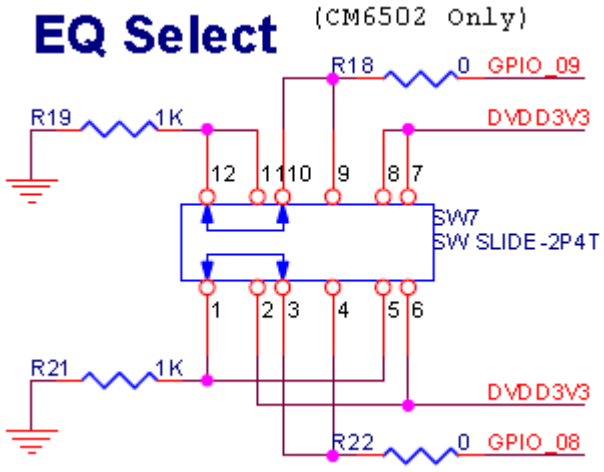


R34 & R35 for audio quality requierment.

R4 & R6 for USB phy impedance matching.

C7 & C8 for EMI solution.

4.6 USB Interface Design



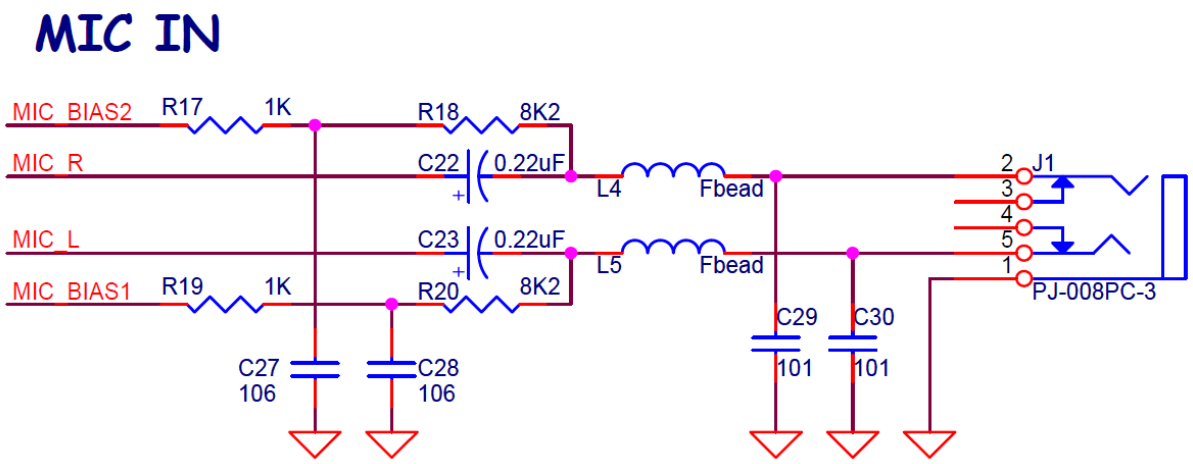
SW7 is a multi switch to set EQ0, EQ1 value.

00	Normal mode
01	Gaming mode
10	Communication mode
11	Movies mode

4.7 GPIO

CM65XXB GPIO 16 ~ 31 supply 2.4V
In use it could Pull Up 3.3V or 5V

4.8 Microphone Interface Design



in use CM65XXB Microphone Bias supply 1.75V
C22, C23 0.22uF could pass the WHQL & Lower pop noise(plug in).
R17, C27, R18 & R19, C28, R20 filter for Microphone Bias lower noise.

5 Layout Guide

This document provides guideline for the design of High integrated USB audio PCB. It's important to ensure maximum performance proper component placement and routing. This document includes properly isolated digital circuitry and analog circuitry. The effects of ground loop and supply plane geometry, decoupling/ bypassing/ filtering capacitors placement priorities, USB D+ and D- signals, analog power supplies, and analog ground planes.

5.1 General Rules

1. If it's necessary to turn 90°, it's better to use two 135° turn (keep angles >= 135°) or an arc, instead of making a single 90° turn. It can reduce reflection on the signal by minimizing impedance discontinuities.

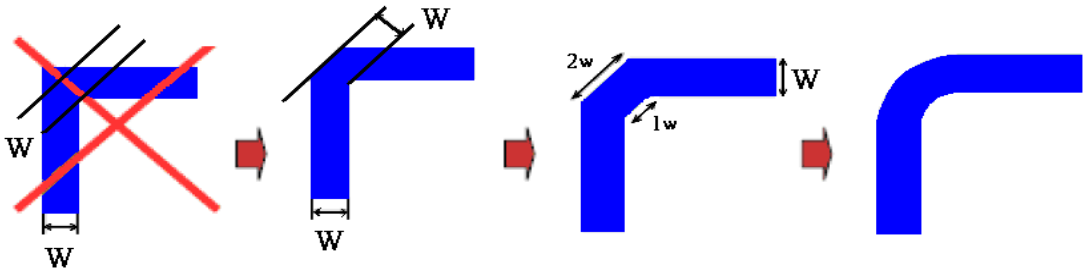


Figure4. Turn Angle

2. The old rules of splitting power and ground into "digital" and "analog" sections do necessarily apply to the many audio devices. AGND and APWR plane as the same region as possible, place DGND and DPWR plane on other region.

3. Use Ferrite Bead to connect different ground plane to avoid the EMI issue.

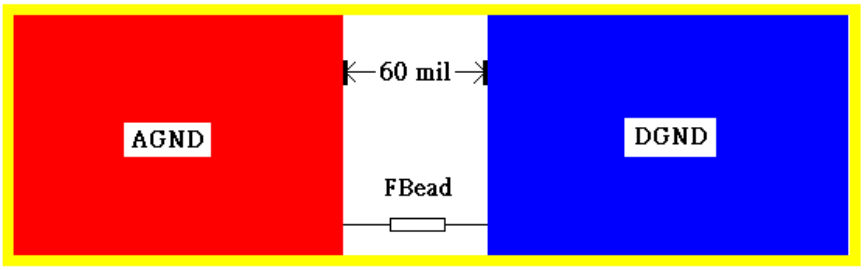


Figure5. AGND and DGND

4. Connect analog and digital power planes at one point through a low impedance bridge or preferably through a ferrite bead.

5. Place some filter capacitors on power supply trace near OP-Amplifier for cleaner power and audio signal to Noise Ratio.

6. If using capacitance 475、272、273 in OP-Amplifier circuitry, select Mylar or other material alike capacitors for better audio quality.

7. To achieve proper ESD/EMI performance; it's suggested to use a 0.1uF capacitor on each cable PWR bus line to chassis GND close to the connector pin. If voltage regulators are used, place a 0.1μF capacitor on both input and output. This is to increase the immunity to ESD and reduce EMI.

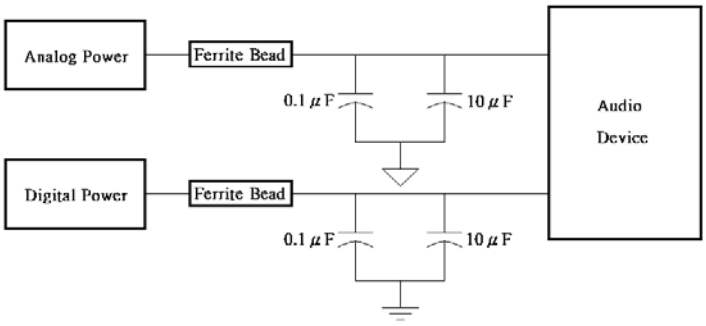


Figure6. Capacitors Array

8. Do not route traces so they cross from one plane to the other. This can cause a broken RF return path resulting in an EMI radiating loop. This is important for higher frequency or repetitive signals. Therefore, on a multi-layer board, it is best to run all clock signals on the signal plane above a solid ground plane.

5.2 Layout design of Ground and Supply Plane geometry

The layout separates the analog and digital ground planes with a 60 to 100 mils gap. The moat helps to isolate noisy digital circuitry from clean analog audio circuitry. The digital and analog ground planes are tied together by a wide link(about 50mils) at a point close to the USB connector. This will be the "drawbridge" that goes across the moat. Do not allow any digital or analog signal traces pass through the drawbridge. Otherwise, the digital noise may get into the analog signals and make audio performance worse.

In order to achieve the best audio performance and prevent crosstalk issue, C-Media recommend that the width of each I/O signal trace be at least 10 mils and the space be at least one time the size of the width of signal trace.

For a layout that helps to reduce noise, separating analog and digital ground planes is needed. The digital components should be placed over the digital ground plane, and the analog components (including the analog power regulators) should be placed over the analog ground plane. In addition to ground planes scheme, digital and analog power supply planes should be partitioned directly over their ground planes. Place analog power coincident with analog ground and digital power coincident with digital ground. If any portion of analog and digital plane overlaps, the distributed capacitance between the overlapping portions will couple digital noise into the analog circuitry. This defeats the purpose of isolating the power planes. The power and ground planes should be separated by approximately 40mils for the four layer PCB design. Using power and ground planes forming a natural, high capacitive, bypass capacitor to reduce overall PCB noise.

5.3 Decoupling and bypassing capacitors

Bypass capacitors on the PCB are used to short digital noise to ground. Commonly, USB audio controller may generate noise when its internal digital circuitry is operating. The current changes arise in the power and ground pins for the related section of the USB audio controller. The goal is to force AC current to flow in the shortest loop from the supply pin through the bypass cap and back into the USB audio controller through the nearby ground pin. A bypassing circuit is supposed to be a low lead inductance between the USB audio controller and the bypass capacitors when in the operating frequency of the USB audio controller. The long-trace will greater the inductance. To avoid long-trace inductance effects, use the shortest traces for bypass capacitors, with wide traces to

reduce impedance. For the best performance, use supply bypass leads of less than one-half inch.

The USB audio controller power supply pins are need the bypass caps, which are located as close as possible to the supply pins. The capacitors must have low inductance and low equivalent series resistance (ESR). Tantalum 10μF surface mount devices are good if they are used in conjunction with 0.1μF ceramics. The filter capacitors with "B" priority, the reference filter to stabilize the reference voltage for internal Ops and reference output filters should be placed close to USB audio controller. A good reference voltage is relative to good analog performance. These decoupling capacitors should be close to the USB audio controller pins (Audio input pin), or positioned for the shortest connections to pins, with wide traces to reduce impedance.

5.4 The USB connector

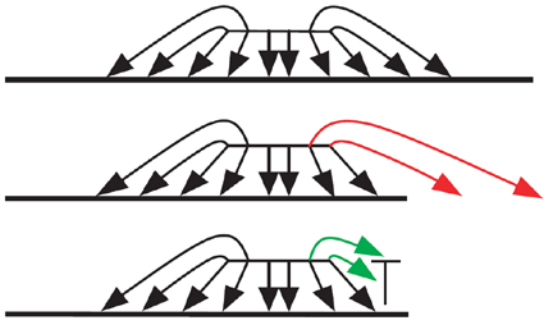
Place the USB device and connector on the un-routed board first. With minimum trace lengths, as equal as possible (D+, D-), route high-speed clock and USB differential signal pair first. Keep the distance between high-speed signals to USB differential signal pair far. Route the USB differential signal pair using a minimum of vias and corners. It can reduce signal reflection and impedance change. If it's necessary to turn 90°, it's better to use two 45° turn or an arc instead of making a single 90° turn. It can reduce reflection on the signal by minimizing impedance discontinuities.

Please don't route USB differential signal pair trace under crystal, oscillator, clock synthesizers, magnetic devices or ICs. It will cause interference. Stubs on USB differential signal pair should be avoided. While stubs exist, it will cause signal reflection and lower the quality. If a stub is unavoidable in the design, no stub should be bigger than 200mils.

5.6 Guard ring on PCB-edges

The mayor advantage of a multilayer PCB with ground-plane is the ground return path below each and every signal or power trace. As shown in Figure 10 the field lines of the signal return to PCB ground as long as an "infinite" ground is available. Traces near the PCB-edges do not have this "infinite" ground and therefore may radiate more than others. Thus signals (e. g. clocks) or power traces (e.g. core power) identified to be critical should not be routed in the vicinity of PCB-edges, or - if not avoidable – should be

accompanied by a guard ring on the PCB edge.



Fingure12. The field lines of the signal return to PCB ground

The intention of the guard ring is that HF-energy, that otherwise would have been emitted from the PCB-edge, is reflected back into the board where it partially will be absorbed. For this purpose ground traces on the borders of all layers (including power layer) should be applied as shown in Figure 10. As these traces should have the same (HF-) potential as the ground plane they must be connected to the ground plane at least every 10 mm.

Advantages of power planes

1. Easy and fast to implement
2. Low inductive power supply
3. Creates a capacity together with ground plane

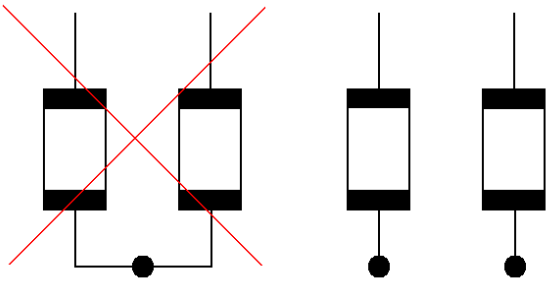
Advantages of routed power supplies

1. Allows the usage of one layer for more than one supply system, thereby reducing the cross -talk
   between these supplies
2. May reduce cross-talk within each supply system
3. Requires more careful power routing
4. Higher supply impedance may require extra capacity for supply stabilization.

5.7 Cross Talk

A VIA has a considerable impedance

As any trace also a VIA has a considerable impedance. Therefore, VIAs of critical circuits such as decoupling circuits must be exclusive for this circuit. The 2 parts of next Figure indicate how a shared VIA causes cross-talk between the involved circuits. The right most part shows the correct wiring.



Fingure13. Bad Screw hole to Cross Talk

5.8 ESD Protection System Design Consideration

The following are additional considerations for ESD protection in a system.

· Metallic shielding for both ESD and EMI

· Chassis GND isolation from the board GND

· Air gap designed on board to absorb ESD energy

· Clamping diodes to absorb ESD energy

· Capacitors to divert ESD energy

6 Preset EQ Modes

As mentioned above, the EQ engine provides 4 preset EQ modes for different user scenarios/applications. Customers can use EEPROM parameters to change the gain of each band of the 4-preset EQ curves according to their needs. Users can use the hardware switch on the product (determined by 2 EQ configuration input pins) to change different EQ mode:

1. Default/Music mode (EQ_SEL0=0, EQ_SEL1=0)
- Flat frequency response
- Keep high-fidelity original audio
- Suitable for music listening or normal usage

2. Gaming mode (EQ_SEL0=0, EQ_SEL1=1)
- Enhance deep and rich bass effects in games
- Experience more realistic bombing, firing and ambient sounds
- Fit best for PC game-play

3. Communication mode (EQ_SEL0=1, EQ_SEL1=0)
- Suppress low and high frequency noises
- Enhance your voice clarity in communication
- Optimized typically for TIA920/UC telephony standard
- Fit only for PC VOIP applications

4. Movies mode (EQ_SEL0=1, EQ_SEL1=1)
- Enhance the common audio bands in movies or musics
- Compensate the weakness of common headphone SPL/frequency characteristics
- Recommended for Movies mode if 4-modes are provided
- Recommended alternative for Default/Music mode (mode 1) for improving headphone driver's performance

Record path also support EQ function. Need firmware support.

—End of Data—

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