4.18 Internal registers

4.18.1 Internal Registers List

Address	Register Description
0x00	USB Global Control Register
0x01	USB Address Register
0x02	USB Global Interrupt Register
0x03	USB Global Interrupt Enable Register
0x04	USB Endpoint Number
0x05	USB Endpoint X Control Register
0x06	USB Endpoint X Status and Control Register
0x07	USB Endpoint FIFO Reset Register
0x08	USB Endpoint Interrupt Register
0x09	USB Endpoint Interrupt Enable Register
0x0a	USB Endpoint X FIFO Data Register
0x0b	USB Endpoint X Byte Count Register
0x0c	USB Frame Number Low Register
0x0d	USB Frame Number High Register
0x0e	COEDC Play_rate + Record_rate
0x0f	Resolution 24-bit Enable of play+ rec
0x10	Peripheral 1 Interrupt Register
0x11	Peripheral 1 Interrupt Enable Register
0x12	Peripheral 2 Interrupt Register
0x13	Peripheral 2 Interrupt Enable Register
0x14	ISO OUT FIFO Read Pointer Low Register
0x15	ISO OUT FIFO Read Pointer High Register
0x16	ISO OUT FIFO Write Pointer Low Register
0x17	ISO OUT FIFO Write Pointer High Register
0x18	ISO OUT FIFO Surplus Number Low Register
0x19	ISO OUT FIFO Surplus Number High Register
0x1a~0x1f	
0x20	Transfer FSM monitor
0x21	Transaction FSM monitor
0x22	MCU access FIFO mapping setting
0x23~0x27	
0x28~0x29	Playback write pointer enable and index
0x2a~0x2b	Playback read pointer enable and index
0x2c~0x2d	Record write pointer enable and index
0x2e~0x2f	Record read pointer enable and index
0x30~0x33	I2C slave data register
0x34~0x35	I2C slave Status register
0x36	I2C slave memory address pointer (MAP)
0x37	I2C slave status register
0x38	
0x39~0x3b	Ext SPI data register
0x3c	Ext SPI control reg0
0x3d	Ext SPI control reg1
0x3e	Ext SPI interrupt
0x3f	
0x40	EQ Band1's Gain Register
0x41	EQ Band2's Gain Register
0x42	EQ Band3's Gain Register
0x43	EQ Band4's Gain Register
0x44	EQ Band5's Gain Register
0x45	EQ Disable & EQ_TEST_MODE Register
0x46	Access which band of EQ filter coefficient
0x47	Filter coefficient port
0x48	EQ sample period
0x49	SoundSwitch setting from software

0x4a	EQ mode gain setting
0x4b~0x4d	Reserved for EQ OP gain
0x4e~0x4f	
0x50	PLL TESTMODE offset_p
0x51	PLL TESTMODE offset_r
0x52	PLL TESTMODE offset_rp
0x53	UART baud rate select
0x54	PLL TESTMODE mode_rp_48m setting
0x55	Software scale setting
0x56	PLL adaptive function enable
0x57	Ext I2S format + slave mode setting
0x58	PLL powerdown and dacfilter disable
0x59	External I2S signal pin and DSP process setting
0x5a	Record source + test setting
0x5b	Playback left channel volume control setting
0x5c	Playback right channel volume control setting
0x5d	Record left channel volume control setting
0x5e	Record right channel volume control setting
0x5f	VR scale read + AGC control path select
0x60	SPDIF Function Control Register(1)
0x61	SPDIF Function Control Register(2)
0x62	SPDIF/IN interrupt status
0x63	SPDIF/OUT channel status (1)
0x64	SPDIF/OUT channel status (2)
0x65	SPDIF/OUT channel status (3)
0x66	SPDIF/IN channel status (1)
0x67	SPDIF/IN channel status (2)
0x68	SPDIF/IN channel status (3)
0x69	SPDIF/IN channel status (4)
0x6a	UART RX Data Register
0x6b	UART TX Data Register
0x6c	Digital microphone setting
0x6d	OFFSET_P Monitor
0x6e	OFFSET_R Monitor
~~0x6f~~	~~OFFSET_E Monitor~~
0x70	EQ-ADC Band1's Gain Register
0x71	EQ-ADC Band2's Gain Register
0x72	EQ-ADC Band3's Gain Register
0x73	EQ-ADC Band4's Gain Register
0x74	EQ-ADC Band5's Gain Register
0x75	EQ-ADC Disable & EQ_TEST_MODE Register
0x76	EQ-ADC Access which band of EQ filter coefficient
0x77	EQ-ADC Filter coefficient port
0x78 ~0x7f	
0x80	(Master mode I^2C) Slave Device Address and Read/Write Control Register
0x81	I^2C Memory Address Pointer (MAP) of Slave Device
0x82	I^2C Memory Address Pointer (MAP2) of Slave Device
0x83 ~0x92	I^2C Data Register(master mode)
0x93	I^2C Control and Status Register 0
0x94	I^2C Control and Status Register 1
0x95	I^2C Download Control and Status
0x96	I^2C Clock Period change
0x97	
0x98~0x99	Internal SPI Data Register
0x9a	Internal SPI Control Register
0x9b~0x9f	
0xa0 ~ 0xa2	IR Logical One Make and Space
0xa3 ~ 0xa5	IR Logical Zero Make and Space
0xa6 ~ 0xa8	IR Header Code Make and Space

0xa9 ~ 0xab	IR Repeat Code Make and Space
0xac	IR_CTRL_0
0xad	IR_CTRL_1
0xae	IR_CTRL_2
0xaf ~ 0xb2	IR Receiver Data Buffer
0xb3	IR RC6 CTRL
0xb4	USB phy power+debug
0xb5	Clock Switch for MCU
0xb6	Module clock ctrl setting1
0xb7	Module clock ctrl setting2
0xb8	Module Reset ctrl setting1
0xb9	IO DC test and PDSW
0xba	CMA112_CODEC analog test and monitor pop noise signal
0xbb	GPIO IO strength setting
0xbc	PDSW/I2C/SPI/SPDIF IO strength setting
0xbd	I2S IO strength setting
0xbe	PLL charge pump current ctrl
0xbf	Testmode value and THD mode
0xc0 ~ 0xc1	GPO Data Register
0xc2 ~ 0xc3	GPI Data Register
0xc4 ~ 0xc5	GPIO Direction Control Register
0xc6 ~ 0xc7	GPIO Interrupt Enable Mask Register
0xc8 ~ 0xc9	GPIO De-bouncing Register
0xca	General Control
0xcb	Buzzer Freq1
0xcc	Buzzer Duty1
0xcd	Buzzer Freq2
0xce	Buzzer Duty2
0xcf	Buzzer On Time
0xd0	Buzzer Cycle Time
0xd1	LED1 Freq
0xd2	LED1 Duty
0xd3	LED1 On Time
0xd4	LED1 Cycle Time
0xd5	LED2 On Time
0xd6	LED2 Cycle Time
0xd7	LED3 On Time
0xd8	LED3 Cycle Time
0xd9	Bounding Option
0xda	GPO_[1:0] Switch Source
0xdb	GPO_[3:2] Switch Source
0xdc	GPO_[5:4] Switch Source
0xdd	GPO_[7:6] Switch Source
0xde	GPO_[9:8] Switch Source
0xdf	GPO_[11:10] Switch Source
0xe0	GPO_[13:12] Switch Source
0xe1	GPO_[15:14] Switch Source
0xe2~0xe3	GPI Remote Choose
0xe4	GPIO pull-up/down Control Register0
0xe5	GPIO pull-up/down Control Register1
0xe6	GPIO pull-up/down Control Register2
0xe7	GPIO pull-up/down Control Register3
0xe8	Share MCU port0
0xe8~0xef	
0xf0	AGC Global Control Register
0xf1	AGC ATTACK TIME CONTROL Register
0xf2	AGC RELEASE TIME CONTROL Register
0xf3	AGC HOLD TIME CONTROL Register
0xf4	AGC Threshold Control Register
0xf5	AGC FIXED GAIN CONTROL Register

0xf6	AGC Global Control Register
0xf7	AGC FIXED GAIN CONTROL
0xf8	AGC Simulate CONTROL
0xf9	AGC GAIN MAX Limit
0xfa	AGC GAIN MIN Limit
0xfb	Clipping LED Timing Control I
0xfc	Clipping LED Timing Control II
0xfd	
0xfe	HID interrupt in start address MSB
0xff	HID interrupt in start address

(POR) : reset by power on reset

USBCON – USB Global Control Register

Address: 00h

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	USBE	**USB Enable Bit** 1 : enable. 0 : disable.	1'b0 (POR)
6	R/W	SUSPCLK	**Suspend USB Clock Bit** 1 : Disable 48 MHz clock input to USB Controller. 0 : Enable 48 MHz clock input to USB Controller.	1'b0
5	R/W	SDRMWUP	**Send Remote Wake-up Bit** 1 : enable. 0 : disable. Must set up RMWUPE of USBCON and equal 1 first. Clear up after 1T write.	1'b0
4			**Reserved**	1'b0
3	R	UPRSM	**Upstream Resume Bit (read only)** Set by hardware when SDRMWUP has been set and if RMWUPE is enabled. Clear up after read.	1'b0
2	R/W	RMWUPE	**Remote Wake-up Enable Bit** 1 : enable. 0 : disable. Note: Do not set this bit if the host has not set the DEVICE_REMOTE_WAKEUP feature for the device.	1'b0
1	R/W	CONFG	**Configuration Bit** When SET_CONFIGURATION Value is set up here.	1'b0
0	R/W	FADDEN	**Function Address Enable Bit** When SET_ADDRESS the Firmware must set 1.	1'b0

USBADDR – USB Address Register

Address: 01h

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	FEN	**Function Enable Bit** 1 : enable. 0 : disable.	1'b0
6-0	R/W	UADD6:0	**USB Address Bits** It shall be written with the value set by a SET_ADDRESS request received by the device firmware.	7'b0

USBINT – USB Global Interrupt Register

Address: 02h

Bits	R/W	Bit Mnemonic	Description	default
7-6			**Reserved**	2'b0
5	R/W	WUPCPU	**Wake Up CPU Interrupt Flag** 1 : interrupt. 0 : none. Set by hardware when EWUPCPU of USBIEN has been set.	1'b0 (POR)
4	R/W	EORINT	**End of Reset Interrupt Flag** 1 : interrupt. 0 : none. Set by hardware when EEORINT of USBIEN has been set.	1'b0 (POR)
3	R/W	SOFINT	**Start of Frame Interrupt Flag** 1 : interrupt. 0 : none. Set by hardware when ESOFINT of USBIEN has been set.	1'b0
2-1			**Reserved**	2'b0
0	R/W	SPINT	**Suspend Interrupt Flag** 1 : interrupt. 0 : none. Set by hardware when ESPINT of USBIEN has been set.	1'b0 (POR)

USBIEN – USB Global Interrupt Enable Register

Address: 03h

Bits	R/W	Bit Mnemonic	Description	default
7-6	R/W		**Reserved**	1'b0
5	R/W	EWUPCPU	**Wake up CPU Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0
4	R/W	EEOFIN	**End Of Reset Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0 (POR)
3	R/W	ESOFINT	**Start Of Frame Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0
2-1			**Reserved**	2'b0
0	R/W	ESPINT	**Suspend Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0

UEPNUM – USB Endpoint Number

Address: 04h

Bits	R/W	Bit Mnemonic	Description	default
7-4	R/W	EPCF7:4	**USB Endpoint Number configuration**	4'h0

			Can setting Endpoint number 0~15 Default setting: EP0(Control) : only = 0 EP1(ISO OUT) : number 1 EP2(ISO IN) : number 2 EP3(Interrupt IN) : number 7 (for compatibility) EP4(Bulk OUT) : number 4 EP5(Bulk IN) : number 5 EP6(Feedback IN) : number 6 EP7(Bulk OUT) : number 8 EP8(Bulk IN) : number 9	
3-0	R/W	EPNUM3:0	**Endpoint Number Bits** Set this field with the number of the endpoint which shall be accessed when reading or writing to registers UEPSTAX, UEPDATX, UBYCTLX or UEPCONX.	4'h0

UEPCONX –USB Endpoint X Control Register (X = EPNUM set in UEPNUM)

Address: 05h

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	EPEN	**Endpoint Enable Bit** 1 : enable. 0 : disable.	1'b0
6	R/W	EPx_DIR	**Endpoint Direction Bit** 1 : Set to configure IN direction. 0 : Set to configure OUT direction. This bit has no effect for Control endpoints. Only valid for EP4, EP5, EP7, EP8 Default EP4 = OUT EP5 = IN EP7 = OUT EP8 = IN	1'bX
5	R/W	EPx_ZLEN	BULK Endpoint zero length packet For EP4, EP5, EP7, EP8 as bulk in endpoint 1'b1 : send zero-length IN packet 1'b0 : IN packet length depended on wt_point Clear to 1'b0 after this zero-length IN packet is transmitted	1'b0
4	R/W		**Reserved**	1'b0
3	R	~~DTGL~~	~~**Data Toggle Status Bit (Read-only)**~~ ~~1 : Set by hardware when a DATA1 packet is received.~~ ~~0 : Set by hardware when a DATA0 packet is received.~~	1'b0
2	R/W		**Reserved**	1'b0
1-0	R/W	~~EPTYPE 1:0~~	~~**Endpoint Type Bits**~~ ~~0 0 : Control endpoint~~ ~~0 1 : Isochronous endpoint~~ ~~1 0 : Bulk endpoint~~ ~~1 1 : Interrupt endpoint~~	2'b0

UEPSTAX – USB Endpoint X Status and Control Register (X = EPNUM set in UEPNUM)

Address: 06h

Bits	R/W	Bit	Description	default

		Mnemonic		
7	R/W	DIR	**Control Endpoint Direction Bit** 1: data stage. 0: Clear otherwise. **NOTE:** When Endpoint Number=2, this bit can turn on valid record bit (VALID_REC).	1'b0
6	R/W	PLAY_REC	**Alternate Setting Bit (AUDIO Device)** 1 : enable. 0 : disable When Endpoint Number = 1 expresses it is PLAY. When Endpoint Number = 2 expresses it is RECORD.	1'b0
5	R/W	STALLRQ	**Stall Handshake Request Bit** 1 : enable. 0 : disable. Set to send a STALL answer to the host for the next handshake. Clear otherwise	1'b0
4	R/W	TXRDY	**TX Packet Ready Control Bit** 1 : enable. 0 : disable. Cleared by hardware when ACK packet was received.	1'b0
3	R/W	STLCRC	**Stall Sent Interrupt Flag/CRC Error Interrupt Flag** 1 : interrupt. 0 : none. Set by hardware after a STALL handshake has been sent as requested by STALLRQ. Cleared by hardware when a SETUP packet was received.	1'b0
2	R/W	RXSETUP	**Received SETUP Interrupt Flag** 1 : interrupt. 0 : none. Clear by software after reading the SETUP data from the endpoint FIFO.	1'b0
1	R/W	RXOUT	**Received OUT Data Interrupt Flag** 1 : interrupt. 0 : none. Clear by software after reading the OUT data from the endpoint FIFO.	1'b0
0	R/W	TXCMP	**Transmitted IN Data Complete Interrupt Flag** 1 : interrupt. 0 : none. Clear by software before setting again TXRDY.	1'b0

UEPRST –USB Endpoint FIFO Reset Register

Address: 07h

Bits	R/W	Bit Mnemonic	Description	default
7			**Reserved**	1'b0
6	R/W	EP6RST	**Endpoint 6 FIFO Reset** 1 : reset. 0 : none. Clear up after write.	1'b0
5	R/W	EP5RST	**Endpoint 5 FIFO Reset**	1'b0

			1 : reset. 0 : none. Clear up after write.	
4	R/W	EP4RST	**Endpoint4 FIFO Reset** 1 : reset. 0 : none. Clear up after write.	1'b0
3	R/W	EP3RST	**Endpoint 3 FIFO Reset** 1 : reset. 0 : none. Clear up after write.	1'b0
2	R/W	EP8RST	**Endpoint 8 FIFO Reset** 1 : reset. 0 : none. Clear up after write.	1'b0
1	R/W	EP7RST	**Endpoint 7 FIFO Reset** 1 : reset. 0 : none. Clear up after write.	1'b0
0	R/W	EP0RST	**Endpoint 0 FIFO Reset** 1 : reset. 0 : none. Clear up after write.	1'b0

UEPINT – USB Endpoint Interrupt Register

Address: 08h

Bits	**R/W**	**Bit Mnemonic**	**Description**	**default**
7			**Reserved**	1'b0
6	R	EP6INT	**Endpoint 6 Interrupt Flag** 1 : interrupt. 0 : none.	1'b0
5	R	EP5INT	**Endpoint 5 Interrupt Flag** 1 : interrupt. 0 : none.	1'b0
4	R	EP4INT	**Endpoint 4 Interrupt Flag** 1 : interrupt. 0 : none.	1'b0
3	R	EP3INT	**Endpoint 3 Interrupt Flag** 1 : interrupt. 0 : none.	1'b0
2	R	EP8INT	**Endpoint 8 Interrupt Flag** 1 : interrupt. 0 : none.	1'b0
1	R	EP7INT	**Endpoint 7 Interrupt Flag** 1 : interrupt. 0 : none.	1'b0
0	R	EP03INT	**Endpoint 0 Interrupt Flag** 1 : interrupt. 0 : none.	1'b0

UEPIEN – USB Endpoint Interrupt Enable Register

Address: 09h

Bits	R/W	Bit Mnemonic	Description	default
7			**Reserved**	1'b0
6	R/W	EP6INTE	**Endpoint 6 Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0
5	R/W	EP5INTE	**Endpoint 5 Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0
4	R/W	EP5INTE	**Endpoint 4 Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0
3	R/W	EP3INTE	**Endpoint 3 Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0
2	R/W	EP8INTE	**Endpoint 8 Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0
1	R/W	EP7INTE	**Endpoint 7 Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0
0	R/W	EP03INTE	**Endpoint 0 Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0

UEPDATX – USB Endpoint X FIFO Data Register (X = EPNUM set in UEPNUM)

Address: 0ah

Bits	R/W	Bit Mnemonic	Description	default
7-0	R/W	FDAT7:0	**Endpoint X FIFO Data**	7'b0

UBYCTX – USB Endpoint X Byte Count Register (X = EPNUM set in UEPNUM)

Address: 0bh

Bits	R/W	Bit Mnemonic	Description	default
7-0	R/W	BYCT7:0	**Byte Count** Byte count of a received data packet.	7'b0

UFNUML– USB Frame Number Low Register(HW not ready)

Address: 0ch

Bits	R/W	Bit Mnemonic	Description	default
7-0	R/W	FNUM7:0	**Frame Number** Lower 8 Bits of the 11-bit Frame Number. Not ready	7'b0

UFNUMH – USB Frame Number High Register (HW not ready)

Address: 0dh

Bits	R/W	Bit Mnemonic	Description	default
7-6			**Reserved**	2'b0
5	R/W	CRCOK	**Frame Number CRC OK Bit** 1 : ok. 0 : none. Not ready	1'b0
4	R/W	CRCERR	**Frame Number CRC Error Bit** 1 : error. 0 : none. Not ready	1'b0
3	R/W		**Reserved**	1'b0
2-0	R/W	FNUM10:8	**Frame Number** Upper 3 Bits of the 11-bit Frame Number. Not ready	3'b0

COEDC Play_rate + Record_rate

Address: 0eh

Bits	R/W	Bit Mnemonic	Description	default
7-4	R/W	R_FREQ	**Record Frequency Rate** 4'b1000 : 96 KHz. 4'b0111 : 88.2 KHz. 4'b0110 : 48 KHz. (default) 4'b0101 : 44.1 KHz. 4'b0100 : 32 KHz. 4'b0011 : 22.05 KHz. 4'b0010 : 16 KHz. 4'b0001 : 11.025 KHz. 4'b0000 : 8 KHz.	4'b0110
3-0	R/W	P_FREQ	**PLAY Frequency Rate** 4'b1000 : 96 KHz. 4'b0111 : 88.2 KHz. 4'b0110 : 48 KHz.(default) 4'b0101 : 44.1 KHz. 4'b0100 : 32 KHz. 4'b0011 : 22.05 KHz. 4'b0010 : 16 KHz. 4'b0001 : 11.025 KHz. 4'b0000 : 8 KHz.	4'b0110

Resolution 24-bit Enable of play+ rec

Address: 0fh

Bits	R/W	Bit Mnemonic	Description	default
7-2			**Reserved**	6'b0
1	R/W	RBR24E	**Record Bit Resolution 24-bits Enable** 1 : enable. (24-bits) 0 : disable. (16-bits)	1'b0
0	R/W	PBR24E	**Play Bit Resolution 24-bits Enable**	1'b0

			1 : enable. (24-bits) 0 : disable. (16-bits)	

PER1INT – Peripheral 1 Interrupt Register

Address: 10h

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	TESTMODE_INT	**TEST MODE Interrupt Flag** 1 : interrupt. 0 : none. Clear up after write.	1'b0
6	R/W	VR_INT	**VR Interrupt Flag** 1 : interrupt. 0 : none. Clear up after write.	1'b0
5	R/W	GPI_INT	**GPI Interrupt Flag** 1 : interrupt. 0 : none. Clear up after write.	1'b0 (POR)
4	R/W	SPIS_INT	**SPI Slave Interrupt Flag** 1 : interrupt. 0 : none. Clear up after write.	1'b0 (POR)
3	R/W	SPI_INT	**SPI Interrupt Flag** 1 : interrupt. 0 : none. Clear up after write.	1'b0 (POR)
2	R/W	I2CS_INT	**I2C Slave Interrupt Flag** 1 : interrupt. 0 : none. Clear up after write.	1'b0 (POR)
1	R/W	I2CM_INT	**I2C Master Interrupt Flag** 1 : interrupt. 0 : none. Clear up after write.	1'b0 (POR)
0	R/W	IR_INT	**IR Interrupt Flag** 1 : interrupt. 0 : none. Clear up after write.	1'b0

PER1INT – Peripheral 1 Interrupt Enable Register

Address: 11h

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	TESTMODE_INTE	**TestMode Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0
6	R/W	VR_INTE	**VR Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0

5	R/W	GPI_INTE	**GPI Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0 (POR)
4	R/W	SPIS_INTE	**SPI Slave Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0 (POR)
3	R/W	SPI_INTE	**SPI Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0 (POR)
2	R/W	I2CS_INE	**I2C Slave Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0 (POR)
1	R/W	I2CM_INTE	**I2C Master Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0 (POR)
0	R/W	IR_INTE	**IR Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0

PER2INT – Peripheral 2 Interrupt Register

Address: 12h

Bits	R/W	Bit Mnemonic	Description	default
7			**Reserved**	1'b0
6	RO	SE1_INT	**SE1 Interrupt Flag** 1 : interrupt. 0 : none.	1'b0 (POR)
5	R/W	UART_W_INT	**UART TX Interrupt Flag** 1 : interrupt. 0 : none. Clear up after write.	1'b0
4	R/W	BAUD_INT	**BAUD rate Interrupt Flag** 1 : interrupt. 0 : none. Clear up after write.	1'b0
3	R/W	SPI2_INT	**Internal SPI Interrupt Flag** 1 : interrupt. 0 : none. Clear up after write.	1'b0
2	R/W	RATE_INT	**SPDIF Rate Interrupt Flag** 1 : interrupt. 0 : none. Clear up after write.	1'b0
1	R/W	LOCK_INT	**SPDIF Lock Interrupt Flag** 1 : interrupt. 0 : none. Clear up after write.	1'b0
0	R/W	SENSE_INT	**SPDIF Sense Interrupt Flag** 1 : interrupt.	1'b0

			0 : none. Clear up after write.	

PER1INT – Peripheral 2 Interrupt Enable Register

Address: 13h

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	SE1_Clear	**SE1 interrupt Clear Bit** Clear up REG-12[6] after write.	1'b0 (POR)
6	R/W	SE1_INTE	**SE1 Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0 (POR)
5	R/W	UART_W_INTE	**UART TX Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0
4	R/W	BAUD_INTE	**BAUD rate Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0
3	R/W	SPI2_INTE	**Internal SPI Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0
2	R/W	RATE_INE	**SPDIF Rate Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0
1	R/W	LOCK_INTE	**SPDIF Lock Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0
0	R/W	SENSE_INTE	**SPDIF Sense Interrupt Enable Bit** 1 : enable. 0 : disable.	1'b0

ISOFRPL – ISO OUT FIFO Read Pointer Low Register

Address: 14h

Bits	R/W	Bit Mnemonic	Description	default
7-0	R	ISOFRP7:0	**ISO OUT FIFO Read Pointer** Lower 8 Bits of the 10-bits Read Pointer.	8'h0

ISOFRPH – ISO OUT FIFO Read Pointer High Register

Address: 15h

Bits	R/W	Bit Mnemonic	Description	default
7-4			**Reserved**	4'b0
3	RO	VALID_REC	ISO in valid	1'b0
2	RO	VALID_PLAY	ISO out valid	1'b0
1-0	R	ISOFRP9:8	**ISO OUT FIFO Read Pointer** Upper 2 Bits of the 10-bits Read Pointer. p.s. SOFRP9 is indicate ping-pong status, FIFO read pointer over 10'd400 the SOFRP9 will set invert oneself.	2'h0

ISOFWPL – ISO OUT FIFO Write Pointer Low Register

Address: 16h

Bits	R/W	Bit Mnemonic	Description	default
7-0	R	ISOFWP7:0	**ISO OUT FIFO Write Pointer** Lower 8 Bits of the 10-bits Write Pointer.	8'h0

ISOFWPH – ISO OUT FIFO Write Pointer High Register

Address: 17h

Bits	R/W	Bit Mnemonic	Description	default
7-2			**Reserved**	6'b0
1-0	R	ISOFWP9:8	**ISO OUT FIFO Write Pointer** Upper 2 Bits of the 10-bits Write Pointer. p.s. SOFWP9 is indicate ping-pong status, FIFO Write pointer over 10'd400 the SOFWP9 will set invert oneself.	2'h0

ISOFSNL – ISO OUT FIFO Surplus Number Low Register

Address: 18h

Bits	R/W	Bit Mnemonic	Description	default
7-0	R	ISOFSN7:0	**ISO OUT FIFO Surplus Number** Lower 8 Bits of the 10-bits Surplus Number.	8'h0

ISOFSNH –ISO OUT FIFO Surplus Number High Register

Address: 19h

Bits	R/W	Bit Mnemonic	Description	default
7-2			**Reserved**	6'b0
1-0	R	ISOFSN9:8	**ISO OUT FIFO Surplus Number** Upper 2 Bits of the 10-bits Surplus Number.	2'h0

Debug monitor

Address: 20h

Bits	R/W	Bit Mnemonic	Description	default
7-3			**Reserved**	5'b0
2-0	R	TFFSM	**Debug monitor** Transfer FSM monitor.	3'h0

Address: 21h

Bits	R/W	Bit Mnemonic	Description	default
7-6			**Reserved**	3'b0
5-0	R	TAFSM	**Debug monitor** Transaction FSM monitor.	5'h0

MCU access FIFO mapping setting

Address: 22h

Bits	R/W	Bit Mnemonic	Description	default
7-1			**Reserved**	5'b0
0	R/W	**FIFO_24bit_selected**	**MCU access fifo 3/2 byte setting** 1 : 24 bit mapping	1'b1 (POR)

			0 : 16 bit mapping	

Playback Write pointer enable and index

Address: 28h~29h

Bits	R/W	Bit Mnemonic	Description	default
15	R/W	REG_PLAY_WE	Enable register control playback write pointer.	0x0
14:10	RO		Reserved	0x00
9:0	R/W	REG_PLAY_WPT	Playback write pointer register.	0x00

Playback Read pointer enable and index

Address: 2ah~2bh

Bits	R/W	Bit Mnemonic	Description	default
15	R/W	REG_PLAY_RE	Enable register control playback read pointer.	0x0
14:10	RO		Reserved	0x00
9:0	R/W	REG_PLAY_RPT	Playback read pointer register.	0x00

Record Write pointer enable and index

Address: 2ch~2dh

Bits	R/W	Bit Mnemonic	Description	default
15	R/W	REG_REC_WE	Enable register control record write pointer.	0x0
14:11	RO		Reserved	0x00
10:0	R/W	REG_REC_WPT	Record write pointer register.	0x00

Record Read pointer enable and index

Address: 2eh~2fh

Bits	R/W	Bit Mnemonic	Description	default
15	R/W	REG_REC_RE	Enable register control record read pointer.	0x0
14:11	RO		Reserved	0x00
10:0	R/W	REG_REC_RPT	Record read pointer register.	0x00

I²C Slave Register

~~Address: 30h~37h~~

~~Bits~~	~~R/W~~	~~Bit Mnemonic~~	~~Description~~	~~default~~
~~7-0~~	~~R/W~~	~~I2CS_DATA0~~	~~If external MCU wants to do the communication with internal MCU , it can draw on the 8 byte.~~	~~0x00~~

~~**I²C Slave CTRL (USB Reset)**~~

~~Address: 38h~~

~~Bits~~	~~R/W~~	~~Bit Mnemonic~~	~~Description~~	~~default~~
~~7-0~~	~~R/W~~	~~I2CS_CTRL~~	~~Trigger I²C Slave issued interrupt to MCU~~ ~~0->1: Issued I²C Slave Interrupt.~~ ~~1->0: Slave mode Data is received by int MCU.~~ ~~0 : No data is conveyed.~~ ~~1 : Slave mode Data is gotten by int MCU.~~ ~~This bit is programmed by ext MCU to note int MCU there are new arrival data in 0x30~0x37~~	~~0x00~~

I2CS_DATA: 2-Wire serial bus data register

Address: 30~33h

Bits	R/W	Bit Mnemonic	Description	Default

31:0	R/W	MCU_data0~F	The data received from or transmitted to master device. This register can not be written when 2-wire slave serial bus status is busy.	0000h (POR)

I2CS_STATUS: 2-Wire serial bus status register

Address: 34~35h

Bits	R/W	Bit Mnemonic	Description	Default
~~15~~	~~R/W~~	~~I2c_mas_sel~~	~~I2C master/slave select~~	~~1b~~
14:12	R		Reserved	0h
11	R/W	Thld_int_mask	Threshold interrupt mask: 1: mask ; 0: non-mask ; default :0	0b (POR)
10	R	Write_data_ready	Interrupt happened, auto-cleared after read	0b (POR)
9	R/W	I2c_s_reset	0: 2-wire serial bus in normal operation (default) 1: 2-wire serial bus in reset state	0b (POR)
8	R/W	Dri_tran_st	**initiated transaction status** 1: The last initiated transaction failed, write 1 to clear.	0b (POR)
7	R/W	Rd_tran_st	**Read transaction status** 1: a new read transaction received, write 1 to clear.	0b (POR)
6	R/W	Wr_tran_st	**Write transaction status** 1: a new write transaction received, write 1 to clear.	0b (POR)
5:1	R	Data_len	The data length of the last write transaction received, 00000: 1 byte (MAP only) 00001: 2 byte (MAP + 1 byte data) 00010: 3 byte (MAP + 2 byte data) 00011: 4 byte (MAP + 3 byte data) 00100: 5 byte (MAP + 4 byte data) … 01111: 16 byte (MAP + 15 byte data) . 10000: 17 byte (MAP + 16 byte data) Others: Reserved	0b (POR)
0	R	busy	The 2-wire serial bus status, 0: idle, 1: busy	0b (POR)

Note: When I2C issue interrupt to MCU, MCU need to read the data numbers that threshold data count specified. And wait another interrupt until the total data transfer completed.

I2CS_MAP: Memory address pointer (MAP)

Address: 36h

Bits	R/W	Bit Mnemonic	Description	Default
7:0	R/W	MCU_MAP	The memory address of the read or write transactions from MCU. Address 0 is reserved for initiated transaction.	00h (POR)

I2CS_STATUS: 2-Wire serial bus status register

Address: 37h

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	Sync_en	**Synchronization enable** 1: enable (the synchronization selection bit will decide the method adopted). 0: disable (MCU and ARC should guarantee no data lost themselves).	1b (POR)
6	R/W	Int_polarity	The polarity control of pin INT_OUT (initiated transaction interrupt), 0: high active, 1: low active	0b (POR)
5:4	R/W	Slave_addr	Slave Device Address 00: select 0001000 (10h) as slave address 01: select 0001001 (12h) as slave address 10: select 0001010 (14h) as slave address 11: select 0001011 (16h) as slave address	01b (POR)
3	R/W	Sync_sel	**Synchronization method selection** 1: Data synchronization. When this bit is one, if the current transaction has not been serviced by ARC, the clock line of the 2-wire serial bus will be pulled low. Under this situation, the MCU can not start a new transaction or continue the current read transaction until the clock line goes back to high. 0: Ready pin synchronization. If the MCU can not support open drain 2-wire serial bus, this bit should be set to zero. Under this situation, the MCU can not start a new transaction or continue the current read transaction until the pin XSLAVE_RDY goes high to signal that the driver has serviced the current transaction. Driver should use "driver acknowledge" to signal the processing of the current transaction is completed.	1b (POR)
2	R/W	Int_mask	**Interrupt Mask** 0: interrupt will happen at a read/write transaction received or a driver initiated transaction failed 1: interrupt will not happen	0b (POR)
1	R/W	Dri_init_tran	**Driver initiated transaction** Write 1 to start Driver initiated transaction. This bit is cleared automatically, after ARC initiated transaction starts. The ARC initiated transaction should be issued only when the 2-wire slave serial bus is idle. Otherwise, it will be ignored. The ARC initiated transaction will cause pin INT_OUT to send out an interrupt for MCU. After MCU responded with a Write-MAP-Address-0-Only transaction and a subsequent read transaction, interrupt INT_OUT will	0b (POR)

			be de-asserted. However, if the MCU does not act as what is expected (a write MAP-Address-0-Only transaction and a subsequent read transaction), the interrupt INT_OUT will be still de-asserted, but the ARC initiated transaction status is used to signal a fail status to ARC. In this case, the driver should consider to repeat the failed Driver initiated transaction again.	
0	R/W	ack	Driver Acknowledge means driver has processed the current transaction. Write 1 to acknowledge. This bit will be cleared automatically.	0b (POR)

SPI I/F Registers Descriptions for EXT

SPI Data Register

Address: 39h~3bh

Bits	R/W	Bit Mnemonic	Description	default
23-0	R/W	Data0	The data (which include address, r/w, and data bits) written to or read from the codec. The bits in this register should be interpreted according to the individual codec. The content of this register, after a write operation completes, has no meaning. The content of this register, after a read operation completes, should reference the document of individual codec to see how many bits in this register is valid. For example, if codec is Analog Device AD1837, then SPI_Data_Reg[9:0] will be valid data	0x0000 0000 (POR)

SPI Control Register 0

Address: 3ch

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	slv_mst	SPI master/slave mode 0 : master mode 1: slave mode	1'b1 (POR)
6	R/W	long_mode	SPI slave address length 0: 1-byte address 1: 2-byte address	1'b1 (POR)
5			Reserved	1'b0(POR)
4	R/W	ra8815_rw	RA8815 3-wire mode R/W 0 : Write command 1: Read command	1'b0 (POR)
3	R/W	si_mode	Serial interface mode 0 : normal SPI mode 1: Serial interface mode	1'b0 (POR)
2	R/W	si_mode_rs	Serial interface RS/A0 output 0: RS/A0==0 for 8th bit 1: RS/A0==1 for 8th bit	1'b0 (POR)
1-0	R/W	data_len	The data length of read/write, 00: Reserved 01: 1 bytes	1'b0 (POR)

			10: 2 bytes 11: 3 bytes	

*Note:

1. Bit [4]: RA8815 3-wire mode is designated for RA8815 LCD controller.
2. Bit [3]: Serial interface mode is designated for other LCD controllers such as ST7565, NT7606, etc. It is write-only which the data cannot read out from LCD controller.
3. Bit [2]: In Serial interface mode, A0 is for ST7565; RS is for NT7606.
4. Bit [1:0]: Both RA8815 and Serial interface mode are two-byte in total length.

SPI Control Register 1

Address: 3dh

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	spi_start	Trigger SPI read/write command 0->1: trigger SPI read/write command. 1->0: SPI interface had completed current task. 0 : SPI interface is idle and ready for work. 1 : SPI interface is running.	1'b0 (POR)
6	R/W	spi_lh_edge	SPI CEN control 0: codec latch control data at SPI clock low (default) 1: codec latch control data at SPI clock high	1'b1 (POR)
~~5~~	~~R/W~~	~~cs10~~	~~Chip/Codec select~~ ~~0: Chip/Codec 0~~ ~~1: Chip/Codec 1~~	~~1'b0~~
4-3	R/W	frq_sel	SPI clock period 00: 330 ns 01: 980 ns 10: 1300 ns 11: 1600 ns (1.6 micro-second)	2'b0 (POR)
2	R/W	first_leading_bit	First data bit of 2-bit leading mode	1'b0(POR)
1	R/W	second_leading_bit	Second data bit of 2-bit leading mode	1'b0(POR)
0	R/W	leading_bit_mode	RA8815 2-bit leading mode 0: No leading bits 1: 2-bit leading for each transaction	1'b0 (POR)

SPI Interrupt

Address: 3eh

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	CPOL	Clock Polarity	1'b1(POR)
6	R/W	CPHA	Clock Phase	1'b1(POR)
5-4	R/W		Reserved	2'b0(POR)
3	RO	slv_hid	SPI slave flag to HID interrupt 0: access to internal register 1: flag to HID interrupt	1'b0 (POR)
2	RO	slv_rw	SPI slave read/write flag 0: read 1: write	1'b0 (POR)
1	R/W	slv_int_en	SPI slave interrupt 0: no interrupt 1: interrupt (Default) Ext MCU can program this bit to make slave	1'b1 (POR)

			mode interrupt	
0	R/W	mst_int_en	SPI master interrupt enable 0: disable 1: enable (Default) Control HW to make master mode interrupt	1'b1 (POR)

*Note:

1. Bit [1]: When SPI interface is slave mode, SPI interrupt happened when bit [1] ==1, which is written by external MPU via SPI. Interrupt (HID) would be cleaned once address 0x10 was written.
2. Bit [0]: When SPI interface is master mode, SPI interrupt happened when bit [0] ==1 and every SPI master command completed. Interrupt (HID) would be cleaned once address 0x10 was written.

EQ Register Description for Playback

EQ Maximum Range

Bits	R/W	**Bit Mnemonic**	Description	Default
7-0	R/W		EQ Maximum range (defined by EEPROM now) MAX attributes can range from +31.75 dB (0x7F) down to 0.00 dB (0x00) in steps of 0.25 dB (0x01). 0x30 means +12 dB for MAX. MIN attributes is minus MAX. 0x30 means -12 dB for MIN.	

Gain Value (decimal)	Meaning
0	-12 dB
1	-11.5 dB
2	-11 dB
3	-10.5 dB
4	-10 dB
5	-9.5 dB
6	-9 dB
7	-8.5 dB
8	-8 dB
9	-7.5 dB
10	-7 dB
11	-6.5 dB
12	-6 dB
13	-5.5 dB
14	-5 dB
15	-4.5 dB
16	-4 dB
17	-3.5 dB
18	-3 dB
19	-2.5 dB
20	-2 dB
21	-1.5 dB
22	-1 dB
23	-0.5 dB
24	0 dB
25	+0.5 dB
26	+1 dB
27	+1.5 dB
28	+2 dB

29	+2.5 dB
30	+3 dB
31	+3.5 dB
32	+4 dB
33	+4.5 dB
34	+5 dB
35	+5.5 dB
36	+6 dB
37	+6.5 dB
38	+7 dB
39	+7.5 dB
40	+8 dB
41	+8.5 dB
42	+9 dB
43	+9.5 dB
44	+10 dB
45	+10.5 dB
46	+11 dB
47	+11.5 dB
48	+12 dB

EQ Band1's Gain Register
Address: 0x40

Bits	R/W	**Bit Mnemonic**	Description	Default
7-6	R/W		Reserved	0x0
5-0	R/W	Band1_ctrl_Mx	Band1's Gain : -3.5dB(default)	6'h11

EQ Band2's Gain Register
Address: 0x41

Bits	R/W	**Bit Mnemonic**	Description	Default
7-6	R/W		Reserved	0x0
5-0	R/W	Band2_ctrl_Mx	Band2's Gain : -3.5dB(default)	6'h11

EQ Band3's Gain Register
Address: 0x42

Bits	R/W	**Bit Mnemonic**	Description	Default
7-6	R/W		Reserved	0x0
5-0	R/W	Band3_ctrl_Mx	Band3's Gain : -3.5dB(default)	6'h11

EQ Band4's Gain Register
Address: 0x43

Bits	R/W	**Bit Mnemonic**	Description	Default
7-6	R/W		Reserved	0x0
5-0	R/W	Band4_ctrl_Mx	Band4's Gain : -3.5dB(default)	6'h11

EQ Band5's Gain Register
Address: 0x44

Bits	R/W	**Bit Mnemonic**	Description	Default
7-6	R/W		Reserved	0x0
5-0	R/W	Band5_ctrl_Mx	Band5's Gain : -3.5dB(default)	6'h11

EQ Disable & EQ_TEST_MODE Register
Address: 0x45

Bits	R/W	**Bit Mnemonic**	Description	Default
~~7~~	~~R/W~~	~~Load_org~~	~~Load coefficient of the selection of sound switch setting.~~	~~0x0~~
5-0	R/W	OP_gain_pre	OP gain	6'd24

~~1~~	~~R/W~~	~~Eq_test_mode~~	~~EQ_TEST_MODE~~	~~1'b0~~
~~0~~	~~R/W~~	~~Eq_off~~	~~EQ Disable~~	~~1'b1~~

【NOTE】EQ Disable only can be modified after USBRST and before sending audio data to RM5013

Registers from 0x47-0 ~ 0x47-b cannot be modified when playing audio data.

1. Write 0x46 to choose band number;
2. Write 0x47 to put 12 bytes coefficient

Access which band of EQ filter coefficient
Address: 0x46

Bits	R/W	**Bit Mnemonic**	Description	Default
7	R/W	Eq_test_mode	EQ_TEST_MODE	1'b0
6	R/W	Eq_off	EQ Disable	1'b1
5-4	R/W		Reserved	0x0
3	R/W	Load_org	Load coefficient of the selection of sound switch setting.	0x0
2-0	R/W	bandnum	Band number	3'b000

Filter coefficient port
Address: 0x47

Bits	R/W	**Bit Mnemonic**	Description	Default
7-0	R/W	Coeff_X	Band'x coefficient value	8'b0

EQ BandX Coefficient Registers Descriptions

EQ BandX's Coefficient A21 Register1
Address: 0x47-0

Bits	R/W	Description	Default
7-0	R/W	BandX's Coefficient A21 Register1(MSB)	TBD

EQ BandX's Coefficient A21 Register2
Address: 0x47-1

Bits	R/W	Description	Default
7-0	R/W	BandX's Coefficient A21 Register2	TBD

EQ BandX's Coefficient A21 Register3
Address: 0x47-2

Bits	R/W	Description	Default
7-0	R/W	BandX's Coefficient A21 Register3	TBD

EQ BandX's Coefficient A21 Register4
Address: 0x47-3

Bits	R/W	Description	Default
7-0	R/W	BandX's Coefficient A21 Register4(LSB)	TBD

EQ BandX's Coefficient A31 Register1
Address: 0x47-4

Bits	R/W	Description	Default
7-0	R/W	BandX's Coefficient A31 Register1(MSB)	TBD

EQ BandX's Coefficient A31 Register2
Address: 0x47-5

Bits	R/W	Description	Default
7-0	R/W	BandX's Coefficient A31 Register2	TBD

EQ BandX's Coefficient A31 Register3
Address: 0x47-6

Bits	R/W	Description	Default
7-0	R/W	BandX's Coefficient A31 Register3	TBD

EQ BandX's Coefficient A31 Register4
Address: 0x47-7

Bits	R/W	Description	Default
7-0	R/W	BandX's Coefficient A31 Register4(LSB)	TBD

EQ BandX's Coefficient S Register1
Address: 0x47-8

Bits	R/W	Description	Default
7-0	R/W	BandX's Coefficient S Register1(MSB)	TBD

EQ BandX's Coefficient S Register2
Address: 0x47-9

Bits	R/W	Description	Default
7-0	R/W	BandX's Coefficient S Register2	TBD

EQ BandX's Coefficient S Register3
Address: 0x47-a

Bits	R/W	Description	Default
7-0	R/W	BandX's Coefficient S Register3	TBD

EQ BandX's Coefficient S Register4
Address: 0x47-b

Bits	R/W	Description	Default
7-0	R/W	BandX's Coefficient S Register4(LSB)	TBD

EQ sample period
Address: 0x48

Bits	R/W	**Bit Mnemonic**	Description	Default
7-0	R/W	Sample_period	Gain tracking step, unit is one sample time	8'h0a

SoundSwitch setting from software
Address: 0x49

Bits	R/W	**Bit Mnemonic**	Description	Default
7-3	R/W		Reserved	0x00
2	R/W		SoundSwitch_sel. 1→means SoundSwitch value comes from software.	0x1
1-0	R/W		SoundSwitch[1:0] from software	0x0

EQ mode gain setting
Address: 0x4a

Bits	R/W	**Bit Mnemonic**	Description	Default
7-2	R/W		Reserved	0x0
1-0	R/W	Mode_sel	For access band gain in each mode 2'b00 : default 2'b01 : gaming 2'b10 : communication 2'b11 : movie **Please set this value first, then**	2'b0

			access 0x40 ~0x44 gain setting	

PLL TESTMODE offset_p
Address: 50h

Bits	R/W	Bit Mnemonic	Description	Default
7-0	R/W	TESTOFT_P[8:1]	programming offset to debug PLL_P	8'h20

PLL TESTMODE offset_r
Address: 51h

Bits	R/W	Bit Mnemonic	Description	Default
7-0	R/W	TESTOFT_R[8:1]	programming offset to debug PLL_R	8'hBD

PLL TESTMODE offset_rp
Address: 52h

Bits	R/W	Bit Mnemonic	Description	default
~~7-4~~	~~R/W~~	~~TESTOFT_R[12:9]~~	~~programming offset to debug PLL_R~~	~~4'h2~~
~~3-0~~	~~R/W~~	~~TESTOFT_P[12:9]~~	~~programming offset to debug PLL_P~~	~~4'h7~~
7-4	R/W		Reserved	
3-2	R/W	TESTOFT_R[10:9]	programming offset to debug PLL_R	2'b10
1-0	R/W	TESTOFT_P[10:9]	programming offset to debug PLL_P	2'b01

UART baud rate select
Address: 53h

Bits	R/W	Bit Mnemonic	Description	default
2-0	R/W	Pllcodecreg03	UART baud rate select (Write this register will trigger BAUD_INT) 101: 57600Hz 100: 38400Hz 011: 19200Hz 010: 9600Hz 001: 4800Hz 000: 2400Hz	3'b101 (POR)

PLL TESTMODE mode_rp_48m setting
Address: 54h

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	OFFSET_REG_EN	Offset and mode can be controlled by register 1: The offset will be set from register setting.	1'b0
~~6~~	~~R/W~~	~~TMODE_48M~~	~~TMODE_48M~~	~~1'b1~~
5	R/W	TMODE_P	TMODE_P	1'b0
4	R/W	TMODE_R	TMODE_R	1'b1
~~3-0~~	~~R/W~~	~~TESTOFT_48M[12:9]~~	~~programming offset to debug PLL_48M~~	~~4'h9~~

PLL Software scale setting
Address: 55h

Bits	R/W	Bit Mnemonic	Description	default

7-6			Reserved.	2'b0
5	R/W	SW_SCALE	Software scale enable 1:enable, 0:disable	1'b0
4:0	R/W	REG_SCALE	Scale value for PLL adjustment	5'h8

PLL adaptive function enable
Address: 56h

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	PD_PLAY	Power-Down playback PLL.	1'b0
6	R/W	PD_REC	Power-Down record PLL.	1'b0
~~5~~	~~R/W~~	~~PD_HDA~~	~~Power-Down HDA PLL.~~	~~1'b0~~
5:4	R/W	SW_USB	Control bits for USB switch: 2'b00: USB20 Off, USB11 Off. 2'b01: USB20 Off, USB11 On. 2'b10: USB20 On, USB11 Off. 2'b11: USB20 On, USB11 On.	2'b0 (POR)
3	R/W	HBSCALDN	Difference of Fifo read/write pointer judge value	1'b0
2	R/W	DISPLLAD	disable PLL HW adaptive adjustment; default = 1'b0	1'b0
1	R/W	PLLBINEN_R	PLL HW adaptive adjustment by binary tree enable when record;default = 1'b0 (disabled)	1'b0
0	R/W	PLLBINEN	PLL HW adaptive adjustment by binary tree enable when playback;default = 1'b0 (disabled)	1'b0

Ext I2S format + slave mode setting
Address: 57h

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	PLAY_SLV	Slave mode playback, use external BCLK and LRCK	1'b0
6	R/W	LJTFD_SLV_P	DAC slave mode Left-justified 1'b1 : left-justified	1'b0
5	R/W	LJTFD_P	DAC left justified format; 1'b0 : I2S format	1'b0
4	R/W	REC_SLV	Slave mode record, use external BCLK and LRCK	1'b0
3	R/W	LJTFD_SLV	ADC slave mode Left-justified 1'b1 : left-justified	1'b0
2	R/W	LJTFD	ADC left justified format; 1'b0 : I2S format	1'b0
1	R/W	FSX512P	Playback MCLK-to-LRCK ratio 1'b1 : I2S Mclk with 512fs; 1'b0 : with 256fs	1'b0
1	R/W	FSX512R	Record MCLK-to-LRCK ratio 1'b1 : I2S Mclk with 512fs; 1'b0 : with 256fs	1'b0

PLL powerdown and dacfilter disable
Address: 58h

Bits	R/W	Bit Mnemonic	Description	default
7:6	R/W	Codec_selp	Playback Codec Select ~~00: Select External HDA~~	2'b10

			01: Select External I2S 10: Select Internal I2S 11: Select Internal I2S with DSP	
5:4	R/W	Codec_selr	Record Codec Select ~~00: Select External HDA~~ 01: Select External I2S 10: Select Internal I2S 11: Select Internal I2S with DSP	2'b10
3	R/W	PD_USB_PLL	Power down PLL used for USB	1'b0
2	R/W	PD_CODEC_PLL	Power down PLL used for codec	1'b0
1	R/W	PDBIAS	Power down PLL bias	1'b0
0	R/W	dac_disable	If dac filter is off but adc filter is on, set this bit to 1 let register be programmed by adc mclk.	1'b0

External I2S signal pin and DSP process setting
Address: 59h

Bits	**R/W**	**Bit Mnemonic**	**Description**	**Default**
7	R/W	ADCMK_EXT	Using Ext I2S ADC MCLK 1'b1: use ; 1'b0: doesn't	1'b0
6	R/W	ADC_MKEN	Ext I2S ADC master clock output enable 1'b1: enable; 1'b0:disable Include pin: ADC_MCLK	1'b0
5	R/W	ADC_BLKEN	Ext I2S ADC clock output enable, 1'b1:enable; 1'b0:disable Include pins: ADC_BCLK+ADC_LRCK	1'b0
4	R/W	ADC_DSPEN	Ext I2S ADC data output enable for DSP process, 1'b1 : enable; 1'b0:disable Include pin: ADC_DOUT	1'b0
3	R/W	DACMK_EXT	Using Ext I2S DAC MCLK 1'b1: use ; 1'b0: doesn't	1'b0
2	R/W	DAC_MKEN	Ext I2S DAC master clock output enable 1'b1: enable; 1'b0:disable Include pin: DAC_MCLK	1'b0
1	R/W	DAC_BLKEN	Ext I2S DAC clock output enable, 1'b1: enable ; 1'b0: disable Include pins : DAC_BCLK+DAC_LRCK	1'b0
0	R/W	DAC_DOEN	Ext I2S DAC data output enable, 1'b1: enable ; 1'b0: disable Include pin : DAC_DOUT	1'b0

Record source + test setting
Address: 5ah

Bits	**R/W**	**Bit Mnemonic**	**Description**	**default**
7	R/W	STAND_ALONE	Enable this bit if treated RM5023 as a stand-alone device.	1'b0

6	R/W	MONOCH	ADC Mono channel	1'b0
5	R/W	SPEEDUP	Speed up the clock for simulation	1'b0
4	R/W	ENBLTWAV	Playback HW building sine wave	1'b0
3	R/W	ADCMON_EN	ADC→ SPDIFO monitor ch enable; 1'b1 : enabl	1'b0
2	R/W	SFTMUTEPS	Soft_mute_bypass; 1'b1= by pass	**1'b1**
1	R/W	MUTE_FC	~~Set this bit to 1 when spdif source has no copyright~~ Mute SPDIF In	1'b0
0	R/W	DIGREC	Set this bit to 1 when record source is from spdif	1'b0

Playback left channel volume control setting
Address: 5bh

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	da_mute_l	Mute left channel for playback	1'b0
6:0	R/W	da_gain_l	-62~+0dB, 1dB/Step	7'b0111100

Playback right channel volume control setting
Address: 5ch

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	da_mute_r	Mute right channel for playback	1'b0
6:0	R/W	da_gain_r	-62~+0dB, 1dB/Step	7'b0111100

da_gaina_l/da_gain_r volume control mapping table

Amplitude(dB)	Code	Amplitude(dB)	Code	Amplitude(dB)	Code
-60	0000000	-37	0010111	-14	0101110
-59	0000001	-36	0011000	-13	0101111
-58	0000010	-35	0011001	-12	0110000
-57	0000011	-34	0011010	-11	0110001
-56	0000100	-33	0011011	-10	0110010
-55	0000101	-32	0011100	-9	0110011
-54	0000110	-31	0011101	-8	0110100
-53	0000111	-30	0011110	-7	0110101
-52	0001000	-29	0011111	-6	0110110
-51	0001001	-28	0100000	-5	0110111
-50	0001010	-27	0100001	-4	0111000
-49	0001011	-26	0100010	-3	0111001
-48	0001100	-25	0100011	-2	0111010
-47	0001101	-24	0100100	-1	0111011
-46	0001110	-23	0100101	0	0111100
-45	0001111	-22	0100110	1	0111101
-44	0010000	-21	0100111	2	0111110
-43	0010001	-20	0101000	3	0111111
-42	0010010	-19	0101001	4	1000000
-41	0010011	-18	0101010	5	1000001
-40	0010100	-17	0101011	6	1000010
-39	0010101	-16	0101100		
-38	0010110	-15	0101101		

Record left channel volume control setting
Address: 5dh

Bits	R/W	Bit Mnemonic	Description	Default

7			Reserved	1'b0
6	R/W	ad_mute_l	Mute left channel for record	1'b0
5:0	R/W	ad_gain_l	-16~+12dB, 1dB/Step	6'b010000

Record right channel volume control setting
Address: 5eh

Bits	R/W	Bit Mnemonic	Description	Default
7			Reserved	1'b0
6	R/W	ad_mute_r	Mute right channel for record	1'b0
5:0	R/W	ad_gain_r	-16~+12dB, 1dB/Step	6'b010000

ad_gain_l/ad_gain_r volume control mapping table

Amplitude(dB)	Code	Amplitude(dB)	Code	Amplitude(dB)	Code
-16	000000	5	010101	26	101010
-15	000001	6	010110	27	101011
-14	000010	7	010111	28	101100
-13	000011	8	011000	29	101101
-12	000100	9	011001	30	101110
-11	000101	10	011010	31	101111
-10	000110	11	011011	32	110000
-9	000111	12	011100	33	110001
-8	001000	13	011101	34	110010
-7	001001	14	011110	35	110011
-6	001010	15	011111	36	110100
-5	001011	16	100000	37	110101
-4	001100	17	100001	38	110110
-3	001101	18	100010	39	110111
-2	001110	19	100011	40	111000
-1	001111	20	100100	41	111001
0	010000	21	100101	42	111010
1	010001	22	100110	43	111011
2	010010	23	100111	44	111100
3	010011	24	101000	45	111101
4	010100	25	101001		

VR scale read and AGC control path
Address: 5fh

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	AGC_CTRL_ANA	AGC volume control path 1: AGC control analog gain 0: AGC control digital gain	1'b1
6	R/W	GPIO_CLK24M	Output 24MHz clock to GPIO_10 pin, providing CM7000 working clock, This bit is invalid if GPIO_10 used to be AGC clipping LED output. 1'b1=output 24MHz enable	1'b0
5:0	RO	VR_OUT	VR volume response from analog	1'b0

SPDIF Function Control Register(1)
Address: 60h

Bits	R/W	Bit Mnemonic	Description	default

7	R/W	MUTE_SPDIFO	Mute SPDIF-Out	1'b0
6	R/W	LOCK_PAR	LOCK_INTR trigger level 0: low to high, 1: high to low	1'b0
5	R/W	SENSE_PAR	SENSE_INTR trigger level 0: low to high; 1: high to low	1'b0
4	R/W	IG_SPDV	SPDIF/IN valid bit detect enabled.	1'b0
3	R/W	RATE_MASK	1: RATE_INT is un-masked	1'b0
2	R/W	LOCK_MASK	1: LOCK_INT is un-masked	1'b0
1	R/W	SENSE_MASK	1: SENSE_INT is un-masked	1'b0
0	R/W	SPDFLOOP	internal SPDIF/IN loopback to SPDIF/OUT	1'b0

SPDIF Function Control Register(2)

Address: 61h

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	SPDI_COPY	Set to 1 if you want to enable copyright check function.	1'b0
6:5	R/W	SPDI_SMT	SPDIF input hysteresis 2'b00: 0 2'b01: 82mV(default) 2'b10: 153mV 2'b11: 282mV	2'b01
4	RO	rate_4844or96	Data sample rate (1: 96K 0: 44.1K or 48K). This bit is used in some device without correct sample frequency information (bit19:16)	1'b0
3	RO	VALID_IN	SPDIF-In Validity.	1'b0
2	R/W	SPDI_EN	enable SPDIF-In	1'b0
1	R/W	VALID	SPDIF-Out Validity.	1'b1
0	R/W	SPDO_EN	enable SPDIF-Out	1'b1

SPDIF IN Interrupt Status

Address: 62h

Bits	R/W	Bit Mnemonic	Description	default
7:6	R/W	SRC_NUM	01: one source number 00: Do not take into account	2'b0
5			Reserved	1'b0
4	RO	RATE_INT_	SPDIN smp rate change interrupt. Write 1 to clear	1'b0
3	RO	LOCK_INT_	Interrupt of SPDIN data is locked or not. Write 1 to clear	1'b0
2	RO	SENSE_INT_	Interrupt of SPDIN data is sensed or not. Write 1 to clear.	1'b0
1	RO	LOCK_STUS	indicate SPDIN data is locked or not	1'b0
0	RO	SENSE_STUS	indicate there is transition in SPDIN	1'b0

SPDIF Out Status Register(1)

Address: 63h

Bits	R/W	Bit Mnemonic	Description	default
7:6	R/W	LEN	11: indicates word length is 24 bits 10: indicates word length is 16 bits 00: Not indicated	2'b00
5:4	R/W	CHN_NUM	10: right channel for stereo channel format 01: left channel for stereo channel format	2'b00

			00: Do not take into account	
3	R/W	PRE	1: indicates filter pre-emphasis is 50/15us 0: indicates without pre-emphasis	1'b0
2	R/W	COPY	1: indicates no copyright is asserted 0: indicates copyright is asserted	1'b1
1	R/W	AUDIO	1: indicates data in Non-PCM Audio 0: indicates data is Linear PCM samples	1'b0
0	R/W	PRO	1: indicates Professional use 0: consumer use	1'b0

SPDIF Out Status Register(2)

Address: 64h

Bits	R/W	Bit Mnemonic	Description	default
7:0	R/W	CC[7:0]	Category Code; Programmed according to IEC standards	7'b0

SPDIF Out Status Register(3)

Address: 65h

Bits	R/W	Bit Mnemonic	Description	default
7:6	R/W	CGMS	Copy Generation Management System 00: copying is permitted without restriction	2'b00
5:4	R/W	ACC	Clock accuracy. 00: Level II	2'b00
3:0	R/W	OSF	Original sampling frequency. 0000: Not indicated	4'b0000

SPDIF In Status Register(1)

Address: 66h

Bits	R/W	Bit Mnemonic	Description	default
7-6	RO		Copy Generation Management System 00: copying is permitted without restriction	2'b0
5-4	RO		Clock accuracy. 00: Level II	2'b0
3	RO		1: indicates filter pre-emphasis is 50/15us 0: indicates without pre-emphasis	1'b0
2	RO		1: indicates no copyright is asserted 0: indicates copyright is asserted	1'b0
1	RO		1: indicates data in Non-PCM Audio 0: indicates data is Linear PCM samples	1'b0
0	RO		1: indicates Professional use 0: consumer use	1'b0

SPDIF In Status Register(2)

Address: 67h

Bits	R/W	Bit Mnemonic	Description	Default
7	RO		Programmed according to IEC standards	1'b0
6-0	RO		Category Code; Programmed according to IEC standards	7'b0

SPDIF In Status Register(3)

Address: 68h

Bits	R/W	Bit Mnemonic	Description	Default

7-4	RO		Original Sampling Frequency	4'b0000
3-0	RO		Sample Frequency 0000: 44.1KHz 0010: 48KHz 1000: 88.2KHz 1010: 96KHz 0001: Not indicated	4'b0000

SPDIF In Status Register(4)

Address: 69h

Bits	R/W	Bit Mnemonic	Description	Default
7-4	RO		Channel number	4'b0
3-0	RO		Source number	4'b0

UART RX Data Register

Address: 6ah

Bits	R/W	Bit Mnemonic	Description	Default
7-0	R/W	Pllcodecreg1a	UART RX Data Register	8'b0

UART TX Data Register

Address: 6bh

Bits	R/W	Bit Mnemonic	Description	Default
7-0	R/W	Pllcodecreg1b	UART TX Data Register	8'b0

Digital microphone setting

Address: 6ch

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	MASK_EQ_FS	Do not disable EQ function even if operated other than 44.1/48KHz. 1: EQ can support all sampling rate 0: EQ just support 44.1/48KHz	1'b0
6-3	R/W		Reserved	4'b0
2	R/W	DMICDIV2	Dig mic clock is 6.144M/2(48KHz) ; 5.6448M/2(44.1KHz)	1'b0
1	R/W	DMICDIV4	Dig mic clock is 6.144M/4(48KHz) ; 5.6448M/4(44.1KHz)	1'b0
0	R/W	DIGIMIC_EN	Digital microphone enable; 1'b1: enable; 1'b0 : disable	1'b0

PLL 98M offset monitor

Address: 6dh

Bits	R/W	Bit Mnemonic	Description	default
7-0	R	AOFF_P[7:0]	98.304MHz offset monitor	8'h80 (POR)

PLL 90M offset monitor

Address: 6eh

Bits	R/W	Bit Mnemonic	Description	default
7-0	R	AOFF_R[7:0]	90.3168MHz offset monitor	8'h10 (POR)

~~**PLL 96M offset monitor**~~

Address: 6fh

Bits	R/W	Bit Mnemonic	Description	default
~~7-0~~	~~R~~	~~AOFF_E[7:0]~~	~~96MHz offset monitor~~	~~8'hc4~~

EQ Register Description for Record

The contents of Register 70~77h are same as Register 40~47h

(master mode)I²C Slave Device Address and Read/Write Control Register (Power Reset)

Address: 0x80

Bits	R/W	Bit Mnemonic	Description	Default
7-1	R/W	SA_reg	The target slave device address.	0xA8(POR)
0	R/W	SA_reg	1: read, 0: write	1'b0(POR)

I²C Memory Address Pointer (MAP) of Slave Device (Power Reset)

Address: 0x81

Bits	R/W	Bit Mnemonic	Description	Default
7-0	R/W	MAP_reg	The register low byte address of salve device to be read or written.	8'b0(POR)

I²C Memory Address Pointer (MAP2) of Slave Device (Power Reset)

Address: 0x82

Bits	R/W	Bit Mnemonic	Description	Default
7-0	R/W	MAP2_reg	The register high byte address of salve device to be read or written.	8'b0(POR)

I²C Data Register (Power Reset)

Address: 0x83 ~ 0x92

Bits	R/W	Bit Mnemonic	Description	Default
7-0	R/W	data0~ data15	The data read from or written to the slave device.	8'b0(POR)

I²C Control and Status Register 0 (Power Reset)

Address: 0x93

Bits	R/W	Bit Mnemonic	Description	Default
7-0	R/W	i2c_ctrl_reg1	Data length of read/write command 8'h1: 1 byte, minimum length 8'h2: 2 bytes … 8'h7: 7 bytes 8'h10: 16 bytes, maximum length Others: Reserved	0x14 (POR)

I²C Control and Status Register 1 (Power Reset)

Address: 0x94

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	i2c_start	Trigger I2C read/write command 0->1: trigger I2C read/write command. 1->0: I2C interface had completed current	1'b0 (POR)

			task. 1 : I2C interface is idle and ready for work. 1 : I2C interface is running.	
6	R/W	i2c_reset	Reset I2C interface 0 : Not reset I2C interface 1 : Reset I2C interface	1'b0 (POR)
5	R/W	map_len	MAP length 0 : 8-bit MAP 1 : 16-bit MAP	1'b0 (POR)
4	R/W	clk_sync	Clock Synchronization 0: off 1: on, when slave pull-down SCLK, master would pause	1'b1 (POR)
3	R/W	fast_std	I2C speed mode 0 : Standard mode, 100kHz 1 : Fast mode, 400kHz	1'b0 (POR)
2	R/W	map_only	MAP only write command 0 : Write command. 1 : MAP only write command.	1'b0 (POR)
1	R/W	auto_rd	Auto read command 0 : Read command. 1 : Auto read command.	1'b1 (POR)
0	R	i2c_ctrl_reg2	Slave NACK error occur 2 : No error 3 : Slave NACK error occur	1'b0 (POR)

*Note: Write-MAP-Only: An operation which only writes the register MAP the salve device

I²C Download Control and Status (Power Reset)

Address: 0x95

Bits	/W	Bit Mnemonic	Description	Default
7	R/W	I2c_mas_sel	I2C master/slave select	1'b1 (POR)
6-4	R/W		Reserved	3'b000
3	RO	CHKSUM_ERR	Check sum Error 1. If in LD_PHASE, the check sum value was calculated by I2C load data. 2. If in CHK_PHASE, the check sum value was calculated by SRAM read content.	1'b0
2	RO	CHK_FINISH	CHECK phase done 1: finish download data CHECK	1'b0
1	R/W	CHK_PHASE	MCU select CHECK phase to read SRAM data for check-sum check. 1: enable (after disable LD_PHASE) 0: set 0 after complete	1'b0 (POR)
0	R/W	LD_PHASE	MCU select LOAD phase to access SRAM from download. 1: enable 0: set 0 after complete	1'b0 (POR)

I²C Clock Period Setting (Power Reset)

Address: 0x96

Bits	/W	Bit	Description	Default

		Mnemonic		
7	W	CHG_ENABLE	MCU can program I2C clock; 1'b1: enable	1'b0 (POR)
6	R/W		Reserved	1'b0
5-0	W	CHG_FREQ	Set I2C-master clock period. The clock period=83.3*5*(CHG_FREQ+1) Ex: CHG_FREQ = 6'd48 I2C Clock Period=83.3*5*(48+1)=20408ns HW limitation CHG_FREQ >= 6'h3	6'h0 (POR)

SPI I/F Registers Descriptions for Internal Control

SPI Data Register

Address: 98h~99h

Bits	R/W	Bit Mnemonic	Description	default
15-0	R/W	Data0/1	The data (which include address, r/w, and data bits) written to or read from the codec. The bits in this register should be interpreted according to the individual codec. The content of this register, after a write operation completes, has no meaning. The content of this register, after a read operation completes, should reference the document of individual codec to see how many bits in this register is valid.	0x0000 (POR)

SPI Control Register

Address: 9Ah

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	spi_start	Trigger SPI read/write command 0->1: trigger SPI read/write command. 1->0: SPI interface had completed current task. 4 : SPI interface is idle and ready for work. 1 : SPI interface is running.	1'b0 (POR)
6:3	R/W		Reserved	1'b0(POR)
2:1	R/W	frq_sel	SPI clock period 00: 330 ns 01: 980 ns 10: 1300 ns 11: 1600 ns (1.6 micro-second)	2'b0 (POR)
0	R/W	mst_int_en	SPI master interrupt enable 0: disable (default) 1: enable ~~(default)~~ Control HW to make master mode interrupt	1'b0 (POR)

*Note:

1. Bit [0]: When SPI interface is master mode, SPI interrupt happened when bit [0] ==1 and every SPI master command completed. Interrupt (HID) would be cleaned once address 0x10 was written.

IR Logical One Make and Space (USB Reset)

Address Offset: A0~A2h

Bits	R/W	Bit Mnemonic	Description	Default
23:16	R/W	Logical_One_Control_3	Bit[23]:Data Level 1T	8'h00

			1: data level is high to low (RC5/RC6) 0: data level is low to high (NEC) Bit[19:18]:Logical One 2T counter[9:8] Bit[17:16]:Logical One 1T counter[9:8] (RC5=0x80, RC6=0x80, NEC=0x00)	
15:8	R/W	Logical_One_Control_2	Logical One 2T counter[7:0] (RC5=0x16, RC6=0x0B, NEC=0x2A)	8'h2A
7:0	R/W	Logical_One_Control_1	Logical One 1T counter[7:0] (RC5=0x16, RC6=0x0B, NEC=0x0E) Default Condition: RC5 Device rising edge means logic-one 1T: 22*40u = 880usec 2T: 22*40u = 880usec	8'h0E

IR Logical Zero Make and Space (USB Reset)

Address Offset: A3~A5h

Bits	R/W	Bit Mnemonic	Description	Default
23:16	R/W	Logical_Zero_Control_3	Bit[19:18]:Logical Zero 2T counter[9:8] Bit[17:16]:Logical Zero 1T counter[9:8] (RC5=0x00, RC6=0x00, NEC=0x00)	8'h0
15:8	R/W	Logical_Zero_Control_2	Logical Zero 2T counter[7:0] (RC5=0x16, RC6=0x0B, NEC=0x0E)	8'h0E
7:0	R/W	Logical_Zero_Control_1	Logical Zero 1T counter[7:0] (RC5=0x16, RC6=0x0B, NEC=0x0E)	8'h0E

IR Header Code Make and Space (USB Reset)

Address Offset: A6~A8h

Bits	R/W	Bit Mnemonic	Description	Default
23:16	R/W	Header_Control_3	Bit[23]:header Level 1T 1: data level is high to low (RC5) 0: data level is low to high (NEC/RC6) Bit[21:20]: header period Set to 1 for RC6/NEC Set to 2 for RC5 Bit[19:18]:Header 2T counter[9:8] Bit[17:16]:Header 1T counter[9:8] (RC5=0x90, RC6=0x10, NEC=0x10)	8'h10
15:8	R/W	Header_Control_2	Header 2T counter[7:0] (RC5=0x16, RC6=0x16, NEC=0x70)	8'h70
7:0	R/W	Header_Control_1	Header 1T counter[7:0] (RC5=0x16, RC6=0x42, NEC=0xE1)	8'hE1

IR Repeat Code Make and Space (USB Reset)

Address Offset: A9~Abh

Bits	R/W	Bit Mnemonic	Description	Default
23:16	R/W	Repeat_Control_3	Bit[19:18]:Repeat control 2T counter[9:8] Bit[17:16]:Repeat control 1T counter[9:8] (RC5=--, RC6=--, NEC=0x00)	8'h0
15:8	R/W	Repeat_Control_2	Repeat control 2T counter[7:0] (RC5=--, RC6=--, NEC=0x38)	8'h38
7:0	R/W	Repeat_Control_1	Repeat control 1T counter[7:0] (RC5=--, RC6=--, NEC=0x00)	8'h00

IR_CTRL_0 (USB Reset)

Address Offset: Ach

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	Repeat_mask	1: Mask interrupt if repeat. 0: interrupt to MCU even if repeat.	1'b0
6	R/W	IR_Release	Release bit This bit is a write clear reg.	1'b0
5:0	R/W	Divider_N	Clock divider (Reference clock is 1MHz) Default working clock period is 40usec.	8'h28

IR_CTRL_1 (USB Reset)

Address Offset: Adh

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	DATA_Length[7]	1: rising phase detect means logic 1. (ex:RC5/RC6) 0: rising phase detect means logic 0. This bit is valid only if bit6 be set to 1.	1'b0
6	R/W	DATA_Length[6]	1: Bi-Phase coding (ex: RC5/RC6) 0: Pulse Distance coding (ex: NEC)	1'b0
5:0	R/W	DATA_Length[5:0]	Receiver Data Length (bits)	6'h20

IR_CTRL_2 (USB Reset)

Address Offset: Aeh

Bits	R/W	Bit Mnemonic	Description	Default
7:0	R/W	Tolerance	Tolerance range for determine data format is one or zero. [7:4]: data phase tolerance [3:0]: header phase tolerance	8'h55

IR Receiver Data Buffer

Address Offset: Afh~B2H

Bits	R/W	Bit Mnemonic	Description	Default
31:0	R	IR_Code	Receiver Data Buffer	32'h0

IR_RC6_CTRL (USB Reset)

Address Offset: B3h

Bits	R/W	Bit Mnemonic	Description	Default
7:6	R/W	Reserved		
5	RO	NEC_Rep	NEC Repeat status	1'b0
4	RO	RC6_Tgl	RC6 Toggle bit status	1'b0
3	R/W	RC6	RC6 Select	1'b0
2:0	RO	RC6_Mode	RC6 Mode bits	3'h0

USB phy power+debug

Address: B4h

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	IDNPDEN	When this pin is set to high, the internal DN pull-down resistor R3 (19.525 kΩ, ± 27%) is enabled.	1'b0 (POR)
6	R/W	IDPPDEN	When this pin is set to high, the internal DP pull-down resistor, R2 (19.525 kΩ ± 27%), is enabled.	1'b0 (POR)
5	R/W	IPUSW2EB	When this pin is set to low, the internal pull-up resistor R4 or R6 (1.02 kΩ, ± 48%) is disabled	1'b0 (POR)
4	R/W	EXT_USBPHY	Using external USB phy; 1'b1 : switch ext Philips usb phy 1'b0: using int 0.11um usb phy	1'b0 (POR)

3	R/W	SP	1'b1: operates at full speed; 1'b0: operates at low speed	1'b1 (POR)
2	R/W	USBPHY_MONT	Monitor Usb 1.1 phy all signal by GPIO25-32 pins 1'b1: monitor ; 1'b0 : disable	1'b0 (POR)
1	R/W	IPUSW1EB	When this pin is set to low, the internal pull-up resistor R1 or R5 (1.24 kΩ, ± 27%) is enabled Set "0" the internal pull-up R (1.24Kohm) is enabled ; MCU control this bit to pull-up R; default =1'b1 no pull-up R	1'b1 (POR)
0	R/W	EB(suspend)	RX enable(low active), RCV will drive to "0" when it goes high and enters a suspend mode; default = 1'b0 not suspend	1'b0 (POR)

Clock Switch for MCU
Address: B5h

Bits	R/W	Bit Mnemonic	Description	Default
7-5	R/W		Reserved	3'b0
4	R/W	CLKBYPASS	PLL stable clock filter disable 1'b1 : bypass CLK48M clock filter 1'b0: enable CLK48M clock filter Default : 1'b1	1'b1 (POR)
3	R/W	EXTBYPASS	Sub module reset extend 1'b1: bypass; only 1 T usbclk 1'b0 : extend > 1ms Default : 1'b1	1'b1 (POR)
2-0	R/W	MCUCLKSW	3'b100: 48Mhz 3'b011: 24Mhz 3'b010: 12Mhz 3'b001: 6Mhz 3'b000: 3Mhz Default : 6MHz	3'b010 ~~3'b001~~ (POR)

Module clock ctrl setting1
Address: B6h

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	SRAMCLK_G	Program SRAM CLK gated ctrl 1'b1 : gated	1'b1 (POR)
6	R/W	FIFOCLK_G	FIFO CLK gated ctrl 1'b1 : gated	1'b0 (POR)
5	R/W	RECCLK_G	Rec logic gated ctrl 1'b1 : gated	1'b0 (POR)
4	R/W	PLAYCLK_G	Play logic gated ctrl 1'b1 : gated	1'b0 (POR)
3	R/W	SPDOCLK_G	SPDIFOUT clock gated ctrl 1'b1 : gated	1'b0 (POR)
2	R/W	SPDICLK_G	SPDIFIN clock gated ctrl 1'b1 : gated	1'b0 (POR)
1	R/W	IRCLK_G	IR clock gated ctrl 1'b1 : gated	1'b0 (POR)
0	R/W	USBCLK_PRE_G	Peripheral USBCLK gated ctrl 1'b1 : gated	1'b0 (POR)

Module clock ctrl setting2
Address: B7h

Bits	R/W	Bit Mnemonic	Description	Default
7-4	R/W		Dummy bits	4'b0000
3	R/W	I2CMCLK_G	I2C-master clock gated ctrl 1'b1 : gated	1'b0 (POR)
2	R/W	I2CSCLK_G	I2C-slave clock gated ctrl 1'b1 : gated	1'b0 (POR)
1	R/W	SSPICLK_G	Internal SPI clock gated ctrl 1'b1 : gated	1'b0 (POR)
0	R/W	MSPICLK_G	External SPI clock gated ctrl 1'b1 : gated	1'b0 (POR)

Module Reset ctrl setting1
Address: B8h

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	FIFO_GRSTN	FIFO ctrl module reset ctrl 1'b1 : normal; 1'b0 : reset; 1T active (usbclk domain)	1'b1
6	R/W	IR_GRSTN	IR module reset ctrl 1'b1 : normal; 1'b0 : reset; 1T active (usbclk domain)	1'b1
5	R/W	REC_GRSTN	REC module reset ctrl 1'b1 : normal; 1'b0 : reset; 1T active (usbclk domain)	1'b1
4	R/W	PLAY_GRSTN	Play module reset ctrl 1'b1 : normal; 1'b0 : reset; 1T active (usbclk domain)	1'b1
3	R/W	I2C_GRSTN	I2C-master module reset ctrl 1'b1 : normal; 1'b0 : reset; 1T active (usbclk domain)	1'b1
2	R/W	SSPI_GRSTN	Internal SPI module reset ctrl 1'b1 : normal; 1'b0 : reset; 1T active (usbclk domain)	1'b1
1	R/W	MSPI_GRSTN	External SPI module reset ctrl 1'b1 : normal; 1'b0 : reset; 1T active (usbclk domain)	1'b1
0	R/W	SPDIF_GRSTN	SPDIF module reset ctrl 1'b1 : normal; 1'b0 : reset; 1T active (usbclk domain)	1'b1

IO DC test and PDSW
Address: B9h

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W		Reserved	1'b0(POR)
6	R/W	IO_CELL_VAL	IO cell value	1'b0(POR)
5	R/W	SW_IOCELL_DC	Switch IO cell control 1'b1: for DC character test 1'b0: use as normal function	1'b0 (POR)
4	R/W	PIN_PULLUP	1'b1 :all bi-direction PIN pull-up	1'b0(POR)
3	R/W	PIN_PULLDOWN	1'b1: all bi-direction PIN pull-down	1'b0(POR)
2	R/W	PIN_ALL_OUT	Under SW_IOCELL_DC=1'b1 1'b1: all bi-direction PIN as output 1'b0: all bi-direction PIN as input	1'b0(POR)
1	R/W	PDSW_P	Power down Peripheral component 1'b1: power down	1'b1 (POR)

			All GPIO[31:0] are changed as input mode	
0	R/W	GAINPASS	Mass product gain test pass 1'b1 : pass ; 1'b0: fail	1'b0 (POR)

CMA112_CODEC analog test and monitor pop noise signal

Address: Bah

Bits	R/W	Bit Mnemonic	Description	Default
7-3	R/W		Reserved	4'b0
3	R/W	MONT_POP	Monitor pop noise ctrl signal	1'b0(POR)
2	R/W	ADC_ASICOUT	ADC output D_LY, D_RY 1'b1 : output int D_LY/D_RY 1'b0: disable	1'b0 (POR)
1	R/W	ADC_FPGAIN	ADC filter input by FPGA 1'b1 : D_LY, D_RY from FPGA 1'b0: disable	1'b0 (POR)
0	R/W	DAC_DWA_TEST	DAC DWA test enable 1'b1 : enable ; 1'b0 : disable	1'b0 (POR)

GPIO IO Strength Setting

Address: BBh

Bits	R/W	Bit Mnemonic	Description	Default
7:6	R/W	GPIO_DRIVE3	GPIO25~32 IO strength setting	2'b01 (POR)
5:4	R/W	GPIO_DRIVE2	GPIO17~24 IO strength setting	2'b01 (POR)
3:2	R/W	GPIO_DRIVE1	GPIO9~16 IO strength setting	2'b01 (POR)
1:0	R/W	GPIO_DRIVE0	GPIO1~8 IO strength setting	2'b01 (POR)

Note : 2'b00=4mA, 2'b01=8mA, 2'b10=12mA, 2'b11=16mA

GPIO IO Strength Setting

Address: BCh

Bits	R/W	Bit Mnemonic	Description	Default
7:6	R/W	I2C_DRIVE	I2C IO strength setting 2'b00=2mA, 2'b01=4mA, 2'b10=6mA, 2'b11=8mA	2'b11 (POR)
5:4	R/W	SPI_DRIVE	SPI IO strength setting 2'b00=2mA, 2'b01=4mA,2'b10=6mA, 2'b11=8mA	2'b11 (POR)
3:2	R/W	SPDIF_DRIVE	SPDIFO IO strength setting 2'b00=2mA, 2'b01=4mA,2'b10=6mA, 2'b11=8mA	2'b11 (POR)
1:0	R/W	PDSW_DRIVE	PDSW IO strength setting 2'b00=2mA, 2'b01=4mA,2'b10=6mA, 2'b11=8mA	2'b11 (POR)

I2S IO Strength Setting

Address: BDh

Bits	R/W	Bit Mnemonic	Description	Default
7:5	R/W		Reserved	4'b0
3:2	R/W	I2SDA_DRIVE	I2S-DAC IO strength setting 2'b00=2mA, 2'b01=4mA,2'b10=6mA, 2'b11=8mA	2'b11 (POR)
1:0	R/W	I2SAD_DRIVE	I2S-ADC IO strength setting 2'b00=2mA, 2'b01=4mA,2'b10=6mA, 2'b11=8mA	2'b11 (POR)

PLL charge pump current ctrl

Address: BEh

Bits	R/W	Bit Mnemonic	Description	Default
7:4	R/W		Reserved	4'b0(POR)
3:0	R/W	B_PLL	I2S-ADC IO strength setting	4'b0(POR)

TESTMODE value and THD mode

Address Offset: 0xBFh

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W		Reserved	1'b0
6~4	R	CODECmode[2:0] Same as {GPIO_4,GPIO_3,GPIO_2}	Under Tmode = 3'b001; See analog test	3'b0
3	R	TESTMODE	TESTMODE; 1'b1: at testmode	1'b0
2-0	R	TMODE[2:0]	Enter which testmode	3'b0

GPO Data Register (Power Reset)

Address Offset: C0-C1h

Bits	R/W	Bit Mnemonic	Description	Default
15:0	R/W	GPO_0_reg GPO_1_reg	GPO data register which represents	16'h0 (POR)

GPI Data Register

Address Offset: C2-C3h

Bits	R/W	Bit Mnemonic	Description	Default
15:0	R		GPI data register which represents	16'h0 (POR)

GPIO Direction Control Register (Power Reset)

Address Offset: C4-C5h

Bits	R/W	Bit Mnemonic	Description	Default
15:0	R/W	GPOE_0 GPOE_1	GPIO output enable register which represents for pin XGPIO[15:0] 1: the corresponding pins are used as output 0: the corresponding pins are used as input	16'h0 (POR)

GPIO Interrupt Enable Mask Register (Power Reset)

Address Offset: C6-C7h

Bits	R/W	Bit Mnemonic	Description	Default
15:0	R/W	GPI_EN	GPIO_E, GPIO interrupt enable mask which represents for pins, XGPIO[15:0] 1: enable, 0: disable	16'h0 (POR)

GPIO De-bouncing Register (Power Reset)

Address Offset: C8-C9h

Default Value: 0000h (MSB -> LSB)

Bits	R/W	Bit Mnemonic	Description	Default
15:0	R/W	GPI_Deb	Enable the clock scale of mini-second (32	16'h0

			ms) for de-bouncing, default 1 1: enable, 0: disable	(POR)

General Control (Power Reset)
Address Offset: CAh

Bits	R/W	Bit Mnemonic	Description	default
7	R/W		Reserved	1'b0(POR)
6	R/W	General_Ctrl[6]	LED3 Control Selector (0: HW, 1: SW)	1'b0(POR)
5	R/W	General_Ctrl[5]	LED3 SW Output Enable	1'b0(POR)
4	R/W	General_Ctrl[4]	LED2 Control Selector (0: HW, 1: SW)	1'b0(POR)
3	R/W	General_Ctrl[3]	LED2 SW Output Enable	1'b0(POR)
2	R/W	General_Ctrl[2]	LED1 Control Selector (0: HW, 1: SW)	1'b0(POR)
1	R/W	General_Ctrl[1]	LED1 SW Output Enable	1'b0(POR)
0	R/W	General_Ctrl[0]	Buzzer Output Enable	1'b0(POR)

Buzzer Freq1 (Power Reset)
Address Offset: CBh

Bits	R/W	Bit Mnemonic	Description	default
7-0	R/W	Buzzer_Freq_1	Buzzer Output Frequency Counter 1 (Base On 23.44 KHz Clock)	8'h8 (POR)

Buzzer Duty1 (Power Reset)
Address Offset: 0xCCh

Bits	R/W	Bit Mnemonic	Description	default
7-0	R/W	Buzzer_Duty_1	Buzzer Output Duty Cycle Counter 1 (Base On 23.44 KHz Clock)	8'h4 (POR)

Buzzer Freq2 (Power Reset)
Address Offset: 0xCDh

Bits	R/W	Bit Mnemonic	Description	default
7-0	R/W	Buzzer_Freq_2	Buzzer Output Frequency Counter 2 (Base On 23.44 KHz Clock)	8'h4C (POR)

Buzzer Duty2 (Power Reset)
Address Offset: 0xCEh

Bits	R/W	Bit Mnemonic	Description	default
7-0	R/W	Buzzer_Duty_2	Buzzer Output Duty Cycle Counter 1 (Base On 23.44 KHz Clock)	8'h26 (POR)

Buzzer On Time (Power Reset)
Address Offset: 0xCFh

Bits	R/W	Bit Mnemonic	Description	Default
7-0	R/W	Buzzer_ON_Time	Buzzer Output ON Time	8'h50 (POR)

Buzzer Cycle Time (Power Reset)

Address Offset: 0XD0h

Bits	R/W	Bit Mnemonic	Description	Default
7-0	R/W	Buzzer_Cycle_Time	Buzzer Output ON Time	8'hC0 (POR)

LED Freq (Power Reset)

Address Offset: 0XD1h

Bits	R/W	Bit Mnemonic	Description	default
7-0	R/W	LED_Freq	LED1 Output Frequency	8'h17 (POR)

LED Duty (Power Reset)

Address Offset: 0Xd2h

Bits	R/W	Bit Mnemonic	Description	default
7-0	R/W	LED_Duty	LED1 Output Duty Cycle	8'h18 (POR)

LED1 On Time (Power Reset)

Address Offset: 0xD3h

Bits	R/W	Bit Mnemonic	Description	default
7-0	R/W	LED1_ON_Time	LED1 Output ON Time	8'h0c (POR)

LED1 Cycle Time (Power Reset)

Address Offset: 0xD4h

Bits	R/W	Bit Mnemonic	Description	default
7-0	R/W	LED1_Cycle_Time	LED1 Output Cycle Time Time unit is ~2.2msec 22msec * 24 = 528msec LED will ON-OFF 2 times per sec	8'h18 (POR)

LED2 On Time (Power Reset)

Address Offset: 0xD5h

Bits	R/W	Bit Mnemonic	Description	default
7-0	R/W	LED2_ON_Time	LED2 Output ON Time	8'h31 (POR)

LED2 Cycle Time (Power Reset)

Address Offset: 0xD6h

Bits	R/W	Bit Mnemonic	Description	default
7-0	R/W	LED2_Cycle_Time	LED2 Output Cycle Time	8'h30 (POR)

LED3 On Time (Power Reset)

Address Offset: 0xD7h

Bits	R/W	Bit Mnemonic	Description	default
7-0	R/W	LED3_ON_Time	LED3 Output ON Time	8'h18 (POR)

LED3 Cycle Time (Power Reset)

Address Offset: 0xD8h

Bits	R/W	Bit Mnemonic	Description	default
7-0	R/W	LED3_Cycle_Time	LED3 Output Cycle Time LED will ON-OFF 1 times per sec	8'h30 (POR)

Bounding Option

Address Offset: 0xD9h

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	URSTN_MASK	USB Reset Mask: If this bit set to 1, we will ignore USB reset from host.	2'b0 (POR)
6	R/W	SOF_SEL	SOF select: 0: SOF is coming from host command 1: SOF is coming from IR clock counter	2'b0 (POR)
5	R	SEL6	Pin SEL6	1'b0
4	R	SEL5	Pin SEL5	1'b0
3	R	SEL4	Pin SEL4	1'b0
2	R	SEL3	Pin SEL3	1'b0
1	R	SEL2	Pin SEL2	1'b0
0	R	SEL1	Pin SEL1	1'b0

GPO Switch Source (Power Reset)

Address Offset: 0xDAh

Bits	R/W	Bit Mnemonic	Description	default
7-4	R/W	GPO_SW0_H	4'h0:GPO[0]=gpo[0] 4'h1:GPO[0]=LED1 4'h2:GPO[0]=LED2 4'h3:GPO[0]=LED3 4'h4:GPO[0]=Buzzer Others: GPO[0]=1'b0	4'h0 (POR)
3-0	R/W	GPO_SW0_L	4'h0:GPO[1]=gpo[1] 4'h1:GPO[1]=LED1 4'h2:GPO[1]=LED2 4'h3:GPO[1]=LED3 4'h4:GPO[1]=Buzzer Others: GPO[1]=1'b0	4'h0 (POR)

Address Offset: 0xDBh

Bits	R/W	Bit Mnemonic	Description	default
7-4	R/W	GPO_SW1_H	4'h0:GPO[2]=gpo[2] 4'h1:GPO[2]=LED1 4'h2:GPO[2]=LED2 4'h3:GPO[2]=LED3 4'h4:GPO[2]=Buzzer Others: GPO[2]=1'b0	4'h0 (POR)
3-0	R/W	GPO_SW1_L	4'h0:GPO[3]=gpo[3] 4'h1:GPO[3]=LED1 4'h2:GPO[3]=LED2 4'h3:GPO[3]=LED3 4'h4:GPO[3]=Buzzer Others: GPO[3]=1'b0	4'h0 (POR)

Address Offset: 0xDCh

Bits	R/W	Bit Mnemonic	Description	default
7-4	R/W	GPO_SW2_H	4'h0:GPO[4]=gpo[4] 4'h1:GPO[4]=LED1 4'h2:GPO[4]=LED2 4'h3:GPO[4]=LED3 4'h4:GPO[4]=Buzzer Others: GPO[4]=1'b0	4'h0 (POR)
3-0	R/W	GPO_SW2_L	4'h0:GPO[5]=gpo[5] 4'h1:GPO[5]=LED1 4'h2:GPO[5]=LED2 4'h3:GPO[5]=LED3 4'h4:GPO[5]=Buzzer Others: GPO[5]=1'b0	4'h0 (POR)

Address Offset: 0xDDh

Bits	R/W	Bit Mnemonic	Description	default
7-4	R/W	GPO_SW3_H	4'h0:GPO[6]=gpo[6] 4'h1:GPO[6]=LED1 4'h2:GPO[6]=LED2 4'h3:GPO[6]=LED3 4'h4:GPO[6]=Buzzer Others: GPO[6]=1'b0	4'h0 (POR)
3-0	R/W	GPO_SW3_L	4'h0:GPO[7]=gpo[7] 4'h1:GPO[7]=LED1 4'h2:GPO[7]=LED2 4'h3:GPO[7]=LED3 4'h4:GPO[7]=Buzzer Others: GPO[7]=1'b0	4'h0 (POR)

Address Offset: 0xDEh

Bits	R/W	Bit Mnemonic	Description	default
7-4	R/W	GPO_SW4_H	4'h0:GPO[8]=gpo[8] 4'h1:GPO[8]=LED1 4'h2:GPO[8]=LED2 4'h3:GPO[8]=LED3 4'h4:GPO[8]=Buzzer Others: GPO[8]=1'b0	4'h0 (POR)
3-0	R/W	GPO_SW4_L	4'h0:GPO[9]=gpo[9] 4'h1:GPO[9]=LED1 4'h2:GPO[9]=LED2 4'h3:GPO[9]=LED3 4'h4:GPO[9]=Buzzer Others: GPO[9]=1'b0	4'h0 (POR)

Address Offset: 0xDFh

Bits	R/W	Bit Mnemonic	Description	default
7-4	R/W	GPO_SW5_H	4'h0:GPO[10]=gpo[10] 4'h1:GPO[10]=LED1 4'h2:GPO[10]=LED2 4'h3:GPO[10]=LED3 4'h4:GPO[10]=Buzzer Others: GPO[10]=1'b0	4'h0 (POR)

3-0	R/W	GPO_SW5_L	4'h0:GPO[11]=gpo[11] 4'h1:GPO[11]=LED1 4'h2:GPO[11]=LED2 4'h3:GPO[11]=LED3 4'h4:GPO[11]=Buzzer Others: GPO[11]=1'b0	4'h0 (POR)

Address Offset: 0XE0h

Bits	R/W	Bit Mnemonic	Description	default
7-4	R/W	GPO_SW6_H	4'h0:GPO[12]=gpo[12] 4'h1:GPO[12]=LED1 4'h2:GPO[12]=LED2 4'h3:GPO[12]=LED3 4'h4:GPO[12]=Buzzer Others: GPO[12]=1'b0	4'h0 (POR)
3-0	R/W	GPO_SW6_L	4'h0:GPO[13]=gpo[13] 4'h1:GPO[13]=LED1 4'h2:GPO[13]=LED2 4'h3:GPO[13]=LED3 4'h4:GPO[13]=Buzzer Others: GPO[13]=1'b0	4'h0 (POR)

Address Offset: 0XE1h

Bits	R/W	Bit Mnemonic	Description	default
7-4	R/W	GPO_SW7_H	4'h0:GPO[14]=gpo[14] 4'h1:GPO[14]=LED1 4'h2:GPO[14]=LED2 4'h3:GPO[14]=LED3 4'h4:GPO[14]=Buzzer Others: GPO[14]=1'b0	4'h0 (POR)
3-0	R/W	GPO_SW7_L	4'h0:GPO[15]=gpo[15] 4'h1:GPO[15]=LED1 4'h2:GPO[15]=LED2 4'h3:GPO[15]=LED3 4'h4:GPO[15]=Buzzer Others: GPO[15]=1'b0	4'h0 (POR)

GPI Remote Choose

Address Offset: 0xE2~E3h

Bits	R/W	Bit Mnemonic	Description	default
15:0	R/W	GPI_RWL GPI_RWH	D0==1'b1:GPI[0] remote wake up enable D1==1'b1:GPI[1] remote wake up enable D2==1'b1:GPI[2] remote wake up enable D3==1'b1:GPI[3] remote wake up enable D4==1'b1:GPI[4] remote wake up enable D5==1'b1:GPI[5] remote wake up enable D6==1'b1:GPI[6]	16'h0 (POR)

			remote wake up enable D7==1'b1:GPI[7] remote wake up enable D8==1'b1:GPI[8] remote wake up enable D9==1'b1:GPI[9] remote wake up enable D10==1'b1:GPI[10] remote wake up enable D11==1'b1:GPI[11] remote wake up enable D12==1'b1:GPI[12] remote wake up enable D13==1'b1:GPI[13] remote wake up enable D14==1'b1:GPI[14] remote wake up enable D15==1'b1:GPI[15] remote wake up enable	

GPIO pull-up/down Control Register0

Address Offset: 0xE4

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	GPIO_PD0[7]	GPIO_1 ~ GPIO_7 pad control 1'b1:75k pull down; 1'b0 : 75k pull up	1'b1 (POR)
6	R/W	GPIO_PD0[6]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
5	R/W	GPIO_PD0[5]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
4	R/W	GPIO_PD0[4]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
3	R/W	GPIO_PD0[3]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
2	R/W	GPIO_PD0[2]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
1	R/W	GPIO_PD0[1]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
0	R/W	GPIO_PD0[0]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)

GPIO pull-up/down Control Register1

Address Offset: 0xE5

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	GPIO_PD1[7]	GPIO_8~GPIO_16 pad control 1'b1:75k pull down; 1'b0 : 75k pull up	1'b1 (POR)
6	R/W	GPIO_PD1[6]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
5	R/W	GPIO_PD1[5]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
4	R/W	GPIO_PD1[4]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
3	R/W	GPIO_PD1[3]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
2	R/W	GPIO_PD1[2]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
1	R/W	GPIO_PD1[1]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
0	R/W	GPIO_PD1[0]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)

GPIO pull-up/down Control Register2

Address Offset: 0xE6

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	GPIO_PD2[7]	GPIO17~GPIO24 pad control 1'b1:75k pull down; 1'b0 : 75k pull up	1'b1 (POR)

6	R/W	GPIO_PD2[6]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
5	R/W	GPIO_PD2[5]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
4	R/W	GPIO_PD2[4]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
3	R/W	GPIO_PD2[3]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
2	R/W	GPIO_PD2[2]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
1	R/W	GPIO_PD2[1]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
0	R/W	GPIO_PD2[0]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)

GPIO pull-up/down Control Register3

Address Offset: 0xE7

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	GPIO_PD3[7]	GPIO25~GPIO32 pad control 1'b1:75k pull down; 1'b0 : 75k pull up	1'b1 (POR)
6	R/W	GPIO_PD3[6]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
5	R/W	GPIO_PD3[5]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
4	R/W	GPIO_PD3[4]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
3	R/W	GPIO_PD3[3]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
2	R/W	GPIO_PD3[2]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
1	R/W	GPIO_PD3[1]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)
0	R/W	GPIO_PD3[0]	1'b1:75k pull down; 1'b0 : 75k pull up	1'b1(POR)

Share MCU port0

Address Offset: 0xE8

Bits	R/W	Bit Mnemonic	Description	Default
7-2	R/W		reserved	6'b0
1	R/W	SH_UART	Shared with {GPIO_17,GPIO_18} = {MCU_RXD, MCU_TRX}	1'b0 (POR)
0	R/W	SH_GPIO_P[0]	GPIO_8~GPIO_16 pins shared for Mcu port0	1'b0 (POR)

AGC Global Control Register

Address: 0xf0

Bits	R/W	Description	Default
7	R/W	AGC_PRE_EN: Enable AGC function even if Host didn't send ISO-In packet.	0x0
6	R/W	Gain increase enable, else Gain decrease Gain increase means that the real gain value increased follow by the numeric of gain increased.	0x0
5	R/W	AGC Left channel ~~close~~ enable	0x0
4	R/W	AGC Right channel ~~close~~ enable	0x0
3	R/W	Reserved	0x0
2-0	R/W	Each increase GAIN Step	0x1

AGC ATTACK TIME CONTROL

Address: 0xf1

Bits	R/W	Description	Default
7-6	R/W	Reserved	0x00
5-0	R/W	AGC Attack time, time increases by 43us with every step, 6'h03 default 0.129ms	0x03

AGC RELEASE TIME CONTROL

Address: 0xf2

Bits	R/W	Description	Default
7-6	R/W	Reserved	0x00

5-0	R/W	AGC Release time, time increases by 22ms with every step, 6'h03 default 66ms	0x03

AGC HOLD TIME CONTROL

Address: 0xf3

Bits	R/W	Description	Default
7-6	R/W	Reserved	0x00
5-0	R/W	AGC Hold time, time increases by 22ms with every step, 6'h0C default 264ms	0x0c

AGC Threshold Control Register

Address: 0xf4~f6

Bits	R/W	Description	Default
7-0	R/W	Max Threshold of PCM unit. It will clip the output value equal as the threshold if estimated value exceeded. {PCM 7FFFFF * -3dB(0.708)} =~ 24'h5A9FBD {PCM 7FFFFF * -1dB(0.981)} =~ 24'h721483	0x721483

AGC FIXED GAIN CONTROL

Address: 0xf7

Bits	R/W	Description	Default
7-6	R/W	Pre Max Threshold add dB unit default add 1dB (0~3dB)	0x1
5-0	R/W	Set the fixed gain of amplifier: two's compliment dB unit The maximum range of AGC adjustment. By default, if AGC enable, the fixed gain will be added in original gain value. F0[6]=1 means default increase fixed gain when AGC enable. F0[6]=1 means default decrease fixed gain.	0x9

AGC Simulate CONTROL

Address: 0xf8

Bits	R/W	Description	Default
7	R/W	TTEST enable for simulation 1: enable 0: disable	0x0
6-5	R/W	Reserved	0x0
4	R/W	Volume overflow output enable 1: enable 0: disable Don't care AGC function.	0x0
3-0	R/W	Reserved	0x0

AGC GAIN MAX Limit

Address: 0xf9

Bits	R/W	Description	Default
7-6	R/W	Reserved	0x0
5-0	R/W	ADC gain maximum limit form MCU Setting Default: ~~20dB~~ 30dB (0x30 invert = 0x0F = 30dB for Analog)	~~0x24~~ 0x30

AGC GAIN MIN Limit

Address: 0xfa

Bits	R/W	Description	Default
7-6	R/W	Reserved	0x0
5-0	R/W	ADC gain minimum limit form MCU Setting Default: ~~-6dB~~ 0dB (0x12 invert = 0x2D = 0dB for Analog)	~~0x0a~~ 0x12

Clipping LED Timing Control I

Address: 0xfb

Bits	R/W	Description	Default
7-4	R/W	LED turn off time by time unit reference 0xf8[5:4]	0x4

		default 4 * 64ms(time unit) = 256 ms	
3-0	R/W	LED turn on time by time unit reference 0xf8[5:4] default 2 * 64ms(time unit) = 128 ms	0x2

Clipping LED Timing Control II

Address: 0xfc

Bits	R/W	Description	Default
7	R/W	Breathing Light function enable 1:enable ; 0:disable	0x0
6	R/W	Reserved	0x0
5-4	R/W	1. If Breathing Light disable, it means LED trun time unit 11:256, 10:128, 01:64, 00:32 ms 2. If enable, it means breathing light unit when over. 11:2.8sec, 10:1.4sec, 01:0.7sec, 00:0.35sec	0x0
3-0	R/W	LED total work time by 0.5s with every step Once the clipping LED be triggered, it will keep On-Off during total work time.	0x4

Start Address of Input Register Data

Address: 0xfe

Bits	R/W	Description	Default
7-0	R/W	Starting Address of HID Interrupt In and HID Get Report , MSB part	0x00 (POR)

Address: 0xff

Bits	R/W	Description	Default
7-0	R/W	Starting Address of HID Interrupt In and HID Get Report	0x00 (POR)

4.18.2 internal CMA112 register description:

I²S Decoder Configuration Registers

Address Offset: 00h

Default Value: 92h (MSB -> LSB) (POR)

Bit	Attribute	Description
7:6	R/W	I2S PCM Resolution 00: 16-bit 01: 20-bit 10: 24-bit (default) 11: 32-bit (only valid when BCLK/LRCK = 128 or 256)
5:4	R/W	Reserved
3	R/W	**Data Format** 0 : I2S Mode (default) 1 : Left Justified Mode ~~(default)~~
2:0	R/W	Reserved

Address Offset: 01h

Default Value: 80h (MSB -> LSB) (POR)

Bit	Attribute	Description
7:5	R/W	Reserved
4	R/W	Reserved
3	R/W	Reserved
2:1	R/W	BCLK/LRCK Ratio, how many BCLK cycles in one LRCK cycle DACR[1:0] 00 : 64 (default) 01 : 128 10 : 256 (only valid when MCLK/LRCK = 256 or 512) 11 : Reserved
0	R/W	Reserved

I²S Encoder Configuration Registers

Address Offset: 02h

Default Value: 92h (MSB -> LSB) (POR)

Bit	Attribute	Description
7:6	R/W	I2S PCM Resolution 00: 16-bit 01: 20-bit 10: 24-bit (default) 11: 32-bit (only valid when BCLK/LRCK = 128 or 256)
5:4	R/W	Reserved
3	R/W	**Data Format** 0 : I2S Mode (default) 1 : Left Justified Mode ~~(default)~~
2:0	R/W	Reserved

Address Offset: 03h

Default Value: 80h (MSB -> LSB) (POR)

Bit	Attribute	Description
7:5	R/W	Reserved
4	R/W	
3	R/W	

2:1	R/W	BCLK/LRCK Ratio, how many BCLK cycles in one LRCK cycle DACR[1:0] 00 : 64 (default) 01 : 128 10 : 256 (only valid when MCLK/LRCK = 256 or 512) 11 : Reserved
0	R/W	Reserved

Digital Codec Control Registers

Address Offset: 04h
Default Value: 40h (MSB -> LSB) (POR)

Bit	Attribute	Description
7	R/W	Reserved
6	R/W	**AD_HPF_EN,** 1: enable adc high pass filter, 0: disable adc high pass filter , default:1
5.	R/W	**DA_HPF_EN,** 1: enable dac high pass filter, 0: disable dac high pass filter , default:0
4	R/W	**DA_192K_EN**: set sampling rate of DAC path is 192K. Default: 0
3	R/W	**DA_96K_EN**: set sampling rate of DAC path is 96K. Default: 0
2	R/W	**AD_192K_EN:** set sampling rate of ADC path is 192K. Default: 0
1	R/W	**AD_96K_EN**: set sampling rate of ADC path is 96K. Default: 0
0	R/W	**TEST_MODE**: enable DA-AD internal loop. Default: 0

Address Offset: 05h
Default Value: 00h (MSB -> LSB) (POR)

Bit	Attribute	Description
7	R/W	**zc_en**: zero cross. Default: 0
6:2	R/W	Reserved
1	R/W	**mute_p_r**: mute Right channel in digital part. Default: 0
0	R/W	**mute_p_l:** mute Left channel in digital part. Default: 0

Analog Codec Control Registers

Address Offset: 06h
Default Value: 00h (MSB -> LSB) (POR)

Bit	Attribute	Description
7	RO	**D_OVR2D75**: VR status when XVOLADJ input voltage over 2.75v
6	R/W	**SVR_EN**: Default: 0
5:0	R/W	**SVRVOL**: Analog VR volume control(-1dB/step) 000000:-0.02dB 111110:-73dB 111111:mute Default: <000000> -0.02 dB

Address Offset: 07h
Default Value: 0Ch (MSB -> LSB) (POR)

Bit	Attribute	Description
7:4	R/W	Reserved
3	R/W	**VMICAM**: Mute Micro_in Left/Right path At mixer. Default:1
2	R/W	**VLNIAM~~L~~**: Mute Line_in Left/Right path At mixer. Default:1
~~1~~	~~R/W~~	~~**VMICM**: Micro_in Mute. Default:1~~

~~0~~	~~R/W~~	~~**VLNIM**: Line_in Mute. Default:1~~

Address Offset: 08h
Default Value: 1Ch (MSB -> LSB) (POR)

Bit	Attribute	Description
7:6	R/W	Reserved
5:0	R/W	**VMICL<5:0>**: Micro_in volume control(-1dB/step) <010000>:32dB <111110>:-14dB <111111>:Mute Default**:** <011100> 20dB

Address Offset: 09h
Default Value: 1Ch (MSB -> LSB) (POR)

Bit	Attribute	Description
7:6	R/W	Reserved
5:0	R/W	**VMICR<5:0>**: Micro_in volume control(-1dB/step) <010000>:32dB <111110>:-14dB <111111>:Mute Default**:** <011100> 20dB

Address Offset: 0Ah
Default Value: 21h (MSB -> LSB) (POR)

Bit	Attribute	Description
7:6	R/W	Reserved
5:0	R/W	**VLNIL<5:0>**: Line_in volume control(-1dB/step) <010101>:12dB <111110>:-29dB <111111>:Mute Default**:** <100001> 0dB

Address Offset: 0Bh
Default Value: 21h (MSB -> LSB) (POR)

Bit	Attribute	Description
7:6	R/W	Reserved
5:0	R/W	**VLNIR<5:0>**: Line_in volume control(-1dB/step) <010101>:12dB <111110>:-29dB <111111>:Mute Default**:** <100001> 0dB

Address Offset: 0Ch
Default Value: 00h (MSB -> LSB) (POR)

Bit	Attribute	Description
7:1	R/W	Reserved
0	R/W	**VDAM**: Mute DAC analog Left/Right path At mixer. Default: 0

Address Offset: 0Dh
Default Value: 00h (MSB -> LSB) (POR)

Bit	Attribute	
7:6	R/W	Reserved
5:0	R/W	**VML<5:0>**: Mast volume control(-1dB/step) 000000: 0 dB 111110: -62dB 111111:mute Default**:** <000000>0 dB

Address Offset: 0Eh
Default Value: 00h (MSB -> LSB) (POR)

Bit	Attribute	Description
7:6	R/W	Reserved
5:0	R/W	**VMR<5:0>**: Mast volume control(-1dB/step) 000000: 0 dB 111110: -62dB 111111:mute Default**:** <000000>0 dB

Address Offset: 0Fh
Default Value: 3Fh (MSB -> LSB) (POR)

Bit	Attribute	Description
7	R/W	Reserved
6	R/W	**VADM**: Mute Recording. Default: 0
5	R/W	**EN_AA**: Enable power at Micro_in and Line_in monitor A_A path. Default: 1
4	R/W	**EN_DA**: Enable Power at Playback path. Default: 1
3	R/W	**VMASTM**: MUTE playback volume. Default:1
2	R/W	**EN_AD**: Enable total ADC path. Default: 1
1	R/W	**EN_VBG**: Enable Power at Bandgap and Current reference block. Default: 1
0	R/W	**EN_VAG**: Enable OP common refence source. Default: 1

Address Offset: 10h
Default Value: 02h (MSB -> LSB) (POR)

Bit	Attribute	Description
7:6	R/W	**ADSEL<1:0>**: To select ADC left/Right channel input path 00: Line_in 01:A_A path and DAC Mixer path 10:Micro_in 11: A_A Path mixer Default:00
5	R/W	**ENL_ACREF**: To enable (low) the reference point from board in the recording gain stage.
~~5~~	~~R/W~~	~~**EN_DIFF**: Enable Micro_in using instrument amplifier structure At this mode, to disable micro_in digital gain. Default: 0~~
~~4:0~~	~~R/W~~	~~**VADL_DIF<4:0>**: Recording volume controle(1.5 dB/step) For micro_in Instrument differential amplifier with EN_DIFF=H. <00000> : 51.01dB ; <11111>:7.49dB Default:<01111> 28.68dB~~
4:2		**Reserved**
1	R/W	**EN_XLOCOM**: Enable the power of Driver XLOCOM Default: 1
0	R/W	**MONO_EN**: Enable the MONO IN/OUT in AA path Default: 0

Address Offset: 11h
Default Value: 21h (MSB -> LSB) (POR)

Bit	Attribute	Description
7:6	R/W	Reserved
5:0	R/W	**VADL<5:0>**: Recording volume control (-1 dB/step) If ADSEL = 00 or 01 Default: <100001> 0 dB If ADSEL = 10 or 11 Default: <011001> 20 dB

Address Offset: 12h
Default Value: 21h (MSB -> LSB) (POR)

Bit	Attribute	Description
7:6	R/W	Reserved
5:0	R/W	**VADR<5:0>**: Recording volume control (-1 dB/step) If ADSEL = 00 or 01 Default: <100001> 0 dB If ADSEL = 10 or 11 Default: <011001> 20 dB

Address Offset: 13h
Default Value: 1Dh (MSB -> LSB) (POR)

Bit	Attribute	Description
7:5	R/W	Reserved
4	R/W	**CLAMP**: To enable adc input signal amplitude limiter. Default:1
3	R/W	**DAIN_SEL**: To select DAC analog filter from DACMOD. Default:1
2	R/W	**QA**: To enable Line driver at saving power mode. Default:1
1	R/W	**TMOD**: To enable ADC recording path from XMICL/R and XLNIL/R PAD. Default: 0
0	R/W	**VREF_SEL**: To select internal reference source from Bandgap. Default:1

Address Offset: 14h
Default Value: 10h (MSB -> LSB) (POR)

Bit	Attribute	Description
7:6	R/W	Reserved
5:4	R/W	**SEL_TVH** : Select DC voltage to XMICL/R and XLNIL/R path at test mode When SEL_TVH<1:0>=1x, the DC voltage is 2.8V at test mode. When SEL_TVH<1:0>=01, the DC voltage is 1.71875V at test mode. When SEL_TVH<1:0>=00, the DC voltage is 0.7V at test mode.
3	R/W	Reserved
2	R/W	**TST_AD_IN**: Enable to test Recording Volume step. Default: 0
1	R/W	**EN_VTST**: Enable DC voltage input to XMICL/R and XLNIL/R path at test mode. Default: 0
~~0~~	~~R/W~~	~~**SEL_TVH** : Select DC voltage to XMICL/R and XLNIL/R path at test mode~~ ~~H : To select 1.72V~~ ~~L : To select 1.05V~~ ~~Default:1~~

IO pad Control Registers

Address Offset: 15h
Default Value: 02h (MSB -> LSB) (POR)

Bit	Attribute	Description
7:3	R/W	Reserved
2:0	R/W	**IO_DRIVE**, IO pad driving capability, default : 3'b010

Debug Mode Control Registers (for digital codec)

Digital dafilter

Address Offset: 16h
Default Value: 00h (MSB -> LSB) (POR)

Bit	Attribute	Description
7	R/W	Reserved

6	R/W	Reserved
5	R/W	1: Monitor left channel DAC output, default: 0
4	R/W	1: Monitor right channel DAC output, default: 0
3	R/W	1: Monitor left channel sigma delta modulator input, default: 0
2	R/W	1: Monitor right channel sigma delta modulator input, default: 0
1	R/W	1: Monitor left channel DAC input, default: 0
0	R/W	1: Monitor right channel DAC input, default: 0

Digital adfilter

Address Offset: 17h

Default Value: 00h (MSB -> LSB) (POR)

Bit	Attribute	Description
7	R/W	Reserved
6	R/W	Reserved
5	R/W	Reserved
4	R/W	Reserved
3	R/W	Reserved
2	R/W	1: Monitor left channel ADC output, default: 0
1	R/W	1: Monitor right channel ADC output, default: 0
0	R/W	1: Monitor left & right channel ADC input, default: 0

Resolve glitch from dac_mclk & adc_mclk

Address Offset: 18h

Default Value: 00h (MSB -> LSB) (POR)

Bit	Attribute	Description
7:2	R/W	Reserved
1	R/W	**DAC_GLITCH_RESET**: pull reset of 16 cycles period for DAC codec. Default: 0.
0	R/W	**ADC_GLITCH_RESET**: pull reset of 16 cycles period for ADC codec. Default: 0.

Digital Codec Gain Selection

Address Offset: 19h

Default Value: 00h (MSB -> LSB) (POR)

Bit	Attribute	Description
7	R/W	Reserved
6:4	R/W	Coefficient of ADC_HPF for lower band edge. $1-z^{-1} / 1-z^{-1}+coefficient*z^{-1}$ 3'b001 :2^-9, -1.85dB 3'b010 :2^-11, -0.156dB 3'b100 :2^-12, -0.05dB Others :2^-10, -0.54dB
3:2	R/W	**DAC_GAIN_SEL**: select digital dac gain degree. 00 : 1.92 01 : 1.92*0.99 10 : 1.92*0.98 11 : 1.92*0.97 Default: 00.
1:0	R/W	**ADC_GAIN_SEL**: select digital adc gain degree. 00 : 1.40625 01 : 1.40625*0.99 10 : 1.40625*0.98 11 : 1.40625*0.97 Default: 00.

Part 2 of Analog Codec Control Registers

Address Offset: 1Ah
Default Value: 0Fh (MSB -> LSB) (POR)

Bit	Attribute	Description
7:5	R/W	Reserved
~~4:0~~	~~R/W~~	~~**VADR_DIF<4:0>**: Recording volume controle(1.5 dB/step)~~ ~~For micro_in Instrument differential amplifier with EN_DIFF=H.~~ ~~<00000> : 51.01dB ; <11111>:7.49dB~~ ~~Default:<01111> 28.68dB~~

Control the Bias Current

Address Offset: 1Bh
Default Value: 00h (MSB -> LSB) (POR)

Bit	Attribute	Description
7:4	R/W	Reserved
3:0	R/W	**IREF_TEST<3:0>:** IREF_TEST<1:0>:to control the bias current for opamp in adc,dac. IREF_TEST<3:2>:to control the bias current for vag buffer. Default=0000

Reverse Clock Phase to Analog Part

Address Offset: 1Ch
Default Value: 00h (MSB -> LSB) (POR)

Bit	Attribute	Description
7:2	R/W	Reserved
1	R/W	1: Reverse CLKDA phase to analog part. Default : 0
0	R/W	1: Reverse CLKAD phase to analog part. Default : 0

MBIST

Address Offset: **1E**h
Default Value: 00h (MSB -> LSB) (POR)

Bit	Attribute	Description
7:4	R/W	Reserved
3	RO	**BIST_Finish:** Selected memory BIST done without any error 0:uncomplete 1:completed successfully
2	RO	**BIST_Fail:** Selected memory BIST Fail, defect occurred in memory 0:n/a 1:BIST fail
1	R/W	**ADMODE:** ADC or DAC memory selected for BIST mode 0: DAC memory 1:ADC memory default:0
0	R/W	**BISTMODE:** Memory BIST mode enable, default: 0

6.4 gain table

(1)LNI VOL /DAC VOL (REC PATH)

In REC Path, when LNI or DAC path is chosen, VADL(R) <5:0>'s gain is as following table.					
VADL<5:3>	**VADL<2:0>**	Ri (kΩ)	Gain1(dB)	Gain2(dB)	**Total Gain(dB)**

VADR<5:3>	VADR<2:0>				
111	**111**	44.774	-30.00	0	**-30.00**
111	**110**	39.905	-29.00	0	**-29.00**
111	**101**	35.566	-28.00	0	**-28.00**
111	**100**	31.698	-27.00	0	**-27.00**
111	**011**	28.251	-26.00	0	**-26.00**
111	**010**	25.179	-25.00	0	**-25.00**
111	**001**	22.440	-24.00	0	**-24.00**
111	**000**	20.000	-23.00	0	**-23.00**
110	**111**	44.774	-22.00	0	**-22.00**
110	**110**	39.905	-21.00	0	**-21.00**
110	**101**	35.566	-20.00	0	**-20.00**
110	**100**	31.698	-19.00	0	**-19.00**
110	**011**	28.251	-18.00	0	**-18.00**
110	**010**	25.179	-17.00	0	**-17.00**
110	**001**	22.440	-16.00	0	**-16.00**
110	**000**	20.000	-15.00	0	**-15.00**
101	**111**	44.774	-14.00	0	**-14.00**
101	**110**	39.905	-13.00	0	**-13.00**
101	**101**	35.566	-12.00	0	**-12.00**
101	**100**	31.698	-11.00	0	**-11.00**
101	**011**	28.251	-10.00	0	**-10.00**
101	**010**	25.179	-9.00	0	**-9.00**
101	**001**	22.440	-8.00	0	**-8.00**
101	**000**	20.000	-7.00	0	**-7.00**
100	**111**	44.774	-6.00	0	**-6.00**
100	**110**	39.905	-5.00	0	**-5.00**
100	**101**	35.566	-4.00	0	**-4.00**
100	**100**	31.698	-3.00	0	**-3.00**
100	**011**	28.251	-2.00	0	**-2.00**
100	**010**	25.179	-1.00	0	**-1.00**
100	**001**	22.440	0.00	0	**0.00(Default)**
100	**000**	20.000	1.00	0	**1.00**
011	**111**	44.774	2.00	0	**2.00**
011	**110**	39.905	3.00	0	**3.00**
011	**101**	35.566	4.00	0	**4.00**

011	**100**	31.698	5.00	0	**5.00**
011	**011**	28.251	6.00	0	**6.00**
011	**010**	25.179	7.00	0	**7.00**
011	**001**	22.440	8.00	0	**8.00**
011	**000**	20.000	9.00	0	**9.00**
010	**111**	44.774	10.00	0	**10.00**
010	**110**	39.905	11.00	0	**11.00**
010	**101**	35.566	12.00	0	**12.00**
010	**100**	31.698	13.00	0	**13.00**
010	**011**	28.251	14.00	0	**14.00**
010	**010**	25.179	15.00	0	**15.00**
010	**001**	22.440	16.00	0	**16.00**
010	**000**	20.000	17.00	0	**17.00**
001	**111**	20.000	17.00	1	**18.00**
001	**110**	20.000	17.00	2	**19.00**
001	**101**	20.000	17.00	3	**20.00**
001	**100**	20.000	17.00	4	**21.00**
001	**011**	20.000	17.00	5	**22.00**
001	**010**	20.000	17.00	6	**23.00**
001	**001**	20.000	17.00	7	**24.00**
001	**000**	20.000	17.00	8	**25.00**
000	**111**	20.000	17.00	9	**26.00**
000	**110**	20.000	17.00	10	**27.00**
000	**101**	20.000	17.00	11	**28.00**
000	**100**	20.000	17.00	12	**29.00**
000	**011**	20.000	17.00	13	**30.00**
000	**010**	20.000	17.00	14	**31.00**
000	**001**	20.000	17.00	15	**32.00**
000	**000**	20.000	17.00	16	**33.00**

(2)MIC VOL (REC PATH)

In REC Path, when MIC path is chosen, VADL(R) <5:0>'s gain is as following table.					
VADL<5:3> **VADR<5:3>**	**VADL<2:0>** **VADR<2:0>**	Ri(kΩ)	Gain1(dB)	Gain2(dB)	**Total Gain(dB)**
111	**111**	44.774	-18.00	0	**-18.00**

111	**110**	39.905	-17.00	0	**-17.00**
111	**101**	35.566	-16.00	0	**-16.00**
111	**100**	31.698	-15.00	0	**-15.00**
111	**011**	28.251	-14.00	0	**-14.00**
111	**010**	25.179	-13.00	0	**-13.00**
111	**001**	22.440	-12.00	0	**-12.00**
111	**000**	20.000	-11.00	0	**-11.00**
110	**111**	44.774	-10.00	0	**-10.00**
110	**110**	39.905	-9.00	0	**-9.00**
110	**101**	35.566	-8.00	0	**-8.00**
110	**100**	31.698	-7.00	0	**-7.00**
110	**011**	28.251	-6.00	0	**-6.00**
110	**010**	25.179	-5.00	0	**-5.00**
110	**001**	22.440	-4.00	0	**-4.00**
110	**000**	20.000	-3.00	0	**-3.00**
101	**111**	44.774	-2.00	0	**-2.00**
101	**110**	39.905	-1.00	0	**-1.00**
101	**101**	35.566	0.00	0	**0.00**
101	**100**	31.698	1.00	0	**1.00**
101	**011**	28.251	2.00	0	**2.00**
101	**010**	25.179	3.00	0	**3.00**
101	**001**	22.440	4.00	0	**4.00**
101	**000**	20.000	5.00	0	**5.00**
100	**111**	44.774	6.00	0	**6.00**
100	**110**	39.905	7.00	0	**7.00**
100	**101**	35.566	8.00	0	**8.00**
100	**100**	31.698	9.00	0	**9.00**
100	**011**	28.251	10.00	0	**10.00**
100	**010**	25.179	11.00	0	**11.00**
100	**001**	22.440	12.00	0	**12.00**
100	**000**	20.000	13.00	0	**13.00**
011	**111**	44.774	14.00	0	**14.00**
011	**110**	39.905	15.00	0	**15.00**
011	**101**	35.566	16.00	0	**16.00**
011	**100**	31.698	17.00	0	**17.00**
011	**011**	28.251	18.00	0	**18.00**

011	**010**	25.179	19.00	0	**19.00**
011	**001**	22.440	20.00	0	**20.00(Default)**
011	**000**	20.000	21.00	0	**21.00**
010	**111**	44.774	22.00	0	**22.00**
010	**110**	39.905	23.00	0	**23.00**
010	**101**	35.566	24.00	0	**24.00**
010	**100**	31.698	25.00	0	**25.00**
010	**011**	28.251	26.00	0	**26.00**
010	**010**	25.179	27.00	0	**27.00**
010	**001**	22.440	28.00	0	**28.00**
010	**000**	20.000	29.00	0	**29.00**
001	**111**	20.000	29.00	1	**30.00**
001	**110**	20.000	29.00	2	**31.00**
001	**101**	20.000	29.00	3	**32.00**
001	**100**	20.000	29.00	4	**33.00**
001	**011**	20.000	29.00	5	**34.00**
001	**010**	20.000	29.00	6	**35.00**
001	**001**	20.000	29.00	7	**36.00**
001	**000**	20.000	29.00	8	**37.00**
000	**111**	20.000	29.00	9	**38.00**
000	**110**	20.000	29.00	10	**39.00**
000	**101**	20.000	29.00	11	**40.00**
000	**100**	20.000	29.00	12	**41.00**
000	**011**	20.000	29.00	13	**42.00**
000	**010**	20.000	29.00	14	**43.00**
000	**001**	20.000	29.00	15	**44.00**
000	**000**	20.000	29.00	16	**45.00**

(3)LNI VOL (AA PATH)

VLNIL<5:3> **VLNIR<5:3>**	**VLNIL<2:0>** **VLNIR<2:0>**	Ri (kΩ)	**Gain (dB)**
111	**111**	44.77	**-30.00**
111	**110**	39.91	**-29.00**
111	**101**	35.57	**-28.00**
111	**100**	31.70	**-27.00**
111	**011**	28.25	**-26.00**
111	**010**	25.18	**-25.00**
111	**001**	22.44	**-24.00**
111	**000**	20.00	**-23.00**
110	**111**	44.77	**-22.00**
110	**110**	39.91	**-21.00**
110	**101**	35.57	**-20.00**
110	**100**	31.70	**-19.00**

110	**011**	28.25	**-18.00**
110	**010**	25.18	**-17.00**
110	**001**	22.44	**-16.00**
110	**000**	20.00	**-15.00**
101	**111**	44.77	**-14.00**
101	**110**	39.91	**-13.00**
101	**101**	35.57	**-12.00**
101	**100**	31.70	**-11.00**
101	**011**	28.25	**-10.00**
101	**010**	25.18	**-9.00**
101	**001**	22.44	**-8.00**
101	**000**	20.00	**-7.00**
100	**111**	44.77	**-6.00**
100	**110**	39.91	**-5.00**
100	**101**	35.57	**-4.00**
100	**100**	31.70	**-3.00**
100	**011**	28.25	**-2.00**
100	**010**	25.18	**-1.00**
100	**001**	22.44	**0.00**
100	**000**	20.00	**1.00**
011	**111**	44.77	**2.00**

011	**110**	39.91	**3.00**
011	**101**	35.57	**4.00**
011	**100**	31.70	**5.00**
011	**011**	28.25	**6.00**
011	**010**	25.18	**7.00**
011	**001**	22.44	**8.00**
011	**000**	20.00	**9.00**
010	**111**	44.77	**10.00**
010	**110**	39.91	**11.00**
010	**101**	35.57	**12.00**
010	**100**	31.70	**13.00**
010	**011**	28.25	**14.00**
010	**010**	25.18	**15.00**
010	**001**	22.44	**16.00**
010	**000**	20.00	**17.00**

Note:

1.When VLNIL(R)<5:0>=111111, VLNIL(R)M_EN will set to high to mute the LNIL(R) path in MIXER.

2. Digital Core should make sure that the value of VLNIL(R)<5:0> can't not smaller than 010000.

(4)MIC VOL (AA PATH)

VMICL<5:3> **VMICR<5:3>**	**VMICL<2:0>** **VMICR<2:0>**	Ri (kΩ)	**Gain** **(dB)**
111	**111**	44.77	**-15.0**
111	**110**	39.91	**-14.0**
111	**101**	35.57	**-13.0**
111	**100**	31.70	**-12.0**
111	**011**	28.25	**-11.0**
111	**010**	25.18	**-10.0**

111	**001**	22.44	**-9.0**
111	**000**	20.00	**-8.0**
110	**111**	44.77	**-7.0**
110	**110**	39.91	**-6.0**
110	**101**	35.57	**-5.0**
110	**100**	31.70	**-4.0**
110	**011**	28.25	**-3.0**
110	**010**	25.18	**-2.0**

110	**001**	22.44	**-1.0**
110	**000**	20.00	**0.0**
101	**111**	44.77	**1.0**
101	**110**	39.91	**2.0**
101	**101**	35.57	**3.0**
101	**100**	31.70	**4.0**
101	**011**	28.25	**5.0**
101	**010**	25.18	**6.0**
101	**001**	22.44	**7.0**
101	**000**	20.00	**8.0**
100	**111**	44.77	**9.0**
100	**110**	39.91	**10.0**
100	**101**	35.57	**11.0**
100	**100**	31.70	**12.0**
100	**011**	28.25	**13.0**
100	**010**	25.18	**14.0**
100	**001**	22.44	**15.0**
100	**000**	20.00	**16.0**
011	**111**	44.77	**17.0**

011	**110**	39.91	**18.0**
011	**101**	35.57	**19.0**
011	**100**	31.70	**20.0**
011	**011**	28.25	**21.0**
011	**010**	25.18	**22.0**
011	**001**	22.44	**23.0**
011	**000**	20.00	**24.0**
010	**111**	44.77	**25.0**
010	**110**	39.91	**26.0**
010	**101**	35.57	**27.0**
010	**100**	31.70	**28.0**
010	**011**	28.25	**29.0**
010	**010**	25.18	**30.0**
010	**001**	22.44	**31.0**
010	**000**	20.00	**32.0**

Note:

1. When VMICL(R)<5:0>=111111, VMICL(R)M_EN will set to high to mute the MICL(R) path in MIXER.

2. Digital Core should make sure that the value of VMICL(R)<5:0> can't not smaller than 010000.

(5)DRIVER

VML<5:0> VMR<5:0>		**Gain(dB)**	**VML<5:0> VMR<5:0>**		**Gain(dB)**
63	**111111**	**MUTE**	**31**	**011111**	**-31**
62	**111110**	**-62**	**30**	**011110**	**-30**
61	**111101**	**-61**	**29**	**011101**	**-29**
60	**111100**	**-60**	**28**	**011100**	**-28**
59	**111011**	**-59**	**27**	**011011**	**-27**
58	**111010**	**-58**	**26**	**011010**	**-26**
57	**111001**	**-57**	**25**	**011001**	**-25**

56	111000	-56	24	011000	-24
55	110111	-55	23	010111	-23
54	110110	-54	22	010110	-22
53	110101	-53	21	010101	-21
52	110100	-52	20	010100	-20
51	110011	-51	19	010011	-19
50	110010	-50	18	010010	-18
49	110001	-49	17	010001	-17
48	110000	-48	16	010000	-16
47	101111	-47	15	001111	-15
46	101110	-46	14	001110	-14
45	101101	-45	13	001101	-13
44	101100	-44	12	001100	-12
43	101011	-43	11	001011	-11
42	101010	-42	10	001010	-10
41	101001	-41	9	001001	-9
40	101000	-40	8	001000	-8
39	100111	-39	7	000111	-7
38	100110	-38	6	000110	-6
37	100101	-37	5	000101	-5
36	100100	-36	4	000100	-4
35	100011	-35	3	000011	-3
34	100010	-34	2	000010	-2
33	100001	-33	1	000001	-1
32	100000	-32	0	000000(Default)	0