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ARM big.LITTLE™ processing is an energy saving technology where the highest performance ARM CPUs are combined with the most efficient ARM CPUs in a combined processor subsystem to deliver greater performance at lower power than today's best-in-class systems. With big.LITTLE processing, software workloads are dynamically and instantly transitioned to the appropriate CPU based on performance needs. This software load balancing is so fast that it is completely seamless to the user. By selecting the optimum processor for each task, big.LITTLE can reduce energy consumption in the processor by 70% or more on light workloads and background tasks, and by 50% for moderately intense work, while still delivering the peak performance of the high performance cores.

More information can be found below or on the Think big.LITTLE microsite

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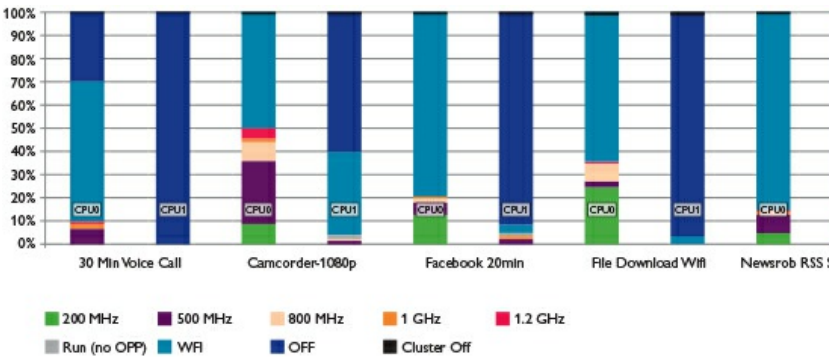
Background

The performance demanded of current smartphones and tablets is increasing at a much faster rate than the capacity of batteries or the power savings from semiconductor process advances. At the same time, users are demanding longer battery life within roughly the same form factor. This conflicting set of demands requires innovations in mobile SoC design beyond what process technology and traditional power management techniques can deliver.

The usage pattern for smartphones and tablets is dynamic: Periods of high processing intensity tasks, such as gaming and web browsing alternate with typically longer periods of low processing intensity tasks such as texting, e-mail and audio.



Innovative power savings techniques are required to sustain the dramatic pace of performance increases in mobile platforms while preserving and increasing the power efficiency and battery life.

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big.LITTLE Processing

ARM big.LITTLE processing is designed to deliver the vision of the right processor for the right job. In current big.LITTLE system implementations a 'big' ARM Cortex™-A15 processor is paired with a 'LITTLE' Cortex™-A7 processor to create a system that can accomplish both high intensity and low intensity tasks in the most energy efficient manner. For example, the performance capabilities of the Cortex-A15 processor can be utilized for heavy workloads, while the Cortex-A7 can take over to process most efficiently majority of smartphone workloads. These include operating system activities, user interface and other always on, always connected tasks.

By coherently connecting the Cortex-A15 and Cortex-A7 processors via the CoreLink™ CCI-400 coherent interconnect, the system is flexible enough to support a variety of big.LITTLE use models, which can be tailored to the processing requirements of the tasks.

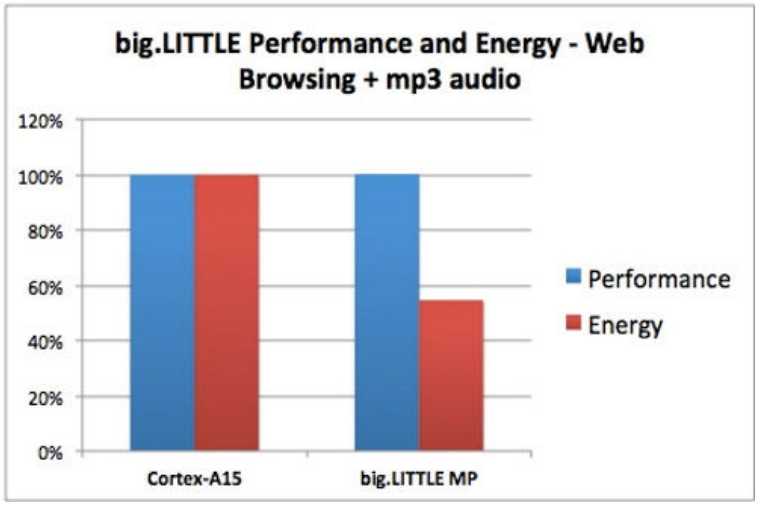
The central tenet of big.LITTLE is that the processors are architecturally identical. Both Cortex-A15 and Cortex-A7 implement the full ARMv7A architecture including Virtualization and Large Physical Address Extensions. Accordingly, all instructions will execute in an architecturally consistent way on both Cortex-A15 and Cortex-A7, albeit with different performances. The implementation defined feature set of Cortex-A15 and Cortex-A7 is also similar. Both processors can be configured to have between one and four cores and both integrate a level-2 cache inside the processing cluster. Additionally, each processor implements a single AMBA® 4 coherent interface that can be connected to a coherent interconnect such as CoreLink CCI-400

Future Implementations

In a similar fashion, the ARMv8 architecture-based Cortex-A53 and Cortex-A57 processor can also be implemented in a big.LITTLE configuration. In this case, the processors will be connected by the CoreLink CCN-504 coherent interconnect that enables a fully-coherent, high-performance many-core solution that supports up to 16 cores on the same silicon die.

Real World Performance Metrics

Energy savings of 50 percent for moderately intense workloads like web browsing, and savings of up to 70 percent for background workloads like mp3 audio playback have been measured. These measurements compare the average power consumption of a big.LITTLE system with a system with only the big processor, under full DVFS power management and core idle policies in each case.



These results were initially measured on test silicon and have recently been replicated on partner silicon across a range of typical mobile workloads. The software changes to take advantage of big.LITTLE are typically done in the OS kernel scheduler and are completely transparent for the application running on that OS.