Micro-Needle Camera with a 2-Wire Interface

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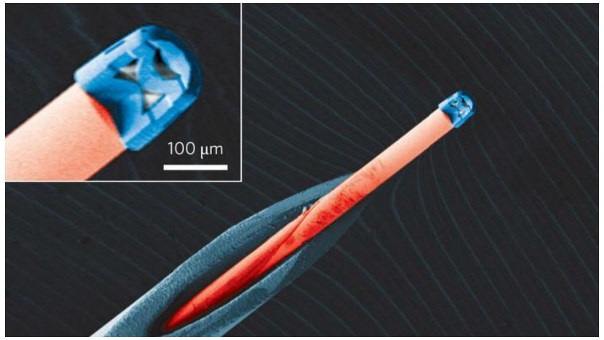
What is a needle camera?

- Initially, endoscope procedures were largely limited to the throat and other large passageways. Now, you can use tiny cameras mounted on needles to examine other parts of your body.



- Needle cameras have applications ranging from diagnosis all the way to surgical procedures.

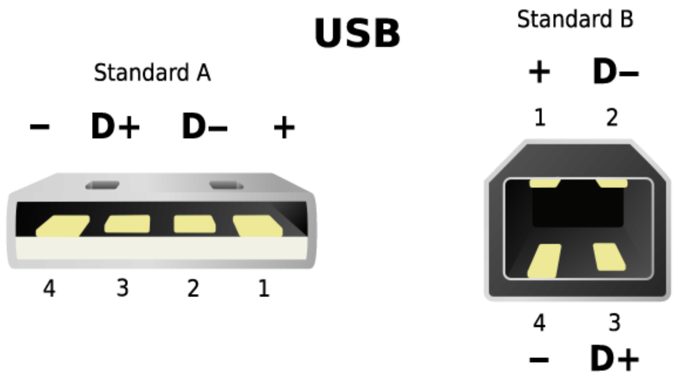
- Needle cameras can also be used for 3D modelling of internal structures such as blood vessels.

Why a 2-wire interface?

- Generic communication interfaces use 4-wire interfaces with two wires carrying the signal and two wires carrying power.

- Cannot be used for a micro-needle camera as DC currents cause chemical reactions resulting in corrosion of wires.

- Also want to minimize the wires in contact with the body.



- Need some way to integrate power and data onto the same wires.

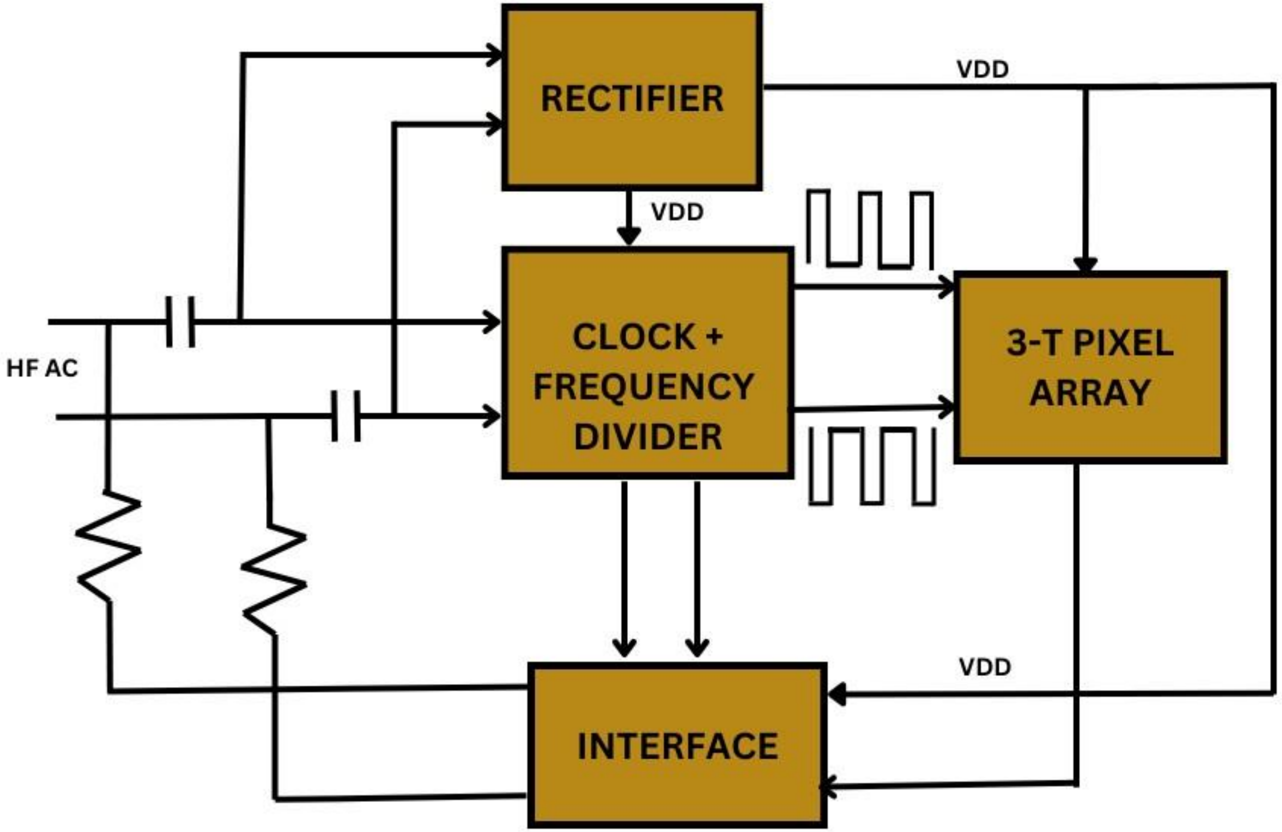
- One way: Frequency-Division Multiplexing

(HF Power combined with LF Data Signals)

Design Goals

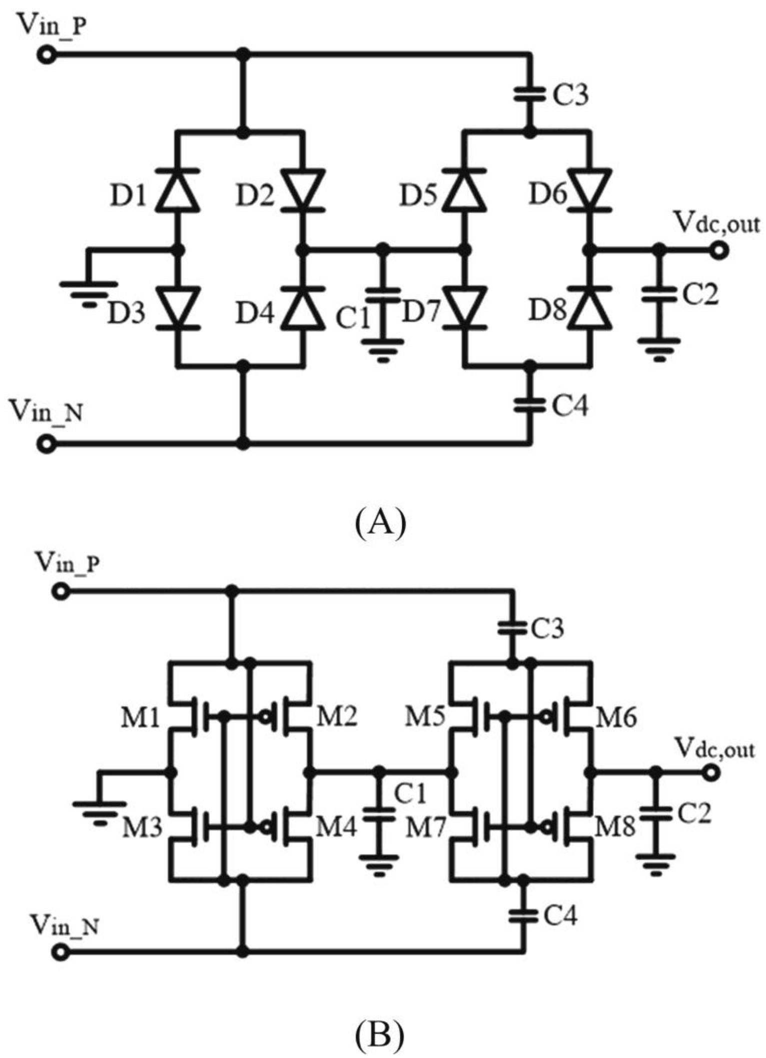
- 8-px resolution.
- Data transmission over the two wires.
- Power Optimization and reduce complexity.
- Make it work altogether.

Micro-needle Camera Design Overview

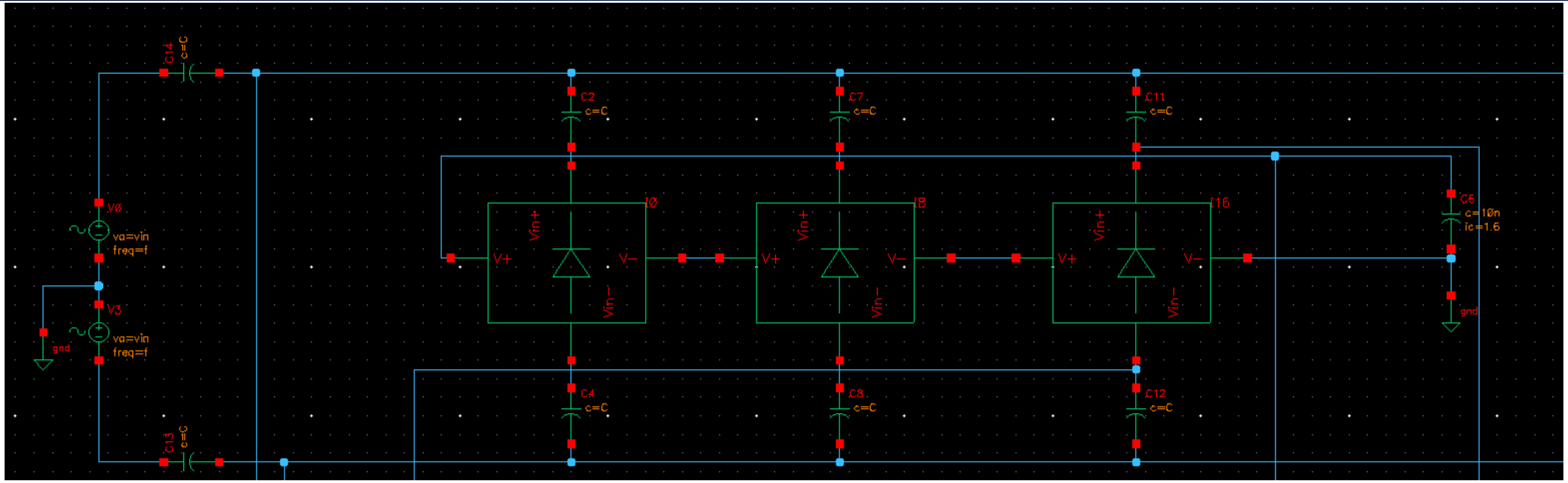


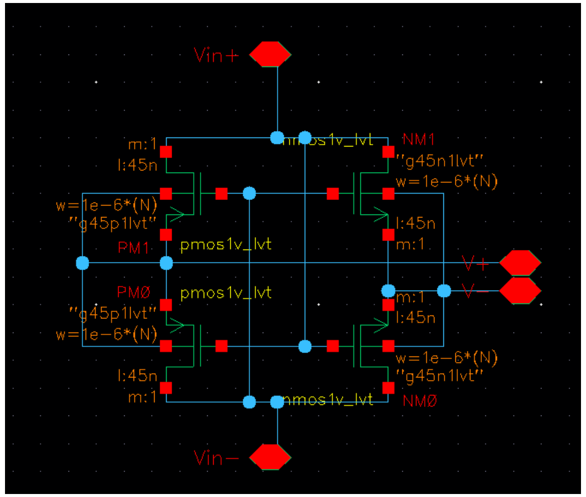
CMOS Rectifier

- CMOS rectifier has no voltage drop unlike the diode bridge rectifier.
- Can be cascaded together to provide a larger rectified voltage.
- Can give multiple DC voltage tap-out points.
- The current capability can be increased by increasing either frequency or the capacitances C3 and C4.

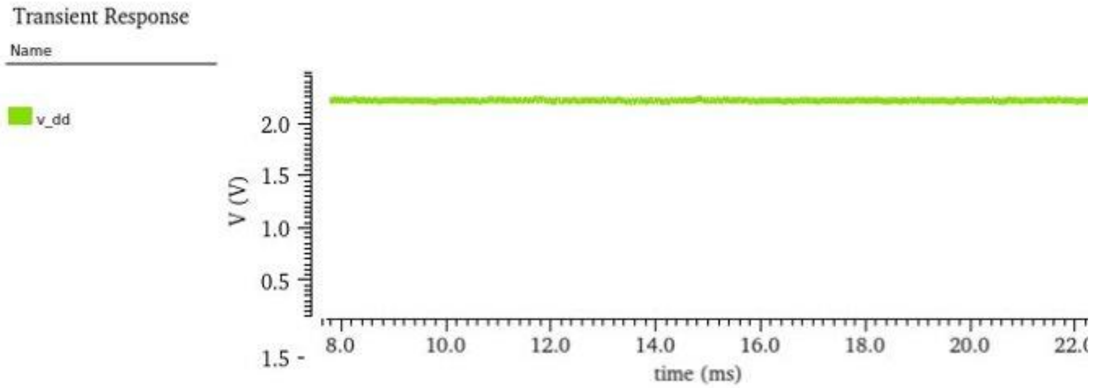


CMOS Rectifier Implemented – 3 Stage

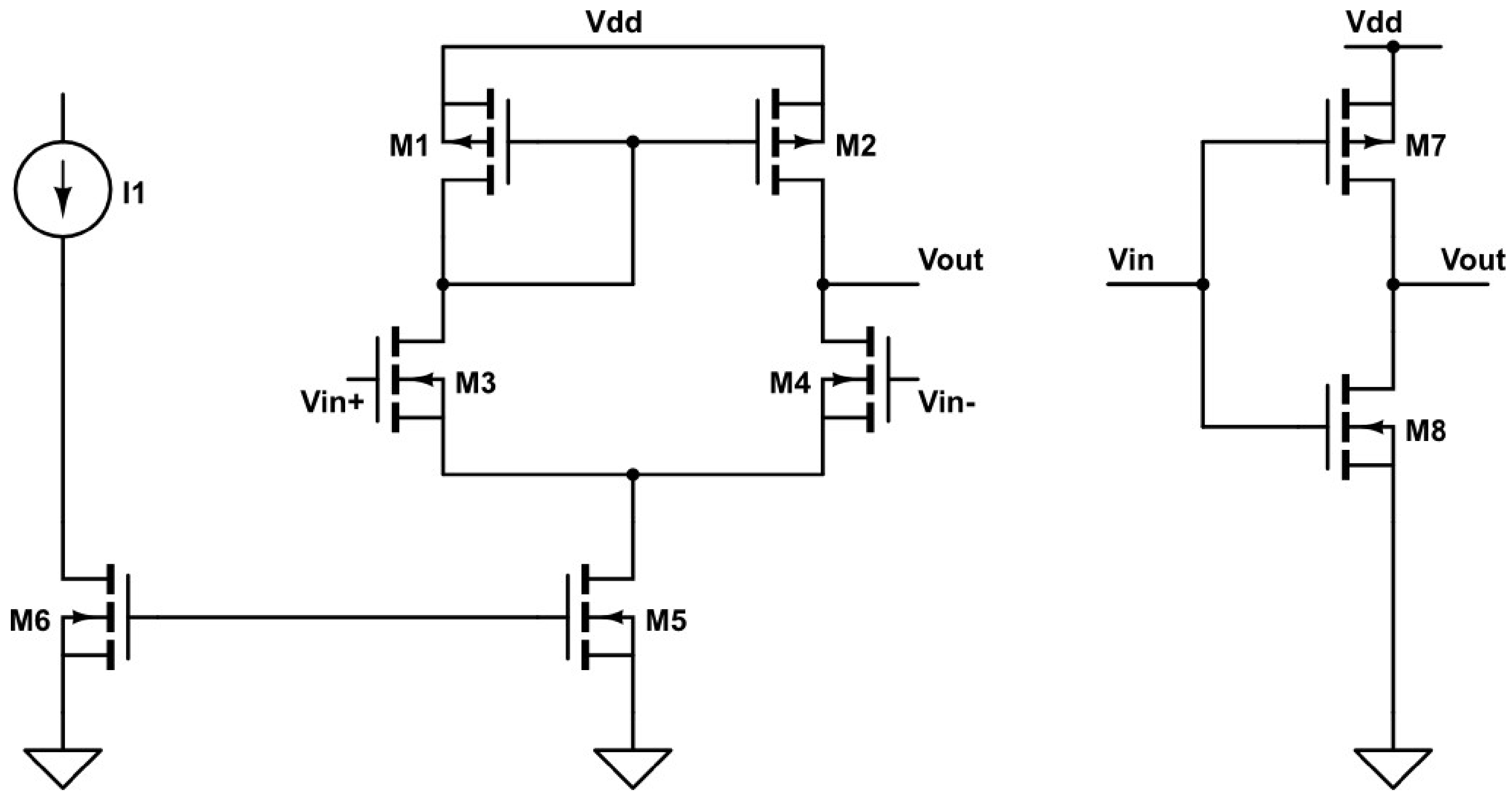




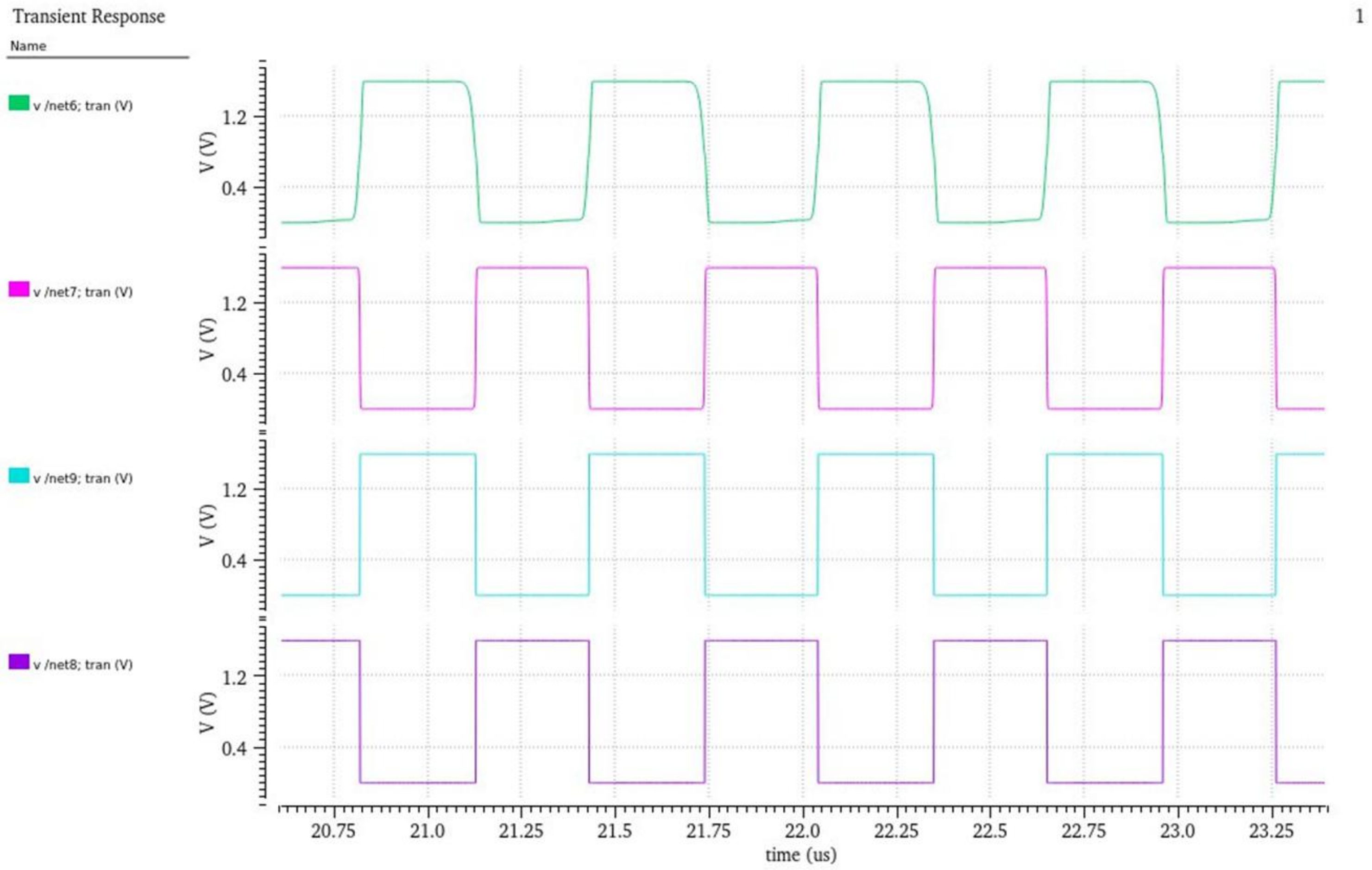
VDD Steady State Value = 2.23V



Clock Circuit Design



Generated Clock Pulses



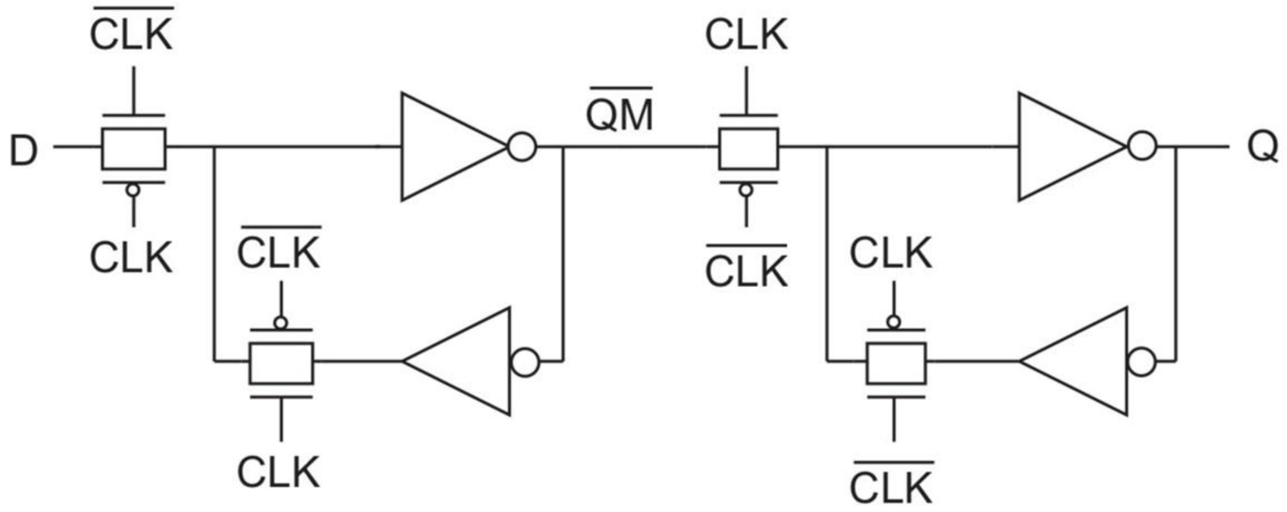
← Diff Pair Output

← First Inverter

← CLK

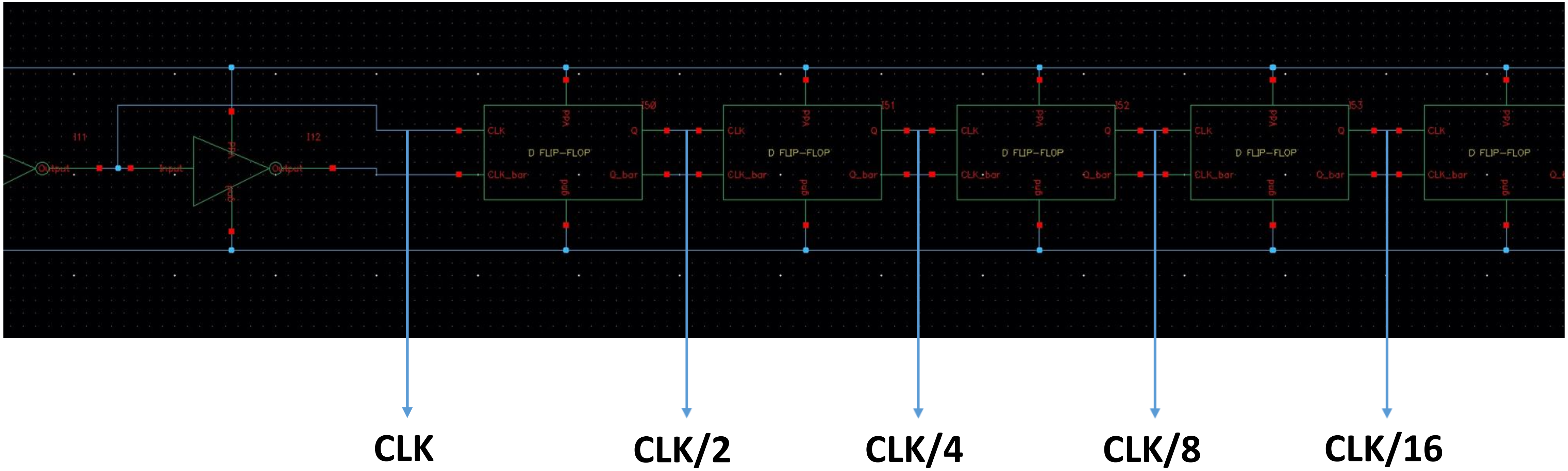
← $\overline{\text{CLK}}$

Frequency Divider

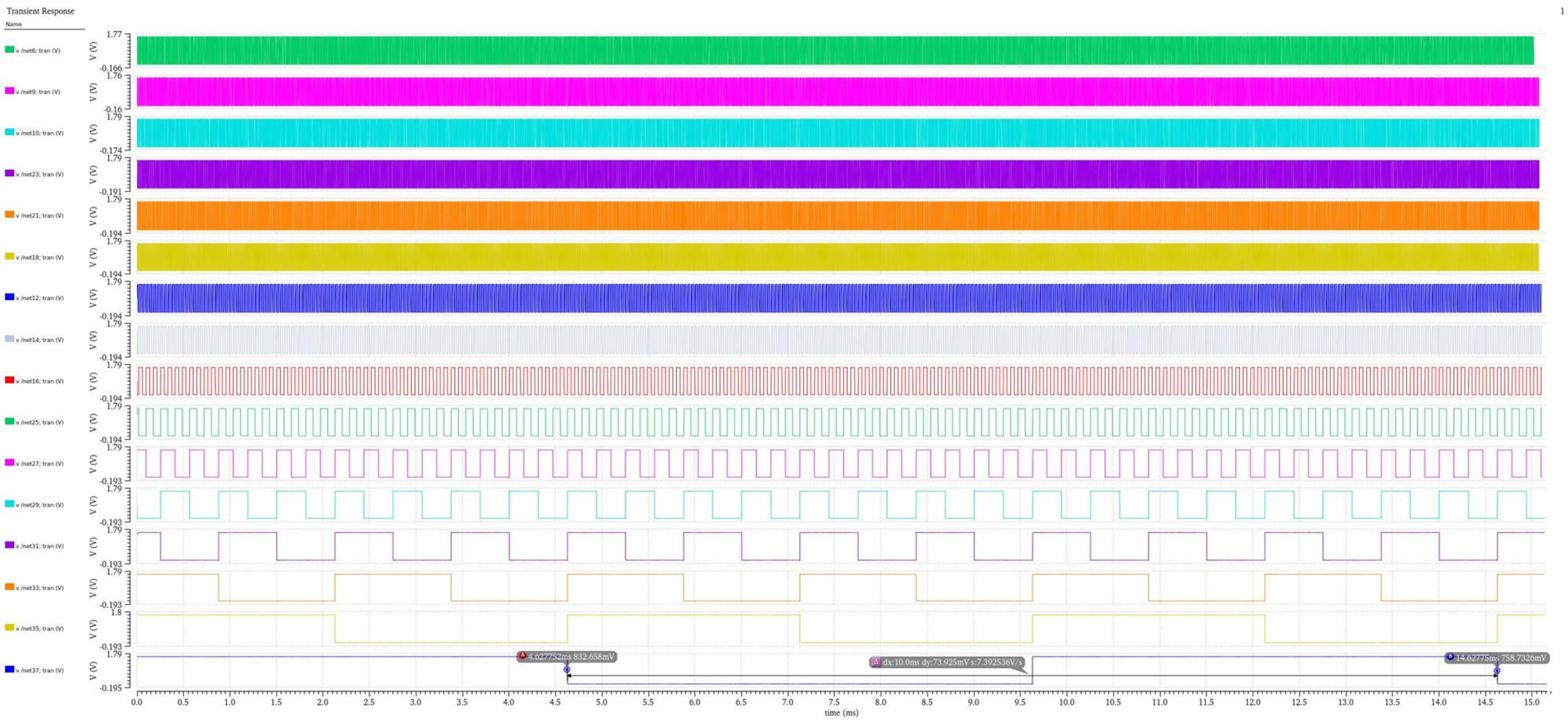


- D flip-flop: divide the frequency by 2
- 14 flip flops: divide the frequency from original 1.6384MHz to 100Hz

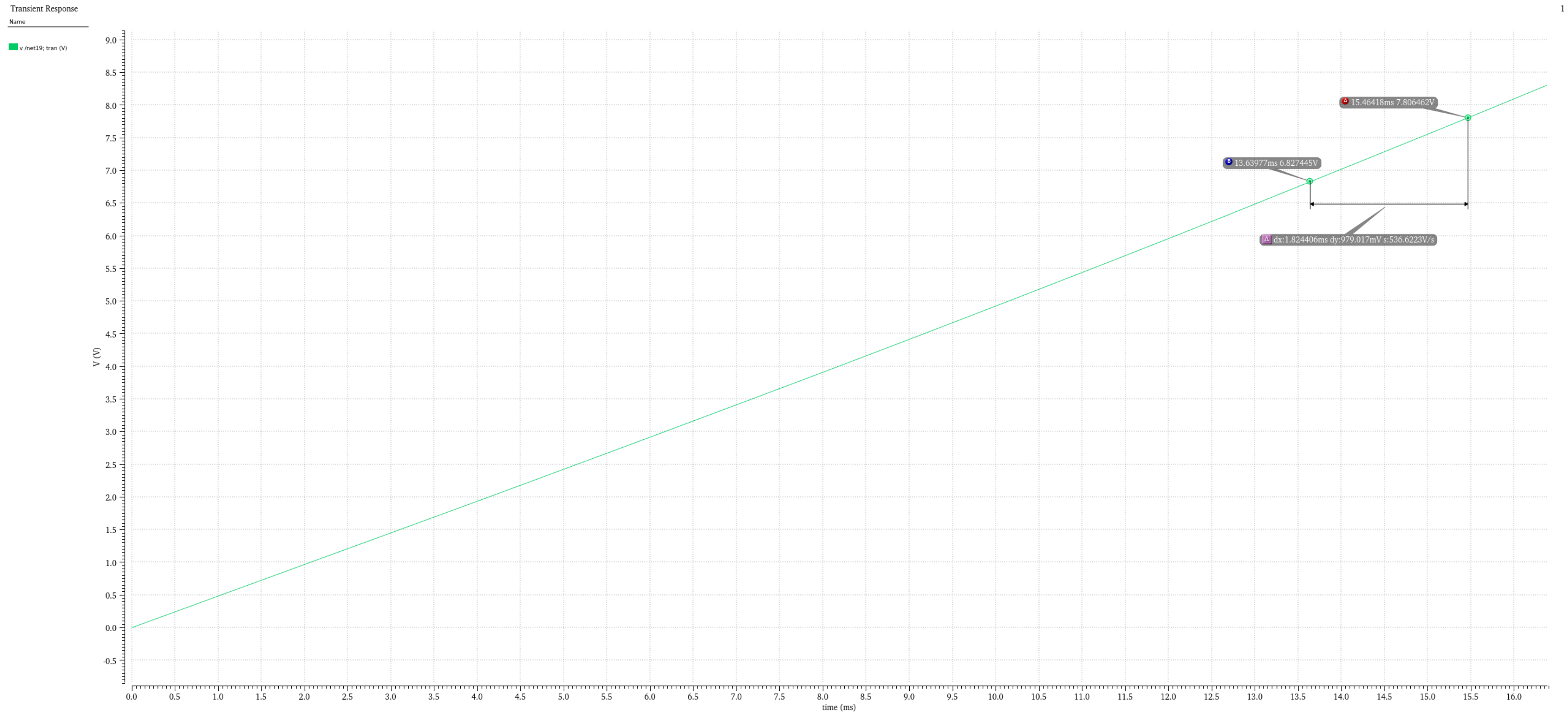
Clock Divider



Generated Clock Pulses

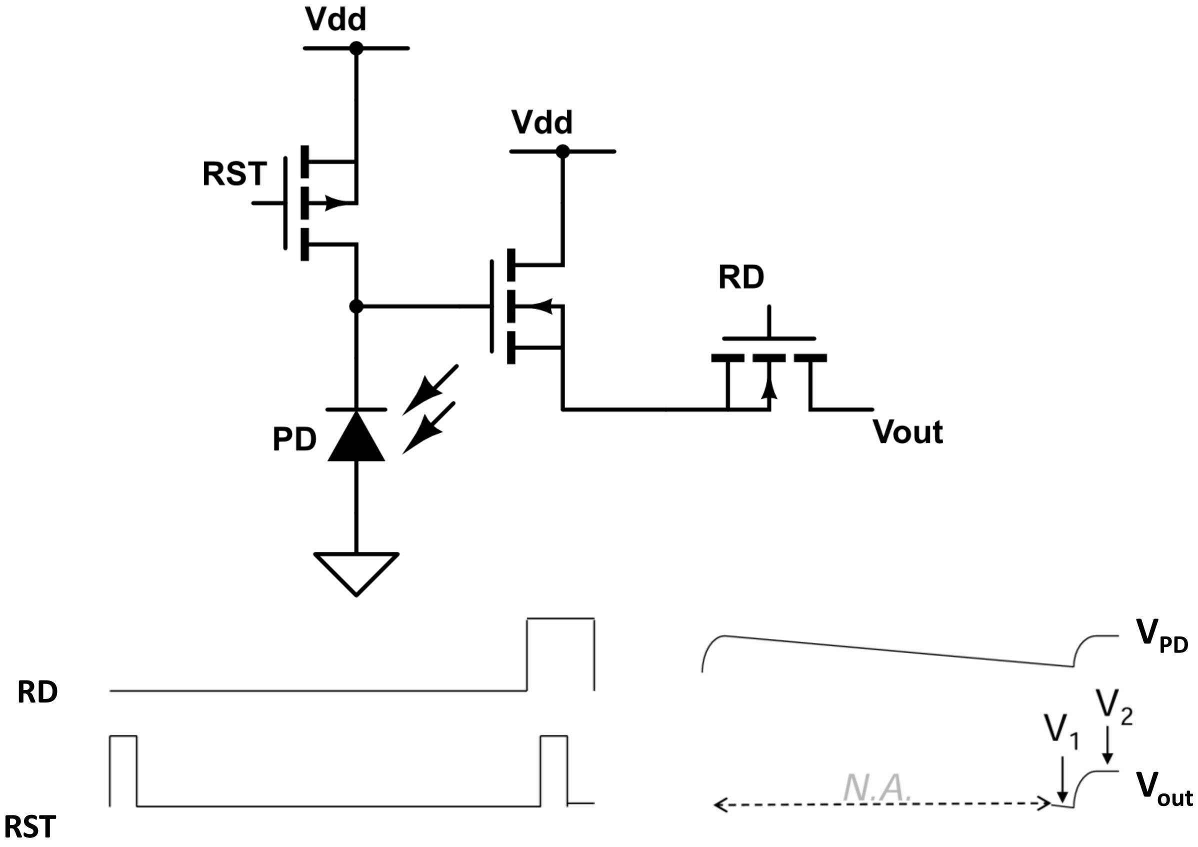


Performance Evaluation



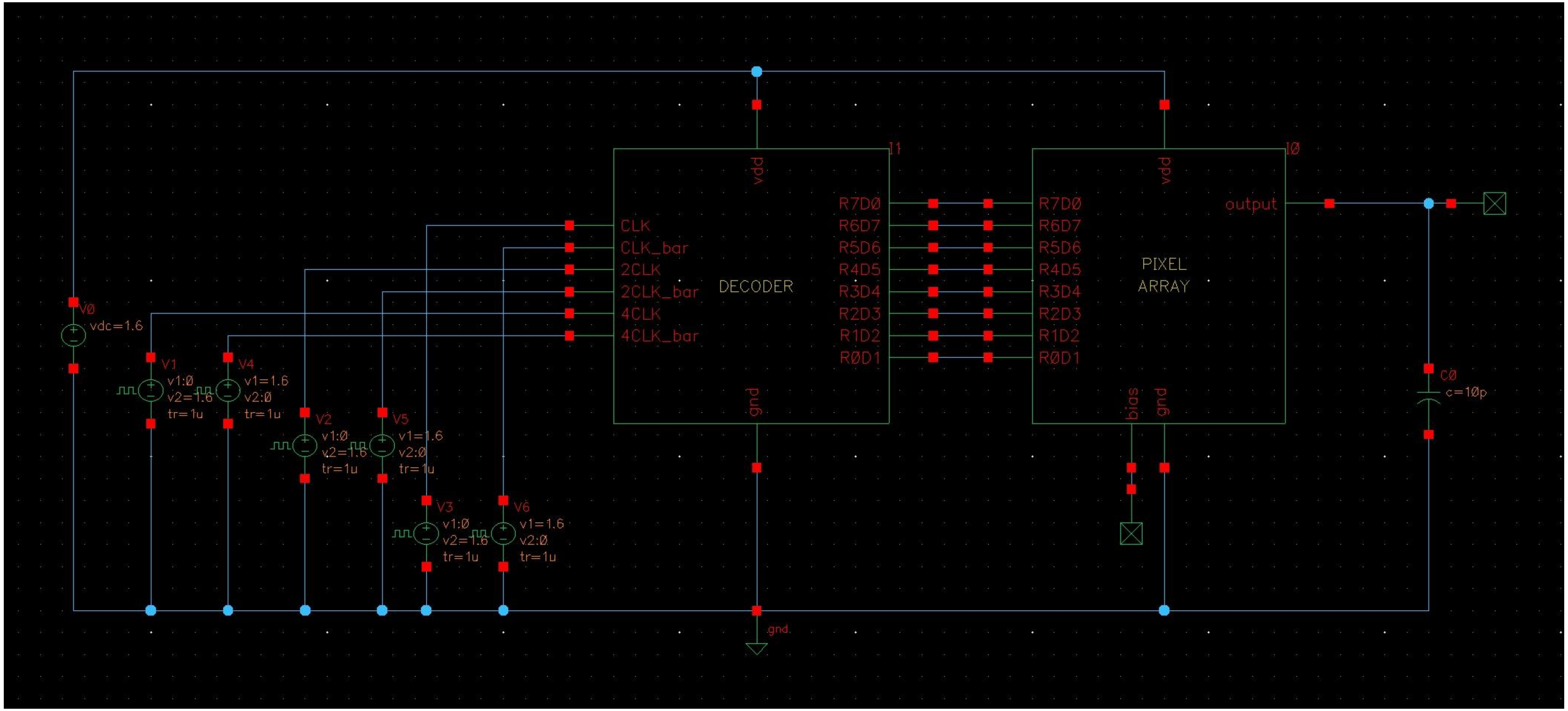
- Cap = 1n F
- Average Current = 0.53 µA
- Power = 0.85 µW

3-Transistor Pixel



- Reset Transistor (RST)
  - Pre-charge the photodiode to starting voltage V_{RST}
- Source follower(SF) transistor
  - Amplifies the final output current
- RD Transistor
  - Outputs the value of the circuit when selected
- Photodiode(PD)
  - $V_{PD\_RST} = V_{DD} - V_{TH(RST)}$

8-Pixel Design Overview



Single 3-Transistor Pixel Simulation

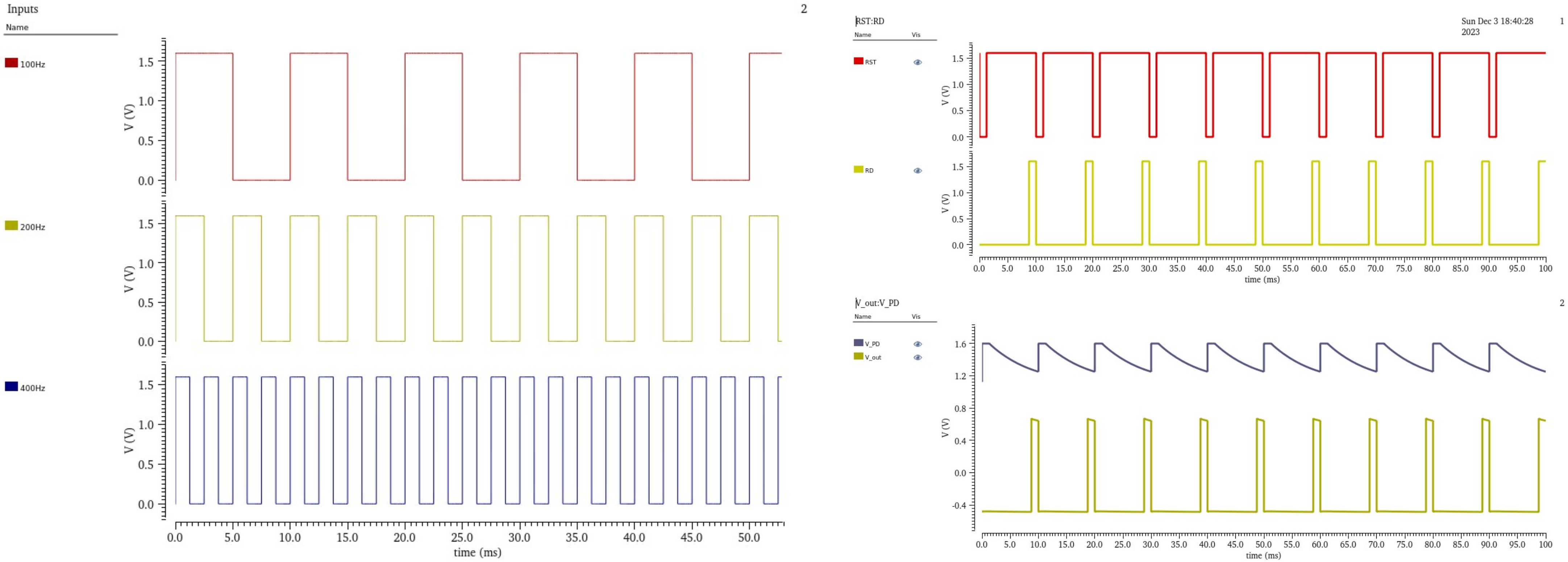
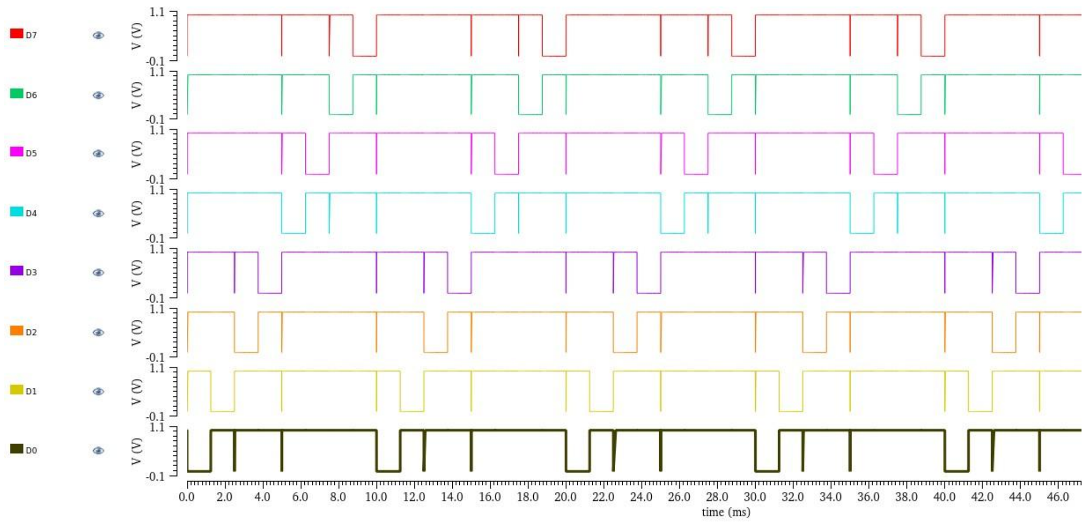
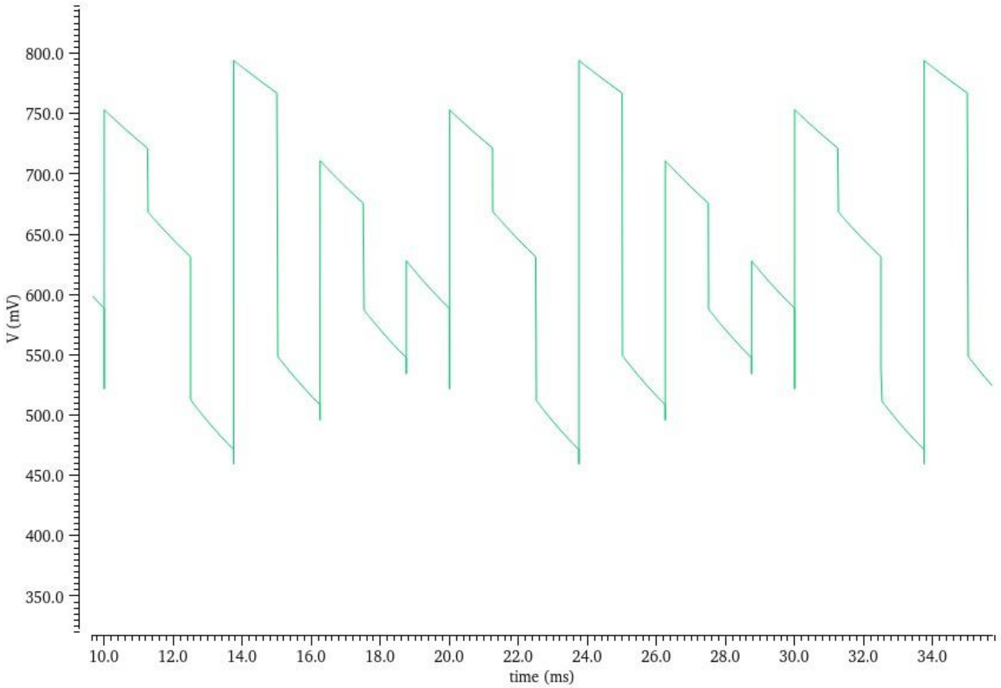


Figure 3: Active Pixel Inputs and Outputs

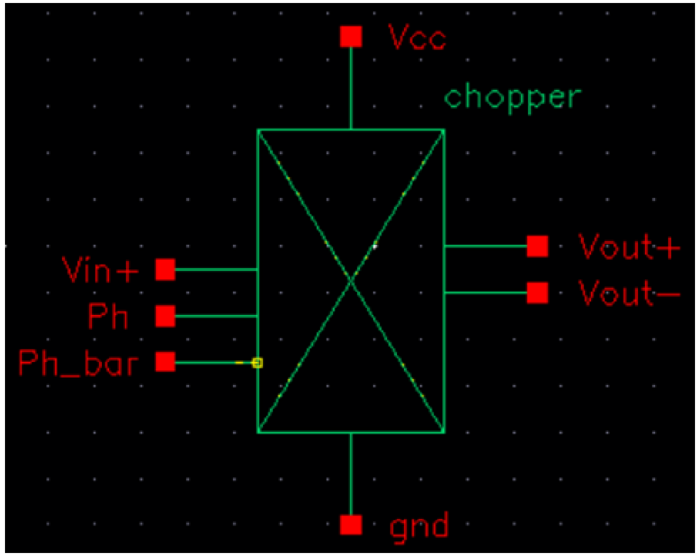
Decoder - 8 Pixel Simulation

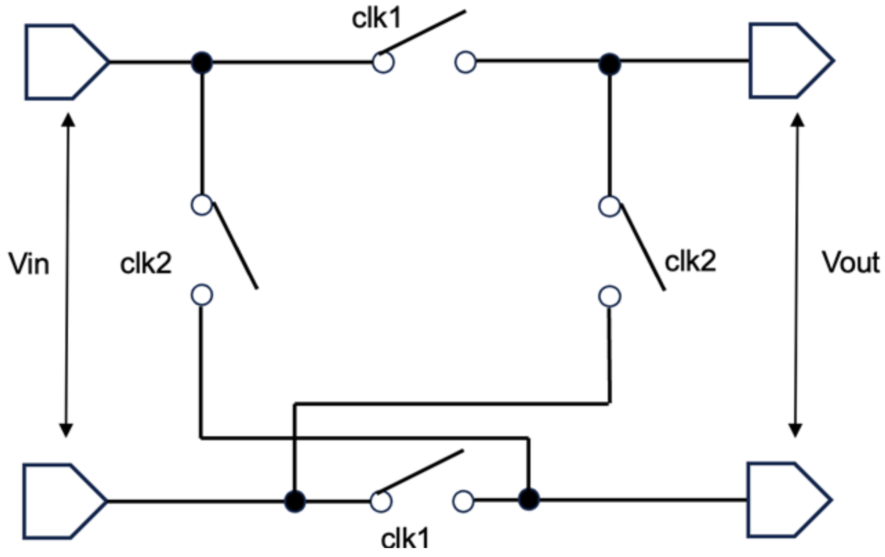




- Read N
- Reset N-1

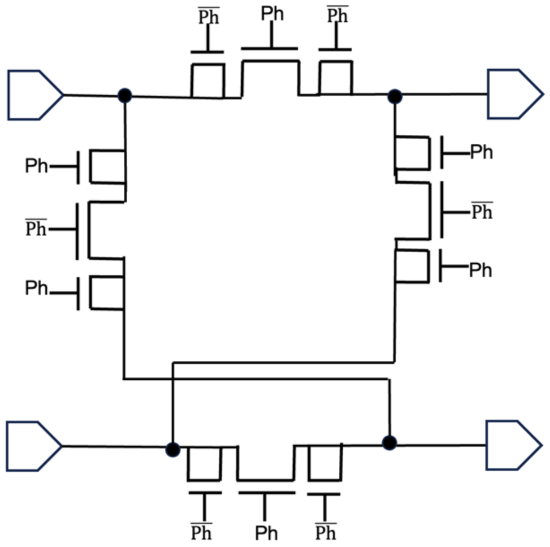
Interface

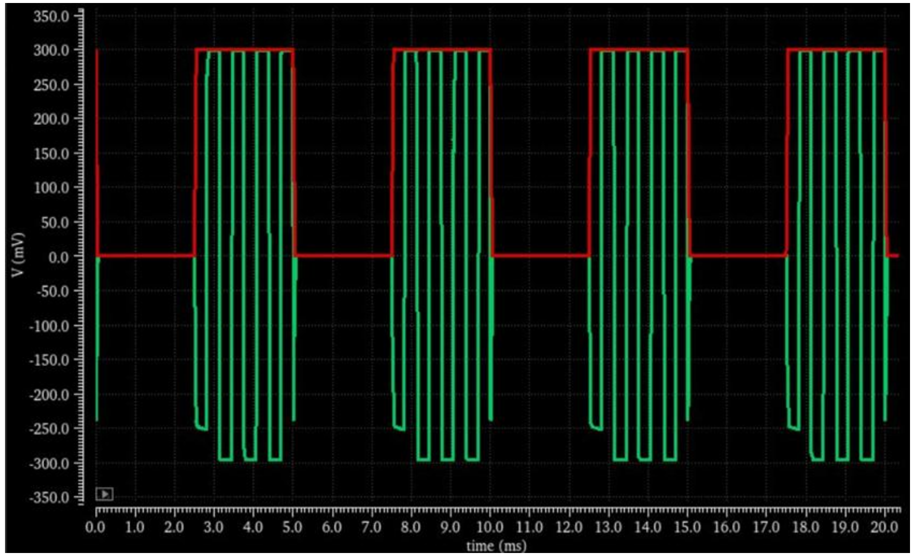




- provides inverting and non-inverting signal separately
- Two inverted clocks control the MOS transistor switches to exchange differential input signals

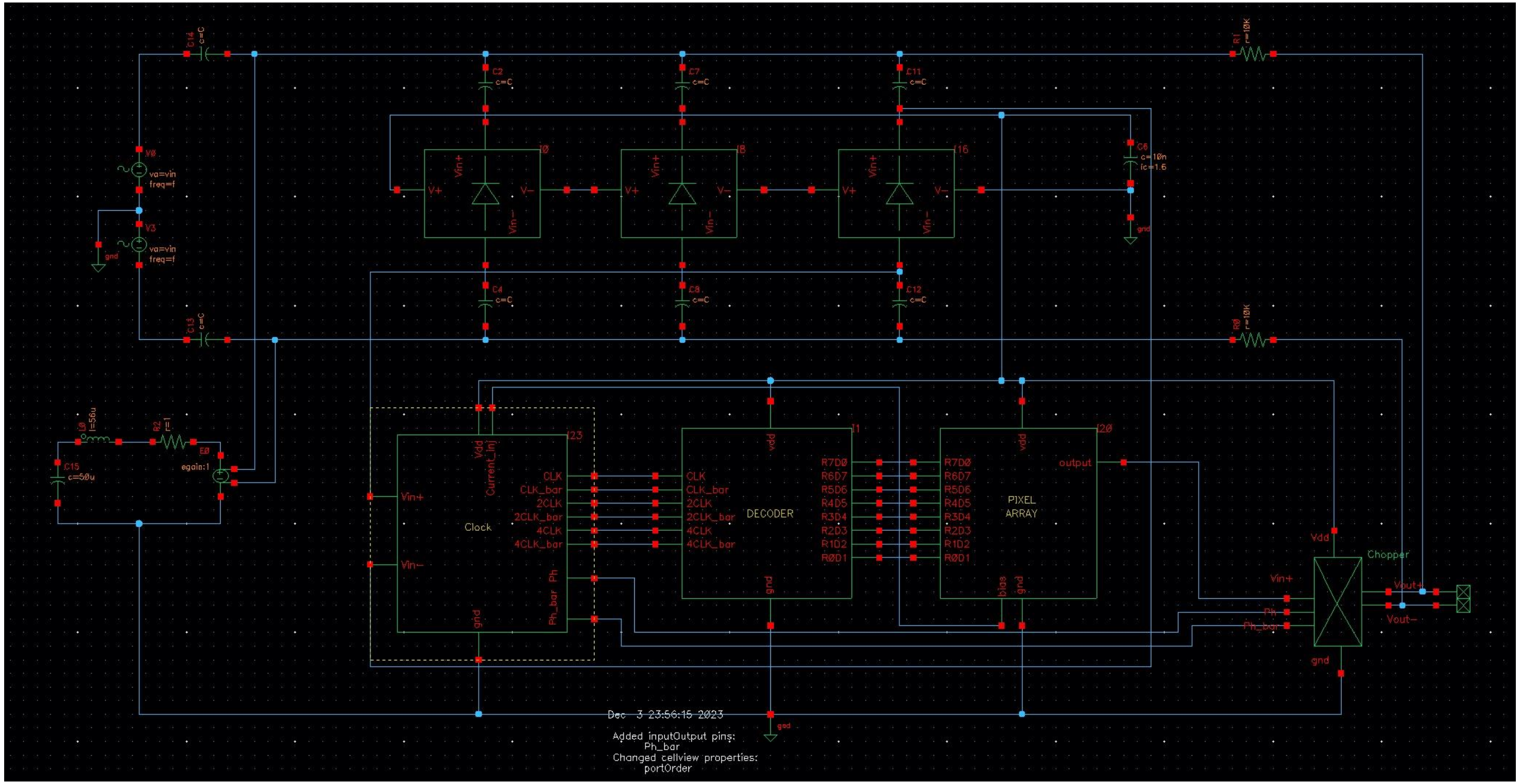
Interface Implementation



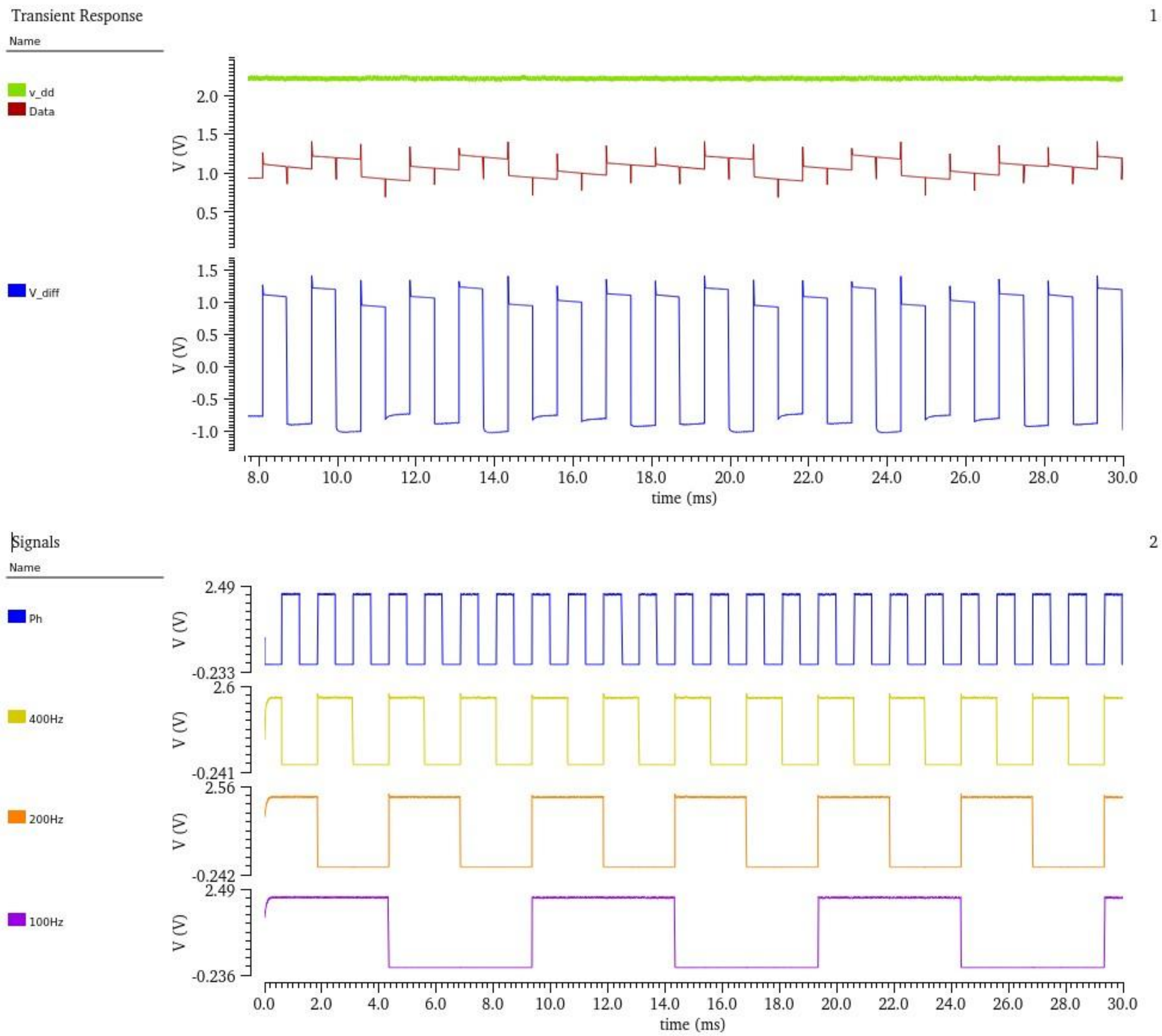


- Dummy Switch: Its clock is opposite to that of the main switch
- When the main switch is turned off, the leaked charge is absorbed by the open switches on both sides

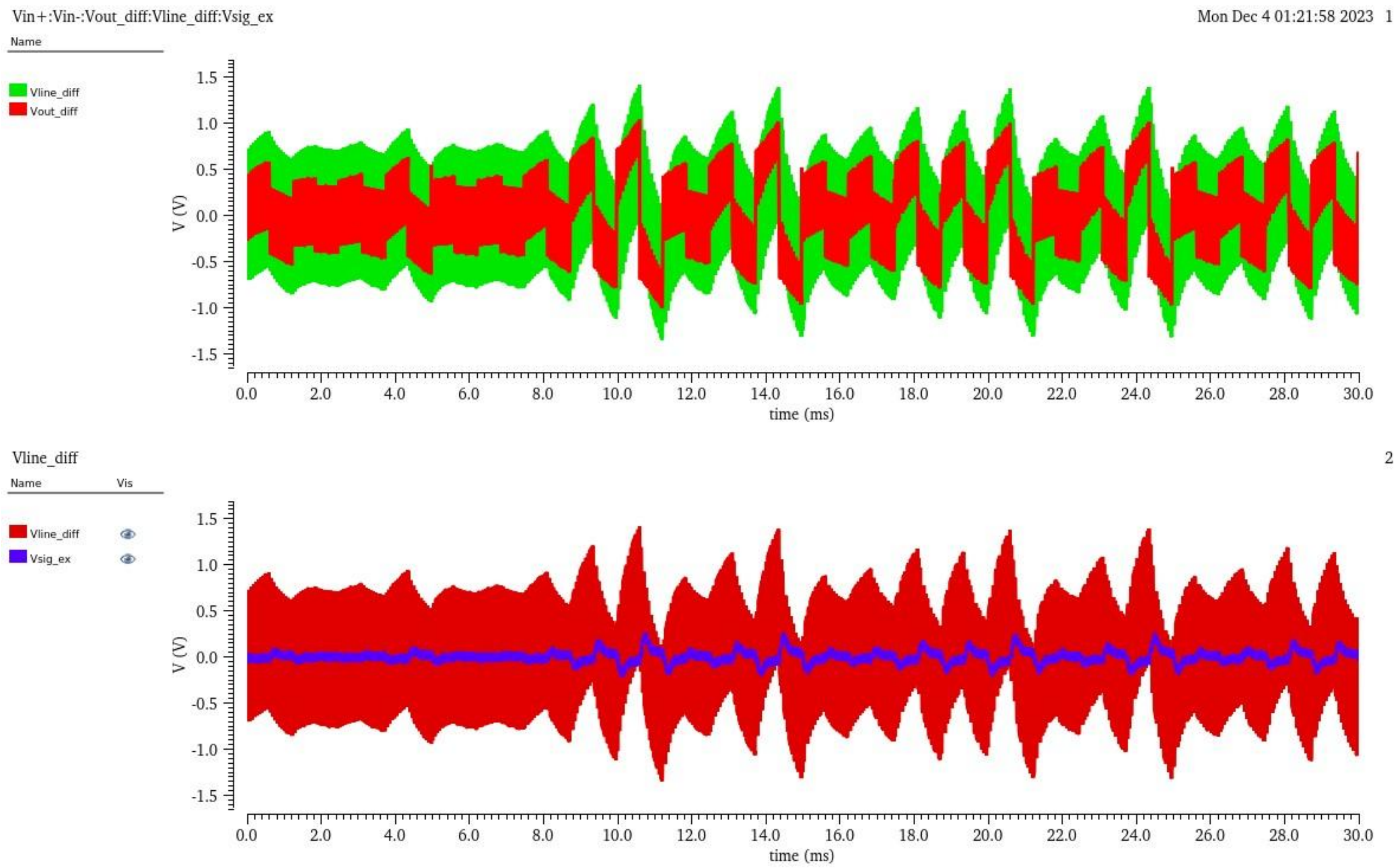
Complete Schematic



Open-loop Results



Closed-loop Results



Reference

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