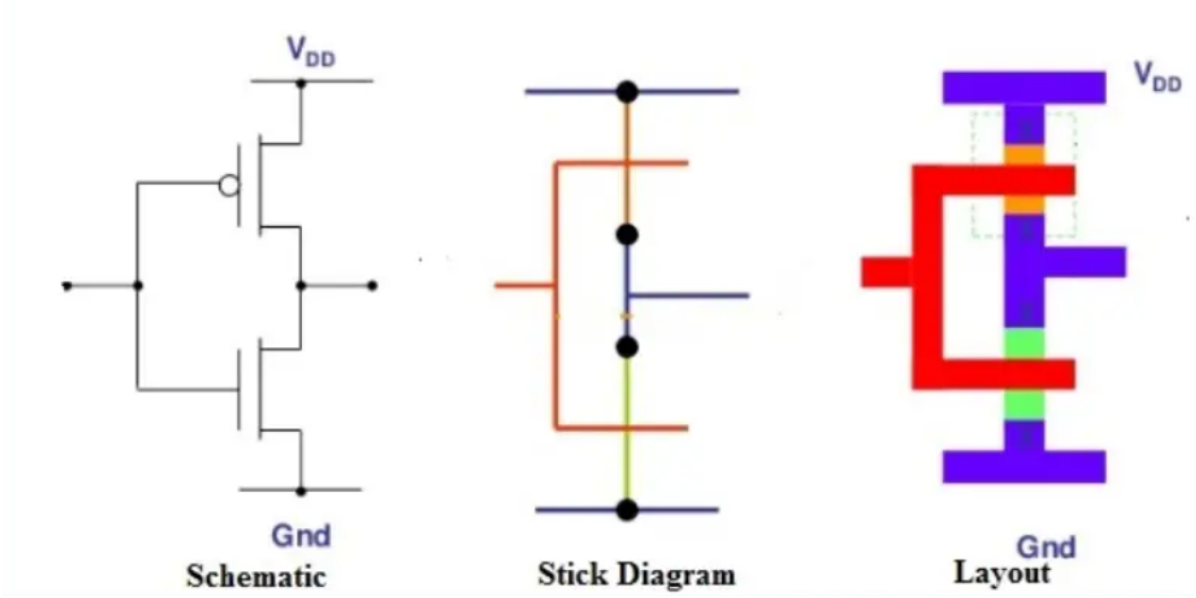
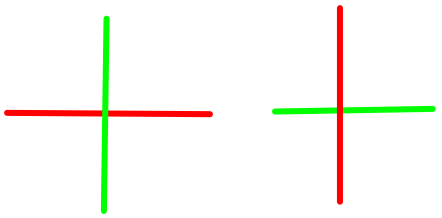
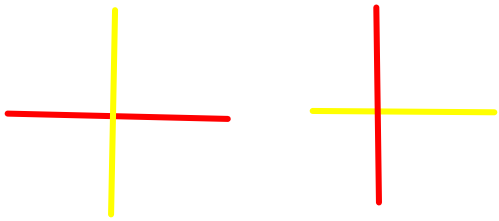
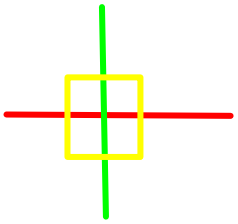
Stick Diagram

A stick diagram is a diagrammatic representation of a chip layout that helps to abstract a model. Stick diagrams are used to convey the layer information with the help of color code.

Layer name	Layer color	Representation
1. Metal	Blue	
2. Polysilicon	Red	
3. N+ diffusion	Green	
4. P+ diffusion	yellow	
5. Contact	Black	
6. Demarkation line	Brown	

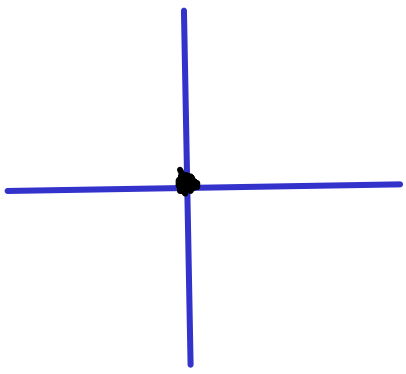
Brown



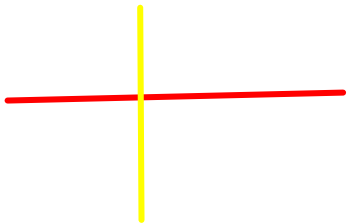
Transistor	Color Coding	Representation
1. NMOS Transistor	Red over green	
2. PMOS Transistor	Red over yellow	
3. NMOS Depletion type transistor	Red over green with yellow box at centre	

Rules to draw stick diagram:

1. When two or more "sticks" of same type cross or touch each other that represents electrical contact

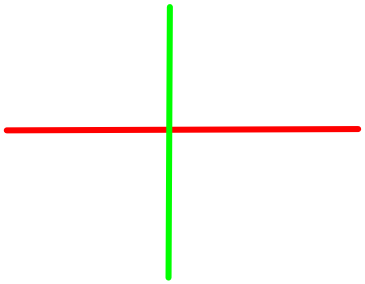


2. When two or more sticks of different type cross or touch each other , there is no electrical contact.

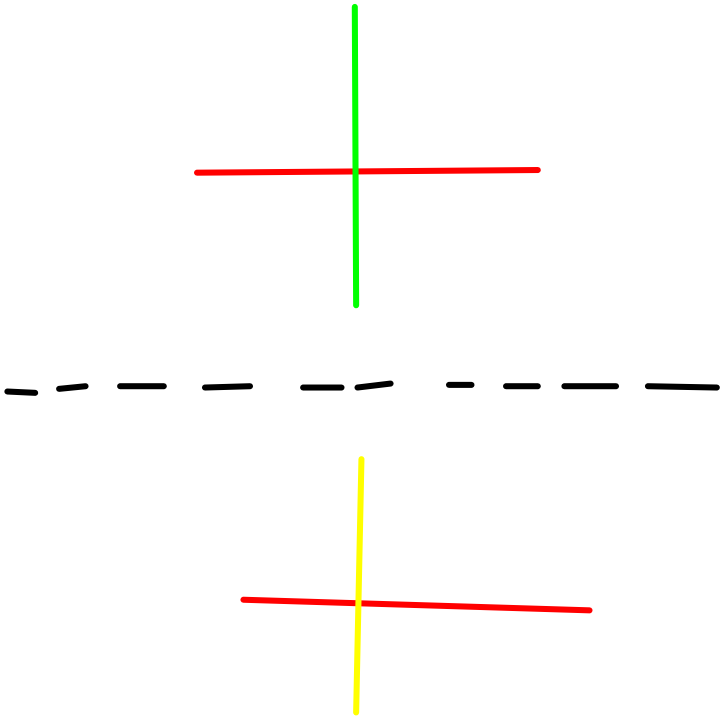


If you want provide electric contact, then you need to use "Black" dot.

3. When poly crosses the diffusion layer, that represents a "transistor"



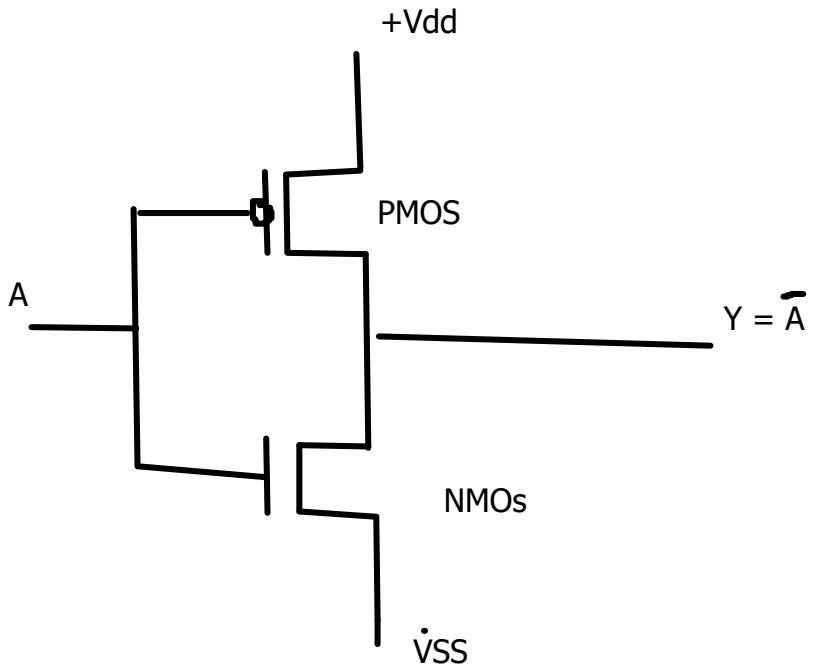
4. Draw a demarkation line to seperate PMOS and NMOS in CMOS circuits



y = A bar

If I have 1 input, then I require 1 PMOS and 1 NMOS

If I have 3 inputs, then I need 3 PMOS and 3 NMOS



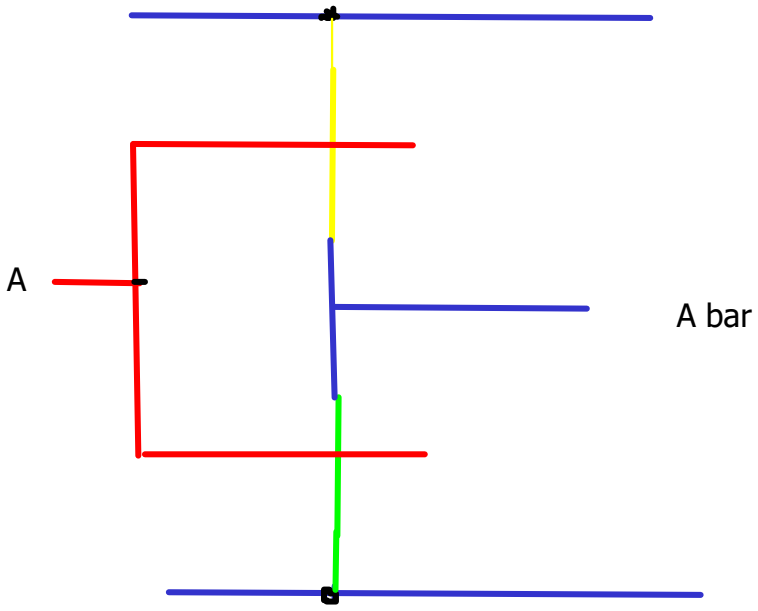
Draw the metal lines (Vdd, Vss)

Draw the transistors

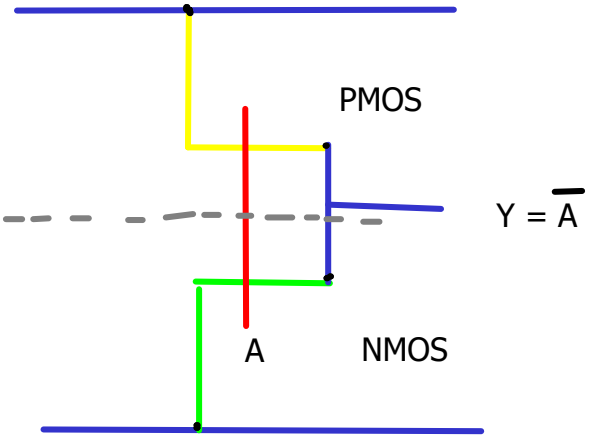
Join the interconnection with metal layer (blue)

Join the different wires/layers with contacts (black)

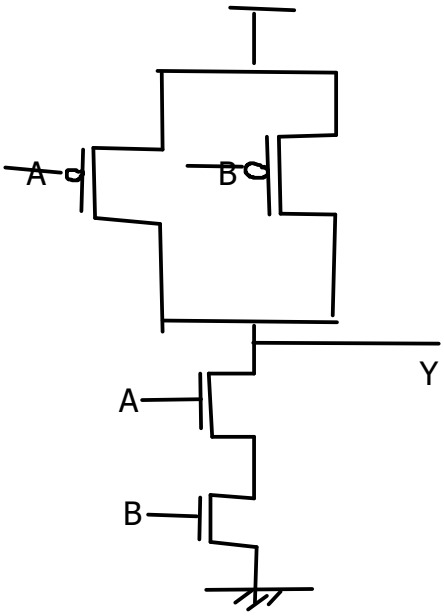
Draw the demarcation lines

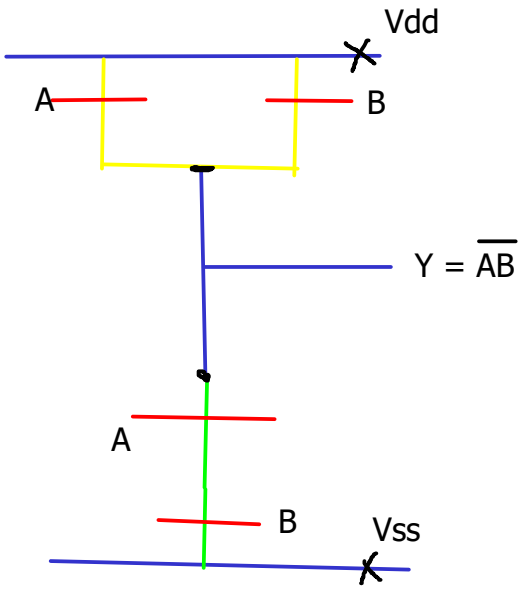


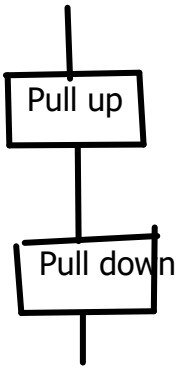
Another type of CMOS inverter



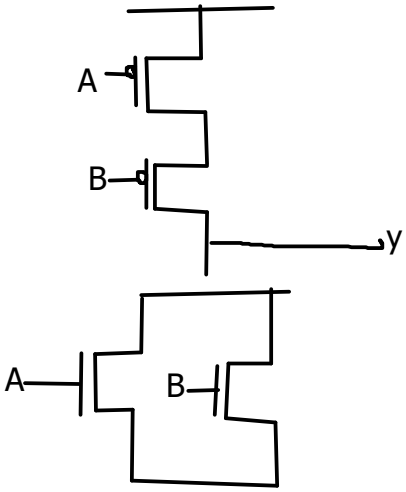
Stick diagram of Nand Gate. $Y = \overline{A.B}$

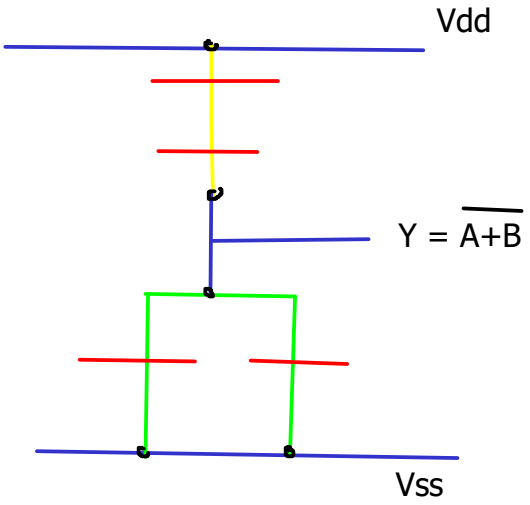






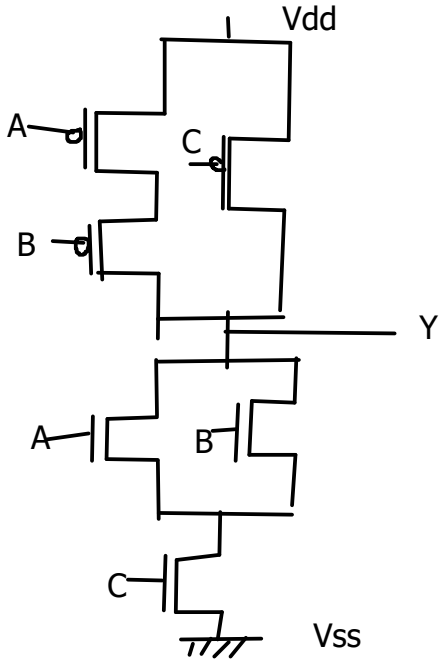
Stick diagram of NOR Gate $Y = \overline{A+B}$

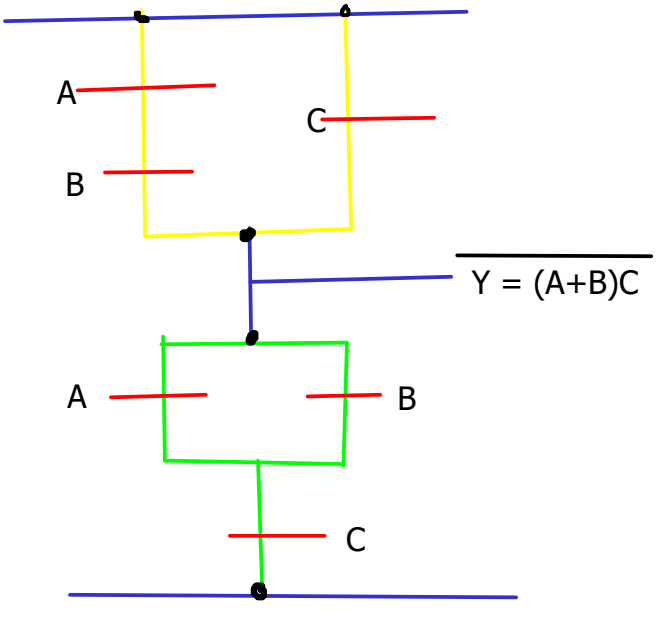


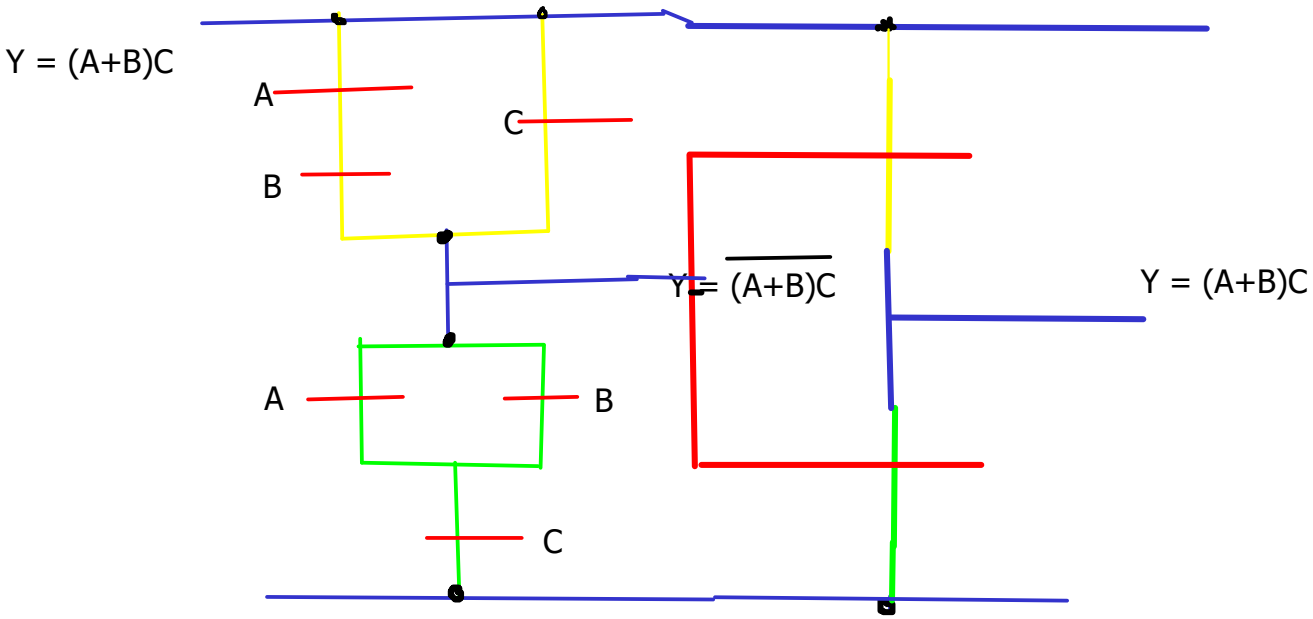


$Y = \overline{(A+B)C}$

And p p





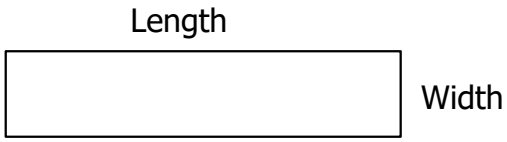


$\overline{\overline{A}} = A$

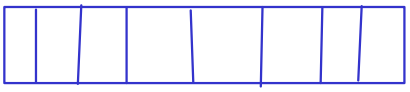
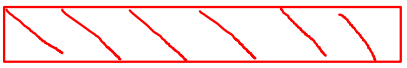
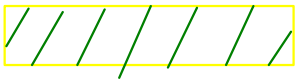
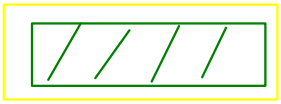
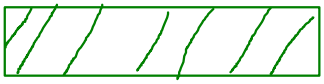
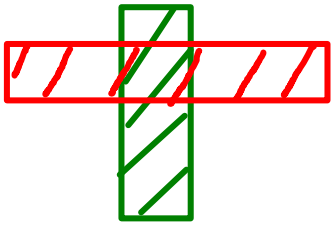
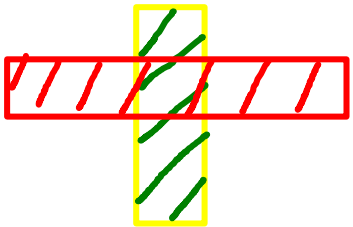
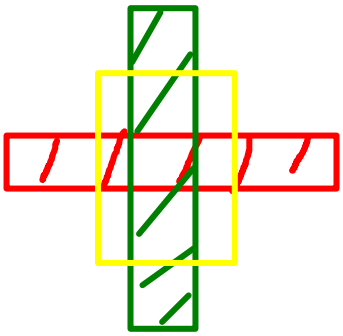
Mos Layout Layers

Layout: The fabrication on a silicon wafer is done with the help of layout diagrams.

All the layers in layout represented by its length and width.



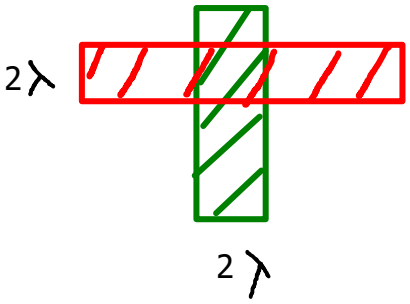
$Z = L / W$

Name of the layer	Color coding of layer	Representation
1. Metal -1	Blue (vertical line)	
2. Metal -2	Blue (Horizontal line)	
3. Polysilicon	Red	
4. P+ diffusion	1. Yellow border with green line 2. Green lines and border with yellow outer box	 
5. N+ diffusion	Green box with line	
6. Contact	Black	
7. NMOS Transistor	Red over N+ diffusion	
8. PMOS Transistor	Red over P+ diffusion	
9. Depletion Mode NMOS	Red over green with ion implantation	

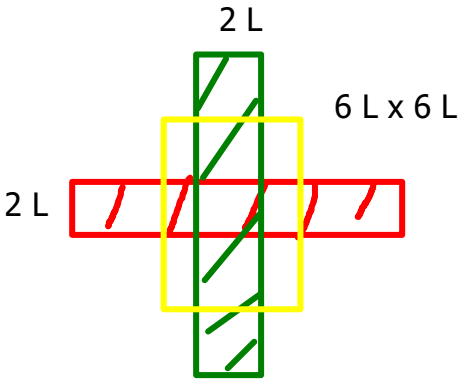
Lambda λ based design rules for Mask Layout

micrometer design rule

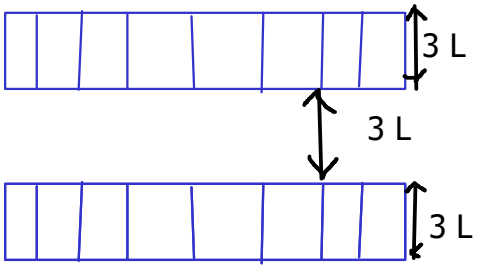
1. NMOS TRansistor



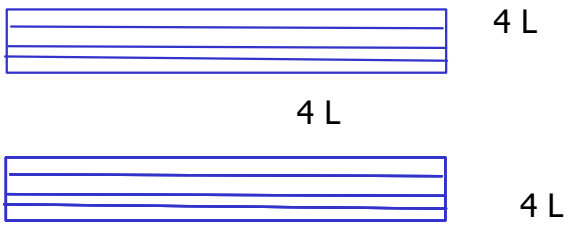
3. Depletion Mode NMOS

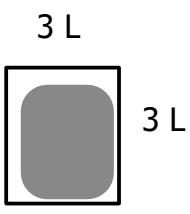


Metal -1



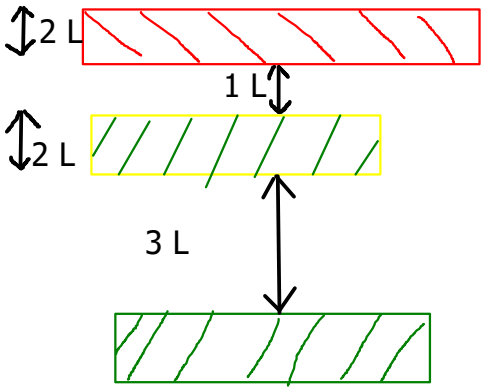
Metal 2





Contact cut

Contact cut is used to give connections between two different layers



1. Spacing between 2 polysilicons = 2 lambda

2. Spacing between 2 diffusions = 3 lambda

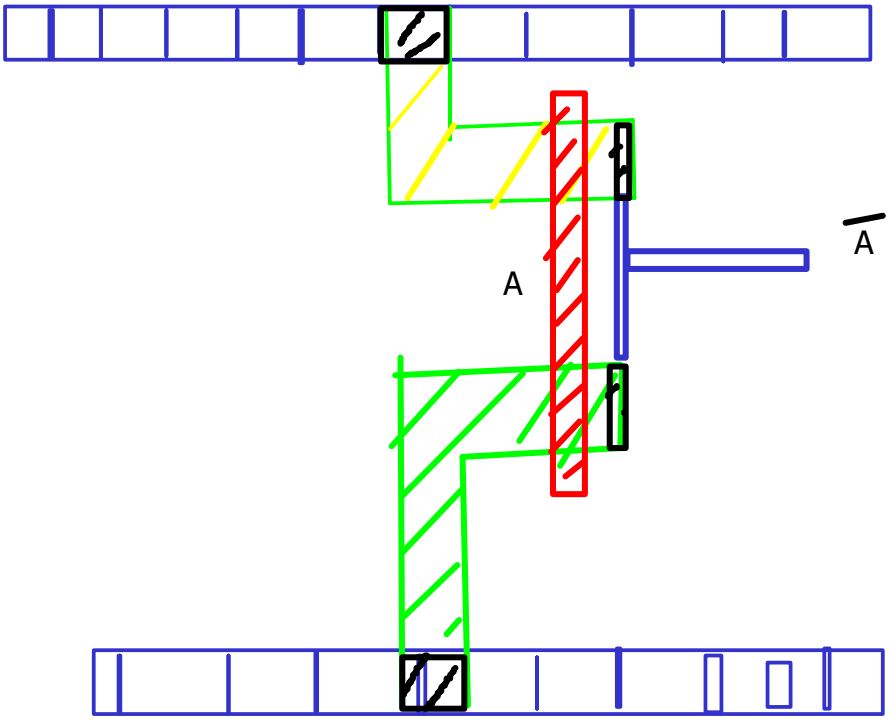
3. Spacing between Polysilicon and diffusion = 1 Lambda

4. Spacing between 2 metal -1 = 3 lambda

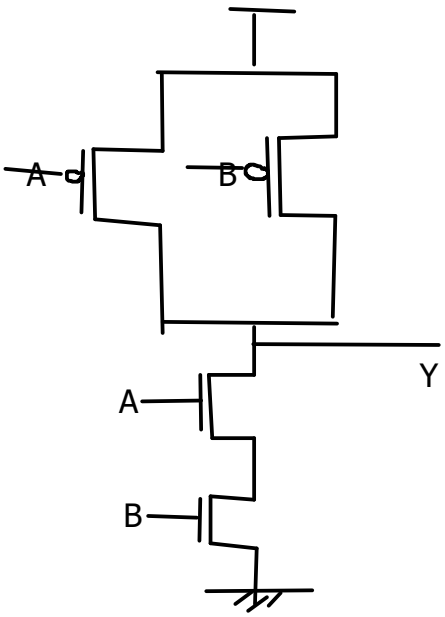
If the thickness and spacing between the layers is less than given value, then there exist an electrical contact between them.

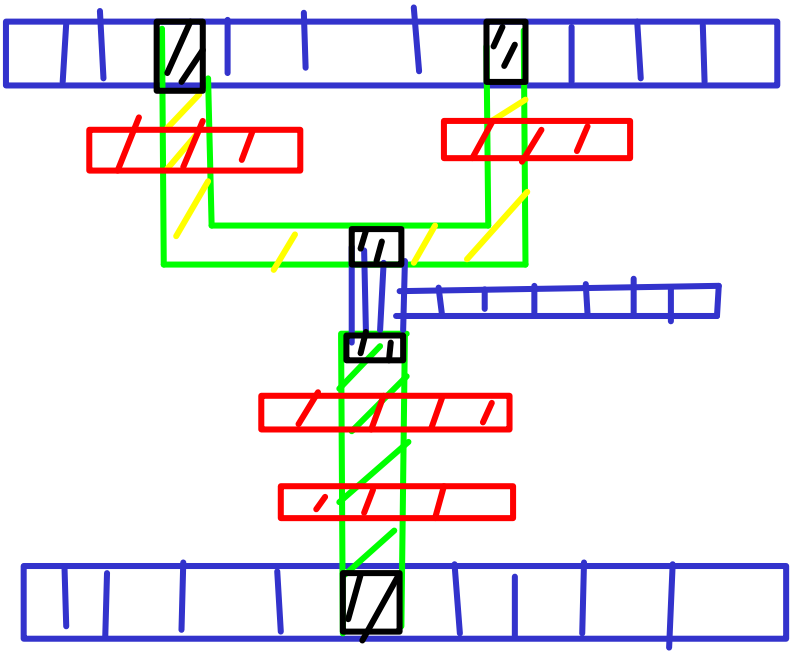
4th December, 2023

Layout design of CMOS Inverter



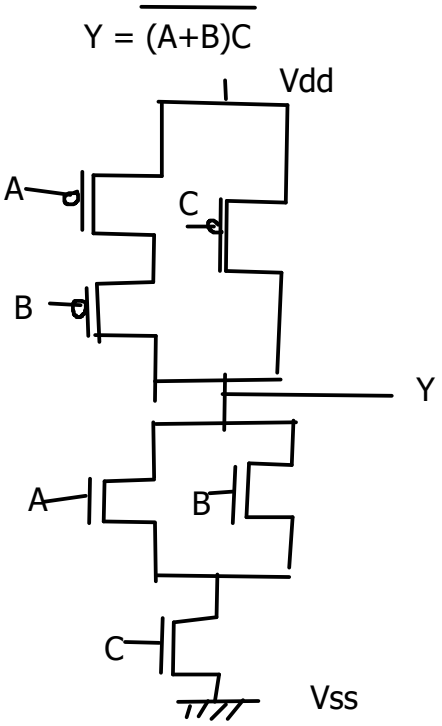
Layout Representation of Nand Gate

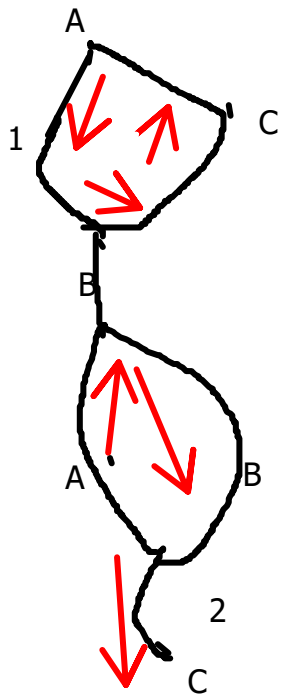




Stick diagram are constructed in few steps:

1) The first step is to construct a logic graph of schematic diagram.
   a) Identify each transistor by a unique name of its gate signal (A, B and C)
   b) Then identify each connections to the transistor by a unique name 1 and 2.





Euler Path {A,B, C}

2) The second step is to construct one euler path for both the pull up and pull down network.

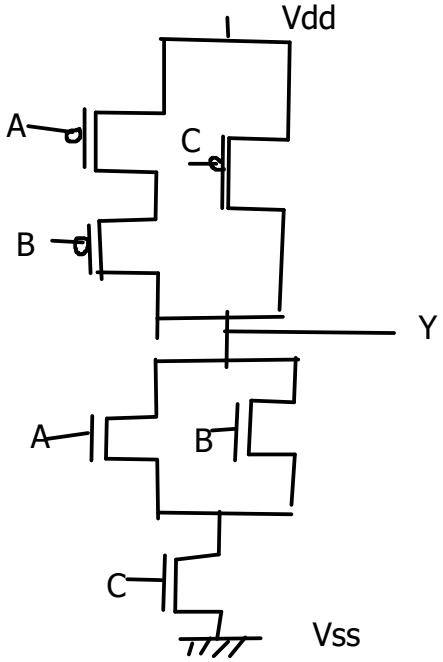
a) Euler paths are defined by a path that traverses each node in the path, such that each edge is visited only once.

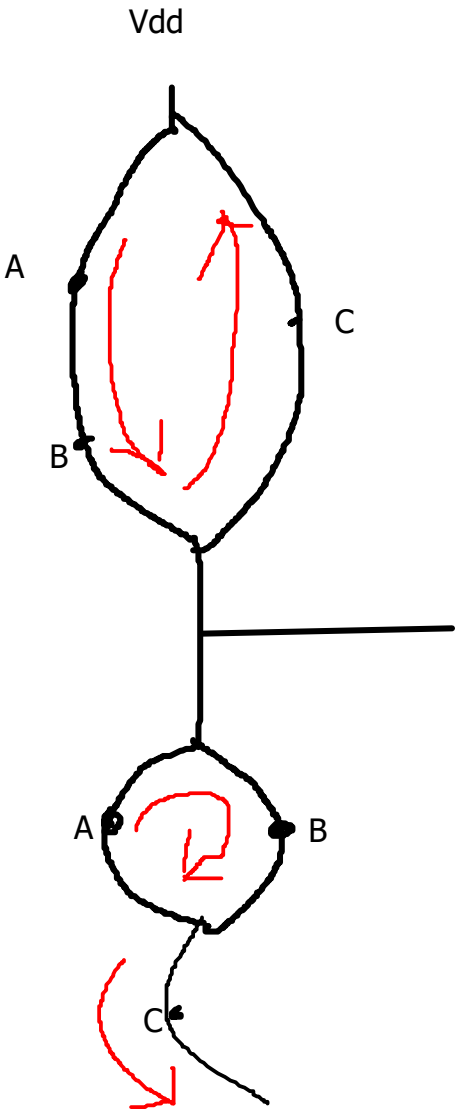
b) The path is defined by the order of each transistor name. If the path traverses transistor A then B then C, then the path name is {A,B,C}

c) The Euler path of the pull up network must be the same as the path of Pull down network.

3) After getting euler path , its time to layout the stick diagram.

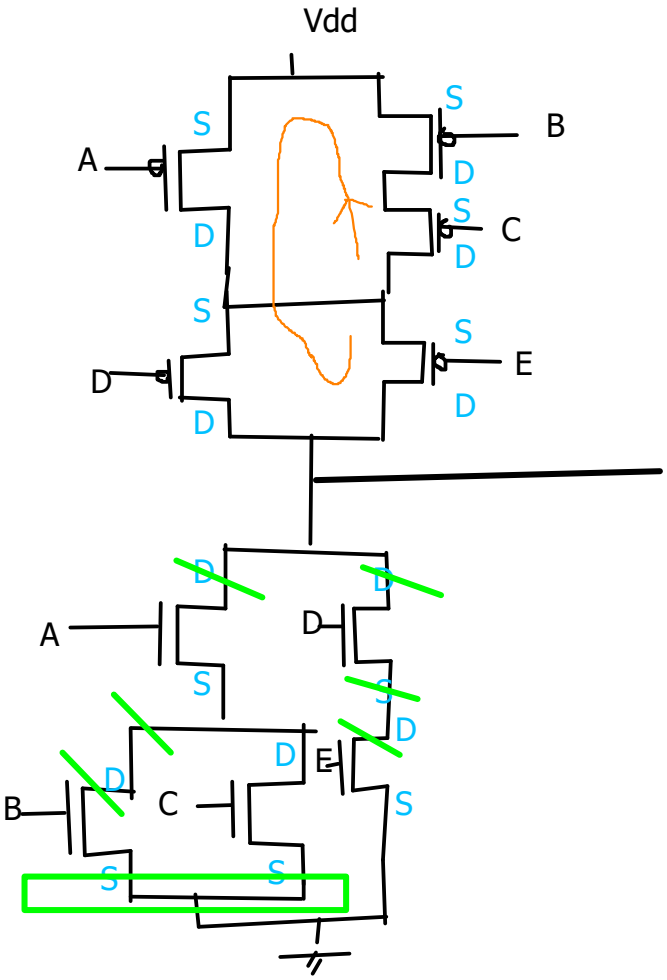
$Y = \overline{(A+B)C}$

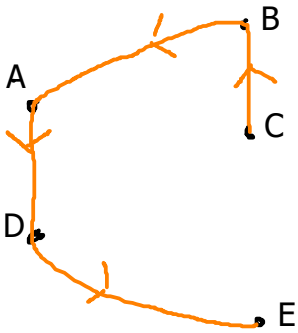




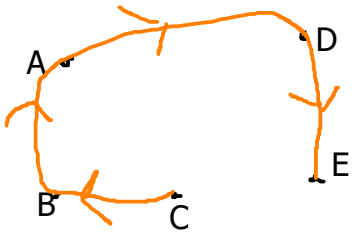
Draw the stick diagram for the Boolean function $Y = \overline{A(B+C)+D.E}$

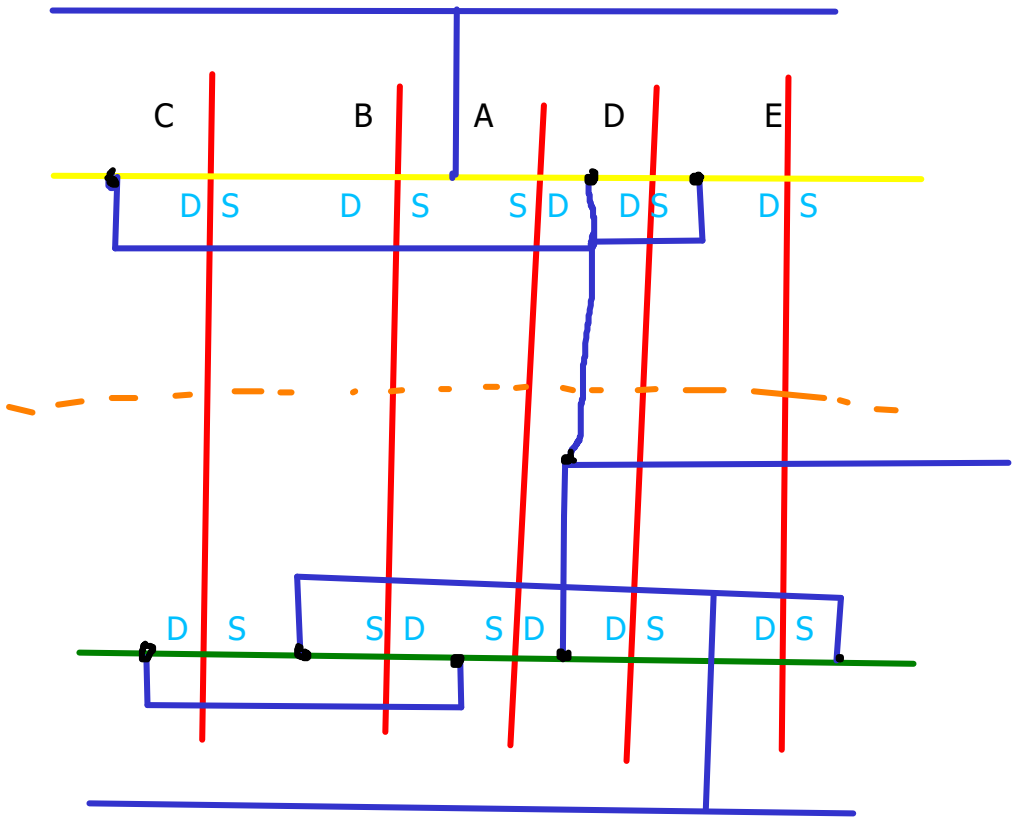
Schematic Diagram





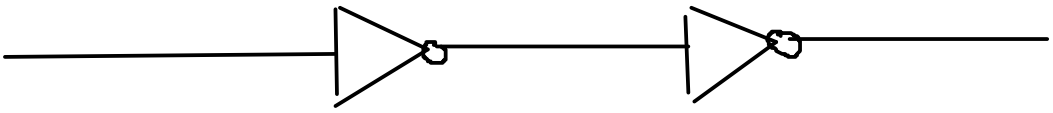
Euler Path
C-> B -> A -> D-> E





13th dec, 2023

Pull up to pull down ratio of nMos Inverter => 4:1

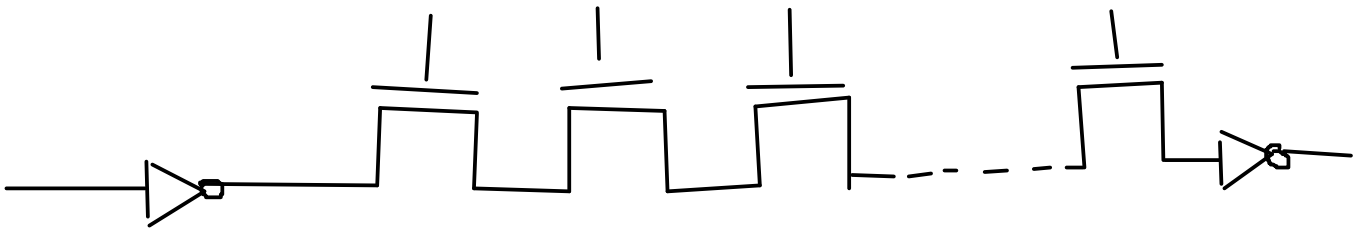


inv 1 invv 2

Z = L/ W

Z pu : Z pd = 4: 1 (Derivation already done in class)

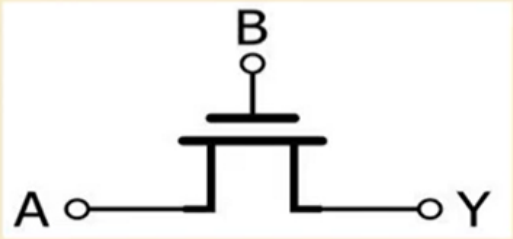
Pull up to pull down ratio for NMOS inverter driven through one or more pass transistor



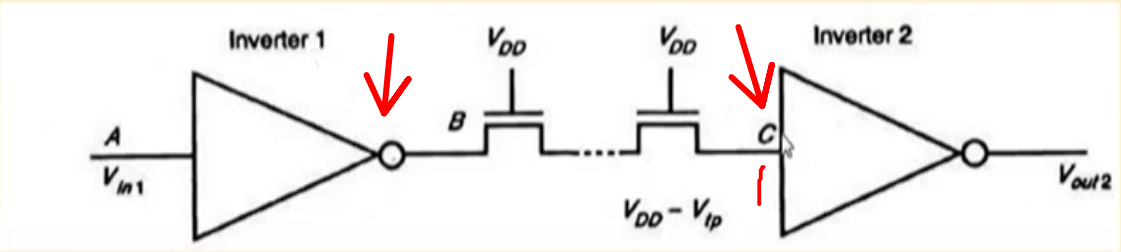
8:1 .

Pull -Up to Pull-Down ratio for an nMOS Inverter driven through one or more Pass Transistors

- **Pass Transistor:** The isolated nature of the gate allows the MOS transistors to be used as switches in series.
- This application of MOS transistor is called Pass Transistor, by which switching logic arrays are formed.

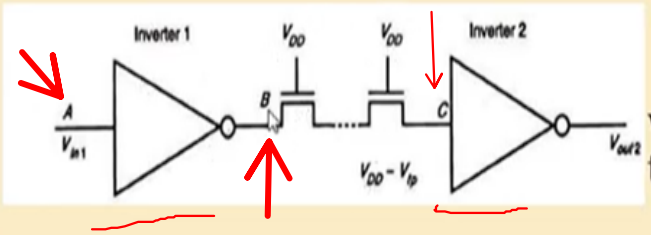


- Let us consider an arrangement in which the input to inverter 2 comes from the output of inverter 1, but passes through one or more nMOS transistors as shown in Fig. (These transistors are called pass transistors).



- The connection of pass transistors in series will degrade the logic 1 level into inverter 2 so that the output will not be a proper logic 0 level.

- The critical condition is , when point A is at 0 volts and B is thus at V_{DD}. but the voltage into inverter-2 at point C is now reduced from V_{DD} by the threshold voltage of the series pass transistor.



•Therefore, the input voltage to inverter-2 is

$$V_{in2} = V_{DD} - V_{tp}$$

where V_{tp} = threshold voltage for a pass transistor.

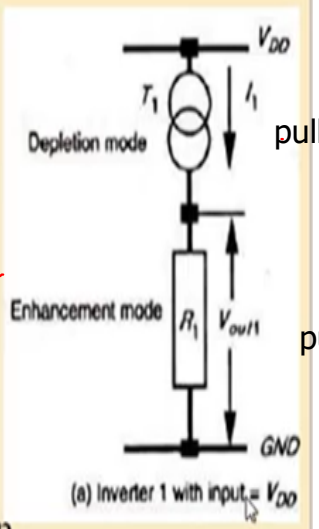
- Let us consider the inverter 1 with input = VDD. If the input is at V_{DD} , then the pull-down transistor T2 is conducting but with a low voltage across it; therefore, it is in its resistive region represented by R1 in Fig.(a) below. Meanwhile, the pull up transistor T1 is in saturation and is represented as a current source.

Vds = Ids x R1

- For Enhancement mode the pull down transistor :

$$I_{ds} = K\frac{W_{p.d.1}}{L_{p.d.1}}\left((V_{DD} - V_t)V_{ds1} - \frac{V_{ds1}^2}{2}\right)$$

$$R_1 = \frac{V_{ds1}}{I_{ds}} = \frac{1}{K}\frac{L_{p.d.1}}{W_{p.d.1}}\left(\frac{1}{V_{DD} - V_t - \frac{V_{ds1}}{2}}\right)$$



Since Vds is small, Vds1/2 can be neglected in the above expression.

$$R_1 \doteq \frac{1}{K}Z_{p.d.1}\left(\frac{1}{V_{DD} - V_t}\right) \quad \text{.....eq-1}$$

- Now, for depletion mode pull-up transistor in saturation with Vgs = 0

$$I_{ds} = K\frac{W}{L}\frac{(V_{gs} - V_t)^2}{2}$$ ....(in saturation region)

$$I_1 = I_{ds} = K\frac{W_{p.u.1}}{L_{p.u.1}}\frac{(-V_{td})^2}{2}$$ eq-2

The product of eq 1 & 2 gives V_{out1}

$$V_{out1} = I_1 R_1 = \frac{Z_{p.d.1}}{Z_{p.u.1}}\left(\frac{1}{V_{DD} - V_t}\right)\frac{(V_{td})^2}{2}$$ eq-3

V = I R

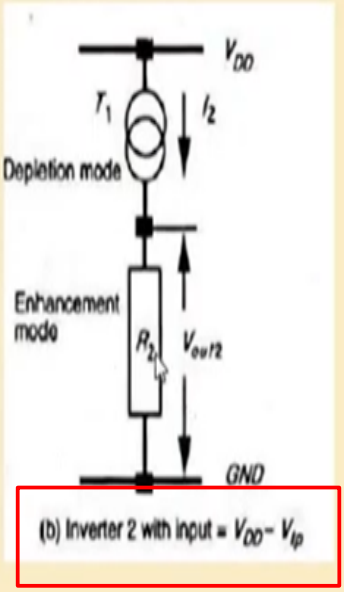
- Consider inverter-2, when input $V_{DD} = V_{DD} - V_{tp}$

$R2 = Vds2/Ids2$

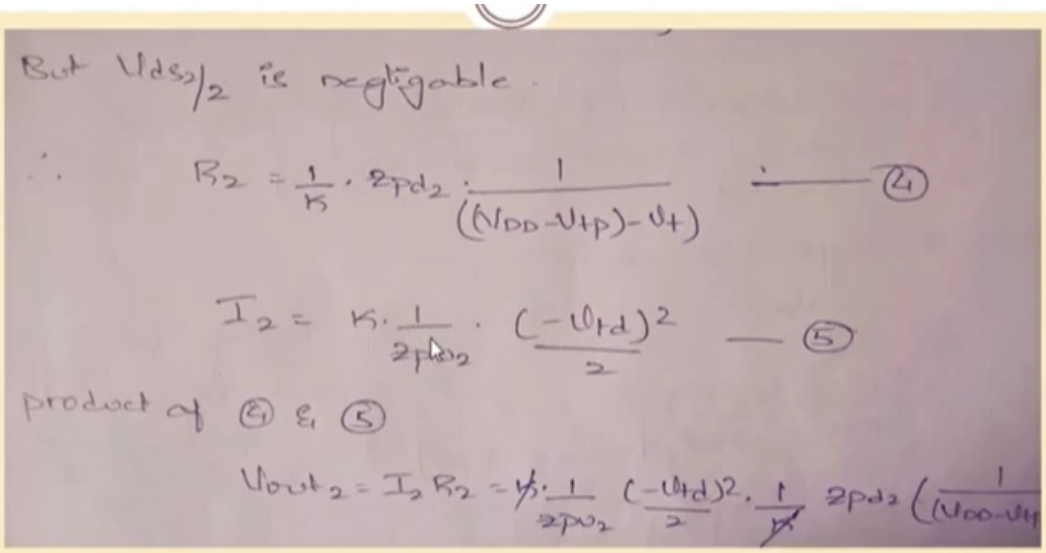
$$I_{ds2} = K\cdot\frac{W_{pd2}}{L_{pd2}}\left[(V_{DD} - V_{tp} - V_t) - \frac{V_{ds}}{2}\right]V_{ds}$$

$$\therefore R_2 = \frac{V_{ds2}}{K\cdot\frac{W_{pd2}}{L_{pd2}}\left[(V_{DD} - V_{tp} - V_t) - \frac{V_{ds2}}{2}\right]V_{ds2}}$$

But $V_{ds2}/2$ is negligable.



(b) Inverter 2 with input = $V_{DD} - V_{tp}$



$$V_{out2} = I_2 R_2 = \frac{Z_{p.d.2}}{Z_{p.u.2}} \left(\frac{1}{V_{DD} - V_{tp} - V_t} \right) \frac{(-V_{td})^2}{2} \quad \text{.....eq-6}$$

- If inverter-2 is to have the same output voltage under these conditions then $V_{out1} = V_{out2}$. That is $I_1R_1 = I_2R_2$

$$V_{out1} = I_1 R_1 = \frac{Z_{p.d.1}}{Z_{p.u.1}} \left(\frac{1}{V_{DD} - V_t} \right) \frac{(V_{td})^2}{2} = V_{out2} = I_2 R_2 = \frac{Z_{p.d.2}}{Z_{p.u.2}} \left(\frac{1}{V_{DD} - V_{tp} - V_t} \right) \frac{(-V_{td})^2}{2}$$

$$\frac{Z_{p.u.2}}{Z_{p.d.2}} = \frac{Z_{p.u.1}}{Z_{p.d.1}} \frac{(V_{DD} - V_t)}{(V_{DD} - V_{tp} - V_t)} \quad \text{.....eq-7}$$

- Now, consider the typical values, V_{DD}=1.0

$$V_t = 0.2V_{DD}$$

$$V_{tp} = 0.3V_{DD}^*$$

$$\frac{Z_{p.u.2}}{Z_{p.d.2}} = \frac{Z_{p.u.1}}{Z_{p.d.1}} \frac{0.8}{0.2}$$

- Therefore

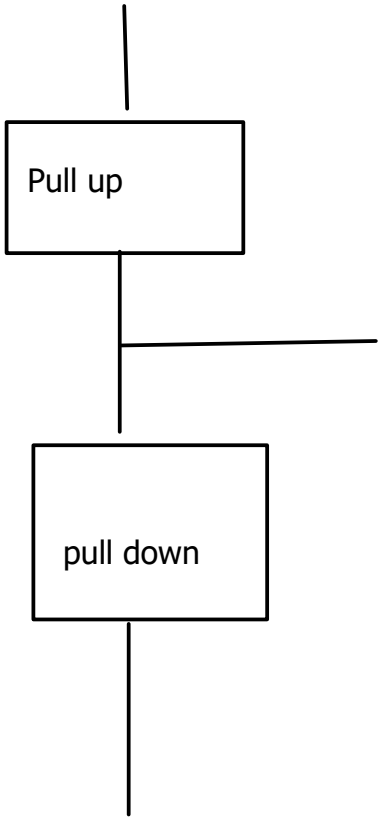
$$\frac{Z_{p.u.2}}{Z_{p.d.2}} \div 2 \frac{Z_{p.u.1}}{Z_{p.d.1}} = \frac{8}{1}$$

From the above theory it is clear that, for an n-MOS transistor
(i). An inverter driven directly from the output of another should have a Zp.u/ Zpd. ratio of ≥ 4/1.
(ii).An inverter driven through one or more pass transistors should have a Zp.u./Zp.d ratio of ≥8/1

Final Syllabus

1. CMOS Fabrication
2. Stick Diagram
3. Design rules and Layout
4. Lambda based design rule
5. CMOS inverter (different ways) ct2
6. NOT, Nand, different boolean expressions, SR Latch ct2
7. CMOS Multiplexer, CMOS Half Adder -> ct2
8. pull up to pull down ratio of nmos inverter
9. Voltage transfer Characteristics of CMOS inverter (5 regions) -> ct2

========= END OF VLSI COURSE ========



In pull up,
we can use
1) Resistor as a load
2) NMOS (dep)
3) NMOS (enh)
4) PMOS transistor

In pull down -> enhancement mode NMOS transistor