Computer Architecture (CSE-2207)

Cpu Organization: Instruction formats

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August 22, 2023

Instruction Formats and ALU

- → Instruction formats are based on how ALU executes instructions.
- → ALU takes operands as inputs to perform execution of instructions.
- → Operands may be there in Registers or in Memory, based on that instructions formats are there with different computers.



Stack CPU

- → In Stack CPU, ALU operations are performed on stack data only.
- → So, both operands of ALU are always there on stack only.
- → Stack works as per Last In First Out (LIFO).
- → Default address of operand becomes Top of Stack.
- → So here, No address is required in instruction format with stack CPU.
- → So instruction Format includes only Opcode.
- → In Stack Insertion and deletion takes place at the same time.

Accumulator CPU

- → In Accumulator CPU, one operand always stored in Accumulator.
- → So, second operand may be any general purpose register or Memory.
- → After arithmetic or Logical operation answer will be stored in Accumulator.
- → As one operand is Accumulator, in instruction we need address of second operand only.
- → So basic instruction format is



Accumulator based Architecture (From any where (in CPU) ALU ADD R3 ACC + AC+R3

General Purpose CPU

- → In this type of CPU, operands may be there in register or in memory.
- → If operands are there in register then CPU will be having more registers.
- → If operands are there in memory then CPU will be having less registers.
- → So basic instruction format is

OPCODE OPER	ND 1 OPERAND 2
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Instruction Format

Instruction Format Type	Instruction Format	Example
Zero Address Instruction	MODE OPCODE	CMA CME
One Address Instruction	MODE OPCODE OPERAND	ADD 06H LDA 20H
Two Address Instruction	MODE OPCODE OPERAND1 OPERAND2	MOV R1, R2 ADD AX, BX
Three Address Instruction	MODE OPCODE OPERAND1 OPERAND2 OPERAND3	ADD R1 , R2 , R3 SUB R1 , R2 , R3

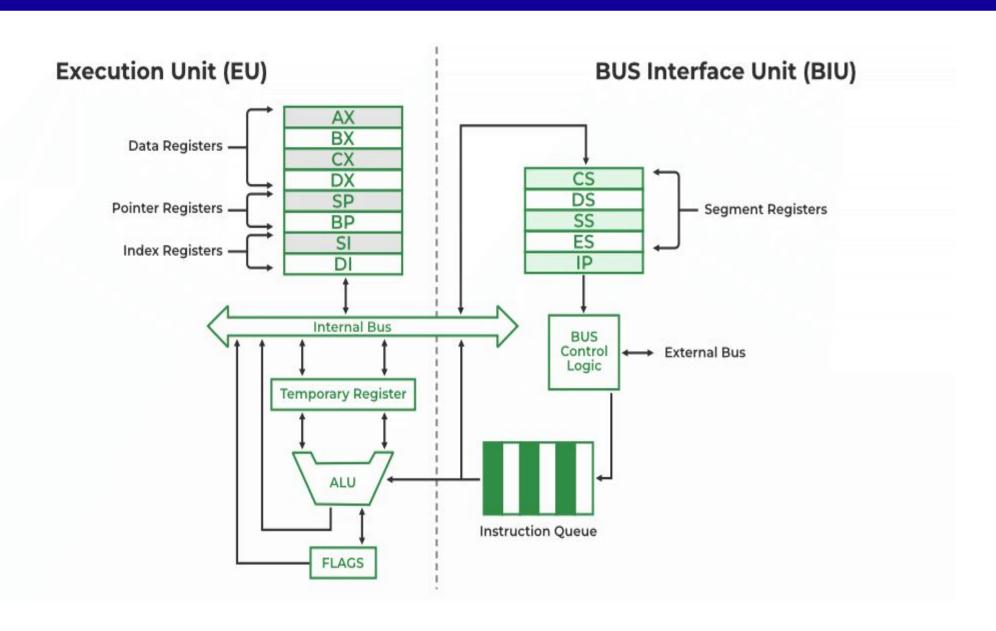
Example

A Processor has 512 distinct instructions and 80 general purpose registers. A 24 bits instruction word has an opcode, one register operand and a memory operand. How many bits are reserved for the memory operand field?

A Processor has 40 distinct instructions and 24 general purpose registers. A 32 bits instruction word has an opcode, two register operands and an immediate operand. The numbers of bits available for the immediate operand is _____?

A Machine has 24 bits instruction format. It has 32 registers and each of which is 32 bits long. It needs to support 49 instructions. Each instruction has two register operands and one immediate operand. If the immediate operand is signed integer, the minimum value of immediate operand is

General Purpose Register



THANK YOU