VLSI Design (CSE-4411)

MOSFET

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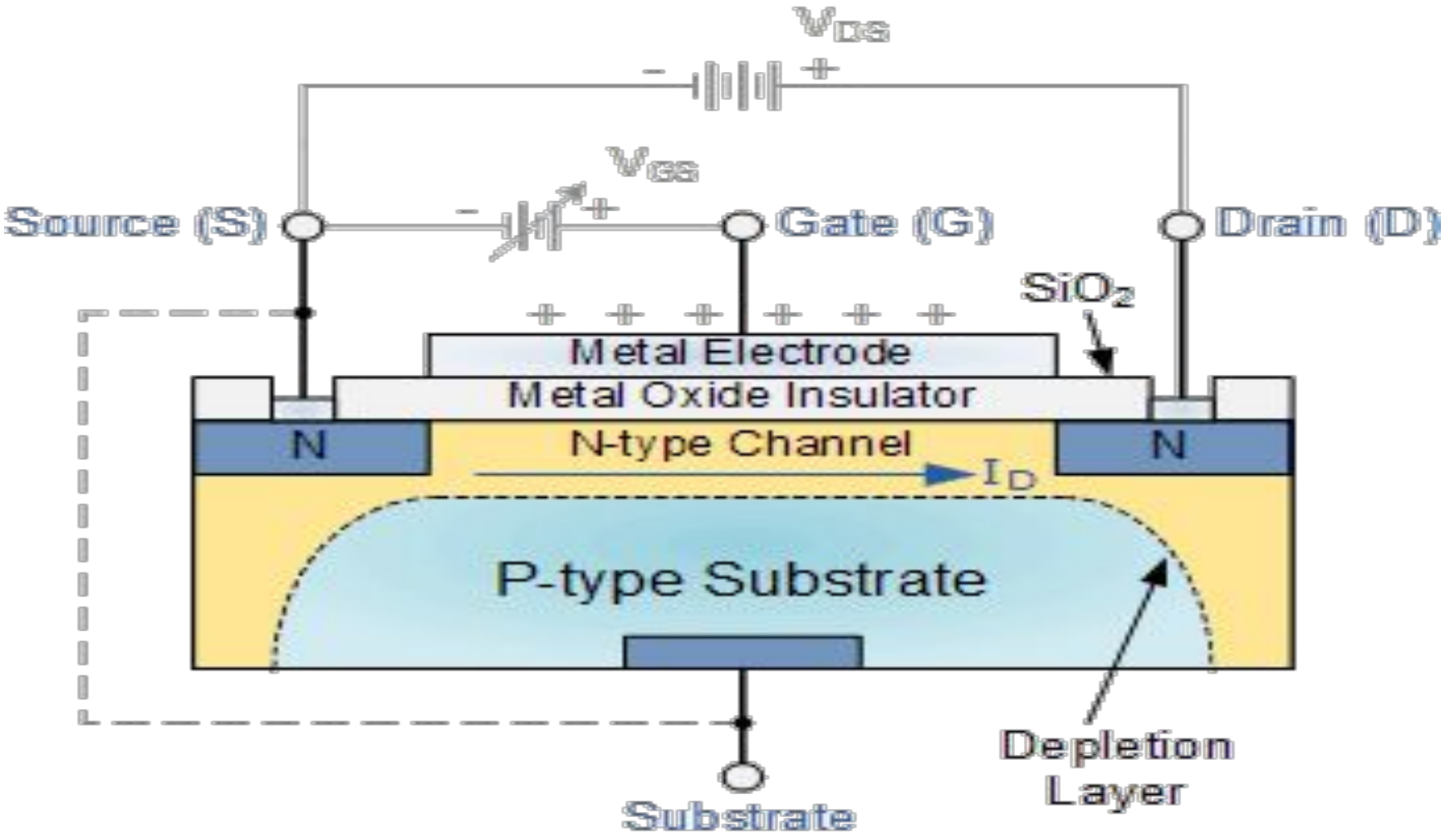
MOSFET


V_{DS}
V_{GS}
Source (S)
Gate (G)
Drain (D)
SiO_2
Metal Electrode
Metal Oxide Insulator
N
N-type Channel
N
I_D
P-type Substrate
Depletion Layer
Substrate

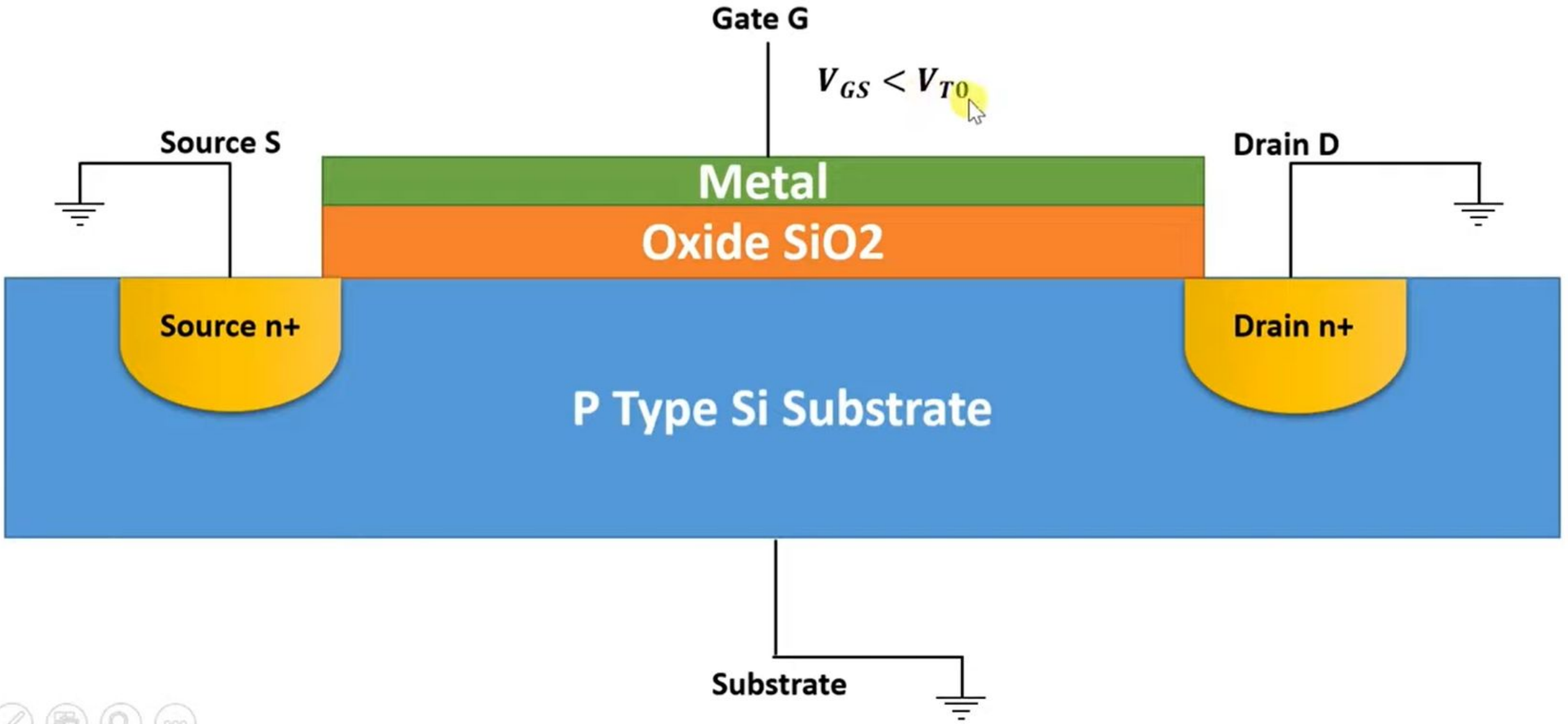
Types of MOS Transistor

There are two types of MOS transistor based on channel.

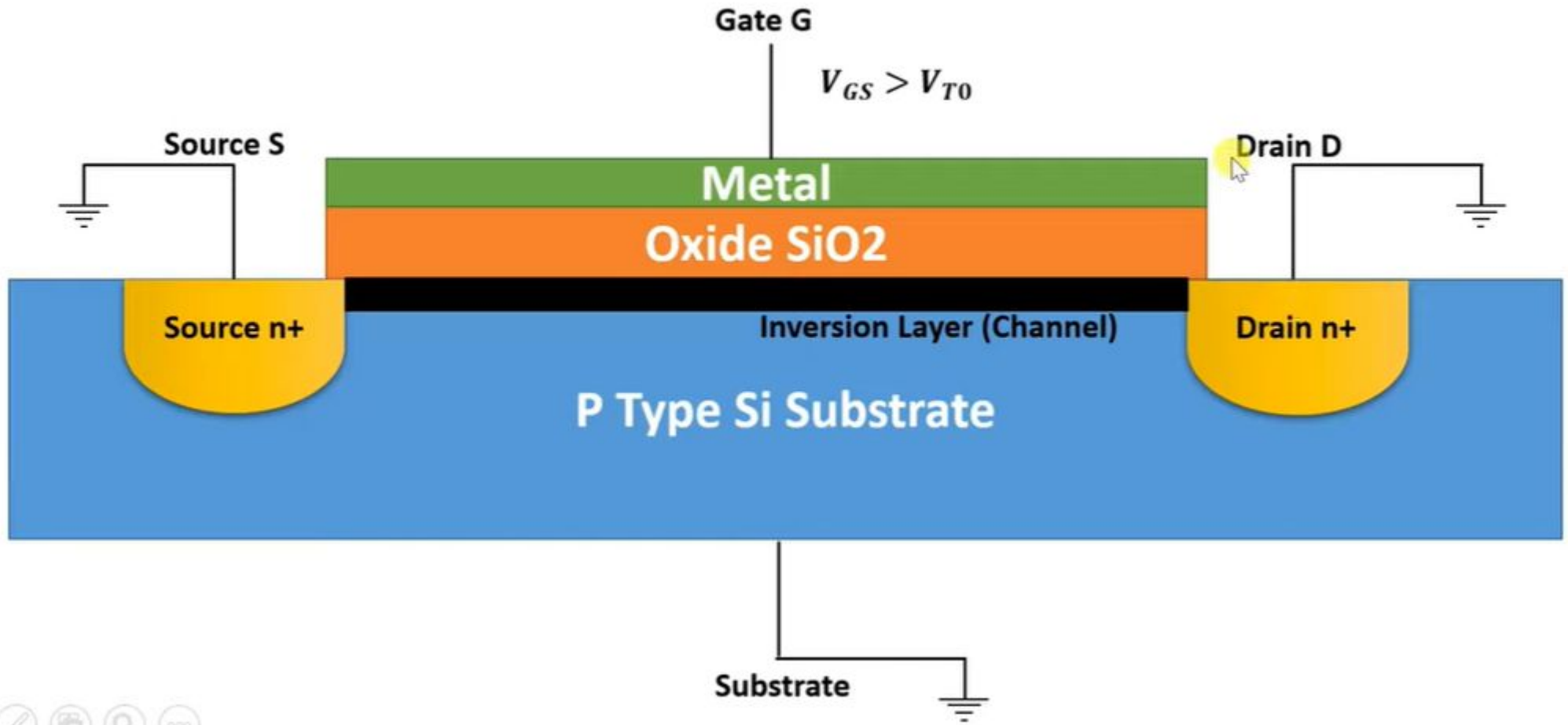
Enhancement type MOS Transistor : It has no conducting channel region at zero gate bias voltage.

Depletion type MOS Transistor : It has conducting channel region at zero gate bias voltage.

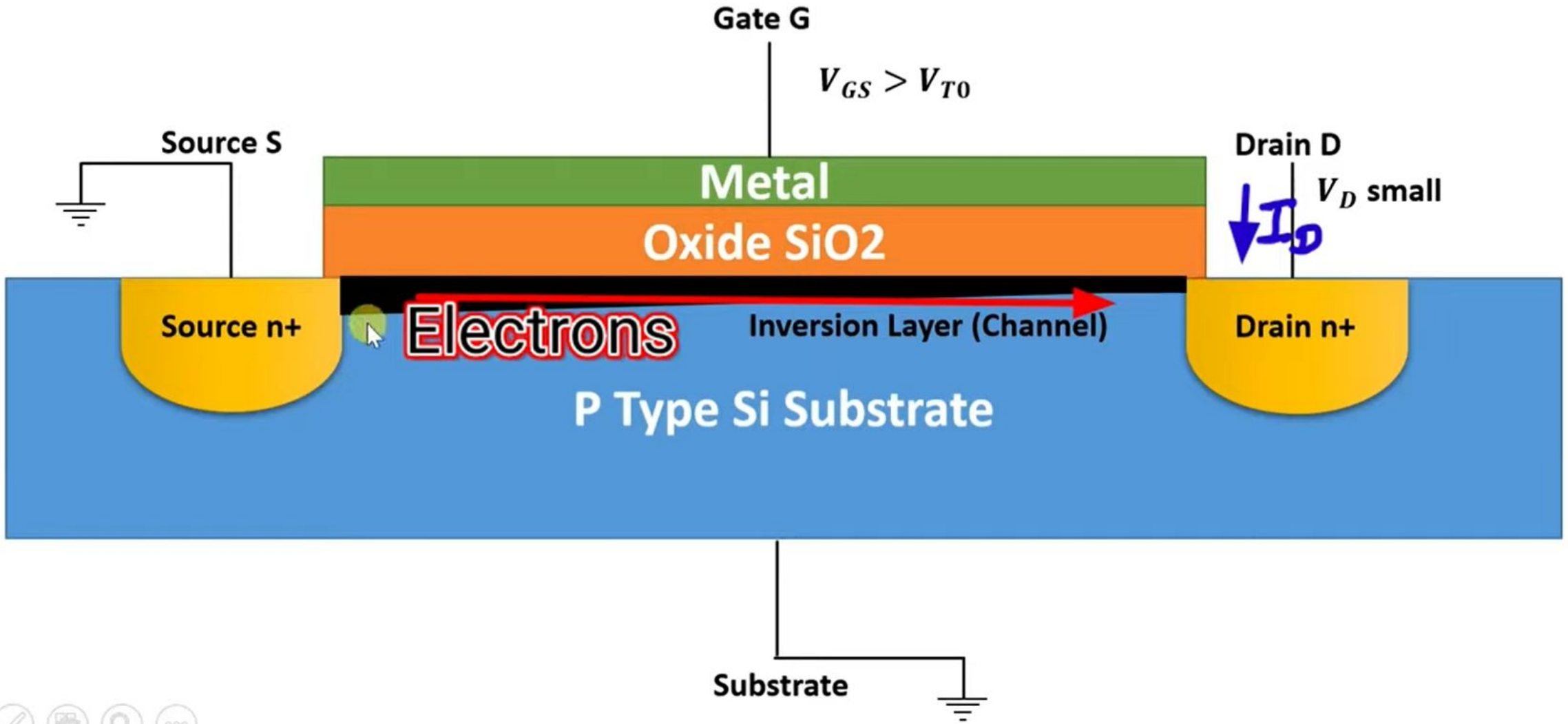
Working of n channel in cut off region



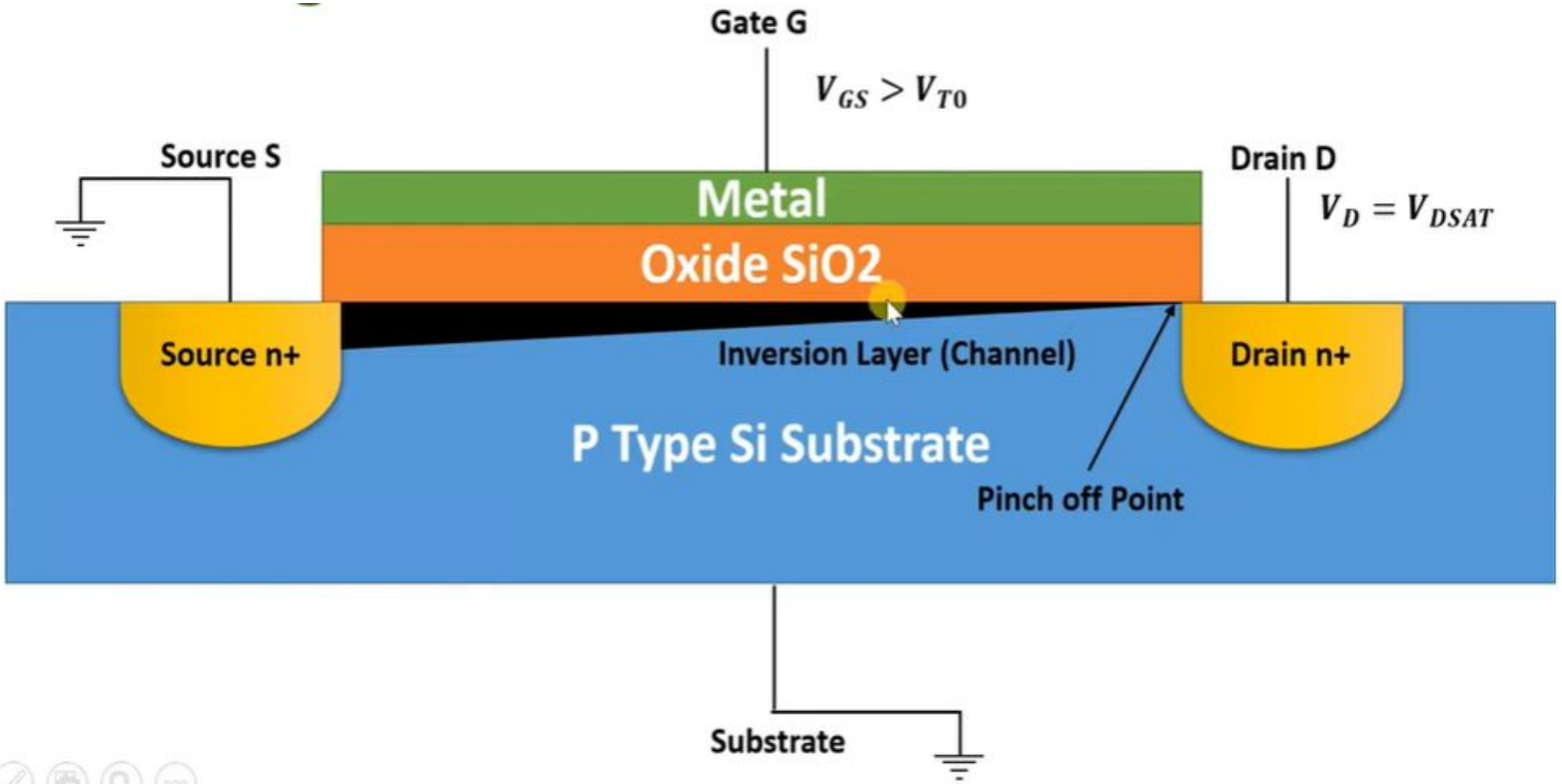
Working of n channel in cut off region



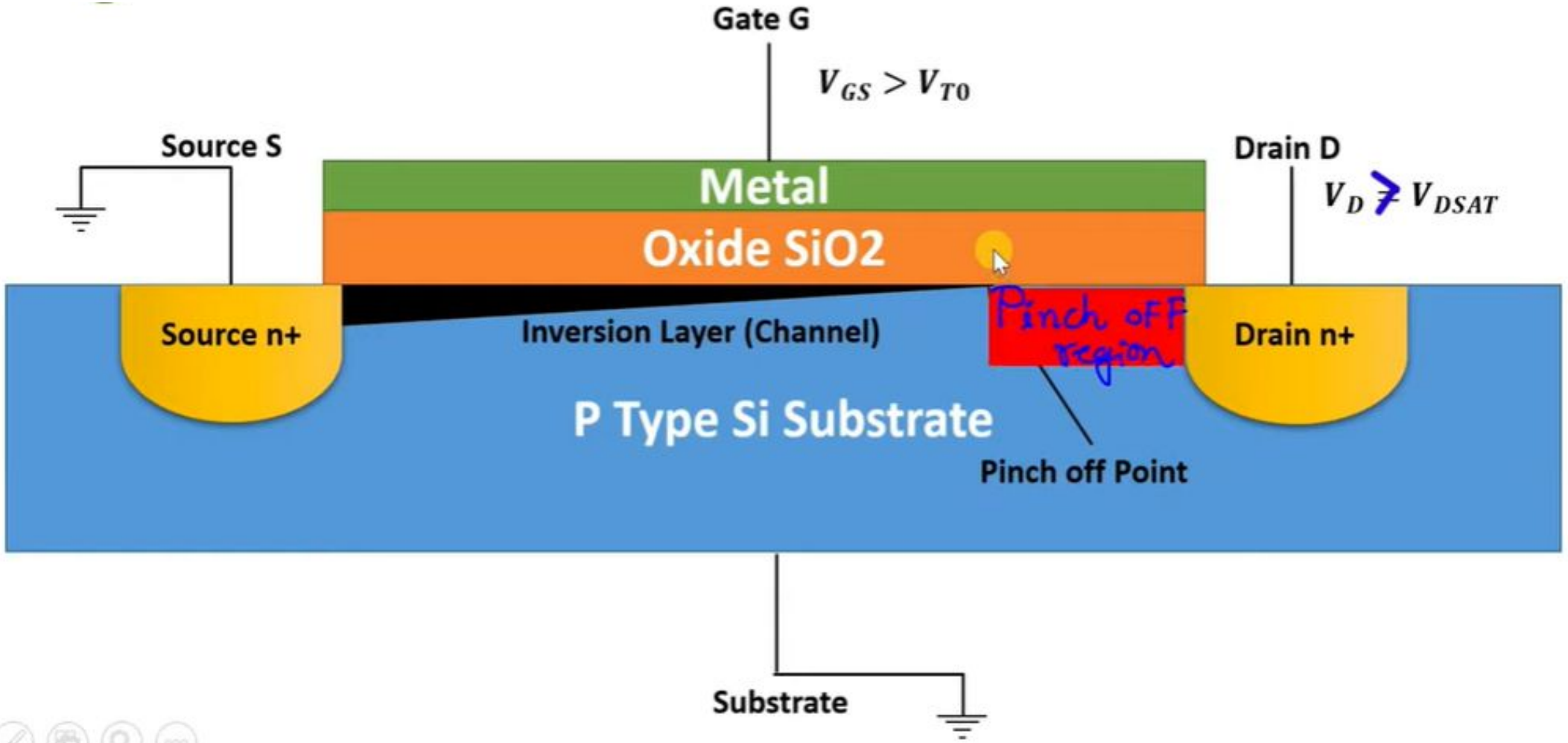
Working of n channel in linear region



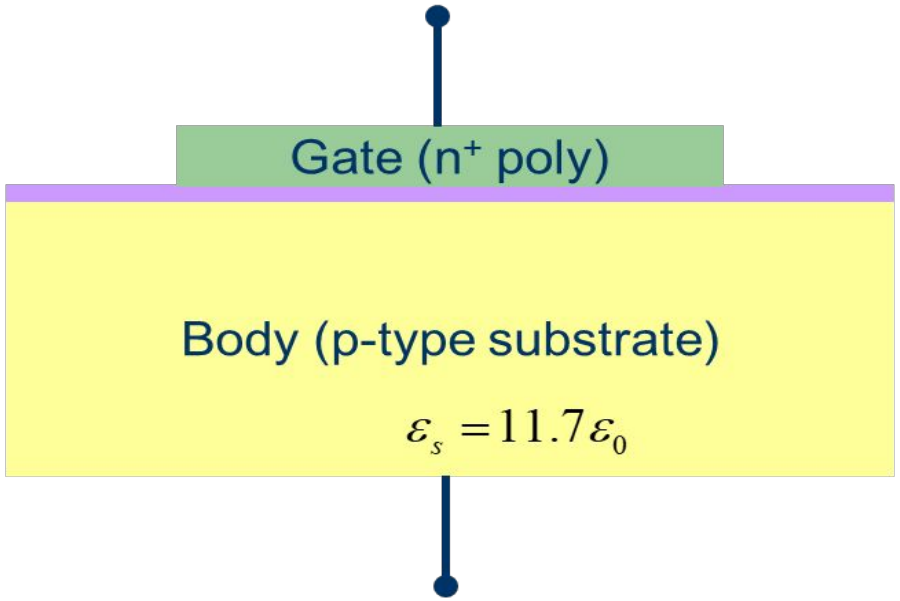
Working of n channel in linear region



Working of n channel in saturation region



MOS Capacitor



Oxide (SiO_2)

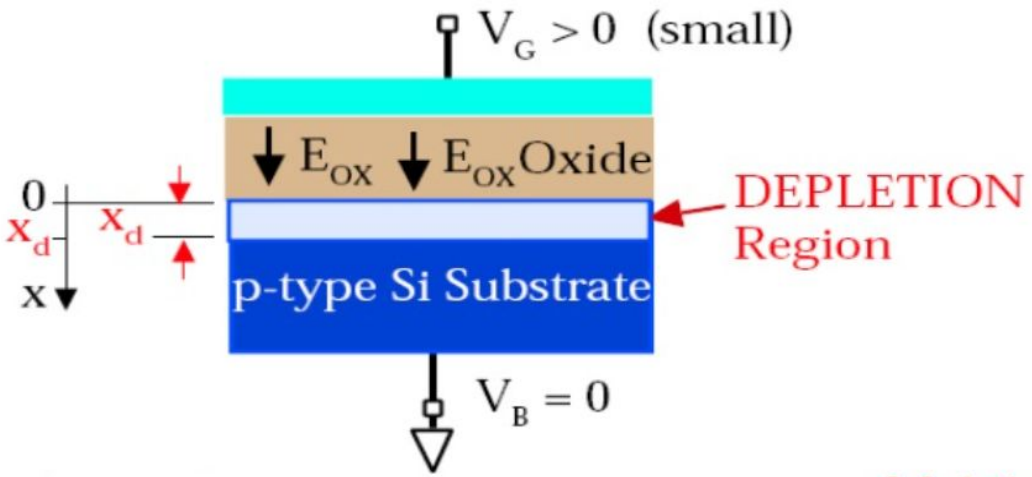
$\varepsilon_{ox} = 3.9\varepsilon_0$

Very Thin!

$t_{ox} \sim 1\text{nm}$

- MOS = Metal Oxide Silicon
- Sandwich of conductors separated by an insulator
- "Metal" is more commonly a heavily doped polysilicon layer n^+ or p^+ layer
- NMOS → p-type substrate, PMOS → n-type substrate

Depletion Region Charge



$$dQ = -qN_A dx$$

Mobile charge in thin layer parallel to Si surface

$$d\phi = -\frac{x}{\varepsilon_{Si}} dQ = x\frac{qN_A}{\varepsilon_{Si}} dx$$

Change in surface potential to displace dQ

$$\int_{\phi_s}^{\phi_F} d\phi = \int_0^{x_d} x\frac{qN_A}{\varepsilon_{Si}} dx \rightarrow \phi_F - \phi_s = \frac{qN_A}{2\varepsilon_{Si}} x_d^2$$

$$x_d = \sqrt{\frac{2\varepsilon_{Si}|\phi_F - \phi_s|}{qN_A}}$$

Depletion Region Charge

$$Q = -qN_A x_d = -\sqrt{2qN_A\varepsilon_{Si}|\phi_F - \phi_s|}$$

N_A = Acceptor impurity
E_{si} = permittivity of Silicon

Components of Threshold Voltage

Components of Threshold Voltage:

- Work function difference between gate and channel
- Gate voltage component to change surface potential
- Gate voltage component to offset depletion region charge
- Voltage component to offset fixed charges in gate oxide and silicon oxide interface

Threshold Voltage Calculation

- Work function difference ϕ_{GC} in between the gate and the channel is given by

$$\phi_{GC} = \phi_F(Substrate) - \phi_M(Metal)$$

$$\phi_{GC} = \phi_F(Substrate) - \phi_F(Gate\ polysilicon)$$

- For surface inversion, surface potential should change form ϕ_F to $-\phi_F$. So net change will be $-\phi_F - (\phi_F) = -2\phi_F$.
- When voltage is applied at gate, it repelled holes deeper inside substrate, and it forms depletion region. This region has ions which forms offset voltage due to charges of ions near the surface.
- So depletion region charge density at surface inversion ($\phi_S = -\phi_F$) is given by

$$Q_{BO} = -\sqrt{2qN_A\varepsilon_{Si}|-2\phi_F|}$$

- If substrate bias is given with V_{SB} then depletion region charge density is given by

$$Q_B = -\sqrt{2qN_A\varepsilon_{Si}|-2\phi_F + V_{SB}|}$$

- So, the component of voltage which nullify the value will be $-Q_B/C_{OX}$, where C_{OX} is gate oxide capacitance per unit area.
- There is also fixed positive charge density Q_{OX}, it is due to lattice imperfections at the interface.
- So the forth component for threshold voltage will be $-Q_{OX}/C_{OX}$.
- So, for zero substrate bias, threshold voltage is given by

$$V_{TO} = \phi_{GC} - 2\phi_F - \frac{Q_{BO}}{C_{OX}} - \frac{Q_{OX}}{C_{OX}}$$

- For non zero substrate bias, threshold voltage is given by

$$V_T = \phi_{GC} - 2\phi_F - \frac{Q_B}{C_{OX}} - \frac{Q_{OX}}{C_{OX}}$$

$$V_T = \phi_{GC} - 2\phi_F - \frac{Q_{BO}}{C_{OX}} - \frac{Q_{OX}}{C_{OX}} - \frac{Q_B - Q_{BO}}{C_{OX}}$$

$$V_T = V_{TO} - \frac{Q_B - Q_{BO}}{C_{OX}}$$

- Here,

$$\frac{Q_B - Q_{BO}}{C_{OX}} = \frac{-\sqrt{2qN_A\varepsilon_{Si}}}{C_{OX}}\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

- So Threshold voltage is given by

$$V_T = V_{TO} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

- Where, ϒ is substrate bias or body effect coefficient $\gamma = \frac{\sqrt{2qN_A\varepsilon_{Si}}}{C_{OX}}$

Threshold Voltage Calculation

$$V_{T0} = \Phi_{GC} - 2\phi_{F(sub)} - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

Q_{B0}:

$$Q_{B0} = -\sqrt{2qN_A\varepsilon_{Si}|2\phi_{F(sub)}|}$$

$$= -\sqrt{2(1.6\text{x}10^{-19}\,\text{C})(10^{16}\,\text{cm}^{-3})(1.06\text{x}10^{-12}\,\text{Fcm}^{-1})|2\text{x}0.35\text{V}|}$$

F = C/V

$$= -4.87 \text{ x } 10^{-8}\,\text{C/cm}^2$$

C_{ox}:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{0.34\text{x}10^{-12}\,\text{Fcm}^{-1}}{500\text{x}10^{-8}\,\text{cm}} = 6.8\text{x}10^{8}\,\text{F/cm}^2$$

Q_{ox}:

$$Q_{ox} = qN_{ox} = (1.6\text{x}10^{-19}\,\text{C})(4\text{x}10^{10}\,\text{cm}^{-2}) = 6.4\text{x}10^{-9}\,\text{C/cm}^2$$

$$\frac{Q_{B0}}{C_{ox}} = \frac{-4.87\text{x}10^{8}\,\text{C/cm}^2}{6.8\text{x}10^{8}\,\text{F/cm}^2} = -0.716\,\text{V} \qquad \frac{Q_{ox}}{C_{ox}} = \frac{6.4\text{x}10^{-9}\,\text{C/cm}^2}{6.8\text{x}10^{8}\,\text{F/cm}^2} = 0.094\,\text{V}$$

$$V_{T0} = -0.95\text{V} - (-0.70\,\text{V}) - (-0.72\,\text{V}) - (0.09\,\text{V}) = 0.38\text{V}$$

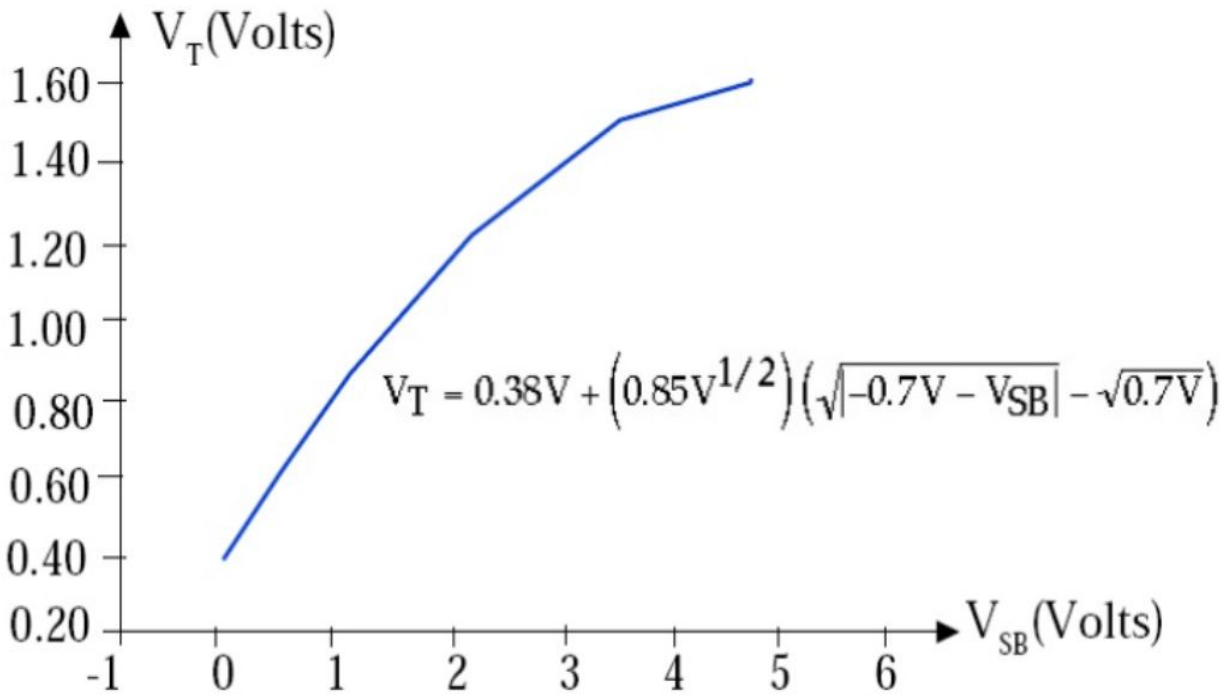
Threshold Voltage Body Bias Example

$$V_T = V_{T0} + \gamma\left(\sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

where

$$V_{T0} = 0.38V$$

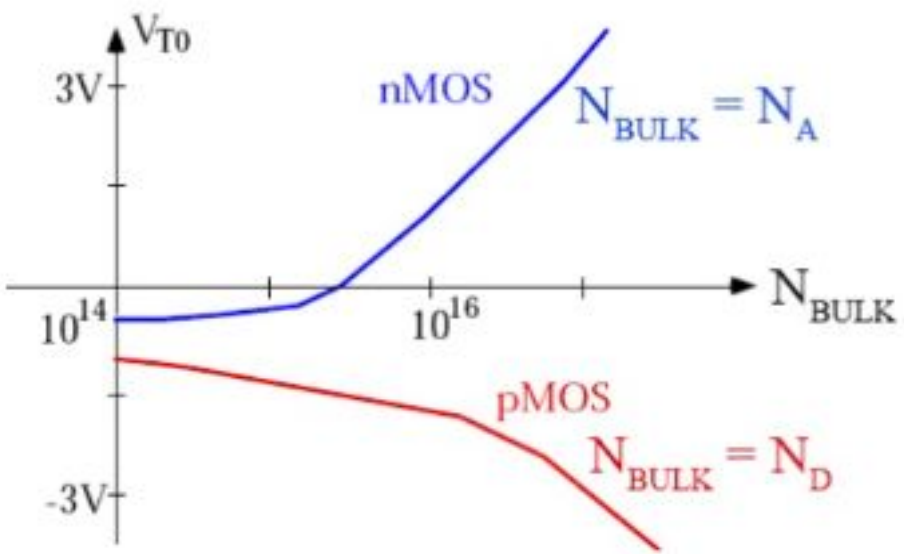
$$\gamma = 0.85V^{1/2}$$

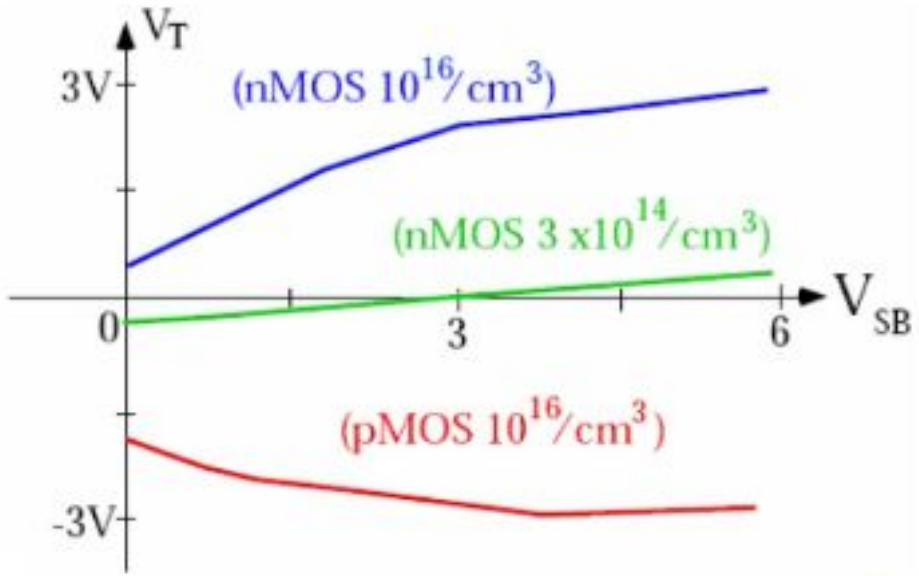


Threshold Voltage for MOS Transistor

n-channel -> p-channel

- ϕ_F is negative in nMOS, positive in pMOS
- Q_{B0}, Q_B are negtive in nMOS, positive in pMOS
- γ is positive in nMOS, negative in pMOS
- V_{SB} is positive in nMOS, negative in pMOS





Textbook and readings

- **CMOS VLSI Design: A Circuits and Systems Perspective**
  - **Book by David Harris and Neil Weste**

THANK YOU