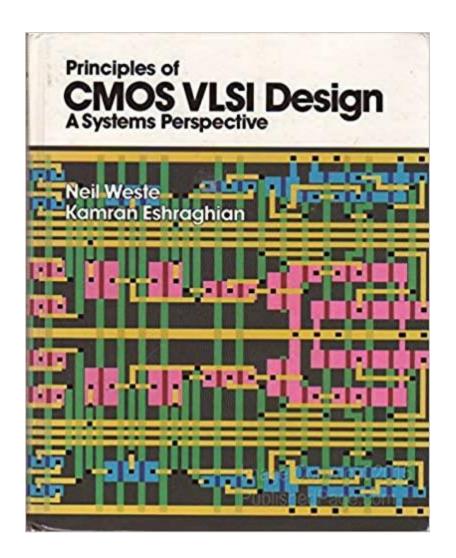
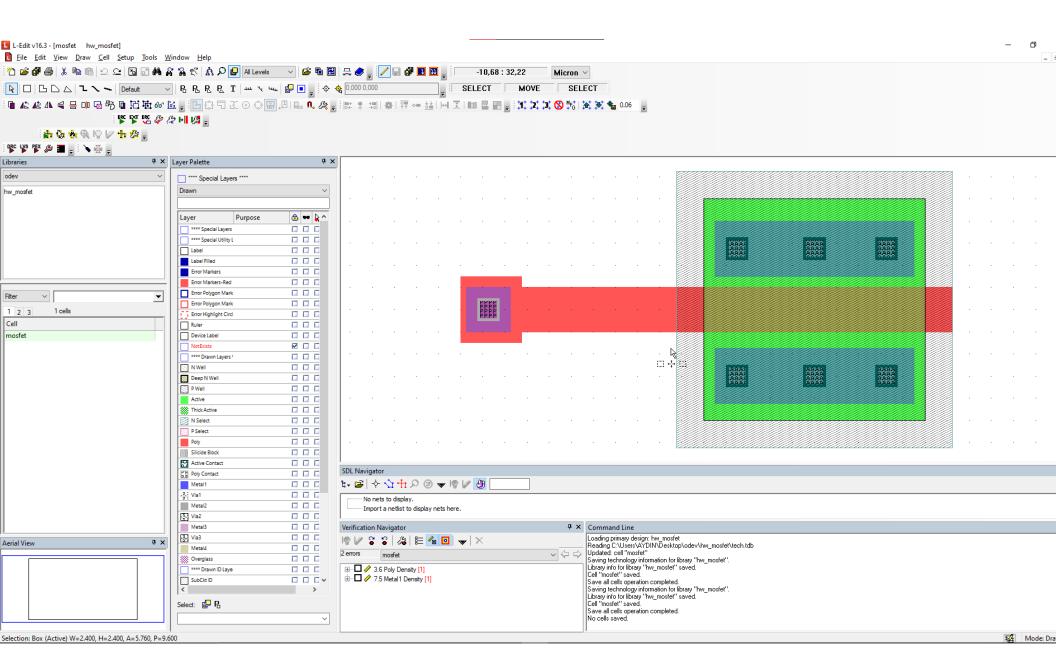
VLSI Design Assigment in L-Edit

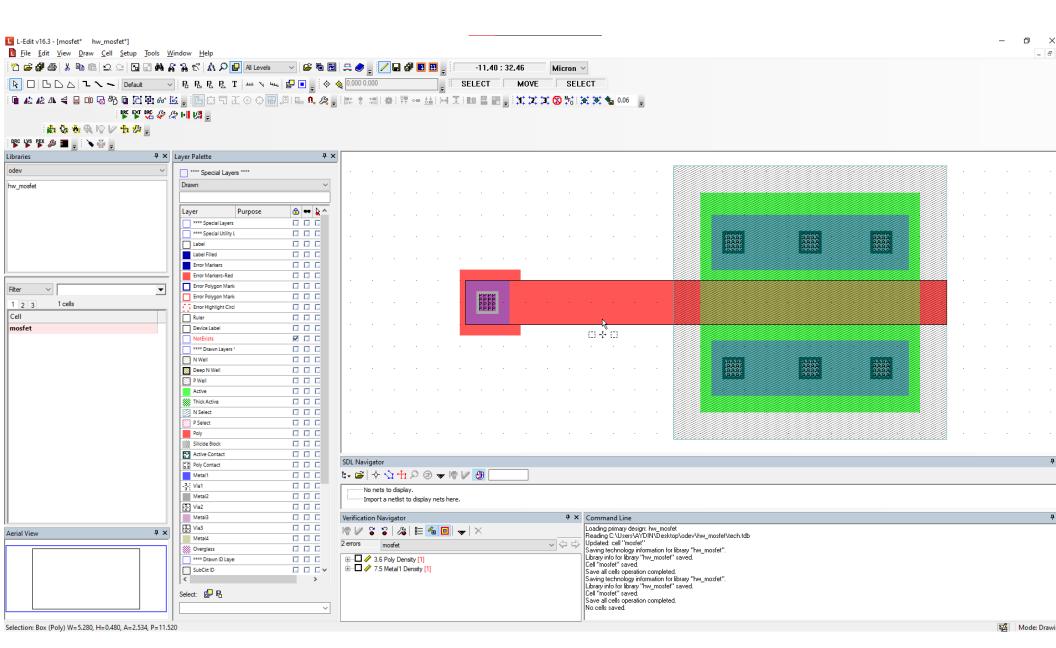


INTRODUCTION TO ENGINEERING APPLICATIONS

Prof. Dr. Alp Oral Salman Prof. Dr. Ali Tangel

Ahmed Göktuğ Aydın - 200208054





```
******************************
* SPICE netlist generated by HiPer Verify's NetList Extractor
* Extract Date/Time: Thu Apr 22 15:37:42 2021
* L-Edit Version: L-Edit Win64 16.30.20150626.05:33:01
* Rule Set Name:
* TDB File Name: C:\Users\AYDIN\Desktop\hw mosfet\lib.defs
* PX Command File:
               C:\Users\AYDIN\Desktop\hw mosfet\Generic 025.ext
* Command File:
* Cell Name:
                 mosfet
* Write Flat: NO
.model NMOS
************
M1 3 1 2 4 NMOS 1=4.8e-007 w=2.4e-006 ad=2.016e-012 as=1.872e-012 pd=6.48e-006 ps=6.36e-006 $ (8.94 33.42 11.34 33.9)
* Top level device count
* M(NMOS) 1
* Number of devices: 1
* Number of nodes: 4
```