AN61290

PSoC 3 and PSoC 5LP Hardware Design Considerations

Author: Mark Ainsworth

Associated Part Family: All PSoC 3 and PSoC 5LP family devices

Associated Code Examples: None

Related Application Notes: see Related Documents

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This application note reviews topics for designing a hardware system around a PSoC® 3 or PSoC 5LP MCU device, including pin connections for power system, reset, and programming and debug interfaces.

Contents

1 Introduction

PSoC 3 and PSoC 5LP devices provide power and flexibility for analog and digital applications, beyond what traditional MCUs offer. However, this flexibility raises new considerations when designing a PSoC device into a printed circuit board (PCB).

These considerations include proper connections for device power, reset, crystal, programming, and other pins.

Good board layout techniques are also important, especially for CapSense and precision analog applications.

Finally, the PSoC device must be configured to work optimally in its hardware environment. The PSoC Creator™ IDE is used for this purpose.

This application note provides information on each of these topics, so that you can successfully design PSoC into a PCB and hardware environment.

This application note assumes that you have some basic familiarity with PSoC 3 or PSoC 5LP devices and the PSoC Creator IDE. If you are new to PSoC 3 or PSoC 5LP, you can find introductions in AN54181, Getting Started with PSoC 3 and AN77759, Getting Started with PSoC 5LP. If you are new to PSoC Creator, see the PSoC Creator home page.

For PSoC 4, see AN88619, PSoC 4 Hardware Design Considerations.

2 Package Selection

One of the first decisions you must make for your PCB is which PSoC package to use. Several considerations drive this decision, including number of I/O pins required, PCB and product size, PCB design rules, and thermal and mechanical stresses.

PSoC 3 and PSoC 5LP devices are available in as many as five packages: 100-TQFP, 68-QFN, 48-QFN, 48-SSOP, and wafer level chip scale packages (CSP). PSoC 3 CSP is 72 pins, and PSoC 5LP CSP is 99 pins. Following are some package selection criteria:

100-TQFP and 48-SSOP:

- Easier to route signals due to large pitch and the open area below the part
- Disadvantages are larger package, and lower mechanical stability and thermal conduction.

68-QFN and 48-QFN:

- QFN packages are smaller
- More mechanical stability and better thermal conduction
- Disadvantages are:
  - More difficult to route signals due to the center pad
  - Mechanical stress on the center pad may cause electrical performance changes

For more information, see AN72845, Design Guidelines for QFN Packaged Devices.

CSP: CSP is a true die-scale package. It offers the smallest footprint for each I/O pin count of any standard package. It is used in applications with:

- Very small PCB size
- Flexible printed circuits (FPC)

However, the manufacturing process is more complex and requires specialized knowledge. For more information see:

- AN89611, PSoC 3 and PSoC 5LP Getting Started with Chip Scale Packages
- AN69061, Design, Manufacturing, and Handling Guidelines for Cypress Wafer Level Chip Scale Packages.

All PSoC 3 and PSoC 5LP devices in CSP packages have a factory-installed bootloader. For details, see the device datasheet.

3 Power System

The PSoC power system is based on separate supplies and returns for analog, digital, I/O pins, and boost, as Table 1 and Figure 1 on page 3 show.

Table 1. PSoC 3 and PSoC 5LP Power Domains

Power Domain	Associated Power and Return Pins
Analog	V_{DDA}, V_{CCA}, V_{SSA}
Digital	V_{DDD} (2), V_{CCD} (2), V_{SSD} (2)
I/O pins	V_{DDIO0}, V_{DDIO1}, V_{DDIO2}, V_{DDIO3}, V_{SSD}
Boost	V_{BAT}, V_{SSB}, IND, V_{BOOST} (not shown in Figure 1, see Figure 6)

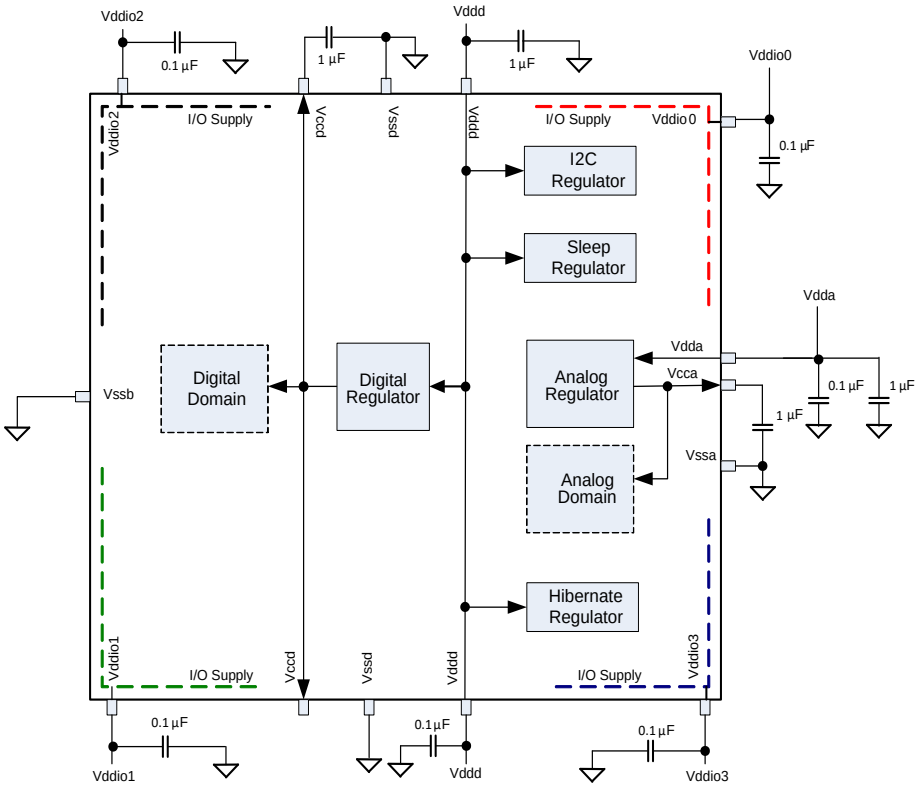
3.1 PSoC Power Pin Connections

The analog system power voltage, applied to V_{DDA} relative to V_{SSA}, can be as high as 5.5 V (absolute maximum), and must be greater than or equal to all other applied power voltages. That is, the voltage applied to the other V_{DDX} power pins, relative to V_{SSD}, must be ≤ V_{DDA}.

The minimum voltage that can be applied to any V_{DDX} power pin is 1.8 V.

To reduce power supply noise throughout the device, each V_{DDX} pin should be connected to a 0.1 µF or a 1 µF ceramic decoupling capacitor, as Figure 1 shows. The PCB trace between the pin and the capacitor should be as short and wide as possible – for more information see Appendix A. One or more 10 µF bulk decoupling capacitors can also be used.

Figure 1. PSoC 3 and PSoC 5LP Power System



Note: It is good practice to check the datasheets for your bypass capacitors, specifically the working voltage and the DC bias specifications. With some capacitors, the actual capacitance can decrease considerably when the DC bias (V_{DDX} or V_{CCX} in Figure 1) is a significant percentage of the rated working voltage.

Figure 1 also shows that within the PSoC device are two regulators – analog and digital – that take the V_{DDA} and V_{DDD} inputs and output 1.8 V to their respective power domains. The regulator outputs are also routed to pins V_{CCA} and V_{CCD}, respectively. A 1 µF ±10% X5R capacitor must be connected between the respective V_{CCX} and V_{SSX} pins, with as short a trace as possible.

Note that in Figure 1 V_{CCD} is routed to two pins; these two pins must be connected on the PCB. The PCB trace between the two V_{CCD} pins should be as short as possible; ideally, it should be run underneath the device directly between the two pins. For QFN packages with center pads, the trace can be run through vias to another PCB layer.

In Figure 1 only one of the V_{CCD} pins has a capacitor. Optionally, the other V_{CCD} pin may be connected to a 0.1 µF capacitor.

Cypress PSoC 3 and PSoC 5LP kit schematics provide good examples of how to incorporate PSoC into board schematics. For more information, see Related Documents.

3.2 Unregulated Mode

The usual way to power PSoC 3 or PSoC 5LP is in "regulated mode". In this mode voltage is applied to the V_{DDX} pins, and is not directly applied to the V_{CCX} pins. The internal analog and digital regulators are turned ON, and their outputs drive their respective domains within the device.

To reduce power consumption, PSoC can also be powered in "unregulated mode". In this mode, the V_{CCX} pins are directly powered and the analog and digital regulators are turned OFF.

In unregulated mode, the V_{CCX} pin voltage must be from 1.71 V to 1.89 V. The V_{DDX} pins must be tied to their respective V_{CCX} pins, but **do not** power the V_{CCX} pins with V_{DDX}-level voltages such as 3.3 V or 5.5 V, or the device may be damaged. For more information, see the device datasheet or Technical Reference Manual (TRM).

At reset, the regulators are always turned on as a default, and code generated by PSoC Creator does not turn them off. So to reduce the current in unregulated mode, you must add code to turn off the regulators; see the TRM for details.

Since the USBIOs are powered from V_{DDD} (see V_{DDIO} and Total Chip Power Considerations), and the USB bus does not operate at 1.8 V, you cannot use the PSoC USB feature with unregulated mode.

3.3 External Regulator Considerations

In either regulated or unregulated mode, it is likely that you will use power supply regulator devices to drive the PSoC power pins. (Other devices can be used, such as a battery or solar cell; see Boost Converter.) There are several regulator design considerations for maximizing PSoC performance.

One major decision is whether to use linear or switching regulators. Linear regulators are simple and low cost, and require fewer passive components. They also have fast transient response for switching loads, and very low noise and ripple. This makes them ideal for CapSense and other precision analog designs – if you have such an application, consider powering PSoC V_{DDA} (or V_{CCA} in unregulated mode) with a linear regulator.

However, linear regulators have limitations including low efficiency, and at higher currents may require large footprint thermal components such as heat sinks. Note also that linear regulators are always step-down converters – Vin must always be greater than Vout.

You can improve linear regulator efficiency by using low dropout (LDO) linear regulators. These devices enable Vout to be nearly equal to Vin, thereby reducing power loss and heat.

Switching regulators have a much higher efficiency, and often use less board space. However, switching regulators usually have more ripple and noise, and slower transient response. They are generally acceptable for digital circuits; the PSoC V_{DDD} and V_{DDIOx} pins are typically driven by a switching regulator.

As part of overall system design, review the performance and power requirements of each PSoC subsystem – digital, analog, and I/O pin groups – as well as the power requirements of other devices on your PCB. Then select one or more regulators to meet those requirements. For example, a small linear regulator may be used to power V_{DDA}, and a switching regulator for the other V_{DD} pins.

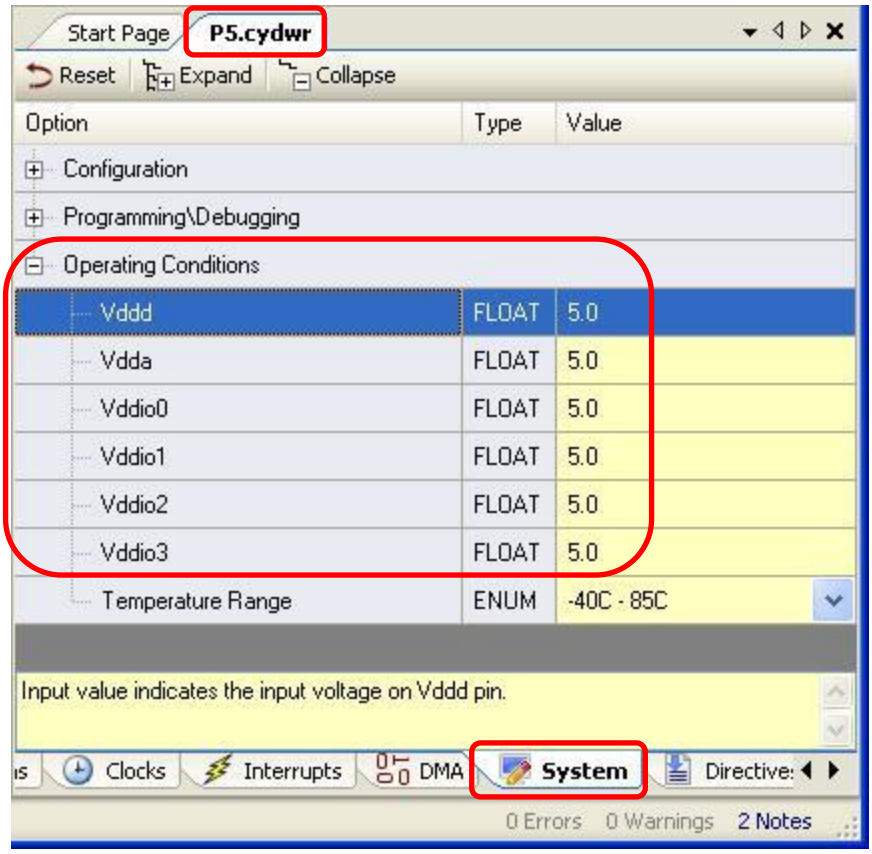
Note that both regulator types require a number of passive components, including input and output capacitors and feedback resistors. Switching regulators require an inductor and a Schottky diode. Carefully specify passive components to maximize regulator performance.

As always, good PCB layout techniques are required for high-performance power supply and analog system design. See Appendix A for PCB layout tips.

3.4 PSoC Creator Settings for Device Power

PSoC Creator automatically configures Components for optimal performance for the voltages applied to the power pins. To do this, PSoC Creator needs to know the value of these voltages. Use the **System** tab in your PSoC Creator project's design-wide resources (DWR) window, as Figure 2 shows.

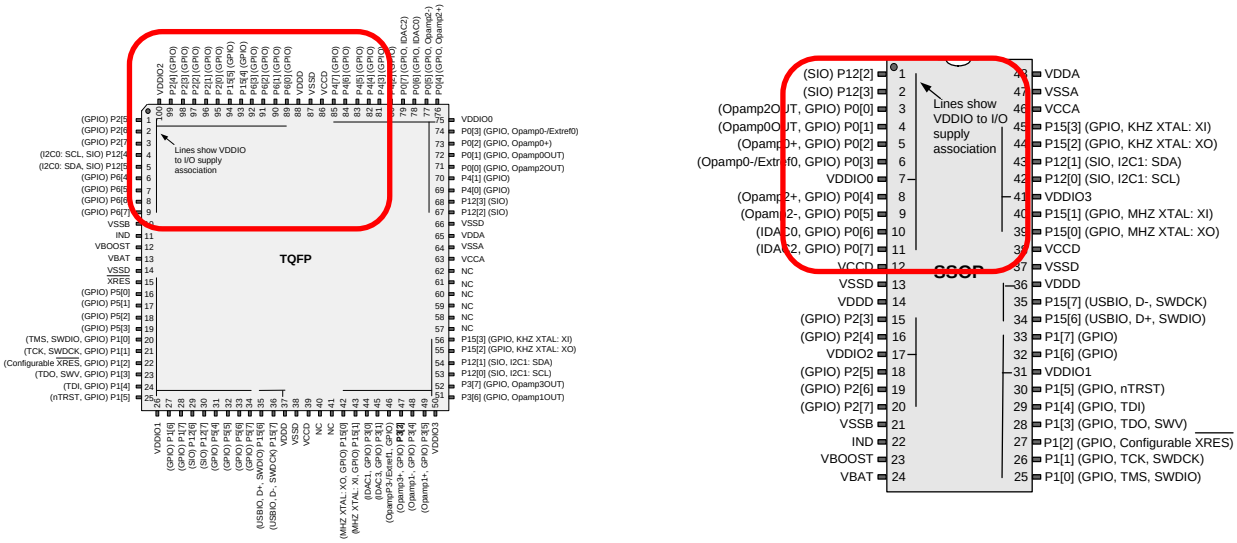
Figure 2. Device Power Settings in PSoC Creator



3.5 V_{DDIO} and Total Chip Power Considerations

Each V_{DDIO} pin powers a specific set of I/O pins, as Figure 3 shows. (The USBIOs are powered from the adjacent V_{DDD}.) This lets you support different voltage levels on interfaces to other devices, which reduces the need for level shifter devices on the PCB.

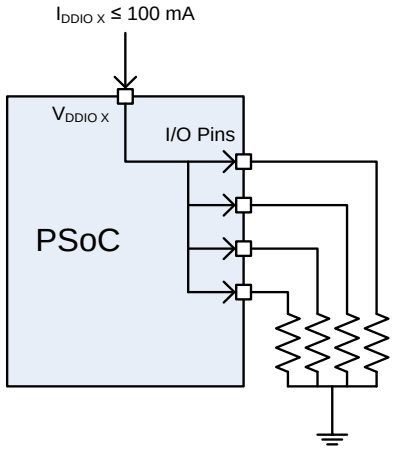
Figure 3. PSoC 3 100-TQFP and 48-SSOP Pinouts



The 68-QFN, 48-QFN, and CSP packages are not shown but are similar. See the device datasheet for information on these packages.

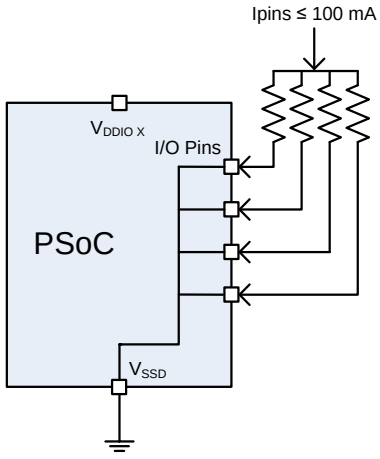
Each V_{DDIO} may source up to a total of 100 mA to its associated I/O pins, as Figure 4 shows.

Figure 4. V_{DDIO} Current Limit



Conversely, for the 100-pin, 68-pin, and CSP devices, the set of I/O pins associated with any V_{DDIO} may sink up to a total of 100 mA, as Figure 5 shows.

Figure 5. I/O Pins Current Limit



For the 48-pin PSoC 3 devices, the set of I/O pins associated with V_{DDIO0} plus V_{DDIO2} may sink up to a total of 100 mA. The set of I/O pins associated with V_{DDIO1} plus V_{DDIO3} may sink up to a total of 100 mA.

3.6 Thermal Considerations

Under certain conditions it may be possible for the chip to dissipate as much as 0.5 W. With that much power in a device, you should consider taking steps to keep it from overheating.

To do this, first check the datasheet for the thermal resistance from junction to ambient (θ_{JA}), for the package that you intend to use. θ_{JA} is expressed in units of °C/watt, for example the θ_{JA} for the 100-pin PSoC 3 is 34 °C/watt.

If the device must dissipate 0.5 W, then the maximum temperature difference between the device junction and the ambient air surrounding the device is θ_{JA} times the maximum power, or 34 °C/watt x 0.5 watt = 17 °C. Since the specified maximum operating junction temperature of the device is 100 °C, the maximum allowable ambient air temperature is 100 – 17 = 83 °C. If you use the 48-SSOP package, which has a higher θ_{JA} of 49 °C/watt, then the maximum allowable ambient air temperature is 100 – (49 x 0.5) = 75.5 °C.

Note: The datasheet specifications for θ_{JA} are typical. You should design your product such that the ambient air temperature is much less than the allowable maximum.

Note: With the above calculation, if the θ_{JA} or the power dissipated is low, the maximum allowable ambient air temperature could theoretically approach the 100 °C junction temperature limit. However, the product's industrial-range ambient air temperature limit of 85 °C still applies.

For more information, see AN72845, Design Guidelines for QFN Packaged Devices.

3.7 Power Ramp-up Considerations

As mentioned previously, the voltages at the V_{DDD} and V_{DDIO} pins must be less than or equal to that on V_{DDA}.

When powering up the device, the maximum ramp rate for any V_{DDx} pin is 1 V / 15 µs, or 0.066 V/µs.

The power pins can be brought up in any order as long as once they are stable, V_{DDA} is the highest voltage.

3.8 Boost Converter

In addition to the power pins, PSoC 3 and PSoC 5LP provide a high-efficiency boost converter that can power the device from supply voltages as low as 0.5 V. This enables the device to be powered directly from a single battery or solar cell. You can also use the boost converter to power other devices besides the PSoC.

As Figure 6 shows, the boost converter system uses four device pins:

- VBAT: input voltage
- VSSB: input voltage ground
- IND: Inductor connection
- VBOOST: output voltage

External components required for use with the boost are capacitors, an inductor, and a Schottky diode. For more information on the boost converter and performance specifications see one of the device datasheets or TRM.

To enable the boost converter in a PSoC Creator project, simply drag a Boost Converter Component symbol to the project schematic. (It is in the Component Catalog window, Cypress tab, System node.) Then configure the input and output voltage and other parameters for your application, as Figure 7 shows.

Figure 6. Boost Converter Typical Application

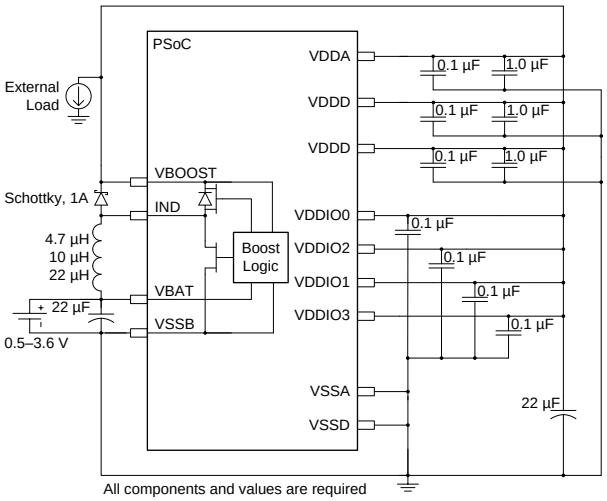
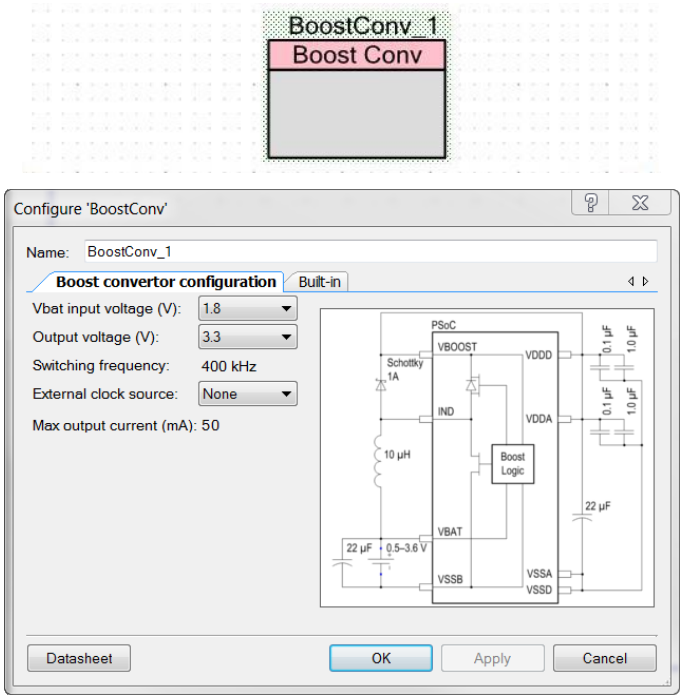


Figure 7. PSoC Creator Boost Converter Component



The boost converter block is enabled at device reset, with an output voltage of 1.8 V. This allows the device to start up when the input voltage to the boost is below the minimum to power the chip. The settings for the PSoC Creator Boost Component take effect when the API function BoostConv_Start() is called. You can adjust the Component parameters during run time using boost component API functions. See the Boost Component datasheet for details.

If the boost converter is not used, tie the VBAT, VSSB, and VBOOST pins to ground and leave the IND pin unconnected.

4 I/O Pins

PSoC 3 and PSoC 5LP provide a flexible set of I/O ports and pins. Any function – analog or digital – can be routed to almost any I/O pin, which can help to optimize your PCB layout.

There are three types of pins: general-purpose I/O (GPIO), performance I/O (SIO), and USBIO. Following are brief descriptions of each type.

GPIO:

- Support for routing of digital or analog functions, interrupts, segment LCD drive, and CapSense. (For more information on CapSense, see AN64846, Getting Started with CapSense.) Up to 4 mA source and 8 mA sink.
- Some pins share functions with certain blocks – for example, opamps, analog voltage references, current DAC outputs, crystal oscillators, and programming and debug
- LVTTL or CMOS mode, with many different drive and slew rate options

Most of the I/O port pins are GPIO. For more information, see application note AN72382, Using PSoC 3 and PSoC 5LP GPIO Pins.

SIO:

SIO is the same as GPIO except:

- Higher drive strength – up to 4 mA source and 25 mA sink
- Programmable output drive levels and input levels for voltage level shifting. An SIO pin can actually act as an analog comparator; see a device datasheet for details.
- Overvoltage tolerance up to 5.5 V, and hot swap capability
- Some SIO pins can be used to enable wake from sleep mode on I^2C address match. For more information, see application note AN77900, PSoC 3 and PSoC 5LP Low Power Modes and Power Reduction Techniques.
- No analog, LCD, or CapSense support

One I/O port, P12, is all SIO pins. For more information, see application note AN60580, PSoC 3 and PSoC 5LP SIO Tips and Tricks.

USBIO:

- Support for full speed USB 2.0. Note that if the USBIO pins (D- and D+ on P15[7:6] respectively) are to be connected to a USB bus then 22-Ω 1% resistors must be placed in series with the pins, close to the package leads. The USB D+ pull-up is integrated into that USBIO pin.
- Limited GPIO capability if USB is not used – no analog, LCD, or CapSense support

For more information on all three pin types, see the device datasheet or TRM.

4.1 I/O Pin Selection

When you create a schematic with a PSoC device, you should select which pins go to which functions in the following order:

1. **Power pins:** How many different or separate voltages are required for digital, analog, and I/O power? Is the boost converter needed? See Power System for details.
2. **Fixed pins:** Will you need the following features:
   - Device reset? Some packages have a dedicated pin for this purpose, and with some devices pin P1[2] can be configured as a reset input. See Device Reset for details.
   - Flash programming or debug, using JTAG or SWD? If not, the pins can be used as GPIOs – see Programming and Debug for details.
   - MHz or 32 kHz crystal oscillator? If not, the pins can generally be used as GPIOs – see Oscillators for details.
   - Analog features, such as opamp, current DAC output, external voltage reference? If not, the pins can be used as GPIOs – see Analog Connections for details.
   - USB? If not, the USBIO pins can be used as limited GPIOs – see USBIO description. They can also be used for flash programming and debug – see Programming and Debug for details.

- Wake from sleep on I^2C address match? Depending on the package, one or two pairs of SIO pins are available for this purpose. For details see a device datasheet, TRM, or application note AN77900, PSoC 3 and PSoC 5LP Low Power Modes and Power Reduction Techniques.

3. **SIO pins:** Will you need any of the SIO-unique features described previously? If not, these pins can be used as GPIOs for digital functions.
4. **GPIO pins for analog functions:** You can optimize the analog routing within PSoC by carefully selecting GPIO pins for your analog functions. For more information, see application notes AN58827, Internal Routing Considerations for PSoC 3 and PSoC 5LP Analog Designs, and AN58304, PSoC 3 and PSoC 5LP Pin Selection for Analog Designs.
5. **GPIO / SIO pins for digital functions:** All remaining pins can be used for digital I/O functions, and can be assigned to simplify or optimize your PCB layout.

   If a GPIO, SIO, or USBIO is not used, it should be left floating and in the high impedance analog state – see I/O Pins and Device Reset.

Note: Special cases exist for use of configurable P1[2], and in high-reliability applications:

- For devices with both XRES and P1[2]: Configure P1[2] as a digital input with the resistive pull-up enabled. For high-reliability applications, leave P1[2] unconnected (and pulled up).
- For devices with only P1[2]:
  - If P1[2] is being used as a GPIO, or it is not being used: Configure it as a digital input with the resistive pull-up enabled. For high-reliability applications, leave P1[2] unconnected (and pulled up).
  - If P1[2] is being used as XRES: This configuration is not recommended for high-reliability applications.

Any device pin marked “do not use” (DNU) must be left unconnected and floating. Note that in devices without USB the USBIO pins are DNU.

4.2 I/O Pins and Device Reset

The I/O pins are always in one of three states relative to device reset:

1. While reset is active, all I/O pins are in the high-impedance analog state.
2. When a PSoC device comes out of reset, the state for each I/O port can be set to high-impedance analog (the default), pull-up or pull-down. See Figure 10 on page 12. Each port’s state is saved in nonvolatile latches (NVLs), and is automatically applied at reset. For more information on NVLs, see the device datasheet or TRM.
3. The final state for each I/O pin is determined by PSoC Creator project settings, and is applied before the code reaches main().

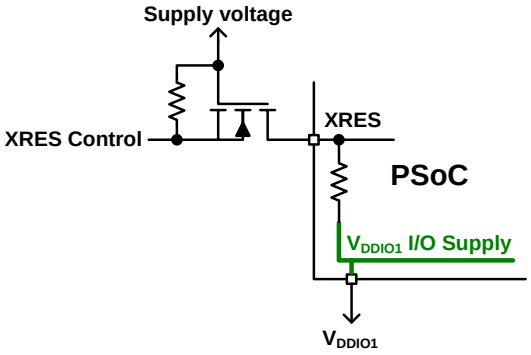
4.3 I/O Pins and Level Shifting

In many applications, PSoC I/O pins must be connected to devices that operate at different voltage levels. There are several ways to do this:

- Connect a V_{DDIOx} pin to the same VDD voltage as the other device, as long as the V_{DDIOx} is less than or equal to the PSoC V_{DDA} voltage. This allows direct pin-to-pin connection between a PSoC I/O pin that is driven by the V_{DDIOx} and the other device's I/O pin.
- When driving an output voltage from PSoC to the other device, put the PSoC I/O pin in open drain drives low mode. Then on the wire between the I/O pins, add a pull-up resistor to the V_{DD} of the device with the input pin. The pull-up may be either external or within the device's I/O pin. Note that some buses such as I^2C require pull-up resistors and open-drain pins.
- When the other device is driving an output voltage to a PSoC input, put the PSoC I/O pin in resistive pull-up mode. Then use a FET and a resistor to form a level shifter, as Figure 8 shows.

  Note that this technique also applies to the PSoC XRES pin. The XRES pin is active low and has an internal pull-up resistor to V_{DDIO1}, as Figure 8 shows. For more information, see Device Reset.

Figure 8. FET Level Shifter for PSoC XRES Input

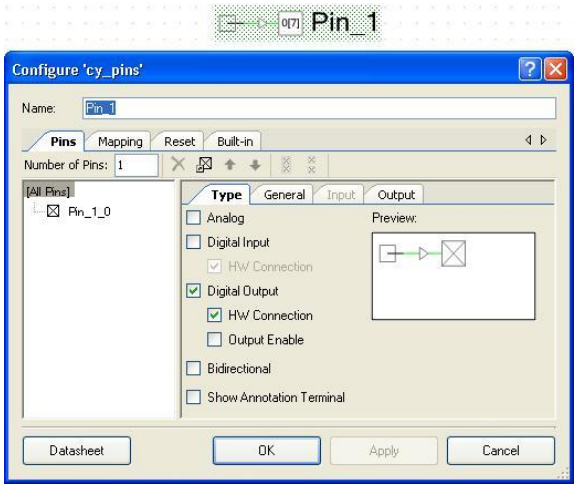


4.4 I/O Pins and PSoC Creator

All of the PSoC 3 or PSoC 5LP I/O pins' states and functions can be controlled by PSoC Creator project settings, through the Pins Component. The Pins Component lets you easily set up all pin parameters and drive modes. It enables easy pin usage by hardware, firmware, or both. To use the Pins Component, just drag it onto the project schematic and bring up the configuration dialog – see Figure 9.

To connect a hardware function to a pin, just drag a wire between the function and the pin on the project schematic. Note that pins can be grouped in multiple ways, and can include bus wire connections. See the Pins Component datasheet for details.

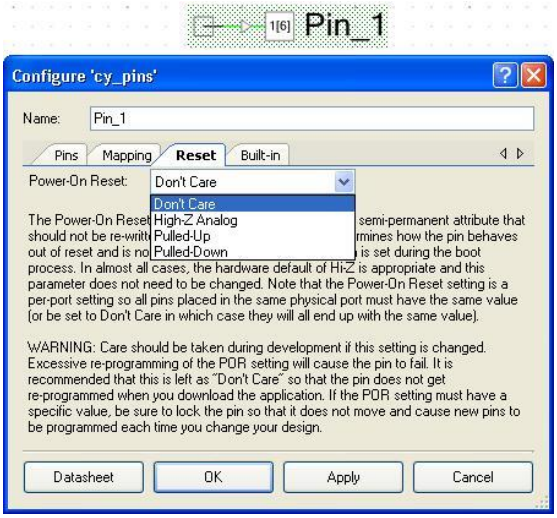
Figure 9. Pins Component and Configuration



To set the reset value of a pin (see I/O Pins and Device Reset), go to the **Reset** tab of the dialog and select one of the options – see Figure 10.

Remember that the Reset setting is applied to an entire port, not to individual pins. If you attempt to have pins with different reset settings on the same port, PSoC Creator gives you an error message. The **Don't Care** and **High-Z Analog** (the default) settings are acceptable for most applications.

Figure 10. Pins Component Reset Setting

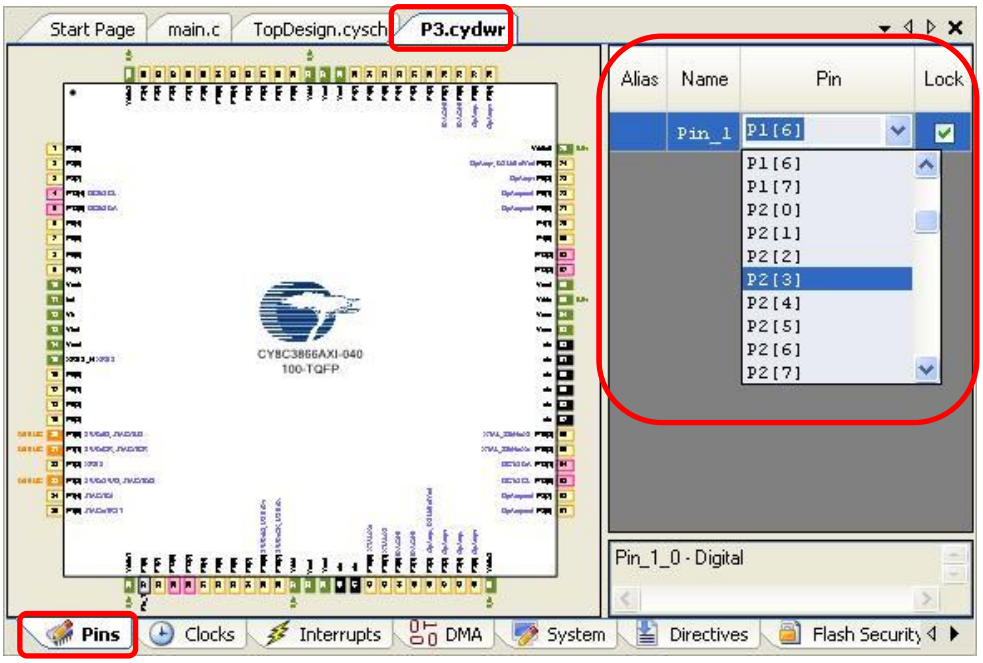


After you add all your Pins Components to the PSoC Creator schematic, and configure them, you can associate them with the physical pins on the device. PSoC Creator can do this for you; it tries to find the best fit based on:

- Your Pins Component configuration settings, including reset values and pin grouping
- Internal routing of analog and digital signals to the pins
- Dedicated pin assignments such as USB or I^2C

In many cases, you may want to lock, or force, a pin assignment. Use the **Pins** tab in the DWR window for this purpose, as Figure 11 shows.

Figure 11. Pins Component and Configuration



4.5 EMC / ESD Protection

GPIO and SIO pins have fast and slow output slew rate options for some drive modes. Use the slow slew rate option to reduce electromagnetic emissions, generally for signals less than 1 MHz. The fast slew rate is for signals between 1 MHz and 33 MHz. The slew rate is individually configurable for each pin.

It is good design practice to protect I/O pins, and consequently the device itself, from electrostatic discharge (ESD) by putting on the PCB a 50 Ω to 100 Ω resistor in series with any I/O pin that is routed off the PCB – for example to a button or a connector.

For further protection against high static discharges or other sources of high transient voltages, you can use a transient voltage suppressor (TVS) diode. TVS diodes absorb the high peak energy of a transient event. For more information, see the datasheets published by multiple TVS diode manufacturers.

For more information on electromagnetic compatibility (EMC) and ESD considerations, see AN80994, PSoC EMC Best Practices, and Appendix A.

5 Device Reset

All PSoC 3 and PSoC 5LP devices have power-up reset. When the device is powered up, it is held in reset until all of the V_{DDX} and V_{CCX} supplies reach levels for correct operation. For details, see a device datasheet or TRM, or the application note AN60616, PSoC 3 and PSoC 5LP Startup Procedure.

Another reset method uses a reset pin, called XRES. As Table 2 shows, 100-pin and 68-pin packages have a dedicated XRES. PSoC 3 48-pin packages do not have a dedicated reset pin, instead P1[2] is configured by factory default to act as a reset pin. If a reset pin is not required then this pin can be reprogrammed to be a GPIO.

For more information on using P1[2] in high-reliability applications, see these recommendations.

Table 2. PSoC 3 or PSoC 5LP Reset Pins

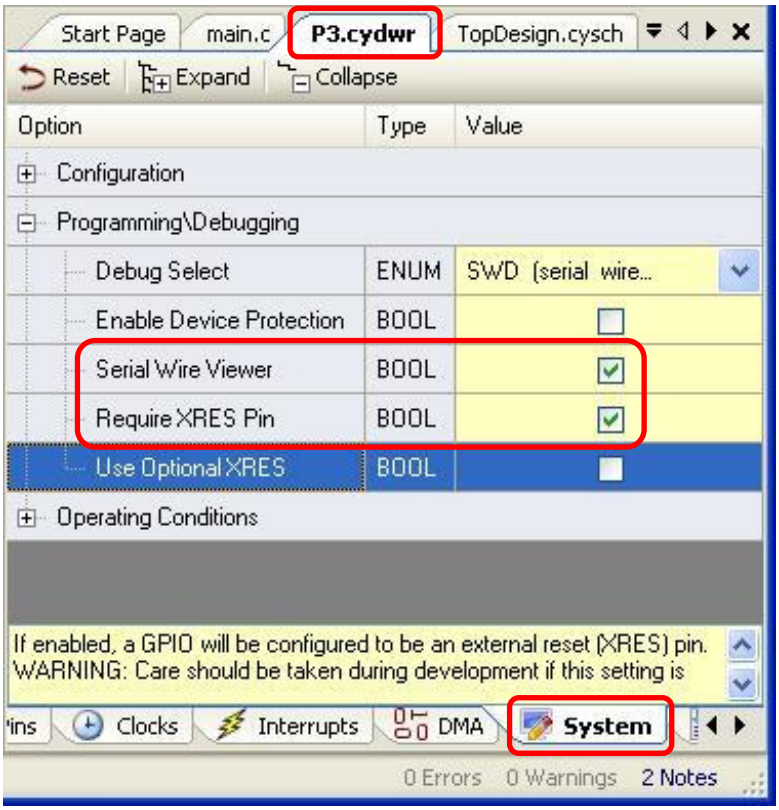
Package	Dedicated XRES Pin	P1[2] Factory Default Setting
100-TQFP	Yes	GPIO
68-QFN	Yes	GPIO
48-QFN *	No	XRES
48-SSOP *	No	XRES
72-CSP **	Yes	GPIO
99-CSP ***	Yes	GPIO

* PSoC 5LP devices are not available in 48-pin packages and always have a dedicated XRES pin.
** PSoC 3 only
*** PSoC 5LP only

For 48-pin PSoC 3 devices, use PSoC Creator to configure P1[2] as either GPIO or XRES. Go to the **System** tab in the PSoC Creator project's design-wide resources (DWR) window, as Figure 12 shows. The setting is saved in nonvolatile latches (NVLs) and is automatically applied at reset. For more information on NVLs, see a device datasheet or TRM.

For 48-pin PSoC 3 devices, if you need an XRES connection then check the **Use Optional XRES** box. For 100-pin and 68-pin devices, you can usually leave this box unchecked because these devices already have a dedicated XRES pin.

Figure 12. PSoC Creator XRES Settings



To reset the device through a reset pin, hold the pin at a low voltage for at least 1 µs. When the pin is released, an internal pull-up resistor brings the voltage up to V_{DDIO1} and the device comes out of reset.

6 Programming and Debug

PSoC 3 and PSoC 5LP support both the joint test action group (JTAG) and serial wire debug (SWD) interfaces for device flash programming and debug.

A third interface, single wire viewer (SWV), is also available for "printf-style" debugging. (The term refers to a common way to debug C code – critical parts of the code have calls to the library function printf(), to report in real-time the status and performance of the code.)

All interfaces exist on the same set of pins in I/O port 1:

- JTAG: P1[4], P1[3], P1[1], P1[0]. An optional JTAG signal, nTRST, can be input on P1[5].
- SWD: P1[1], P1[0]
- SWV: P1[3]

To connect to a programming device, such as the Cypress CY8CKIT-002 MiniProg3, you need a 10-pin, dual row, 50-mil pitch connector. Recommended connectors are the Samtec FTSH-105-01-L-DV-K (surface mount) and the FTSH-105-01-L-D-K (through hole) or similar available from other vendors. Figure 13 shows the signal assignments for SWD and JTAG.

Figure 13. SWD and JTAG Pin Assignments for MiniProg3

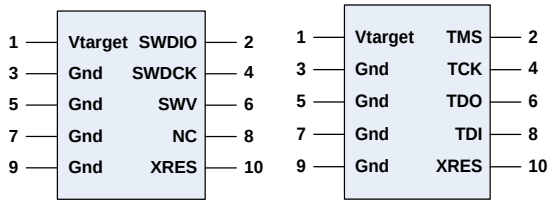


Figure 14 and Figure 15 show the connections between this header and the device JTAG / SWD / SWV pins. For more information see the device datasheets and TRMs. Another good programming reference is at General PSoC Programming.

Figure 14. SWD Connections to PSoC 3 or PSoC 5LP

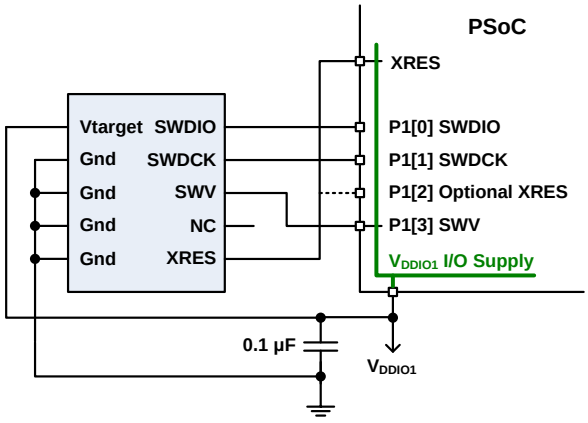
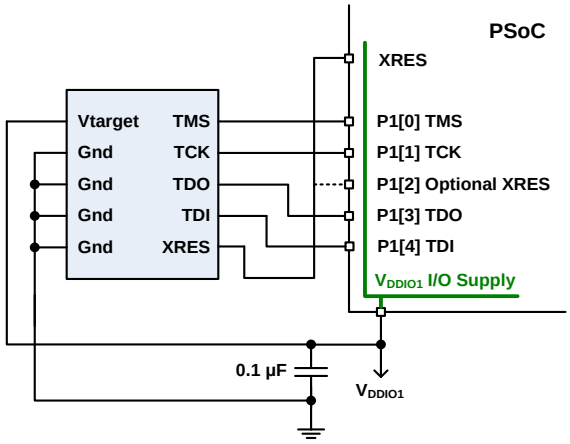


Figure 15. JTAG Connections to PSoC 3 or PSoC 5LP



For 100-TQFP and 68-QFN devices, connect the reset to the dedicated XRES pin. For PSoC 3 48-pin devices, P1[2] is configured by factory default to be an XRES; connect the reset to that pin.

Only one interface – JTAG, or SWD and SWV – is available at a time. If flash programming or debug are not required, the I/O port pins can be used as GPIOs – see I/O Pins.

The SWD interface is also available on the two USBIO pins. This option is useful if you are not using USB and you need the P1 pins for GPIO purposes. See USBIO description for details.

Note: Cypress PSoC 3 and PSoC 5LP kit schematics provide good examples of how to incorporate PSoC into board schematics. For more information, see Related Documents.

6.1 PSoC Creator Debug Settings

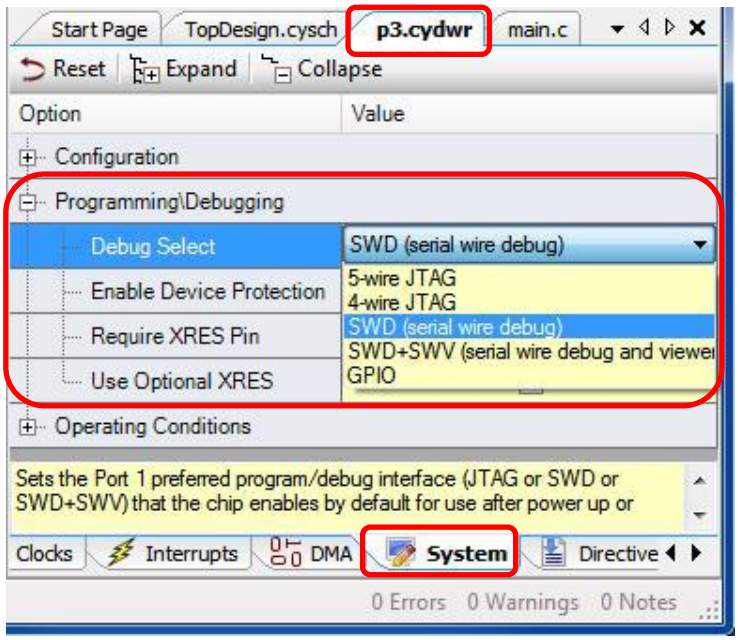
Use PSoC Creator to configure the device's P1 pins for the desired programming/debug interface. Go to the **System** tab in the PSoC Creator project's design-wide resources (DWR) window – see Figure 16.

If the USBIOs are to be used for the SWD interface, set the **Debug Select** setting to **GPIO**.

The settings are saved in nonvolatile latches (NVLs) and automatically applied at reset. For more information on NVLs see the device datasheet or TRM.

As Figure 17 shows, for the current setting on the System tab PSoC Creator shows in the **Pins** tab the corresponding pins, with the label DEBUG.

Figure 16. PSoC Creator Debug Settings



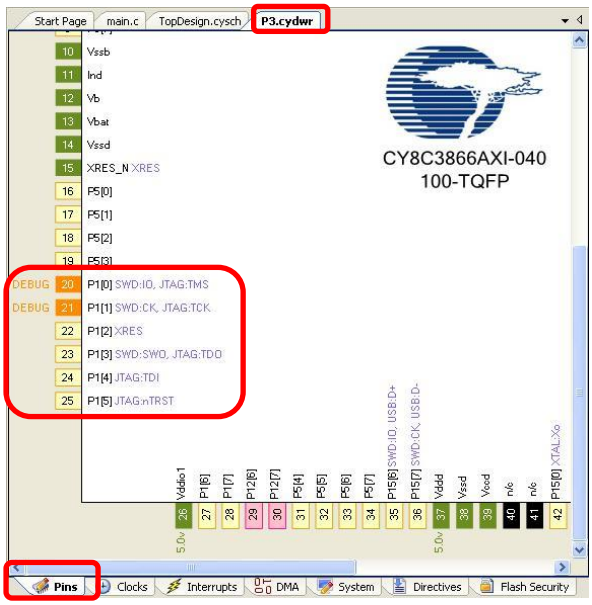
6.2 Port Acquisition

If you choose the GPIO setting, the P1 pins are initialized as GPIOs. However, you can still do an acquire operation to enable a JTAG or SWD interface on these pins.

An acquire operation can only be done in SWD mode. A special sequence of 1s and 0s is sent over a pin pair during a key window of 8 µs after reset. The acquire can be done to either the P1[1:0] pins or the USBIOs; that pin pair is then used as the SWD interface.

When using the SWD interface over the P1 pins, you can change the interface to JTAG. Similarly, you can change from the JTAG interface to SWD. For details on acquisition and interface management, see PSoC 3 Device Programming Specifications or PSoC 5LP Device Programming Specifications.

Figure 17. PSoC Creator Debug Pin Indications



7 Oscillators

The PSoC 3 and PSoC 5LP clocking system is highly versatile and configurable. For many designs, no external crystal is required – the internal main oscillator (IMO) and PLL together can generate up to an 80 MHz clock, accurate to ±1% over voltage and temperature. For basic timing purposes, an internal low-speed oscillator is also provided; output frequencies are 100 kHz, 33 kHz, and 1 kHz.

For more information on the PSoC clocking system, see a device datasheet, TRM, or application note AN60631, PSoC 3 and PSoC 5LP Clocking Resources.

If you need greater system accuracy, PSoC also provides an external crystal oscillator (ECO) that supports crystals from 4 MHz to 25 MHz (MHzECO). And for higher-accuracy timing, such as for a real-time clock (RTC), a second ECO is available that supports a 32.768 kHz crystal (kHzECO).

For more information on the PSoC external oscillators, see application note AN54439, PSoC 3 and PSoC 5LP External Oscillators. This application note gives a detailed explanation of PCB layout techniques for external crystals as well as configuration using PSoC Creator.

If an ECO is not needed, the pins can be used as GPIOs – see I/O Pin Selection.

8 Analog Connections

PSoC 3 and PSoC 5LP devices have a number of GPIO pins that are shared with fixed analog functions. There are several considerations when using these pins for analog functions.

8.1 Delta-Sigma ADC External References

The PSoC 3 and PSoC 5LP delta-sigma ADC has a number of options for input reference voltage, including a 1.024-V reference that is as low as 0.1% accuracy in some devices. Most of these references are available internally; see the device datasheet or TRM for details.

If you need higher accuracy, or a reference voltage that is different from those provided internally, two pins are available to connect an external reference voltage to the ADC. They are P0[3] and P3[2]. PSoC Creator's delta-sigma ADC Component configuration dialog has options to select one of these pins as the ADC reference – see Figure 18.

When you select an External Vref option, you must also enter the value of the reference voltage that you will apply. The applied voltage must be from 0.9 to 1.3 V.

PSoC Creator automatically routes the external reference to the selected pin, as Figure 19 shows. If another Pin Component is already locked to this pin, an error message is displayed.

If you want to use an internal reference, and reduce the noise on that reference, you can connect a filter capacitor to one of these pins. The value of the capacitor depends on your desired noise rolloff as well as your Component settings; 0.1 µF to 1 µF is usually appropriate. To enable this feature in PSoC Creator, select one of the **Internal Bypassed on** options shown in Figure 18.

Figure 18. Delta-Sigma ADC Reference Selection

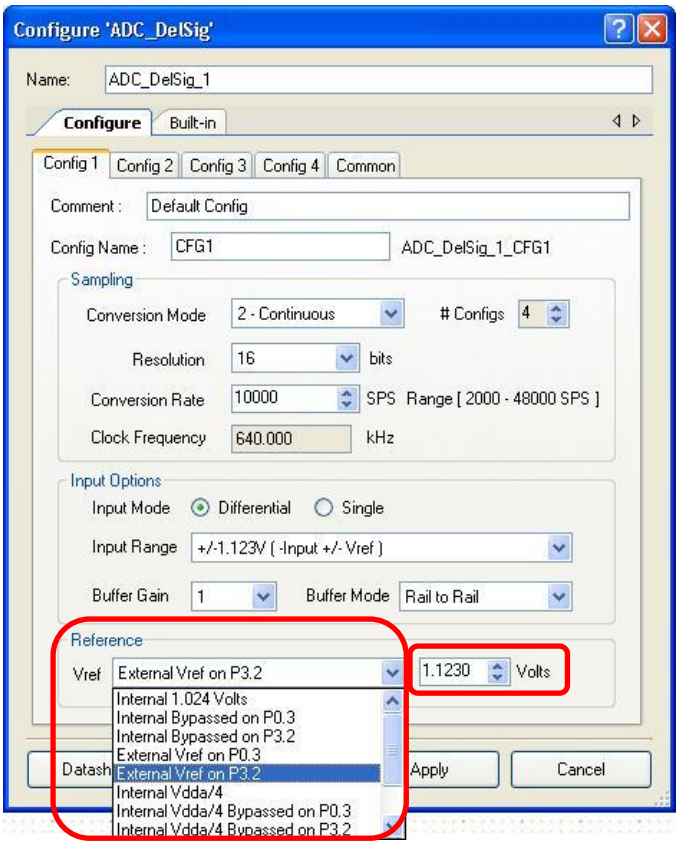
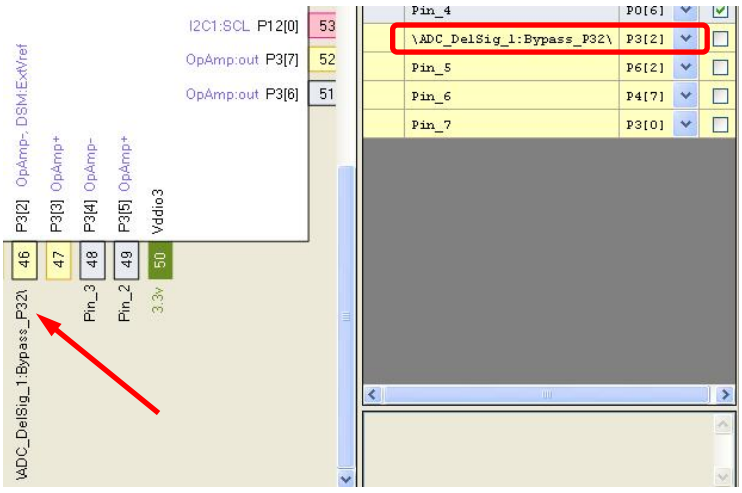


Figure 19. Delta-Sigma ADC Reference Pin



8.2 SAR ADC External References

The PSoC 5LP successive approximation register (SAR) ADCs also have input reference voltage options similar to those for the delta-sigma ADC. See a device datasheet or TRM for details.

Depending on the device, one or two SAR ADCs are available, and an external reference pin exists for each:

- P0[4] for SAR0
- P0[2] for SAR1

PSoC Creator's SAR ADC Component configuration dialog has an option to select one of these pins as the ADC reference, as Figure 20 shows.

When you select the external reference option, you must also enter the value of the reference voltage that you will apply. The applied voltage can range from 0 to V_{DDA}, however a practical range is 1 V to V_{DDA} / 2.

PSoC Creator automatically routes the external reference to the corresponding pin, as Figure 21 shows. If another Pin Component is already locked to this pin, PSoC Creator either tries to use the other SAR ADC, or displays an error message.

If you want to use an internal reference, and reduce the noise on that reference, you can connect a filter capacitor to the pin. The value of the capacitor depends on your desired noise rolloff as well as your Component settings; 0.1 µF to 1 µF is usually appropriate. To enable this feature in PSoC Creator, select the **Internal Vref, bypassed** option in the SAR configuration dialog.

To force PSoC Creator to use SAR 0 or SAR 1, and thus force the choice of reference pin, go to the DWR window, **Analog** tab, right-click the SAR block, and select **Relocate**, as Figure 22 shows. For more information on analog manual placement and routing, see the PSoC Creator help article *Analog Device Editor*.

Figure 20. SAR ADC Reference Selection

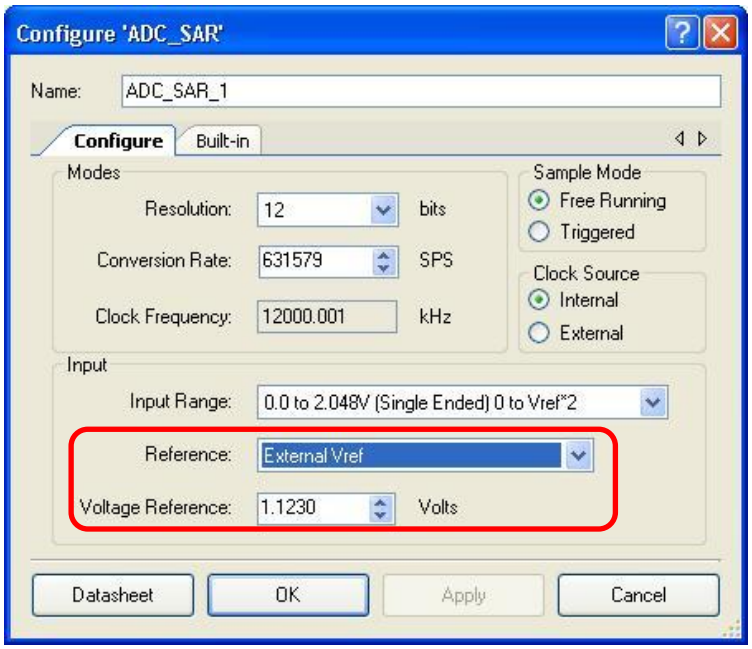


Figure 21. SAR ADC Reference Pin

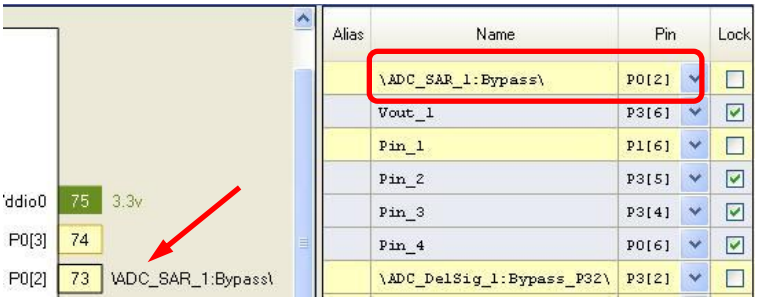
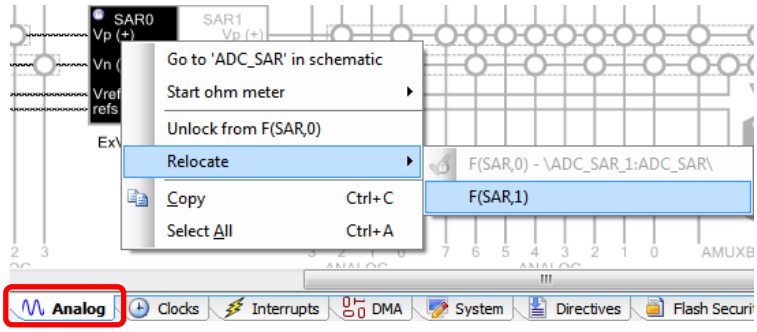


Figure 22. Relocate SAR ADC Component



8.3 Current DAC (IDAC) Outputs

PSoC 3 and PSoC 5LP devices have as many as four DACs that can operate in either voltage or current mode (VDAC or IDAC). The IDAC outputs can be routed throughout the analog routing system – see the device datasheet or TRM for details.

In addition to internal routing, the IDAC outputs can be routed to a set of dedicated low-resistance output pins. There is one pin for each DAC, as Table 3 shows.

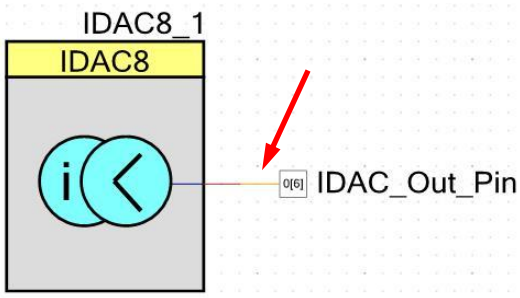
Table 3. IDAC Dedicated Pin Assignments

IDAC	Dedicated Iout Pin
IDAC0	P0[6]
IDAC1	P3[0]
IDAC2	P0[7]
IDAC3	P3[1]

The IDACs have three output current ranges – 32 µA, 255 µA, and 2.04 mA. If the IDAC is set to the highest range, the output must be routed to the corresponding dedicated Iout pin. There is no direct support for this in PSoC Creator; instead do the following:

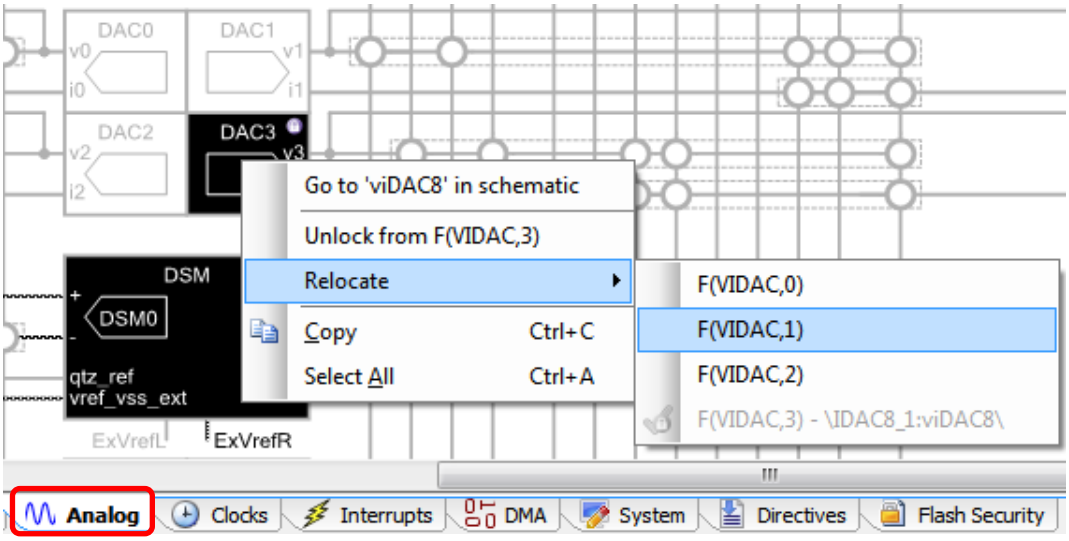
1. Place the Current DAC Component and the Pin Component onto the schematic and connect them. In the DWR window, lock the Pin Component to the Iout pin that you want to use. See Figure 23.

Figure 23. Schematic for Dedicated Iout



2. In the DWR window, **Analog** tab, right-click the DAC block to relocate it, as Figure 24 shows. For more information on analog manual placement and routing, see the PSoC Creator help article *Analog Device Editor*.

Figure 24. Relocate DAC Component



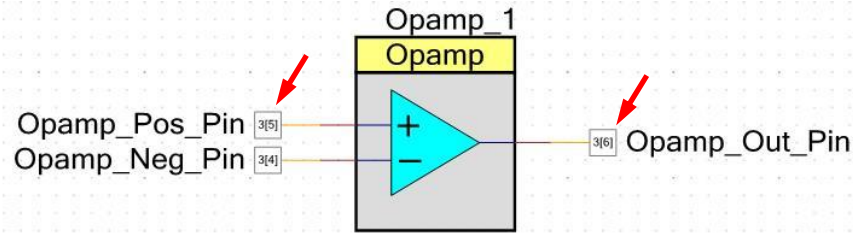
8.4 Opamp Connections

Similar to DACs, PSoC 3 and PSoC 5LP devices have as many as four opamps that, in addition to internal routing, have low-resistance connections to dedicated pins. Each opamp has three dedicated pins, for the + and – inputs, and the output. See the device datasheet for details.

In PSoC Creator, if an Opamp Component is used, its *output* is always routed to its associated output pin. However, similar to the DACs, there is no direct support for dedicated *input* pin placement for opamps; instead, do the following:

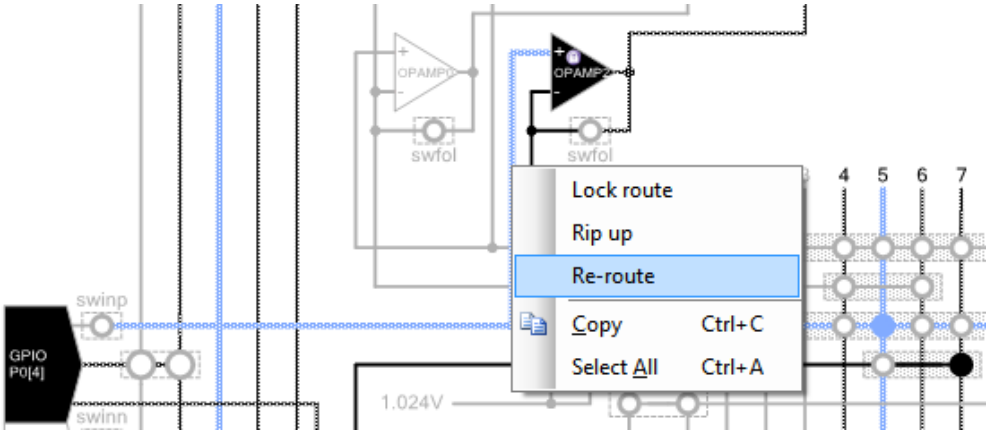
1. Place the Opamp and Pin Components onto the schematic and connect them. In the DWR window, lock the Pin Components to the opamp pins that you want to use. See Figure 25.

Figure 25. Schematic for Dedicated Opamp Pins



2. In the DWR window, Analog tab, right-click the opamp block to relocate it, as in SAR ADC or Current DAC, or re-route the connections to the opamp as Figure 26 shows. For more information on analog manual placement and routing, see the PSoC Creator help article *Analog Device Editor*.

Figure 26. Relocate Opamp Component



9 Summary

Many of the hardware considerations given in this application note are similar to those for other MCU devices. However, the power and flexibility of PSoC 3 and PSoC 5LP raise additional topics, such as selecting the best pins for the application and using opportunities to simplify and optimize PCB routing.

This application note has provided information on each of these topics, so that you can successfully design PSoC 3 or PSoC 5LP devices into a PCB and hardware environment.

Use the Schematic Checklist in Appendix B to check your hardware design and PSoC Creator settings.

10 Related Documents

The following application notes are a good source for more detailed information:

- AN54181 – Getting started with PSoC 3
- AN77759 – Getting started with PSoC 5LP
- AN58304 – PSoC 3 and PSoC 5LP Pin Selection for Analog Designs
- AN58827 – PSoC 3 and PSoC 5LP Internal Analog Routing Considerations
- AN57821 – PSoC 3, PSoC 4 and PSoC 5LP Mixed Signal Circuit Board Layout Considerations
- AN77900 – PSoC 3 and PSoC 5LP Low Power Modes and Power Reduction Techniques
- AN72382 – Using PSoC 3 and PSoC 5LP GPIO Pins
- AN60580 – PSoC 3 and PSoC 5LP SIO Tips and Tricks
- AN60616 – PSoC 3 and PSoC 5LP Startup Procedure
- AN60631 – PSoC 3 and PSoC 5LP Clocking Resources
- AN54439 – PSoC 3 and PSoC 5LP External Oscillator
- AN72845 – Design Guidelines for QFN Packaged Devices
- AN89611 – PSoC 3 and PSoC 5LP Getting Started with Chip Scale Packages
- AN69061 – Design, Manufacturing, and Handling Guidelines for Cypress Wafer Level Chip Scale Packages
- AN88619 – PSoC 4 Hardware Design Considerations
- AN80994 – Design Considerations for Electrical Fast Transient (EFT) Immunity
- AN64846 – Getting Started with CapSense

Cypress PSoC 3 and PSoC 5LP kit schematics are good examples of how to incorporate PSoC into board schematics. It may be helpful to review the following Cypress kit schematics:

- CY8CKIT-001 common development platform with CY8CKIT-009 PSoC 3 processor module.
- CY8CKIT-001 common development platform with CY8CKIT-010 PSoC 5LP processor module.
- CY8CKIT-030 PSoC 3 precision analog development kit
- CY8CKIT-050 PSoC 5LP precision analog development kit
- CY8CKIT-059 PSoC 5LP low cost development kit

Note: On the kit web page, scroll to the link “Board Design Files (Schematic, … “.

An Altium designer library is available for PSoC 3 and PSoC 5LP in the various supported packages.

About the Author

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Appendix A. PCB Layout Tips

Note: Before beginning a PCB layout for PSoC, it is a good idea to look at AN57821, PSoC Mixed Signal Circuit Board Layout Considerations. Appendix A of that application note shows example PCB layouts and schematics for various PSoC 3 and PSoC 5LP packages. The same information for the 100-TQFP package is in the device datasheet.

Note: Cypress PSoC 3 and PSoC 5LP kit schematics provide good examples of how to incorporate PSoC into board schematics. For more information, see Related Documents.

There are many classic techniques for designing PCBs for low noise and electromagnetic compatibility (EMC). Some of these techniques include:

- **Multiple layers:** Although they are more expensive, it is best to use a multi-layer PCB with separate layers dedicated to the V_{SS} and V_{DD} supplies. This gives good decoupling and shielding effects. Provide separate fills on these layers for V_{SSA}, V_{SSD}, V_{DDA}, and V_{DDD}.

  To reduce cost, a 2-layer or even a single-layer PCB can be used. In that case, you must have a good layout for all V_{SS} and V_{DD}.

- **Ground and Power Supply:** There should be a single point for gathering all ground returns. Avoid ground loops, or minimize their surface area. All component-free surfaces of the PCB should be filled with additional grounding to create a shield, especially when using 2-layer or single-layer PCBs.

  The power supply should be close to the ground line to minimize the area of the supply loop. The supply loop can act as an antenna and can be a major emitter or receiver of electromagnetic interference (EMI).

- **Decoupling:** The standard decoupler for external power is a 100 µF capacitor. Supplementary 0.1 µF capacitors should be placed as close as possible to the V_{SS} and V_{DD} pins of the device, to reduce high frequency power supply ripple.

  Generally, you should decouple all sensitive or noisy signals to improve EMC performance. Decoupling can be both capacitive and inductive.

- **Component Position:** You should separate the different circuits on the PCB according to their EMI contribution. This helps reduce cross-coupling on the PCB. For example, separate noisy high current circuits, low voltage circuits, and digital components.

- **Signal Routing:** Check the routing of the following signal types to improve EMC performance:
  - Noisy signals, for example signals with fast edge times
  - Sensitive and high impedance signals
  - Signals that capture events, such as interrupts and strobe signals

  To increase EMC performance, keep the trace lengths as short as possible, and isolate the traces with V_{SS} traces. To avoid crosstalk, do not route traces near or parallel to other noisy and sensitive traces.

For more information, several references are available:

- The Circuit Designer's Companion, Second Edition, (EDN Series for Design Engineers) by Tim Williams
- PCB Design for Real-World EMI Control (The Springer International Series in Engineering and Computer Science), by Bruce R. Archambeault and James Drewniak
- Printed Circuits Handbook (McGraw Hill Handbooks), by Clyde Coombs
- EMC and the Printed Circuit Board: Design, Theory, and Layout Made Simple, by Mark I. Montrose
- Signal Integrity Issues and Printed Circuit Board Design, by Douglas Brooks
- Cypress AN80994, PSoC 3, PSoC 4, and PSoC 5LP EMC Best Practices

Appendix B. Schematic Checklist

Each item in the following checklist should be confirmed (☑) or noted as not applicable (NA). For example, if you choose unregulated mode, you can mark all the items of Power (regulated mode) as NA

Catalog	Item	☑ / NA	Remark
Power	Is the voltage at the V_{DDA} pin always greater than or equal to the voltages at the V_{DDD} and V_{DDIO} pins?		
	If there are multiple power domains on the PCB, have the V_{DDIOx} pins been assigned accordingly?		
	Are the correct capacitors connected to each V_{DDA}, V_{DDD}, and V_{DDIO} pin? Do the capacitors have appropriate working voltage and DC bias specifications?		
	Are the correct capacitors connected to each V_{CCA} and V_{CCD} pin? Do the capacitors have appropriate working voltage and DC bias specifications?		
	Are the power voltage ramp-up speeds limited?		
	Do the PSoC Creator DWR settings match the actual V_{DDX} voltages?		
	For each V_{DDIO}, are the total I/O currents less than the current limit?		
	Does your package selection have the correct thermal resistance for your anticipated total chip power?		
Boost	Have you determined the correct input and output voltages, and component values?		
	Are the PSoC Creator Boost Component settings correct?		
	If the boost is NOT being used: Are the V_{BAT}, V_{SSB}, and V_{BOOST} pins connected to ground, and is the IND pin unconnected?		
Power (regulated mode)	Are the power supply pin connections made in accordance with Figure 1?		
	Are the voltages (including ripples) at each V_{DDA}, V_{DDD}, and V_{DDIO} pin in the range of 1.8 V to 5.5 V?		
Power (unregulated mode)	Are you NOT using USB?		
	Are the voltages (including ripples) at each V_{CCA} and V_{CCD} pin in the range of 1.71 V to 1.89 V?		
	Are the V_{DDX} pins tied to the respective V_{CCX} pins?		
	Do you have code to turn off the regulators?		
I/O Pins	Have your pin selections been optimized for your PCB / application? See I/O Pin Selection on page 9.		
	Is there voltage level shifting associated with any I/O pins? Are correct circuits for level shifting designed in?		
	Have the reset states for all I/O pins been determined and set correctly?		
	For devices with a configurable P1[2] that is configured as a GPIO, is the pin configured as a digital input with the resistive pull-up enabled?		
	Are all unused I/O pins left floating and in the high-impedance analog state?		
	Have slew rate options been set for low-frequency signals, to reduce EMI?		
	Have series resistors been added to all pins being routed off the PCB, for ESD protection?		
	Are all device pins marked “do not use” (DNU) left unconnected and floating? Note that in devices without USB the USBIO pins are DNU.		
Reset	Is the reset pin connection in accordance with Device Reset on page 14?		
	Is there voltage level shifting associated with the reset pin? Is a correct circuit for level shifting designed in?		
	Is the PSoC Creator DWR setting for Reset correct?		
Programming and Debugging	Are the JTAG or SWD pin connections in accordance with Programming and Debug on page 15?		
	Are the PSoC Creator DWR settings for Programming and Debug correct?		

Catalog	Item	☑ / NA	Remark
Oscillators	Are the crystals and external components connected correctly?		
	Are the PSoC Creator DWR settings for Programming and Debug correct?		
Analog Connections	Is the PSoC Creator Delta-sigma ADC Component reference option set correctly for the pin being used? Is a bypass capacitor connected to the correct pin?		
	Are the PSoC Creator SAR ADC Component reference options set correctly for the PSoC 5LP pins being used? Are bypass capacitors connected to the correct pins?		
	Are the IDACs with the high output current option routed to the correct pins?		
	Are the opamp +, -, and output terminals routed to the correct pins?		
PCB	Does your PCB layout implement the techniques suggested in Appendix A?		

Document History

Document Title: AN61290 - PSoC 3 and PSoC 5LP Hardware Design Considerations

Document Number: 001-61290

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2924169	KHE	04/29/2010	New Application Note
*A	3412687	MKEA	11/01/2011	Revised and added content for PSoC Creator 2.0 and PSoC 5, and for customer feedback Updated template
*B	3437958	MKEA	11/14/2011	Updated Thermal Considerations section
*C	3468199	MKEA	12/18/2011	Modified description of PSoC 3 and PSoC 5 maximum source and sink currents.
*D	3478442	MKEA	12/29/2011	Updated reference to application note AN72382 on page 6 and 15 Fixed typo
*E	3524079	MKEA	02/13/2012	Added note for Vccx capacitors for PSoC 5 sleep mode. Clarified that configurable reset on P1[2] is not available on PSoC 5.
*F	3616646	MKEA	05/14/2012	Added references to two application notes and the PSoC Programming Guide. Added section on powering in unregulated mode. Updated template.
*G	3819481	MKEA	11/22/2012	Updated for PSoC 5LP and PSoC Creator 2.1 SP1.
*H	3935205	MKEA	03/15/2013	Added Package Selection section. Clarified Vddio source / sink. Added references to AN57821. Replaced references to AN66083 with AN77900. Updated Figure 15. Miscellaneous text updates.
*I	4036570	MKEA	06/21/2013	Added references to CY kit schematics. Deleted reference to obsolete application note AN53781. Miscellaneous text and formatting changes.
*J	4150362	MKEA	12/13/2013	Added text and references for CSP packages. Added text on reduced capacitance with DC bias Added link to PSoC 3 and PSoC 5LP Altium Designer Library.
*K	4284914	MKEA	02/18/2014	USBIO descriptions updated in multiple sections. Analog sections revised to mention Analog Device Editor. Updated for 80 MHz PSoC 5LP. Miscellaneous minor edits.
*L	4381386	MKEA	05/16/2014	Added Appendix B. Miscellaneous minor edits.
*M	4488726	MKEA	09/12/2014	Clarified usage of P1[2] as a configurable GPIO, in high-reliability applications.
*N	4829706	GJV	07/09/2015	Corrected boost pin names and added updated boost block diagram.
*O	5705702	BENV	04/21/2017	Updated logo and copyright
*P	5882424	MKEA	09/13/2017	Added section 3.3, External Regulator Considerations. Added section 4.3, I/O Pins and Level Shifting. Added level shifting to the checklist in Appendix B. Added a statement on usage of TVS diodes to section 4.5, EMC / ESD Protection Added references to AN64846, Getting Started with CapSense. Other miscellaneous edits.

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