Alexander D. **Gotsis**

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Education

Carnegie Mellon University — *Pittsburgh, Pennsylvania*

M.S. in Electrical and Computer Engineering with University Honors (Overall GPA 3.67/4.00) — *May 2020*

B.S. in Electrical and Computer Engineering with University Honors (Overall GPA 3.49/4.00) — *May 2019*

- CIT Dean's List Fall 2015, Spring 2017, and Spring 2018, Senior Leadership Recognition, University Honors

Selected Coursework

Operating Systems Design & Impl.	Embedded Systems Software Engineering	Advanced Storage Systems	Capstone Design
Logic Design and Verification	Intro to Computer Architecture	Structure & Design of Digital Systems	Secure Coding

Experience

VMware — *Palo Alto, California*

Member of Technical Staff 3 - Virtual Machine Monitor Team — *May 2020 - Present*

- The Virtual Machine Monitor (VMM) team handles core CPU virtualization for server and hosted VMware products and manages components of the virtual platform, including many virtual devices.
- Core member of subteam developing general purpose API for vendors to create virtual devices based on hardware (PCI, SR-IOV, S-IOV) that are capable of live-migration to other hosts and suspend/resume. State must be extracted from devices.
- Devise and implement method to use IOMMU to track DMA by hardware to VM main memory, allowing live-migration of virtual devices based on physical devices. Work on this initiative required working at all levels of the kernel and user components of virtualization.
- Contribute to implementation of virtual machine monitor for the ARM architecture and effort to deprivilege much of the monitor.

NVIDIA — *Santa Clara, California*

GPU RTL Design + Verification Intern - CUDA Unified Virtual Memory Systems Software Intern — *July 2019 - December 2019*

- Perform bugfixes and improvements on the Unified Virtual Memory (UVM) Linux kernel module of the CUDA kernel-mode driver and its unit and performance tests. Implement and verify a new cross-platform performance test for the Copy Engine to guide development.
- Improvements to GPU Frontend (FE) design and verification team infrastructure and performance suite.

MITRE — *Bedford, Massachusetts*

Embedded Software Intern — *May 2018 - August 2018*

- Develop and test a multiple power & clock fault testing/exploitation suite as Python interfaces for Arbitrary Waveform Generators.
- Profile Dwenguino AVR instructions and develop suite for profiling other hardware implementations.
- Alter programmable logic for secure video game console eCTF to store symmetric keys. Win 2nd place in eCTF and Iron Flag Award.

Robotany — *Pittsburgh, Pennsylvania*

Electrical Engineering Power Systems Intern — *May 2017 - May 2018*

- Design 3-phase delta 240V electrical power system for robotic vertical farm, fixture wiring, and control racks.
- Specify and implement power system including conduits, transformers, and load centers. Manage and direct assembly teams.

Skills & Hobbies

C / C++ (Exp.)	OS / Kernel (Exp.)	Python (Adv.)	ARM	Embedded	FPGAs	Computer Architecture	Climbing
Rust (Int.)	UNIX (Adv.)	Git	x86	Lab Equipment	SystemVerilog	Rapid Prototyping	Backpacking

Projects & Extracurriculars

- **Pop Up Metro** Miscellaneous Consulting (2021-Present)
  Pop Up Metro provides trials of transit systems with battery powered metro cars. Consult on projects for a battery charger and signal lights.
- **UNIX-like Kernel from Scratch** Operating Systems Design & Implementation - 15-410 / 605 (Spring 2018)
  Designed & implemented the entirety of a small (14k loc) and robust UNIX-like kernel on x86-32 with a partner over 8 weeks. Some features include kernel-level threads, user-level threads, condition variables, mutexes, readers-writers locks, and virtual memory management.
- **RTL Design/Verification Projects** Logic Design & Verification - 18-341 (Fall 2018), Computer Architecture - 18-447 (Spring 2019)
  Designed & implemented optimized pipelined matrix multiply-accumulate, concurrent "NoC" packet router, and more in SystemVerilog. Implemented a series of increasingly complex RISC-V processors ranging from a single-cycle design to an out-of-order architecture.
- **MIT Mystery Hunt 2023** Puzzle Author, Puzzle Editor, Technical Team (Jan 2022 - Present)
  Author, edit, and work on technical infrastructure of puzzlehunt to have at least 100 puzzles. Focus on backend & interactive components.
- **Activities Board Technical Committee** Core Member & Executive Board (2015 - 2020)
  Direct & implement production services for campus events including 3-phase power systems, rigging, and professional audio & lighting.
- **CMU Explorers Club (CMUX)** Member (2015), Hiking Chair & Treasurer (2016-2020)
  CMUX is an club dedicated to making outdoor activities more accessible. Organize hikes as Hiking Chair. Manage finances as Treasurer.