Computer Organization & Architecture

UNIT-1

Fixed point and Floating point Number representation:

1. Program has 50 instructions, an average 5 clocks per instructions, the CPU executer 1 MHz clock rate. How much time is required to execute this program?

2. Two machine designs were proposed M_1 uses 2 MHz clock and consume 20% extra clocks per instruction with respect to M_2. If it is required the speed up of machine-1 is 2.2 times compared to machine -2. What should be the clock frequency of machine- 2

3. A program has 60% floating point operations and 40% integer operations. Floating point operation takes twice of integer operation in machine A. In its improved version 'B' floating point operation takes $\frac{1}{3}$ of time when compared to A. What is the speed up with improved version?

4. Consider the signed number is represented in 2's complement notation and it is placed in 16-bit register, the number P = F87BH.
   Which of the following 4-digit hexadecimal number gives P × 8 is
   (A) $(C3D8)_{16}$ (C) $(F878)_{16}$
   (B) $(187B)_{16}$ (D) $(987B)_{16}$

5. Which of the following multiplier pattern is exactly devisable by 1111 1111 1011. Let 2's Complement notation is use for representing the number
   (A) 1111 111 0000 (C) 10001
   (B) 1111 111 0010 (D) 1111 1000 0000

6. Which of the following answer gives the multiplication of two signed numbers which are represented in 2's complement
   1111 1010 × 0000 1010
   (A) 1000 (C) 60
   (B) −100 (D) −60

7. The range of integers that can be represented by an n-bit 2's complement number system is
   (A) $-(2^{n-1})$ to $(2^{n-1}-1)$
   (B) $-(2^{n-1}-1)$to $(2^{n-1}-1)$
   (C) $-2^{n-1}$to 2^{n-1}
   (D) $-(2^{n-1}+1)$to $(2^{n-1}-1)$

8. The 2's complement representation of $(-539)_{10}$ in hexadecimal is
   (A) ABE
   (B) DBC
   (C) DE5
   (D) 9E

9. Represents the following numbers in 2's complement binary representation
   (A) $(-43)_{10}$
   (B) $(-23)_{10}$
   (C) $(-123)_{10}$

10. The 2's complement representation of $(-539)_{10}$ in hexadecimal is
    (E) ABE
    (F) DBC
    (G) DE5
    (H) 9E

11. A) Let P, Q, R are 8- bit binary signed number represented in sign magnitude, 1's complement and 2's complement notations respectively, value of $P \times R + Q$ in 2's complement notation

$P = 10101010$, $Q = 1111\ 1111$, $R = 1111\ 1111$

B) If the binary pattern of 'p' is denoted in 2's complement notation its value in decimal

c) Two's complement notation is used to represent P, Q.

$P = 1111\ 1011$

$Q = 1100\ 1101$

Statement 1: P is exactly divisible by -3

Statement 2: Q is exactly divisible by -5

(A) Only S_1 is true
(B) Only S_2 is true
(C) Both statement is true
(D) Neither True

12. The n-bit fixed point representation of an unsigned real number X uses f bits for the fraction part. Let $i = n - f$,the range of decimal values for 'X' in this representation

(A) 2^{-f} to 2^{i}
(B) 2^{-f} to $\left(2^{i} - 2^{-f}\right)$
(C) 0 to 2^{c}
(D) 0 to $2^{i} - 2^{-f}$

13. Consider a 16-bit register of the following format is used to store floating point number. Mantissa is normalized signed magnitude fraction, exponent is in excess 64-form, the base of the system is '2'
    (a) How many bits allocated for fraction mantissa?
    (b) Express the largest value stored in the above register as the power of '10'
    (c) What is the 16-bit pattern that represents $(-21.75)_{10}$ in the above register?

14. Consider the following 16-bit register which is used to store floating point number

S	$E_{(K)}$	$M_{(9)}$

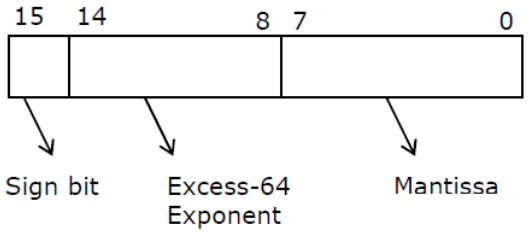
    Mantissa = Normalized sign magnitude fraction form
    Exponent = Biased form
    Base =2
    (a) What is the bias and value expression
    (b) What is the range of positive mantissa
    (c) Discuss above the distribution
    (d) Pattern for $(13.7)_{10} \times 2^{13}$

15. Consider an IBM system which uses 32-bit register for representing the floating point number the mantissa is implicit normalized number exponent is in excess 128- form and the base of the system is - 2
    What will be the 8-digit hexadecimal pattern for storing the $(63.5)_{10}$ value?

16. An IBM system uses 32-bit register to represent floating point value. Base of the system is 16, bias is excess 64-form, and mantissa is normalized sign magnitude fraction
    (a) 8-digit hexadecimal pattern which represents decimal $(7.5)_{10}$ value.
    (b) Range of positive mantissa

Statement for Linked Answer Questions 15 and 16

Consider the following floating-point format.



Mantissa is a pure fraction in sign-magnitude form.

17. The decimal number 0.239×2^{13} has the following hexadecimal representation (without normalization and rounding off):
    (A) 0D 24
    (B) 0D 4D
    (C) 4D 0D
    (D) 4D 3D

18. The normalized representation for the above format is specified as follows. The mantissa has an implicit 1 preceding the binary (radix) point. Assume that only 0's are padded in while shifting a field.

    The normalized representation of the above number (0.239×2^{13}) is:

    (A) 0A 20
    (B) 11 34
    (C) 49 D0
    (D) 4A E8

19. It is required to store $(-14.25)_{10}$ in IEEE754 single precision. Which of the hexadecimal pattern denote this value?
(A) C164 0000
(B) 416C 0000
(C) 4164 0000
(D) C16C 000

20. Consider a 32-bit register which is used to store the floating point number in single precision IEEE 754 format. Compute the value given by the register

01000 00111 0000 …….. 0
31 0

21. Hexadecimal pattern "$-\infty$" in IEEE 754 format
(A) 0x ffff ffff
(B) 0x fff ffff
(C) 0x ff80 0000
(D) 0x ffff 8000

22. If the 32-bit register is having all one's

31 0
111 ……..1

(A) $-\infty$
(B) $2^{-\infty}$
(C) $2^{+\infty}$
(D) NAN

23. Given the following binary number in 32-bit (single precision) IEEE–754 format:
00111110011011010000000000000000
The decimal value closest to this floating-point number is
(A) 1.45×10^{1}
(B) 1.45×10^{-1}
(C) 2.27×10^{-1}
(D) 2.27×10^{1}

24. The decimal value 0.5 in IEEE single precision floating point representation has
(A) fraction bits of 000…000 and exponent value of 0
(B) fraction bits of 000…000 and exponent value of -1
(C) fraction bits of 100…000 and exponent value of 0
(D) no exact representation

25. Which of the following operation result in overflow in case of 1's complement arithmetic? Assume the size of the operand is 8-bit.
(A) 1111 1111 + 0000 0000
(B) 1111 0000 + 0000 1111
(C) 1111 1111 + 1111 1111
(D) 0100 0001 + 0100 0000

26. Consider $Z = X + Y$ and Z_s , X_s Y_s are denoting the sign bits. Which of the following expression indicating an overflow
(A) $X_s \oplus Y_s \oplus Z_s$
(B) $X_s \odot Y_s \odot Z_s$
(C) $Z_s X_s' Y_s' + X_s Y_s Z_s'$
(D) $X_s' Y_s Z_s + X_s Y_s' Z_s$

27. When two 8-bit numbers $A_7 \ldots A_0$ and $B_7 \ldots B_0$ in 2's complement representation (with A_0 and B_0 as the least significant bits) are added using a ripple-carry adder, the sum bits obtained are $S_7 \ldots S_0$ and the carry bits are$C_7 \ldots C_0$. An overflow is said to have occurred if

(A) the carry bit C_7 is 1

(B) all the carry bits ($C_7 \ldots C_0$) are 1

(C) $(A_7 . B_7 . \bar{S}_7 + \bar{A}_7 . B_7 . S_7)$ is 1

(D) $(A_0 . B_0 . \bar{S}_0 + \bar{A}_0 . \bar{B}_0 . S_0)$ is 1

28. What is the booths recording pattern for $(-43)_{10}$

UNIT- 2
MEMORY ORGANIZATION

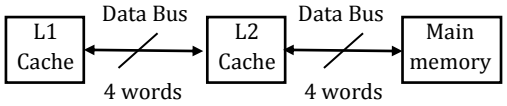
Memory Hierarchy and Cache Memory:

29. Consider a 2 level memory system, where L_1 memory is twice faster than L_2 has hit ratio 80% with access time 20ns.
    (i) What is average access time?
    (ii) What is the throughput of this memory system?
    (iii) If Hit ratio is 100% in L_1. What will be the access time of L_2 Memory?

30. Consider a 3-level memory system of the following specification
    $T_1 = 10\,\text{ns/word}\,, H_1 = 80\%$
    $T_2 = 50\ \text{ns/word}, H_2 = 90\%$
    $T_3 = 200\ \text{ns/word}, H_3 = 100\%$
    If the referred word is available in leavel-1 memory it is handover to the processor, If it is not available in level-1, a two-word block is first is moved from level-2, to level-1 and from L_1 is given to the processor, if it is not present even in level-2 and 4-word block is front moved from level-3 to level-2 and associated block is moved from leavel-2 to level-1
    (A) What is the average access time?
    (B) What is the throughput of 3 level memory systems?

Common Data for Questions 30 and 31

A computer system has an L1 and an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words, the block size in L2 cache is 16 words. The memory access times are 2 nanoseconds, 20 nanoseconds & 200 nanoseconds for L1 cache, L2 cache and main memory unit respectively.



31. When there is a miss in L1 cache and a hit in L2 cache, a block is transferred from L2 cache to L1 cache. What is the time taken for this transfer?
    (A) 2 nanoseconds
    (B) 20 nanoseconds
    (C) 22 nanoseconds
    (D) 88 nanoseconds

32. When there is miss in both L1 cache and L2 cache, first a block is transferred from main memory to L2 cache, and then a block is transferred from L2 cache L1 cache. What is the total time taken for these transfers?
    (A) 222 nanoseconds
    (B) 888 nanoseconds
    (C) 902 nanoseconds
    (D) 968 nanoseconds

33. Consider a main memory of 2 million words and cache memory of 32 KB, both are partitioned into 1K word blocks and the word size is 16 bits
    (A) How many bits required for physical address?
    (B) How many blocks are present in main memory and in cache memory
    (C) What will be the number of TAG bits and TAG memory with respect to the following address mapping
        (a) Direct address mapping
        (b) Associative mapping
        (c) 4-way set associative mapping
        (d) It is required to divide cache controller for TAG matching. Each entry of TAG controller maintains TAG information of the block along with '1' used bit, 1 modified bit, and 1 valid bit. How much memory is required for cache controller for this Meta data for each of the above mappings?
34. Consider a 32-bit processor which contains 2 GB main memory, 512 cache blocks. Each block maintains 128 bytes.
    a) What will be the number of bits required for physical address?
    b) If it is 4-way set associative. How many bits will be present in word field , tag field and set offset.
    c) Find out number of bits in cache index.
35. A cache contains 'n'blocks with each block having 'n' words. The number of TAG bits for this direct mapping is 'n'. How many words are present in physical memory

36. Consider 2 cache organizations ,First one is 32 KB, two-way set associative with 32 byte block size, the second is of same size with direct mapped. In the both case the physical address is 32-bit. A 2×1 multiplexer has latency of 0.6ns, while a k−bit comparator has latency of $\frac{k}{10}$ ns. If the hit latency of the set associative mapped cache H_1 and direct mapped cache is H_2
    1. The value of H_1 is?
        (A) 2.4 ns
        (B) 2.3 ns
        (C) 1.8 ns
        (D) 1.7 ns
    2. The value of H_2 is?
        (A) 2.4 ns
        (B) 2.3 ns
        (C) 1.8 ns
        (D) 1.7 ns

37. A Cache memory has 80% hit for read operation and 90% for write operation, T_C(Time for access cache) = 10ns/word and T_m(Time for memory access) =100 ns/w. Whether it is read (or) Write miss, entire 2-load block is to be moved from main memory to cache. Let there are 20% references are for write operations with write-through
    (A) What is average read access time
    (B) What is average write access time
    (C) What is average access time when both read and write are considered
    (D) Through put of the memory system
    (E) Repeat the above problem with write back strategy so that at any point of time 30% cache blocks are dirty. Assume that cache is full initially

38. In a specific implementation the cache hit takes 2 clocks for read operation, 5 clock for cache miss for write operation the cache hit takes 4 clocks and cache miss takes 10 clocks. The hit ratio for both read and write is 80%, A program requires 60 instructions fetches, 100 operand fetches, and 100 operand write operations. How many clocks are required on an average per operation_____

39. Consider a cache of 4 blocks is used to satisfy following the main memory references, initially the cache is empty. Compute the number of HITs and cache status per FIFO, LRU, OPTIMAL, DIRECT MAPPING, & 2-way set associative.
    References are :7,4,13,4,7,12,19,4,26,12,12,110,19,12,&7

40. Consider a Direct Mapped Cache with 8 cache blocks (numbered 0−7). If the memory block requests are in the following order 3, 5, 2, 8, 0, 63, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24. Which of the following memory blocks will not be in the cache at the end of the sequence?
    (A) 3 (C) 20
    (B) 18 (D) 30

41. Consider a direct mapped cache of 8 blocks is used for implementing following program segment:

```
float a[10][10]
        int i ;
For (i=0; i<10;i++)
        For (j=0;j<10;j++)
                A[i][j]=8.0;
```

    Float element occupies 4bytes, the block size is 12bytes and Array is stored in ROW MAJOR ORDER (RMO). Find out number of hits____

42. Consider machine with 2-way set associative data cache of size 64KB, block size is 16bytes. The cache is managed using 32-bit virtual address page size is 4KB and Array APR[1024][1024] is stored in virtual page OXFF000 and it is stored in row major order[RMO], the cache is initially empty, no prefetching is done with respect to the only data reference of the following program.

```
Double APR [1024][1024]
        int i,j;
  For (i = 0; i < 1024; i + +)
        For (j = 0; j < 1024 ; j + +)
                APR [j][j] = 0.0;  (Let the size of the double is 8 bytes)
```

1).Total size of the TAG in cache directory is

(A) 32 kbits
(B) 34 kbits
(C) 64 kbits
(D) 68 kbits

2). what is the hit ratio for this initialization program is

(A) 0%
(B) 25%
(C) 50%
(D) 75%

3). Which of the following array element has the same cache index as APR[0][0]

(A) APR[0][4]
(B) APR[4][0]
(C) APR[0][5]
(D) APR[5][0]

43. The read access times and the hit ratios for different caches in a memory hierarchy are as given below:

Cache	Read access time(in nanoseconds)	Hit ratio
I-Cache	2	0.8
D-Cache	2	0.9
L2-Cache	8	0.9

The read access time of main memory is 90 nano-seconds. Assume that the caches use the referred-word-first read policy and the write back policy. Assume that all the caches are direct mapped caches. Assume that the dirty bit is always 0 for all the blocks in the caches. In execution of a program, 60% of memory reads are for instruction fetch and 40% are for memory operand fetch. The average read access time in nanoseconds (up to 2 decimal places) is _____

44. In a k – way set associative cache, the cache is divided into v sets, each of which consists of k lines. The lines of a set are placed in sequence one after another. The lines in set s are sequenced before the lines in set (s+1). The main memory blocks are numbered 0 onwards. The main memory block numbered j must be mapped to any one of the cache lines from

(A) (j mod v)×k to (j mod v) × k+(k−1)
(B) (j mod v) to (j mod v) +(k−1)
(C) (j mod k) to (j mod k) +(v−1)
(D) (j mod k)× v to (j modk) ×v+(v−1)

45. Consider a machine with a byte addressable main memory of 2^{32} bytes divided into blocks of size 32 bytes. Assume that a direct mapped cache having 512 cache lines is used with this machine. The size of the tag field in bits is _____
46. Assume that for a certain processor, a read request takes 50 nanoseconds on a cache miss and 5 nanoseconds on a cache hit. Suppose while running a program, it was observed that 80% of the processor's read requests result in a cache hit. The average read access time in nanoseconds is ____.
47. The size of the physical address space of a processor is 2^P bytes. The word length is 2^W bytes. The capacity of cache memory is 2^N bytes. The size of each cache block is 2^M words. For a K-way set-associative cache memory, the length (in number of bits) of the tag field is
    (A) $P - N - \log2\ K$ (B) $P - N + \log2\ K$
    (C) $P - N - M - W - \log2\ K$ (D) $P - N - M - W + \log2\ K$

48. A computer system implements a 40-bit virtual address, page of 8 kilobytes, and a 128-entry translation look-aside buffer (TLB) organized into 32 sets each having four ways. Assume that the TLB tag does not store any process id. The minimum length of the TLB tag in bits is _____
49. A certain processor uses a fully associative cache of size 16 kB, The cache block size is 16 bytes. Assume that the main memory is byte addressable and uses a 32-bit address. How many bits are required for the Tag and the Index fields respectively in the addresses generated by the processor?
    A).24 bits and 0 bits B). 28 bits and 4 bits C).24 bits and 4 bits D).28 bits and 0 bits
50. In a two-level cache system, the access times of L_1 and L_2 caches is 1 and 8 clock cycles, respectively. The miss penalty from the L_2 cache to main memory is 18 clock cycles. The miss rate of L_1 cache is twice that of L_2. The average memory access time (AMAT) of this cache system is 2 cycles. The miss rates of L_1 and L_2 respectively are
    (A) 0.111 and 0.056
    (B) 0.056 and 0.111
    (C) 0.0892 and 0.1784
    (D) 0.1784 and 0.0892

51. An 8KB direct-mapped write-back cache is organized as multiple blocks, each size of 32-bytes. The processor generates 32-bit addresses. The cache controller contains the tag information for each cache block comprising of the following.
    1 valid bit,1 modified bit
    As many bits as the minimum needed to identify the memory block mapped in the cache.
    What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache?
    (A) 4864 bits
    (B) 6144 bits
    (C) 6656 bits
    (D) 5376 bits
52. Consider a 4-way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates a 20-bit address of a word in main memory. The number of bits in the TAG, LINE and WORD fields are respectively:
    (A) 9, 6, 5
    7, 7, 6
    (B) 7, 5, 8
    (C) 9, 5, 6

Statement for Linked Answer Questions 51 and 52

A computer has a 256-KByte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

53. The number of bits in the tag field of an address is
    (A) 11
    (B) 14
    (C) 16
    (D) 27

54. The size of the cache tag directory is
    (A) 160 Kbits
    (B) 136 Kbits
    (C) 40 Kbits
    (D) 32 Kbits
55. If the associativity of a processor cache is doubled while keeping the capacity and block size unchanged, which one of the following is guaranteed to be NOT affected?
    (A) Width of tag comparator
    (B) Width of set index decoder
    (C) Width of way selection multiplexor
    (D) Width of processor to main memory data bus
56. The amount of ROM needed to implement a 4-bit multiplier is
    (A) 64 bits (B) 128 bits (C) 1k bits (D) 2k bits

57. A RAM chip has a capacity of 1024 words of 8 bits each (1K × 8). The number of 2 ×4 decoders with enable line needed to construct a 16K × 16 RAM from 1K ×8 RAM is____

UNIT -3

Instructions Formats, Addressing Modes and Instructions Pipeline

58. A processor has 64 registers and certain 32-bit ISA (Instruction Set Architecture) and it supports 256 Instructions. If the instruction format

Opcode	Reg 1	Reg 2	Immediate operand

What is the maximum value unsigned integer supported by immediate operand?

59. m-bit instruction is stored in 2^n word memory .The system supported 1-address and 2-address instructions. If there are 'q' 2-address instructions in Instruction Set Architecture (ISA). What will be the number of 1-address instructions?

60. Consider a hypothetical processor with an instruction of type LW R1, 20(R2), which during execution reads a 32-bit word from memory and stores it in a 32-bit register R1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register R2. Which of the following best reflects the addressing mode implemented by this instruction for the operand in memory?

(A) Immediate addressing
(B) Register addressing
(C) Register Indirect Scaled Addressing
(D) Base Indexed Addressing

61. A processor has 16 integer registers (R0, R1, .. , R15) and 64 floating point registers (F0, F1... F63). It uses a 2-byte instruction format. There are four categories of instructions: Type-1, Type-2, Type-3, and Type-4. Type-1 category consists of four instructions, each with 3 integer register operands (3Rs). Type-2 category consists of eight instructions, each with 2 floating point register operands (2Fs). Type-3 category consists of fourteen instructions, each with one integer register operand and one floating point register operand (1R+1F). Type-4 category consists of N instructions, each with a floating point register operand (1F). The maximum value of N is _____.

62. A hypothetical machine supports both one-address and 2-address instructions, the 16-bit instruction are stored in 128-word memory, if there are '2' two-address instructions. What will be the number of 1-address instructions supported by this machine?

(A) 128 (B) 256 (C) 512 (D) 384

63. Consider a processor with byte addressable memory. Assume that all registers, including Program Counter (PC) and Program Status Word (PSW), are of size 2 bytes. A stack in the main memory is implemented from memory location (0100)16 and it grows upward. The stack Pointer (SP) point to the top element of the stack. The current value of SP is (016E)16. The CALL instruction is of two words, the first word is the op-code and the second word is the starting address of the subroutine (one word =2 bytes). The CALL instruction is implemented as follows:

- Store the current value of PC in the stack
- Store the value of PSW register in the stack
- Load the starting address of the subroutine in PC

The content of PC just before the fetch of a CALL instruction is (5FA0)16. After execution of the CALL instruction, the value of the stack pointer is

(A) $(016A)_{16}$ (B) $(016C)_{16}$ (C) $(0170)_{16}$ (D) $(0172)_{16}$

64. Which of the following is/are true of the auto increment addressing mode?

1. It is useful in creating self -relocating code
2. If it is included in an Instruction Set Architecture, then an additional ALU is required for effective address calculation
3. The amount of increment depends on the size of the data item accessed

(A) 1 only (B) 2 only (C) 3 only (D) 2 and 3 only

65. Match each of the high level language statements given on the left hand side with the most natural addressing mode from those listed on the right hand side.

1. A[I]=B[J];	a) indirect addressing
2. while [*A++];	b) indexed addressing
3. int temp=*x;	c) Auto increment

66. Consider a RISC machine where each instruction is exactly 4 bytes long. Conditional and unconditional branch instructions use PC-relative addressing mode with Offset specified in bytes to the target location of the branch instruction. Further the Offset is always with respect to the address of the next instruction in the program sequence. Consider the following instruction sequence

If the target of the branch instruction is i, then the decimal value of the Offset is _____ .

Instruction Number	Instruction
i:	Add R2,R3,R4
i+1:	Sub R5,R6,R7
i+2:	cmp R1,R9,R10
i+3:	beq R1, offset

67. Match the following :

Addressing Mode	Location of operand
a. Implied	i. Registers which are in CPU
b. Immediate	ii. Register specifies the address of the operand

c. Register d. Register Indirect	iii. Specified in the register iv. Specified implicitly in the definition of instruction

Codes:

	a	B	c	d
(A)	iv	Iii	i	ii
(B)	iv	I	iii	ii
(C)	iv	Ii	i	iii
(D)	iv	Iii	ii	i

68. Matchings:

X. Indirect Y. Immediate Z. Auto decrement	1. Loop 2. Pointers 3. Constant

69. Matchings:

x. Indirect y. Indexed z. Base register	1. Array Implementation 2. Relocatable writing 3. Passing array as parameter

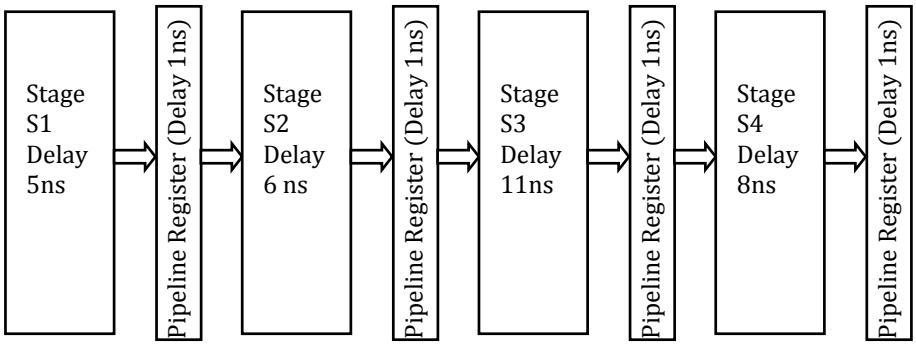
70. Matchings:

P. Base Q. Index R. Stack S. Implied	1. Reentry 2. Accumulator 3. Array 4. Position Independent code

71. Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delays for FI, DI, FO, EI and WO are 5ns, 7ns, 10ns, 8ns and 6ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 12 instructions I1, I2, I3… I12 is executed in this pipelined processor. Instruction I4 is the only branch instruction and its branch target is I9. If the branch is taken during the execution of this program , the time (in ns) needed to complete the program is

(A) 132 (B) 165 (C) 176 (D) 328

72. Consider an instruction pipeline with four stages (S1, S2, S3 and S4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure



What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?

(A) 4.0 (B) 2.5 (C) 1.1 (D) 3.0

73. Instruction execution in a processor is divided into 5 stages. Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Execute (EX), and Write Back (WB). These stages take 5, 4, 20, 10, and 3 nanoseconds (ns) respectively. A pipelined implementation of the processor requires buffering between each pair of consecutive stages with a delay of 2 ns. Two pipelined implementation of the processor are contemplated:
I).a naive pipeline implementation (NP) with 5 stages and
II). an efficient pipeline (EP) where the OF stage is divided into stages OF1 and OF2 with execution times of 12 ns and 8 ns respectively.
The speedup (correct to two decimal places) achieved by EP over NP in executing 20 independent instructions with no hazards is _____

74. Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to 2 gigahertz. Assume that there are no stalls in the pipeline. The speed up achieved in this pipelined processor is _____.

75. Consider a 6-stage instruction pipeline, where all stages are perfectly balanced. Assume that there is no cycle-time overhead of pipelining. When an application is executing on this 6-stage pipeline, the speedup achieved with respect to non-pipelined execution if 25% of the instructions incur 2 pipeline stall cycles is _____.

76. An instruction pipeline has five stages, namely, instruction fetch (IF), instruction decode and register fetch (ID/RF), instruction execution (EX), memory access (MEM), and register write back (WB) with stage latencies 1 ns, 2.2 ns, 2 ns, 1 ns, and 0.75 ns, respectively (ns stands for nanoseconds). To gain in terms of frequency, the designers have decided to split the ID/RF stage into three stages (ID, RF1, RF2) each of latency 2.2/3 ns. Also, the EX stage is split into two stages (EX1, EX2) each of latency 1 ns. The new design has a total of eight pipeline stages.

A program has 20% branch instructions which execute in the EX stage and produce the next instruction pointer at the end of the EX stage in the old design and at the end of the EX2 stage in the new design. The IF stage stalls after fetching a branch instruction until the next instruction pointer is computed. All instructions other than the branch instruction have an average CPI of one in both the designs. The execution times of this program on the old and the new design are P and Q nanoseconds, respectively. The value of P/Q is _____.

77. The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Write back (WB). The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards. The number of clock cycles required for completion of execution of the sequence of instructions is _____

78. Consider the following processors (ns stands for nanoseconds). Assume that the pipeline registers have zero latency.
P1: Four-stage pipeline with stage latencies 1 ns, 2 ns, 2 ns, 1 ns.
P2: Four-stage pipeline with stage latencies 1 ns, 1.5 ns, 1.5 ns, 1.5 ns.
P3: Five-stage pipeline with stage latencies 0.5 ns, 1 ns, 1 ns, 0.6 ns, 1 ns.
P4: Five-stage pipeline with stage latencies 0.5 ns, 0.5 ns, 1 ns, 1 ns, 1.1 ns.
Which processor has the highest peak clock frequency?
(A) P1
(B) P2
(C) P3
(D) P4

79. Consider a 4 stage pipeline processor. The number of cycle needed by the four instructions I1,I2,I3,I4 in stages S1, S2, S3, S4 is shown below:

	S1	S2	S3	S4
I1	2	1	1	1
I2	1	3	2	2
I3	2	1	1	3
I4	1	2	2	2

What is the number of cycles needed to execute the following loop?
for (i=1 to 2) {I1; I2; I3; I4 ;}
(A) 16 (B) 23 (C) 28 (D) 30

80. Consider the sequence of machine instruction given below:
MUL R5, R0, R1
DIV R6, R2, R3
ADD R7, R5, R6
SUB R8, R7, R4

In the above sequence, R0 to R8 are general purpose registers. In the instruction shown, the first register stores the result of the operation performed on the second and the third registers. This sequence of instructions is to be executed in a pipelined instruction processor with the following 4 stages: (1) instruction Fetch and Decode (IF), (2) Operand Fetch (OF), (3) Perform Operation (PO) and (4) Write back the result (WB).
The IF, OF and WB stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD or SUB instruction, 3 clock cycle for MUL instruction and 5 clock cycles for DIV instruction. The pipelined processor uses operand forwarding from the PO stage to the OF stage. The number of clock cycle taken for the execution of the above sequence of instructions is _____

UNIT -4
IO- ORGANIZATION

81. Consider a 10 KBPS device transferring the data byte by byte, two designers were suggested
    (i) Programmed control transfer
    (ii) Interrupt driven transfer
    The interrupt overhead is 4 μs per byte. What is the performance gain of the interrupt transfer over program controlled transfer?

82. If 1MBPS is operated in cycle stealing mode such that whenever 64 bit word available it will be transferred into the memory in 1micro seconds. What is the percentage of the time CPU gets blocked due to DMA transfer?

83. A processor is using 600 MHz clock ,it consumes 1600 clocks for initialization, 800 clocks for termination. A device of 100 MBPS is connected; it is required to transfer a file of 400 KB. What is the percentage of time processor contribution in this data transfer?

84. On a non-pipelined sequential processor, a program segment, which is the part of the interrupt service routine, is given to transfer 500 bytes from an I/O device to memory.
    Initialize the address register
    Initialize the count to 500
    LOOP: Load a byte from device
    Store in memory at address given by address register
    Increment the address register
    Decrement the count
    If count! = 0 go to LOOP
    Assume that each statement in this program is equivalent to a machine instruction which takes one clock cycle to execute if it is a non-load/store instruction. The load-store instructions take two clock cycles to execute.
    The designer of the system also has an alternate approach of using the DMA controller to implement the same transfer. The DMA controller requires 20 clock cycles for initialization and other overheads. Each DMA transfer cycle takes two clock cycles to transfer one byte of data from the device to the memory.
    What is the approximate speed up when the DMA controller based design is used in a place of the interrupt driven program based input-output?
    (A) 3.4 (B) 4.4 (C) 5.1 (D) 6.7

85. A hard disk with a transfer rate of 10 Mbytes/second is constantly transferring data to memory using DMA. The processor runs at 600 MHz, and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation?
    (A) 5.0% (B) 1.0% (C) 0.5% (D) 0.1%

86. The Size of the data count register of a DMA controller is 16 bits. The processor needs to transfer a file of 29,154 kilobytes from disk to main memory. The memory is byte addressable. The minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory is _____ .

Secondary Memory

87. Consider a disk which is having 10 equidistance tracks the inner track capacity is 10 MB and its diameter is 1 cm, the adder track diameter is 10 cm, what is the capacity of the disk, if it is moving with constant linear velocity

88. Consider a disk which is having 256 tracks, 512 sectors, 4096 B/sector, the disk is moving with 3000 RPM. The seek time is 10ms
(i) What is the capacity of the disk?
(ii) How many bits are required to address the disk?
(iii) How much time have it taken to read 64 KB file which was placed from 64th sector of outer track, the current position Read/Write head is 4th sector inner track.
(iv) The cycle stealing mode of DMA used to that whenever 32 B word is available, it will be placed in 8 ns time What is the percentage time process on is blocked due to DMA.

89. Consider a disk drive with the following specifications:
16 surfaces, 512 tracks/surface, 512 sectors/track, 1 KB/sector, rotation speed 3000 rpm. The disk is operated in cycle stealing mode whereby whenever one byte word is ready it is send to memory similarly, for writing the disk interface reads a 4 byte word from the memory in each DMA cycle .Memory cycle time is 40 nsec. The maximum percentage of time that the CPU gets blocked during DMA operation is:
(A) 10 (B) 25 (C) 40 (D) 50

90. Consider a disk pack with 16 surfaces, 128 tracks per surface and 256 sectors per track, 512 bytes of data are stored in a bit serial manner in a sector. The capacity of the disk pack and number of bits required to specify a particular sector in the disk are respectively
(A) 256 Mbyte, 19 bits
(B) 256 Mbyte, 28 bits
(C) 512 Mbyte, 20 bits
(D) 64 Gbyte, 28 bits

91. If the overhead for formatting a disk is 96 bytes for 4000 bytes sector,
(a). Compute the unformatted capacity of the disk for the following parameters:
Number of surfaces: 8
Outer diameter of the disk: 12 cm
Inner diameter of the disk: 4 cm
Number of sectors/track: 20
Inner track space: 0.1mm
(b). If the disk in (a) is rotating at 3600 rpm, determine the effective data transfer rate which is defined as the number of bytes transferred per second between disk and memory

92. Consider a disk system which is constructed with each track is having 63 sectors, the system is organized into 1000 cylinders, sector address is given cylinder wise, logical address contains a triple $< c, h, s >$ c = Cylinder number, h = Surface number s = sector number .Assume that number of surfaces in this organization is 20
The sector 0 is addressed with $< 0,0,0 >$
The sector 1 is addressed with $< 0,0,1 >$
(i) Compute the sector address for a triple $< 400,16,43 >$
(ii) Which will be the triple address for 1039th sector?

93. A disk is maintaining 100 libraries which are randomly placed, for each library it requires 1 disk is having 6000 rpm, seek time is 1.2 times of average rotational latency. The data transfer time of library is negligible. How much time is required to load all 100 libraries to memory?

94. Consider a disk system contain 4096 cylinders (0-4095), 64 surfaces (0-63), 64 sectors per track (0-63). Each sector can held 512 bytes.
(i) What will be the sector number, if it is having logical address <1023, 56, 48>
(ii) What will be the cylinder number for a sector whose linear address is 5554440?
(iii) Capacity of the disk system
(iv) How many bits are require to address this disk system
(v) 1 GB file is stored from <100, 10, 10>. It occupies contiguous sector onwards. What will be the cylinder number of last sector?

95. How long does it take to load a 64K program from a disk whose average seek time is 30 msec, whose rotation time is 20msec, and whose tracks hold 32K
A). for a 2K page size?
B). For a 4 K page size?
The pages are spread randomly around the disk.

96. Consider a disk pack with a seek time of 4 milliseconds and rotational speed of 10000 rotations per minute (RPM). It has 600 sectors per track and each sector can store 512 bytes of data. Consider a file stored in the disk. The file contains 2000 sectors. Assume that every sector access necessitates a seek, and the average rotational latency for accessing each sector is half of the time for one complete rotation. The total time (in milliseconds) needed to read the entire file is _____.

97. Consider a typical disk that rotates at 15000 rotations per minute (RPM) and has a transfer rate of 50×10^6 bytes/sec. If the average seeks time of the disk is twice the average rotational delay and the controller's transfer time is 10 times the disk transfer time, the average time (in milliseconds) to read or write a 512-byte sector of the disk is _____.

98. Consider a hard disk with 16 recording surfaces (0-15) having 16384 cylinders (0-16383) and each cylinder contains 64 sectors (0-63). Data storage capacity in each sector is 512 bytes. Data are organized cylinder – wise and the addressing format is <cylinder no., surface no., sector no>. A file of size 42797 KB is stored in the disk and the starting disk location of the file is < 1200, 9, 40>. What is the cylinder number of the last sector of the file, if it is stored in a contiguous manner?
(A) 1281
(B) 1282
(C) 1283
(D) 1284

Registers Allocation

The following code segment is executed on a processor which allows only register operands in its instructions. Each instruction can have atmost two source operands and one destination operand. Assume that all variables are dead after this code segment.

```
c = a + b;
d = c * a;
e = c + a;
x = c * c;
if (x > a) {
 y = a * a;
}
else {
 d = d * d;
 e = e * e;
}
```

99. Suppose the instruction set architecture of the processor has only two registers. The only allowed compiler optimization is code motion, which moves statements from one place to another while preserving correctness. What is the minimum number of spills to memory in the compiled code?
(A) 0
(B) 1
(C) 2
(D) 3

100. What is the minimum number of registers needed in the instruction set architecture of the processor to compile this code segment without any spill to memory? Do not apply any optimization other than optimizing register allocation.
(A) 3
(B) 4
(C) 5
(D) 6