VLSI Testing (CMPE 418/646)
University of Maryland Baltimore County

Verilog Netlist Description

This document gives a brief explanation on the structure of a circuit netlist in Verilog. What follows shows how we define the circuit given in Fig. 1 using Verilog HDL and the gates in the given library (GSCLib). You can find the GSCLib in the "benchmarks" directory given in Hw5.

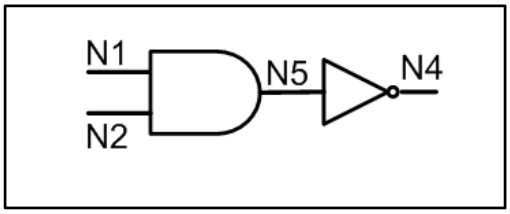

Figure 1. the schematic of a sample circuit (circuit1)

Input File Format (Verilog Netlist)

1. The file begins with the "module" keyword followed by the module name and list of primary inputs and primary outputs within parenthesis and separated using ','.
   Example: module circuit1 (N1,N2,N4);

2. The primary inputs of a circuit are identified using the keyword "input" followed by list of inputs separated using ','.
   Examle: input N1,N2;

3. The primary outputs are designated with keyword "output" and the list of outputs follows.
   Example: output N4;

4. The wires in the circuit are identified using the "wire" keyword.
   Example: wire N5;

5. The architecture is then described using the gate types mentioned below.

Gate Types

You can use any gate from your library. In this homework we only consider the following gates defined in your library (GSCLib.v):

- AND2X1
- OR2X1
- NAND2X1
- NOR2X1
- XOR2X1
- INVX1
- BUFX1

6. A Gate definition includes 3 items separated by one or more spaces.

- 2-Input, 1-Output Gate:

Gate_Type Gate_name (.Y(Output_of_Gate),.A(Input_1),.B(Input_2));
Example: AND2X1 AND_1 (.Y(N5),.A(N1),.B(N2));

- 1-Input, 1-Output Gate:

Gate_Type Gate_name (.Y(Output_of_Gate),.A(Input_1));
Example: INVX1 INV_1 (.Y(N4),.A(N5));

7. All lines end with semicolon.

8. Comments are to be ignored when the file is being processed
//single line comment
/* Multi line
Comment*/

9. The definition of the module ends with the keyword "endmodule".

Figure 2 shows the Verilog netlist of the circuit shown in Figure 1.

```
module circuit1 (N1,N2,N4);
input N1,N2;
output N4;
wire N5;

//Gates in the module
AND2X1 AND_1 (.Y(N5),.A(N1),.B(N2));
INVX1 INV_1 (.Y(N4),.A(N5));
endmodule
```

Figure2. Verilog netlist of the circuit shown in Figure 1