VLSI Design Verification and Testing (CMPE 418, CMPE/ENEE 646)

University of Maryland Baltimore County

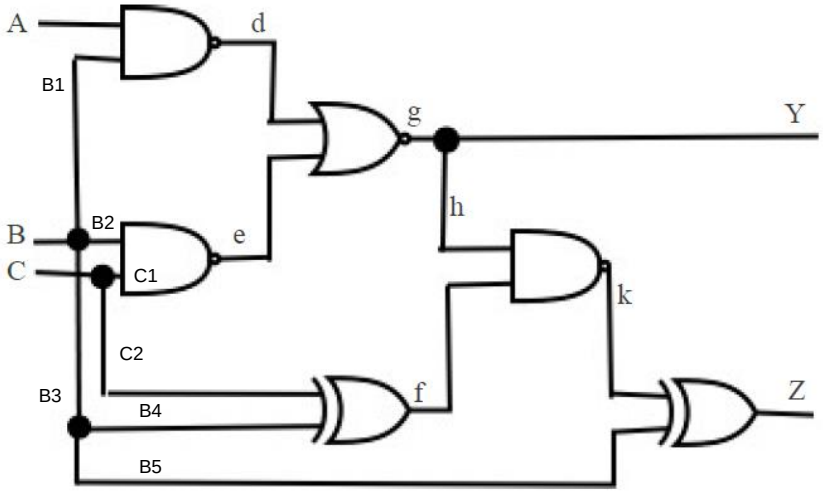
Fall 2024

HW5b: Test generation and Fault Simulation

Due: Nov. 7, 2024

In this lab you are to check how Tetramax performs fault simulation and test generation. Please find the related files and tutorials in Blackboard. For this lab please take the following steps.

1. Without using the tool, generate test patterns that detect all stuck at faults in the following circuit (the is the same circuit you had in Hw3). Please target **each fault separately** and generate **all** test patterns for each fault. Then using the generated patterns, find the **minimal set** of patterns that can detect all faults.



2. Follow the document that discusses how you can describe a circuit in the gate level in Verilog ("Verilog-Netlist Description" file given to you in the folder called "Tutorial"). Then write the Verilog netlist of the above circuit. Use Tetramax to perform test-generation for all faults in this circuit. Check the generated output files and compare it with your answer in part1 and discuss your observations in the report. Look up the fault classes you come across in the tmax user **guide** and describe your results based on them too.

3. Use Tetramax to perform test-generation and fault-simulation for the circuit my-circuit.v. Please report the following:

   For test generation problem:

- Total number of faults
- The number of test patterns generated to detect all stuck-at faults
- Fault-classes statistics (# of detectable faults, Undetectable faults, etc)
- Test coverage (is the number of detected faults over the number of detectable faults)

For fault simulation problem use the faults included in the fault_list_1 file and report the following:

- Total number of faults
- Fault-classes statistics (# of detectable faults, Undetectable faults, etc)
- Fault coverage
- Test coverage

4. Repeat the fault simulation problem and this time target all stuck-at faults (not only the faults included in the fault_list_1). Then report:

- Total number of faults
- Fault-classes statistics (# of detectable faults, Undetectable faults, etc)
- Fault coverage
- Test coverage

Deliverables:

-Your answer for step 1.
- The verilog file for step 2 (submit the *.v file)
- All output files generated by Tetramax for steps 2-4.
- A PDF file that includes your report for all steps.