VLSI Design Verification and Testing (CMPE 418/646)
University of Maryland Baltimore County
Tutorial: Test generation and Fault Simulation

In this lab, you will be doing test pattern generation and fault simulation. You are provided with a verilog netlist, library files and scripts that will help you perform test pattern generation and fault simulation.

The "Tutorial-Lab" folder contains two sub folders

1. Test_Generation
2. Fault_Simulation

The Test_Generation folder contains files that are used to generate test patterns. The files are

1. Test_Generation.tcl – A tcl script that automates the test pattern generation process.
2. my-circuit.v – Verilog netlist for which test patterns are to be generated
3. mylib.v – The library file

The Fault_Simulation folder contains

1. Fault_Simulation.tcl – A tcl script automating the fault simulation procedure
2. my-circuit.v – Verilog netlist for which test patterns are to be generated
3. mylib.v – The library file
4. Fault_Sim.pattern – The patterns for which fault simulation are to be done are available here.
5. faults_list_1 – List of uncollapsed faults that is read during fault simulation.

To run tcl script in shell mode, use the following shell command

$tmax –shell –tcl Test_Generation.tcl

$tmax –shell –tcl Fault_Simulation.tcl

A. Test Pattern Generation using TetraMAX

1. If necessary, preprocess your netlist to meet the requirements of TetraMAX.

2. Read in the netlist.

3. Read in the library models.

4. Build the ATPG design model.

5. Perform test DRC and make any necessary corrections.

6. Prepare the design for ATPG, set up the fault list, analyze buses for contention, and set the ATPG options.

7. Run automatic test pattern generation.

8. Review the test coverage and rerun ATPG if necessary.

9. Rerun ATPG.

10. Save the test patterns and fault list.

Running Test Pattern Generation

1. Create a working folder and copy all the files that are available in Test_Generation to the working folder.

2. Open Tetramax and click on the "Cmd" button

3. Select Test_Generation.tcl in the window that pops up

4. The following files are generated

- 1. ATPG_pattern.pattern – Contains the test patterns for faults mentioned in the Test_Generation.tcl file
- 2. faults_list_1 – List of uncollapsed faults
- 3. faults_left – The list of faults that are not detected.

Command Description - Test_Generation.tcl

The netlist and library files are read. The model is built. The clock signal and scan chains are defined (for sequential circuits). The design rule is checked. The stuck at fault model is then selected and list of faults are added. The ATPG is run to generate the test patterns.

The test patterns generated are written in a file called ATPG_pattern.pattern in the STIL format. The list of uncollapsed faults are available in faults_list_1 file. The file faults_left contains the undetected faults.

read_netlist ./mylib.v

read_netlist ./my-circuit.v # (Read in the netlist – The netlist and library models are read in through the following commands)

run_build_model c6288 **#(Build the ATPG Model)**

run_drc

set_faults -model stuck

remove_faults -all

add_faults -all

The Preparation for ATPG is done using these commands. The fault model is set to stuck and all faults are added to the fault list.

run_atpg -ndetects 1

ATPG is run, one pattern is generated per fault.

write_patterns ./ATPG_pattern.pattern -exclude setup -format stil -replace

write_faults faults_list_1 -uncollapsed -all -replace

write_faults faults_left -class ND -replace

The test patterns generated are written in a file called ATPG_pattern.pattern in the STIL format. The list of uncollapsed faults are available in faults_list_1 file. The file faults_left contains the faults that are not detected.

B. Fault Simulation using TetraMAX

1. Prepare the functional test patterns for fault simulation.
2. Prepare the design for fault simulation.
3. Read in the external functional patterns.
4. Perform a good machine simulation.
5. Perform fault simulation to fault-grade the functional test patterns.
6. Write the fault list.
7. Save the fault list if you intend to perform ATPG later.

Running Fault Simulation

1. Create a working folder and copy all the files that are available in Fault_Simulation to the working folder.

2. Open Tetramax and click on the "Cmd" button

3. Select Fault_Simulation.tcl in the window that pops up

4. The following files are generated

    - fault.left – The faults that are not testable by the patterns given

Command Description – Fault_Simulation.tcl

set_patterns -external ./Fault_Sim.pattern

Use this command to select the source of patterns to use for simulation, fault simulation, or test generation. The ATPG patterns are read from the Fault_Sim file.

set_simulation -measure sim

This command is used to set the simulation-related control parameters. Specifies whether the faulty machine simulation performed by the run_fault_simulation command uses the expected data from the current patterns or the expected data as simulated by TetraMAX for the good machine. This option has no effect on the results of good machine simulation. The default behavior is to use the data supplied in the functional patterns during the faulty machine simulation. Selecting -measure sim causes the TetraMAX good machine simulated values to be used instead of the values in the patterns.

run_simulation -override_differences

Use this command to perform simulation of the current pattern source determined by the set_patterns command and report any differences between simulated and expected values. This

simulation can be performed in the presence of a selected fault and will report all failures that result from the fault.

run_fault_sim

You use this command to perform fault simulation using the current fault list and the current

selection of the pattern source.