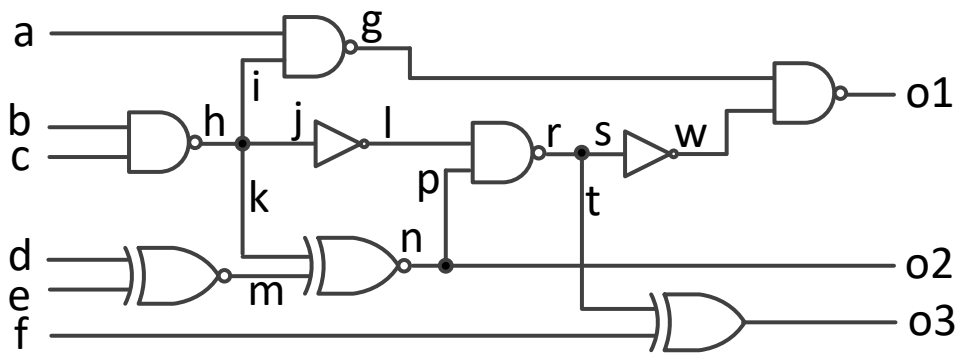
VLSI Testing (CMPE 418/646)
University of Maryland Baltimore County
Fall 2024

EQUIVALENT FAULT COLLAPSING
Due: Nov. 7, 2024

In this lab you are to check how Tetramax performs fault collapsing for a given circuit. Please take the following steps.

1. Follow the document that discusses how you can describe a circuit in the gate level in Verilog. Then write the Verilog netlist of the following circuit. This is the same circuit you had in Hw1.



   Use Synopsys-Tetramax test tool to extract the list of total faults as well as the list of faults after fault collapsing and compare these lists with your list in Hw1 and show the differences (if any).

2. Use Synopsys-Tetramax test tool to extract the list of total faults for c1908_new.v and c2670_new.v circuits before and after fault collapsing and find the collapse-ratio for these circuits (The circuits' netlist have been posted in blackboard). In your report, show the number of faults before and after collapsing and the collapse ratio in each case. Also, please include the list of faults before/after fault collapsing for each circuit in your report.

   Deliverables:

   - The verilog file for step 1 (submit the *.v file)
   - A PDF file that includes your report for part2 and part 3.