SHF: Medium: A Pathway for Combining Formal, Static, and Dynamic Analysis of Real-World Embedded Systems

1 Overview and Objectives

1.1 Problem Statement

The core problem we aim to address in this proposal is that *use of formal modeling, advanced static analysis, and advanced dynamic analysis tools in C and C++* for verification and validation, especially on critical, timing-dependent, embedded and cyber-physical systems, is prohibitively difficult and lacks sufficient synergy for effective application in real-world projects. This limitation applies even to systems built in an academic research context, unless the context is specifically that of using such systems (that is, unless the research is primarily *about* methods for verifying and testing systems, rather than work on an embdeded system for its own sake). Furthermore, even when use of these techniques to ensure correctness, reliability, or security *is* a focus of the project, such use is almost always limited to one type of effort—model checking, theorem proving, or dynamic analysis (e.g., automated test case generation). A major cause for this difficulty is the *lack of synergy* between these related efforts, the failure of effort in one context to transfer to another context. In short:

- Learning to use a formal modeling language and tool, such as UPPAAL [12], PRISM [68], or SPIN [63], provides help in discovering defects in a high-level, abstract formulation of a model or protocol, but seldom helps with implementation-level problems not directly modeled in the formalism.
- Many static analysis tools are primarily "bug detectors" (e.g, Coverity or CodeSonar), whose output is essentially limited to a list of possible problems. These tools, however, seldom provide any means for producing tests that can help distinguish false positives from real problems with the code.
- More powerful static analysis tools, such as FRAMA-C [65], provide proofs of correctness for limited aspects of a system, and a rich specification and annotation language. There is no connection between this annotation and either formal modeling or test generation using anything other than a concolic tool that is limited in functionality and scalability.
- There are a large variety of automated test generation tools; however, again, effort spent in learning one of these tools only partially applies to learning a different tool. Furthermore, many of the most powerful such tools (e.g., AFL [104]) are specialized to the problem of finding memory safety vulnerabilities, and provide no support for the kind of testing needed for other types of faults in e.g., communication protocols used in distributed embedded systems. Finally, none of these tools significantly leverage specification and verification effort from formal modeling or advanced static analysis.

Consider the case of an engineer working on a custom, low-energy consumption, communication protocol for use in a distributed system consisting of low-power sensors and actuators. If the engineer builds a formal model of the protocol, she will discover that this extensive effort provides no help, other than an improved concept of the system, in proving the correctness of the actual implementation, even if the property to be proved exists in the model. If the engineer begins instead by building an automated test generation harness she again discovers that despite having spent considerable time expressing pre-conditions and post-conditions for various functions in the implementation, to guide test generation, the work must be duplicated when she decides to try to formally prove the correctness of core functionality. Had she begun with the proofs, again, logically related (or even equivalent) information would have to be re-expressed, in a different language, to perform test generation. Not only must our engineer learn three tools, but effort spent in using one tool almost never carries over to another approach. In almost all cases, there is simply not enough time or energy available to make use of the full spectrum of available technology. In practice, *no advanced correctness technology may be used at all.* After all, it is hard to predict which technology will have the greatest payoff, or even work at all, so perhaps it is best to just put more effort into manual testing.

1.2 Proposed Solution

While allowing efforts from any form of formal or automated verification or validation attempt to maximally carry over to other forms (i.e., formal models to code annotations for static analysis, code annotations to test harnesses, test harnesses to code annotations, test harnesses to formal models, formal models to test harnesses, and code annotations to formal models) is the ideal goal, simply making it possible to follow *one* critical path to combine methods is feasible given current technologies in the sub-domains (formal modeling, static analysis, and dynamic analysis) and a set of specific advances in bridging the gap between the technologies. This project proposes to make it possible to introduce specifications into implementation code that can be directly checked using sophisticated automated test generation strategies, including symbolic execution, advanced fuzzing, explicit-state model checking, and SAT/SMT-based bounded model checking. Furthermore, these specifications can be directly exported to form the basis for formal models using, e.g., timed automata, or imported from a timed automata representation. To further improve the value of our approach, we focus on integrating static and dynamic analysis tools that are, themselves, frameworks/front-ends allowing application of multiple approaches. This project is specifically focused on communication protocol implementations in embedded systems where timing is critical to the modeling of behavior, but we expect that our solution will generalize to other critical C and C++ systems development scenarios. Note that target the common, hard, case where our approach will be applied to systems with partial or complete implementations: typical legacy embedded C code. We expect developers to learn new tools, but not new programming paradigms or languages. The contribution to embedded systems design therefore is not a radical reworking of development methods, which, like many formal methods efforts in the past, is unlikely to achieve widespread adoption, but the introduction of, essentially, *an advanced form of unit testing, with more powerful methods for specifying "testing and verification problems" and more powerful, low-effort ways to try to solve those problems.* The end-result for embedded systems engineers will be an approach to development that works with legacy code, and does not require a fundamental shift in approach, but will *support* early adoption of formal modeling as, e.g., timed automata, if present, and, critically, will allow engineers to express the correctness properties in a full-featured way directly in code, while enabling use of a variety of methods to check those properties. This will modify development, in that design-for-testability and design-for-verifiability will become second nature. Just as the introduction of the possibility to express *and check* strong typing constraints changed Python development practices for high-value projects, the introduction of the possibility to express *and check* correctness properties will change embedded system development.

1.2.1 PI Qualifications

PI Groce has a long history with formal methods, including involvement in design and development of well-known model checkers, and application of model checkers at NASA/JPL on flight software for the Mars rovers. More recently, he has primarily focused on developing algorithms and tools for automated software testing; he is a core member of the DeepState [43, 44, 97] and TSTL [62] design and development teams. He brings to this project practical experience using verification and testing tools on real systems, and engineering such tools to be usable by engineers who are domain experts, not verification or testing experts.

Co-PI Nghiem has an extensive background in control and autonomous systems, and application of formal methods in control systems. He has long experience working with timed automata and the UPPAAL tool family. He developed, and was granted a U.S. patent for, methods for testing and verifying temporal logic specifications of hybrid systems—systems with both continuous and discrete behaviors. He brings to this project advanced knowledge of real-time embedded systems and practical experience applying verification methods and tools to them. He will also apply our methods and approaches to a multi-agent robotics system.

Co-PI Flikkema's current work includes research in energy-efficient embedded systems and networks, inference of the embedding environment, wireless sensor/actuator networks for monitoring and control of environmental and ecological systems, and cybersecurity with focus on IoT. Like Co-PI Nghiem, he ensures that developed approaches will be suitable for engineers whose primary focus is *building working systems*.

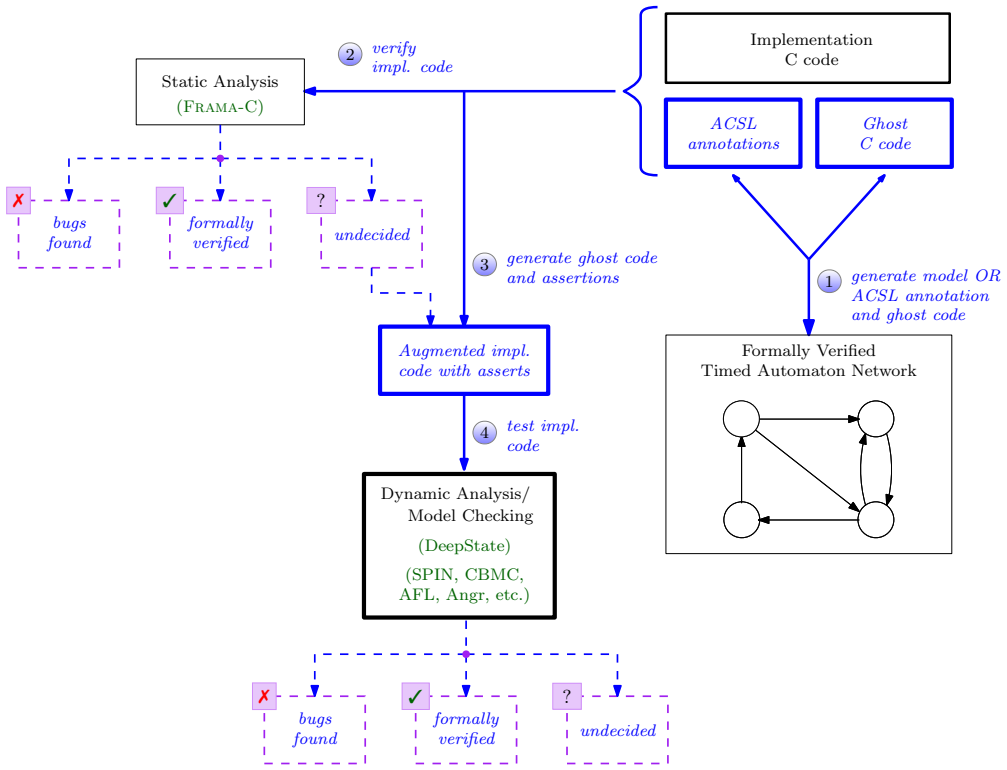

Figure 1: Overview of the proposed research.

1.3 Intellectual Merit

The aim of this proposal is to (1) identify a set of principles for the analysis (formal, static, and dynamic) of communication protocols and their implementations in embedded systems; (2) implement these theoretical principles in tools usable by engineers developing such systems; and (3) use these tools in two real applications. In the first case study, we will formally, statically, and dynamically analyze networks of wireless sensor/actuator nodes deployed in the Southwest Experimental Garden Array (SEGA) [102, 39], a distributed facility for examining climatic, genetic, and environmental factors in plant ecology. The second case study will use the tools to formally verify and dynamically test the distributed coordination code of multiple autonomous ground and aerial robots in a lab setting.

Figure 1 shows the overall concept. The core open research problems addressed are represented by two sets of arrows. First, an engineering design, expressed as C code, is provided, and annotated with correctness properties and information about the expected environment (constraints on sensor values, etc.). From this, code to apply advanced static analysis or generation of timed automata (TA) models, can be automatically generated. Our goal is to certify whether the C code truly implements the correctness properties in question:

1. First, the TA model can be used to check high-level properties of the design, ignoring many low-level implementation details. If core timing properties are wrong, finding bugs in the implementation is best left until the basic design is correct. However, this step may be skipped.
2. The implementation code with the ACSL annotations and ghost code is checked by a static analysis tool, such Frama-C. There are three possible outcomes: **verified:** the implementation can be formally verified, which means that it meets the design specifications that can be checked statically; **bugs found:** non-spurious bugs are found in the implementation, showing that it can violate the specification, and the bugs must be fixed; or **undecided:** the static analysis tool is unable to prove or disprove correctness of the implementation, which will often be the case.
3. Finally, the focus of our efforts is a multi-pronged attempt to refute correctness (or increase our confidence

in it) via dynamic analysis—automated test generation—and implementation-level model checking. Ghost code, additional runtime assertions, and needed test-harnesses are *automatically generated* from the annotated code.

4. The augmented implementation code is then analyzed using the DeepState [43] framework, which serves as a front-end to highly scalable fuzzers, as well as to symbolic execution tools and explicit-state and SAT/SMT-based bounded model checkers that can detect more bugs at the cost of restricted applicability or scalability. Generated test cases may prove the system faulty, or they may leave us more confident the system is correct.

Our focus is on providing a unified specification method that can be applied to source code itself, and on the dynamic analysis and explicit-state and SAT/SMT bounded model checking aspects of the approach. We believe these approaches are currently the most difficult to apply, and the most likely to dramatically improve the ability to detect bugs in complex embedded systems designs.

Principles: Assuming that a communication protocol can in theory be described as (probabilistic) timed automata [6], which satisfies temporal logic formulas [22], and implemented as a set of imperative programs that realize these timing constraints and other correctness conditions, we ask:

- Given a set of annotated programs, how can we best automatically find bugs in those programs (and, in some circumstances, for some properties, prove correctness), based on the annotated specification?
- Can we generate a skelton of the timed automata model from annotated programs, in order to facilitate analysis of the design, in order to increase adoption of design-level analysis by traditional embedded systems developers?

Note that these problems differ considerably from the more studied, but more limited, synthesis problem. We are not assuming that system development will involve first producing a formal model, then using that model to automatically generate an implementation; rather, we consider the typical real-world scenario, where modeling is a separate activity, either undertaken after implementation due to concerns about reliability, or an activity during design that only indirectly informs the implementation. That is, the more studied problem is producing a runtime semantics for a model; we address the problem of reconciling a runtime semantics with a model semantics, without unrealistic burden on engineers. We begin with the implementation side, because while realtively few embedded systems engineers currently use formal models, all must implement their systems. Furthermore, to the extent that developers do more rigorous testing and analysis of their systems, they primarily use unit tests, simple fuzzing, and static analysis. Any method that aims to increase the adoption of formal methods and more powerful automated test generation approaches, including implementation-level model checking and symbolic execution, is likely to be successful to the extent that it enters the design and implementation process via this existing "bridge to engineers and developers."

Tools: We will focus on C code, using DeepState [43] as a front-end for dynamic and implementation-level model checking approaches, and UPPAAL [12] and PRISM [68] for the analysis of protocols; FRAMA-C will provide a powerful static analysis framework, and we well adopt the ACSL language developed for FRAMA-C as a basis for our specification language. The primary open research questions here are numerous, and include: (1) how to extend existing specification languages to support timing and uncertainty; (2) how to assign the same meaning to a specification construct in various contexts, ranging from fuzzing to symbolic execution to explict-state model checking to bounded model checking in the "dynamic" DeepState world, and including a static context for FRAMA-C and a modeling conext for timed automata. (3) how to handle intra-program parallelism; (4) how to effectively translate a failed proof effort in FRAMA-C into a representation of a testing problem (to find counterexamples refuting that proof could be possible) in a dynamic setting; and (5) how to ensure that the methods are sufficiently automatic and behave in ways engineers (not formal modeling, static, or dynamic analysis experts) will expect.

Our focus will be on *practical* solutions, guided by the embedded domain experts, rather than on purely theoretical approaches that do not scale to real systems. Practical solutions here require fundamental contributions to system and specification design and semantics and static and dynamic analysis methods.

2 Background and Preliminary Research

2.1 Static Analysis and Deductive Verification with FRAMA-C

While the correctness of an implementation with respect to a formal functional specification provides a very strong form of guarantee, it can be very costly to achieve. Currently it is mostly reserved to domains where it is required by regulations or offers a competitive advantage. In practice, it is very useful to rely on a combination of formal methods to achieve an appropriate degree of guarantee: automatic static analysis to ensure the absence of runtime errors, deductive verification to prove functional correctness, and runtime verification for parts of code that cannot be (or are not yet) proved using deductive verification, or parts of code that contain *warnings* from static analysis requiring confirmation.

This project will use FRAMA-C (`https://frama-c.com`) [65]. It is a widely-used source code analysis platform that aims at conducting verification of industrial-size programs written in ISO C99 source code. FRAMA-C fully supports combinations of different approaches, by providing its users with a collection of *plugins* for static and dynamic analyses of safety- and security-critical software. Moreover, collaborative verification across cooperating plugins is enabled by their integration on top of a shared kernel, and their compliance to a common specification language: ACSL [10]. ACSL, for ANSI/ISO C Specification Language, is based on the notion of contract as in JML. ACSL allows users to specify functional properties of programs through pre/post-condition, and provides different ways to define predicates and logic functions. Many built-in predicates and logic functions are provided, to handle, for example, pointer validity or separation. FRAMA-C is very appropriate for the verification of typical legacy embedded C code. Its specification language is rich but easy to understand: ACSL is essentially a typed first-order logic that contains C expressions.

Value analysis is a program analysis technique that computes a set of possible values for every program variable at each program point. It is based on the *abstract interpretation* technique proposed by Cousot and Cousot in the 1970's [33]. Its main idea is to compute an abstract view of values of variables in the form of *abstract domains*. For example, a usual abstract view for a number value is an interval. Value analysis can be very useful to detect potential runtime errors or prove their absence. Typical examples include invalid pointers, invalid array indices, arithmetic overflows or division by zero. It can also help to prove other properties for which domain-based reasoning can be efficient. The EVA (Evolved Value Analysis) plugin is strongly integrated into the FRAMA-C ecosystem. It offers a basis for many other derived plugins (see [65]).

WP is a *deductive verification* plugin provided with FRAMA-C. It is based on a weakest precondition calculus. Given a C program annotated in ACSL, WP generates the corresponding proof obligations that can be discharged by SMT solvers or with interactive proof. A combination of automatic and interactive proofs often offers a good trade-off for a complete proof. Indeed, some properties can only be defined recursively, and in this case, SMT solvers often become inefficient, trying to unroll them. By using inductive or axiomatically defined functions, we can prevent this behavior but reasoning about them still requires induction, a task that SMT solvers are not good at. Thus, the last step is generally to state lemmas that can be directly instantiated by SMT solvers. This last step hinders the adoption of FRAMA-C as it requires the users to also master the COQ proof assistant or another interactive theorem prover. Our recent work showed how to avoid using an interactive theorem prover for this last step [17]. Function contracts in ACSL and loop annotations (verified using SMT solvers) are used instead of ACSL lemmas and COQ proof scripts. This is in line with the goal of this project: to provide automated tools usable by real-world developers.

FRAMA-C was initially designed as a static analysis platform, but it was later extended with plugins for dynamic analysis. One of these plugins is E-ACSL, a runtime verification tool. E-ACSL supports runtime assertion checking [32]. Assertions are very convenient for detecting errors and providing information about how a failure occurred. In FRAMA-C, E-ACSL is both the name of the assertion language and the name of a plugin that generates C code to check these assertions at runtime. E-ACSL is a subset of ACSL: the specifications written in this subset can therefore be used both by WP and E-ACSL. WP tries to prove the correctness of these assertions *statically* using automated provers, while the plugin E-ACSL is used to translate these assertions into executable C code. In this case the assertions are checked *dynamically*.

2.2 Dynamic Analysis with DeepState

While FRAMA-C provides powerful tools for static detection of program faults and generation of runtime checks for properties that cannot be discharged by formal proof or sound static analysis, it provides only limited, and difficult-to-scale, ability to generate program inputs to exercise runtime checks, limited to one tool, PathCrawler [100], that aims to produce a unit test for a single function, using concolic testing (dynamic symbolic execution [42]). In cases where this fails to scale, PathCrawler will fail. Furthermore, PathCrawler is tuned to the problem of testing a single function, not producing more complex scenario-based tests of a set of functions that must coordinate state changes. Finally, PathCrawler is not an open source, extensible system, may be costly to acquire and use, and is arguably impossible to extend.

The limitation of dynamic analysis tools to PathCrawler is a major weakness of FRAMA-C from the perspective of a user. Scalability of symbolic-execution-based test generation methods is extremely difficult to predict, and producing complete and exhaustive preconditions that allow a function to be tested entirely in isolation is often either too time-consuming or essentially impossible, because the actual environment is only represented by the set of states reachable using a set of coordinating functions or a library. These problems are pressing, for several reasons. First, full formal proof of correctness is, at present, impractical for most realistic systems. The actual work of fault detection and validation of software still relies, fundamentally, on effective testing. Moreover, modeling and even static approaches often must rest on a basis of numerous un-examined assumptions about the behavior of hardware systems and low-level system behavior (e.g., what operating system calls actually return). Only actual concrete inputs—tests—can be executed in a completely realistic environment, including real hardware. Only tests can satisfy regulatory requirements on code coverage such as those imposed on civilian avionics by DO-178B and its successors [87]. Furthermore, only testing can prove faults are not spurious, the result of imprecise abstraction or weak assumptions. In sum, dynamic analysis can detect otherwise invisible faults, and confirm the reality of statically detected faults.

Most developers do not know how to use symbolic execution tools; developers seldom even know how to use less challenging tools such as gray-box fuzzers, even relatively push-button ones such as AFL [104]. Even those developers whose primary focus is critical security infrastructure such as OpenSSL are often not users, much less expert users, of such tools. Furthermore, different tools find different faults, have different scalability limitations, and even have different show-stopping bugs that prevent them from being applied to specific testing problems. DeepState [43] addresses these problems. First, developers *do*, usually, know how to use unit testing frameworks, such as JUnit [40] or Google Test [2]. DeepState makes it possible to write parameterized unit tests [95] in a GoogleTest-like framework, and automatically produce tests using symbolic execution tools [90, 92, 89, 79], or fuzzers like AFL [104] or libFuzzer [88]. DeepState targets the same space as property-based testing tools such as QuickCheck [30], ScalaCheck [82], Hypothesis [76], and TSTL [48, 62], but with harnesses that look like C/C++ unit tests. DeepState is the first tool to provide a front-end that can make use of a growing variety of back-ends for test generation. Developers who write tests using DeepState can expect that DeepState will let them, without rewriting their tests, make use of new symbolic execution or fuzzing advances. The harness/test definition remains the same, but the method(s) used to generate tests may change over time. In contrast, most property-based tools only provide random testing, and symbolic execution based approaches such as Pex [94, 96] or KLEE [24], while similar on the surface in some ways, have a single back-end for test generation. DeepState's flexibility is evident: in the last few months, DeepState added support for the Eclipser [29], Angora [26], and Honggfuzz [3] fuzzers, as well as an ensemble [28] mode supporting the use of multiple fuzzers at once [25].

In effect, DeepState targets the same space (providing the technology and translation between different semantics necessary to use different verification/bug-detection technologies) as this proposal, but narrowed to the domain of generating test inputs. DeepState has already been used to test (and find bugs in) a user-mode ext3-like file system developed at the University of Toronto [93, 45]. DeepState is being considered as a basis for automatic testing for components in NASA's open source flight software framework FPrime [19, 80], and is a fully open source system [97], supported by Trail of Bits (a New York based security analysis company, which uses DeepState in security audits). DeepState is being considered as a future extension to the core

GoogleTest framework. Although only released in early 2018, DeepState is already one of the most popular property-based testing and fuzzing projects on GitHub.

3 Research Plan

3.1 From Timed Automata to FRAMA-C

It is notoriously difficult to design correct and secure communication protocols. One of the most famous examples is the Needham Schroeder Public Key protocol [81]. It took 18 years to discover a flaw in this protocol [75], and it was done using formal methods. Networks of timed automata are formalisms suitable for the formalization of protocols. They are the basis of model checkers such as UPPAAL [34] and PRISM [68] that have been used successfully in the verification of network protocols [106, 58, 64, 91]. These tools find issues with abstract formulations of protocols, but cannot help with implementation details that not modeled.

But the *implementation* details of a correct protocol also matter as the Heartbleed vulnerability in the OpenSSL implementation shows. In the case of Heartbleed, the problem was a C runtime error: an access to an invalid memory region, and it was due to an implicit assumption on the input of a function that was actually false. Combinations of static and dynamic analyses can detect such vulnerabilities [66] because they are not due to complex interactions related to the protocol.

The methodology we envision combines the use of model-checkers such as UPPAAL and PRISM for the verification of protocols, with frameworks for static and dynamic analysis of C programs, namely FRAMA-C and DeepState, for the verification of the *implementations* of protocols.

We consider FRAMA-C, and its specification language ACSL pivotal in this approach. The research challenge here is to translate networks of timed automata into ACSL annotations and C ghost code for enabling the verification of the C code implementing the protocol modeled by the timed automata:

1. The translation of networks of automata into annotations to be used within the FRAMA-C code analyzer.
   Previous work co-authored by co-PI Loulergue on the Contiki [37] lightweight operating system for the Internet of Things showed that various approaches can be applied to the verification of the same code. For checking the correctness of the linked list API of Contiki, it includes the use of ghost arrays [15]. Ghost code is a part of a program that is added for the purpose of specification. Such code should not interfere with regular code. Erasing it should make no observable difference in the program results. This approach made it possible to perform most proofs automatically using the FRAMA-C/WP tool, only a small number of auxiliary lemmas being proved interactively in the COQ proof assistant (later replaced by so-called lemma functions and loop annotations to avoid the use of COQ [17]). This work relied on an elegant segment-based reasoning over the companion array developed for the proof.
   This approach, however, is expressed in parts of the ACSL language that cannot be translated to executable C code, i.e. that do not belong to the E-ACSL subset. In a broader verification context, especially as long as the whole system is not yet formally verified, it is very useful to rely on runtime verification, in particular to test client modules that use the list module. A variant of the list module specification [74] that belongs to the executable subset E-ACSL of ACSL can also be transformed into executable C code. A newer approach [16] relies on logic lists: they are part of the ACSL standard library of inductively defined logical data structures. In the case of Contiki, a logic list provides a convenient high-level view of the linked list. The specifications of all functions is now proved faster and almost automatically. All these approaches are based on a predicate, or a combination of a predicate and a logic function, that relates the data structure (linked list), and a representation of it for specification purposes. Figure 2 shows the logic list representation (left) and array representation (right). In the former case, the logic list `ll` represents the linked list from root `bl` to cell `el`. In the latter case, the companion array `cArr` (`n` cells from index `index`) represents the linked list from `root` to cell `bound`.
   We expect several translations of networks of automata to be considered. Some may be easier to understand for C programmers not familiar with formal specifications (ghost code). Some may be more efficient for deductive verification (logical data structures). Some may be more suited for dynamic verification while still being amenable to deductive verification. The first approach will rely on ghost code. The automata

```
struct list { struct list *next; T data; };
typedef struct list ** list_t;

/*@ inductive linked{L}(struct list *bl,
                      struct list *el,
                      \list<struct list*> ll) {
  case linked_ll_nil{L}:
    \forall struct list *el; linked{L}(el, el, \Nil);
  case linked_ll_cons{L}:
    \forall struct list *bl, *el,
      \list<struct list*> tail; \separated(bl, el)
      ==> \valid(bl) ==> linked{L}(bl->next, el, tail)
      ==> separated_from_list(bl, tail)
      ==> linked{L}(bl, el, \Cons(bl, tail));
  } */
```

```
/*@ inductive linked_n{L}(struct list *root,
                        struct list *bound,
                        struct list **cArr,
                        integer index, integer n) {
    case linked_n_bound{L}:
      \forall struct list **cArr, *bound, integer
           index; 0 <= index <= MAX_SIZE
        ==> linked_n(bound, cArr, index, 0, bound);
    case linked_n_cons{L}:
      \forall struct list *root, **cArr, *bound,
          integer index, n; 0 < n ==> 0 <= index
        ==> 0 <= index + n <= MAX_SIZE
        ==>    \valid(root) ==> root == cArr[index]
        ==> linked_n(root->next, cArr, index + 1, n -
             1, bound)
        ==> linked_n(root, cArr, index, n, bound);
  } */
```

Figure 2: Linked List Representation in ACSL

will be translated as C code. The states of the model may contain variables: a C structure will be used to represent states. Transitions could be modeled as function calls. Such translations will be implemented as a FRAMA-C plugin, and will be automatic. However events and states of the automata will need to be associated with respectively specific execution events and memory states of the C programs. We expect to experiment manually with this mapping in case studies before enhancing the plugin to provide support for it. In particular this means the developer will have to write representation predicates such as those of Figure 2 mapping states of the automata model to more concrete and detailed states of the C programs.

2. Although deductive verification about *algorithmic complexity* is possible from source code [98, 84, 56], such a formal approach is not appropriate for this project, essentially because these approaches deal with complexity rather than execution time, and there is no precise enough translation from one to the other.
   Time constraints on the transitions will be translated into new ACSL annotations. Then we will rely on static analysis tools for worst-case execution time estimation. There are recent projects [77] that explore taking advantage of semantics information to improve WCET estimation, as well as preliminary work showing the benefits of such an approach [21].
   A C program with ACSL annotations very often provides a large variety of semantic information including intervals for variable values, and information about loops such as relations between the number of iterations and other variables. Exploiting this information will require us to be able to modify the WCET tool. This requirement excludes the best WCET estimator, aiT [38], a closed source commercial tool. Heptane [59] and `OTAWA` [9] are two actively developed open source projects with software architectures designed to ease extending the tools. Heptane is focused on cache analysis while `OTAWA` supports more processor architectures. For our case studies, `OTAWA` seems the best alternative for verifying if the bound obtained by WCET estimation on the code indeed satisfies the time constraints obtained for the timed automata.
3. The main part of the code where the specification of the automata will be used should be a kind of event loop. However this loop may be incomplete in the sense that it may not consider all the possible events, or even may not be structured as an event loop in the case most events are handled through interrupts. Although FRAMA-C does not directly handle concurrency, its CONC2SEQ [13] plugin (co-authored by co-PI Loulergue) allows for the analysis of parallel compositions of C programs through program transformation to sequential C programs [14]. The main part of the simulating program is a loop that handles control switch among the various threads. This loop can be used as the main event loop in a concurrency context.

3.2 From FRAMA-C to DeepState

As discussed above, a full workflow for verification of realistic systems requires a first-class, flexible, *dynamic* analysis component, such as DeepState [43]. The research challenge is to translate ACSL-annotated

code for use in FRAMA-C into a full-featured DeepState test harness:

1. The *specification* of correctness must be translated into an executable form. To some extent, the existence of the E-ACSL executable subset of ACSL, and libraries for runtime checking of properties satisfies this condition. DeepState can support any C/C++ executable method of checking for correctness. However, some executable specifications need to be modified to be efficiently handled when the DeepState back-end is a symbolic execution tool. DeepState's nature as a test generation tool means that it supports constructs, such as `Minimum`, `Maximum`, and `Pump`, not usually available in executable specifications. Tailoring E-ACSL usage for DeepState therefore requires a custom effort, including extending the semantics of executable specifications and optimizing the implementation for symbolic execution and fuzzing. Finally, because our domain critically involves timing, we need to implement DeepState handling (and E-ACSL representations for) deadlines, and specification of function-level deadlines including arbitrary, specified, "runtimes" for code that operates via simulation rather than real hardware (or in symbolic execution).
2. The *assumptions* that control which tests are considered valid must be translated in the same way; normally, E-ACSL simply translates these into further assertions (as pre-conditions to check at runtime), but in DeepState, we need to distinguish between `ASSUME` constructs where failure indicates an invalid test and `ASSERT` constructs where failure indicates a failing test.
3. The inputs to a function must be translated into code controlling the input values that DeepState provides, including ranges and types. When input types are simple, this process is straightforward; however, when functions take, e.g., arbitrarily sized arrays, linked lists, or other complex structures, this becomes a problem of constructing a test harness that (1) makes fuzzing and symbolic execution scalable but (2) uses large enough structures to expose subtle bugs. Moreover, because DeepState supports strategies for input generation, such as forking concrete states for values too complex for symbolic execution using the `Pump` construct, the translation must determine when such strategies are appropriate, and apply them.
4. In many cases, checking a single function may not be an effective way to detect faults; only a sequence of API calls can expose a problem in a system (e.g., that a function produce a state that causes another function to violate an invariant). ACSL annotations provide enough information for a fully-automated translation to a harness enabling dynamic analysis in the case of proving properties of a single function, but not for groups of functions. Moreover, even in cases where the violation of a specification can, in theory, be discovered without calling multiple functions, the state space may be too large to explore with a fuzzer or symbolic execution tool. In such cases, exploring only states produced by valid call sequences has two benefits: first, the space itself may be much smaller, and easier to explore, than the full set of possible input values. Second, errors in this part of the input space are more important. Even if a precondition is not sufficiently restrictive to guarantee correct behavior, if the "bad" inputs are never, in practice, generated by the functions that modify system state, the fault may not matter. In cases where constructing a sufficiently exact precondition is difficult for engineers, such "in-use" verification may be the only avenue to system assurance; proof is impossible without a restrictive enough precondition, and dynamic methods may scale very poorly to, e.g., a large unstructured byte buffer such as a hash table. We propose to let users annotate (in an extension of ACSL) sets of functions to be tested as an API-call-sequence group, extending recent work exploring this concept [18, 86]. E.g., annotating a set of file system functions (`mkdir`, `rmdir`, `readdir`, etc.) as such a group could allow the automatic generation of a DeepState harness that checks for cases where a sequence of valid function calls can violate a precondition or cause a fault despite preconditions being satisfied.

These goals require significant advances in two areas of dynamic analysis: first, a complete and principled approach to the problem of handling pre-conditions/assumption semantics, and second, an investigation of how to let fuzzers take advantage of the significant additional structure provided by property-based testing, including such assumptions. Consider the code in Figure 3. This defines two different tests of software that reads sensor values and incorporates them into a system state. The two tests check two different properties: `UpdateNeverSlow` ensures that updating the sensor is never too slow. It is checked, potentially, over *all* valid inputs, not just ones produced by the actual sensor reading code in `acquire_s1` and `acquire_s2`. The

```
void update_state(struct state_t *s, uint64_t bv) {
  ASSUME(valid_state(s));
  ASSUME(valid_bv(bv));
  ...
}
void process_both_sensor_readings(struct state_t *s) {
  ASSUME(valid_state(s));
  unit64_t s1_bv = acquire_s1();
  update_state(s, s1_bv);
  unit64_t s2_bv = acquire_s2();
  update_state(s, s2_bv);
}
void process_one_sensor_reading(struct state_t *s) {
  ASSUME(valid_state(s));
  unit64_t s1_bv = acquire_s1();
  update_state(s, s1_bv);
}
```

```
struct state_t *NewState() {
  return
    DeepState_Malloc(sizeof(struct state_t));
}
TEST(SensorReading, UpdateNeverSlow) {
  struct state_t *s = NewState();
  uint64_t bv = DeepState_UInt64();
  DeepState_Timeout(
    [&]{update_state(s, bv);},
    MAX_EXPECTED_UPDATE_TIME);
}
TEST(SensorReading, AvoidCrashes) {
  struct state_t *s = NewState();
  for(int i = 0; i < TEST_LENGTH; i++) {
    OneOf(
        [&]{process_both_sensor_readings(s);},
        [&]{process_one_sensor_reading(s);});
  }
}
```

Figure 3: Sensor reading code and DeepState test harness

second test, `AvoidCrashes` starts the system up in some valid state, and repeatedly either reads both sensors or only sensor one. There is no explicit property, only the expectation that the system will not crash; tests can be executed using LLVM sanitizers to check for integer overflow and other undefined behavior. Generating such harnesses automatically from ACSL specifications is a significant challenge, but our research agenda also includes solving problems that would appear even for manual harnesses. For example, what is the proper semantics of the `ASSUME` in `update_state`? It depends on the test. In `UpdateNeverSlow`, a fuzzer will often generate an input value that violates the (possibly complex) requirements on valid states and sensor readings. These invalid inputs should not be flagged as bugs (the default behavior of E-ACSL), but instead the test should be abandoned without indicating that it failed. However, in `AvoidCrashes`, since we are not directly generating state values, that is, `update_state` is not an *entry point* for the test, assumption violations should result in failed tests. We aim to synthesize code to make assumptions automatically take on the proper semantics during test execution (including symbolic execution using constraint solvers), without the user having to redefine the behavior.

This point about preconditions/`ASSUME` brings up a second point. Preconditions, when they have an `ASSUME` semantics, are fundamentally different than other branches in code. A fuzzer will attempt to explore the behavior of branches in `valid_state` and `valid_bv` just as it explores branches in `update_state` or `acquire`. However, it is often possible to enumerate a vast number of paths that differentiate only invalid inputs, and so produce very little real testing. A classic example is "testing" a file system by producing a huge variety of unmountable file system images, rather than actually executing any POSIX operations at all [49, 53]. DeepState knows which branches are pre-conditions, and so can help avoid this problem. In some fuzzers, this means prioritizing inputs to mutate based on whether they execute any code other than validity checks; but in fuzzers such as Angora [26] and Eclipser [29] that use lightweight constraint-solving to cover branches, the process can be more sophisticated. We have begun discussions with the Eclipser team, and they confirm that identifying precondition code and devising suitable heuristics to handle it (e.g., never solve for a negation of a passed check) should improve performance. Devising effective heuristics to tune both "classic" mutation fuzzers and concolic gray-box fuzzers promises to improve test generation not only in our context, but in general. Fuzzing of individual functions or sets of functions is a highly promising area: most fuzzing is applied at the whole-program level, where learning to produce interesting inputs can be an overwhelming problem. By focusing on a middle-ground between unit testing and whole-program fuzzing, that is by using modern fuzzer technology to drive property-driven testing, the problem may be more tractable. Prioritizing paths that are not input validation is an explicit goal of, e.g., AFLFast [20], but it must work with an implicit definition based on path frequencies, while we have access to more precise data. Given the possible complexity of a state validity check, there may be hard-to-reach—but fundamentally

uninteresting—ways to create invalid input; AFLFast will prioritize such paths, while our approach will (correctly) avoid them.

This effort also connects to a second fuzzing research thrust: making specification elements that do not correspond to simple code coverage visible to a fuzzer. In this example, consider the `DeepState_Timeout` check (note that this itself is functionality we will develop as part of handing timing constraints in FRAMA-C and DeepState). Unless we break down the timing analysis explicitly using a set of conditional branches, coverage-driven fuzzers cannot distinguish an execution that is very slow (close to violating the constraint) from one that has the minimum execution time possible. We propose to make timing of such specified events visible to a fuzzer, by modifying coverage bit-vectors to incorporate bucketing of execution time. Once we add such novel coverage measures, and introduce distinctions between coverage classes (as with preconditions), we will research how to balance competing priorities in more complex notions of coverage. In addition to implicit execution properties such as timing, this effort can apply to coverage of data structures, which is also a critical problem in fuzzing data-driven code such as machine-learning algorithms, where much of the behavior is implicit in, e.g., the route taken through a forest of decision trees. We assume that as we investigate real world examples, further challenging research problems in property-based fuzzing will arise and require improving fuzzer science and art. In essence, this proposal aims to extend the work, including AFLFast [20], FairFuzz [73], VUzzer [85], and other efforts [107, 8], that prioritizes certain program paths over others in an intelligent way, by specializing that set of approaches to the case of property-based testing with a stronger specification and understanding of interacting functions and data structures.

3.3 Case Study: Sensor/Actuator Networks for Ecological Monitoring and Control

Overview: The first case study informing this research is the embedded software used in the Southwest Experimental Garden Array (SEGA) [31, 41, 11]. SEGA is a large collection of operational wireless sensor/actuator networks for monitoring and control of ecological systems, located at 17 sites in the states of Arizona and California. Currently, SEGA consists of 138 wireless nodes and is planned to expand to a total of 154 nodes at 21 sites in the coming years. As a genetics-based climate change research platform, SEGA allows scientists to quantify the ecological and evolutionary responses of species to changing climate conditions. Multiple long-term and large-scale scientific experiments are conducted at SEGA sites.

The SEGA nodes use a multi-processor architecture. A central processor provides services, including scheduling and dispatch of tasks, storage, and a message-passing interface for wireless networking. Plug-in satellite processors handle transducer sampling, actuation, and related computational tasks. In addition to allowing true parallelism, this architecture enables hardware-level improvements in energy efficiency, since each satellite can be optimized for its specific task. More practically, it admits the rapid implementation of highly heterogeneous nodes that incorporate a wide range of sensing and actuation capabilities. The nodes synchronously interact with neighbors in a multi-hop, self-organizing/healing network; synchronization is implemented as scheduled rendezvous in time slots; slot boundaries are managed by a lightweight global time synchronization protocol that is integrated with low-level communication synchronization. The nodes use a custom time-triggered RTOS tightly integrated with a time/frequency-hopped PHY/MAC protocol. This approach minimizes communication energy cost, which dominates the overall energy consumption.

Problem: Because timing is critical and is determined by the embedded system hardware and software, most testing has occurred at the network level, with extensive in-lab testing with small networks and instrumented field tests. However, it has been found in long-term deployments that occasionally the networking fails and nodes become isolated—we think due to a complex set of subtle bugs rooted in different levels of timing abstraction. When such a failure occurs, it often spreads from one node to others, causing nodes to seek to rejoin and expend high levels of energy for radio operation and eventually deplete their energy sources. Eventually, subnets, or sometimes the entire site, are disabled and humans must visit the site to reboot it. Such failures could affect or even destroy (e.g., via over-watering), long-running scientific experiments.

Since access to SEGA installations can be difficult, and in the long run many may be located so remotely that it is cost-prohibitive to send humans to address problems, discovering the source of these in-operation

faults, identifying other faults, and generally improving the reliability of the system is critical. We therefore aim to use SEGA (in particular the protocol in question and its implementation) as our primary case study. This will enable us to apply our approach in a practical setting, and ensure that what we produce is actually usable by engineers of real systems. SEGA is an ideal case study for several reasons. First, the above mentioned network problem enables exploring how to design, prove, and test time-critical systems in a way that does no harm: human life is not affected in this application, and data is not lost since all sensed information is logged as a local back-up. On the other hand, reliable operation is important, and failure costly. Finally, this application uses common data structures for task control blocks, and the operating system at each node schedules and dispatches both periodic and pseudo-randomly scheduled tasks. Thus the system is representative of general applications of scheduling and synchronization in time-critical systems. The embedded code is written in C, enabling the use of both FRAMA-C and DeepState. SEGA will help us understand how our theory and tools can improve the correctness, reliability, and safety of cyber-physical and IoT applications.

Plan: First, we will model the protocol itself as a timed automata in UPPAAL or PRISM, in order to ensure that there is not a subtle flaw in the protocol itself, and to model our expectations of behavior in the real system. Then, following our proposed workflow, we will automatically annotate the implementation with specifications extracted from the timed automata model and attempt to prove components of the code faithfully represent the intended behavior. Either of these steps may expose the source of the mysterious networking failures. Whether at this point the current problem is identified or not, we will finally use DeepState, driven by harnesses automatically generated by our tools, to generate tests of the implementation components in question. Even if FRAMA-C is able to prove most individual functions correct, which we believe is unlikely, the DeepState testing may expose faults that are not part of the specification. The above workflow will be conducted by an Embedded System Engineering student, who is familiar with the SEGA IoT system but does not have expertise in software verification and testing, using the software tools developed in this project. Feedback from the engineer in this case study will inform us how to develop and improve the theory and tools for practical usages by non-expert users in real applications.

3.4 Case Study: Distributed Coordination in Multi-Robot Systems

Overview: Coordinated operation of multiple autonomous robots (multi-robot systems) has many important real-world applications [23, 103]. For example, in a rescue, security, or disaster response mission, several autonomous aerial robots can coordinate to survey an area, monitor some target objects or activities, and guide ground robots or vehicles. In such applications, each robot is autonomous but has the capability to coordinate efficiently and safely with other robots to complete a shared mission, often in a distributed manner without any central coordinator. Such coordination is essential in real-world applications where the environment is constantly and unexpectedly changing, but is also very challenging. The Intelligent Control Systems (ICONS) Lab at NAU, directed by co-PI Nghiem, is developing distributed control and planning methods for multi-robot systems on a platform that includes quadcopters and four fully autonomous vehicles. One of the most critical challenges of this research the guarantee of the safety, of a coordination plan, which is typically implemented in C code on the embedded computers of the robots and usually involves wireless inter-robot communication, sensing, and actuation.

Problem: Validation of a distributed coordination method for a multi-robot system is currently performed using a mix of theoretical proof (for limited settings), extensive computer-based simulations, simulation-based falsification techniques, and real experiments. Even when a method is validated by proofs and/or simulations, it often fails in real experiments due to discrepancies between models and reality/implementation. The methods and tools proposed in this project will help control and robotics researchers, who usually do not have expertise in software verification and testing, overcome this challenge.

Plan: First, we will model a coordination plan/algorithm for multiple robots as a (potentially very complex) network of timed automata. Performance specifications will be expressed in temporal logics, e.g., the

Signal Temporal Logic (STL) [36], and checked against the model using verification and testing tools such as UPPAAL or S-TaLiRo [7]. This step ensures that the original coordination algorithm has no subtle flaws. An implementation of the algorithm in C code, distributed among the robots, will be developed by a robotics/control student. The implementation will then be automatically annotated with a specification using our tools. Next, we will attempt to prove that components of the code faithfully represent the coordination algorithm. Given the complexity of multi-robot coordination algorithms, we do not expect FRAMA-C to be able to prove all the components of the implementation correct. We will thus use DeepState harnesses automatically generated by our tools to generate tests of the implementation components not yet verified by FRAMA-C. Finally, we will perform experiments with aerial and ground robots in the ICONS Lab. The very different nature and complexity of this study, compared to SEGA, will ensure that our methods and tools work in a variety of kinds of real systems.

3.5 Work Plan and Evaluation Approach

The project will be organized into three phases, described by work packages. In the first phase, T3.1 will be conducted along with T1.1 and T2.1, and will inform the development in these tasks. In the second phase, the focus will be on the development of translation methods in T1.2 and T2.2. In the last phase, software tools will be developed (tasks T1.3 and T2.3) and applied to the case studies (tasks T3.2, T4.1, and T4.2), whose results and feedback will help refine the developed tools. It is important that the tasks of the work packages are carried out in tandem and in close collaboration. The timeline of the tasks will be structured as shown in Figure 4.

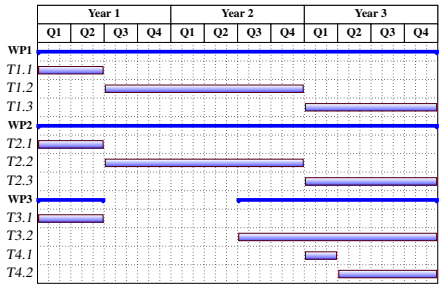

Figure 4: Project schedule.

Work Package 1 (WP1): This work package concerns the principles and extensions to FRAMA-C for automatic translation of networks of timed automata into ACSL and ghost code (see Section 3.1): WP1 consists of the following tasks:

- T1.1: This task will study the formal semantics of timed automaton networks defined in UPPAAL and PRISM, and define an appropriate set of the timed automaton semantics considered in this project. The semantics would be rich enough for modeling the application systems considered in the project, specifically in WP3, while simple enough for the translation into annotations usable by static analysis tools (FRAMA-C) and dynamic analysis tools (DeepState). As such, there will be close collaboration and iterative design steps between this task and the other work packages.
- T1.2: This task will develop several methods for automatic translation of timed automaton networks into ACSL annotations and/or ghost code. Depending on the target usage, whether for static analysis or dynamic analysis or being inspected by programmers, a suitable method will be developed.
- T1.3: We will implement the methods developed in T1.2 as FRAMA-C plugins. The developed tools will be tested on the case studies (WP3), whose results will inform the tool development process.

One Ph.D. student will be needed to conduct the work in this work package, which will last for the entire duration of the project. The student will collaborate closely with students in WP2 and WP3.

Evaluation: Evaluation of WP1 will be determined by the set of timed automata networks that can be translated into ACSL and ghost code, and the ability to use that code to prove properties. We will use benchmark examples (realistic code found on GitHub or in embedded systems textbooks) to some extent, and simple test cases for constructs, but primarily rely on our case studies for evaluation.

Work Package 2 (WP2): This work package covers methods and tools to automatically translate ACSL-annotated code in FRAMA-C into a DeepState test harness (Section 3.2):

- T2.1: This task will extend the E-ACSL semantics and optimize the implementation of symbolic execution and fuzzing, so that ACSL annotations generated from timed automaton networks (in WP1) can be used in DeepState to test implementation code.

- T2.2: This task will develop methods to translate annotations and ghost code generated for static analysis in WP1 to test specifications in DeepState. It will be carried out concurrently with tasks T1.1 and T1.2 in WP1, and will inform the design and method development in those tasks.
- T2.3: In this task, we will implement the methods developed in T2.1 as extensions to DeepState. The tools will be applied to the case study in WP3, whose results will inform the development of the tools.
- T2.4: In this task, we will augment DeepState and fuzzers in the multiple ways described in Section 3.2.

The execution of this work package will span the entire duration of the project. One Ph.D. student will work on the tasks in WP2, and collaborate with the students in WP1 and WP3.

Evaluation: Evaluation of Work Package 2 will be determined by the successful generation of DeepState harnesses for ACSL annotated code, and the successful application of those harnesses to generate tests for realistic systems. We will again use benchmarks and simple examples to some extent, but primarily rely on our connection to case studies. In the case of test generation, in addition to faults detected, we will use code coverage and other standard benchmarks [67].

Work Package 3 (WP3): This work package will focus on the applications described in Sections 3.3 and 3.4, as both a way to inform the methodology and tool developments in the other work packages and case studies in two completely different domains to validate our methods and tools. WP3 includes two case studies:

SEGA case study (Section 3.3): This application is divided into two tasks:
- T3.1: In this task, the existing SEGA system will be studied thoroughly to extract the key requirements and characteristics of the embedded system implementation. Timed automaton models of the communication protocol used in the system, at different levels of abstraction, will be developed and formally verified in UPPAAL and/or PRISM. The system information and models resulted from this task will inform the semantics design and method developments in WP1 and WP2. As time allows, and pending results with communication protocol, we will extend this to include sensing and control elements.
- T3.2: This task will apply the tools developed in WP1 and WP2 to the SEGA system, in order to detect and fix bugs in the current implementation that cause the intermittent failures mentioned in Section 3.3. It will also provide feedback to the other work packages to refine and improve our tools.

Robotics case study (Section 3.4): this study, in the last year of the project, is divided into two tasks:
- T4.1: In this task, a multi-robot coordination algorithm currently used with our existing multi-robot system will be modeled as a network of timed automata. Using our insights into the robotics application, we will express its performance specifications, particularly its safety requirements, in temporal logics and formally verify or test them in tools like UPPAAL, PRISM, or S-TaLiRo. This task will extend the semantics and methods developed to applications beyond communication protocols.
- T4.2: This task will apply the tools developed in WP1 and WP2 to the coordinated multi-robot system, in order to validate the implementation code and detect and fix its bugs. It will also provide feedback to the other work packages to refine and improve the tools developed in this project.

As the tasks in this work package are conducted in tandem with WP1 and WP2, to form a feedback loop with the developments in other work packages, it will last for the entire duration of the project. We expect that groups of undergraduate students and two Ph.D. students, who will join the project in the second and third years, in collaboration with the Ph.D. students in WP1 and WP2, will perform the work.

Evaluation: In essence, this task *is* the evaluation aspect of our project, which forms one of the major thrusts of the project. The successful application of WP1 and WP2 tools to the case studies is essentially the driving factor in determining our success in the project. The measure of success is (1) faults detected and corrected (2) functionality proven correct in FRAMA-C and (3) coverage and other measures of generated tests.

4 Related Work

A fundamental goal of this project is to reduce both user effort and the opportunity for user effort by allowing minimizing (ideally to one) the number of times a user must specify an aspect of system correctness.

The principle that important information should have a "single point of truth" is widely accepted in software engineering, even in such foundational early advances as avoiding repeated magic numbers by the use of named constants. Such a principle can be extended to specification and definition of test harnesses. Early work emphasizing this goal of both reducing work and chance of error in specification and test generation included the effort by Groce and Joshi to use a single harness for both model-checking and random testing, in the verification of the Mars Science Laboratory's file system [47, 49, 53]. In later work, Groce and Erwig extended this idea to propose development of a single language with a unified semantics for a wide variety of dynamic test generation tools [46]; this approach is essentially realized in the DeepState [43] system. Indeed, FRAMA-C and ACSL [10] and DeepState are both arguably limited instantiations of this goal: providing a single language, interface, and semantics that is applied to a variety of methods (static or dynamic) for checking that a specification holds. This project aims to further extend this goal by extending it to include a formal timed-automata model and to connect the primarily static and dynamic approaches.

There are several work on the implementation and verification of distributed systems, and code extraction from automata modeling in the proof assistant COQ [99, 101, 83] Systems developed in this way are executable thanks to COQ's extraction mechanism (to OCaml [78] code). While being very interesting, these proposals require that the developers master COQ, and start from the modeling activity to generate code. They are therefore not applicable in the context of the verification of legacy embedded C code.

Testing real-time systems modeled by networks of timed automata was investigated by the authors of the tool UPPAAL [61, 60, 70] and implemented in the tools UPPAAL-TRON (`http://people.cs.aau.dk/~marius/tron/index.html`) and UPPAAL-COVER (`http://www.hessel.nu/CoVer/index.php`). These tools generate tests, either offline or online, for conformance testing of a real-time system with respect to its model and an environment model, both as timed automaton networks. In both cases, the real-time system is considered a black-box with an input/output interface through which the test generator or monitor can change the system inputs and observe the system outputs. The actual implementation code is not considered and is in fact hidden from the testing tools. While this approach is general, it has several drawbacks. It requires a centralized input/output interface accessible to the testing tools. Such an interface is not always available in all systems, especially in large-scale distributed systems like the sensor/actuator networks considered in our case study. Furthermore, by considering only the (timed) input/output behavior of a system, this approach may not be able to test internal system behaviors and therefore miss opportunities for a better test coverage. Finally, regardless of how thorough the tests are, generally they will not be able to provide a formal guarantee of the conformance between the implementation and the model / specifications. On the contrary, if the system code is available, our proposed approach can potentially provide such a guarantee.

5 Broader Impacts

Improving Software System Reliability: A key element of our approach is to focus on realistically deployable techniques. Part of this effort is concentrated in our internal effort to apply our methods to the SEGA project. However, we also plan to aim for early integration with NASA's FPrime [19, 80] open source flight software architecture and platform; PI Groce is already in discussion with engineers at NASA's Jet Propulsion Laboratory, and engaged in producing tests for the FPrime autocoder using DeepState. This integration will allow our methods to be applied to CubeSat missions (and other flight software systems), leading to improved reliability for low-budget space-based scientific efforts. We expect, in the long run, that our approaches will lead to more reliable and robust development in many embedded and cyberphysical systems domains, and contribute to a more secure and reliable Internet of Things. One key goal of this project is to increase the synergy between formal modeling, heavyweight static analysis, and advanced dynamic analysis using automated test generation tools, and thus adoption of all three methods.

Education and Outreach: The proposed research yields several opportunities for enhancing CS education, recruiting new CS majors, and retaining CS students, particularly members of underrepresented groups. In addition to the activities discussed at length in the Broadening Participation in Computing plan, PI Groce will work with the NAU Student ACM Chapter to present a series of "excursions in testing" that introduce

automated testing to students, using DeepState to find bugs in real world code, including code from media player libraries; in advanced meetings, integrating DeepState with FRAMA-C will be demonstrated as well. The work of Guzdial [57] has shown that media computation is a potentially effective way to both recruit and retain female and under-represented minority students in computer science. Groce is also teaching a class on automated testing of embedded systems to graduate and undergraduate students. Co-PI Nghiem is preparing a new graduate-level course on autonomous vehicles, based on the F1/10 platform (`http://f1tenth.org/`), to be offered to EE and CS students at NAU. To prepare students in addressing one of the greatest challenges of autonomous driving, namely safety guarantee, the course will incorporate the methods and tools developed in this project to teach students about safety, verification, and testing. Each year, Loulergue teaches CS451/551 Mechanized Reasoning about Programs to about 40 students. This class is based on FRAMA-C, and Loulergue transitions his research on formal methods into this class. Loulergue has presented many FRAMA-C tutorials in conference such as ISSRE, ACM SAC, FM, SecDev, *etc.*, and will continue to do so.

6 Results From Prior NSF Support

PI Groce: The most relevant prior NSF support for PI Groce is CCF-1217824, "Diversity and Feedback in Random Testing for Systems Software," with a total budget of $491,280 from 9/2012 until 9/2015, a collaborative proposal with John Regehr of the University of Utah. **Intellectual Merit:** The results of CCF-1217824 included a number of advances to practical automated generation and use of tests, a key focus of this proposal as well. E.g., an approach to creating "quick tests" from a test suite by minimizing each test with respect to its code coverage [52], won the Best Paper award at the 2014 International Conference on Software Testing. CCF-1217824 produced a general set of results focused on making automated random testing usable by practitioners, and using symbolic execution on larger, realistic software. Publications resulting from this grant were numerous [51, 27, 105, 52, 50, 4, 55, 62, 54, 5]. **Broader Impact:** The results of CCF-1217824 have been used in teaching software engineering classes. Work from the project contributed to the discovery of previously unknown faults in important software systems, including LLVM and GCC, and is widely used in compiler testing [71, 69, 35, 72]. Tools and data sets from CCF-1217824 are available via GitHub in multiple repositories and projects (TSTL, Csmith, CReduce, etc.).

Co-PI Flikkema: Flikkema is co-PI on the Southwest Experimental Garden Array (SEGA) funded by an NSF development MRI (DEB-1126840), with a total budget of $2,848,876 from 10/2011 until 9/2017. **Intellectual Merit:** SEGA is a facility distributed across a 1615m elevation gradient in Arizona that supports long-term research to increase understanding of and mitigate climate change using knowledge of genetic variation in species of concern. It consists an array of eleven gardens and supporting distributed monitoring and control cyberinfrastructure for the study of gene-by-environment interactions and enabling development of strategies to best manage for future climates. **Broader Impact:** With 9 successfully completed projects to date, SEGA currently supports 11 experiments and has resulted in over 35 publications and 20 conference presentations. SEGA results are available online [1].

Co-PI Loulergue & Co-PI Nghiem: have not received any NSF support.

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