

# FMitF: Track I: A Pathway for Combining Formal, Static, and Dynamic Analysis of Real-World Embedded Systems

## 1 Problem Statement, Overview, and Objectives

The core problem we aim to address in this proposal is that *use of formal modeling, advanced static analysis, and advanced dynamic analysis* for verification and validation, especially on critical embedded systems, is prohibitively difficult and lacks sufficient synergy for cost-effective application. This is true even of systems built in an academic research context: that is, unless the research is primarily *about* methods for verifying and testing systems, rather than work on an embedded system for its own sake, these methods are hard to apply. Furthermore, even when use of these techniques to ensure correctness, reliability, or security *is* a focus of the project, such use is almost always limited to one type of effort—model checking, theorem proving, or automated test generation. A major cause for this difficulty is the *lack of synergy* between these related efforts, the failure of effort in one context to transfer to another context. In short:

- Learning to use a formal modeling language and tool, such as UPPAAL [10], PRISM [59], or SPIN [55], provides help in discovering defects in a high-level, abstract formulation of a model or protocol, but seldom helps with implementation-level problems not directly modeled in the formalism.
- Many static analysis tools are primarily “bug detectors” (e.g., Coverity or CodeSonar), whose output is essentially limited to a list of possible problems; devising test inputs to reject false positives is hard.
- More powerful static analysis tools, such as FRAMA-C [56], provide proofs of correctness for limited aspects of a system, and a rich specification and annotation language. However, there is little or no connection between this annotation and either formal modeling or state-of-the-art test generation.
- There are a large variety of automated test generation tools; however, effort spent learning one tool only partially transfers to another tool. Furthermore, many of the most powerful such tools (e.g., AFL [91]) are specialized to the problem of finding *crashes*, and do not leverage other types of specification efforts *at all*.

Consider the case of an embedded systems engineer working on a custom, low-energy consumption, communication protocol for use in a network of low-power sensors and actuators. If she builds a formal model of the protocol, she will likely discover that this extensive effort provides no help, other than an improved concept of the system, in proving the correctness of her *implementation*. If the engineer begins instead by building an automated test generation harness she will find that, despite having spent considerable time expressing pre-conditions and post-conditions for various functions in the implementation, the work must be duplicated when she decides to try to formally prove the correctness of core functionality. Had she begun with the proofs, again, logically related (or even equivalent) information would have to be re-expressed, in a different language, to perform test generation. Not only must our engineer learn three tools, but effort spent in using one tool almost never carries over to another approach. In almost all cases, there is simply not enough time or energy available to make use of the full spectrum of available technology. In practice, *no advanced correctness technology may be used at all*. After all, it is hard to predict which one(s) will have the greatest payoff, or even work at all, so perhaps it is best to just put more effort into manual testing.

### 1.1 Proposed Solution

While allowing efforts from any form of formal or automated verification or validation attempt to carry over to other forms (i.e., formal models to code annotations for static analysis, code annotations to test harnesses, test harnesses to code annotations, test harnesses to formal models, formal models to test harnesses, and code annotations to formal models) is the ideal goal, simply making it possible to follow *one* critical path to combine methods is feasible given current technologies in the sub-domains (formal modeling, static analysis, and dynamic analysis) and a set of specific advances in bridging the gap between the technologies.

Which path is most important to realize? Our approach is based in the reality of the embedded systems domain, where, while formal modeling is sometimes used, there is, in real-world efforts, *always* an implementation. The most basic obstacle to the adoption of formal methods in embedded systems work is that if there is only the usual informal design effort or the adaptation of a legacy implementation, formal methods

are often simply inapplicable. By focusing on *adding annotations to implementation code*, and exploiting those annotations to enable a set of potentially bug-finding or correctness-proving analyses, we promise to *always* give embedded systems engineers a reasonable payoff, often in the form of *tests showing real bugs*.

This project therefore proposes to make it possible to introduce specifications into implementation code that can be directly checked using sophisticated automated test generation strategies, including symbolic execution, advanced fuzzing, explicit-state model checking, and SAT/SMT-based bounded model checking. Furthermore, these specifications can be directly exported to form the basis for formal models using, e.g., timed automata. In the long run, to benefit those developers who are more open to formal methods already, we hope that these annotations can be imported from a timed automata representation, but we begin where most embedded systems developers are, now, not where we hope they may be, someday. We additionally focus on using frameworks/front-ends allowing application of multiple approaches. Our commitment is to enabling *a maximum diversity of analysis methods with a minimum of specification and tool-learning effort*, to make formal methods attractive *simply because of their expected cost-benefit ratio*.

This project is specifically focused on embedded and networked systems, specifically wireless sensor networks and multi-robotic systems, where timing, communication, interactions with the physical world, and uncertainty are some major challenges in modeling the system behaviors. However, we anticipate that our solution will generalize to other application domains that share the characteristics and main challenges with our applications. We expect developers to learn new tools, but not new programming paradigms or languages. The proposed contribution to embedded systems design is not a radical reworking of development methods, which, like many formal methods efforts in the past, would be unlikely to achieve widespread adoption, but the introduction of *an advanced form of unit testing*, that works with, e.g., legacy code, with more powerful methods for specification and checking of correctness. This will modify development, in that design-for-testability and design-for-verifiability will become second nature—just as the introduction of the possibility to express *and check* strong typing constraints changed Python development practices for projects where reliability and correctness really mattered. This project is therefore based on the following core ideas:

- 1. The primary obstacle to adoption of formal methods approaches in embedded systems development is not a lack of relevant methods and tools.**
- 2. In particular, there are methods and tools that apply to the *implementation* of embedded systems in C and C++; every embedded software system requires an implementation.**
- 3. However, learning and using any one of these tools may or may not “pay off” and the effort spent is only of limited application when applying another tool.**
- 4. Therefore, to improve embedded systems development via formal methods we need:**
  - (a) an *implementation-focused common framework* for applying methods and tools and**
  - (b) a focus on *practically-inspired* improvements to methods and tools.**

## 1.2 Field Application Domains

The proposed research is motivated by applications in embedded and networked systems, in particular wireless sensor networks and multi-robot systems. A wireless sensor network (WSN) consists of multiple, often many, sensor nodes that communicate via a wireless network with servers and/or other sensor nodes. In a WSN, each sensor monitors some physical quantities, such as air temperature, humidity, and CO<sub>2</sub> concentration level, and exchanges its measurement data with other entities for specific objectives, such as for monitoring and forecasting wildfires. Each sensor node typically has some limited computing power (an embedded microprocessor) and limited energy provided by a battery and/or a renewable energy source. Furthermore, wireless communication in a WSN is often subject to frequent packet drops and other failures. Consequently, some of the major challenges for the reliability and correctness of WSNs include timing and communication uncertainty, and computing and energy constraints. In addition, testing and verifying code for sensor nodes faces another significant hurdle due to the nature of interacting directly with the physical world, which involves another level of uncertainty and is not always easily replicable in a software testing or verification tool. A multi-robot system (MRS) consists of multiple robots, possibly of different types

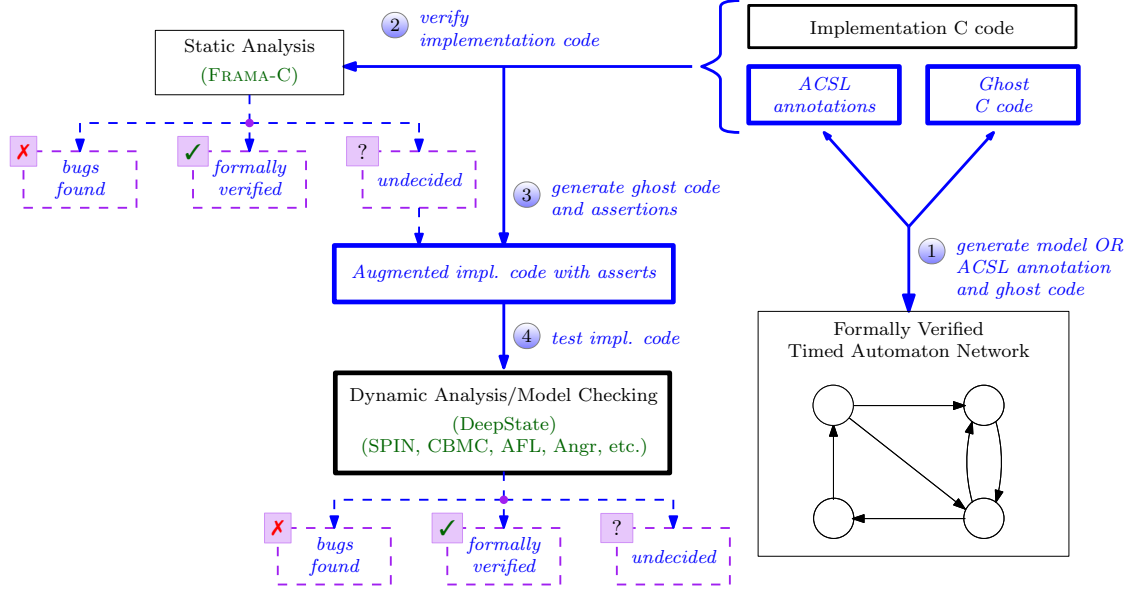


Figure 1: Overview of the proposed research.

such as terrestrial robots and aerial drones, which coordinate to perform certain tasks, such as package delivery, disaster rescue, and surveillance. An MRS carries similar major challenges as a WSN. Due to the complexity of their dynamics and interactions with the physical world, testing and verifying software for robots, especially cooperative robots in a MRS, is particularly challenging.

In summary, this project focuses on the following major challenges of the field application domains of embedded and networked systems: (1) timing and communication uncertainty, (2) complex dynamic behaviors, and (3) interactions with the physical world. They will be addressed by a combination of approaches, from both the formal method and software testing disciplines and the field application disciplines. Case studies in real-world WSNs and MRS, which are representative of embedded and networked systems and their challenges, will be used for validating and demonstrating our proposed solution.

### 1.3 PI Qualifications

See the collaboration plan for an extensive examination of PI Qualifications; in brief, PI Groce has extensive history with formal methods and testing tool development, and practical application to real-world embedded systems. Co-PI Nghiem is an expert in control and autonomy for robotics, including use of formal methods, and Co-PI Flikkema has extensive experience with deployed real-world embedded systems and networks.

### 1.4 Intellectual Merit

The aim of this proposal is to (1) identify a set of principles for the analysis (formal, static, and dynamic) of implementations of embedded and networked systems; (2) match these theoretical principles with tools usable by engineers developing such systems; and (3) enable the synergistic use of enhanced versions of these tools in real applications through a common framework with minimal duplication of effort and maximal extraction of information from shared annotations. In the first case study, we will analyze networks of wireless sensor nodes deployed in the Southwest Experimental Garden Array (SEGA) [89, 31] – a distributed facility for examining climatic, genetic, and environmental factors in plant ecology – and in the Distributed Sensing & Computing Over Sparse Environments (DISCOVER) Platform – an NSF CCRI project that develops a large-scale and diverse testbed for wireless sensor networks and multi-robot systems. The second case study will use the framework to formally verify and dynamically test implementations of autonomous control and coordination of multiple autonomous terrestrial and aerial robots on the DISCOVER platform.

Figure 1 shows the overall concept. The core open research problems addressed are represented by two sets of arrows. First, an engineering design, expressed as C code, is provided, and annotated with correctness properties, information about the expected environment (constraints on sensor values, etc.), and hints to guide heuristic application of tools ranging from fuzzers to symbolic execution engines to model checkers. While they are not the focus of this project, code to apply advanced static analysis or timed automata (TA) model skeletons can also be automatically generated. Our goal is to certify whether the C code truly implements the correctness properties in question, with a focus on dynamic approaches:

1. A (generated) TA model can be used to check high-level properties of the design, ignoring many low-level implementation details. However, this step is often skipped in practice.
2. The implementation code with the ACSL annotations and ghost code can be checked by a static analysis tool, such as FRAMA-C. In some cases this will verify the code, and in other cases a definite bug will be found; but often the result will be “undecided” and further analysis required to see if a bug is spurious or real. Again, this step can be skipped, though it is likely low-cost and beneficial.
3. Finally, the focus of our efforts is a multi-pronged attempt to refute correctness (or increase our confidence in it) via dynamic analysis—automated test generation—and implementation-level model checking. Ghost code, additional assertions, and needed test-harnesses are *automatically generated* from annotated code.
4. The augmented implementation code is then analyzed using the DeepState [35] framework, which serves as a front-end to highly scalable fuzzers, as well as to symbolic execution tools and explicit-state and SAT/SMT-based bounded model checkers that can detect more bugs at the cost of restricted applicability or scalability. Generated test cases may prove the system faulty, or improve confidence in the system.

Our focus is on providing a unified specification method that can be applied to source code itself, and on enabling and enhancing the dynamic analysis and explicit-state and SAT/SMT bounded model checking aspects of the approach. We believe these approaches are currently the most difficult to apply, and the most likely to dramatically improve the ability to detect bugs in complex embedded systems designs.

**Principles:** Assuming that an algorithm for an embedded and networked system, such as a communication protocol, can in theory be described as (probabilistic) timed automata [5], which satisfies temporal logic formulas [15], and implemented as a set of imperative programs that realize these timing constraints and other correctness conditions, we ask:

- Given a set of annotated programs, how can we best automatically find bugs in those programs (and, in some circumstances, for some properties, prove correctness), based on an annotated specification?
- Can we generate a skeleton of a timed automata model from annotated programs, in order to facilitate adoption of design-level analysis by traditional embedded systems developers?

Note that these problems differ considerably from the more studied, but more limited, synthesis problem. We are not assuming that system development will involve first producing a formal model, then using that model to automatically generate an implementation; rather, we consider the typical real-world scenario, where modeling is a separate activity, either undertaken after implementation due to concerns about reliability, or an activity during design that only indirectly informs the implementation. That is, the more studied problem is producing a runtime semantics for a model; we address the problem of reconciling a runtime semantics with a model semantics, without unrealistic burden on engineers. To the extent that developers apply more rigorous testing and analysis of their systems, they primarily use unit tests and static analysis (and occasionally rudimentary fuzzing). Any effort to increase the adoption of formal methods and automated test generation approaches, including implementation-level model checking and symbolic execution, is likely to be successful to the extent that it enters embedded systems engineering practice via this existing pathway. Engineers at Google have referred to this approach as “meeting developers where they are” [73].

**Tools:** We will focus on C code, using DeepState [35] as a front-end for dynamic and implementation-level model checking approaches, and UPPAAL [10] and PRISM [59] for the analysis of protocols; FRAMA-C will provide a powerful static analysis framework, and we will adopt its ACSL language developed for FRAMA-C as a basis for our specification language. The primary open research questions here are numerous, and include: (1) how to extend existing specification languages to support timing, interrupts, and uncertainty;

(2) how to assign the same meaning to a specification construct in various contexts, ranging from fuzzing to symbolic execution to explicit-state model checking to bounded model checking in the “dynamic” DeepState world, and including a static context for FRAMA-C and a modeling context for timed automata; (3) how to minimize annotation burden while allowing developers to include information that can be exploited by those methods: e.g., to make intelligent use of pre-conditions in fuzzing, to automatically derive loop bounds in bounded model checking, and to restrict branching factors and store state in explicit-state model checking; (4) how to handle intra-program parallelism; (5) how to ensure that the methods are sufficiently automatic and behave in ways engineers (not formal modeling, static, or dynamic analysis experts) will expect. Our focus will be on *practical* solutions, guided by the embedded domain experts, rather than on purely theoretical approaches that do not scale to real systems. Practical solutions here require fundamental contributions to system and specification design and dynamic analysis and model checking technologies.

**Field applications:** This project will contribute significantly to the field domains of embedded and networked systems, especially in safety-critical applications where correctness and reliability are vital. The practical methods and tools developed by our team will enable domain experts, particularly domain engineers without formal training in formal methods and software testing, to test and verify their code against critical requirements to not only reduce bugs but also gain confidence in their systems.

## 2 Background and Preliminary Research

### 2.1 A Foundation for Implementation-Level Specification

Ideally, the development of critical embedded systems should rely on a combination of formal methods to achieve an appropriate degree of guarantee: automatic static analysis to ensure the absence of some runtime errors, deductive verification to prove functional correctness of aspects of the code, and runtime verification for parts of the code that cannot be (or are not yet) proved using deductive verification, or that generated *warnings* from static analysis requiring confirmation of a problem or refutation of the feasibility of an error. A core question in our approach is how to represent a specification in a way that is intimately tied to real implementation code. However, as development of a specification language is not our primary focus, we prefer to build on existing work in the area, extending it as required.

This project will therefore make use of the ideas developed in the ongoing work on the FRAMA-C (<https://frama-c.com>) [56] tool as a foundation for a specification and annotation language. FRAMA-C is a widely-used source code analysis platform that aims at enabling verification of industrial-size programs written in ISO C99. FRAMA-C supports combinations of different approaches, by providing its users with a collection of *plugins* for static and dynamic analyses of safety- and security-critical software. Moreover, collaborative verification across cooperating plugins is enabled by their integration on top of a shared kernel, and, most critically for our purposes, their compliance to a common specification language: ACSL [8]. ACSL, the ANSI/ISO C Specification Language, is based on the notion of a contract as in JML, the Java Modeling Language [64]. ACSL allows users to specify functional properties of programs through pre/post-conditions, and provides different ways to define predicates and logic functions. Many built-in predicates and logic functions are provided, to handle, for example, pointer validity or separation; ACSL is essentially a typed first-order logic that contains C expressions, and is designed to be rich but easy to understand. FRAMA-C is already applicable to verification of typical legacy embedded C code.

Using ACSL/FRAMA-C means that while focusing on dynamic analysis and model checking, our approach automatically provides an additional benefit for embedded systems engineers: access to the current set of powerful FRAMA-C static analyses. FRAMA-C provides both abstract interpretation [28] based analysis plugins and deductive verification plugins based on a weakest precondition calculus; the latter have recently been improved to make proof without interacting with a theorem prover easier for engineers [11].

FRAMA-C was designed as a static analysis platform, but has been extended with limited plugins for dynamic analysis. One of these plugins is E-ACSL, which supports runtime assertion checking [25]. In FRAMA-C, E-ACSL is both the name of the assertion language and the name of a plugin that generates C

code to check these assertions at runtime. E-ACSL is a subset of ACSL. The plugin E-ACSL is used to translate a subset of FRAMA-C assertions into executable C code. However, the E-ACSL plugin does not support all the specification constructs we need, or assist developers in the most difficult part of dynamic analysis: constructing a set of tests that exercise the checks. The only assistance provided by FRAMA-C in this task is, as discussed in the next section, very limited in capability. Again, rather than “re-inventing the wheel” and offering a solution that lacks a strong static aspect we aim to address this limitation, and extend ACSL and E-ACSL, in accordance with our focus on common frameworks and cross-tool synergy.

## 2.2 Dynamic Analysis with DeepState

While FRAMA-C provides powerful tools for static detection of program faults and generation of runtime checks for properties that cannot be discharged by formal proof or sound static analysis, it provides only limited, and difficult-to-scale, ability to generate program inputs to exercise runtime checks, limited to one tool, PathCrawler [87], that aims to produce a unit test for a single function, using concolic testing (dynamic symbolic execution [34]). In cases where this fails to scale, PathCrawler will fail. Furthermore, PathCrawler is tuned to the problem of testing a single function, not producing more complex scenario-based tests of a set of functions that must coordinate state changes. Finally, PathCrawler is not an open source, extensible system, may be costly to acquire and use, and is arguably impossible to extend.

The limitation of dynamic analysis tools to PathCrawler is a major weakness of FRAMA-C from the perspective of a user. Scalability of symbolic-execution-based test generation methods is extremely difficult to predict, and producing complete and exhaustive preconditions that allow a function to be tested entirely in isolation is often either too time-consuming or essentially impossible, because the actual environment is only represented by the set of states reachable using a set of coordinating functions or a library. These problems are pressing, for several reasons. First, full formal proof of correctness is, at present, impractical for most realistic systems. The actual work of fault detection and validation of software still relies, fundamentally, on effective testing. Moreover, modeling and even static approaches often must rest on a basis of numerous un-examined assumptions about the behavior of hardware systems and low-level system behavior (e.g., what operating system calls actually return). Only actual concrete inputs—tests—can be executed in a completely realistic environment, including real hardware. Only tests can satisfy regulatory requirements on code coverage such as those imposed on civilian avionics by DO-178B and its successors [75]. Furthermore, only testing can prove faults are not spurious, the result of imprecise abstraction or weak assumptions. In sum, dynamic analysis can detect otherwise invisible faults, and confirm the reality of statically detected faults.

Most developers do not know how to use symbolic execution tools; developers seldom even know how to use less challenging tools such as gray-box fuzzers, even relatively push-button ones such as AFL [91]. Even those developers whose primary focus is critical security infrastructure such as OpenSSL are often not users, much less expert users, of such tools. Furthermore, different tools find different faults, have different scalability limitations, and even have different show-stopping bugs that prevent them from being applied to specific testing problems. DeepState [35, 36] addresses these problems. First, developers *do*, usually, know how to use unit testing frameworks, such as JUnit [32] or Google Test [1]. DeepState makes it possible to write parameterized unit tests [84] in a GoogleTest-like framework, and automatically produce tests using symbolic execution tools [78, 80, 77, 67], or fuzzers like AFL [91] or libFuzzer [76]. DeepState targets the same space as property-based testing tools such as QuickCheck [23], ScalaCheck [69], Hypothesis [66], and TSTL [40, 52], but with harnesses that look like C/C++ unit tests. DeepState is, most importantly, the first tool to provide a front-end that can make use of a growing variety of back-ends for test generation. Developers who write tests using DeepState can expect that DeepState will let them, without rewriting their tests, make use of new symbolic execution or fuzzing advances. The harness/test definition remains the same, but the method(s) used to generate tests may change over time. In contrast, most property-based tools only provide random testing, and symbolic execution based approaches such as Pex [83, 85] or KLEE [17], while similar on the surface in some ways, have a single back-end for test generation. DeepState’s flexibility is evident: in the last year, DeepState added support for the Eclipser [22], Angora [19], and Honggfuzz [2] fuzzers, as well as an ensemble [21] mode supporting the use of multiple fuzzers at once [18].

DeepState has already been used to test (and find bugs in) a user-mode ext3-like file system developed at the University of Toronto [81, 37], and is being considered as a basis for automatic testing for in NASA’s open source flight software framework FPrime [13, 68]. Although only released in early 2018, DeepState is already one of the most popular property-based testing and fuzzing projects on GitHub, and has been used internally by both startups and well-established companies, and in security audits by Trail of Bits. There have even been informal discussions of integrating DeepState, once matured, into a future release of the GoogleTest [1] platform. PI Groce is at present the lead developer for DeepState.

### 3 Research Plan

#### 3.1 DeepState and Automated Test Generation

Applying DeepState to real embedded systems requires us to meet many challenges:

1. The *specification* of correctness must be translated into an executable form. To some extent, the existence of the E-ACSL executable subset of ACSL, and libraries for runtime checking of properties satisfies this condition. DeepState can support any C/C++ executable method of checking for correctness. However, some executable specifications need to be modified to be efficiently handled when the DeepState back-end is a symbolic execution tool. DeepState’s nature as a test generation tool means that it supports constructs, such as Minimum, Maximum, and Pump, not usually available in executable specifications. Tailoring E-ACSL usage for DeepState therefore requires a custom effort, including extending the semantics of executable specifications and optimizing the implementation for symbolic execution and fuzzing. Finally, because our domain critically involves timing, we need to implement DeepState handling of (and E-ACSL representations for) deadlines, and specification of function-level deadlines including arbitrary, specified, “runtimes” for code that operates via simulation rather than real hardware (or in symbolic execution). Similar, but in some ways even more complex, challenges are posed by the ubiquity of *interrupts* in embedded code, a problem addressed by very little previous work in fuzzing [79].
2. The *assumptions* that control which tests are considered valid must be translated in the same way; normally, E-ACSL simply translates these into further assertions (as pre-conditions to check at runtime), but in DeepState, we need to distinguish between ASSUME failures (invalid tests) and ASSERT failures (bugs).
3. The inputs to a function must be translated into code controlling the input values that DeepState provides, including ranges and types. When input types are simple, this process is straightforward; however, when functions take, e.g., arbitrarily sized arrays, linked lists, or other complex structures, this becomes a problem of constructing a test harness that (1) makes fuzzing and symbolic execution scalable but (2) uses large enough structures to expose subtle bugs. Moreover, because DeepState supports strategies for input generation, such as forking concrete states for values too complex for symbolic execution using the Pump construct, the translation must determine when such strategies are appropriate, and apply them.
4. In many cases, checking a single function may not be an effective way to detect faults; only a sequence of API calls can expose a problem in a system (e.g., that a function produce a state that causes another function to violate an invariant). ACSL annotations provide enough information for a fully-automated translation to a harness enabling dynamic analysis in the case of proving properties of a single function, but not for groups of functions. Moreover, even in cases where the violation of a specification can, in theory, be discovered without calling multiple functions, the state space may be too large to explore with a fuzzer or symbolic execution tool. In such cases, exploring only states produced by valid call sequences has two benefits: first, the space itself may be much smaller, and easier to explore, than the full set of possible input values. Second, errors in this part of the input space are more important. Even if a precondition is not sufficiently restrictive to guarantee correct behavior, if the “bad” inputs are never, in practice, generated by the functions that modify system state, the fault may not matter. In cases where constructing a sufficiently exact precondition is difficult for engineers, such “in-use” verification may be the only avenue to system assurance; proof is impossible without a restrictive enough precondition, and dynamic methods may scale very poorly to, e.g., a large unstructured byte buffer such as a hash table. We propose to let users annotate (in an extension of ACSL) sets of functions to be tested as an

```

void update_state(struct state_t *s, uint64_t bv) {
    ASSUME(valid_state(s));
    ASSUME(valid_bv(bv));
    ...
}
void process_both_sensor_readings(struct state_t *s) {
    ASSUME(valid_state(s));
    unit64_t s1_bv = acquire_s1(), s2_bv = acquire_s2();
    update_state(s, s1_bv); update_state(s, s2_bv);
}
void process_one_sensor_reading(struct state_t *s) {
    ASSUME(valid_state(s));
    unit64_t s1_bv = acquire_s1();
    update_state(s, s1_bv);
}

struct state_t *NewState() {
    return DeepState_Malloc(sizeof(struct state_t));
}
TEST(SensorReading, UpdateNeverSlow) {
    struct state_t *s = NewState();
    DeepState_Timeout(
        [&]{update_state(s, DeepState_UInt64());},
        MAX_EXPECTED_UPDATE_TIME);
}
TEST(SensorReading, AvoidCrashes) {
    struct state_t *s = NewState();
    for(int i = 0; i < TEST_LENGTH; i++) {
        OneOf(
            [&]{process_both_sensor_readings(s);},
            [&]{process_one_sensor_reading(s);});
    }
}

```

Figure 2: Sensor reading code and DeepState test harness

API-call-sequence group, extending recent work exploring this concept [12, 74]. E.g., annotating a set of file system functions (`mkdir`, `rmdir`, `readdir`, etc.) as a group would enable automatic generation of a DeepState harness to check for sequences violating file system invariants.

5. Finally, DeepState and, in fact, general-purpose fuzzers such as AFL, have, to date, been exclusively (to our knowledge) used in what might be deemed conventional environments. As recently noted, “the tight coupling between hardware and firmware and the diversity found in embedded systems makes it hard to perform dynamic analysis on firmware” and existing mainstream fuzzing tools offer almost no support to embedded developers for simulation and emulation [26].

These goals require significant advances in three areas of dynamic analysis: first, a complete and principled approach to the problem of handling pre-conditions/assumption semantics, and second, an investigation of how to let fuzzers take advantage of the significant additional structure provided by property-based testing, including such assumptions. Consider the code in Figure 2. This defines two different tests of software that reads sensor values and incorporates them into a system state. The two tests check two different properties: `UpdateNeverSlow` ensures that updating the sensor is never too slow. It is checked, potentially, over *all* valid inputs, not just ones produced by the actual sensor reading code in `acquire_s1` and `acquire_s2`. The second test, `AvoidCrashes` starts the system up in some valid state, and repeatedly either reads both sensors or only sensor one. There is no explicit property, only the expectation that the system will not crash; tests can be executed using LLVM sanitizers to check for integer overflow and other undefined behavior. Generating such harnesses automatically from ACSL specifications is a significant challenge, but our research agenda also includes solving problems that would appear even for manual harnesses. For example, what is the proper semantics of the `ASSUME` in `update_state`? It depends on the test. In `UpdateNeverSlow`, a fuzzer will often generate an input value that violates the (possibly complex) requirements on valid states and sensor readings. These invalid inputs should not be flagged as bugs (the default behavior of E-ACSL), but instead the test should be abandoned without indicating that it failed. However, in `AvoidCrashes`, since we are not directly generating state values, that is, `update_state` is not an *entry point* for the test, assumption violations should result in failed tests. We aim to synthesize code to make assumptions automatically take on the proper semantics during test execution (including symbolic execution using constraint solvers).

This point about preconditions/ASSUME brings up a second point. Preconditions, when they have an `ASSUME` semantics, are fundamentally different than other branches in code. A fuzzer will attempt to explore the behavior of branches in `valid_state` and `valid_bv` just as it explores branches in `update_state` or `acquire`. However, it is often possible to enumerate a vast number of paths that differentiate only invalid inputs, and so produce very little real testing. A classic example is “testing” a file system by producing a huge variety of unmountable file system images, rather than actually executing POSIX operations [41, 45]. DeepState knows which branches are pre-conditions, and so can help avoid this problem. In some fuzzers, this



means prioritizing inputs to mutate based on whether they execute any code other than validity checks; but in fuzzers, such as Angora [19] and Eclipser [22], that use lightweight constraint-solving to cover branches, the process can be more sophisticated. We have begun discussions with the Eclipser team, and they confirm that identifying precondition code and devising suitable heuristics to handle it (e.g., never solve for a negation of a passed check) should improve performance. Fuzzing of individual functions or sets of functions is a highly promising area: most fuzzing is applied at the whole-program level, where input generation can simply be too hard. By focusing on a middle-ground between unit testing and whole-program fuzzing—using fuzzer technology to drive property-driven testing—the problem is made tractable. Prioritizing paths that include more than just input validation is an explicit goal of, e.g., AFLFast [14], but it must work with an implicit definition based on path frequencies, while we have access to ground truth. Given the complexity of state validity checks, there may be hard-to-reach—but uninteresting—ways to create invalid input; AFLFast will *prioritize* such paths, while we will (correctly) avoid them.

This effort also connects to a second fuzzing research thrust: making specification elements that do not correspond to simple code coverage visible to a fuzzer. In this example, consider the `DeepState.Timeout` check (note that this itself is functionality we will develop as part of handling timing constraints in FRAMA-C and DeepState). Unless we break down the timing analysis explicitly using a set of conditional branches, coverage-driven fuzzers cannot distinguish an execution that is very slow (close to violating the constraint) from one that has the minimum execution time possible. We propose to make timing of such specified events visible to a fuzzer, by modifying coverage bit-vectors to incorporate bucketing of execution time. Once we add such novel coverage measures, and introduce distinctions between coverage classes (as with preconditions), we will research how to balance competing priorities in more complex notions of coverage. In addition to implicit execution properties such as timing, this can apply to coverage of data structures, for fuzzing data-driven code such as machine-learning algorithms, where much behavior is implicit—e.g., the route taken through a forest of decision trees. In general we aim to extend the work [14, 65, 72, 93, 7], that prioritizes certain program paths in an intelligent way, by exploiting our extended ACSL/E-ACSL.

Finally, these elements must be tied to the problem of applying fuzzing and related methods in embedded-relevant execution environments. We plan to investigate multiple potential solutions, initially focusing on integrating fuzzing the approach taken by the just-released HALucinator (<https://github.com/embedded-sec/halucinator> tool [26] for virtualizing firmware via the Hardware Abstraction Layer. The embedded context is also likely to add additional notions of coverage and path relevance to those discussed above, ones tied to specific emulation environments.

### 3.2 DeepState and SAT/SMT-Based Bounded Model Checking

While automated test generation by fuzzing or binary-level symbolic execution can be highly effective as a means for finding bugs in code, other approaches are also needed to handle the kinds of code especially common in embedded contexts. In particular, embedded software often includes a large number of functions that perform complex low-level bit operations, especially for interacting with hardware and “parsing” network packets (from traditional wireless or RF-derived signals) communicating in very low-level protocols. Fuzzing or binary symbolic analysis often has trouble finding exact bit-values; it is well known that, e.g., inverting even non-cryptographic hashes is hard for either approach. Direct translation to bounded SAT (from source, not compiled code) on the other hand, often easily handles such input generation problems.

CBMC, the C Bounded Model Checker [58] is a well-known tool that analyzes C programs using a translation to SAT or SMT queries based on a bounded unrolling of loops. CBMC is an actively developed project, and has been used extensively in real-world development for years, including in automotive/embedded code development at Bosch and General Electric [82], in analysis of Amazon Web Services infrastructure [27], and in the analysis of flight software systems at NASA’s Jet Propulsion Laboratory [45]. Using CBMC requires writing custom test harnesses using CBMC’s API for expressing nondeterminism, and running the tool with a specified bound on loop executions, in addition to other complex configuration options.

We propose to allow CBMC to be used as a backend for verification by DeepState, with a seamless interface, just as DeepState currently supports symbolic analysis engines such as angr and Manticore. It is

notoriously hard to guess when a SAT/SMT based approach to code analysis will work well and when it will fail to scale; using a DeepState harness will allow users to try CBMC at “no cost.”

Moreover, because choosing loop unwinding bounds imposes a serious burden on embedded engineers, we will investigate their automatic determinations. One approach is to instrument fuzzer or symbolic-execution engine generated tests to record iterations of loops, and then use the maximum bound observed. Additionally, for small functions (the most likely targets for DeepState-CBMC: complex but compact bit-manipulation code), the mutation-based approach proposed by Groce et. al [48] may work. Finally, in some cases CBMC may be able to find interesting bugs for cases where the loop unrollings are limited, but cannot scale to larger depth limits. Using the same instrumentation that we use to estimate loop bounds, we will use the ability to guide fuzzers by alternative “coverage” to focus fuzzer runs on executions with more loop iterations than the bound explored by CBMC. This will offer engineers a true partnership between verification methods.

### 3.3 DeepState and Explicit-State Model Checking

Just as some functions are best analyzed using bounded model checking, some dynamic analysis problems are best handled by explicit-state model checking that actually executes C code, like a fuzzer, but with the capability to store states and backtrack, in order to exhaustively explore a state space, using either actual comparison of stored states or comparison of abstractions of states to guide exploration. This approach is particularly attractive for exploring sequences of API calls; this kind of test generation was used in efforts that uncovered dozens of errors in file systems at NASA/JPL [45].

The SPIN model checker [55] offers execution of C code with backtracking [53, 54]. DeepState’s `OneOf` construct has a semantics that can be matched with the SPIN nondeterministic choice, which in part inspired the DeepState construct [39, 38]. However, integrating SPIN as a back-end for DeepState is even more challenging than integrating CBMC. With CBMC, it is plausible that the mapping from DeepState to CBMC semantics can be performed entirely in terms of changing included headers so that CBMC-specific constructs have differing implementations (but not semantics); SPIN however executes C code in the context of a PROMELA model, which requires rewriting a DeepState model to embed test choices inside SPIN’s constructs. This also means “lifting” DeepState API calls to the PROMELA level outside the C code, and bridging between nondeterminism visible to SPIN and determinism within C code; PI Groce’s previous work [39] can serve as a foundation. A more fundamental problem is that while CBMC and DeepState can share a semantics for, e.g., `DeepState_Int64()`, a PROMELA model with a branching factor of, e.g.,  $2^{64}$  will not work. Possible solutions range from using results from fuzzing to choose a limited range, to translating “flat” bit-value selection into a sequence of choices with a larger range but bias towards certain values, to using SPIN to control a seed and deterministically choosing random values [39], a hybrid fuzzing/explicit-state model checking approach. All of these approaches have potential problems (e.g., still significant state-space explosion), and all may be needed to handle different verification problems.

### 3.4 Generation of Timed Automata Model Skeletons

As noted above, one of our core assumptions is that timed automata can model the underlying protocols in many embedded systems. However, analysis of timed automata models using UPPAAL [10] and PRISM [59] is at present a skill only a small number of embedded engineers have mastered. In order to encourage more engineers to make use of these powerful formalisms, we will also develop a method to extract timed automata model skeletons for both of these model checkers from annotated C code.

### 3.5 Case Studies

The above briefly introduces a number of problems that we know in advance must be dealt with in order to enable a pathway for combining formal, static, and dynamic analysis. At heart, however, we aim to allow *case studies* to prioritize our efforts, and are certain that other challenges will arise during these efforts. The studies informing this research is the embedded software of wireless sensor nodes used in the Southwest Experimental Garden Array (SEGA) [24, 33, 9] and of wireless sensor nodes and mobile robots in the Distributed Sensing & Computing Over Sparse Environments (DISCOVER) Platform.

### 3.5.1 Communication Protocol for Wireless Sensor Nodes in SEGA

**Overview:** SEGA is a large collection of operational wireless sensor/actuator networks for monitoring and control of ecological systems, located at 17 sites in the states of Arizona and California. Currently, SEGA consists of 138 wireless nodes and is planned to expand to a total of 154 nodes at 21 sites in the coming years. As a genetics-based climate change research platform, SEGA allows scientists to quantify the ecological and evolutionary responses of species to changing climate conditions. Multiple long-term and large-scale scientific experiments are conducted at SEGA sites. The SEGA project was led by NAU, and the group of co-PI Flikkema developed and are maintaining the wireless nodes, including their embedded software. The SEGA nodes use a multi-processor architecture, in which a central processor provides OS-level services while plug-in satellite processors handle transducer sampling, actuation, and related computational tasks. In addition to allowing true parallelism, this architecture enables hardware-level improvements in energy efficiency, since each satellite can be optimized for its specific task. ~~More practically, it admits the rapid implementation of highly heterogeneous nodes that incorporate a wide range of sensing and actuation capabilities.~~ The nodes synchronously interact with neighbors in a multi-hop, self-organizing/healing network, implemented by a custom communication protocol designed by the group of co-PI Flikkema. The nodes use a custom time-triggered RTOS tightly integrated with a time/frequency-hopped PHY/MAC protocol. This approach minimizes communication energy cost, which dominates the overall energy consumption.

**Challenges:** Because timing is critical and is determined by the embedded system hardware and software, most testing has occurred at the network level, with extensive in-lab testing with small networks and instrumented field tests. However, it has been found in long-term deployments that occasionally the networking fails and nodes become isolated—we think due to a complex set of subtle bugs rooted in different levels of timing abstraction. When such a failure occurs, it often spreads from one node to others, causing nodes to seek to rejoin and expend high levels of energy for radio operation and eventually deplete their energy sources. Eventually, subnets, or sometimes the entire site, are disabled and humans must visit the site to reboot it. Such failures could affect or even destroy (e.g., via over-watering), long-running scientific experiments. ~~Since access to SEGA installations can be difficult, and in the long run many may be located so remotely that it is cost-prohibitive to send humans to address problems, discovering the source of these in-operation faults, identifying other faults, and generally improving the reliability of the system is critical.~~ We aim to use SEGA (in particular the protocol in question and its implementation) as our case study. This will enable us to apply our approach in a practical setting, and ensure that what we produce is actually usable by engineers of real systems. SEGA is an ideal case study for several reasons. First, the above mentioned network problem enables exploring how to design, prove, and test time-critical systems in a way that does no harm: human life is not affected in this application, and data is not lost since all sensed information is logged as a local back-up. On the other hand, reliable operation is important. Finally, this application uses common data structures for task control blocks, and the operating system at each node schedules and dispatches both periodic and pseudo-randomly scheduled tasks. Thus the system is representative of general applications of scheduling and synchronization in time-critical systems written in C.

**Plan:** Following our proposed workflow, we will first annotate the implementation with specifications of correctness properties. We may model the protocol itself as a timed automaton in UPPAAL or PRISM, in order to ensure that there is not a subtle flaw in the protocol itself, and to model our expectations of behavior in the real system (and to better understand needed specifications). Either of these steps may expose the source of the mysterious networking failures. We will use DeepState, driven by harnesses automatically generated by our tools, to generate tests of the implementation components in question, using fuzzing at first, followed by CBMC and SPIN model checking once prototype back-ends are available. ~~For the purpose of verification and testing, the uncertainty inherent in the physical environment and in wireless communication will be modeled by probabilistic timed automata.~~ The above workflow will be conducted by an Embedded System Engineering student, who is familiar with the SEGA IoT system but does not have expertise in software verification and testing, using the software tools developed in this project. Feedback from the engineer in this

case study will inform us how to develop and improve the theory and tools for practical usages by non-expert users in real applications.

### 3.5.2 Embedded Software of Wireless Sensor Nodes and Robots in DISCOVER

**Overview:** DISCOVER is a cyberinfrastructure testbed for remote, rural, and sparsely populated areas. The project is funded by NSF and led by NAU, whose team includes co-PI Flikkema (PI of DISCOVER) and co-PI Nghiem (co-PI of DISCOVER in charge of robotics). DISCOVER consists of a fabric of highly configurable Internet-of-Things (IoT) sensor nodes, autonomous and highly capable terrestrial robots and drones, and a heterogeneous wireless network. DISCOVER sites will be located at the campuses of NAU, Navajo Technical University, and Clemson University, as well as several remote sites. The platform will enable focused research in many domains, including data science and machine learning, heterogeneous networked services, distributed computing and AI, control, autonomous robots, and in-network computation, among many others. We will use DISCOVER for two case studies: one on embedded software for wireless sensor nodes and the other on distributed coordination in multi-robot systems. Coordinated operation of multiple autonomous robots has many important real-world applications [16, 90], e.g., in rescue, security, or disaster response missions. In such applications, each robot is autonomous but has the capability to coordinate efficiently and safely with other robots to complete a shared mission, often in a distributed manner. Such coordination is essential in real-world applications where the environment is constantly and unexpectedly changing. One of the most critical challenges of this application is to guarantee the safety of a coordination plan, which is typically implemented in C code on the embedded computers of the robots and usually involves wireless inter-robot communication, sensing, and actuation.

**Challenges:** As a community research platform, DISCOVER will allow users, who are researchers in relevant field domains, to develop software code and experiments for the DISCOVER stationary nodes (i.e., sensor nodes) and mobile nodes (i.e., terrestrial robots and drones). A critical step of the process supported by DISCOVER is automatic verification and testing of the embedded code submitted by users for live experiments. We expect that submitted code is developed by researchers who are not trained in computer science and who do not usually apply best practices in software engineering. We also expect that submitted code will have a wide spectrum of code quality and may be malicious, either by chance or intentionally. Automatic functional testing of user code will therefore be of critical importance for the operation and sustainability of DISCOVER. Another challenge is the fact that the code to be tested and verified is for embedded systems that have highly complex physical dynamics (in the case of robots) and interactions with the physical world and with other physical systems. Such physical aspects cannot be easily described in code for the purpose of software verification and testing. Therefore, sophisticated software-based and hardware-in-the-loop simulations, including embedded hardware emulators and robot simulators, are necessary, for which several options will be developed by the DISCOVER team.

**Plan:** For the wireless sensor nodes, where a major part of their operation is related to data storage and communication, our planned approach will be similar to that of the SEGA case study. For the robotic nodes, we will focus on multi-robot coordination since other user errors, such as unauthorized hardware access and unauthorized maneuvers of robots, can be prevented or mitigated through a combination of techniques such as containerization, access rights, and geofencing. Our approach will be briefly described below. First, we will model a coordination plan for multiple robots as a (potentially very complex) network of timed automata. Performance specifications will be expressed in temporal logics, e.g., the Signal Temporal Logic (STL) [30], and checked against the model using verification and testing tools such as UPPAAL or S-TaLiRo [6]. While we do not expect actual user code to be accompanied by formal models, in our case study, this step ensures that the original coordination plan has no subtle flaws, and helps us determine properties that need formulation at the implementation level. An implementation of the algorithm in C code, distributed among the robots, will be developed by a robotics/control student. The implementation will be annotated with a specification in our extended ACSL/E-ACSL. We will then use DeepState harnesses to generate tests of the implementation components using fuzzing, symbolic execution, and both bounded SAT/SMT based

and explicit-state model checking. Finally, we will determine if a timed automata skeleton extracted from the implementation code corresponds to and would help create a full specification such as we developed before beginning implementation. The very different nature and complexity of this study, compared to stationary sensor nodes, will ensure that our methods and tools work in a variety of kinds of real systems. To overcome the challenge stemming from the complex physical dynamics and interactions of the robots, we will utilize a sophisticated robot simulation environment, based on the Robot Operating System (ROS) [71], with a rich set of predefined scenarios, developed by the DISCOVER team (specifically by the group of co-PI Nghiem). An interface between the robot simulation software and the tools developed in this project will be created to enable seamless verification and testing of the robotic code.

### 3.6 Work Plan

The project will be organized into two phases, described by work packages. In the first phase, T3.1 will be conducted along with T1.1 and will inform the development in these tasks. In the second phase, the focus will be on the application of tools in T1.2 in tandem with T2. Tasks related to case studies (tasks T4.1, and T4.2), whose results and feedback will help refine the developed tools will be especially emphasized in the final phases of the project. The timeline of the tasks will be structured as shown in Figure 3.

**Work Package 1 (WP1):** This work package concerns the development of and use of ACSL and E-ACSL extensions for use in embedded system implementation code.

- T1.1: This task will consider needed extensions for handling real-world embedded systems. In particular, there will be a focus on a study of the formal semantics of timed automaton networks defined in UPPAAL and PRISM, to determine the extent to which shared semantics can be assigned making it possible to carry implementation annotations into such formal models (see T4.2) and, in theory, translate properties from such models into implementation annotations. As such, there will be close collaboration and iterative design steps between this task and the other work packages.

- T1.2: This task will take feedback from applications of tools to generate tests and proofs (T2) into account, to add annotations that are focused on heuristic guidance for tools, not correctness per se.

One Ph.D. student will conduct this work, which will last for the entire duration of the project.

**Evaluation:** Evaluation of WP1 will be determined by ability of embedded engineers to agree that the key properties, including those related to timed automata models, to be checked are (1) all representable by the annotations (2) easy to construct (given the basic difficulty of systems specification) (3) easy to read when produced by others and (4) maintainable after introduction.

**Work Package 2 (WP2):** This work package covers methods and tools to automatically translate ACSL/E-ACSL-annotated code in into a DeepState test harness (Section 3.1), the development of DeepState back-ends for CBMC and SPIN, with appropriate mechanisms to ease the use of these tools, and improvements to fuzzers to improve test generation:

- T2.1: This task will optimize the implementation of symbolic execution and fuzzing in DeepState, so that ACSL/E-ACSL annotations and extensions from WP1 can be used effectively.
- T2.2: This task will develop DeepState back-ends for CBMC and SPIN, inform annotations needed to handle loop bounds, memory tracking and matching, and make use of feedback from fuzzing.

The execution of this work package will also span the entire duration of the project. Because the tasks in this package are also based on developing verification and test generation tools (thus formal methods expertise), the same Ph.D. student will work on WP1 and WP2. We separate the WPs primarily to emphasize that specification extensions and tool support are somewhat orthogonal concerns, and evaluated differently.

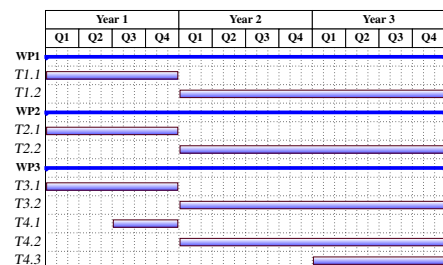


Figure 3: Project schedule.

**Evaluation:** Evaluation of WP2 will be determined by the application of DeepState harnesses to generate tests for realistic systems. We will use benchmarks and simple examples to some extent, but primarily rely on our connection to case studies. In the case of test generation, in addition to faults detected, we will use code coverage and other standard benchmarks [57]. We expect to publish papers on advances in fuzzing technology and fundamental issues arising from the CBMC and SPIN back-ends with respect to handling loop bounds and memory tracking/matching.

**Work Package 3 (WP3):** This work package will focus on the field applications described in Section 3.5, as both a way to inform the methodology and tool developments in the other work packages and case studies to validate our methods and tools. WP3 includes the following case studies:

**Wireless sensor network (WSN) case studies on SEGA and DISCOVER.** This is divided into two tasks:

- T3.1: In this task, the wireless sensor node systems will be studied thoroughly to extract the key requirements and characteristics of the embedded system implementations. Timed automaton models of the communication protocol in each system, at different levels of abstraction, may be developed and formally verified in UPPAAL and/or PRISM, to inform task T1.1. The system information and models resulting from this task will inform the semantics design and method developments in WP1 and WP2. As time allows we will extend this work to include sensing elements.
- T3.2: This task will apply the tools developed in WP1 and WP2 to the WSN systems, to detect and fix bugs in the communication protocol implementations; in particular, the bugs that cause the intermittent failures in SEGA. It will also provide feedback to the other work packages to refine and improve our tools.

**Multi-robot system case study on DISCOVER.** This study is divided into three tasks:

- T4.1: In this task, a standard multi-robot coordination algorithm will be modeled as a network of timed automata. Using our insights into the robotics application, we will express its performance specifications, particularly its safety requirements, in temporal logics and formally verify or test them in tools like UPPAAL, PRISM, or S-TaLiRo. This task will extend the developed semantics and methods to applications beyond communication protocols, to identify further needed runtime extensions and semantic connections between timed automata theory, implementation annotations, and runtime checks.
- T4.2: This task will apply the tools developed in WP1 and WP2, and the robot simulation environment of the DISCOVER platform, to the coordinated multi-robot system, in order to validate the implementation code and detect and fix possible bugs. It will also provide feedback to the other work packages to refine and improve the tools developed in this project.
- T4.3: This task will aim to use the work on the robotics effort to prototype a mapping from implementation code annotations in ACSL/E-ACSL and extensions into skeletons of models in timed automata formalisms.

As the tasks in this work package are conducted in tandem with WP1 and WP2, to form a feedback loop with the developments in other work packages, it will last for the entire duration of the project. We expect that groups of undergraduate students, in collaboration with an embedded systems Ph.D. student and the Ph.D. students in WP1 and WP2, will perform the work. Close collaboration with the DISCOVER team, led by Dr. Flikkema and Dr. Nghiem, is expected.

**Evaluation:** In essence, this task is the evaluation aspect of our project, which forms one of the major thrusts of the project. The successful application of WP1 and WP2 tools to the case studies is essentially the driving factor in determining our success in the project. The measure of success is: (1) faults detected and corrected; (2) functionality proven correct using CBMC, symbolic execution engines, or SPIN; (3) coverage and other measures of generated tests; and (4) reported usability and value by embedded systems engineers, particularly students. For T4.3, the evaluation will be based on a formal comparison of the extracted skeleton with full timed automata models developed by embedded systems experts. The degree of success will be estimated based on the correspondence with a real model.

## 4 Contributions to Formal Methods and the Field

The contributions to formal methods proposed include:



- Fundamental contributions to integrating formal specification languages developed for use in static analysis and theorem proving with dynamic analysis, producing a common semantics for formal, static, and dynamic checking of correctness. Handling of timing and interrupts are notable examples of problems to be addressed in this effort.
- Enhanced ability of fuzzing and other test generation methods to make use of information from formal specifications, and integrate feedback about, e.g., specification coverage into test generation heuristics.
- Common semantics and a framework for fuzzing, symbolic execution, SAT/SMT-based bounded model checking, and explicit-state model checking.
- Approaches to using feedback from fuzzing to guide bounded or explicit-state model checking.
- Translations from implementation-level specification to (probabilistic) timed automata models.

The contributions to the field include:

**Truong: Update!!!**

- New development and design methods that focus on implementation-level specification of correctness of code as a guiding principle for embedded systems.
- Tactics and strategies for incorporating the above methods into legacy efforts, where existing code bases require additional specification and annotation.
- Best-practices for using formal, static, and dynamic tools in debugging legacy systems problems.

Because of our focus on practical integration and extension of existing tools and methods to real-world embedded systems, our *evaluation* of the degree to which these contributions have been realized is described in the work plan above, integrated with description of case study efforts.

## 5 Related Work

A fundamental goal of this project is to reduce both user effort and the opportunity for user effort by allowing minimizing (ideally to one) the number of times a user must specify an aspect of system correctness. The principle that important information should have a “single point of truth” is widely accepted in software engineering, even in such foundational early advances as avoiding repeated magic numbers by the use of named constants. Such a principle can be extended to specification and definition of test harnesses. Early work emphasizing this goal of both reducing work and chance of error in specification and test generation included the effort by Groce and Joshi to use a single harness for both model-checking and random testing, in the verification of the Mars Science Laboratory’s file system [39, 41, 45]. In later work, Groce and Erwig extended this idea to propose development of a single language with a unified semantics for a wide variety of dynamic test generation tools [38]; this approach is essentially realized in the DeepState [35] system. Indeed, FRAMA-C and ACSL [8] and DeepState are both arguably limited instantiations of this goal: providing a single language, interface, and semantics that is applied to a variety of methods (static or dynamic) for checking that a specification holds. This project aims to further extend this goal by extending it to include a formal timed-automata model and to connect the primarily static and dynamic approaches.

The implementation and verification of distributed systems, and code extraction from automata modeling in the proof assistant COQ [86, 88, 70] is a topic of some previous work. Such proposals require that the developers master COQ, and start from the modeling activity to generate code. They are therefore not applicable in the context of the verification of legacy embedded C code, the common case in the real world.

Testing real-time systems modeled by networks of timed automata was investigated by the authors of the tool UPPAAL [51, 50, 61] and implemented in the tools UPPAAL-TRON (<http://people.cs.aau.dk/~marius/tron/index.html>) and UPPAAL-COVER (<http://www.hessel.nu/CoVer/index.php>). These tools generate tests, either offline or online, for conformance testing of a real-time system with respect to its model and an environment model, both as timed automaton networks. In both cases, the real-time system is considered a black-box with an input/output interface through which the test generator or monitor can change the system inputs and observe the system outputs. The actual implementation code is not considered and is in fact hidden from the testing tools. While this approach is general, it has several drawbacks. It requires a centralized input/output interface accessible to the testing tools. Such an interface is not always available in

all systems, especially in large-scale distributed systems like the sensor/actuator networks considered in our case study. Furthermore, by considering only the (timed) input/output behavior of a system, this approach may not be able to test internal system behaviors and therefore miss opportunities for a better test coverage.

## 6 Broader Impacts

**Improving Software System Reliability:** A key element of our approach is to focus on realistically deployable techniques. We aim for early integration with NASA’s FPrime [13, 68] open source flight software architecture and platform; PI Groce is already in discussion with engineers at NASA’s Jet Propulsion Laboratory, and engaged in producing tests for the FPrime autocoder using DeepState. This integration will allow our methods to be applied to CubeSat missions (and other flight software systems), leading to improved reliability for low-budget space-based scientific efforts. We expect, in the long run, that our approaches will lead to more reliable and robust development in many embedded and cyberphysical systems domains, and contribute to a more secure and reliable Internet of Things.

**Education and Outreach:** The proposed research yields several opportunities for enhancing CS education, recruiting new CS majors, and retaining CS students, particularly members of underrepresented groups. In addition to the activities discussed at length in the Broadening Participation in Computing plan, PI Groce will work with the NAU Student ACM Chapter to present a series of “excursions in testing” that introduce automated testing to students, using DeepState to find bugs in real world code, including code from media player libraries; in advanced meetings, integrating DeepState with FRAMA-C will be demonstrated as well. The work of Guzdial [49] has shown that media computation is a potentially effective way to both recruit and retain female and underrepresented students in computer science. Groce is also teaching a class on automated testing of embedded systems to graduate and undergraduate students. Co-PI Nghiem has developed a new course at NAU on autonomous vehicles, based on the F1/10 platform (funded by NSF). To prepare students in addressing one of the greatest challenges of autonomous driving, namely safety guarantee, future offerings of the course will incorporate the methods and tools developed in this project to teach students about safety, verification, and testing.

**Broadening Participation in Computing (BPC):** The goal of the BPC component of this project is to *increase the number of females who are involved or choose careers in computing, at NAU and in the local community of Flagstaff, Arizona.* Our plan carefully integrates active learning experiences designed for female students at both the undergraduate and middle school/junior high levels. **Undergraduate Education Experience -** We will reach female students in three degree programs at the 2nd-year level: Computer Science, Computer Engineering, and Electrical Engineering. In CS, we will target CS 200 Introduction to Computer Organization; in EE and CE, we will target EE 215 Microprocessors. We will integrate a new project in which teams of female (and possibly male, due to the current lack of females in EE, CE, and CS) students imagine and create exciting and meaningful one-day active learning experiences and projects for female student teams in grades 7-9. In both courses, we will bring in expert female speakers to facilitate development of students’ understanding how to design these projects so they are marker events in the students’ lives. We will also explicitly address increasing the awareness of the challenges faced by females of all ages in STEM careers. **Outreach to grades 7-9 -** As noted above, the undergraduate teams will develop active learning and design project “Build Events” for girls in grades 7-9. We will recruit female undergraduates who have taken CS 200/EE 215 to become mentors in the one-day events for the grade 7-9 students. We will schedule these events as part of the annual Flagstaff Festival of Science, and plan them for Saturdays to avoid conflicts with school schedules, maximizing participation. The Flagstaff Festival of Science ([www.scifest.org](http://www.scifest.org)), now in its 31st year and enjoying wide financial and participatory support in the community, holds over 100 events for all ages over a 10-day period in the Fall, and is an ideal venue in which to participate. **Facilities and Support -** By scheduling the grade 7-9 Build Events on Saturdays, we will be able to use the educational laboratories of the School of Informatics, Computing & Cyber Systems (SICCS) for the Flagstaff Festival of Science events. We have requested \$2,000 for each in years 2 and 3 for materials (primarily embedded development boards) for these experiences.



## 7 Results From Prior NSF Support

**PI Groce:** The most relevant prior NSF support for PI Groce is CCF-1217824, “Diversity and Feedback in Random Testing for Systems Software,” with a total budget of \$491,280 from 9/2012 until 9/2015, a collaborative proposal with John Regehr of the University of Utah. **Intellectual Merit:** The results of CCF-1217824 included a number of advances to practical automated generation and use of tests, a key focus of this proposal as well. E.g., an approach to creating “quick tests” from a test suite by minimizing each test with respect to its code coverage [44], won the Best Paper award at the 2014 International Conference on Software Testing. CCF-1217824 produced a general set of results focused on making automated random testing usable by practitioners, and using symbolic execution on larger, realistic software. Publications resulting from this grant were numerous [43, 20, 92, 44, 42, 3, 47, 52, 46, 4]. **Broader Impact:** The results of CCF-1217824 have been used in teaching software engineering classes. Work from the project contributed to the discovery of previously unknown faults in important software systems, including LLVM and GCC, and is widely used in compiler testing [62, 60, 29, 63]. Tools and data sets from CCF-1217824 are available via GitHub in multiple repositories and projects (TSTL, Csmith, CReduce, etc.).

**Co-PI Flikkema and co-PI Nghiem** are PI and co-PI, respectively, on the Distributed Sensing & Computing Over Sparse Environments (DISCOVER) Platform funded by an NSF CCRI grant (2120485), with a total budget of \$1,366,513 from 10/2021 until 9/2024. **Intellectual Merit:** DISCOVER is a cyberinfrastructure testbed for remote, rural, and sparsely populated areas, consisting of a fabric of highly configurable and fixed and mobile Internet-of-Things nodes and a heterogeneous wireless network. It will enable focused research on new breeds of algorithms that address a range of challenges around prioritization and optimization of computation and communication in remote, less populous and rural areas. **Broader Impact:** DISCOVER will provide a research platform for investigation of distributed computing, networking, security, control and coordination solutions in a heterogeneous configurable cyber-physical system infrastructure that will provide critical services for areas and populations at increasing risk of being underserved. The education and outreach impacts of this project include training and research opportunities for undergraduate students, engaging underrepresented minority students, and developing hands-on research experiments for K-12 students.

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