

Condition Monitoring of Power Electronic Systems Through Data Analysis of Measurement Signals and Control Output Variables

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Abstract—A major disadvantage of existing condition monitoring methods is the need for additional sensors and measuring equipment. In this work, this disadvantage is eliminated by completely avoiding additional hardware. Instead, software-based methods from the field of machine learning are used. Therefore, measurement signals and control output variables are utilized, which are acquired and processed in any power electronic system for the purpose of converter control. The publication focuses on two main converter components: power semiconductors and dc-link capacitor. For each component, the aging mechanisms that have been studied in the literature are explained. Based on the aging mechanisms, the degradation indicators are identified. Then, a converter model is built that allows the variation of degradation indicators in order to analyze their effects on the available dataset. These findings form the basis for mathematical models, which detects future failure mechanisms of this type during converter operation. The test setup must offer the possibility of generating reproducible failure cases in various components with the aid of additional failure equipment. Finally, failure mechanisms are intentionally introduced at the test bench in order to validate the methodology of the developed approach.

Index Terms—Condition monitoring, dc-link capacitor, machine learning, power semiconductors, reliability.

I. INTRODUCTION

POWER electronics is a key technology for sustainable energy generation and environmentally friendly mobility. Power converters are used to transform regeneratively generated energy from wind and sun to the power grid or to transmit electrical energy over long distances with high-voltage direct current transmission. Due to modern power electronics, it is possible to convert energy very efficiently over a wide power range—from a few watts in the power supply of cell phone chargers to many megawatts in the energy sector. Power converters are also a central component of any electric, variable-speed drive system. In industry, electric drive systems play an essential role. Factories are equipped with numerous electrically driven machine tools and industrial drives, which increase the degree of automation of many processes and improve productivity. The increasing share of

renewable energies in power generation, the growing share of electric vehicles in private transport, and the modernization of existing industrial plants are leading to a growing number of power converters. The requirements for power electronics in energy and drive technology are becoming more challenging. In addition to power density, functionality, and energy efficiency, the reliability of power electronic systems is playing a significant role. The reliability of a system is the probability that an item will perform its intended functions for a specified time interval under specified conditions [1]. In the following, the concept of maintenance-based reliability improvement is presented.

A. Maintenance-Based Increase in Reliability

One way to increase the reliability of a system is to use maintenance, which is performed during the operational phase. In maintenance-based reliability, we distinguish between preventive and predictive maintenance. In the former, maintenance is performed at fixed time intervals. Often, these time intervals are based on the experience of plant experts who estimate the natural lifetime of a component. In predictive maintenance, the time for maintenance is based on the condition of the asset. This requires knowledge about the condition of the system, which condition monitoring is intended to provide. Condition monitoring is a monitoring concept that aims to detect the condition of a system during operation and, thus, provide early information for necessary repair and maintenance work. The information provided by condition monitoring enables the selection of optimal maintenance intervals and the reduction of downtimes of the system. The present publication is in this subject area.

B. State of the Art

There are three principal approaches of condition monitoring of power converters. The approaches are illustrated here based on the component power semiconductor devices. They can also be applied to other components of the power converter system.

1) *Monitoring of Degradation Indicators*: On the one hand, degradation indicators can be monitored. Degradation indicators provide information about the condition of the converter. A degradation indicator can be captured using both direct and indirect methods. Direct methods make use of a measurement circuit, whereas indirect methods use model estimations. Usually, both methods make use of additional measurement equipment. The following are some examples

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of this approach, which utilizes various degradation indicators. In [8], a measurement circuit was developed, which measures the collector-emitter voltage of the insulated-gate bipolar transistor (IGBT) in the ON state in order to detect the aging mechanism bond wire liftoff. In [7], a method is presented to detect the aging mechanisms solder fatigue and bond wire liftoff by online monitoring of the two degradation indicators: thermal resistance between junction and heatsink R_{th} and differential resistance of the collector-emitter path r_{CE} . The parameters are estimated by an indirect method using a measurement circuit. In [22], the chip temperature is estimated using an analog measurement circuit that evaluates the turn-off time of the IGBT with the aim of detecting wear-related aging mechanisms. Additionally to the aforementioned, the contamination of the cooling system is investigated in [23]. Therefore, low-frequency power losses are applied to the IGBT for a short time during operation. Then, the temperature cycles are determined and the chip temperatures are calculated using a thermal model. With this, the maximum and minimum values of the chip temperature are evaluated. An increase in the maximum temperature indicates the aging mechanism solder fatigue and an increase in the minimum temperature indicates the aging mechanism contamination of the cooling system [23].

2) *Aging-Based Modeling*: Another approach is model-based aging prediction. This approach models a specific aging mechanism that leads to converter failure. Therefore, detailed knowledge of the aging process is required. For example, the aging mechanism loss of blocking capability due to increased leakage currents because of humidity can be modeled using thermomechanical and electrochemical models [24]. In order to estimate the remaining lifetime, the load cycles are counted during converter operation. This usually acts as an input variable for the developed aging models.

3) *Software-Based Methods*: A major disadvantage of the two methods presented so far is the need for additional sensors and measuring equipment, which entails additional costs and sources of failure. The software-based approach overcomes this disadvantage and operates without additional hardware. This results not only in a cost advantage but also in a higher reliability of the power converter system due to the removal of additional potential failure sources.

In [26], 224 MOSFET power semiconductors from ten different manufacturers are undergone to a radiation test in the laboratory in order to collect data. Both the static behavior and the dynamic behavior of the devices when they experience thermal and radiological stress are considered. These collected data are used for the training process of machine learning algorithms. Several algorithms, such as logistic regression, random forest, and gradient boosting classification, are evaluated. Failure-in-time (FIT) is calculated as an output quantity, which indicates the expected failure rate per time unit.

There are also publications that have focused on system identification to determine the condition of components. Al-Greer *et al.* [27] focused on system identification and briefly discusses how to use system identification for health monitoring and fault detection. In [28], it is discussed in detail how a system identification can be used in order to apply a

fault detection of the components of a dc–dc converter. The publication deals with fault detection using a model-based state estimator approach. The error residuals based on signals from the converter and the state estimator output are evaluated. For each system component (capacitance, series resistance, and power devices), fault signatures are collected. The procedure is validated with the help of an experiment, also analyzing the dynamics and the speed of the procedure.

Biglarbegian *et al.* [29] focused on high-frequency gallium nitride (GaN)-based power converters. Especially, the aging mechanism solder fatigue is considered. As a failure precursor of GaN devices, the drain–source resistance $R_{ds(on)}$ is evaluated. In converter operation, the data are collected by monitoring voltage, temperature, and current. From the captured data, $R_{ds(on)}$ is identified by using an algorithm that follows the Bayes theorem. Thereby, the probability density of the unknown model parameters is calculated, with which the resistance $R_{ds(on)}$ is determined. Recently, several publications have been published in the field of digital twins of power converter systems. A digital twin is a virtual representation that operates as the real-time digital model of a physical object. In [30], the application of a digital twin based on a general methodology for maintenance optimization is studied. The objective is to find the most cost-effective maintenance strategy for an operational lifetime. Therefore, a real-world power converter use case is investigated.

In [31], a digital twin of a dc–dc converter is established with the aim for condition monitoring of the system components. First, the dc–dc converter is modeled with unknown parameters. In order to estimate the unknown model parameters, a particle swarm optimization (PSO) algorithm is applied. The algorithm uses an objective function, which calculates the difference between the model results of the digital twin and the measurement results with regard to the output quantities as inductor current and output voltage. The aim is to minimize the objective function by means of the PSO algorithm and thus to determine the model parameters that act as health indicators. By observing the health indicators, the degradation trends of the system components, such as capacitor and MOSFET, can be detected.

In [32], a digital twin of a PV energy conversion unit, which consists of a PV source and a power converter, is designed. In the operational phase, the difference between the estimated and measured output is evaluated in order to generate an error residual. Similar to [28], this so-called fault signature is detected in order to identify the fault type. The detection and identification of ten different faults are shown by means of experimental results.

In order to classify the proposed approach between the mentioned publications, the most important characteristics and features are listed here. The special feature of the proposed approach is that it operates on system level. Since the controller output variables are used for the analysis, it is theoretically possible to detect all changes at system level. However, this is coupled with the requirement that the different aging mechanisms and the effects on the investigated data must be differentiated. The publication focuses on the two converter components power semiconductors and dc-link

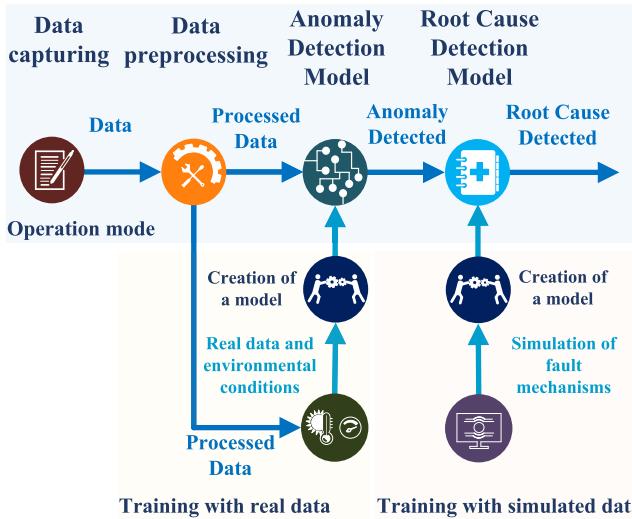


Fig. 1. Approach to condition monitoring consisting of four steps: data capturing, data preprocessing, anomaly detection, and root cause detection.

capacitor, whereby the approach can be extended to other system components such as the current sensors, cooling system, and mechanic components. As failure mechanisms, the heating of the power semiconductor chips and the capacitance loss of the dc-link capacitors are investigated.

In this proposed approach, the power converter model is not used as a virtual representation, and however, it is used in order to perform aging simulations and thus to create new models that recognize certain patterns in the existing data. This means that there is no requirement that the power converter model must have the exact same output results as the real-world converter like in the digital twin method. Since the presented approach works with datasets, methods and tools from data analysis are used. Hence, the proposed method is a hybrid of data- and model-based approaches. For data collection, outlier detection, and anomaly detection, data-based methods are used. For the root cause detection, the knowledge of aging simulation is used to generate mathematical models.

II. PROPOSED APPROACH

In this work, an approach to condition monitoring is developed, which does not require additional sensors and only uses the available data. The block diagram of the approach is shown in Fig. 1.

The first step of the approach is data capturing. Here, the data relevant for condition monitoring are saved. In the context of this work, all output control variables of the control system are collected. The next step is data preprocessing. Statistical methods are used to detect outlier data points [20], [21]. Those points are eliminated from the dataset. Then, the processed data are passed to the data analysis, which consists of a two-step procedure: anomaly detection and root cause detection.

In order to distinguish between aging mechanisms of the power electronic components and changes in the operational or environmental conditions, a preliminary stage of anomaly detection is implemented. The anomaly detection model aims to detect an anomaly within the dataset. This algorithm is trained with real data. The underlying algorithm is a computation paradigm that determines the severity of an anomaly.

The procedure can be considered as a kind of data library. In the training phase, this data library is filled with the data of the converter reference behavior with inclusion of operational and environmental conditions. Environmental conditions can be any parameters such as outdoor temperature, humidity, and vibration depending on the practical application. For the purpose of this publication, the power module temperature has been included in the dataset. Since power electronic components such as power semiconductor devices are very sensitive to temperature, this information is necessary. In the training process, the normal behavior is described by means of a mathematical model. During converter operation, the new incoming operating data are collected and compared with the data from the data library, which was recorded during the training phase, including all relevant environmental and operating conditions. This ensures that a correct comparison is made between the data recorded in the training process and the new incoming dataset.

If an anomaly is detected, the dataset is passed to the root cause detection model. The goal of the root cause detection model is to locate the cause of aging as well as determine the severity of aging. The root cause detection model is a machine learning algorithm trained with simulation data from different failure cases. Machine learning generates knowledge from experience by learning patterns based on the existing data. These identified patterns can be generalized and applied to a new, unknown dataset in order to make predictions. For the data generation, simulation models are required that are able to simulate failure cases at different levels. The application of this principle for the early detection of power converter failures is the focus of this publication.

The data preprocessing and the anomaly detection have been introduced in our previous publication [2]. Therefore, these aspects will not be described further in this current publication. The root cause detection has already been discussed in our publication [3]. In this article, however, a more detailed explanation is given by specific examples in Section VI-B.

A. Following Structure

In Section IV, a simulation model is developed, which is used to simulate specific failure cases. In Section IV-A, the converter is modeled with ideal components. In Section IV-B, the model will be extended to include degradation indicators. This will enable the simulation of various failure scenarios. Before that, however, the aging mechanisms and the corresponding degradation indicators will be determined in Section III.

Then, the correlations between the degradation indicators and the available data are evaluated in Section VI-B. For each aging mechanism, patterns are identified, which represents a specific feature of the failure case that has occurred. Such specific patterns, which can be used to determine the failure case, are called features in the field of machine learning. A feature denotes a characteristic attribute or property of an observed phenomenon. Features provide an indication of the failure case and allow differentiation between different failure cases.

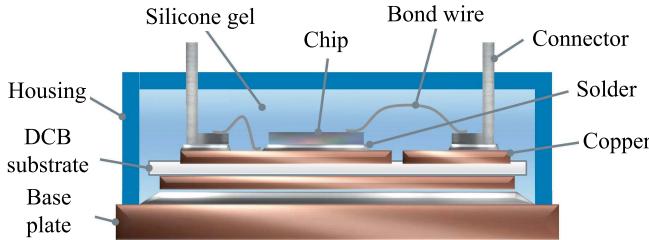


Fig. 2. Structure of a power semiconductor module [5].

Based on the determined correlations, suitable mathematical models are trained in Section VI-B. These models are capable of detecting failure cases using the available data. In order to test these created models, specific changes and manipulations are induced to the converter system at the test bench, as given in Section VII.

III. AGING MECHANISMS AND DEGRADATION INDICATORS

The publication focuses on two converter components as follows:

- 1) power semiconductors;
- 2) dc-link capacitor.

For each component, we will explain several aging mechanisms that have been studied in the literature. Based on the aging mechanisms, the degradation indicators are identified.

A. Power Semiconductors

In commercial markets, three-phase bridges are nowadays offered in compact, so-called power semiconductor modules. This type of housing was first introduced to the market by the manufacturer Semikron in 1975 [4]. The required IGBTs and diodes are integrated into one housing. The structure of a power semiconductor module is shown in Fig. 2.

Many aging mechanisms of power semiconductors occur at the module level [6]–[12]. The reason for this is the layered structure. Different materials are used for the individual layers, which have to fulfill various tasks and conditions [12], [13]. As a result, the thermal expansion coefficients of the involved materials used can differ. During load cycles, temperature cycles occur, which leads to different expansions of the individual materials and thus also to thermomechanical stresses at the interfaces. Over time, this leads to cracks and fractures at the interfaces.

The interface between the bond wires and the semiconductor chips is a failure-prone spot. The bond wires of the power semiconductor module are usually made of aluminum and the semiconductor chips of silicon. The thermal expansion coefficients of the two materials differ by a factor of almost eight [6]. Aging mechanisms at this spot are referred to in the literature as bond wire failure [7]–[9]. This failure mechanism is divided into two subgroups, bond wire cracking and bond wire liftoff, depending on whether a fracture or a complete separation of the bond wire has occurred.

The separation of a bond wire results in a smaller cross-sectional area for the current and therefore to a larger ohmic resistance. This relationship is further investigated in [7]

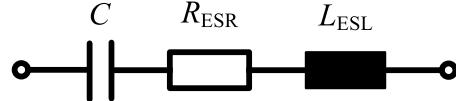


Fig. 3. Simplified impedance model of a capacitor.

in which individual bond wires are cutoff and the increase in differential resistance is detected. In Section IV-B, the differential resistance of the conduction characteristics is explained and then integrated into the converter model from Section IV.

Another wear-out failure describes the aging of the solder and is called solder fatigue [10]–[12]. According to Fig. 2, the solder is the connecting link between the semiconductor and the copper metallization. This junction, which consists of the material tin, is prone to failure. Due to the differences in thermal expansion coefficients, thermomechanical stresses occur at the solder when temperatures fluctuate, leading to cracks and delamination over time.

There are two degradation indicators that provide information about solder fatigue. In [10], it is shown that solder fatigue leads to a change in conduction characteristics of the collector-emitter path. Furthermore, in [7], the correlation between the thermal resistance from the chip to the heat sink and the condition of the solder is determined.

B. DC-Link Capacitor

There are three different capacitor types: electrolytic, film, and ceramic capacitors [14]. The material used for the dielectric medium is the crucial component that determines the performance and properties of the capacitor. In this article, the film capacitor is investigated in more detail. Film capacitors provide a balanced performance in terms of cost, equivalent series resistance (ESR), capacitance, ripple current, and reliability [14]. However, the low operating temperature must be considered since polypropylene has a low melting temperature of around 165 °C [25].

An essential degradation indicator that provides information about the condition of a capacitor is its value of the capacitance [14]–[16]. This applies to all capacitor types. In terms of reliability, film capacitors have an important unique characteristic of self-healing capability. Locally occurring dielectric breakdowns (e.g., due to overvoltage) of a film capacitor can be eliminated with the capacitor regaining its full operational capability except for a negligible reduction in capacitance. However, the total capacitance may be reduced over time due to an increase in such damaged areas. It is assumed that 95%–98% of the original capacitance value is the limit for the usability of a film capacitor [14]. In addition, the ESR can also be used to estimate the condition of a capacitor [17]–[19]. Fig. 3 shows the simplified impedance model of a capacitor, which consists of three components: the capacitance, the ESR, and the equivalent series inductance (ESL).

Fig. 4 shows the corresponding frequency diagram, which is determined by these three components and can therefore be divided into three frequency ranges. Depending on the frequency, one or the other component, such as the capacitance, the ohmic resistance, or the inductance, is the dominating

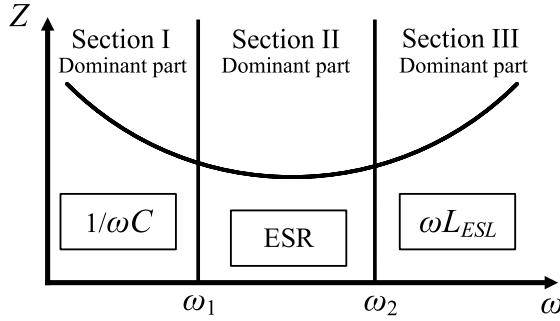


Fig. 4. Simplified impedance diagram of a capacitor.

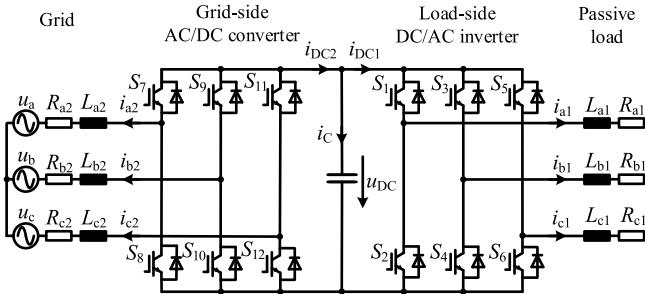


Fig. 5. Inverter with a rectifier, a dc link, and a dc/ac inverter.

component. For electrolytic capacitors, the degradation limit is reached when the ESR doubles [14].

IV. MODELING

In this article, an inverter with three-phase rectifier, a dc link, and a dc/ac inverter on the output side is investigated. Fig. 5 shows the circuit topology. This circuit is one of the most important circuits in the field of power electronics. It is used in many important applications, for instance, in the field of industrial robots and renewable energies.

This circuit is described with the use of differential equations. Subsequently, these equations are transformed into the state-space equation. In Section IV-A, the components of the power electronic system are considered ideal. Accordingly, the power semiconductor components behave like ideal switches, which assumes the value $S = 1$ when the switch is closed and $S = 0$ when the switch is open. In Section IV-B, the degradation indicators are additionally considered and implemented in the converter model.

A. Converter Model

The state-space representation is described by the first-order state differential equation and by the output equation as follows:

$$\vec{x} = A \cdot \vec{x} + B \cdot \vec{u} \quad (1)$$

$$\vec{y} = C \cdot \vec{x} \quad (2)$$

where \vec{x} denotes the state variable, \vec{y} denotes the output variable, and \vec{u} denotes the input variable. The coefficients $A-C$ are matrices. The state variable \vec{x} contains the load- and grid-side currents as well as the dc-link voltage (3). The output variable \vec{y} is identical with the state variable \vec{x} —consequently, the matrix C represents the unit matrix. The grid voltages u_a ,

u_b , and u_c represent the input variable of the system \vec{u}

$$\vec{x} = \begin{pmatrix} i_{a1} \\ i_{b1} \\ i_{c1} \\ i_{a2} \\ i_{b2} \\ i_{c2} \\ u_{DC} \end{pmatrix}, \quad \vec{y} = \begin{pmatrix} i_{a1} \\ i_{b1} \\ i_{c1} \\ i_{a2} \\ i_{b2} \\ i_{c2} \\ u_{DC} \end{pmatrix}, \quad \vec{u} = \begin{pmatrix} u_a \\ u_b \\ u_c \end{pmatrix}. \quad (3)$$

To identify the two matrices A and B , the state-space equation is multiplied by the matrix E . This results as follows:

$$E \cdot \vec{x} = F \cdot \vec{x} + G \cdot \vec{u}. \quad (4)$$

The two matrices to be identified are shown in the following:

$$A = E^{-1} \cdot F, \quad B = E^{-1} \cdot G. \quad (5)$$

A total of seven differential equations are set up—four voltage equations, two current equations, and one equation describing the dc-link voltage. Each three of these equations refer to one three-phase bridge circuit. First, the load-side converter will be considered here. The voltage equation, which represents the mesh between phases a and b , is described by the voltage $[(S_1 - S_2) - (S_3 - S_4)]/2 \cdot u_{DC}$. The right-hand side of the equation is formulated by the voltage drop across the individual components. The equation results in the following:

$$\frac{(S_1 - S_2) - (S_3 - S_4)}{2} \cdot u_{DC} \\ = R_{a1} \cdot i_{a1} + L_{a1} \cdot \frac{di_{a1}}{dt} - R_{b1} \cdot i_{b1} - L_{b1} \cdot \frac{di_{b1}}{dt}. \quad (6)$$

Now, the mesh equation between phases b and c is set up (7), which is analogous to (6)

$$\frac{(S_3 - S_4) - (S_5 - S_6)}{2} \cdot u_{DC} \\ = R_{b1} \cdot i_{b1} + L_{b1} \cdot \frac{di_{b1}}{dt} - R_{c1} \cdot i_{c1} - L_{c1} \cdot \frac{di_{c1}}{dt}. \quad (7)$$

The voltage equation describing the relationship between phases a and c is intentionally not included since this information is contained in the two equations before and is therefore redundant. To include this equation would have the consequence that the matrices E and F would become singular. A singular matrix is not invertible. However, this property is a requirement for the matrix E in order to solve the equations in (5).

Analogous to the procedure just described, the two voltage equations that are related to the grid-side converter can be set up. The two voltage equations are the same as (6) and (7) only with the exception that the grid voltages have to be included in the formulas. This is why the formulas are not further elaborated here.

Now, the current equations are set up. For this purpose, Kirchhoff's 1st law is used, which states that in a node of an electrical network, the sum of the inflowing currents is equal to the sum of the outflowing currents. In terms of the load-side converter, the following equation can be obtained from this since the three-phase currents flow to a node and their sum must therefore equal zero

$$i_{a1} + i_{b1} + i_{c1} = 0. \quad (8)$$

However, this equation would create a zero row in the matrix E from (5), which would make this matrix singular and thus not invertible. To solve this problem, (8) is derived. By derivation, the equation does not lose its validity. Hereafter, the following equation results, which is considered in the state-space representation

$$\dot{i}_{a1} + \dot{i}_{b1} + \dot{i}_{c1} = 0. \quad (9)$$

Similarly, the following equation applies to the power converter on the line side

$$\dot{i}_{a2} + \dot{i}_{b2} + \dot{i}_{c2} = 0. \quad (10)$$

To couple the load side with the grid side, an equation is needed, which describes the dc-link voltage as a function of the load and line currents. The general equation for determining the voltage across a capacitor with constant electrical capacitance C_{DC} is

$$u_{DC}(t) = u_{DC}(0) + \int_0^t \frac{\dot{i}_C}{C_{DC}} dt = u_{DC}(0) + \int_0^t \frac{i_{DC2} - i_{DC1}}{C_{DC}} dt. \quad (11)$$

The current flowing through the dc-link capacitance is described by the difference of the two dc currents i_{DC2} and i_{DC1} (11). These are determined by the phase currents and by the transistor switching states as follows:

$$u_{DC}(t) = u_{DC}(0) + \int_0^t \frac{(S_2 \cdot i_{a1} + S_4 \cdot i_{b1} + S_6 \cdot i_{c1}) - (S_7 \cdot i_{a2} + S_9 \cdot i_{b2} + S_{11} \cdot i_{c2})}{C_{DC}} dt. \quad (12)$$

After transforming the equations to the state-space representation (4), we obtain the matrices shown in (13)–(16)

$$E = \begin{pmatrix} L_{a1} & -L_{b1} & 0 & 0 & 0 & 0 & 0 \\ 0 & L_{b1} & -L_{c1} & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & L_{a2} & -L_{b2} & 0 & 0 \\ 0 & 0 & 0 & 0 & L_{b2} & -L_{c2} & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{pmatrix} \quad (13)$$

$$C = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{pmatrix} \quad (14)$$

$$F = \begin{pmatrix} -R_{a1} & R_{b1} & 0 & 0 & 0 & 0 & \frac{(S_1 - S_2) - (S_3 - S_4)}{2} \\ 0 & -R_{b1} & R_{c1} & 0 & 0 & 0 & \frac{(S_3 - S_4) - (S_5 - S_6)}{2} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -R_{a2} & R_{b2} & 0 & \frac{(S_7 - S_8) - (S_9 - S_{10})}{2} \\ 0 & 0 & 0 & 0 & -R_{b2} & R_{c2} & \frac{(S_9 - S_{10}) - (S_{11} - S_{12})}{2} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{S_2}{C_{DC}} & \frac{S_4}{C_{DC}} & \frac{S_6}{C_{DC}} & -\frac{S_7}{C_{DC}} & -\frac{S_9}{C_{DC}} & -\frac{S_{11}}{C_{DC}} & 0 \end{pmatrix} \quad (15)$$

$$G = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix}. \quad (16)$$

B. Converter Model With Degradation Indicators

So far, ideal converter components were assumed for modeling the converter. However, in order to enable a systematic investigation of aging mechanisms, model parameters are required, which describes specific aging mechanisms. Such parameters are termed as degradation indicators or sensitive parameters. These parameters can be used for condition monitoring in converter operation. The aim of this section is now to extend this model by the degradation indicators. Therefore, these degradation indicators are integrated into the differential equations. Subsequently, the differential equations are transferred into the state-space representation.

1) Power Semiconductors: The conduction characteristic of the power semiconductor devices was simulated by the two parameters r_{CE} and U_f :

- 1) differential resistance of the collector-emitter path r_{CE} ;
- 2) threshold voltage of the collector-emitter path U_f .

The i_{CE} - U_{CE} conduction characteristic of a power semiconductor device can be described by the following:

$$u_{CE} = U_f + r_{CE} \cdot i_{CE}. \quad (17)$$

These parasitic effects are considered by including the formula (17) for every power semiconductor of the converter topology from Fig. 5. This results in the state-space representation in the following, which has the additional term Z

$$E \cdot \vec{x} = F \cdot \vec{x} + G \cdot \vec{u} + Z. \quad (18)$$

The matrices F and Z result in (19) and (20), while the matrices E , C , and G remain the same as in (13), (14), and (16), (19) and (20), as shown at the bottom of the next page.

Unlike the matrices (13)–(16) from (4), the matrices (19) and (20) have additional terms that contain the information about the conduction characteristics of the power semiconductors. These terms depend on the sign of the phase current. A case distinction must be made for different signs of the phase currents since either the IGBT or the diode conducts depending on the current sign.

2) DC-Link Capacitor: Now, the same principle from Section IV-B1 is applied to the degradation indicators of the dc-link capacitor. The following two degradation indicators are integrated into the existing model from Section IV-A:

- 1) capacitance value C_{DC} of the dc-link capacitor;
- 2) ESR R_{ESR} of the dc-link capacitor.

The parameter C_{DC} is already included in the matrix F as shown in (15). The parameter R_{ESR} is integrated into the equivalent circuit according to Fig. 3. This results in the extended matrix E with the additional parameter R_{ESR} (21).

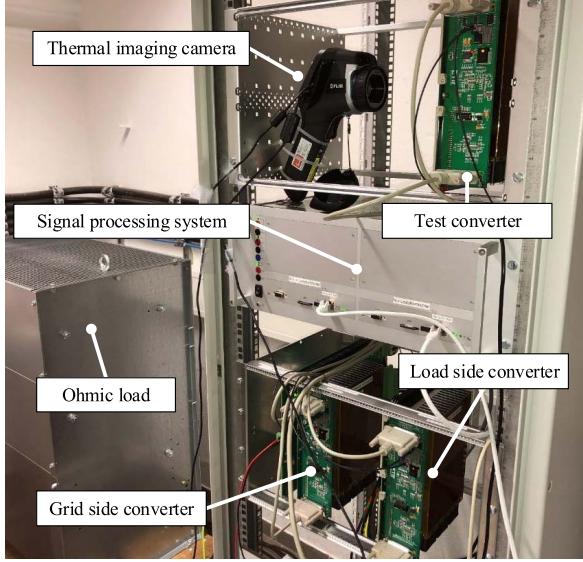


Fig. 6. Test bench.

The other matrices G , F , and Z remain unchanged (21), as shown at the bottom of the page.

Now, the degradation indicators have been integrated into the converter model. The goal of Section VI-B is to vary these degradation indicators and to investigate the effects on the available variables of a power electronic system. Before that, however, Section V introduces the test bench, which forms the basis for the data capturing.

V. TEST BENCH

The test bench represents the topology from Fig. 5. In Section V-B, the test bench is extended by fault devices to allow implementation of intentional fault cases and manipulations on the power converter system.

A. Structure of the Test Bench

The test bench consists of a rectifier that converts the three-phase grid voltage provided by the grid into a dc voltage. This dc voltage is transformed again into a three-phase ac voltage by another power converter. It results in an overall topology that can transform the grid voltage into an output voltage that is variable in amplitude and frequency. A passive load is used, consisting of an ohmic resistor and an inductor. The physical test bench setup can be seen in Fig. 6.

The same type of converter is used for both the grid-side rectifier and the load-side inverter. The inverter is equipped with the EconoPack2 FS75R12KT4 (1200 V/75 A) IGBT module from Infineon and can provide a rated power of 30 kW. The test bench has a measurement system for each of the three-phase output currents, the heat sink temperature, and the dc-link voltage. In addition, the module temperature can be measured using a negative temperature coefficient (NTC) resistor that is located in the power semiconductor module.

B. Failure Devices

The test bench is extended in such a way that intentional implementation of failure cases is possible.

For investigations on the power semiconductor chips, an additional power supply is used. This power supply is connected to the dc link to provide a more constant dc-link voltage and, thus, to decouple the grid side by the high capacitance of the power supply in order to allow a more isolated investigation of the power semiconductors. The power supply EA-PSB 9200-140 is used, which can deliver a maximum voltage of 200 V and a maximum current of 140 A. The maximum power is 10 kW.

$$F = \begin{pmatrix} -R_{a1} - F_{a1} & R_{b1} + F_{b1} & \cdots & \cdots & \cdots & \cdots \\ \vdots & -R_{b1} - F_{b1} & R_{c1} + F_{c1} & \cdots & \cdots & \cdots \\ \vdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ \vdots & \cdots & \cdots & -R_{a2} - F_{a2} & R_{b2} + F_{b2} & \cdots \\ \vdots & \ddots & \ddots & \ddots & -R_{b2} - F_{b2} & R_{c2} + F_{c2} \\ \vdots & \ddots & \ddots & \ddots & \cdots & \cdots \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \end{pmatrix} \quad (19)$$

$$Z = \begin{pmatrix} Z_1 - Z_2 \\ Z_2 - Z_3 \\ 0 \\ Z_4 - Z_5 \\ Z_5 - Z_6 \\ 0 \end{pmatrix} \quad (20)$$

$$E = \begin{pmatrix} L_{a1} & -L_{b1} & 0 & 0 & 0 & 0 & 0 \\ 0 & L_{b1} & -L_{c1} & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & L_{a2} & -L_{b2} & 0 & 0 \\ 0 & 0 & 0 & 0 & L_{b2} & -L_{c2} & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 & 0 \\ S_2 \cdot R_{ESR} & S_4 \cdot R_{ESR} & S_6 \cdot R_{ESR} & -S_7 \cdot R_{ESR} & -S_9 \cdot R_{ESR} & -S_{11} \cdot R_{ESR} & 1 \end{pmatrix} \quad (21)$$

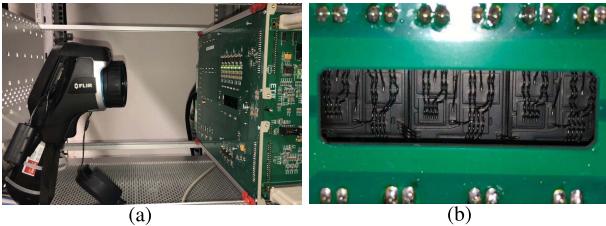


Fig. 7. Test arrangement for gaining access to power semiconductor devices. (a) Thermal imaging camera. (b) Open window in converter.

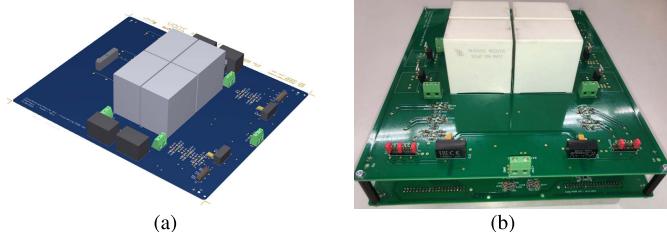


Fig. 8. DC-link capacitor circuit board that allows the variation of the degradation indicators of the dc-link capacitor in converter operation. (a) Layout of the circuit board. (b) Circuit in the real application.

1) Power Semiconductors: In the power section board, an open viewing window has been designed (see Fig. 7). This enables the implementation of failure cases in the power semiconductors. For example, it is possible to heat individual semiconductor chips using a hot air gun and to cut off individual bond wires (bond wire liftoff). In addition, the open viewing window allows the chip temperature to be measured using the FLIR E60 thermal imaging camera during converter operation. Black-painted power modules are used, which allow a more accurate detection of chip temperature through the thermal imaging camera.

2) DC-Link Capacitor: A circuit board has been designed, which allows the variation of the degradation indicators of the dc-link capacitor in converter operation (see Fig. 8). This additional board is attached to the power section board of the converter. The capacitance and the ESR of the dc-link capacitor can be changed. Individual dc-link capacitors can be connected and disconnected using MOSFETs in order to change the total capacitance of the dc link. The board consists of four film capacitors with the brand name ICEL MHBS505500, which can be added separately. The dielectric is made of the material polypropylene. The nominal value of the capacitance is 50 μF with a tolerance of 10%.

The nominal ESR of an inserted capacitor is 2.8 m Ω at a switching frequency of 1 kHz. In addition, the dc-link board can connect an additional ohmic resistor in each path. The additional ohmic path is activated by a MOSFET as well. The value of the additional ohmic resistor is 280 m Ω . This approximately doubles the initial ESR, which consists of the nominal ESR of the capacitor as well as the resistance of the activated MOSFET.

VI. ALGORITHM TO CONDITION MONITORING

This section deals with the machine learning algorithm shown in Fig. 1. The first step of the machine learning algorithm is the data capturing, which is explained in Section VI-A. In Section VI-B, the created root cause detection models are described.

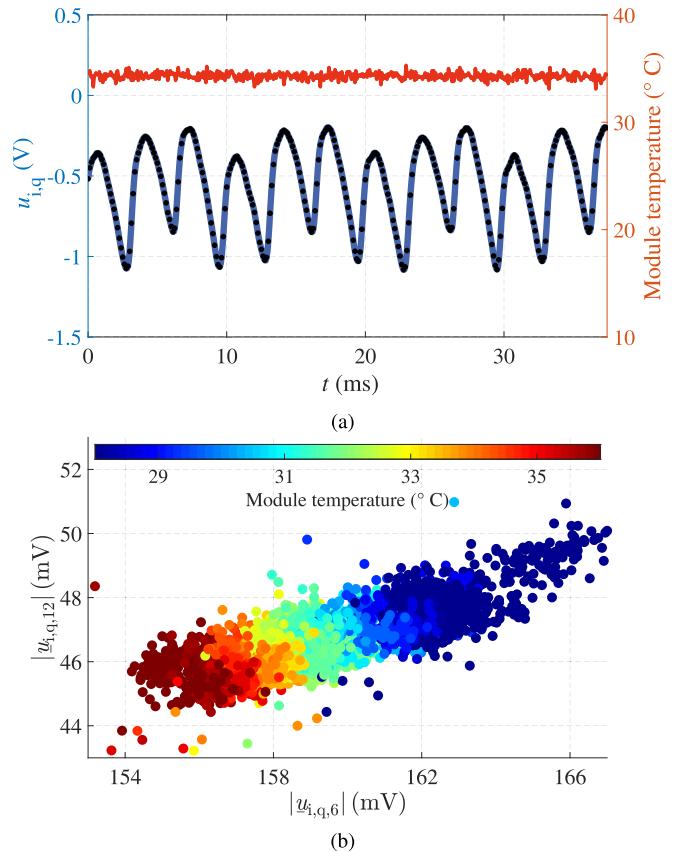


Fig. 9. Measurement results: integral part of the current controller output in q -axis. (a) Time domain. (b) Frequency domain with module temperature dependence.

A. Data Capturing

In this section, the data that are used for condition monitoring is explained. It is the first step of the machine learning algorithm. In Section VI-A1, the data for analyzing the power semiconductor are studied, and then, in Section VI-A2, the data used for monitoring of the dc-link capacitors are investigated.

1) Power Semiconductors: In this work, the controller output variables are considered since the controller always reacts to changes in the system. This means that the controller also reacts to aging of the system components. This principle is used to detect aging mechanisms that have occurred during operation. In [2], the current control system is shown. The output voltages can be divided into a d - and a q -component, which represents the d - and q -axes in the rotational reference system. In addition, the output variables of the control are divided into proportional and integral components. As an example, in Fig. 9(a), the integral part of the current controller output in the q -axis is shown. The module temperature is also recorded. The temperature is included in order to be able to differentiate between temperature-related effects and aging.

The signals are analyzed in the frequency domain. For this purpose, a fast Fourier transformation (FFT) is performed for each electrical period to transform the voltages from the time domain to the frequency domain. The operating point is given in Table I.

TABLE I
PARAMETER SET OF OPERATING POINT

Parameter	Value
Current d-axis i_d	10 A
Current q-axis i_q	0 A
DC link voltage u_{DC}	200 V
Electrical frequency f_{el}	50 Hz
Sampling frequency f_S	16 kHz
Ohmic resistors R_a, R_b, R_c	2.1Ω
Load inductors L_a, L_b, L_c	2 mH

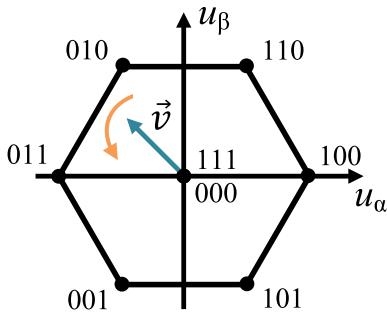


Fig. 10. Space vector diagram with the associated switching states of the power devices.

The dataset consists of 3031 data points since this is the number of electrical periods that are captured, which corresponds to a total duration of 60 s. Fig. 9(b) shows the 6th and 12th harmonics of the integral part of the controller output in the q -axis for the investigated operating point. In addition, the information about the module temperature is included in the data points. A temperature fluctuation can be observed, which is caused by the fan, whose electrical power is not always constant in steady-state operation.

Furthermore, Fig. 9(b) shows that power semiconductor effects affect the sixth harmonic and its multiples in the dq coordinate system. The temperature-related changes in the power semiconductors with regard to the conduction characteristics lead to changes in the 6th and 12th harmonics of the controller outputs. This can be explained graphically with the hexagonal space vector diagram (see Fig. 10). The space vector diagram can be divided into six sectors. In a three-phase system, there are six different states, which sign the three output currents that can have $(+--), (++-), (-+-), (-++), (-+-), (+-+)$. The two states $+++$ and $--$ are not possible. Depending on which state is present, the parasitic effects of the power semiconductors add or subtract to the ideal fundamental wave. When a fundamental wave is passed through, a total of six different states occur exactly once, forming a sixth harmonic.

In order to illustrate the principle, Fig. 11 shows the simulation results of the output vector in the $\alpha\beta$ -frame for numerous electrical periods. In the simulation framework, the power semiconductor devices show parasitic effects, whereby a voltage drop of 6 V is assumed here as an example in order to show the principle. It can be observed that the provided output vector of the controller does not correspond to an ideal circular shape, but for each of the six states, an elevation of the vector can be seen as the parasitic effects of the power semiconductors are compensated by the controller.

The sampling frequency is $f_S = 16$ kHz. Thus, the controller receives a measured value at time intervals of

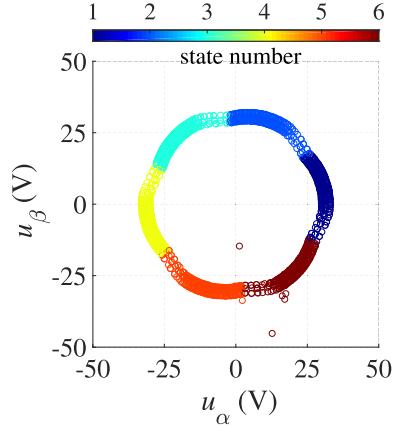


Fig. 11. Simulation results of the controller output voltage in the $\alpha\beta$ -frame when a voltage drop is assumed across the power semiconductors. State number refers to which sign the output currents have as described above.

$T_S = 62.5 \mu\text{s}$. From this value, a controller output variable is calculated, which is represented by one data point. This results in one data point for each time period. The sampling rate of the AD card is 5 Msps. For the measured data recorded by the AD card, the average value is calculated for each time period of $T_S = 62.5 \mu\text{s}$ and fed to the controller. For instance, for a sample rate of 5 Msps and a sampling frequency of $f_S = 16$ kHz, $\lfloor(5 \cdot 10^6)/16000\rfloor = \lfloor 312.5 \rfloor = 312$ values can be measured each time period. From this, an average value is calculated and sent to the controller. As the sampling rate or the number of data points involved in the mean value calculation increases, the noise decreases, and thus, the scatter in the data cloud decreases. In Fig. 12, the relationship between the number of the points included in the mean value calculation in the AD card and the accuracy of the recorded data is shown. The red data points refer to a mean value calculation with 312 data points of the AD card, whereby the gray data points correspond to 32 data points. As an example, the second harmonic is shown in Fig. 12. After collecting data points of the controller output voltages, the mean value of the data cloud can be evaluated. Fig. 12 indicates that there is only a marginal difference in the center points of the data clouds when the accuracy in the data acquisition differs, and however, when fewer data points for the mean value calculation in the AD card are considered, the accuracy is lower and the noise is higher.

However, time can compensate for a lower sampling rate. Even with low sampling rates and large scatter in the data cloud, statements can be made about aging, but more time is then required so that the data clouds are sufficiently compacted. The more time passes during the data acquisition, the more the data cloud is compressed. If a sufficient number of data points are recorded, the center of the data cloud is evaluated, which means that the scatter of the data cloud does not play a significant role in the data evaluation. Even if measurement accuracy is low and noise is high, taking more time can compensate for these shortcomings.

2) DC-Link Capacitor: For the analysis of the dc-link capacitor, the dc-link voltage as a function of time is considered [see Fig. 13(a)]. For every electrical time period from Table I, this curve can be transformed into the diagram in

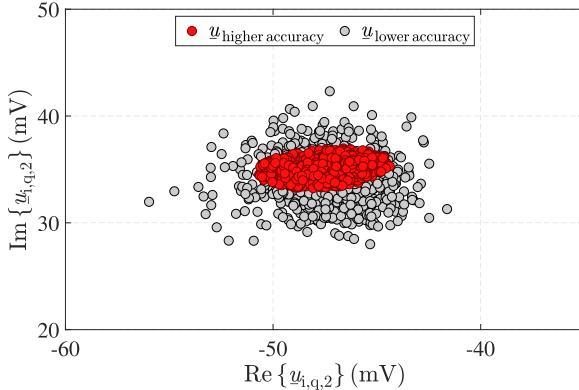


Fig. 12. Measurement results: relationship between the number of the points included in the mean value calculation in the AD card and the accuracy of the recorded data. Red data points refer to a higher accuracy by taking 312 data points into account when averaging the measured data. Gray data points refer to a lower accuracy by considering 32 data points.

Fig. 13(b). Fig. 13(b) shows the data points of ripple and variance of the dc-link voltage that are calculated according to the formulas (22) and (23). In order to calculate the ripple, the maximum and minimum values are determined for every section of an electrical period as follows:

$$u_{\text{Ripple}} = \max(u_{\text{DC},N}) - \min(u_{\text{DC},N}). \quad (22)$$

For the calculation of the variance, the difference from the mean value is calculated and squared (23). N indicates the amount of data for the evaluated section of an electrical period

$$u_{\text{var}} = \frac{1}{N-1} \cdot \sum_{i=1}^N |u_{\text{DC},i} - \text{mean}(u_{\text{DC},N})|^2. \quad (23)$$

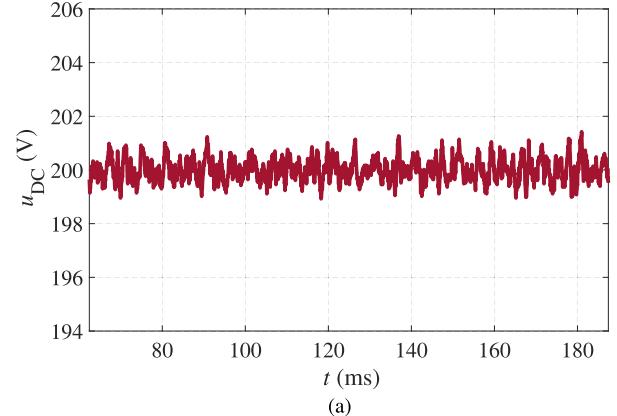
These data clouds can be represented by a mean value, which is based on the Mahalanobis distance. Unlike the Euclidean distance, the Mahalanobis distance also takes the different variances of the two axes into account by considering the covariance matrix [20], [21]. For calculating the mean value of data clouds, a special variant of the Mahalanobis distance is used, which is not distorted by the outlier data points. It is called robust Mahalanobis distance and is further described in [20].

B. Creation of a Root Cause Detection Model

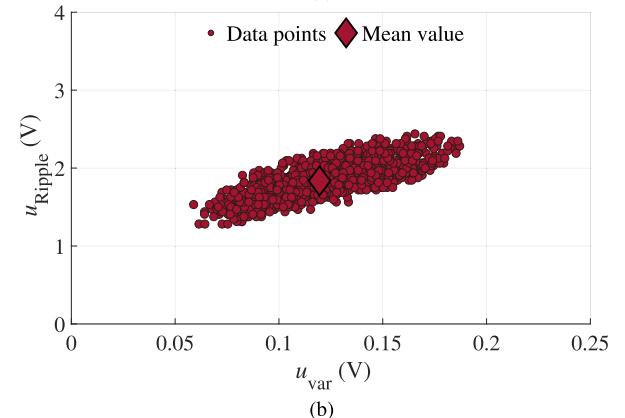
In this section, the models from Section IV are used to vary the degradation indicators in a simulation framework. The correlations between the degradation indicators and the available data are evaluated. Based on this, suitable mathematical models are created, which are capable of detecting these failure cases.

1) *Power Semiconductors*: As an example, the creation of such a model will be shown using the threshold voltage of the IGBTs in the collector-emitter path. First, the threshold voltages of all six IGBTs U_f of the load-side inverter from Fig. 5 are equally varied according to Table II.

The simulation results show that the magnitudes of the sixth harmonics of the controller outputs correlate with the simulated threshold voltages of the IGBTs. The same correlation is also observed for the multiples of the sixth harmonics



(a)



(b)

Fig. 13. Measurement results of the dc-link voltage. (a) Time waveform. (b) Variance and ripple.

TABLE II
VARIATION OF THE IGBT THRESHOLD VOLTAGES

Number of simulations	160
Value range threshold voltage IGBT $U_{f, \text{IGBT}}$	0.41 V - 2 V
Step size threshold voltage IGBT $U_{f, \text{IGBT}}$	0.01 V

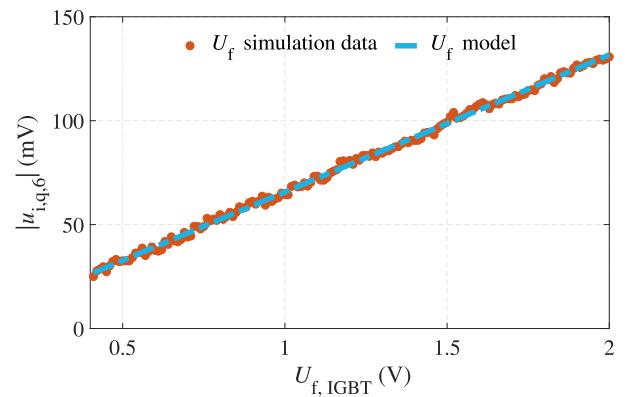


Fig. 14. Simulation results and the corresponding model of the sixth harmonic of the integral component of the q -axis over the simulated threshold voltage of the IGBTs.

(12th, 18th, 24th, and so on). Fig. 14 shows the diagram of the sixth harmonic of the integral component of the q -axis over the simulated threshold voltage of the IGBTs.

The figure indicates a linear relationship between the two variables. Therefore, a linear model is used in order to replicate the simulation results, which is shown in the following:

$$|u_{i,q,6}| = a \cdot U_{f, \text{IGBT}} + b. \quad (24)$$

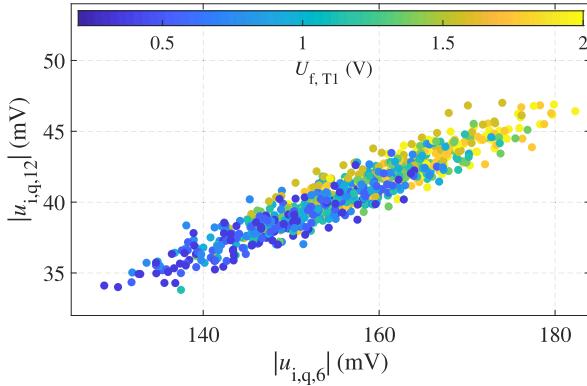


Fig. 15. Simulation results of the 6th and 12th harmonics of the integral component of the q -axis as a function of the varied threshold voltage $U_{f,T1}$ of IGBT T₁.

TABLE III

VARIATION OF THE INDIVIDUAL THRESHOLD VOLTAGES OF THE IGBTs $U_{f,T1,T3,T5}$

Number of simulations	10
Zero point $U_{f,T1,T3,T5}$	1.2365 V
Value range $U_{f,T1,T3,T5}$	0.6365 V - 1.2365 V
Step size $U_{f,T1,T3,T5}$	0.2 V

The coefficients are calculated by using the least square method with the aim of minimizing the error squares between model and simulation. The coefficients of the model are determined to $a = 0.066$ and $b = -2.77 \times 10^{-4}$ with a coefficient of determination that results in $R^2 = 0.9978$. In this simulation, all six IGBTs of a three-phase bridge circuit were increased simultaneously. In practice, changes in individual power semiconductor chips can also occur. To investigate this aspect as well, the variation of the threshold voltage of one single IGBT is evaluated. As an example, this is changed for the positive IGBT of phase a . Fig. 15 shows the 6th and 12th harmonics of the integral component of the q -axis as a function of the varied threshold voltage $U_{f,T1}$ of IGBT T₁.

The increase of the threshold voltage $U_{f,T1}$ yields an increase of the 6th and 12th harmonics of the integral component of the q -axis. In addition, the relationship is valid for the other multiples of the sixth harmonic not shown here. The variation of only one phase yields an asymmetry, which affects the second harmonic in the dq-frame. Here, the IGBTs T₁, T₃, and T₅ were changed according to Table III. The threshold voltages of the three upper IGBT, which cause a positive phase voltage, were modified individually.

Fig. 16 shows the results of this simulation series. The complex plane of the second harmonic of the integral component in the q -axis is illustrated. Starting from the zero point, where there is no asymmetry, a shift of the second harmonic can be observed. The magnitudes of the second harmonic increase with growing asymmetry. In addition, the phase angle of these harmonics changes depending on which IGBT has changed its threshold voltage. The phase angles of the three upper IGBTs have an angular difference of about 120° to each other. Especially, this correlation can be used to determine which power semiconductor chip exactly is damaged.

2) *DC-Link Capacitor*: For creating a root cause model for the dc-link capacitor, the converter model of Section IV-B is used. A degradation indicator is the value of the capacitance

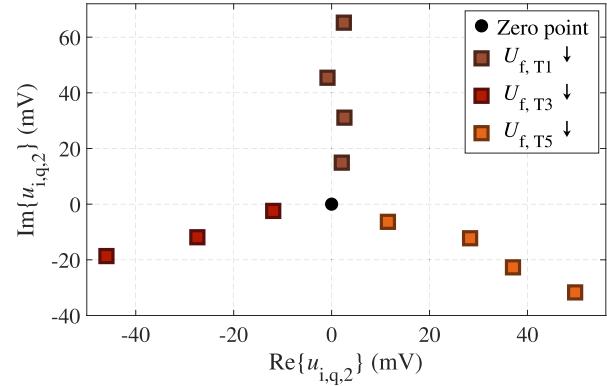


Fig. 16. Simulation results: complex plane of the second harmonic of the integral component in the q -axis as a function of the individual threshold voltages of the positive IGBTs.

TABLE IV

VARIATION OF DC-LINK CAPACITANCE

Number of simulations	350
Value range capacitance C_{DC}	100 μF - 449 μF
Step size capacitance C_{DC}	1 μF

● Simulation data — Model

Fig. 17. Simulation results of the relationship between ripple voltage and the value of the capacitance and the corresponding fit model of the capacity.

C_{DC} . In the following, this variable is simulated according to Table IV.

The simulation results are shown in Fig. 17. The correlation between the ripple and the simulated capacitance value can be seen. An exponential relationship is assumed between the two variables.

Therefore, a second degree exponential function according to the following equation is used to reproduce the simulation results:

$$u_{\text{Ripple}} = a \cdot e^{b \cdot C_{DC}} + c \cdot e^{d \cdot C_{DC}}. \quad (25)$$

In the training process of the algorithm, the coefficients are chosen using the least square method so that the error squares between model and simulation are minimized. Using the MATLAB fitting tool, the coefficients of the model can be determined to $a = 9.68$, $b = -26160$, $c = 2.76$, and $d = -3236$. The coefficient of determination results in $R^2 = 0.9149$.

VII. EXPERIMENTS AND MEASUREMENT RESULTS

A. Power Semiconductors

First, individual chips of the power semiconductor module are heated through the open viewing window of the circuit

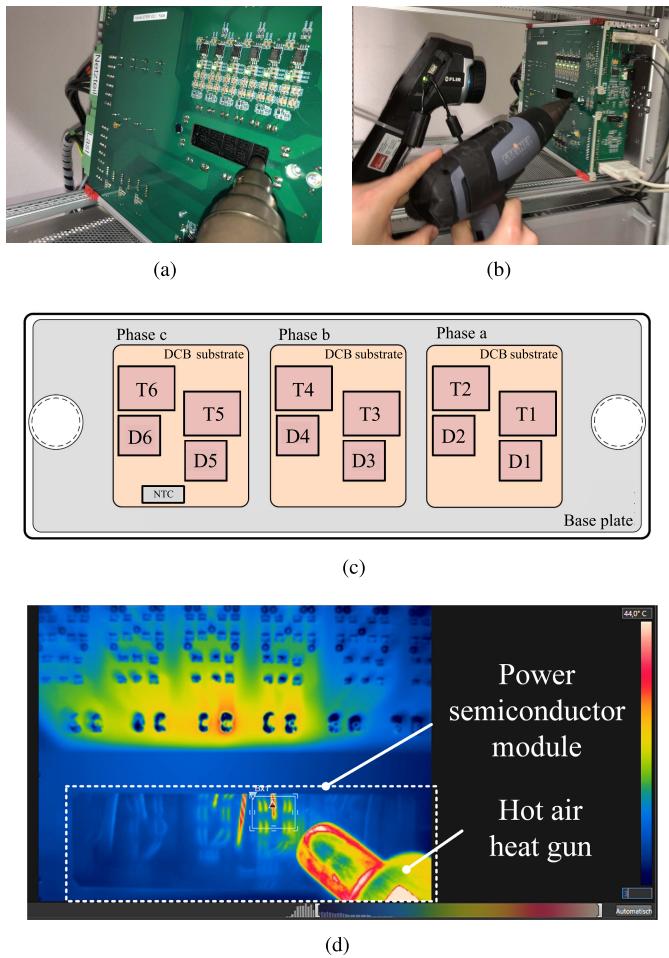


Fig. 18. Heating of individual chips of the power semiconductor module. (a) Heating with hot air heat gun. (b) Recording with thermal camera. (c) Chip names of the power semiconductor module. (d) Results of the thermal imaging camera.

board (see Fig. 7) using a hot air gun. Fig. 18 shows the heating of IGBT T_3 from phase c . In Fig. 18(c), the structure of the power semiconductor module and the chip names is illustrated.

The temperature range of the power semiconductor chips of the operating point from Table I is $40\text{ }^{\circ}\text{C}$ – $45\text{ }^{\circ}\text{C}$. The module temperature is approximately $35\text{ }^{\circ}\text{C}$. Chip T_3 is heated to a maximum temperature above $80\text{ }^{\circ}\text{C}$.

The model results of the root cause detection are evaluated, while the IGBT chip is heated. Therefore, the captured data with the representation form of Fig. 9(b) are transferred to the degradation indicator U_f using the correlation determined in formula (24). The model results of the ON state threshold voltage U_f of the collector–emitter path for the heated and unheated chip as a function of the measured module temperature are shown in Fig. 19.

The model results show a temperature dependence. The module temperature is measured by using the NTC resistor within the module. The ON-state threshold voltage U_f of the collector–emitter path decreases with increasing temperature. The ON-state collector–emitter voltage is a suitable indicator for detecting certain aging mechanisms such as solder fatigue, which is discussed in [10]. In addition, other aging

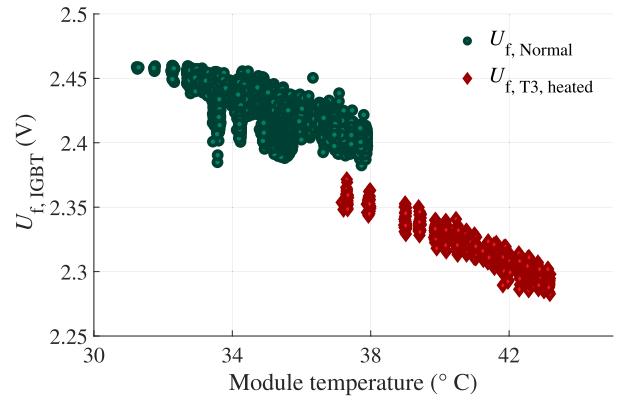


Fig. 19. Model results of the threshold voltage U_f when the IGBT chip T_3 is heated up.

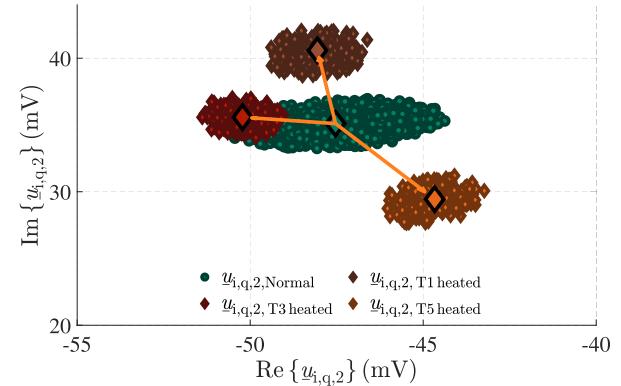


Fig. 20. Measurement results of the second harmonic of the integral component in the q -axis for the single chip heating.

mechanisms can in principle also be identified. All aging mechanisms that lead to the change of the investigated degradation indicators can be covered. One example is the heating of individual chips, which is the focus of this publication. In our previous publication [2], also the aging mechanism bond wire liftoff is considered by using the same method but investigating the mean value of the controller output variable.

However, it must be noted that the value calculated by the model does not necessarily have to correspond to the real, physical value. Due to many power converter effects that are not considered, such as turn-on and turn-off times, model inaccuracies result. Nevertheless, the value could be used as an indicator for certain aging mechanisms. Furthermore, the limits from which value of the threshold voltage the power converter is still considered functional and from which value the power converter must be replaced has to be determined by extensive field or laboratory tests. In addition, the second harmonic of the controller output is considered in the complex plane. In Fig. 20, the measurement results of the individual chip heating are evaluated. Unlike in the simulation, the normal behavior in the second harmonic already has a value that is not equal to zero. This is because there is an initial asymmetry in the system, which comes primarily from the passive load.

As the chips are heated up, a shift in the data cloud can be observed. The phase angles of the three upper IGBTs T_1 , T_3 , and T_5 show an angular difference of about 120° to

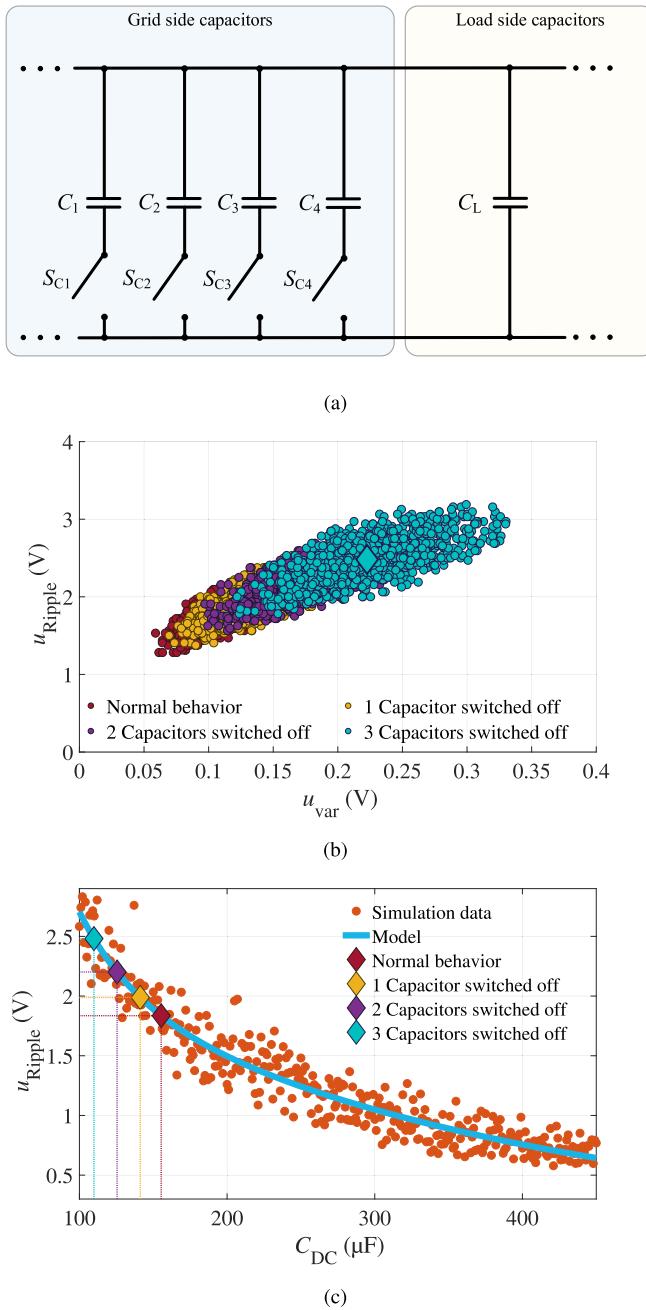


Fig. 21. Measurement and model results depending on the number of switched-OFF capacitors. (a) Block diagram of the switchable capacitors in the capacitor board. (b) Ripple and variance. (c) Model results when value of capacitance is reduced.

each other as also previously observed in the simulation in Fig. 16. Deviations in the angle may result from the fact that completely isolated heating of one chip is not possible in the practical example shown. Starting from the centers of the data clouds, difference vectors are identified, which calculates the shift of the initial data cloud. This allows to determine which power semiconductor chip is heated up.

B. DC-Link Capacitor

According to Fig. 21(a), the individual capacitors are switched OFF and the resulting effects are detected. The

changes that occur are recorded in the diagrams in Fig. 21(b). This diagram indicates that the ripple and the variance of the dc-link voltage increase as the number of connected capacitors decreases since it can be observed that the data cloud shifts toward higher ripples and variances. By calculating the robust Mahalanobis mean value for every data cloud and by inserting this value into the capacitor model of (25), a value of the capacitance can be calculated. The model is capable of detecting the decrease of the dc-link capacitance only by means of the dc-link voltage time waveform of Fig. 13(a).

As in Section VII-A explained, the calculated value of the capacitance may differ from the real value due to model inaccuracies. Still, the model is capable of detecting the decrease in the capacitance with the available data in converter operation. An outlook is to improve and optimize the model in order to get closer to the real value. This can be done, for instance, by including the effects of the digital-to-analog converter into the model to take the noise into account.

VIII. CONCLUSION

In this article, a new approach to condition monitoring of power electronic systems is presented. This approach does not require additional sensors and only uses data that are already available during operation. A complete approach is presented, including the aspects of data acquisition, preprocessing, and analysis. The publication focuses on the two power converter components: power semiconductor devices and dc-link capacitor. For these, the aging mechanisms and corresponding degradation indicators are determined. Subsequently, a power converter model is built, which includes these degradation indicators. This model is used to analyze the effects of the degradation indicators on the available data.

The overall converter test bench is presented. Afterward, the extension of the test bench is explained, which allows intentional implementation of failure cases at different levels. In Section VII, the failure devices are used to implement intentional modifications to the power converter system that represent specific failure mechanisms. Here, the results of the algorithm are evaluated.

For the detection of semiconductor failures, the output control variables of the control and their relevant harmonic oscillations are analyzed. Thereby, the multiples of the sixth harmonic are used. Mathematical models are created, which can calculate the failure severity based on these variables. Furthermore, by considering the second harmonic, it can be determined in which power semiconductor chip exactly the failure has occurred.

The same principle was applied to the dc-link capacitor component. Here, the time signal of the dc-link voltage was converted into a different representation form with ripple and variance. The mathematical model created can calculate capacitance changes of the dc-link capacitor during converter operation. One outlook is the further improvement and optimization of the converter model in order to bring the calculated degradation parameters closer to reality. This allows more accurate predictions of when an aging component needs to be replaced, which forms the basis of predictive maintenance.

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