## Instruction Set

Data Transf	er Ope	erations	byle <sup>5</sup>	oSperior
MOV A,Rn			1	1
MOV A,@Ri			1	2
MOV A,direc	t		2	2
MOV A,#data	a		2	2
MOV Rn,A			1	1
MOV Rn,dire	ct		2	2
MOV Rn,#da	ta		2	2
MOV direct, A	١.	move	2	2
MOV direct,F	₹n	IIIOVE	2	2
MOV direct,(	@Ri		2	2
MOV direct,c	lirect		3	3
MOV direct,#	data		3	3
MOV @Ri,A			1	2
MOV @Ri,di	rect		2	2
MOV @Ri,#d	lata		2	2
MOV DPTR,#			3	3
MOVC A,@A+	DPTR	move from	1	4
MOVC A,@A+	PC	code memory	1	4
MOVX A,@Ri			1	4
MOVX A,@DF	TR	move to/from	1	4
MOVX @Ri,A		data memory	1	4
MOVX @DPT			1	4
PUSH direct		push onto stack	2	2
POP direct		pop from stack	2	2
XCH A,Rn			1	1
XCH A,@Ri		exchange bytes	1	2
XCH A,direc			2	2
XCHD A,@Ri		exchg low digits	1	2

# Boolean Variable Manipulation of Section 1

CLR	С	clear bit to zero	1	1	ı
CLR	bit	clear bit to zero	2	2	ı
SETB	С	set bit to one	1	1	ı
SETB	bit	set bit to one	2	2	ı
CPL	С	complement bit	1	1	ı
CPL	bit	complement bit	2	2	ı
ANL	C,bit	AND bit with C	2	2	ı
ANL	C,/bit	AND (NOTbit) with C	2	2	ı
ORL	C,bit	OR bit with C	2	2	ı
ORL	C,/bit	OR (NOTbit) with C	2	2	ı
MOV	C,bit	move bit to bit	2	2	ı
MOV	bit,C	THOVE DIL IO DIL	2	2	

Progr	am Branchi	ng	byles	OS Period	55
ACALL	. addr11	call subroutine	2	3	
LCALL	addr16	call subroutine	3	4	
RET		return from sub.	1	4	
RETI		return from int.	1	4	
AJMP	addr11		2	3	
LJMP	addr16	iump	3	4	
SJMP	rel	Jump	2	3	
JMP	@A+DPTR		1	3	
JC	rel	jump if C set	2	3	
JNC	rel	jmp if C not set	2	3	
JB	bit,rel	jump if bit set	3	4	
JNB	bit,rel	jmp if bit not set	3	4	
JBC	bit,rel	jmp&clear if set	3	4	
JZ	rel	jump if A = 0	2	3	
JNZ	rel	jump if A not 0	2	3	
CJNE	A,direct,rel		3	4	
CJNE	A,#data,rel	compare and jump if not	3	4	
CJNE	Rn,#data,rel	ľ '	3	4	
CJNE	@Ri,#data,rel	equal	3	4	
DJNZ	Rn,rel	decrement and	2	3	
DJNZ	direct, rel	jump if not zero	3	4	ı
NOP		no operation	1	1	ı

## Arithmetic Operations

neuc Opera	lions	42	0.00
A,Rn		1	1
A,@Ri	add source to A	1	2
A,direct	add Source to A	2	2
A,#data		2	2
A,Rn		1	1
A,@Ri	add with corns	1	2
A,direct	add with carry	2	2
A,#data			2
A,Rn		1	1
A,@Ri	subtract from A	1	2
A,direct	with borrow	2	2
A,#data		2	2
Α		1	1
Rn		1	1
@Ri	increment	1	2
direct		2	2
DPTR *		1	3
Α		1	1
Rn	dooromont	1	1
@Ri	uecrement	1	2
direct		2	2
AB	multiply A by B	1	9
AB	divide A by B	1	9
Α	decimal adjust	1	2
	A,Rn A,@Ri A,direct A,#data A,Rn A,@Ri A,direct A,#data A,Rn A,QRi A,direct A,#data A,Rn A,@Ri A,direct A,#data A,Rn A,@Ri A,direct A,#data A Rn @Ri direct DPTR* A Rn @Ri direct DPTR* A A Rn @Ri direct DPTR* A A A B A B AB	A.@Ri A.direct A.#data A.Rn A.@Ri A.direct A.#data A.Rn A.@Ri A.@Ri A.direct A.#data A.Rn A.direct A.#data A.Rn A.direct A.#data A.rn A.ma A.ma A.ma A.ma A.ma A.ma A.ma A.ma	A,Rn

## \* INC DPTR increments the 24bit value DPP/DPH/DPL

Logical Operations

wiles Schools

Logic	ai Operatio	ns	10,1	0.40
ANL	A,Rn		1	1
ANL	A,@Ri		1	2
ANL	A,direct	logical AND	2	2
ANL	A,#data	logical AND	2	2
ANL	direct,A		2	2
ANL	direct,#data		3	3
ORL	A,Rn		1	1
ORL	A,@Ri		1	2
ORL	A,direct	logical OR	2	2
ORL	A,#data	logical OK	2	2
ORL	direct,A		2	2
ORL	direct,#data	1	3	3
XRL	A,Rn		1	1
XRL	A,@Ri		1	2
XRL	A,direct	logical XOR	2	2
XRL	A,#data	logical AOR	2	2
XRL	direct,A		2	2
XRL	direct,#data		3	3
CLR	Α	clear A to zero	1	1
CPL	Α	complement A	1	1
RL	Α	rotate A left	1	1
RLC	Α	through C	1	1
RR	Α	rotate A right	1	1
RRC	Α	through C	1	1
SWAP	Α	swap nibbles	1	1

## L agand

	Legena
Rn	register addressing using R0-R7
@Ri	indirect addressing using R0 or R1
direct	8bit internal address (00h-FFh)
#data	8bit constant included in instruction
#data16	16bit constant included in instruction
bit	8bit direct address of bit
rel	signed 8bit offset
addr11	11bit address in current 2K page
addr16	16bit address
v	any of: Pn @Pi direct #data

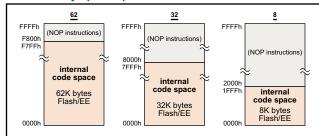
## Instructions That Affect Flags

ADD A,x	C = carry out of bit 7	DA A	C = C or (x>100)
	AC = carry out of bit 3 OV = carry out of bit 6, but not 7	RRC A	C = ACC.7
ADDC Av	C = carry out of bit 7	RLC A	C = ACC.0
ADDC A,X	AC = carry out of bit 3	SETB C	C = 1
	OV = carry out of bit 6, but not 7	CLR C	C = 0
SUBB A,x	C = borrow into bit 7	ANL C,bit	C = C and bit
	AC = borrow into bit 3 OV = borrow into bit 6, but not 7	ANL C,/bit	C = C and NOTbit
		ORL C,bit	C = C or bit
MUL AB	C = 0 OV = (result>255)	ORL C,/bit	C = C or NOTbit
DIV AB	C = 0	MOV C,bit	C = bit
	OV = divide by zero	CJNE x,y,rel	C = (x <y)< td=""></y)<>

## **Pin Functions**

FII		inctions									
MO	ે તુક						٥				
1	56	P1.0 / ADC0 / T2						기니니 2 전 설		3444444	
2	1	P1.1 / ADC1 / T2EX					Щ	Ш			
3	2	P1.2 / ADC2	_	0	ನ ಚಿತ್ರವಾಗಿ ೨೦೦೦ – pin 1 id	7 4 5 4 5 4 7 1	0	<b>←</b>	pin 1 ic	ientifier	$=$ $\frac{3}{3}$
4	3	P1.3 / ADC3				0 41 3 E			D(	C842	
5	4,5	AV <sub>DD</sub>	5 D		ADuC 56pin	2842				MQFP	=
6	6,7,8	AGND	3 4 5 6 6 7 6 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		TOP V	/IEW 35 7 ==				viQi F √IEW	
7	9	CREF	12 🛈	(1	not to	32 9 31 10 Sealer				scale)	
8	10	VREF	13 D 14 D			30 10 11 12 12 12 12 12 12 12 12 12 12 12 12		(		,	
9	11	DAC0	5	44	22828	13					$\equiv$
10	12	DAC1				'	П	Ш			•
11	13	P1.4 / ADC4					4 4	5 6 7	: # f	222222	
12	14	P1.5 / ADC5 / SS									
13	15	P1.6 / ADC6		MOF	રે દુકર			MOE	<sup>ર</sup> ુક		
_										I <del></del>	
14	16	P1.7 / ADC7	l F	27	29	SDATA / MOSI		40	43	ĒĀ	
15	17	RESET	1	28	30	P2.0 / A8 / A16		41	44	PSEN	
16	18	P3.0 / RxD		29	31	P2.1 / A9 / A17		42	45	ALE	
17	19	P3.1 / TxD		30	32	P2.2 / A10 / A18		43	46	P0.0 / AD0	
18	20	P3.2 / INT0	٤	31	33	P2.3 / A11 / A19		44	47	P0.1 / AD1	
19	21	P3.3/INT1/MISO/PWM1		32	34	XTAL1 (in)		45	48	P0.2 / AD2	
20	22	DV <sub>DD</sub>		33	35	XTAL2 (out)		46	49	P0.3 / AD3	
21	23	DGND	:	34	36	DVDD		47	50	DGND	
22	24	P3.4 / T0 / PWMC / PWM0 / EXTCLK	:	35	37,38	DGND		48	51	DV <sub>DD</sub>	
23	25	P3.5 / T1 / CONVST		36	39	P2.4 / A12 / A20		49	52	P0.4 / AD4	
24	26	P3.6 / WR		37	40	P2.5 / A13 / A21		50	53	P0.5 / AD5	
25	27	P3.7 / RD	[	38	41	P2.6/A14/A22/PWM0		51	54	P0.6 / AD6	
26	28	SCLOCK		39	42	P2.7/A15/A23/PWM1		52	55	P0.7 / AD7	
			_	_							

## **Code Memory Space Options**



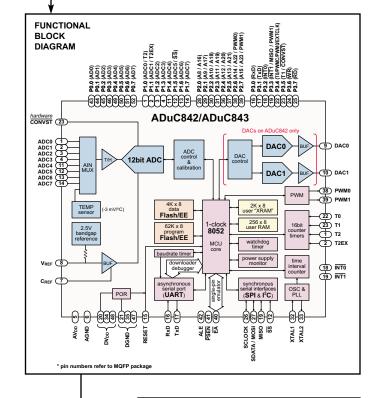
## **Interrupt Vector Addresses**

Interrupt Bit	Interrupt Name	Vector Address	Relative Priority
PSMCON.5	Power Supply Monitor Interrupt	43h	1
WDS	WatchDog Timer Interrupt	5Bh	2
IE0	External Interrupt 0	03h	3
ADCI	End of ADC Conversion Interrupt	33h	4
TF0	Timer0 Overflow Interrupt	0Bh	5
IE1	External Interrupt 1	13h	6
TF1	Timer1 Overflow Interrupt	1Bh	7
ISPI/I2CI	SPI/I <sup>2</sup> C Interrupt	3Bh	8
RI/TI	UART Interrupt	23h	9
TF2/EXF2	Timer2 Interrupt	2Bh	10
TIMECON.2	Time Interval Counter Interrupt	53h	11

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## ADuC842/843 MicroConverter® **Quick Reference Guide**



## A Precision Analog Flash MCU

## The ADuC842/ADuC843 is:

12bit, 5µs, 8channel, self calibrating 0.5LSB INL & 70dB SNR

DAC (ADuC842 only): dual, 12bit,15µs, voltage output <1LSB DNL

## Flash/EEPROM:

62K bytes Flash/EE program memory 4K bytes Flash/EE data memory

## Microcontroller:

"single-cycle" 8052, up to 16.8MIPS 32 I/O lines, programmable PLL clock (131KHz to 16.8MHz from 32KHz crystal)

## Embedded Tools Support:

on-chip download/debug & single-pin emulation functions

## Other on-chip features:

temperature monitor, power supply monitor, watchdog timer, flexible serial interface ports, voltage reference. time interval counter, dual 8/16bit PWM, power-on-reset





ata Memory: RAM, SF	Rs, user Flash/EE (all read/write)	SFR Map
address address	Lower RAM	(reserved)  SPIDAT ADCCON1 EFN 00h (reserved) PSMCON DFN DEN DFN DEN CTN 00h EADRH CTN 00h EADRH CTN 00h EADRA BFN 00h CFG842 AFN 00h (rot used) (rot used) (reserved)  FCON ATN 00h ATN 00h ATN 00h BTN 00h CFG842 AFN 00h ATN 00h BTN 00h ATN 00h AT
27 7Fh General Purpose Area	Sept (bit addresses)	(reserved) (rot used) (rot used) (rot used) (rot used) (rot used) (reserved)
6 2Eh 5 2Dh 4 2Ch	7Fh         7Eh         7Dh         7Ch         7Bh         7Ah         79h         78h           77h         76h         75h         74h         73h         72h         71h         70h           6Fh         6Eh         6Dh         6Ch         6Bh         6Ah         69h         68h           67h         66h         65h         64h         63h         62h         61h         60h	DACCON ABDCCONS ABDCCONS (reserved) (rot used)
2 2Ah 2 29h 3 29h 5 28h 8 Bit Addressable Area	5Fh         5Eh         5Dh         5Ch         5Bh         5Ah         59h         58h           57h         56h         55h         54h         53h         52h         51h         50h           4Fh         4Eh         4Dh         4Ch         4Bh         4Ah         49h         48h           47h         46h         45h         44h         43h         42h         41h         40h	PDACTH ADD CGAINH FAD (TESENVED) (TESENVED) DDMAP DDMAP DDMAP DDMAP OTH CCD ODN (TESENVED) (TO ODN (TO USED) (TO USED) (TO USED) (TO USED) GAT ODN GAT OTN GAT
9 27h 3 26h 7 25h 6 24h	3Fh 3Eh 3Dh 3Ch 3Bh 3Ah 39h 38h 37h 36h 35h 34h 33h 32h 31h 30h 2Fh 2Eh 2Dh 2Ch 2Bh 2Ah 29h 28h 27h 26h 25h 24h 23h 22g 21h 20h	PDACTL ADCGAINL ADCGAINL ADCGAINL (reserved) (reserved) DDMAH DDMAH CBN ON (reserved) (r
5 23h 4 22h 3 21h 2 20h	1Fh 1Eh 1Dh 1Ch 1Bh 1Ah 19h 18h 17h 16h 15h 14h 13h 12h 11g 10h 0Fh 0Eh 0Dh 0Ch 0Bh 0Ah 09h 08h 07h 06h 05h 04h 03h 02h 01h 00h	DACOH   On ADCOT   O
1 1Fh R7 0 1Eh R6 9 1Dh R5 3 1Ch R4 7 1Bh R3 6 1Ah R2 5 19h R1	Flash/EE data space (*XRAM)" extended RAM space	SPICON   DACOL   F8h
6 10h R0 6 0Fh R7 1 0Eh R6 3 0Dh R5 2 0Ch R4 1 0Bh R3 0 0Ah R2 09h R1 08h R0 07h R7 06h R6	sper RAM (direct addressing only)  128 bytes lower RAM (direct or indirect	Feb. 0   F
05h R5 04h R4 03h R3 02h R2 01h R1 00h R0	AM SED datails	HEN OF BANK AND

MDC master mode SDATA output bit   MDC master mode SDATA input b		
ADCOCHI 2 ADC Control register #2 ADCOCHI 3 acquainto managed that   Fig. 1, 8, 2   ADCOCHI 3 acquainto managed that   Fig. 1, 8, 2   ADCOCHI 3 acquainto managed that   Fig. 1, 8, 2   ADCOCHI 3 acquainto managed that   Fig. 1, 8, 2   ADCOCHI 4 ADC Control register #2 ADC ADC Sorrors flag	ADCCON1 ADC Control register #1	T3FD Timer 3 Fractional Divider register
ADCCON2 ADC Control register #2 ADCCON2 ADC Control register #3 ADCCON2 Bit 15 3 4 237 Bit 15 3 4 2		
ADCCON2 ADC Control register #2 ADCCON3 ADC Control register #3 ADCCON3 ADCCON3 ADC Control register #3 ADCCON3 ADCCON3 ADCCON4 ADCCON3 ADCCON4 ADCCON	ADCCON1.6 external Vref select bit (0=on-chip Vref) ADCCON1.5 conversion time = 16 / ADCclk	CHIPID Chip ID Register (AX hex = ADirC842/843)
ACCOMP and CONTRO register #2  ACCOMP ADC CONTRO register #2  ACCOMP ADC CONTRO register #3  ACCOMP ADC CONTRO register #4  ACCOMP ADD REGISTER AD		
ADCCON2 ADC Cortrol register #2  FOR STATE ADC CAND. ADC Cortrol register #3  ADCCON3 To be a first from the property of the p	ADCCON1.2 acq time = [1,2,3,4] / ADCclk ADCCON1.1 Timer2 convert enable	CFG842.7 extended stack-pointer enable (0=disable)
DAY, DAY, mode enable of the control register of the c	ADCCON2 ADC Control register #2	CFG842.6 PWM pins select (0=P2.6/P2.7,1=P3.4/P3.3) CFG842.5 DAC output buffer bypass (0=buffer enabled)
DOWN PROMOTE CONTROL (1997)  DOWN PROMOTE CON	ADCI ADC interrupt floor	
## STATE OF THE PROPERTY OF TH	DMA DMA mode enable CCONV continuous conversion enable bit	CFG842.2 (this bit must contain 0) CFG842.1 select SPI pins (0=default, 1=P3.3/P3.4/P3.5)
## COUNTY ADD CONTROL (PACE)  ## COU	SCONV single conversion start bit	CFG842.0 internal XRAM select (0=external XRAM)
ADCCONS ADC Control register #3 ADCCONS 2 miles resident plant products from plant p	CS2 0 - 7 = ADC0 - ADC7 CS1 8 = temperature sepsor	WDCON Watchdog Timer control register
ADCCOMUSE of the control of the cont	CS0 9=DAC0, A=DAC1, B=AGND, C=VREF	PRE2 0-7=[15.6,31.2,62.5,125,250,500,1000,2000]ms
ADCCOMUSE of the control of the cont		PRE0 >8=reserved
ADCOATAH ADCOATAH ADC Data registers  DMAP, DMAH, DMAH, DMAH, DMA address pointer ADCOATAH ADC Call and address pointer ADCOATAH ADC Call And address pointer ADCOATAH ADC Call And Calleralin coefficients Calleralin coeffic		WDS watchdog status flag (1 indicates watchdog timeout
ADCOATAH ADCOATAH ADC Data registers  DMAP, DMAH, DMAH, DMAH, DMA address pointer ADCOATAH ADC Call and address pointer ADCOATAH ADC Call And address pointer ADCOATAH ADC Call And Calleralin coefficients Calleralin coeffic	ADCCON3.5 number of averages selection bits: ADCCON3.4 [15,1,31,63]	WDWR watchdog write enable bit (set to enable write)
ADCDATAH ADCDATAH ADCDATAH ADCDATAH ADCORD ADCGAINL Calibration coefficients ADCGAINL ADCGAIN	ADCCON3.3 (this bit must contain zero) ADCCON3.2 (this bit must contain one when calibrating)	. emeet i owe cappiy monto control egister
ADCDATAH ADCDATAH ADCDATAH ADCDATAH ADCORD ADCGAINL Calibration coefficients ADCGAINL ADCGAIN	ADCCON3.1 cal type select (0=offset, 1=gain) ADCCON3.0 start calibration bit, cleared by hardware	PSMCON 5 PSM interrupt bit
DMAP, DMAH, DMA address pointer  ADCGAINH ADC Gain ADCGAIN ADC Great ADCOPSH ADCOPSH Calibration coefficients  DACON DAC Cortical register  DACCON BOAC Cortical register DACCON DACE Control register DACCON DATE TRANSPER CONTROL REGIster DACCON DATE TRANSPER CONTROL REGIster DACE CONTROL REGISTER DACE DATE CONTROL REGISTER DATE CONTROL RE	ADCDATAH	PSMCON.3 [(reserved), 3.08V, 2.93V, (reserved)]
ADCGAIN. ADCGAIN. ADCORSI. ADC	ADCDATAL ADC Data registers	PSMCON.1 (reserved)
ADCGAIN! ADC Gain acidifration coefficients and process of the control of the company of the com	DMAP,DMAH,DMAL DMA address pointer	
ADCOFAIL ADCOFISI ADCOMORIS Calibration coefficients DACCON D AC Control register DACCON DAC Control register DACCON BACCONT (Control register DACCON DAC Control register DACCON DAC EngrageSer (I respective consultation of the control register (I respective con		
ADCORS ACCONT Calibration coefficients calibrated calibration coefficients calibrated cal		
DACCON 1 DACCON 2 DACCON 3 DACCON 3 DACCON 3 DACCON 4 DACCON 4 DACCON 4 DACCON 4 DACCON 4 DACCON 4 DACCON 5 DACCON 5 DACCON 5 DACCON 5 DACCON 6 DACCON 6 DACCON 6 DACCON 6 DACCON 7 DACCON 7 DACCON 7 DACCON 7 DACCON 7 DACCON 7 DACCON 8 DACCON 8 DACCON 8 DACCON 8 DACCON 9 DAC	ADCOFSH ADC Offeet	IE Interrupt Enable register #1
DACCON1 DOCCON1 DOCCON		EADC enable ADCI (ADC interrupt)
DACCON1 DOCCON1 DOCCON	DAGGON PLOS III	ES enable RI/TI (serial port interrupt)
DACCON1 DOCCON1 DOCCON	DACCON.7 ModeSelect (0=12bit, 1=8bit)	EX1 enable IE1 (External interrupt 1)
DACCON1 DOCCON1 DOCCON	DACCON.6 DAC1 RangeSelect (0=V <sub>REF</sub> , 1=V <sub>DD</sub> ) DACCON.5 DAC0 RangeSelect (0=V <sub>REF</sub> , 1=V <sub>DD</sub> )	EX0 enable IE0 (External interrupt 0)
DACOH_DACOL_DACOL DACO data registers  PLLCON P.L Control register  PLLCON P.P Control register  PLAN P. POWER P	DACCON.4 Clear DAC1 (0=0V, 1=normal operation) DACCON.3 Clear DAC0 (0=0V, 1=normal operation)	IEIP2 Interrupt Enable/Priority register #2
DACOH_DACOL_DACOL DACO data registers  PLLCON P.L Control register  PLLCON P.P Control register  PLAN P. POWER P	DACCON.2 SynchronousUpdate (1=asynchronous) DACCON.1 PowerDown DAC1 (0=off, 1=on)	IEIP2.6 priority of TII interrupt (time interval) IEIP2.5 priority of PSMI interrupt (power supply monitor)
DACOH_DACOL_DACOL DACO data registers  PLLCON P.L Control register  PLLCON P.P Control register  PLAN P. POWER P	DACCON.0 PowerDown DACO (0=off, 1=on)	IEIP2.4 priority of ISPI interrupt (serial interface) IEIP2.3 (this bit must contain zero)
PLLCON PLLCON PLLCON Secular prevention control bit (Po-XTAL or) PLLCON	DACTH,DACTL DACT data registers	IEIP2.2 enable TII interrupt (time interval) IEIP2.1 enable PSMI (power supply monitor interrupt)
PLICON 3 PLI		IEIP2.0 enable ISPI interrupt (serial interface)
PLLCONS PLLCONS PLLCONS PLLCONS PLCCONS PLCCON		IP Interrupt Priority register
PLUCON 3 PLUCON 3 PLUCON 5 PLUCON 5 PLUCON 5 PLUCON 5 PLUCON 5 PLUCON 6 PLUCON 6 PLUCON 6 PLUCON 7 PLUCON 7 PLUCON 7 PLUCON 7 PLUCON 7 PLUCON 8 PLUCON 8 PLUCON 8 PLUCON 8 PLUCON 8 PLUCON 8 PLUCON 9 PLUCON 8 PLUCON 9 PLU	PLLCON./ oscillator powerdown control bit (0=XTAL on) PLLCON.6 PLL lock indicator flag (0=out of lock)	PT2 priority of TF2/EXF2 (Timer2 overflow interrupt) PS priority of RI/TI (serial port interrupt)
TIMECON 5 sh-how mode select (IP-0 255hour, 1-0. 23hour) TIMECON 5 sh-how mode select (IP-0 255hour, 1-0. 23hour) TIMECON 1 (128h) see, secondos, minutes, hours, 17th (IP-0 128h) see, secondos (IR-0 128hour, 1900, 19	PLLCON.5 (this bit must contain zero) PLLCON.4 (this bit must contain zero)	PT1 priority of IF1 (Timer1 overflow interrupt) PX1 priority of IF1 (expense interrupt 1)
TIMECON 5 sh-how mode select (IP-0 255hour, 1-0. 23hour) TIMECON 5 sh-how mode select (IP-0 255hour, 1-0. 23hour) TIMECON 1 (128h) see, secondos, minutes, hours, 17th (IP-0 128h) see, secondos (IR-0 128hour, 1900, 19	PLLCON.3 "fast interrupt" control bit (0=normal) PLLCON.2 3-bit clock divider value, "CD" (default=3):	PT0 priority of IF0 (External interrupt) PX0 priority of IF0 (external interrupt 0)
TIMECON 5 and the control Control Register TIMECON 5 Action most series (Pol-258hour.) 1-0.23hour) TIMECON 5 INTVAL timebase select bits. (Pol-17 (1994) 1-1.04 (1994) 1-1	PLLCON.1 FCORE = 16,777,216Hz / 2 <sup>CD</sup>	TMOD Timer Mode register
TIMECON.1 time direvier entable bit (0-disable) TIMECON.0 time clock enable clock enable (0-disable) TIMECON.0 time clock enable bit (0-disable) TIMECON.0 time clock enable clock enable (0-disable) TIMECON.0 time clock enable clock enable (0-disable) TIMECON.0 time clock enable (0-disable) TIMECON.0 t	TIMECON Time Interval Counter Control Register	TMOD.3/.7 gate control bit (0=ignore INTx)
TIMECON.1 time direvier entable bit (0-disable) TIMECON.0 time clock enable clock enable (0-disable) TIMECON.0 time clock enable bit (0-disable) TIMECON.0 time clock enable clock enable (0-disable) TIMECON.0 time clock enable clock enable (0-disable) TIMECON.0 time clock enable (0-disable) TIMECON.0 t	TIMECON.6 24-hour mode select (0=0255hour, 1=023hour)	TMOD.2/.6 counter/timer select bit (0=timer) TMOD.1/.5 timer mode selecton bits
Tricle   Tic   Language   Tic   Language   Tic   Language   Lang	TIMECON.4 [128th sec, seconds, minutes, hours] TIMECON.3 single time interval control bit (0=reload&restart)	(upper nibble = Timer1, lower nibble = Timer0)
Tricle   Tic   Language   Tic   Language   Tic   Language   Lang	TIMECON.2 time interval interrupt bit, "TII"  TIMECON 1 time interval enable bit (0=disable&clear)	TCON Timer Control register
HOUR TIC Elapsed Hours Register  Data Flash/EE comand register  Of PROGRAP and September of Processing of Processing September	TIME COOK CHADIC DK (O-GISLIDIC)	TF1 Timer1 overflow flag (auto cleared on vector to ISR) TR1 Timer1 run control (0=off, 1=run)
HOUR TIC Elapsed Hours Register  Data Flash/EE comand register  Of PROGRAP and September of Processing of Processing September	INTVAL TIC Interval Register	TF0 Timer0 overflow flag (auto cleared on vector to ISR)
HOUR TIC Elapsed Hours Register  Data Flash/EE comand register  Of PROGRAP and September of Processing of Processing September		IE1 external INT1 flag (auto cleared on vector to ISR)
HOUR TIC Elapsed Hours Register  Data Flash/EE comand register  Of PROGRAP and September of Processing of Processing September		IEO external INTO flag (auto cleared on vector to ISR)
ECON Data FlashVEE comand register Oth READ page 20th PROGRAM byte 20th READ page 20th PROGRAM byte 20th REAS page 20th READ page 30th READ p		TH0.TL0 Timer0 registers
Data Flash/EE comand register  Oh READ page 6th PENCRAM by mode of the READ page 7th PENCRAM page 1th PENCR	-	
Odh KERY Page 6th ENSTER LLOAD dock 6th ERASE ALL  EARTH_EADRL  EARTH_EADRL  Data FlashVEE address registers  EDATA1, EDATA2, EDATA3, EDATA4  Data FlashVEE data registers  SPICON  SPI Control register  SPICON  SPI Control register  SPICON  SPI Control register  SPICON  SPI Control (nest), 1-40 (nest)  CPC clock polarity select (0+SCLK idea low)  CPC clock polarity select (16+SCLK idea low)  SPINA  SPID SPIN SPID SPID SPID SPICE (16+SCLK idea low)  SPICON  SPI Control register (nest)  SPICON  Modern master mode select bit (0-siave mode)  IZCON  IZC	ECON Data Flash/EE comand register	<u> </u>
BPICON SPI Control register  SPICON SPI Control register  Intercept (see by hardware at end of SPI transfer)  SPICON SP	02h PROGRAM page 0Fh EXIT ULOAD mode	TF2 overflow flag
BPICON SPI Control register  SPICON SPI Control register  Intercept (see by hardware at end of SPI transfer)  SPICON SP	05h FRASE page (all others reserved)	EXF2 external flag
BPICON SPI Control register  SPICON SPI Control register  Intercept (see by hardware at end of SPI transfer)  SPICON SP	06h FRASE ALL	RCER Teceive clock enable (0=1inter Lased for RXD clk)
SPICON SPI Control register  SPICON SPI Control register  SPI interrupt (set by hardware at end of SPI transfer)  SPI SPI interrupt (set by hardware at end of SPI transfer)  SPI SPI interrupt (set by hardware at end of SPI transfer)  SPI SPI interrupt (set by hardware at end of SPI transfer)  SPI SPI SPI interrupt (set by hardware at end of SPI transfer)  SPI		TCLK transmit clock enable (0=Timer1 used for TxD clk) EXEN2 external enable (0=ignore T2EX, 1=cap/rld on T2EX)
SPICON SPI Control register	EADRH,EADRL Data Flash/EE address registers	TCLK transmit clock enable (0=finer1 used for TXD clk) EXEN2 external enable (0=finer1 used for TXD clk) EXEN2 run control (0=stop., 1=run) CNT2 timer/counter select (0=timer, 1=counter)
Portion register (also A0-A7 & Do-D7)	EADRH,EADRL Data Flash/EE address registers EDATA1,EDATA2,EDATA3,EDATA4	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capture/reload select (0=reload, 1=capture)
SPE SPI enable (self-C enable, 1-SP) enable) SPE Description of the SCACK idles low) CPHA clock phase select (0-leading edge latch) SPRO biffate = Frome (12,48,16) ( elaves SPRO+SS) SPIDAT SPI Data register  I2CCON 1°C Control register (in slave mode) 12CCID state = Frome (12,48,16) (elaves SPRO+SS) 12CCID state = Frome (12,48,16) (elaves SPRO+SS) SPIDAT SPI Data register  I2CCON 1°C Control register (in slave mode) 12CCID state = Frome (12,48,16) (elaves mode) 12CCON state = F	EADRH,EADRL Data Flash/EE address registers EDATA1,EDATA2,EDATA3,EDATA4 Data Flash/EE data registers SPICON SPI Control register	CNT2 timer/counter select (0=timer, 1=counter) capture/reload select (0=reload, 1=capture)  TH2,TL2 Timer2 register
SPIDAT   SPI Data register   In Stave mode    12CSD   Select mode   SPIDAT   SPIDAT    12CSD   Select mode of the interrupt enable bit (Ordinable)    12CSD   Select mode of the interrupt decode bits    12CSD   Select mode of the interrupt    12CSD   Select mode   SPIDAT   SPIDAT    12CSD   Select mode   SPIDAT   SPIDAT   SPIDAT    12CSD   Select mode   SPIDAT   SPIDAT   SPIDAT   SPIDAT   SPIDAT    12CSD   SPIDAT	EADRH,EADRL Data Flash/EE address registers  EDATA1,EDATA2,EDATA3,EDATA4  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer)	CNT2 CAP2 TH2,TL2 Timer/counter select (0*etimer, 1*ecounter) TH2,TL2 Timer/counter select (0*etimed, 1*ecapture) TH2,TL2 Timer/counter select (0*etimed, 1*ecapture) Timer/counter select (0*etimed, 1*ecapture) Timer/counter select (0*etimed, 1*ecapture)
SPIDAT   SPI Data register   In Stave mode    12CSD   Select mode   SPIDAT   SPIDAT    12CSD   Select mode of the interrupt enable bit (Ordinable)    12CSD   Select mode of the interrupt decode bits    12CSD   Select mode of the interrupt    12CSD   Select mode   SPIDAT   SPIDAT    12CSD   Select mode   SPIDAT   SPIDAT   SPIDAT    12CSD   Select mode   SPIDAT   SPIDAT   SPIDAT   SPIDAT   SPIDAT    12CSD   SPIDAT	EADRH,EADRL Data Flash/EE address registers  EDATA1,EDATA2,EDATA3,EDATA4  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer)	CNT2   timer/counter select (0=timer, 1=counter)   CAP2
SPIDAT   SPI Data register   In Stave mode    12CSD   Select mode   SPIDAT   SPIDAT    12CSD   Select mode of the interrupt enable bit (Ordinable)    12CSD   Select mode of the interrupt decode bits    12CSD   Select mode of the interrupt    12CSD   Select mode   SPIDAT   SPIDAT    12CSD   Select mode   SPIDAT   SPIDAT   SPIDAT    12CSD   Select mode   SPIDAT   SPIDAT   SPIDAT   SPIDAT   SPIDAT    12CSD   SPIDAT	EADRH,EADRL Data Flash/EE address registers  EDATA1,EDATA2,EDATA3,EDATA4  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer)	CNT2
PCON   C Control register (in slave mode)	EADRH,EADRL Data Flash/EE address registers  EDATA1,EDATA2,EDATA3,EDATA4  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer)	CNT2
Secondary State Mode stop interrupt enable bit (0-disable)   Secondary State Mode   Secon	EARRH,EADRL Data Flash/EE address registers  EDATA1,EDATA2,EDATA3,EDATA4  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer)  SPE SPI enable (GPI-C enable, 1=SPI enable)  SPIM master mode select (0=slave)  CPU, clock polarly select (0=slave)  SPIM SPI bitrate select bits  SPRO bitrate select bits  SPRO bitrate select bits  SPRO bitrate select bits	CNT2
master mode select bit (0=stove mode) IZCRS errial port reset IZCRS errial port reset IZCRS errial port reset IZCRS errial port reset error port port port port port port port	EADRH,EADRL Data Flash/EE address registers  EDATA1, EDATA2, EDATA3, EDATA4  Data Flash/EE data registers  SPICON SPI Control register  SPI SPI interrupt (set by hardware at end of SPI transfer)  WCDL with collision error file. 1 nSPI enable)  SPIM master mode select (0 nslave)  CPHA clock phate select (0 nslave)  CPHA clock phate select (0 nslave)  SPRO bittise = FCome (1/2,48,16) (slave: SPRO=SS)  SPIDAT SPI Data register	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capturerleads elect (0=timer, 1=counter) CAP2 capturerleads elect (0=timed, 1=capture) TH2,TL2 Timer2 register RCAP2H,RCAP2L Timer2 Reload/Capture P0 Port0 register (also A0-A7 & D0-D7) P1 Port1 register (also A0-A7 & D0-D7) P2 Port1 register (analog & digital inputs) TZEX timer/counter 2 capture/reload trigger TP2 Port1 register (also A8-A15 & A16-A23) P3 Port3 register P3 Port3 register
master mode select bit (0=stove mode) IZCRS errial port reset IZCRS errial port reset IZCRS errial port reset IZCRS errial port reset error port port port port port port port	EARRH,EADRL Data FlashVEE address registers  EDATA1, EDATA2, EDATA3  Data FlashVEE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer)  WCOL write collision error flag  WCOL by the collision error flag  SPIM material (or salve)  CPOL clock polarity select (0r-SCLK ides low)  CPOL clock polarity select (0r-SCLK ides low)  SPIM material (or SCLK ides low)  SPIM SPIM select (0r-SCLK ides low)  SPIM select (0r-SCLK ides low)  SPIM SPIM sel	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capturerleads elect (0=timer, 1=counter) CAP2 capturerleads elect (0=timed, 1=capture) TH2,TL2 Timer2 register RCAP2H,RCAP2L Timer2 Reload/Capture P0 Port0 register (also A0-A7 & D0-D7) P1 Port1 register (also A0-A7 & D0-D7) P2 Port1 register (analog & digital inputs) TZEX timer/counter 2 capture/reload trigger TP2 Port1 register (also A8-A15 & A16-A23) P3 Port3 register P3 Port3 register
In the control of the control register	EARRH,EADRL Data FlashVEE address registers  EDATA1, EDATA2, EDATA3  Data FlashVEE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer)  WCOL write collision error flag  WCOL by the collision error flag  SPIM material (or salve)  CPOL clock polarity select (0r-SCLK ides low)  CPOL clock polarity select (0r-SCLK ides low)  SPIM material (or SCLK ides low)  SPIM SPIM select (0r-SCLK ides low)  SPIM select (0r-SCLK ides low)  SPIM SPIM sel	CNT2 timer/counter select (0-timer, 1-counter) CAP2 capturerlead select (0-timer, 1-counter) CAP2 timer/counter select (0-timed, 1-capture) TH2,TL2 Timer/2 register RCAP2H,RCAP2L Timer/2 register PO Port0 register (also A0-A7 & D0-D7) P1 Port1 register (also A0-A7 & D0-D7) T2EX T2EX timer/counter 2 expurier/lead triper/counter 2 expurier/lead triper/counter 2 external input P2 Port3 register (also A0-A7 & A16-A23) P3 Port3 register RD external data memory write strobe timer/counter 1 external input
IZCON   PC Control register (in master mode)	EARH,EADRL Data Flash/EE address registers  EDATA1,EDATA2,EDATA3  Data Flash/EE data registers  SPICON SPICONTOI register  SPICON SPICONTOI register (Include SPICONTOI REGISTER (Include SPICONTOI SPICONTO	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capturerlead select (0=reinad, 1=capture) TH2,TL2 Timer/2 register RCAP2H,RCAP2L Timer/2 Reload/Capture P0 Port0 register (also A0-A7 & D0-D7) P1 Port1 register (analog & digital inputs) T2EX timer/counter 2 capture/reload trigger T2 timer/counter 2 capture/reload trigger P2 Port2 register (also A8-A1 & A1 &
mode master mode SDATA output bit MDE master mode SDATA output shall (0-disable) mode master mode SDATA output shall (0-disable) mode mode mode state mode sDATA input bit MDI master mode SDATA input bit MDI master mode SDATA input bit MDI master mode selbs to the mode) mode mode mode state mode selbs to the mode mode mode mode mode mode mode mod	EARRH,EADRL Data FlashVEE address registers  EDATA1, EDATA2, EDATA3, EDATA4  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer)  WCDU write collision error flag  SPIM mater mode select floresizety (press to the collision of the colli	CNT2 timer/counter select (0-timer, 1-counter) CAP2 captipure/lead select (0-timer, 1-counter) CAP2 timer/counter select (0-timer, 1-counter) CAP2 timer/counter (2-timer) PO Port0 register (also A0-A7 & D0-D7) P1 Port1 register (also A0-A7 & D0-D7) P2 Port2 register (also A0-A7 & D0-D7) P2 Port2 register (also A0-A7 & A10-A23) P3 Port3 register RD external data memory write strobe timer/counter 2 external input RD external data memory write strobe timer/counter (2-timer) RD external data memory write strobe timer/counter (2-timer) RD external data memory write strobe timer/counter (2-timer) RD external input RD exter
IZCADD   FC slave Address register	EARRH,EADRL Data Flash/EE address registers  EDATA1, EDATA2, EDATA3  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer) WCOL write collision error flag  SPE SPI entable (In-PC entable, 1-SPI entable)  CPOL clock polarity select (Or-SCLK, idea low)  CPOL clock polarity select (Or-SCLK, idea low)  CPOL clock polarity select (Or-SCLK, idea low)  SPIDAT SPI Data register  IZCON I'C Control register (in slave mode)  IZCSI slave mode stop interrupt entable bit (In-disable)  IZCSI slave mode stop interrupt entable bit (In-disable)  IZCSI slave mode interrupt decode bits  IZCSI slave mode interrupt mode)	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capturerleads elect (1=timer) PO port0 register (also A0-A7 & D0-D7) P1 port1 register (also A0-A7 & D0-D7) P1 port1 register (analog & digital inputs) T2EX timer/counter 2 external input P2 port2 register (also A8-A15 & A16-A23) P3 port3 register R0 esternal data memory read strobe R1 timer/counter 1 external input T1 timer/counter 1 external input T1 timer/counter 0 external input T2 SECON Serial communications Control register
IZCADD   FC slave Address register	EARRH,EADRL Data Flash/EE address registers  EDATA1, EDATA2, EDATA3  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer) WCOL write collision error flag  SPE SPI entable (In-PC entable, 1-SPI entable)  CPOL clock polarity select (Or-SCLK, idea low)  CPOL clock polarity select (Or-SCLK, idea low)  CPOL clock polarity select (Or-SCLK, idea low)  SPIDAT SPI Data register  IZCON I'C Control register (in slave mode)  IZCSI slave mode stop interrupt entable bit (In-disable)  IZCSI slave mode stop interrupt entable bit (In-disable)  IZCSI slave mode interrupt decode bits  IZCSI slave mode interrupt mode)	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capturerleads elect (1=timer) PO port0 register (also A0-A7 & D0-D7) P1 port1 register (also A0-A7 & D0-D7) P1 port1 register (analog & digital inputs) T2EX timer/counter 2 external input P2 port2 register (also A8-A15 & A16-A23) P3 port3 register R0 esternal data memory read strobe R1 timer/counter 1 external input T1 timer/counter 1 external input T1 timer/counter 0 external input T2 SECON Serial communications Control register
IZCADD1, IZCADD2, IZCADD3   FC secondary slave Address registers	EARRH,EADRL Data Flash/EE address registers  EDATA1, EDATA2, EDATA3  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer) WCOL write collision error flag  SPE SPI entable (In-PC entable, 1-SPI entable)  CPOL clock polarity select (Or-SCLK, idea low)  CPOL clock polarity select (Or-SCLK, idea low)  CPOL clock polarity select (Or-SCLK, idea low)  SPIDAT SPI Data register  IZCON I'C Control register (in slave mode)  IZCSI slave mode stop interrupt entable bit (In-disable)  IZCSI slave mode stop interrupt entable bit (In-disable)  IZCSI slave mode interrupt decode bits  IZCSI slave mode interrupt mode)	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capturerleads elect (1=timer, 1=counter) PO PortO register (also A0-A7 & D0-D7) P1 Port1 register (analog & digital inputs) TZEX timer/counter 2 capturerleads drigger TZEX timer/counter 0 external input TZEX timer/counter 0 external in
IZCADD1, IZCADD2, IZCADD3   IZC secondary slave Address registers	EARRH,EADRL Data Flash/EE address registers  EDATA1, EDATA2, EDATA3  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer) WCOL write collision error flag  SPE SPI control register (set set set set set set set set set set	CNT2 timer/counter select (0*timer, 1*counter) CAP2 capturerleads elect (0*tenden, 1*capture) TH2,TL2 Timer2 register RCAP2H,RCAP2L Timer2 Reload/Capture P0 Port0 register (also Ab-A7 & Db-D7) P1 Port1 register (also Ab-A7 & Db-D7) P2 Port1 register (analog & digital inputs) timer/counter 2 explurerleads trigger T2 timer/counter 2 explurerleads trigger P2 Port2 register (also Ab-A1 & A16-A23) P3 Port3 register RD external data memory read strobe tri timer/counter 1 external input trigger (also Ab-A1 & A16-A23) T1 timer/counter 1 external input timer/counter 1 external input timer/counter 1 external input timer/counter 1 external input timer/counter 0 external input timer/counter 1 external input timer/counter 0 external input timer/co
PC secondary slave Address registers	EARRH,EADRL Data Flash/EE address registers  EDATA1, EDATA2, EDATA3  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer) WCOL write collision error flag  SPE SPI control register (set set set set set set set set set set	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capturerleads elect (1=timer, 1=counter) PO Port0 register (analog & digital inputs) TZEX timer/counter 2 capturerleads tragger TZEX timer/counter 3 capturerleads tragger TZEX timer/counter 3 capturerleads tragger TZEX timer/counter 4 capturerleads tragger TZEX timer/counter 3 capturerleads tragger TZEX timer/counter 4 capturerleads tragger TZEX timer/counter 5 capturerleads tragger TZEX
PWMCON PWM Control register	EARRH,EADRL Data FlashVEE address registers  EDATA1,EDATA2,EDATA3,EDATA4  Data FlashVEE data registers  SPICON SPI Control register  SPI SPI Interrupt (set by hardware at end of SPI transfer)  WCDU write collision error flag  WCDU write collision error flag  SPI SPI Interrupt (set by hardware at end of SPI transfer)  WCDU write collision error flag  CPO (Collision)  CPO (Collision)  CPO (Collision)  SPIN SPI SPI Interrupt (set by hardware set end of SPI transfer)  SPIN SPIN SPI SPI SPIN set (residue)  SPIN SPIN SPI SPIN set (residue)  SPIN SPIN SPIN SPIN SPIN set (residue)  SPIN SPIN set (residue)  SPIN SPIN SPIN set (residue)  SPIN SPIN set (residue)  SPIN SPIN SPIN	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capturerleads elect (1=timer, 1=counter) PO Port0 register (also A0-A7 & D0-D7) P1 Port1 register (analog & digital inputs) timer/counter 2 capturerlead trigger T2EX T2EX P2 Port1 register (analog & digital inputs) timer/counter 2 capturerlead trigger P3 Port3 register RD external data memory red strobe WR external data memory write strobe WR external data memory w
PWINDON 7 PW SONTON register  PWINDON 7 PWIN GOTHON register  PWINDON 7 PWIN mode bits   Dedustabled, 1 register production register power	EARRH,EADRL Data FlashVEE address registers  EDATA1, EDATA2, EDATA3  Data FlashVEE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer) WCOL write collision error flag WCOL by the collision error flag WCOL by the collision error flag WCOL by the collision error flag WCOL clock polarity select (0r-SCLK (ides low) PCOL clock polarity select (1r-SCLK (ides low) PCOL clock polarity select (0r-SCLK	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capturerleade select (0=timer, 1=counter) CAP2 capturerleade select (0=timer, 1=counter) CAP2 capturerleade select (0=timer, 1=counter) CAP2 timer/Capture PO Port0 register (also A0-A7 & D0-D7) P1 Port1 register (also A0-A7 & D0-D7) P1 Port1 register (analog & digital inputs) T/2EX timer/counter 2 exputurerleade trigger T/2 timer/counter 2 exputurerleade trigger T/2 timer/counter 2 exputurerleade trigger T/2 timer/counter 2 external input T/2 timer/counter 2 external input T/2 timer/counter 1 external interrupt T/2 timer/counter 2
PWMCON7 disable P26/B3.4 PWM output (0+enable) PWMCON7 2 = **win/Bibl. **adval/*flexible**. PWMCON8 2 = **win/Bibl. **adval/*flexible**. PWMCON9 2 = **win/Bibl. **adval/*flexible**. PWMCON1 2 = **pwm. **pw	EARH,EADRL Data Flash/EE address registers  EDATA1, EDATA2, EDATA3  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer)  WCOL write collision error flag  SPI SPI enable (0-PC enable, 1-SPI enable)  CPOL clock polarity select (0-SCLK idea low)  CPOL clock polarity select (0-SCLK idea low)  CPOL clock polarity select (0-SCLK idea low)  SPIDAT SPI Data register  I2CCON I*C Control register (in slave mode)  I2CSI  SIRON  SPIDAT SPI Data register  I2CCON I*C Control register (in slave mode)  I2CSI  I2CICIO slave mode stop interrupt enable bit (0-disable)  I2CICIO slave mode interrupt decode bits  I2CICIO slave mode interrupt in master mode)  I2CSI  I2CICIO slave mode interrupt in master mode)  I2CSI  I2CICIO slave mode interrupt in master mode)  I2CSI  I2CICIO slave mode interrupt in master mode)  I2CON I*C Control register (in master mode)  I2CON	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capturerleads elect (1=timer, 1=counter) PO Port0 register (also A0-A7 & DD-D7) P1 Port1 register (analog & digital inputs) T2EX imer/counter 2 external input P2 Port2 register (also A8-A15 & A16-A23) P3 Port3 register RD external data memory read strote RD external data memory read strote T1 timer/counter 1 external input T2 serial port treates detailine SCON Serial port treates detailine SCON Serial port teres detailine SCON Serial port teres detailine SCON Serial port teres detailine T1 timer/counter 1 external infunction control register SCON Serial port teres detailine T2 serial port teres detailine T3 timer/counter 1 external input T4 timer/counter 1 external infunction treated T5 SCON Serial port teres detailine T6 SCON Serial port teres to extensible T7 SCON SERIAL T1 S
PWMCON1 PVM counter = clock / [14,16,16-16-x/x]. PWMCON1 PVM counter = clock / [14,16,16-16-x/x]. PWMCON1 PVM counter = clock / [14,16,16-16-x/x]. PWMCON1 PVM clock source bits [0+5xx4-x/5,16-16-x/x]. PWMCN1 PVM clock source bits [0+5xx4-x/5,16-x/x]. PWM1 PVM Counter = clock / [14,16,16-16-x/x]. PWM1 PVM Counter = clock / [14,16,16-16-x/x]. PWM1 PVM Counter = clock / [14,16,16-16-x/x]. PWM1 PVM Counter = clock / [14,16-16-x/x]. PWM1 PVM Counter = clock / [14,16-x/x]. PV PVM Counter = clock / [14,16-x/x]. PV PVM Counter = clock / [14,16-x]. PV	EARRH,EADRL Data FlashVEE address registers  EDATA1, EDATA2, EDATA3, EDATA4  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer) WCOL write collision error flag WCOL clock polarity select (0r-SCLK idea tow) CPOL clock polarity idea tow) CP	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capturerleade select (0=timer, 1=counter) CAP2 timer/counter select (0=timer, 1=counter) TH2,TL2 Timer/2 register RCAP2H,RCAP2L Timer/2 register PO Port0 register (also A0-A7 & D0-D7) P1 Port1 register (also A0-A7 & D0-D7) P1 Port1 register (analog & digital inputs) timer/counter 2 expurier/lead affigure T2EX timer/counter 2 expurier/lead affigure P2 Port2 register (also A0-A7 & A16-A23) P3 Port3 register RD external data memory write strobe timer/counter 0 external input RD external data memory write strobe timer/counter 0 external input NT1 external data memory write strobe timer/counter 0 external input NT1 external data memory write strobe timer/counter 0 external input NT1 external interrupt 1 NT2 external interrupt 1 NT3 external interrupt 1 NT3 external interrupt 1 NT3 external interrupt 1 NT4 external interrupt 1 NT5 externa
PWMCON.2 PVM counter = clock (1,4,16,64) PVMCON.2 PVM counter = clock (1,4,16,64) PVMCON.2 PVM clock source bits (0=Fxxt),15 1=Fxxta, PVMCON.2 PVM clock source bits (0=Fxxta),15 1=Fxxta, PVMCON.2 PVMCO	EARRH,EADRL Data FlashVEE address registers  EDATA1, EDATA2, EDATA3, EDATA4  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer) WCOL write collision error flag WCOL clock polarity select (0r-SCLK idea tow) CPOL clock polarity idea tow) CP	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capturerleads elect (0=timer, 1=counter) CAP2 capturerleads elect (0=timer, 1=counter) TH2,TL2 Timer2 register RCAP2H,RCAP2L Timer2 Reload/Capture P0 Port0 register (also Ao-A7 & Do-D7) P1 Port1 register (analog & digital inputs) T2EX timer/counter 2 exputurerleads frigger T2EX timer/counter 2 exputurerleads frigger P2 Port2 register (also Ao-A7 & A16-A23) P3 Port3 register RC external input (also Ab-A16 & A16-A23) P3 Port3 register RC external input (also Ab-A16 & A16-A23) P3 Port3 register RC external input (also Ab-A16 & A16-A23) P3 Port3 register RC external input (also Ab-A16 & A16-A23) P3 Port3 register RC external input (also Ab-A16 & A16-A23) P3 Port3 register RC external information (also Ab-A16 & A16-A23) P3 Port3 register RC external information (also Ab-A16 & A16-A23) P3 Port3 register P1 timer/counter 1 external input (also Ab-A16 & A16-A23) P3 Port3 register P1 timer/counter 1 external input (also Ab-A16 & A16-A23) P3 Port3 register P1 timer/counter 1 external input (also Ab-A16 & A16-A23) P3 Port3 register P5 Port3 register P5 Port3 register P5 Port4 register P5 Port5
PWMCON.1 PWM clock source bits [oPFxnx1/5, 1=Fxn., PWMCON.1 2=T0 exit firms.3=Fxpcid.15-77Met/3] PWM01+, PWM01- PWM0 data registers  PWM1+, PWM1- PWM1 data registers  DPCON Data Pointer Control register  DPCON.6 data pointer auto-toggie enable ((Pedisable)) DPCON.1 TSCON.7 Timer 3 Control register  T3CON.7 Timer 3 Control register  Taccon.7 Timer 3 Data d rate enable (Ordisable) DPCON.1 Timer 3 Control register  Timer 3 baud rate enable (Ordisable)	EARRH,EADRL Data FlashVEE address registers  EDATA1,EDATA2,EDATA3  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer)  WCOL write collision error flag  WCOL write collision error flag  LOS SPI interrupt (set by hardware at end of SPI transfer)  WCOL write collision error flag  LOS SPIM matter mode select (for-SCLK idea tow)  CPOL clock polarity select (for-SCLK idea tow)  CPOL clock polarity select (for-SCLK idea tow)  SPIM SPI INTERVENCE (FORSCLK idea tow)  SPIM SPIM SPI INTERVENCE (FORSCLK idea tow)  SPIM SPIM SPI INTERVENCE (FORSCLK idea tow)  SPIM SPIM SPIM SPIM SPIM SPIM SPIM SPIM	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capturerleads elect (0=timer, 1=counter) CAP2 capturerleads elect (0=timer, 1=counter) TH2,TL2 Timer2 register RCAP2H,RCAP2L Timer2 Reload/Capture P0 Port0 register (also Ao-A7 & Do-D7) P1 Port1 register (analog & digital inputs) T2EX timer/counter 2 exputurerleads frigger T2EX timer/counter 2 exputurerleads frigger P2 Port2 register (also Ao-A7 & A16-A23) P3 Port3 register RC external input (also Ab-A16 & A16-A23) P3 Port3 register RC external input (also Ab-A16 & A16-A23) P3 Port3 register RC external input (also Ab-A16 & A16-A23) P3 Port3 register RC external input (also Ab-A16 & A16-A23) P3 Port3 register RC external input (also Ab-A16 & A16-A23) P3 Port3 register RC external information (also Ab-A16 & A16-A23) P3 Port3 register RC external information (also Ab-A16 & A16-A23) P3 Port3 register P1 timer/counter 1 external input (also Ab-A16 & A16-A23) P3 Port3 register P1 timer/counter 1 external input (also Ab-A16 & A16-A23) P3 Port3 register P1 timer/counter 1 external input (also Ab-A16 & A16-A23) P3 Port3 register P5 Port3 register P5 Port3 register P5 Port4 register P5 Port5
PWM0H, PWM0L PWM0 data registers  PWM1H, PWM1L PWM1 data registers  PCON Data Pointer Control register  DPCON Data Pointer Control register  data pointer auto-toggie enable (0-disable)  DPCON	EARRH,EADRL Data FlashVEE address registers  EDATA1, EDATA2, EDATA3, EDATA4  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI Interrupt (set by hardware at end of SPI transfer) WCOL write collision error flag UCOL clock polarity select (0r-SCLK (dies low) UCOL clock polarity select (0r	CNT2 timer/counter select (0-timer, 1-counter) CAP2 captipure/load select (0-teiload; 1-capture) TH2,TL2 Timer2 register RCAP2H,RCAP2L Timer2 register PO Port0 register (also A0-A7 & D0-D7) P1 Port1 register (also A0-A7 & D0-D7) P1 Port1 register (analog & digital inputs) T2EX T2EX T2EX T2EX T2EX T2EX T2EX T2EX
PWM1H, PWM1 L PWM1 data registers  DPCON Data Pointer Control register  DPCON data pointer auto-toggie enable (0-disable) DPCON5 DPCON4 DPCON5 TPCON6 TPCON7	EARRH,EADRL Data FlashVEE address registers  EDATA1, EDATA2, EDATA3, EDATA4  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI Interrupt (set by hardware at end of SPI transfer) WCOL write collision error flag UCOL clock polarity select (0r-SCLK (dies low) UCOL clock polarity select (0r	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capturerleade select (also A0-A7 & D0-D7) P1 Port1 register (also A0-A7 & D0-D7) P1 Port2 register (analog & digital inputs) T2EX timer/counter 2 external input T2EX timer/counter 1 external input T3EX timer/counter 1 exte
DPCON Data Pointer Control register DPCONS data pointer auto-togale enable (O-disable) DPCONS	EARRH,EADRL Data FlashVEE address registers  EDATA1, EDATA2, EDATA3, EDATA4  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer) WCOL write collision error flag WCOL clock polarity select (0r-SCLK ides low) PCOL polarity select (0r-SCLK ides low) PCOL clock polarity select (0r-SCLK ides low) PCOL clock polarity select (0r-SCLK ides low) PCOL PCOL (0r-SCLK ides low) PCOL PCOL (0r-SCLK ides low) PCOL PCOL polarity ideocal bits (0r-siave mode) PWMCON PVM Control register PWMCON PVM counter Polority (174, 16, 64) PVMCON PVMCON PVMCON PVMCON PVMCON PVMCON PV	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capturerleade select (also A0-A7 & D0-D7) P1 Port1 register (also A0-A7 & D0-D7) P1 Port2 register (analog & digital inputs) T2EX timer/counter 2 external input T2EX timer/counter 1 external input T3EX timer/counter 1 exte
data pointer auto-loggie enable (ordisable) DPCON4 DPCON4 DPCON4 DPCON4 DPCON4 DPCON4 DPCON4 DPCON5 DPCON5 DPCON5 DPCON5 DPCON5 DPCON5 DPCON5 DPCON6	EARRH,EADRL Data FlashVEE address registers  EDATA1, EDATA2, EDATA3  Data FlashVEE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer) WOOL write collision error flag  SPI SPI service (SPI) transfer (SPI) transfer) WOOL book polarity select (Or-SCLK (idea low) CPIA clock polarity select (Or-SCLK (idea low) SPIDAT SPI Data register  IZCCON I'C Control register (in slave mode) IZCIDI Select (Idea low) IZCIDI Select (Idea low) IZCIDI Select (Idea low) IZCIDI Select (Idea low) IZCON I'C Control register (in master mode) IZCON I'C Select (in master mode) IZCON	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capturerleade select (0=timer, 1=counter) CAP2 to proprie the select (0=timer, 1=counter) CAP2 to proprie the select (0=timer, 1=counter) CAP2 to prove th
DPCON5 DPCON4 I 1=8052.2-post-inc, 3-post-ofc, 4-LSB[g] DPCON2 DPCON2 DPCON1 I (1=8052.2-post-inc, 3-post-ofc, 4-LSB[g] DPH,DPL (DPTR) Data Pointer Page DPH,DPL (DPTR) DPH,DPL (DPTR) Data Pointer DPH,DPL (DPTR) DATA Concurrent ACC Accumulator  B auxiliary math register  TRICON Timer 3 boud rate enable (0-disable) DPH = 100ff conget (10 baudrate) / loo2	EARRH,EADRL Data Flash/EE address registers  EDATA1, EDATA2, EDATA3  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer) WCOL write collision error flag  POPPA clock polarity select (0~SCLK (ides low)  CPPA clock polarity select (0~SCLK (ides low)  SPROD	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capturerelioad select (0=timer, 1=counter) CAP2 to protect the counter of
T3CON Timer 3 Control register T3CON.7 Timer 3 Daud rate enable (0-disable) T3CON.1 Timer 3 Daud rate enable (0-disable) T3CON.1 Div = logff coset/(16 baudrate) / log2	EARRH,EADRL Data FlashVEE address registers  EDATA1, EDATA2, EDATA3, EDATA4  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI Interrupt (set by hardware at end of SPI transfer) WCOL write collision error flag WCOL clock polarity select (0~SCLK (dies low) CPOL clock polarity decode bile) CPOL clock polarity decode bile CPOL clock polarity decod	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capturerelioad select (also A0-A7 & D0-D7) P1 Port1 register (also A0-A7 & D0-D7) P1 Port2 register (also A8-A15 & A16-A23) P2 Port3 register R2 esternal data memory read strobe selected and transport of the transport of
T3CON Timer 3 Control register T3CON: Timer 3 Daud rate enable (0-disable) T3CON: Timer 3 Daud rate enable (0-disable) T3CON: DIV = log Tcose (16 baudrate) / log2	EARRH,EADRL Data FlashVEE address registers  EDATA1, EDATA2, EDATA3, EDATA4  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI Interrupt (set by hardware at end of SPI transfer) WCOL write collision error flag WCOL clock polarity select (0~SCLK (dies low) CPOL clock polarity decode bile) CPOL clock polarity decode bile CPOL clock polarity decod	CNT2 timer/counter select (0=timer, 1=counter) CAP2 capturerelioad select (also A0-A7 & D0-D7) P1 Port1 register (also A0-A7 & D0-D7) P1 Port2 register (also A8-A15 & A16-A23) P2 Port3 register R2 esternal data memory read strobe selected and transport of the transport of
T3CON Timer 3 Control register T3CON 7 Timer 3 baut rate enable (or-disable) T3CON 2 Timer 3 baut rate enable (or-disable) T3CON 1 Diversified Federate (DIV) T3CON 2 Diversified Federate (DIV) T3CON 3 DIV T3CON 2 DIV T3C	EARRH,EADRL Data FlashVEE address registers  EDATA1, EDATA2, EDATA3, EDATA4  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI Interrupt (set by hardware at end of SPI transfer) WCOL write collision error flag WCOL clock polarity select (0~SCLK (dies low) CPOL clock polarity decode bile) CPOL clock polarity decode bile CPOL clock polarity decod	CNT2 timer/counter select (0-timer, 1-counter) CAP2 captiverieload select (0-teiload; 1-captive) TH2,TL2 Timer2 register RCAP2H,RCAP2L Timer2 register PO Port0 register (also A0-A7 & D0-D7) P1 Port1 register (also A0-A7 & D0-D7) P1 Port1 register (also A0-A7 & D0-D7) P2 Port2 register (also A0-A7 & D0-D7) P3 Port3 register (also A0-A7 & D0-D7) P4 Port3 register (also A0-A7 & D0-D7) P5 Port3 register (also A0-A7 & A10-A23) P6 P0 Port3 register (also A0-A7 & A10-A23) P7 P0 Port3 register (also A0-A7 & A10-A23) P8 Port3 register RD external data memory write strobe WR SCON Serial port flower external data memory WR external data memory write strobe WR external data memory
T3CON.7 Timer 3 baud rate enable (0=disable) T3CON.2 binary divide factor (DIV) T3CON.1 DIV = log[Fcope(/16-baudrate)] / log2	EARTH,EADRL Data FlashVEE address registers  EDATA1, EDATA2, EDATA3, EDATA4  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer) WCOL write collision error flag WCOL spice of the property	CNT2 timer/counter select (0-timer, 1-counter) CAP2 complyur/enional select (0-tenion4) recapture) TH2,TL2 Timer2 register RCAP2H,RCAP2L Timer2 register PO Port0 register (also A0-A7 & D0-D7) P1 Port1 register (also A0-A7 & D0-D7) P1 Port1 register (also A0-A7 & D0-D7) P2 Port2 register (also A0-A7 & D0-D7) P2 Port3 register P2 Port3 register (also A0-A7 & A16-A23) P3 Port3 register RD external data memory wreat strobe with the selection of the
T3CON.1 DÍV = log[F <sub>CORE</sub> /(16-baudrate)] / log2	EARRH,EADRL Data FlashVEE address registers  EDATA1, EDATA2, EDATA3  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer) WCOL write collision error flag WCOL clock polarity select (0r-SCLK idea low) CPOL clock polarity idea low) CPOL clock polarity select (0r-SCLK idea low) CPOL clock polarity idea low) CPOL clock polarity idea low) CPOL clock polarity select (0r-SCLK idea low) CPOL clock polarity idea low) CPOL clock	CNT2 timer/counter select (0-timer, 1-counter) CAP2 complyure/load select (0-teiload; 1-capture) TH2,TL2 Timer2 register RCAP2H,RCAP2L Timer2 register PO Port0 register (also A0-A7 & D0-D7) P1 Port1 register (also A0-A7 & D0-D7) P1 Port1 register (also A0-A7 & D0-D7) P2 Port2 register (also A0-A7 & D0-D7) P2 Port3 register P2 Port2 register (also A8-A15 & A16-A23) P3 Port3 register P4 Port3 register P5 Port3 register P5 Port3 register P6 RD external input R1 strengtoner 2 external input R1 strengtoner 3 e
	EARRH,EADRL Data FlashVEE address registers  EDATA1, EDATA2, EDATA3  Data Flash/EE data registers  SPICON SPI Control register  ISPI SPI interrupt (set by hardware at end of SPI transfer) WCOL write collision error flag WCOL clock polarity select (0r-SCLK idea low) CPOL clock polarity idea low) CPOL clock polarity select (0r-SCLK idea low) CPOL clock polarity idea low) CPOL clock polarity idea low) CPOL clock polarity select (0r-SCLK idea low) CPOL clock polarity idea low) CPOL clock	CNT2 timer/counter select (0-timer, 1-counter) CAP2 complyure/load select (0-teiload; 1-capture) TH2,TL2 Timer2 register RCAP2H,RCAP2L Timer2 register PO Port0 register (also A0-A7 & D0-D7) P1 Port1 register (also A0-A7 & D0-D7) P1 Port1 register (also A0-A7 & D0-D7) P2 Port2 register (also A0-A7 & D0-D7) P2 Port3 register P2 Port2 register (also A8-A15 & A16-A23) P3 Port3 register P4 Port3 register P5 Port3 register P5 Port3 register P6 RD external input R1 strengtoner 2 external input R1 strengtoner 3 e