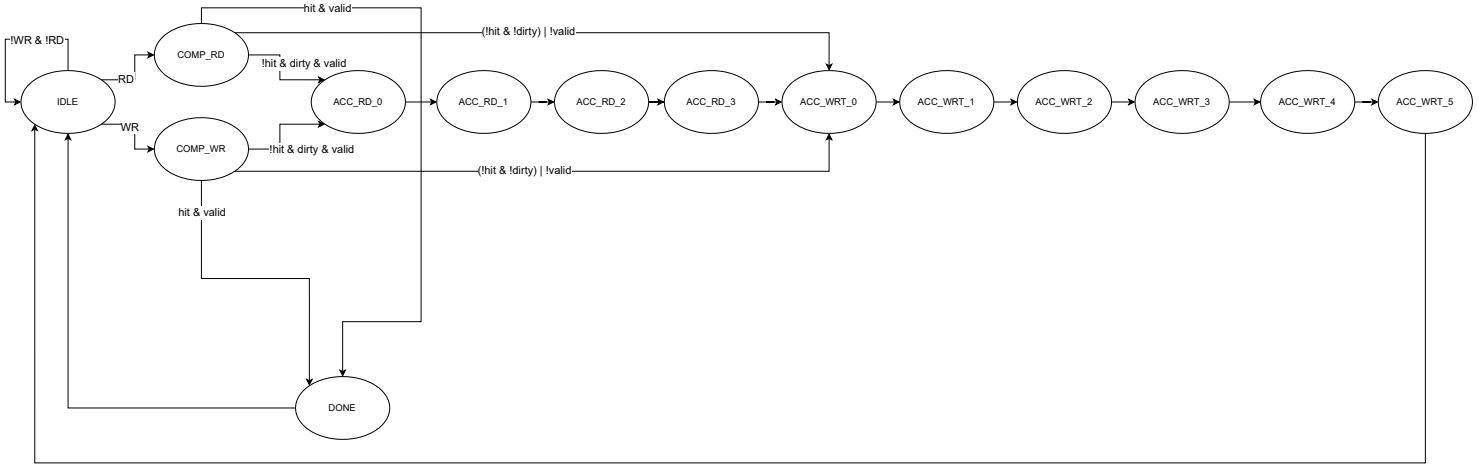
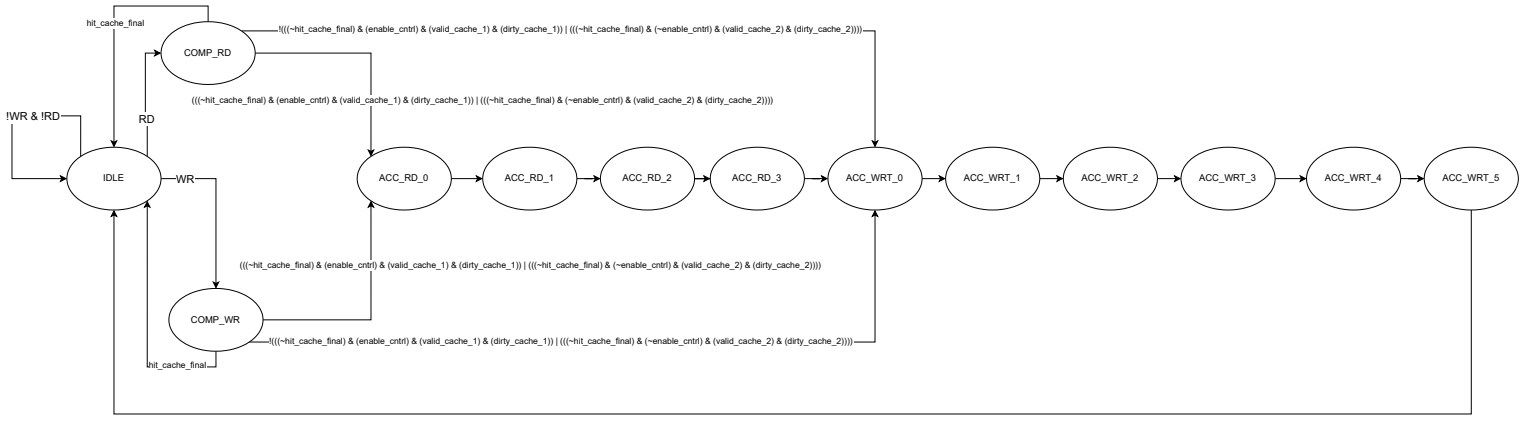
Direct-Mapped Cache State Diagram



State	Reset	IDLE	COMP_RD	COMP_WR	ACC_RD_0	ACC_RD_1	ACC_RD_2
Signal							
nxt_state	IDLE	rd ? COMP_RD : (wr ? COMP_WR : IDLE)	valid_cache ? (hit_cache ? DONE : (dirty_cache ? ACCESS_RD_0 : ACCESS_WR_0)) : ACCESS_WR_0	valid_cache ? (hit_cache ? DONE : (dirty_cache ? ACCESS_RD_0 : ACCESS_WR_0)) : ACCESS_WR_0	ACC_RD_1	ACC_RD_2	ACC_RD_3
enable_cntrl	0	0	1	1	1	1	1
idx_cntrl	0	0	addr[10:3]	addr[10:3]	addr[10:3]	addr[10:3]	addr[10:3]
offset_cntrl	0	0	addr[2:0]	addr[2:0]	0	2	4
comp_cntrl	0	0	1	1	0	0	0
write_cntrl	0	0	0	1	0	0	0
tag_cntrl	x	x	addr[15:11]	addr[15:11]	x	x	x
data_in_cntrl	x	x	x	data_in	x	x	x
valid_in_cntrl	0	0	0	0	0	1	2
addr_in_mem	x	x	x	x	x	x	x
data_in_mem	x	x	x	x	data_out_cache	data_out_cache	data_out_cache
write_mem	0	0	0	0	1	1	1
read_mem	0	0	0	0	0	0	0
Done	0	0	0	0	0	0	0
Stall	1	0	0	0	0	0	0
CacheHit	0	0	0	0	0	0	0
end_state	0	0	0	0	0	0	0
write	0	0	0	1	0	0	0
read	0	0	1	0	0	0	0
hit	0	0	0	1	0	0	0

ACC_RD_3	ACC_WR_0	ACC_WR_1	ACC_WR_2	ACC_WR_3	ACC_WR_4	ACC_WR_5	DONE
ACC_WR_0	ACC_WR_1	ACC_WR_2	ACC_WR_3	ACC_WR_4	ACC_WR_5	IDLE	IDLE
1	1	1	1	1	1	1	0
addr[10:3]	0	0	addr[10:3]	addr[10:3]	addr[10:3]	addr[10:3]	0
6	0	0	0	2	4	6	0
0	0	0	0	0	0	flop_write ? 1'b1 : 1'b0	0
0	0	0	1	1	1	1	0
x	x	x	addr[15:11]	addr[15:11]	addr[15:11]	addr[15:11]	x
x	x	x	(wr & (addr[2:0] == 3'b000)) ? data_in : data_out_mem	(wr & (addr[2:0] == 3'b010)) ? data_in : data_out_mem	(wr & (addr[2:0] == 3'b100)) ? data_in : data_out_mem	(flop_write & (addr[2:0] == 3'b110)) ? data_in : data_out_mem	x
3	0	0	1	1	1	1	0
x	{addr[15:3], 3'b000}	{addr[15:3], 3'b010}	{addr[15:3], 3'b100}	{addr[15:3], 3'b110}	x	x	x
data_out_cache	x	x	x	x	x	x	x
1	0	0	0	0	0	0	0
0	1	1	1	1	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	flop_hit ? 1'b1 : 1'b0
0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

Two-Way Associative Cache State Diagram



State	Reset	IDLE	COMP_RD	COMP_WR	ACC_RD_0	ACC_RD_1	ACC_RD_2	ACC_RD_3	ACC_WR_0	ACC_WR_1	ACC_WR_2	ACC_WR_3	ACC_WR_4	ACC_WR_5	
Signal															
nxt_state	IDLE	rd ? COMP_RD : (wr ? COMP_WR : IDLE)	valid_cache ? (hit_cache ? DONE : (dirty_cache ? ACCESS_RD_0 : ACCESS_WR_0)) : ACCESS_WR_0	valid_cache ? (hit_cache ? DONE : (dirty_cache ? ACCESS_RD_0 : ACCESS_WR_0)) : ACCESS_WR_0	ACC_RD_1	ACC_RD_2	ACC_RD_3	ACC_WR_0	ACC_WR_1	ACC_WR_2	ACC_WR_3	ACC_WR_4	ACC_WR_5	IDLE	
enable_cntrl	0	0	(valid_cache_1 & hit_cache_1) | (~valid_cache_1 & valid_cache_2 & ~hit_cache_final) | (~valid_cache_1 & ~valid_cache_2 & ~hit_cache_final) | (valid_cache_1 & valid_cache_2 & ~hit_cache_final & flop_victim_cntrl)	(valid_cache_1 & hit_cache_1) | (~valid_cache_1 & valid_cache_2 & ~hit_cache_final) | (~valid_cache_1 & ~valid_cache_2 & ~hit_cache_final) | (valid_cache_1 & valid_cache_2 & ~hit_cache_final & flop_victim_cntrl)	flop_en	flop_en	flop_en	flop_en	flop_en	flop_en	flop_en	flop_en	flop_en	flop_en	
en	0	0	(valid_cache_1 & hit_cache_1) | (~valid_cache_1 & valid_cache_2 & ~hit_cache_final) | (~valid_cache_1 & ~valid_cache_2 & ~hit_cache_final) | (valid_cache_1 & valid_cache_2 & ~hit_cache_final & flop_victim_cntrl)	(valid_cache_1 & hit_cache_1) | (~valid_cache_1 & valid_cache_2 & ~hit_cache_final) | (~valid_cache_1 & ~valid_cache_2 & ~hit_cache_final) | (valid_cache_1 & valid_cache_2 & ~hit_cache_final & flop_victim_cntrl)											
idx_cntrl	0	0	addr[10:3]	addr[10:3]	addr[10:3]	addr[10:3]	addr[10:3]	addr[10:3]	0	0	addr[10:3]	addr[10:3]	addr[10:3]	addr[10:3]	
offset_cntrl	0	0	addr[2:0]	addr[2:0]	0	2	4	6	0	0	0	2	4	6	
comp_cntrl	0	0	0	1	0	0	0	0	0	0	0	0	0	flop_write ? 1'b1 : 1'b0	
comp_rw	0	0	1	1	0	0	0	0	0	0	0	0	0	0	
write_cntrl	0	0	0	1	0	0	0	0	0	0	1	1	1	1	
tag_cntrl	x	x	addr[15:11]	addr[15:11]	x	x	x	x	x	x	addr[15:11]	addr[15:11]	addr[15:11]	addr[15:11]	
data_in_cntrl	x	x	x	data_in	x	x	x	x	x	x	(wr & (addr[2:0] == 3'b000)) ? data_in : data_out_mem	(wr & (addr[2:0] == 3'b010)) ? data_in : data_out_mem	(wr & (addr[2:0] == 3'b100)) ? data_in : data_out_mem	(flop_write & (addr[2:0] == 3'b110)) ? data_in : data_out_mem	
data_out_cntrl	0	0	data_out_final	x	x	x	x	x	x	x	(rd & (addr[2:0] === 3'b000)) ? data_out_mem : data_temp	(rd & (addr[2:0] === 3'b010)) ? data_out_mem : data_temp	(rd & (addr[2:0] === 3'b100)) ? data_out_mem : data_temp	(flop_read & (addr[2:0] === 3'b110)) ? data_out_mem : data_temp	
valid_in_cntrl	0	0	0	0	0	0	0	0	0	0	1	1	1	1	
addr_in_mem	x	x	x	x	{tag_out_final, idx_cntrl, offset_cntrl}	{tag_out_final, idx_cntrl, offset_cntrl}	{tag_out_final, idx_cntrl, offset_cntrl}	{tag_out_final, idx_cntrl, offset_cntrl}	{addr[15:3], 3'b000}	{addr[15:3], 3'b010}	{addr[15:3], 3'b100}	{addr[15:3], 3'b110}	x	x	
data_in_mem	x	x	x	x	data_out_final	data_out_final	data_out_final	data_out_final	x	x	x	x	x	x	
write_mem	0	0	0	0	1	1	1	1	0	0	0	0	0	0	
read_mem	0	0	0	0	0	0	0	0	1	1	1	1	0	0	
victim_cntrl	x	x	x	x	x	x	x	x	x	x	x	x	x	~flop_victim_cntrl	
Done	0	0	hit_cache_final	0	0	0	0	0	0	0	0	0	0	1	
Stall	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
CacheHit	0	0	hit_cache_final	0	0	0	0	0	0	0	0	0	0	0	
end_state	0	0	hit_cache_final	0	0	0	0	0	0	0	0	0	0	1	
write	0	0	0	1	0	0	0	0	0	0	0	0	0	0	
read	0	0	1	0	0	0	0	0	0	0	0	0	0	0	