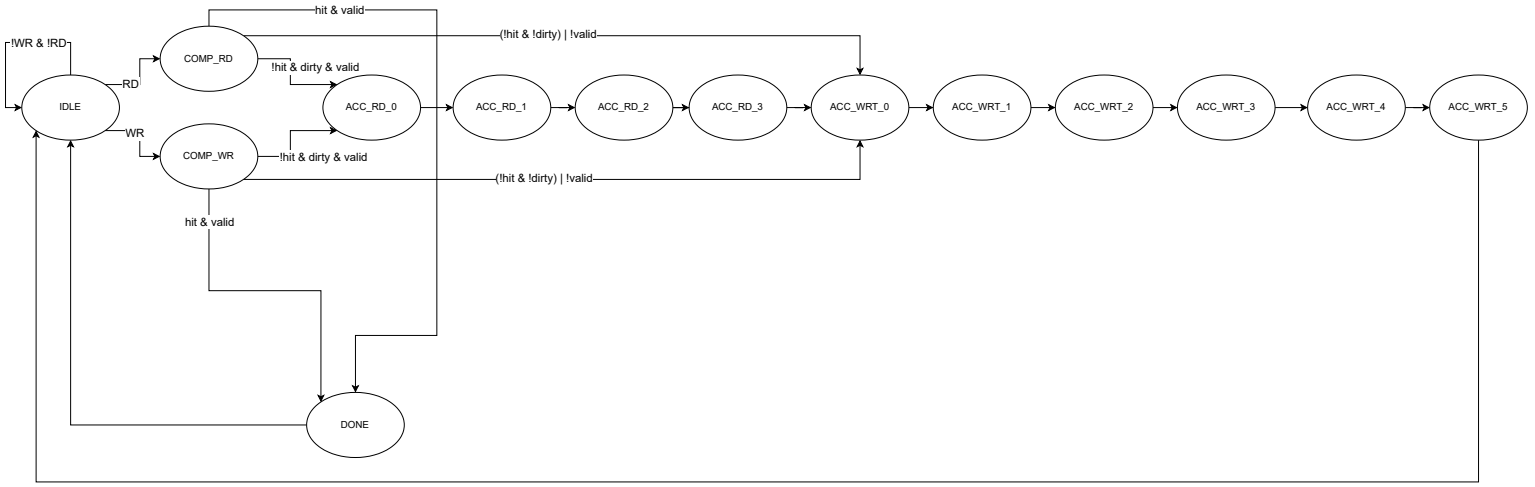


| State | Reset | IDLE | COMP_RD | COMP_WR | ACC_RD_0 | ACC_RD_1 | ACC_RD_2 | ACC_RD_3 | ACC_WR_0 | ACC_WR_1 | ACC_WR_2 | ACC_WR_3 | ACC_WR_4 | ACC_WR_5 | DONE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Signal | | | | | | | | | | | | | | | |
| nxt_state | IDLE | rd ? COMP_RD : (wr ? COMP_WR : IDLE) | valid_cache ? (hit_cache ? DONE : (dirty_cache ? ACCESS_RD_0 : ACCESS_WR_0)) : ACCESS_WR_0 | valid_cache ? (hit_cache ? DONE : (dirty_cache ? ACCESS_RD_0 : ACCESS_WR_0)) : ACCESS_WR_0 | ACC_RD_1 | ACC_RD_2 | ACC_RD_3 | ACC_WR_0 | ACC_WR_1 | ACC_WR_2 | ACC_WR_3 | ACC_WR_4 | ACC_WR_5 | IDLE | IDLE |
| enable_cntrl | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| idx_cntrl | 0 | 0 | addr[10:3] | addr[10:3] | addr[10:3] | addr[10:3] | addr[10:3] | addr[10:3] | 0 | 0 | addr[10:3] | addr[10:3] | addr[10:3] | addr[10:3] | 0 |
| offset_cntrl | 0 | 0 | addr[2:0] | addr[2:0] | 0 | 2 | 4 | 6 | 0 | 0 | 0 | 2 | 4 | 6 | 0 |
| comp_cntrl | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | flop_write ? 1'b1 : 1'b0 | 0 |
| write_cntrl | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| tag_cntrl | x | x | addr[15:11] | addr[15:11] | x | x | x | x | x | x | addr[15:11] | addr[15:11] | addr[15:11] | addr[15:11] | x |
| data_in_cntrl | x | x | x | data_in | x | x | x | x | x | x | (wr & (addr[2:0] == 3'b000)) ? data_in : data_out_mem | (wr & (addr[2:0] == 3'b010)) ? data_in : data_out_mem | (wr & (addr[2:0] == 3'b100)) ? data_in : data_out_mem | (flop_write & (addr[2:0] == 3'b110)) ? data_in : data_out_mem | x |
| valid_in_cntrl | 0 | 0 | 0 | 0 | 0 | 1 | 2 | 3 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| addr_in_mem | x | x | x | x | x | x | x | x | {addr[15:3], 3'b000} | {addr[15:3], 3'b010} | {addr[15:3], 3'b100} | {addr[15:3], 3'b110} | x | x | x |
| data_in_mem | x | x | x | x | data_out_cache | data_out_cache | data_out_cache | data_out_cache | x | x | x | x | x | x | x |
| write_mem | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| read_mem | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| Done | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Stall | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CacheHit | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | flop_hit ? 1'b1 : 1'b0 |
| end_state | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| write | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| read | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| hit | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |