Cycle	Instruction Retired	Reason
1	NA	
2	NA	
3	NA	
4	NA	
5	lbi r0	
6	lbi r5	
7	lbi r6	
8	lbi r7	
9	ld r1 r0 0	
		Next instruction uses r1 (st r5 r1 0), which is a RAW data hazard due to the previous lbi loading into r1. There are 3 stalls to allow for r1's value to be written back in the
10	NOP	writeback stage.
11	NOP	
12	NOP	
13	st r5 r1 0	
14	ld r1 r0 2	
		Next instruction uses r1 (st r6 r1 1), which is a RAW data hazard due to the previous ld loading into r1. There are 3 stalls to allow for r1's value to be written back in the
15	NOP	writeback stage.
16	NOP	
17	NOP	
18	st r6 r1 1	
19	ld r1 r0 4	
		Next instruction uses r1 (st r7 r1 1), which is a RAW data hazard due to the previous ld loading into r1. There are 3 stalls to allow for r1's value to be written back in the
20	NOP	writeback stage.
21	NOP	
22	NOP	

23	st r7 r1 1	
24	halt	
		These two NOPs allow for the memory and writeback stages of instructions before halt to finish, so memory
25	NOP	dump is correct.
26	NOP	