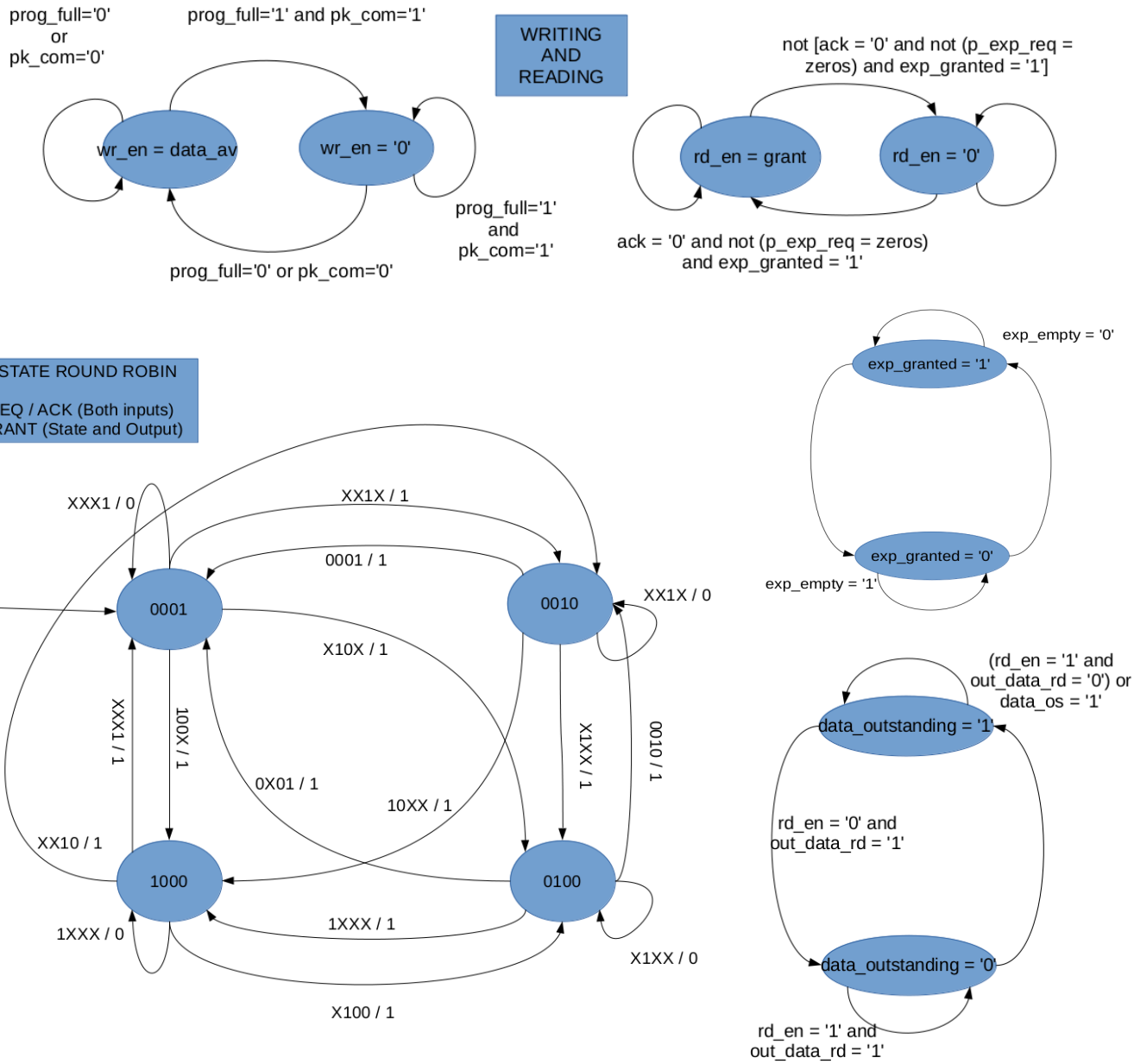
Team B : DigiDestined - Project 04



Components

- The module – Contention Resolution and Switching – with code in CRS.vhd is made up of 2N VOQs and N arbiters.
- A VOQ has a single input port, and N output ports, corresponding to the N output ports. N VOQs correspond to the N input buffer ports, and another N VOQs corresponding to N input express ports. It also takes the corresponding output_ports as the input.
- Each arbiter has as input N buffer ports, corresponding to the N VOQs, and N express buffer ports, corresponding to the other N VOQs. Each arbiter has a single output port.

General Discussion

- Due to the delay involved in the reading of data from a FIFO, there is an idle period of one clock cycle, as the data is read, and then the decision of as to whether this is the last chunk of the packet can be taken.
- Data at the input requires a delay of 3 clk period to arrive at the output port.
- The value of the number of ports, number of data valid bits, data valid bit intervals can all be set in globals.vhd, and this is discussed in the README.
- Care has been taken to ensure that the round robin works despite of interrupts from express data.
- Head of line blocking has also been avoided, by using N FIFOs for each input port.