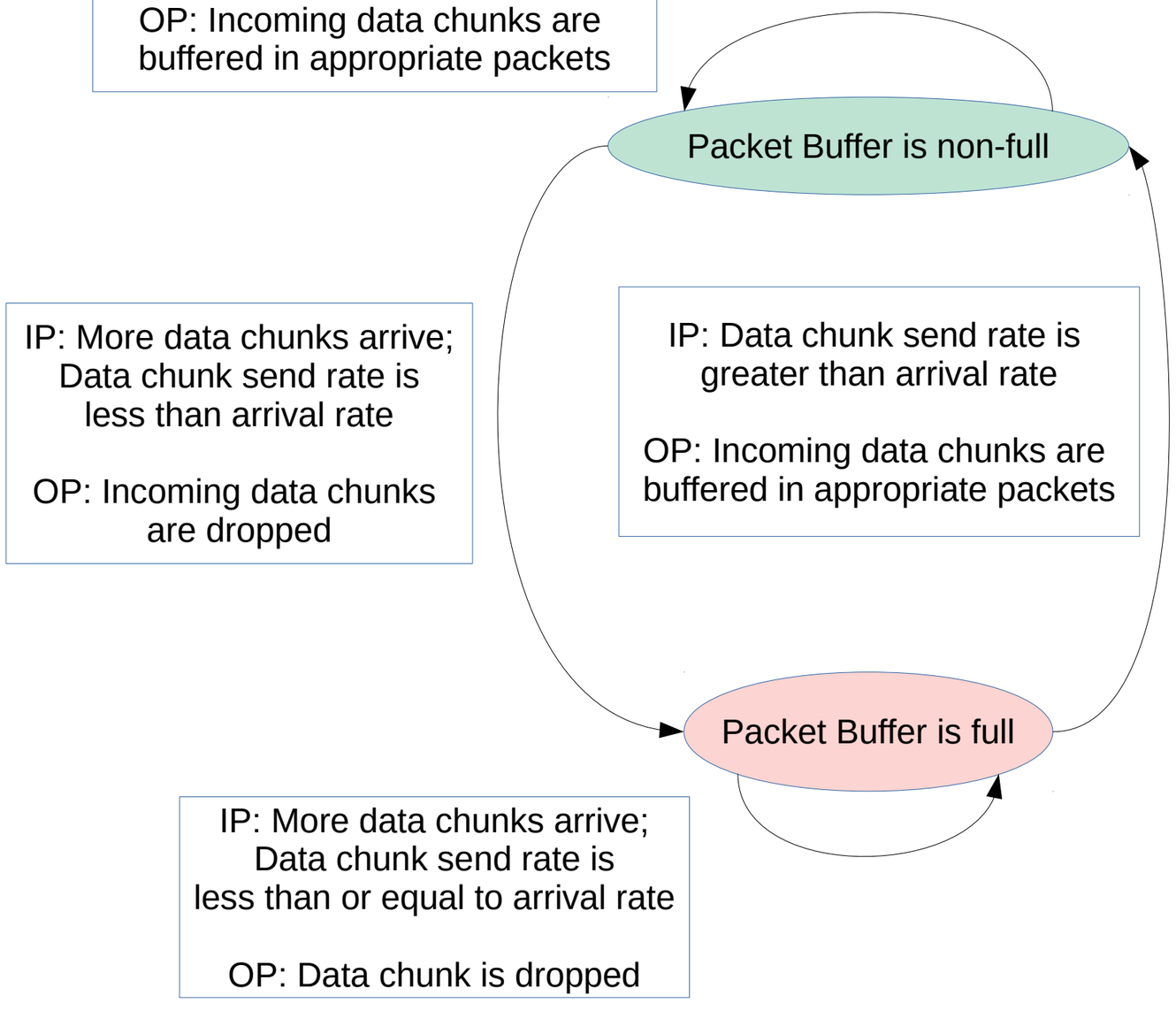
CONTENTION RESOLUTION AND SWITCHING: TEAM B - DIGIDESTINED

170050001 170050018 170050024 170100075 160050085

IP: More data chunks arrive;
Data chunk send rate is
greater than or more than arrival rate

OP: Incoming data chunks are
buffered in appropriate packets



A summary of the architecture:

- The VOQ is a purely combinatorial circuit. Each has 1 input port and n output ports, corresponding to the n output port addresses of the top module.
- Thus, there are 2n VOQs: n for the buf-data and another n for the exp-data.

- The arbiter takes as input 2n ports: n ports corresonding to the exp-data, and another n ports corresponding to the buf-data. It has a single output port, corresponding to the the appropriate output port of the top module.
- Each arbiter maintains 2n packet buffers corresponding to each of the input ports. Whenever the outport_data_rd is '1', it begins sending a completely-arrived-packet from the packet-buffer to the outport_data. Higher priority is given to the exp-data.

The high level algorithm for arbiter is as follows:

while some exp-data-av port is high
    transfer data to outport-exp-buffer
similarly for buf-data
note: two separate buffers are maintained

while outport-exp-buffer is non-empty
    whenever outport-data-rd is high
        transfer one packet from buffer to outport
while outport-exp-buffer is empty
    and outport-buf-buffer is non-empty
    whenever outport-data-rd is high
        transfer one packet from buffer to outport

Whenever the outport_data_rd is high, a round-robin algorithm is run on the packet-buffers, to send the completely-arrived packets to the outport_data. The next packet is sent only after the current packet is completely sent.