Contention Resolution and Switching (Team B - DigiDestined)

Those that affect the state of the CRS are exactly the following:

- outport_data_rd
- exp_data_av
- exp_dv
- buf_data_av
- buf_dv

output_port and output_port_valid do not play a role in sequential logic – they play a role only in the VOQ, which is purely combinatorial in nature.

VOQ is a purely combinatorial circuit – therefore, no state diagram for VOQ

For each of the 2n buffers:

pk_av = nand of all dv bits in that buffer (indicates a complete packet has arrived.)

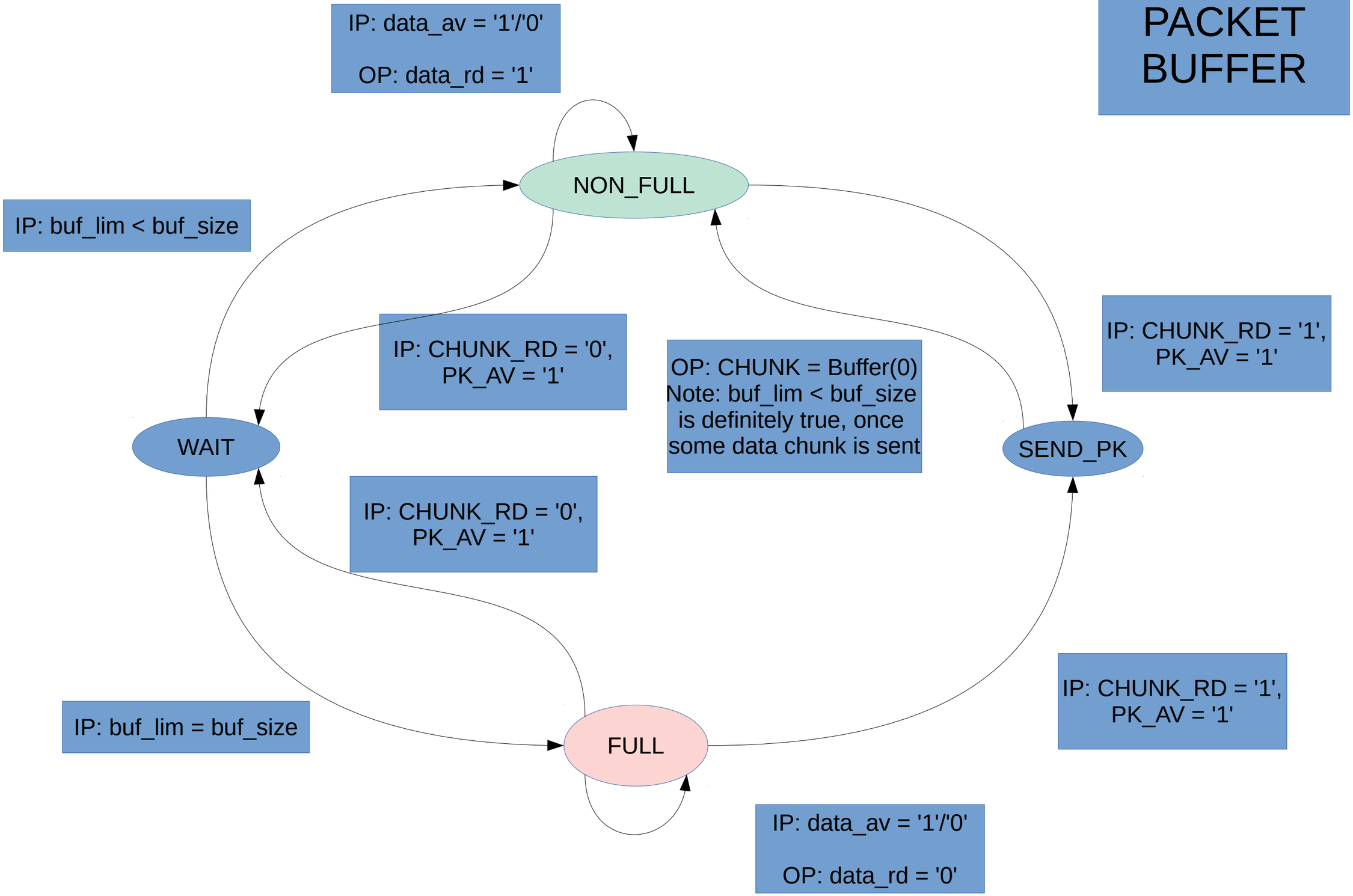
We buffer a data-chunk only if data_av is '1'.

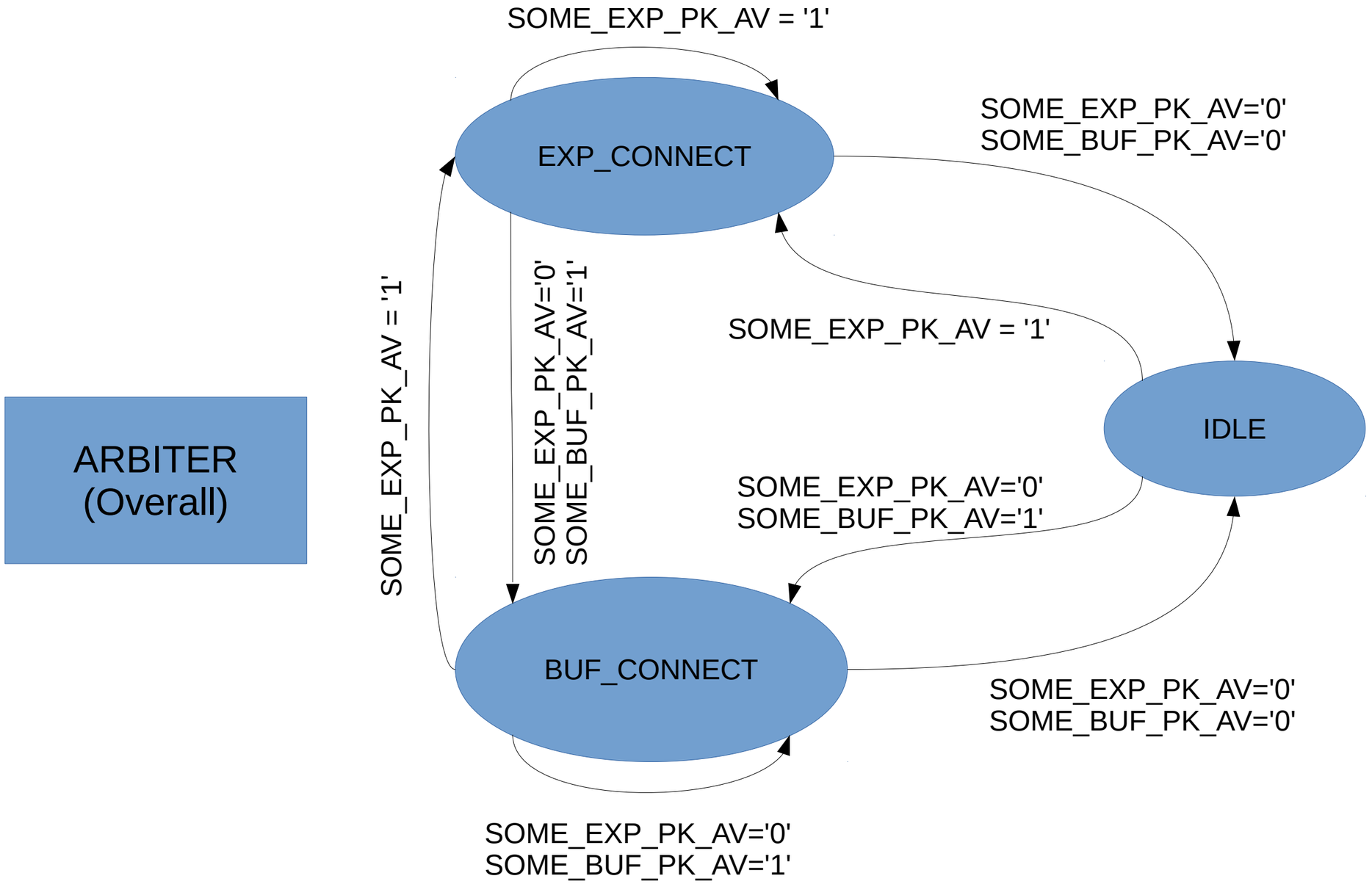
some_pk_av_exp and some_pk_av_buf
- or of all the pk_av in exp or buf

When some_pk_av_exp is '1', we run a round-robin on the exp_packet_buffer's,

Else if some_pk_av_buf is '1' we run a round-robin on the buf_packet_buffer's.

PACKET BUFFER




ARBITER
(Overall)
SOME_EXP_PK_AV = '1'
EXP_CONNECT
SOME_EXP_PK_AV='0'
SOME_BUF_PK_AV='0'
SOME_EXP_PK_AV = '1'
IDLE
SOME_EXP_PK_AV='0'
SOME_BUF_PK_AV='1'
SOME_EXP_PK_AV='0'
SOME_BUF_PK_AV='1'
SOME_EXP_PK_AV = '1'
BUF_CONNECT
SOME_EXP_PK_AV='0'
SOME_BUF_PK_AV='0'
SOME_EXP_PK_AV='0'
SOME_BUF_PK_AV='1'