Homework 10: Verilog

Objective:

Recreate some of the Nand2Tetris Project 1 Elementary Gates in Verilog along with their testbenches, to compare our HDL language against an industry-standard language. The following are the only gates you will recreate:

Not, Not16, And, And16, Or, Or16, Xor, Xor16, DMux, Or8Way

Grading method:

For the chips with larger buses (Not16, And16, Or16, Xor16) you should ***make the basic chip*** (Not, And, Or, Xor) ***parameterized so that you need only have one chip to handle both tests***! You will still need to create a separate testbench for each of the gates above. This means you will turn in the following files ZIP'd together:

Chips: **Not.v, And.v, Or.v, Xor.v, DMux.v, Or8Way.v**

Testbenches: **Not_tb.v, Not16_tb.v, And_tb.v, And16_tb.v, Or_tb.v, Or16_tb.v, Xor_tb.v, Xor16_tb.v, DMux_tb.v, Or8Way_tb.v**

You have been provided with a full testbench for Not_tb.v and Not16_tb.v as examples, and the basic Not.v structure without a solution. Your outputs should look like the corresponding .cmp files from the Nand2Tetris website.

What do you turn in?

The **chip .v files** (there are 6 of them) and **testbench .v files** (there are 10 of them) in a ZIP file per Project Submission Guidelines (see document on Blackboard). Note there is no documentation required for this homework (you already did it in previous homeworks).

Chips	*Compiles?*	*Parameterized?*	*TestBench?*	*TestBench16?*
Not	/7	/7	/3	/3
And	/7	/7	/3	/3
Or	/7	/7	/3	/3
Xor	/7	/7	/3	/3
DMux	/7	----------	/3	----------
Or8Way	/7	----------	/3	----------
Total (100)	**42**	**28**	**18**	**12**

See http://nand2tetris.org/ for test scripts/output files (if you need clarification email your instructor. You will be graded based on this documents requirements).