Homework 3: Combinational Chips (Arithmetic+ALU)

Objective:

Build the gates described in Chapter 2 (see table below), which will test your understanding of Boolean Logic and Arithmetic, building the gates that do so.

Grading method:

If the chip passes *all* the tests specified in the supplied test script, it receives 60% of the grade. 30% goes to it being well built (the lowest number of chips to implement), with the remaining 10% going towards documentation provided for each chip. Generally speaking, we prefer implementations that *use as few chip* ***parts*** *as possible,* even if it implies a less efficient chip design (in term of # of AND/OR/NOT chips). Higher-level chips are considered as one chip part (ex. Mux, DMux, Or8Way, etc.)

What do you turn in?

The **.hdl files** (there are 5 of them: HalfAdder, Full Adder, Add16, Inc16, ALU) and the ***documentation.pdf*** file ONLY (see Documentation Instructions for guidelines on how to do this), in a ZIP file per Project Submission Guidelines (see document on Blackboard).

NOTE: you will only submit one HDL file for the ALU (ALU.hdl), the grading table below assumes that one chip will be tested with BOTH test scripts, this is to maximize partial credit for you in case you aren't able to get the status output flags working.

Chip	***Working?***	***Well built?***
HalfAdder	/ 10	/ 5
FullAdder	/ 10	/ 5
Add16	/ 10	/ 5
Inc16	/ 10	/ 5
ALU + no status outputs (ALU-nostat.tst)	/ 15	/ 5
ALU + full test (ALU.tst)	/ 5	/ 5
Subtotal	/ 60	/ 30
Documentation	/ 10	

See http://nand2tetris.org/02.php for some tips/resources/tools (note that the assignment on the website is substantially different from the assignment that is described above, if you need clarification email your instructor. You will be graded based on this documents requirements).