Homework 2: Intermediate Logic Gates

Objective:
        Build the rest of the logic gates described in Chapter 1 (see list below), yielding a complete basic chip-set. The only building blocks that you can use in this project are primitive Nand gates and the composite gates that you will gradually build on top of them in the last homework and this homework.

Grading method:
        If the chip passes *all* the tests specified in the supplied test script, it receives 60% of the grade. 30% goes to it being well built (the lowest number of chips to implement), with the remaining 10% going towards documentation provided for each chip.

What do you turn in?
        The **.hdl files** (there are 11 of them) and the ***documentation.pdf*** file ONLY (see Documentation Instructions for guidelines on how to do this), in a ZIP file per Project Submission Guidelines (see document on Blackboard).

Chip	*Working?*	*Well built?*
Mux	/ 3	/ 2
DMux	/ 3	/ 2
Not16	/ 6	/ 2
And16	/ 6	/ 3
Or16	/ 6	/ 3
Mux16	/ 6	/ 3
Or8Way	/ 6	/ 3
Mux4Way16	/ 6	/ 3
Mux8Way16	/ 6	/ 3
DMux4Way	/ 6	/ 3
DMux8Way	/ 6	/ 3
Subtotal	/ 60	/ 30
Documentation		/ 10

See *http://nand2tetris.org/01.php for some tips/resources/tools (note that the assignment on the website is substantially different from the assignment that is described above, if you need clarification email your instructor. You will be graded based on this documents requirements).*

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