Albert Gural

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Education

Stanford University **Stanford, CA**
M.S. Electrical Engineering, GPA: 4.0 *June 2018*
Ph.D. Electrical Engineering *Sept. 2016 - present*

- **Murmann Mixed-Signal Group (Boris Murmann)**
- **Selected Coursework:** Large Scale Matrix Computation, Convex Optimization, Deep Learning, Reinforcement Learning, Digital Signal Processing, Information Theory, Analog-Digital Interface Circuits
- **Awards:** NSF Graduate Research Fellowship, The Krishna Kolluri Graduate Fellowship Fund

California Institute of Technology **Pasadena, CA**
B.S. Electrical Engineering with a minor in Computer Science, GPA: 4.0 *June 2016*

- **Selected Coursework:** Senior Thesis (MICS Lab), Machine Learning and Data Mining, Advanced Digital Systems, Mixed-mode ICs, Feedback and Control Circuits, Signal-Processing Systems
- **Awards:** ACM-ICPC (collegiate programming contest) international contestant *Thailand, 2016*

Work and Experience

Stanford University (Boris Murmann Mixed-Signal Group), *PhD Research* *2016-now*

- Researching methods to reduce memory for hardware acceleration of deep learning inference and training.
- Convolutional neural network memory reduction for low memory microcontroller inference, published at the ICML 2019 conference. `http://proceedings.mlr.press/v97/gural19a.html`
- Resistive RAM (RRAM) - based in-memory compute architecture for deep learning inference, published at the ASILOMAR 2019 conference. `DOI:10.1109/IEEECONF44664.2019.9048704`
- Low rank training methods to reduce weight memory writes for training on inference-optimized RRAM devices (ongoing research; draft available on request).
- Multi-modality localization and identification of passive tags for IoT devices (ongoing research).

Stanford University, *Teaching Assistant* *Fall 2018*

- *Analog-Digital Interface Circuits:* Developed and conducted office hours, recorded review sessions, homework, and an ADC design project. Topics covered include sampling and signal processing, analysis of noise in mixed-signal circuits, and ADC/DAC design.

Xilinx, *Machine Learning Intern* *Summer 2017, 2018*

- *Summer 2018:* Improved on state-of-the-art deep RF signal modulation scheme classification accuracy. Developed new methods for quantized training meant for efficient high-accuracy inference on FPGAs. MLSys 2020 conference publication. `https://proceedings.mlsys.org/papers/2020/71`
- *Summer 2017:* Completed two neural network compression projects - (1) 100× condition number improvement of Winograd transforms for convolution layers; (2) 1000× parameter reduction using structured matrix transform technique for fully-connected layers.

Caltech (Azita Emami MICS Lab), *Senior Thesis* *2015-16*

- Novel low-power, high-linearity PLL-based potentiostat for measuring blood glucose levels in TSMC 65nm, published at the VLSI 2017 conference. `DOI:10.23919/VLSIC.2017.8008566`

Caltech (Azita Emami MICS Lab), *Named Summer Undergraduate Research Fellow* *Summer 2015*

- Designed and simulated a novel PLL-based potentiostat for measuring dopamine concentrations *in vivo*.
- Used Cadence Virtuoso with 45nm CMOS predictive models.

California Institute of Technology, *Teaching Assistant* *2014, 2015*

- *Algorithms:* Lectured and created course materials for topics including graph algorithms, greedy algorithms, dynamic programming, flow networks, and linear programming.
- *Electronics Laboratory:* Conducted homework and laboratory sessions in topics including discrete analog components, op-amp circuits, and differential amplifier circuits.

Jane Street Capital, *Software Developer Intern* *Summer 2014*

- Completed two projects - (1) fault-tolerant distributed lock server to replace NFS locks; (2) plugin support for the internal trader tool as well as a plugin ecosystem for trader developers with version control.
- Used OCaml (including the Async monad, RPCs, DynLoader).

Google (Research Division), *Software Engineering Intern* *Summer 2013*

- Developed image processing techniques to clean a sequence of object photos to QA specifications, allowing for a much larger class of object image sequences to be processed; currently for Google Shopping.
- Used C++, OpenCV, and the Ceres non-linear solver library.

Tools and Languages

C, C++, Python (numpy, scipy, scikit-learn, PyTorch, TensorFlow), Mathematica, Matlab, LaTeX, VHDL/Verilog, Java, SPICE, Cadence Virtuoso