ALBERT GURAL

http://www.albertgural.com/

agural@stanford.edu | 703.346.2869

Education

Stanford University   **Stanford, CA**
Ph.D. Electrical Engineering   *Sept. 2016 - present*

- **Murmann Mixed-Signal Group (Boris Murmann)**
- **Selected Coursework:** Fundamentals of Analog Integrated Circuit Design, Principles and Models of Semiconductor Devices
- **Activities/Awards:** The Krishna Kolluri Graduate Fellowship Fund

California Institute of Technology   **Pasadena, CA**
B.S. Electrical Engineering with a minor in Computer Science, GPA: 4.0   *June 2016*

- **Selected Coursework:** Senior Thesis (MICS Lab), Machine Learning and Data Mining, Advanced Digital Systems, Mixed-mode ICs, Feedback and Control Circuits, Signal-Processing Systems
- **Activities/Awards:** ACM-ICPC (international collegiate programming contest - **Honorable Mention** at internationals, *2016, Thailand*; **1st place team** at regionals, *2015*; 4th place team, *2014*), The Kiyo and Eiko Tomiyasu SURF Scholar award (Caltech, *2015*), member of Tau Beta Pi honor society

Work and Experience

Caltech (Azita Emami MICS Lab), *Senior Thesis*   *2015-16*
- Designed a novel low-power, high-linearity PLL-based potentiostat for measuring blood glucose levels.
- Fabricated in TSMC 65nm and successfully tested with glucose solutions *in vitro*.
- Developed an FPGA/NIOS-II testing framework that lead to huge productivity improvements.

Caltech (Azita Emami MICS Lab), *Named Summer Undergraduate Research Fellow*   *Summer 2015*
- Designed and simulated a novel PLL-based potentiostat for measuring dopamine concentrations *in vivo*.
- Used Cadence Virtuoso with 45nm CMOS predictive models.

Jane Street Capital, *Software Developer Intern*   *Summer 2014*
- Completed two projects - (1) fault-tolerant distributed lock server to replace NFS locks; (2) plugin support for the internal trader tool as well as a plugin ecosystem for trader developers with version control.
- Used OCaml (including the Async monad, RPCs, DynLoader).

Google (Research Division), *Software Engineering Intern*   *Summer 2013*
- Developed image processing techniques to clean a sequence of object photos to QA specifications, allowing for a much larger class of object image sequences to be processed; currently for Google Shopping.
- Used C++, OpenCV, and the Ceres non-linear solver library.

California Institute of Technology, *Teaching Assistant*   *2014, 2015*
- *Algorithms:* Lectured and created course materials for topics including graph algorithms, greedy algorithms, dynamic programming, flow networks, and linear programming.
- *Electronics Laboratory:* Conducted homework and laboratory sessions in topics including discrete analog components, op-amp circuits, and differential amplifier circuits.

Projects

Schematic and layout of implantable Potentiostat, fabricated in TSMC 65nm	*Spring 2016*
Design and construction of reflow oven utilizing a fully-analog PI-controller	*Spring 2016*
Potentiostat utilizing an all-digital phase-locked loop in 45nm CMOS technology	*Summer 2015*
Design and construction of 1kW Solid-state Tesla coil	*Summer 2015*
6-8 GHz all-digital delay-locked loop in 45nm CMOS technology, *group project*	*Spring 2015*
8-bit AVR-compatible processor in VHDL for a Xilinx FPGA, *group project*	*Winter 2015*
5MHz bandwidth FPGA-based oscilloscope, designed and built from scratch	*Spring 2014*
Robotrike firmware (interrupt-based OS written exclusively in x86 assembly)	*Fall 2013*

Tools and Languages

C/C++, VHDL/Verilog, Java, Python, OCaml, Haskell, x86 Assembly, LaTeX, Mathematica, Git, Bash, OpenCV, MPI (parallelization platform), Altium, Altera and Xilinx toolchains, SPCIE, Cadence Virtuoso