

Vietnam National University Ho Chi Minh City
HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY



LAB 1:
MOS TRANSISTOR CHARACTERIZATION

Subject: Digital IC Design

Class L03 --- Semester 242

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Lecturer: PhD. Tran Hoang Linh

Ho Chi Minh City, 03-2025

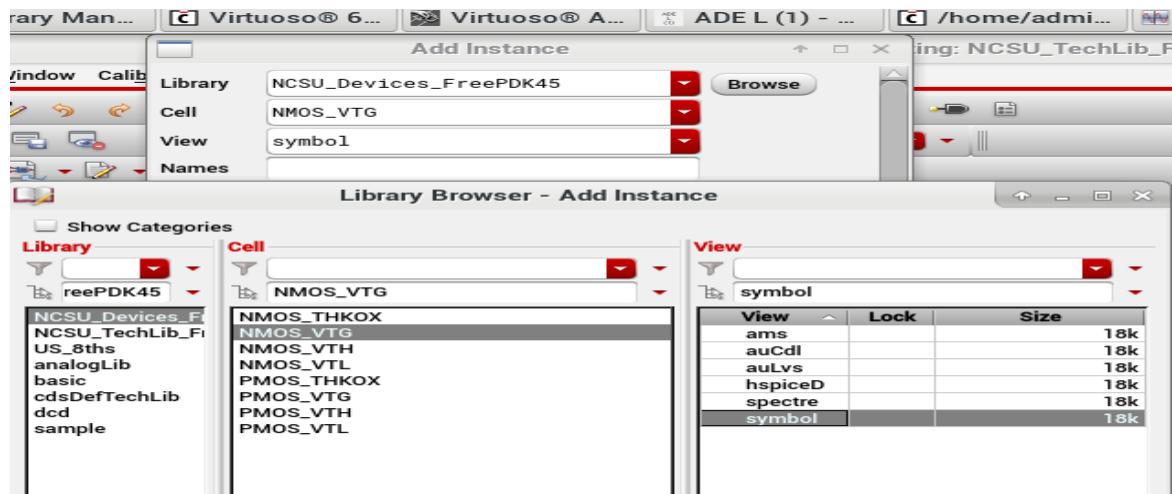
1.EXPERIMENT 1

Objective: Investigate the I-V characteristics of MOS transistors.

Requirements: Simulate the I_D vs V_{GS} and I_D vs V_{DS} characteristics of NMOS_VTG and PMOS_VTG transistors using FreePDK45.

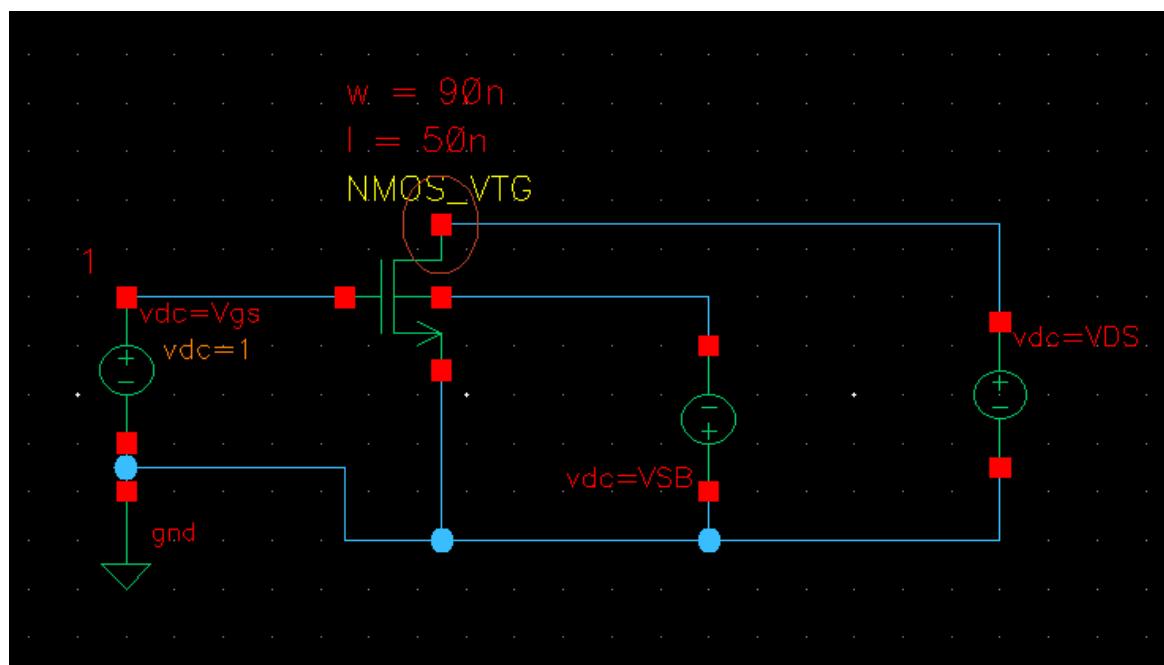
1.1 NMOS_VTG

Choose Nmos in NCSU_Devices_FreePDK45 library



1.1.1 Simulate the I_D vs V_{DS} characteristics of NMOS_VTG

Drawing schematic:



Setting parameters: ADE L, Outputs, M0/D position:

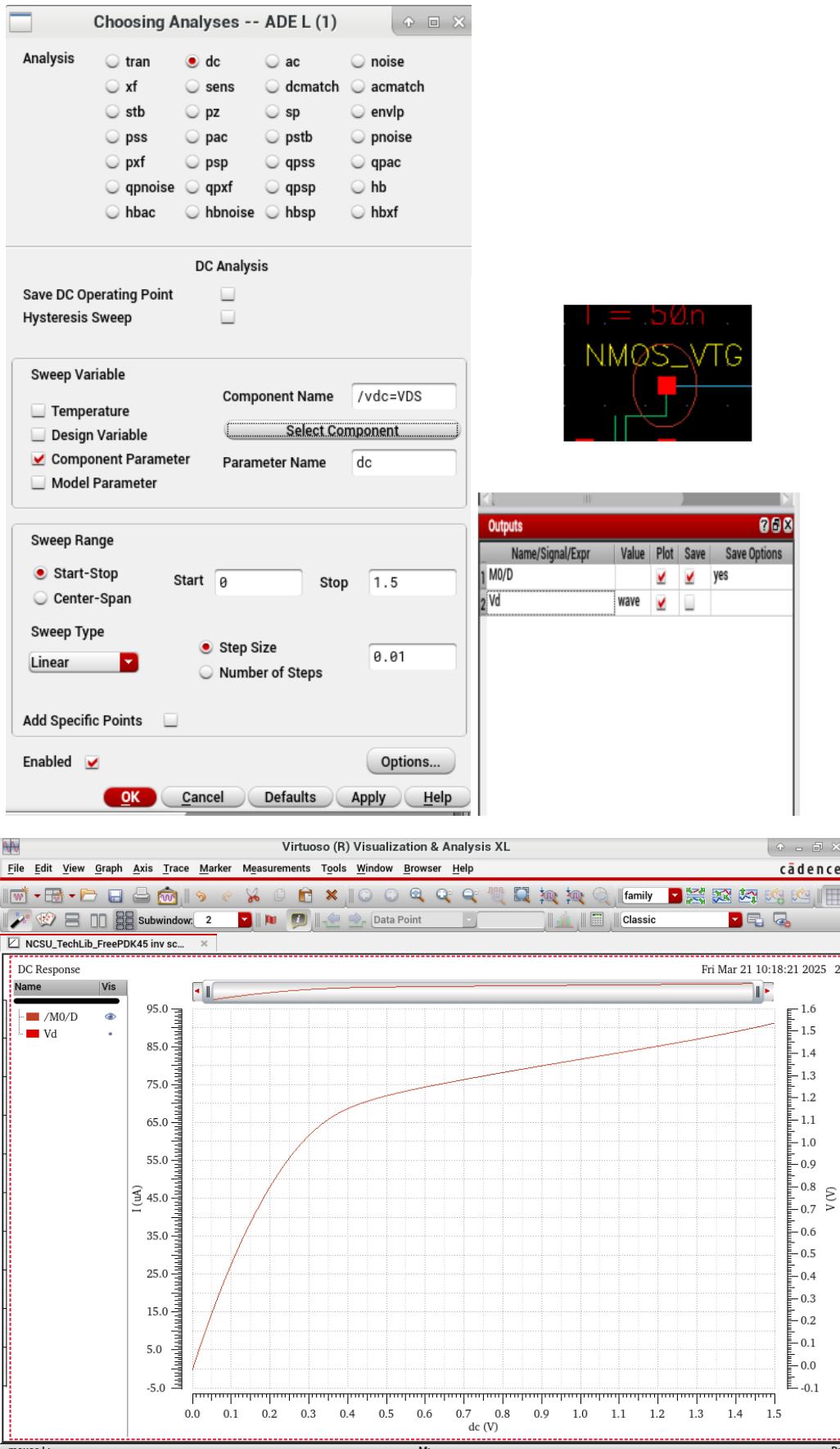
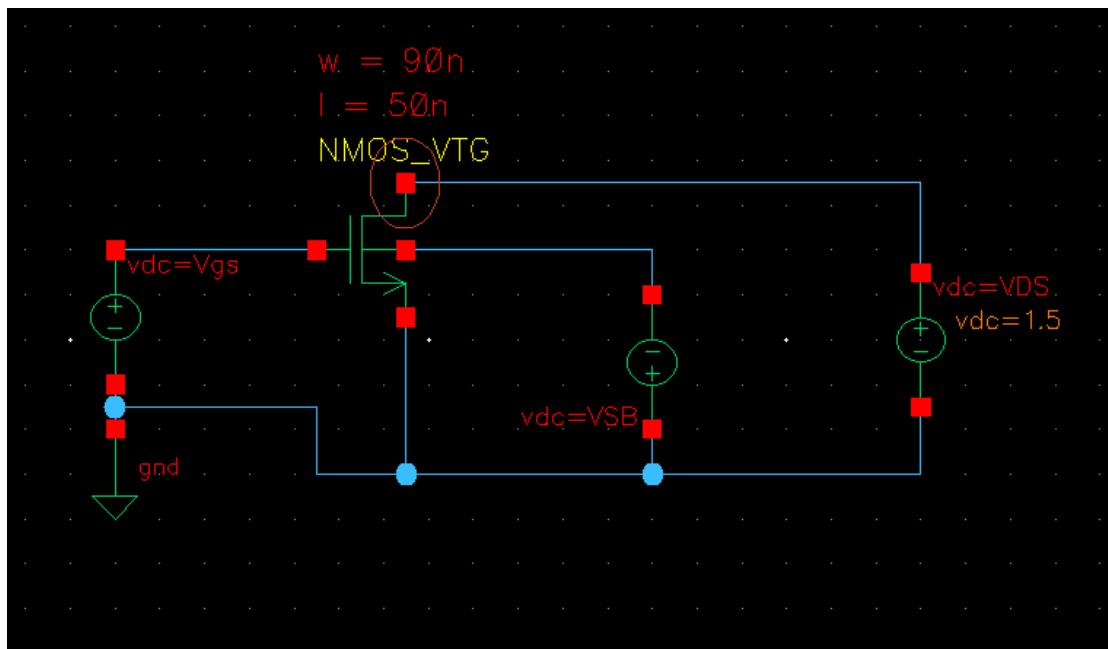


Figure 1.1 Simulate curves I_D vs V_{DS} at $V_{GS} = 1V$, sweeping V_{DS} from $0V$ to $1.5V$ with a step of $10mV$

1.1.2 Simulate the I_D vs V_{GS} characteristics of NMOS_VTG

Drawing schematic



Setting parameters: ADE L, Outputs, M0/D position

Choosing Analyses -- ADE L (1)

<input type="radio"/> tran	<input checked="" type="radio"/> dc	<input type="radio"/> ac	<input type="radio"/> noise
<input type="radio"/> xf	<input type="radio"/> sens	<input type="radio"/> dcmatch	<input type="radio"/> acmatch
<input type="radio"/> stb	<input type="radio"/> pz	<input type="radio"/> sp	<input type="radio"/> envlp
<input type="radio"/> pss	<input type="radio"/> pac	<input type="radio"/> pstb	<input type="radio"/> pnoise
<input type="radio"/> pxf	<input type="radio"/> psp	<input type="radio"/> qpss	<input type="radio"/> qpac
<input type="radio"/> qnoise	<input type="radio"/> qpxf	<input type="radio"/> qpsp	<input type="radio"/> hb
<input type="radio"/> hbac	<input type="radio"/> hnoise	<input type="radio"/> hbsp	<input type="radio"/> hbxf

DC Analysis

Save DC Operating Point
Hysteresis Sweep

Sweep Variable

Temperature Component Name /vdc=Vgs
 Design Variable **Select Component...**
 Component Parameter Parameter Name dc
 Model Parameter

Sweep Range

Start-Stop Start 0 Stop 1.5
 Center-Span

Sweep Type

Linear Step Size 0.01 Number of Steps

Add Specific Points

Enabled Options... OK Cancel Defaults Apply Help

w = 90n
l = 50n
NMOS_VTG

Outputs

Name/Signal/Expr	Value	Plot	Save	Save Options
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2 Vd	Wave	<input checked="" type="checkbox"/>	<input type="checkbox"/>	

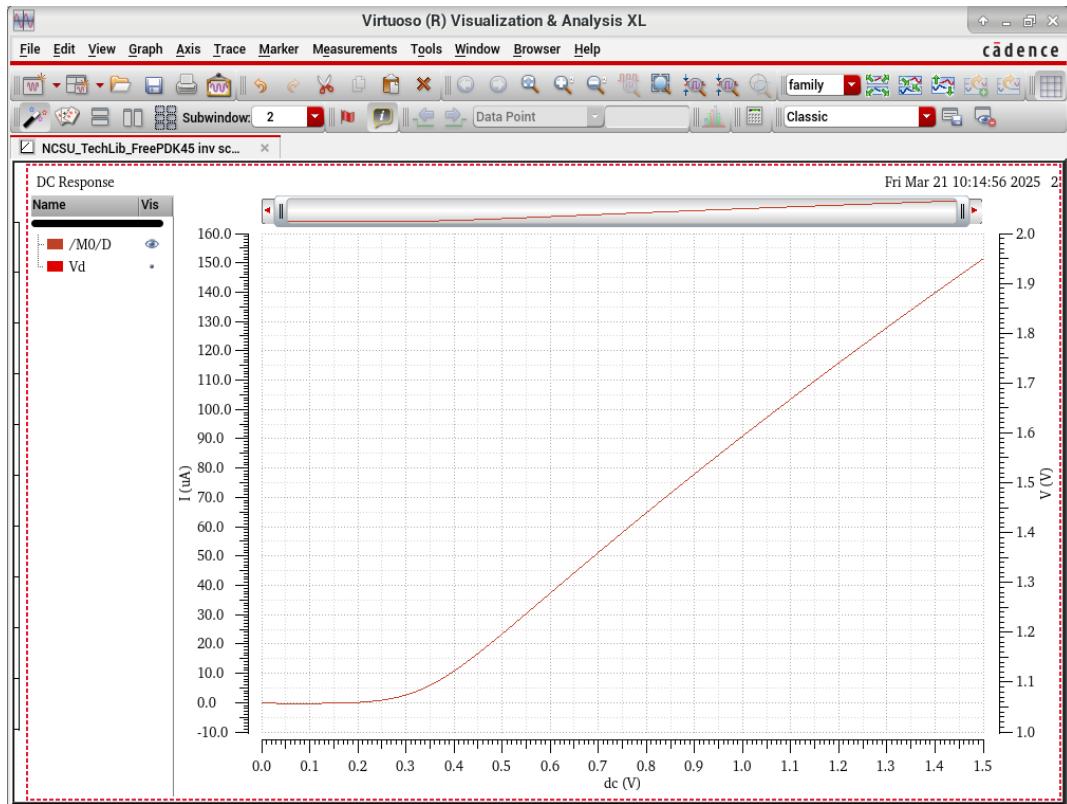
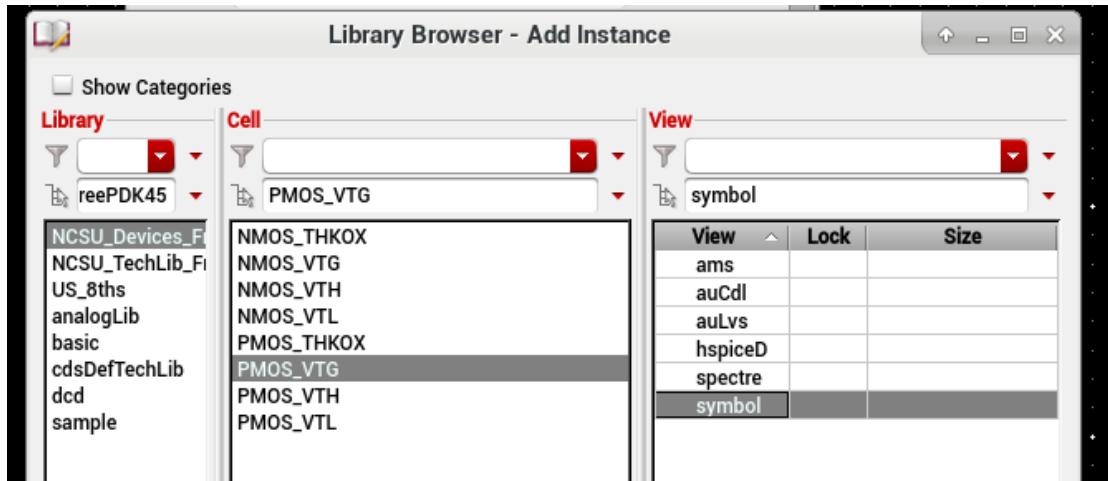


Figure 1.1.2 Simulate curves I_D vs V_{GS} at $V_{DS} = 1.5V$, sweeping V_{GS} from $0V$ to $1.5V$ with a step of $10mV$.

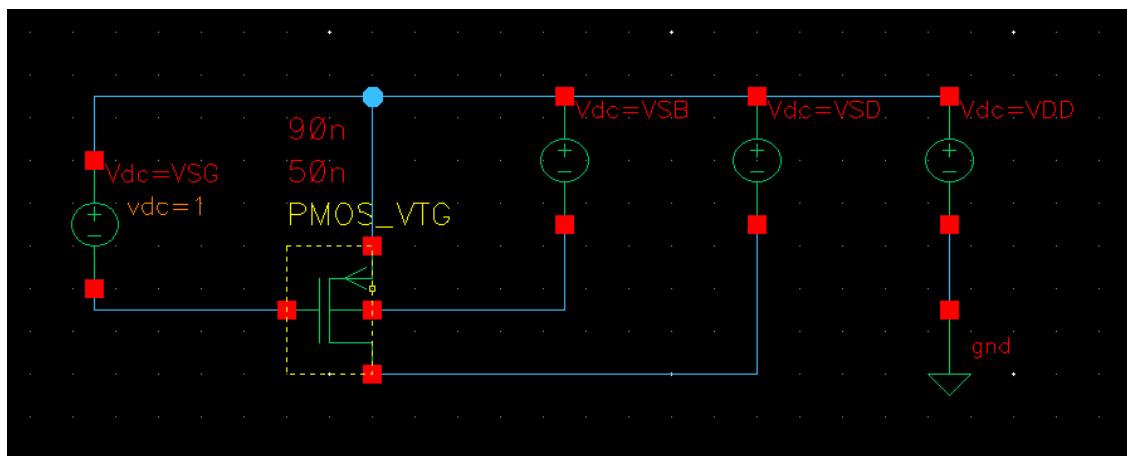
1.2 PMOS_VTG

Choose Pmos in NCSU_Devices_FreePDK45 library



1.2.1 Simulate the I_D vs V_{SD} characteristics of PMOS_VTG

Drawing schematic:



Setting parameters: ADE L, Outputs, M0/D position

Choosing Analyses -- ADE L (2)

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	<input type="radio"/> stb	<input type="radio"/> pz	<input type="radio"/> sp	<input type="radio"/> envlp
	<input type="radio"/> pss	<input type="radio"/> pac	<input type="radio"/> pstb	<input type="radio"/> pnoise
	<input type="radio"/> pxf	<input type="radio"/> psp	<input type="radio"/> qpss	<input type="radio"/> qpac
	<input type="radio"/> qnoise	<input type="radio"/> qpxf	<input type="radio"/> qpsp	<input type="radio"/> hb
	<input type="radio"/> hbac	<input type="radio"/> hbnoise	<input type="radio"/> hbsp	<input type="radio"/> hbxf

DC Analysis

Save DC Operating Point
Hysteresis Sweep

Sweep Variable

<input type="checkbox"/> Temperature	Component Name: /Vdc=VSD
<input type="checkbox"/> Design Variable	<input type="button" value="Select Component"/>
<input checked="" type="checkbox"/> Component Parameter	Parameter Name: dc
<input type="checkbox"/> Model Parameter	

Sweep Range

Start-Stop Start: 0 Stop: 1.5

Center-Span

Sweep Type

Linear
 Number of Steps

Add Specific Points

Enabled

Outputs

Name/Signal/Expr	Value	Plot	Save	Save Options
1 M0/D	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
2 V	wave	<input checked="" type="checkbox"/>	<input type="checkbox"/>	

Buttons: OK, Cancel, Defaults, Apply, Help

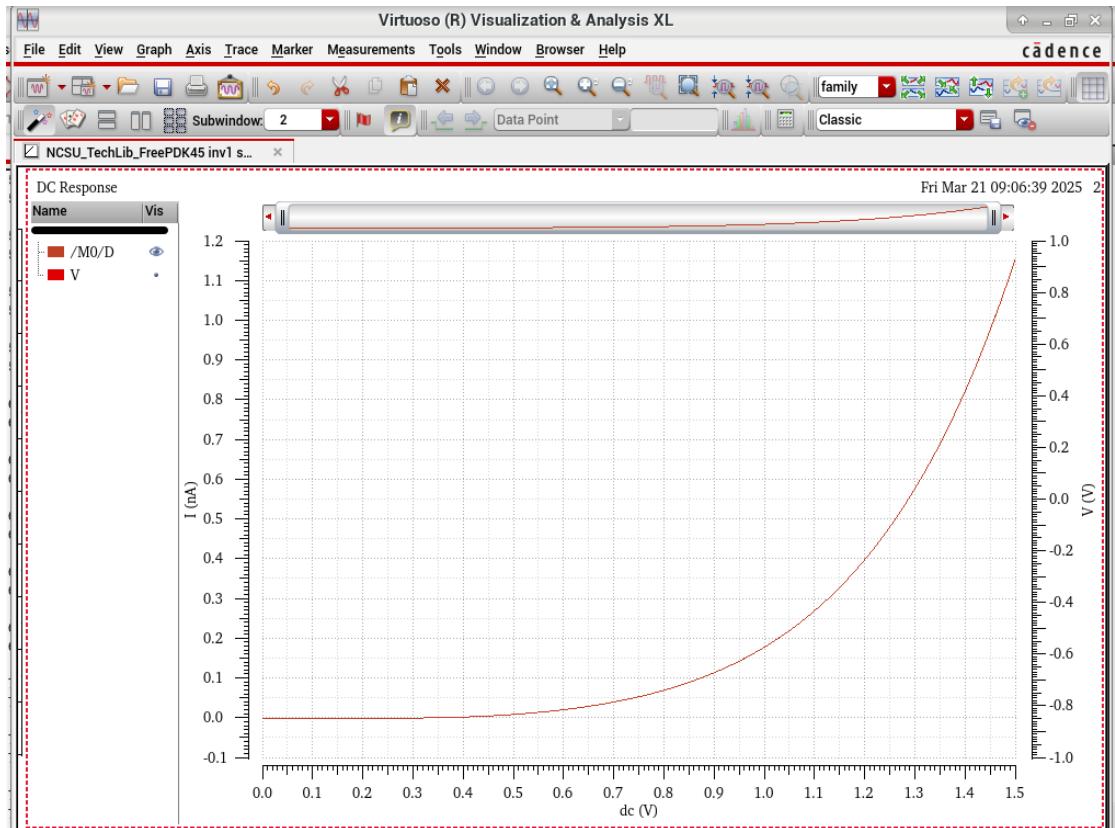
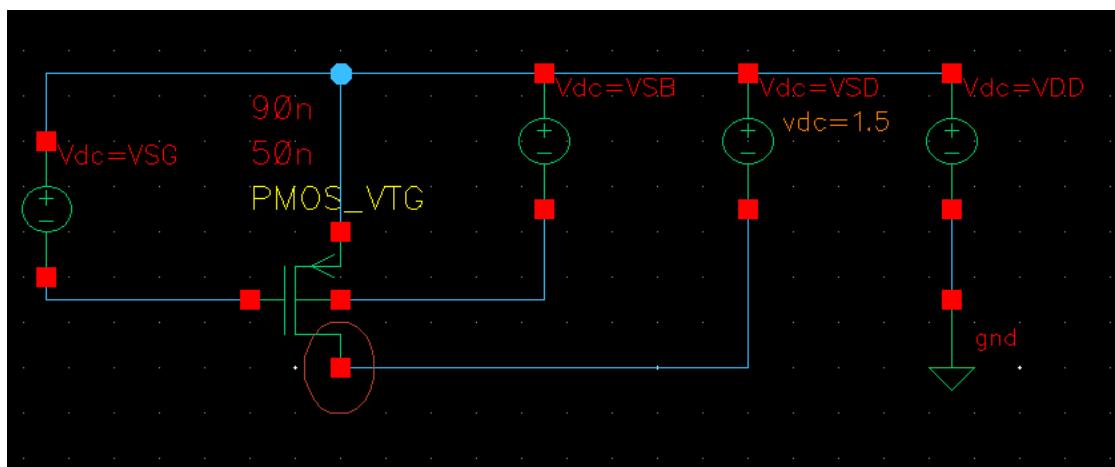


Figure 1.2.1 Simulate curves I_D vs V_{SD} at $V_{SG} = 1V$, sweeping V_{SD} from $0V$ to $1.5V$ with a step of $10mV$.

1.2.2 Simulate the I_D vs V_{SG} characteristics of PMOS_VTG

Drawing schematic



Setting parameters: ADE L, Outputs, M0/D position

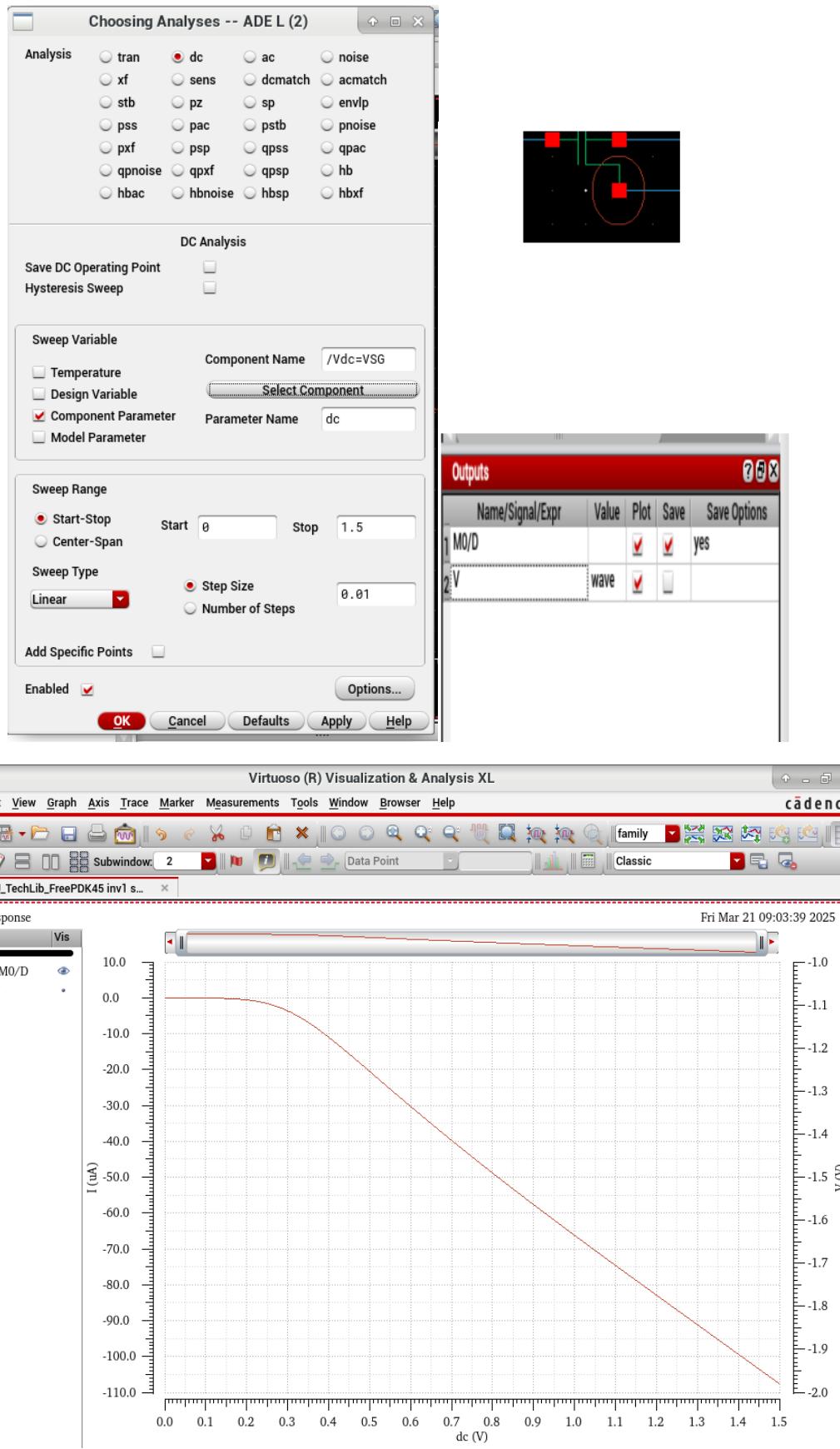


Figure 1.2.2 Simulate curves I_D vs V_{SG} at $V_{SD} = 1.5V$, sweeping V_{SG} from 0V to 1.5V with a step of 10mV.

Questions:

1. Based on the I_D vs V_{GS} characteristics, please estimate the threshold voltage V_{GS} of the NMOS transistor.

When $V_{GS} < V_T$, the drain current I_D is nearly zero, because the conduction channel has not yet formed.

When $V_{GS} \approx V_T$, the drain current I_D begins to increase from a very small value.

When $V_{GS} > V_T$, I_D increases rapidly according to the characteristics of a MOSFET.

From the graph, we can observe that I_D begins to increase significantly when V_{GS} is approximately 0.2 to 0.3V. This is an indication that the conduction channel has started to form, meaning $V_T \approx 0.2$ to 0.3V.

2. Additionally, by analyzing the I_D vs V_{GS} characteristics, determine the conduction region of the NMOS transistor when V_{GS} exceeds V_{GS} . Specify whether the device operates in the linear (triode) region or the saturation region, and provide an explanation.

When V_{GS} exceeds $V_{GS(th)}$:

- Linear (Triode) Region

- Condition:

$$V_{GS} > V_{GS(th)} \text{ and } V_{DS} < (V_{GS} - V_{GS(th)})$$

The MOSFET behaves like a variable resistor, and the drain current is given by:

- $I_D = \frac{1}{2}k(V_{GS} - V_{GS(th)} - \frac{V_{DS}}{2})V_{DS}$
- In this region, increasing V_{DS} results in a nearly linear increase in I_D .

- Saturation (Active) Region

- Condition:

$$V_{GS} > V_{GS(th)} \text{ and } V_{DS} \geq (V_{GS} - V_{GS(th)})$$

The transistor behaves like a current source, and I_D follows the quadratic equation:

- $I_D = \frac{1}{2}k(V_{GS} - V_{GS(th)})^2$
- Here, I_D is mostly independent of V_{DS} .

- From the I_D vs V_{GS} characteristics, we can observe that:

- If $V_{GS} > 1.8V$, the MOSFET operates in the linear (triode) region.
- If $V_{GS} \leq 1.8V$, the MOSFET operates in the saturation region.

3. Based on Figure 3, qualitatively determine the operating regions of the NMOS transistor.

When V_{DS} is small, the drain current I_D increases almost linearly with V_{DS} , indicating that the NMOS is operating in the linear region. When V_{DS} continues to increase and exceeds $V_{GS} - V_T$, the drain current I_D begins to saturate and increases more slowly, which is characteristic of the saturation region.

Based on the graph, when $V_{DS} \approx 0.7V$, the current begins to saturate, confirming the transition point from the linear region to the saturation region.

4. When the NMOS transistor is biased in the saturation region, does the drain current remain constant? Provide a theoretical explanation.

In reality, due to channel length modulation, I_D exhibits a slight increase with V_{DS} .

- A modified equation incorporating channel length modulation is:

$$I_D = \frac{1}{2}k (V_{GS} - V_{GS(th)})^2 (1 + \lambda V_{DS})$$

where λ (channel length modulation parameter) determines how much I_D increases with V_{DS} .

- If λ is small, the transistor behaves like an ideal current source.
- If λ is large, I_D increases more significantly with V_{DS} .

Conclusion

- For short-channel transistors (modern MOSFETs with small channel lengths), λ is significant, so I_D increases noticeably in saturation.
- For long-channel transistors, λ is small, and I_D is nearly constant.

5. Propose methods to reduce the slope of the drain current when the NMOS operates in the saturation region.

Increasing channel length (L): When the channel length L increases, the channel length modulation effect decreases, making the drain current I_D less affected by V_{DS} .

Reducing V_{DS} voltage: If V_{DS} is not too large, the expansion of the depletion region at the drain terminal will have less impact on the effective channel length, helping to reduce the slope of I_D .

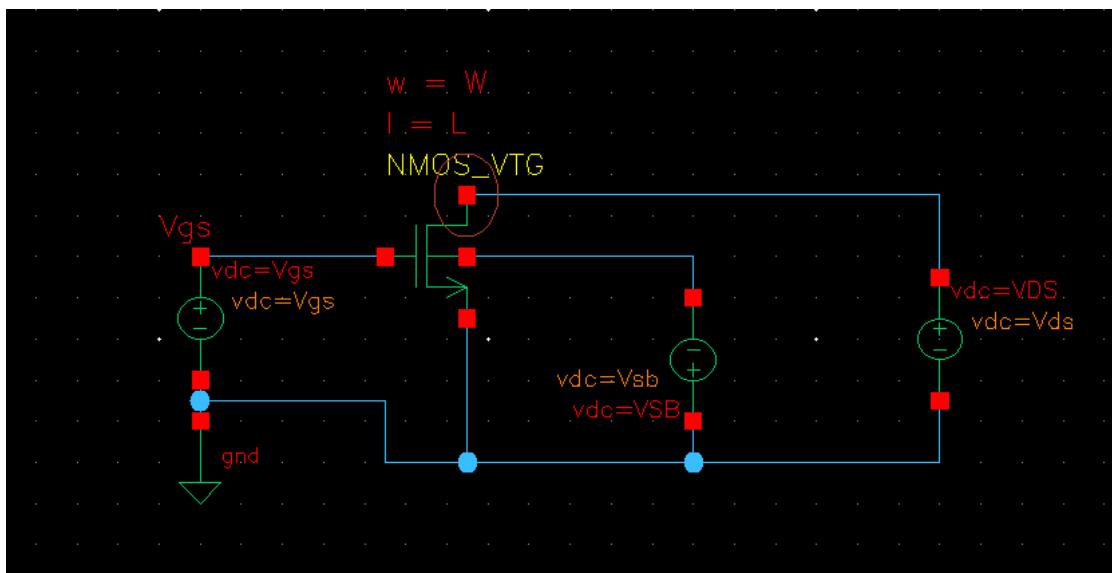
2. EXPERIMENT 2

Objective: Effects of varying VGS and device size.

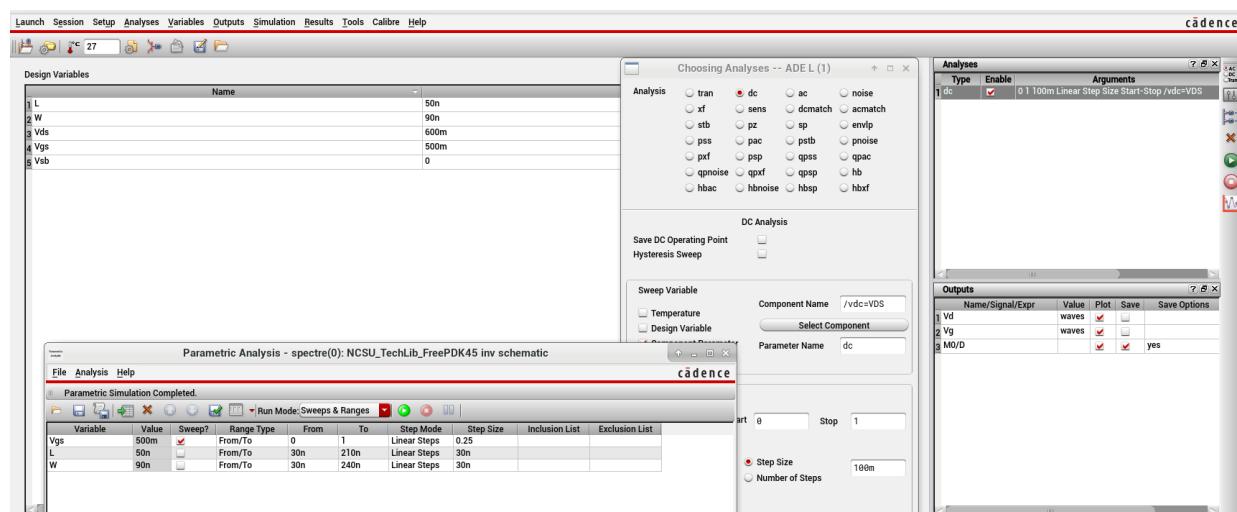
Requirements: Simulate the I_D vs V_GS and I_D vs V_DS characteristics of NMOS_VTG and PMOS_VTG transistors using FreePDK45 and analyze the impact of these parameters.

2.1 NMOS_VTG

Drawing schematic



Setting parameters:



Result:

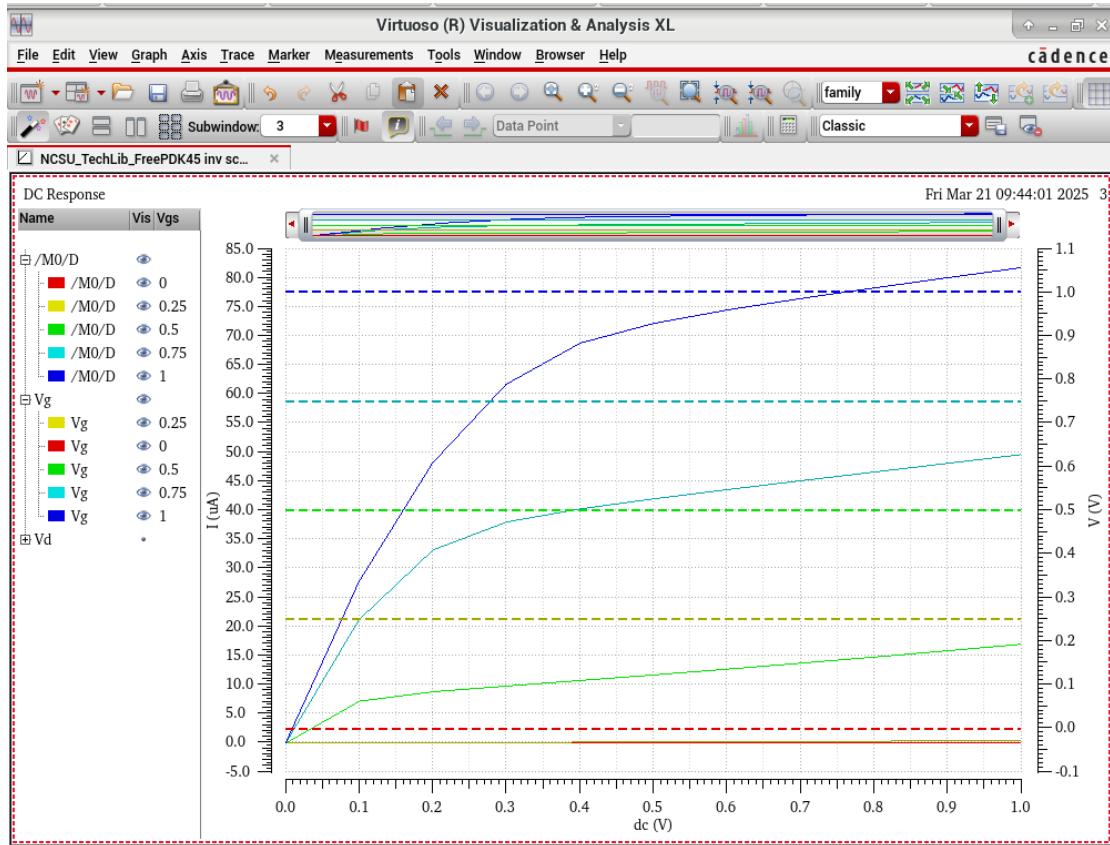


Figure 2.1.1 Simulate curves I_D vs V_{GS} for V_{GS} sweeping from 0V to 1V with a step of 0.25V.

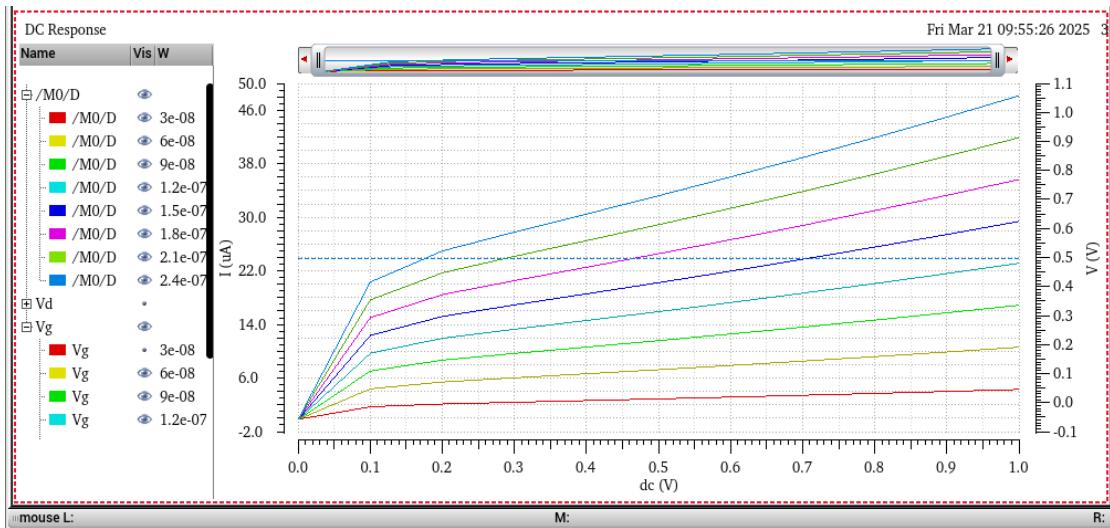


Figure 2.1.2 Simulate curves I_D vs V_{DS} for W sweeping from 30nm to 210nm with a step of 30nm.

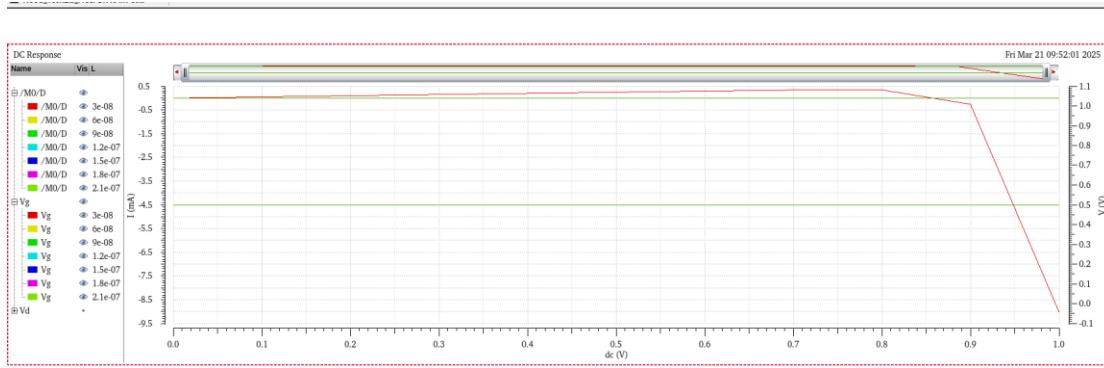
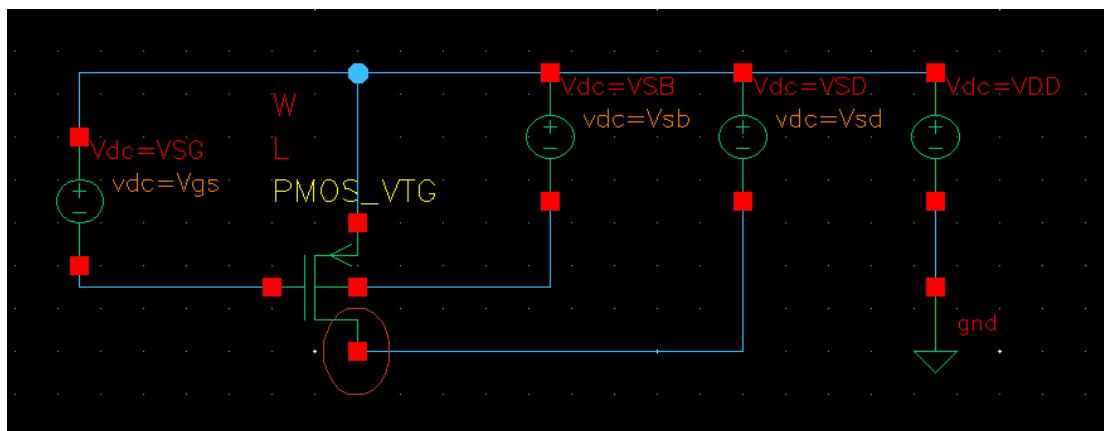


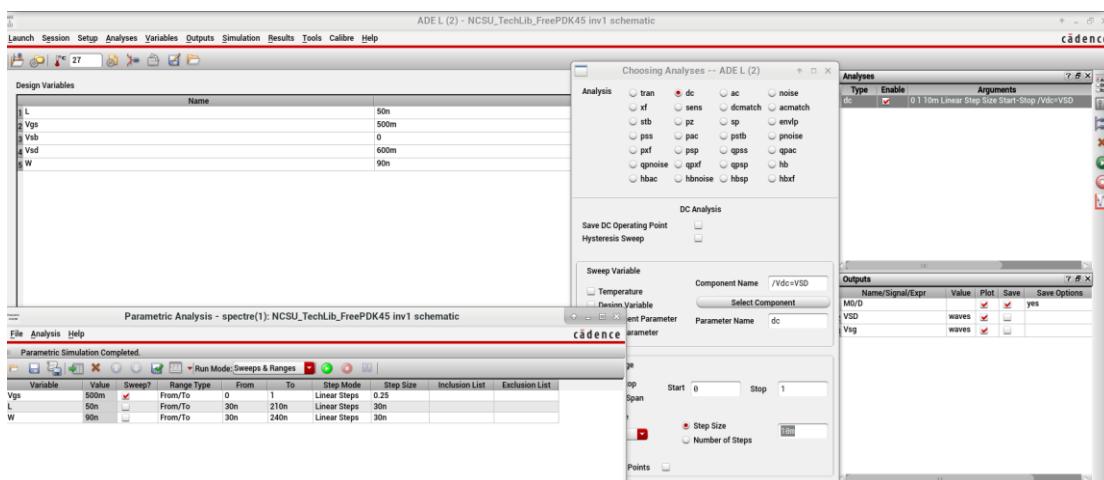
Figure 2.1.3 Simulate curves I_D vs V_{DS} for L sweeping from 30nm to 240nm with a step of 30nm.

2.2 PMOS_VTG

Drawing schematic



Setting parameters:



Result:

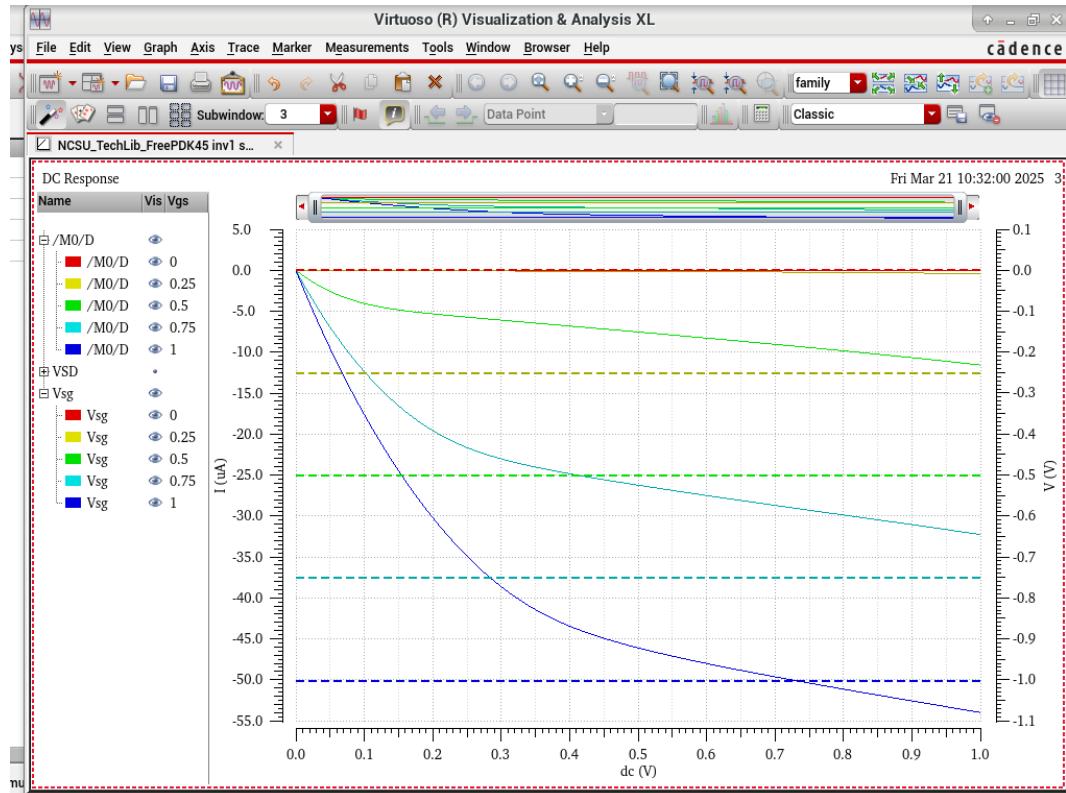


Figure 2.2.1 Simulate curves I_D vs V_{SD} for W sweeping from 30nm to 210nm with a step of 30nm.

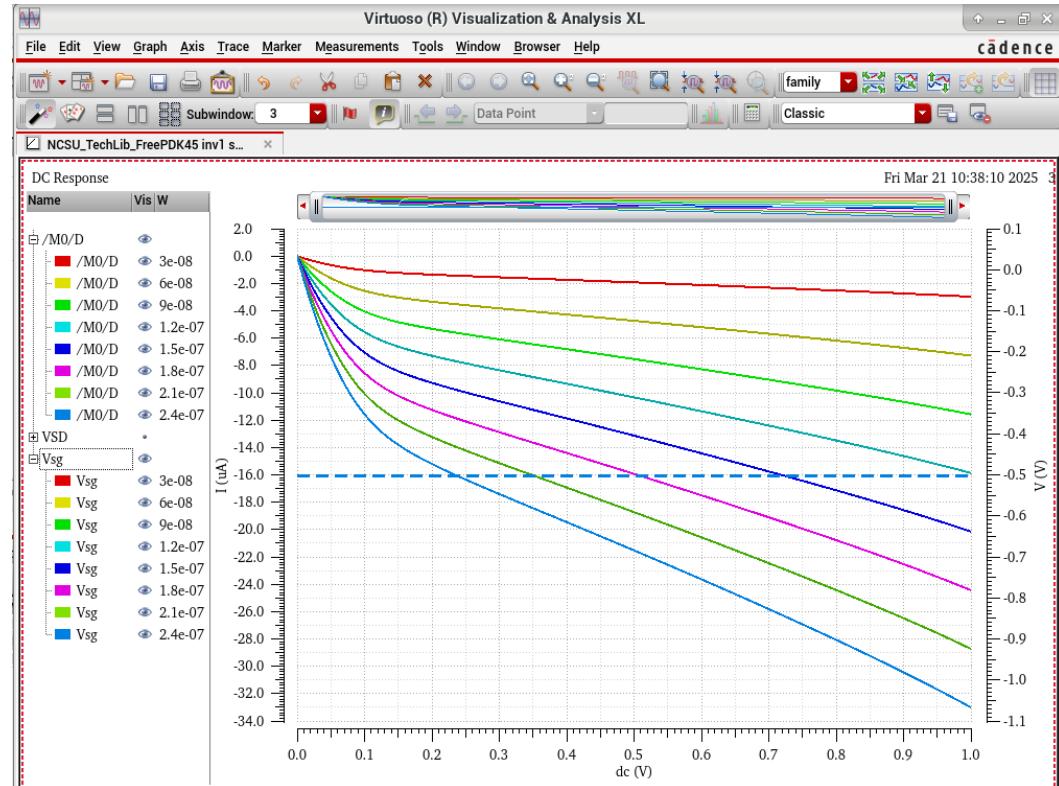


Figure 2.2.2 Simulate curves I_D vs V_{SD} for W sweeping from 30nm to 210nm with a step of 30nm.

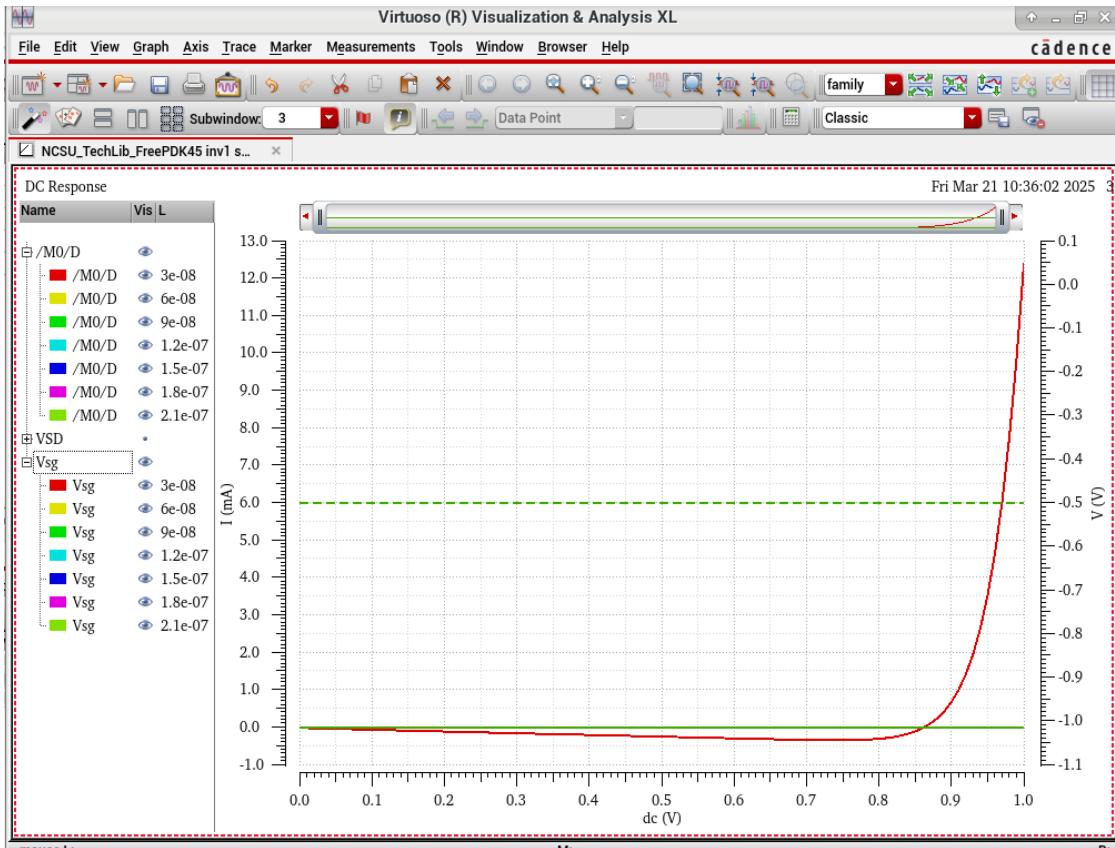


Figure 2.2.3 Simulate curves I_D vs V_{SD} for L sweeping from 30nm to 240nm with a step of 30nm.

EXPERIMENT 3:

Objective: Explore second-order effects (Body effect, Channel-length modulation).

Requirements:

- Simulate the I_D vs V_{GS} and I_D vs V_{DS} characteristics of NMOS_VTG and PMOS_VTG transistors using FreePDK45 and analyze the impact of these parameters.
- Measure, and analyze device characteristics: λ , V_{Th0} , k_p , and γ .

3.1 Simulate the I_D vs V_{GS} and I_D vs V_{DS} characteristics of NMOS_VTG:

- Draw a schematic for the NMOS testbench:

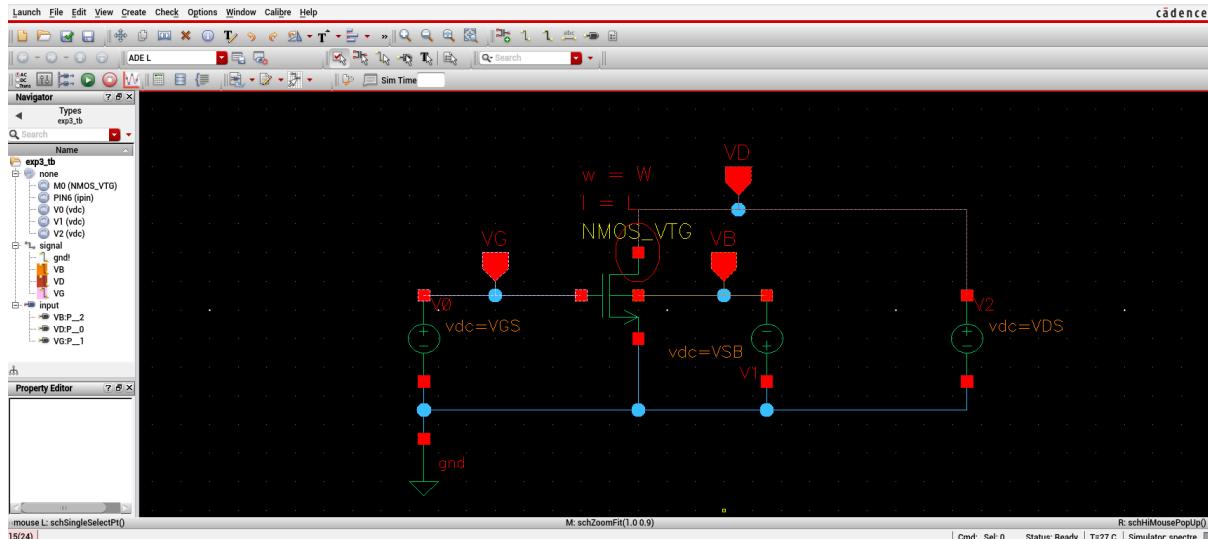


Figure 3.1.1: NMOS testbench

- Set the parameters according to the requirements:

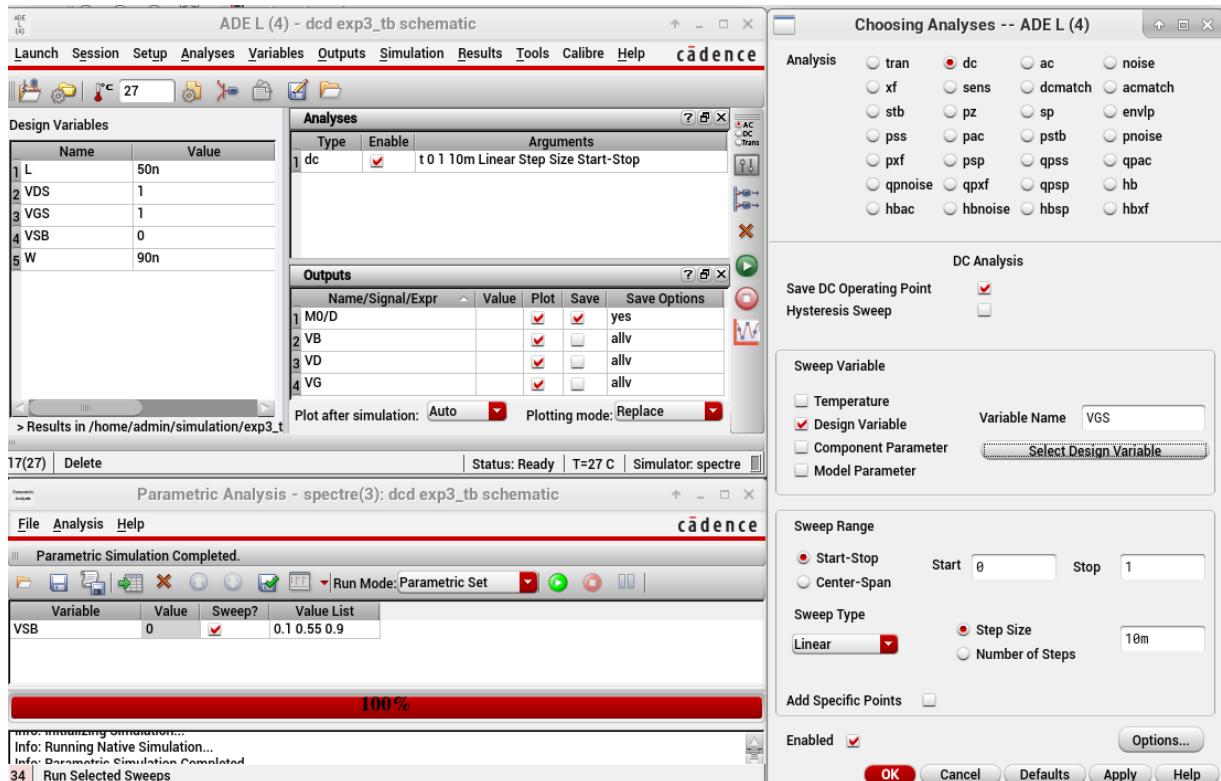


Figure 3.1.2: Setting for drawing I_D vs V_{GS} @ $V_{DS} = 1V$, $V_{SB} = \{0.1, 0.55, 0.9\} V$ and sweeping $V_{GS} = [0,1] V$ step 10mV

- Draw curves I_D vs V_{GS} @ $V_{DS} = 1V$, $V_{SB} = \{0.1, 0.55, 0.9\} V$, and sweeping $V_{GS} = [0,1] V$ with step 10mV:

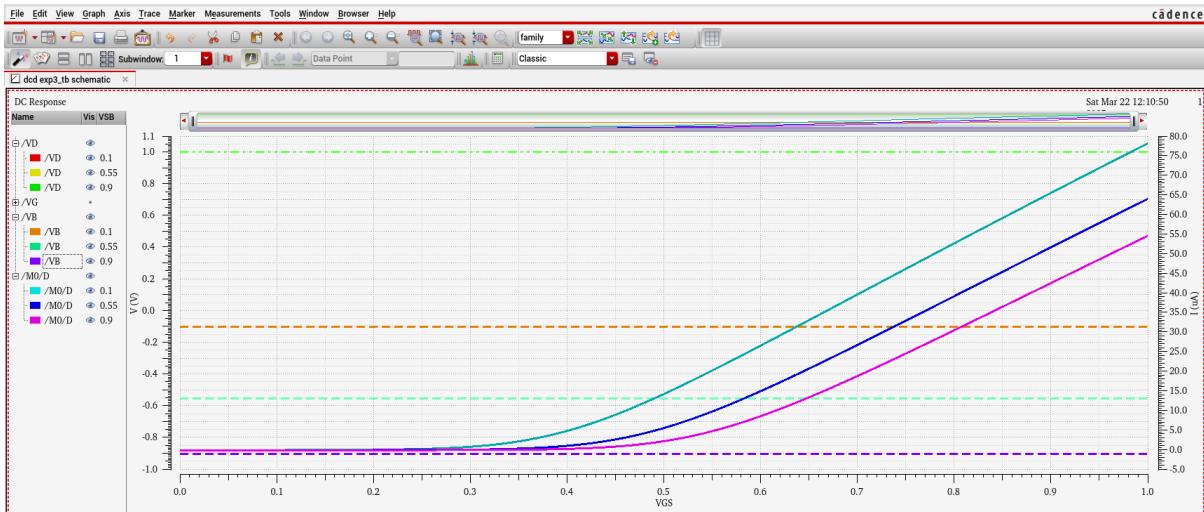


Figure 3.1.3: I_D vs V_{GS} @ $V_{DS} = 1V$, $V_{SB} = \{0.1, 0.55, 0.9\} V$, and sweeping $V_{GS} = [0, 1] V$ with step 10mV

$\Rightarrow V_{SB}$ affects the charge required to invert the channel: Increasing V_s or decreasing V_b increases V_t :

$$V_t = V_{t0} + \gamma(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s})$$

\Rightarrow Decreasing I_D : $I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2(1 + \lambda V_{ds})$ with increasing V_{SB} .

- Similarly, for curves I_D vs V_{DS} @ $V_{GS} = 1V$, $V_{SB} = \{0.1, 0.55, 0.9\} V$ and sweeping $V_{DS} = [0, 1] V$ step 10mV:

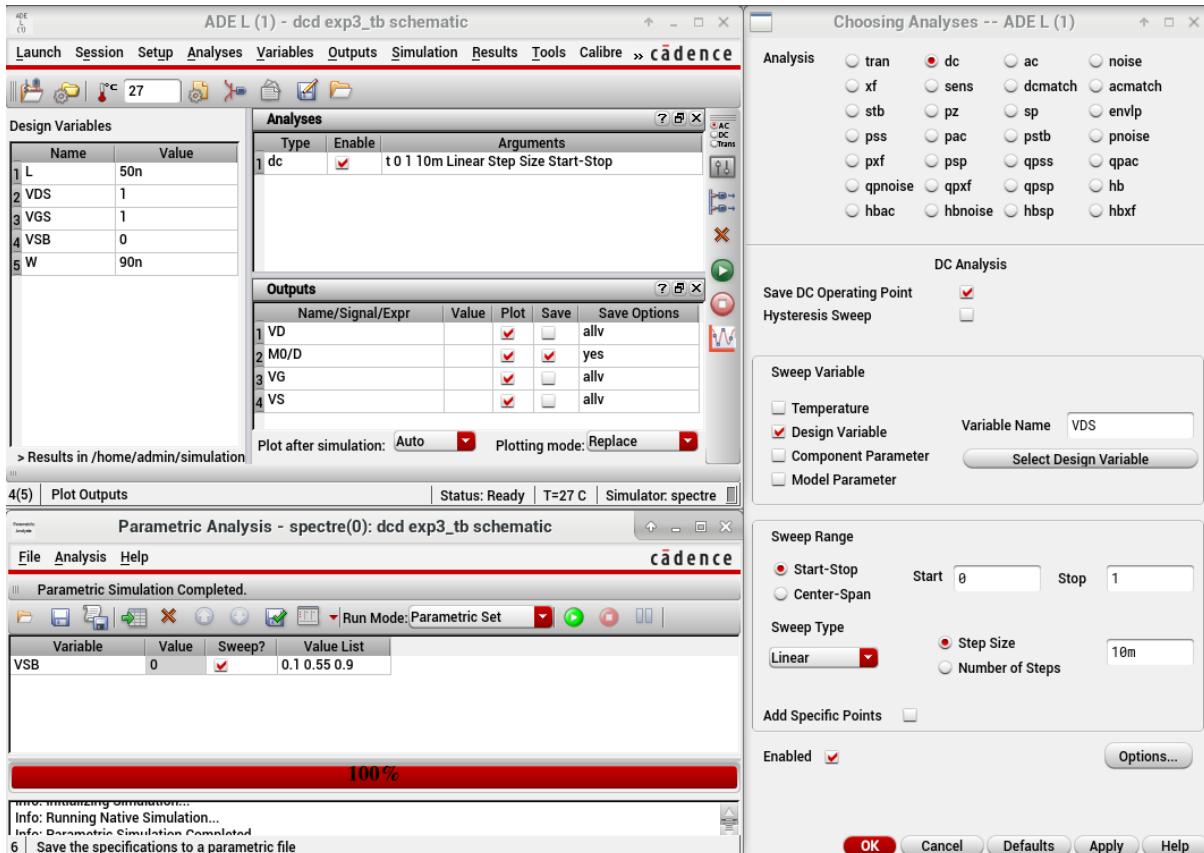


Figure 3.1.4: Setting for drawing I_D vs V_{DS} @ $V_{GS} = 1V$, $V_{SB} = \{0.1, 0.55, 0.9\} V$ and sweeping $V_{DS} = [0,1] V$ step 10mV

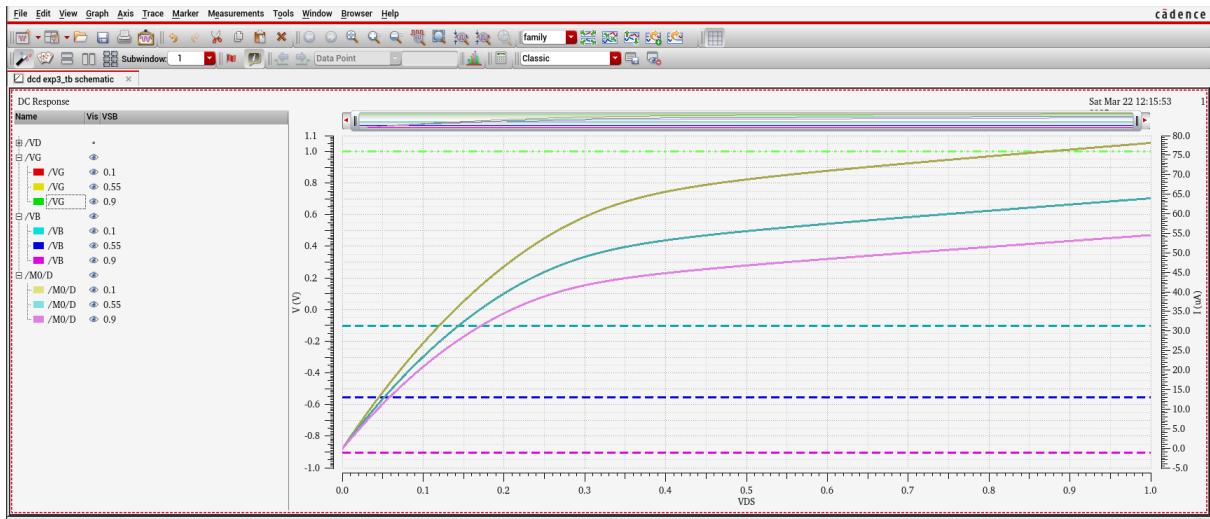


Figure 3.1.5: I_D vs V_{DS} @ $V_{GS} = 1V$, $V_{SB} = \{0.1, 0.55, 0.9\} V$ and sweeping $V_{DS} = [0,1] V$ step 10mV

$\Rightarrow V_{SB}$ affects the charge required to invert the channel: Increasing V_s or decreasing V_b increases V_t :

$$V_t = V_{t0} + \gamma(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s})$$

\Rightarrow Decreasing I_D : $I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2(1 + \lambda V_{ds})$ with increasing V_{SB} .

3.2 Simulate the I_D vs V_{GS} and I_D vs V_{DS} characteristics of PMOS_VTG:

- Draw a schematic for the NMOS testbench:

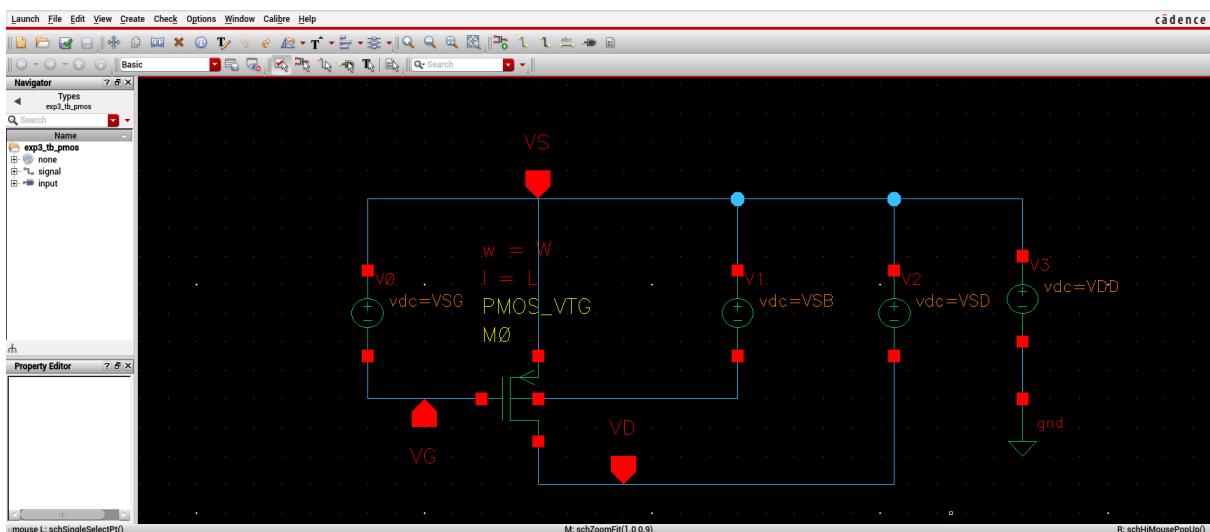


Figure 3.2.1: PMOS testbench

- Set the parameters according to the requirements:

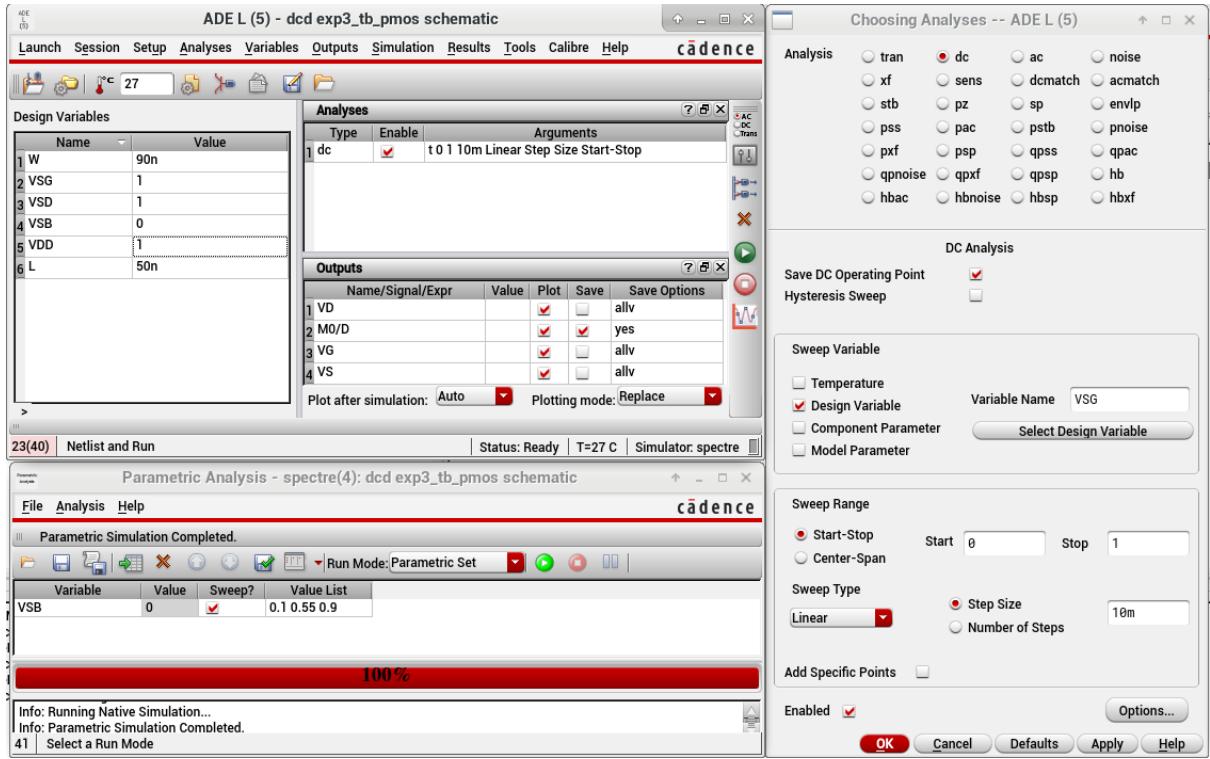


Figure 3.2.2: Setting for drawing I_D vs V_{SG} @ $V_{SD} = 1V$, $V_{SB} = \{0.1, 0.55, 0.9\} V$ and sweeping $V_{SG} = [0,1] V$ step 10mV

- Draw curves I_D vs V_{SG} @ $V_{SD} = 1V$, $V_{SB} = \{0.1, 0.55, 0.9\} V$ and sweeping $V_{SG} = [0,1] V$ step 10mV:

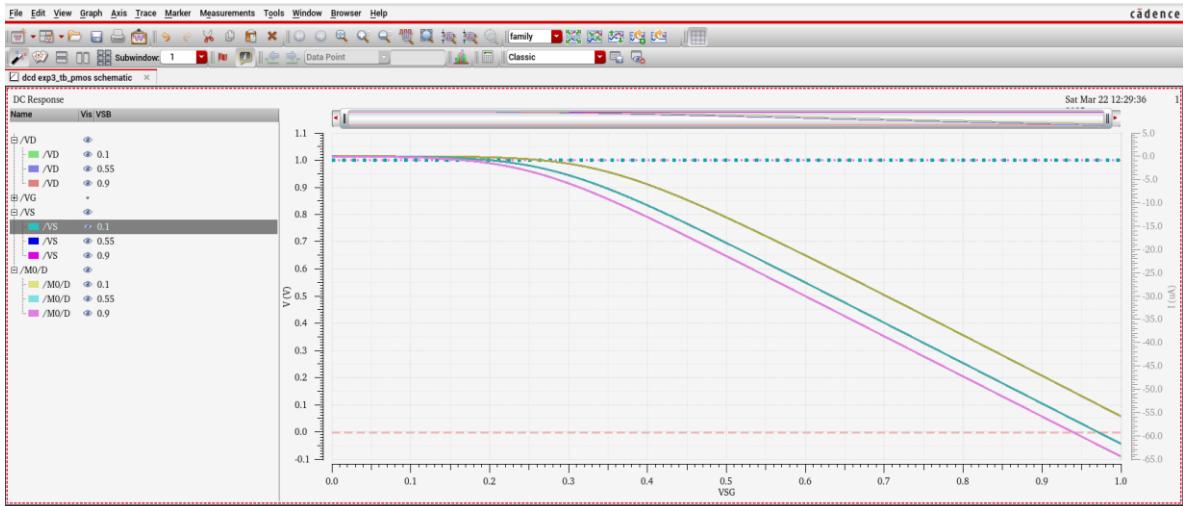


Figure 3.2.3: I_D vs V_{SG} @ $V_{SD} = 1V$, $V_{SB} = \{0.1, 0.55, 0.9\} V$ and sweeping $V_{SG} = [0,1] V$ step 10mV

⇒ V_{SB} affects the charge required to invert the channel: Increasing V_s or decreasing V_b increases V_t :

$$V_t = V_{to} - \gamma(\sqrt{\phi_s + V_{bs}} - \sqrt{\phi_s})$$

=> Decreasing I_D : $I_D = \frac{\beta}{2} (V_{gs} - V_t)^2 (1 + \lambda |V_{ds}|)$ with increasing V_{SB} .

- Similarly, for curves I_D vs V_{SD} @ $V_{SG} = 1V$, $V_{SB} = \{0.1, 0.55, 0.9\} V$ and sweeping $V_{SD} = [0,1] V$ step 10mV

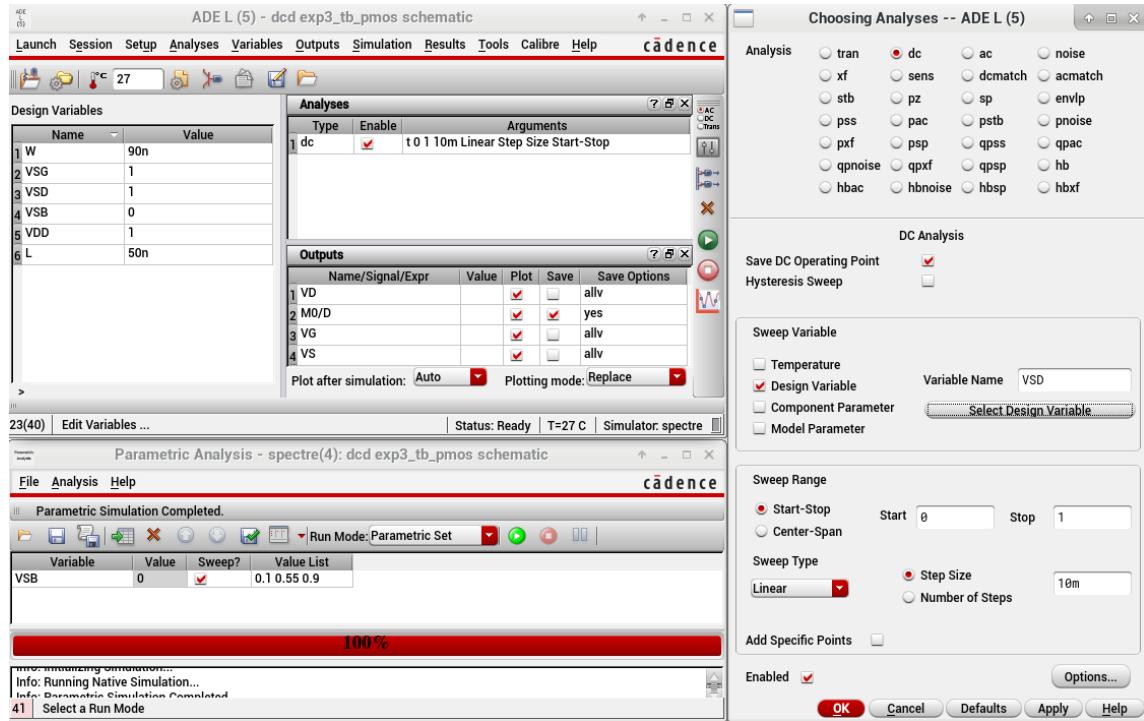


Figure 3.2.4: Setting for drawing I_D vs V_{SD} @ $V_{SG} = 1V$, $V_{SB} = \{0.1, 0.55, 0.9\} V$ and sweeping $V_{SD} = [0,1] V$ step 10mV

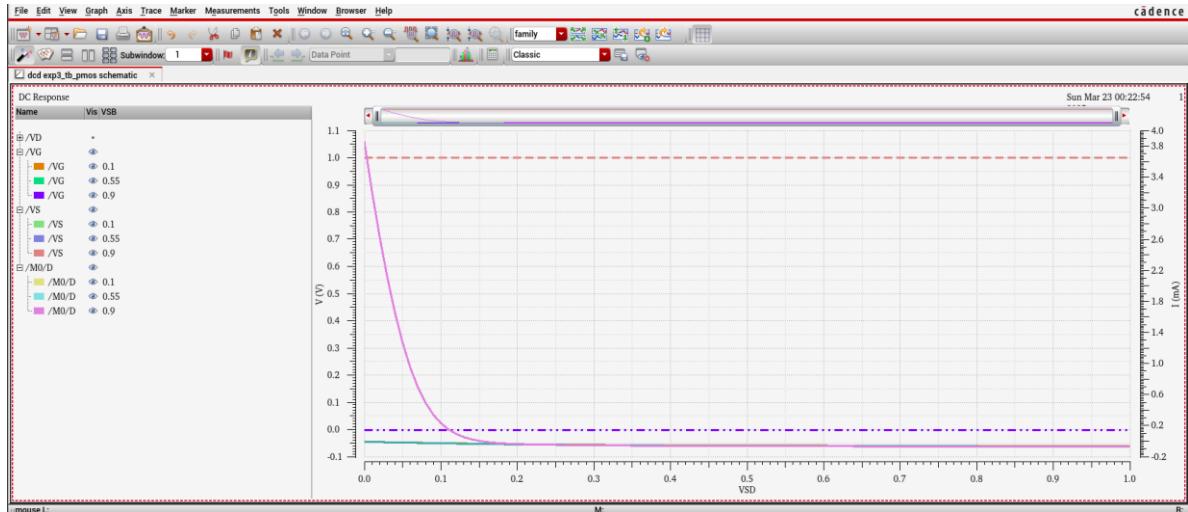


Figure 3.2.5: I_D vs V_{SD} @ $V_{SG} = 1V$, $V_{SB} = \{0.1, 0.55, 0.9\} V$ and sweeping $V_{SD} = [0,1] V$ step 10mV

⇒ V_{SB} affects the charge required to invert the channel: Increasing V_s or decreasing V_b increases V_t :

$$V_t = V_{t0} - \gamma(\sqrt{\phi_s + V_{bs}} - \sqrt{\phi_s})$$

=> Decreasing I_D : $I_D = \frac{\beta}{2} (V_{gs} - V_t)^2 (1 + \lambda |V_{ds}|)$ with increasing V_{SB} .

3.3 Measure, and analyze device characteristics: λ , V_{Th0} , k_p , and γ

Extract the four electrical parameters (k_p , V_{Th0} , λ and γ) for NMOS_VTG, and PMOS_VTG from tool:

- NMOS_VTG:

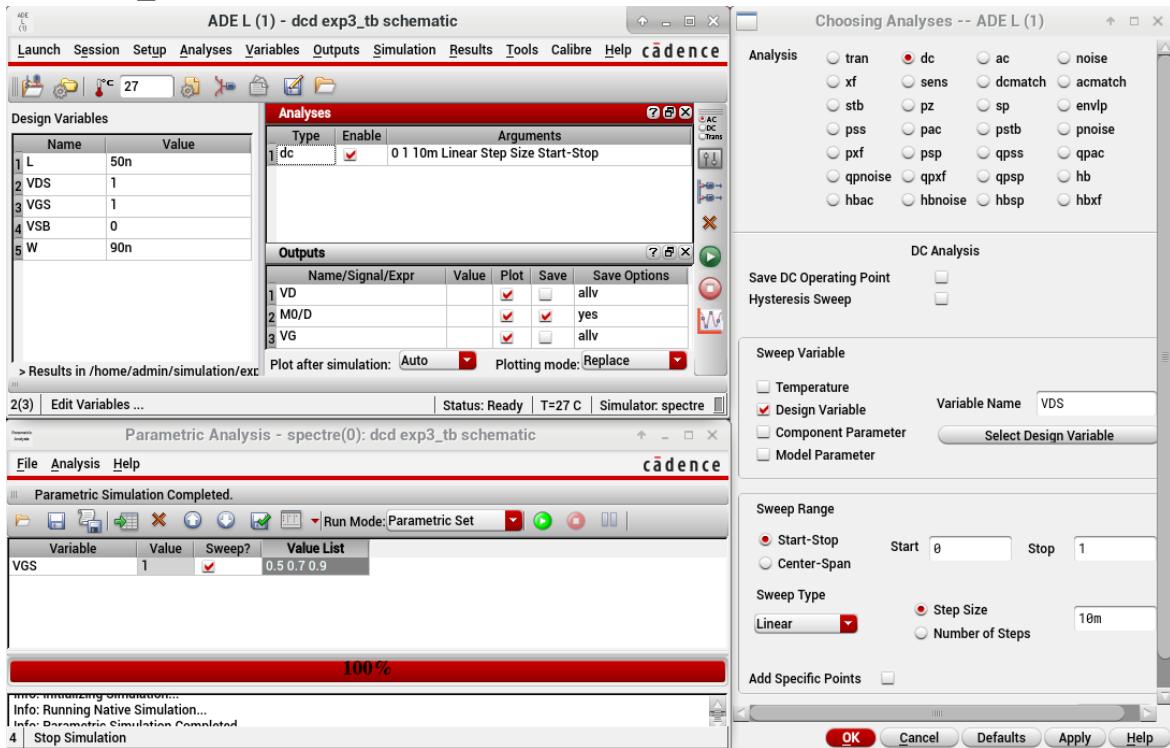


Figure 3.3.1: Setting for drawing I_D vs V_{DS} @ $V_{SB} = 0V$, $V_{GS} = \{0.5, 0.7, 0.9\}$ V and sweeping $V_{DS} = [0,1]$ V step 10mV

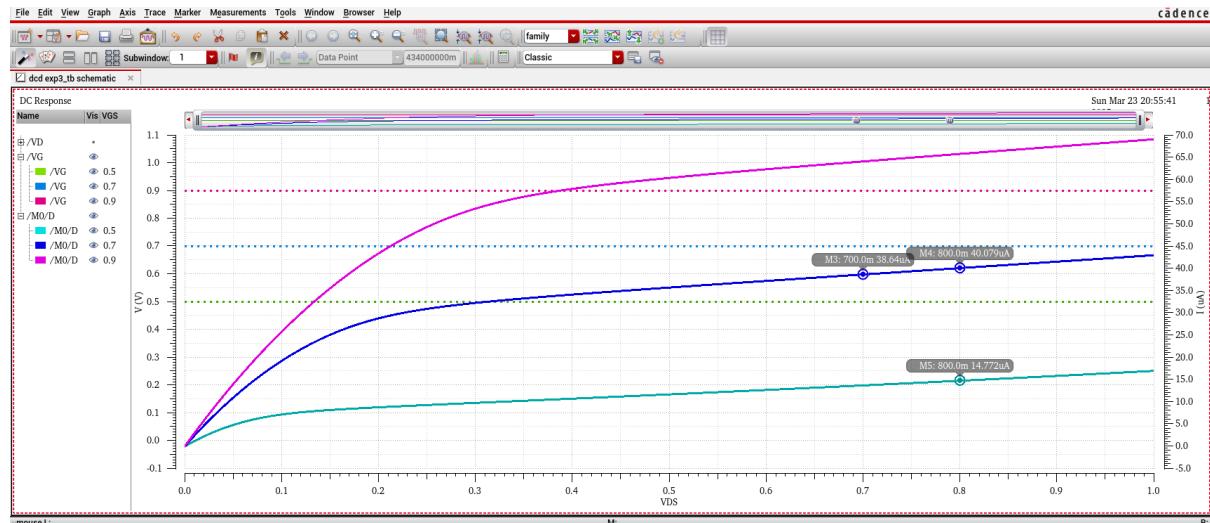


Figure 3.3.2: I_D vs V_{DS} @ $V_{SB} = 0V$, $V_{GS} = \{0.5, 0.7, 0.9\}$ V and sweeping $V_{DS} = [0,1]$ V step 10mV

- Using a curve I_D vs V_{DS} which each curve represents a different V_{GS} value. Any one of these curves can be used to calculate λ . Make sure that V_{bs} is 0V for this

simulation. The formula for calculating λ given two points on the saturation portion of a single curve is:

$$\begin{aligned}\lambda &= \frac{I_{D2} - I_{D1}}{I_{D1}V_{DS2} - I_{D2}V_{DS1}} \\ &= \frac{40.0793\mu A - 38.6402\mu A}{38.6402\mu A \times 0.8V - 40.0793\mu A \times 0.7V} \\ &\approx 0.5038\end{aligned}$$

- Using the saturation portion of the two curves with equal V_{ds} then V_{Th0} can be calculated as:

$$\begin{aligned}V_{Th0} &= \frac{V_{gs1} - V_{gs2} \sqrt{\frac{I_{ds1}}{I_{ds2}}}}{1 - \sqrt{\frac{I_{ds1}}{I_{ds2}}}} \\ &= \frac{0.7 - 0.5 \sqrt{\frac{40.0793\mu A}{14.7724\mu A}}}{1 - \sqrt{\frac{40.0793\mu A}{14.7724\mu A}}} \\ &\approx 0.1910 \text{ (V)}\end{aligned}$$

- Knowing λ and V_{Th0} , k_p can easily be found from the equation for a MOS transistor drain current in the saturation region. A little algebra shows that k_p is:

$$\begin{aligned}k_p &= \frac{2I_D}{\frac{W}{L}(V_{GS} - V_{Th0})^2(1 + \lambda V_{DS})} \\ &= \frac{2 \times 40.0793\mu A}{\frac{90}{50}(0.7 - 0.1910)^2(1 + 0.5038 \times 0.8)} \\ &\approx 122.5101\mu\end{aligned}$$

- To obtain γ you must first give the transistor a non-zero V_{SB} . Next, calculate the new V_{Th} using the same procedure that you used to obtain V_{Th0} where $2\phi_F = 0.7$. γ is given as:

$$\begin{aligned}\gamma &= \frac{V_{Th} - V_{Th0}}{\sqrt{|2\phi_F| + |V_{SB}|} - \sqrt{|2\phi_F|}} \\ &= \frac{0.4366 - 0.1910}{\sqrt{0.7 + 1.2} - \sqrt{0.7}} \\ &\approx 0.4533\end{aligned}$$

- Calculate the new V_{Th} :

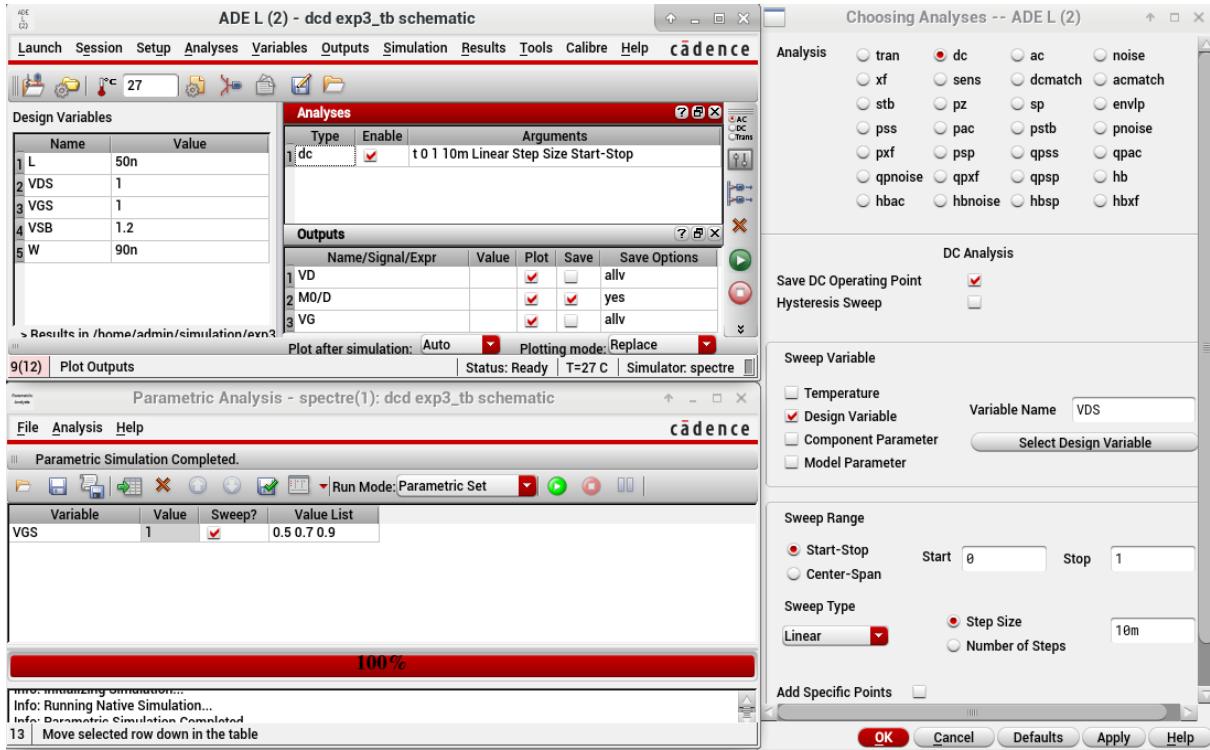


Figure 3.3.3: Setting for drawing I_D vs V_{DS} @ $V_{SB} = 1.2V$, $V_{GS} = \{0.5,0.7,0.9\} V$ and sweeping $V_{DS} = [0,1] V$ step 10mV

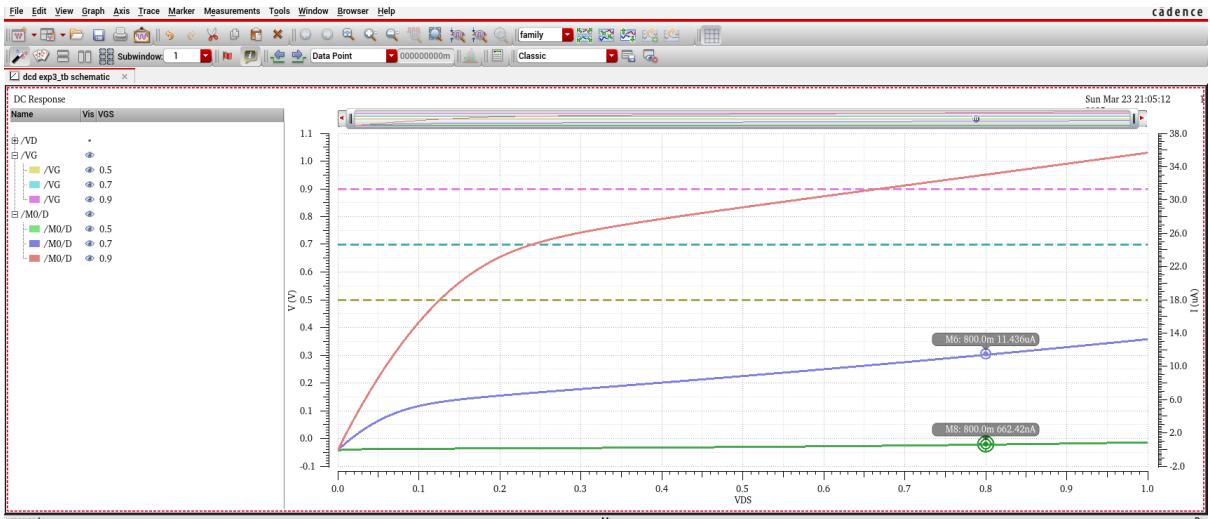


Figure 3.3.4: I_D vs V_{DS} @ $V_{SB} = 1.2V$, $V_{GS} = \{0.5,0.7,0.9\} V$ and sweeping $V_{DS} = [0,1] V$ step 10mV

- PMOS_VTG

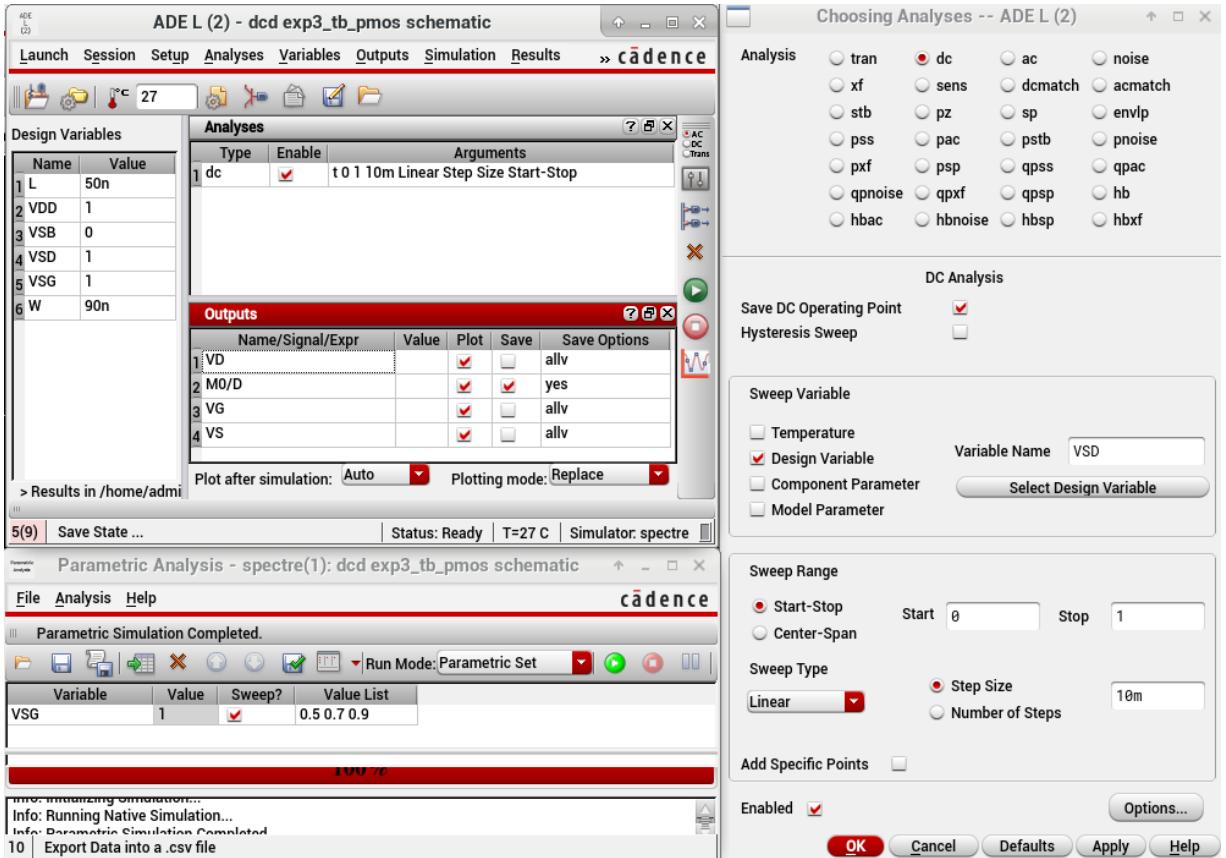


Figure 3.3.5: Setting for drawing I_D vs V_{SD} @ $V_{SB} = 0V$, $V_{SG} = \{0.5,0.7,0.9\} V$ and sweeping $V_{SD} = [0,1] V$ step 10mV



Figure 3.3.6: I_D vs V_{SD} @ $V_{SB} = 0V$, $V_{SG} = \{0.5,0.7,0.9\} V$ and sweeping $V_{SD} = [0,1] V$ step 10mV

- The calculation of parameters for PMOS_VTG is similar to the approach used for NMOS_VTG:

$$\begin{aligned}\lambda &= \frac{I_{D2} - I_{D1}}{I_{D1}V_{DS2} - I_{D2}V_{DS1}} \\ &= \frac{-26.75uA - -25.63uA}{-25.63uA \times 0.9V - -26.75uA \times 0.8V} \\ &\approx 0.6719\end{aligned}$$

$$\begin{aligned}V_{Th0} &= \frac{V_{gs1} - V_{gs2}\sqrt{\frac{I_{ds1}}{I_{ds2}}}}{1 - \sqrt{\frac{I_{ds1}}{I_{ds2}}}} \\ &= \frac{0.7 - 0.9\sqrt{\frac{-25.63uA}{-42.522A}}}{1 - \sqrt{\frac{-25.63uA}{-42.522uA}}} \\ &\approx 0.0057\end{aligned}$$

$$\begin{aligned}k_p &= \frac{2I_D}{\frac{W}{L}(V_{GS} - V_{Th0})^2(1 + \lambda V_{DS})} \\ &= \frac{2 \times (-25.63uA)}{\frac{90}{50}(0.7 - 0.0057)^2(1 + 0.6719 \times 0.8)} \\ &\approx -38.4230u\end{aligned}$$

$$\begin{aligned}\gamma &= \frac{V_{Th} - V_{Th0}}{\sqrt{|2\phi_F| + |V_{SB}|} - \sqrt{|2\phi_F|}} \\ &= \frac{-0.2062 - 0.0057}{\sqrt{0.7 + 0.7} - \sqrt{0.7}} \\ &= -0.6114\end{aligned}$$

- Calculate for the new V_{Th} :

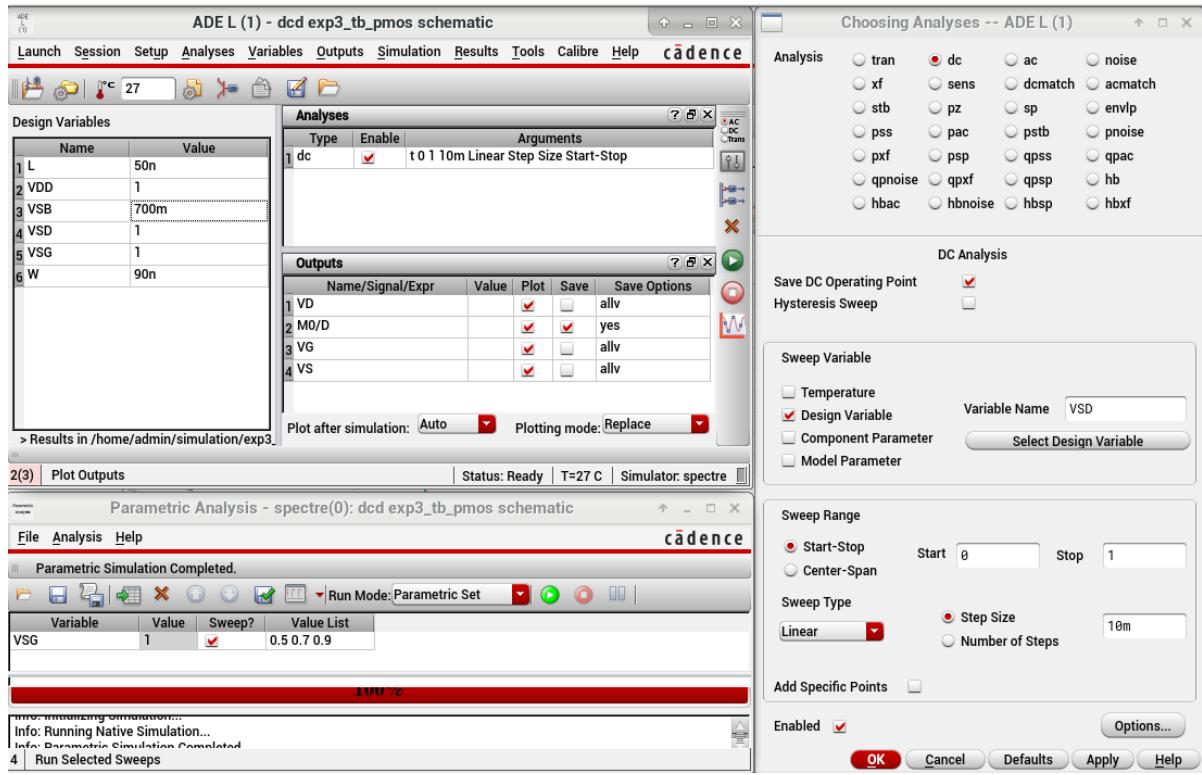


Figure 3.3.7: Setting for drawing I_D vs V_{SD} @ $V_{SB} = 0.7V$, $V_{SG} = \{0.5,0.7,0.9\} V$ and sweeping $V_{SD} = [0,1] V$ step 10mV

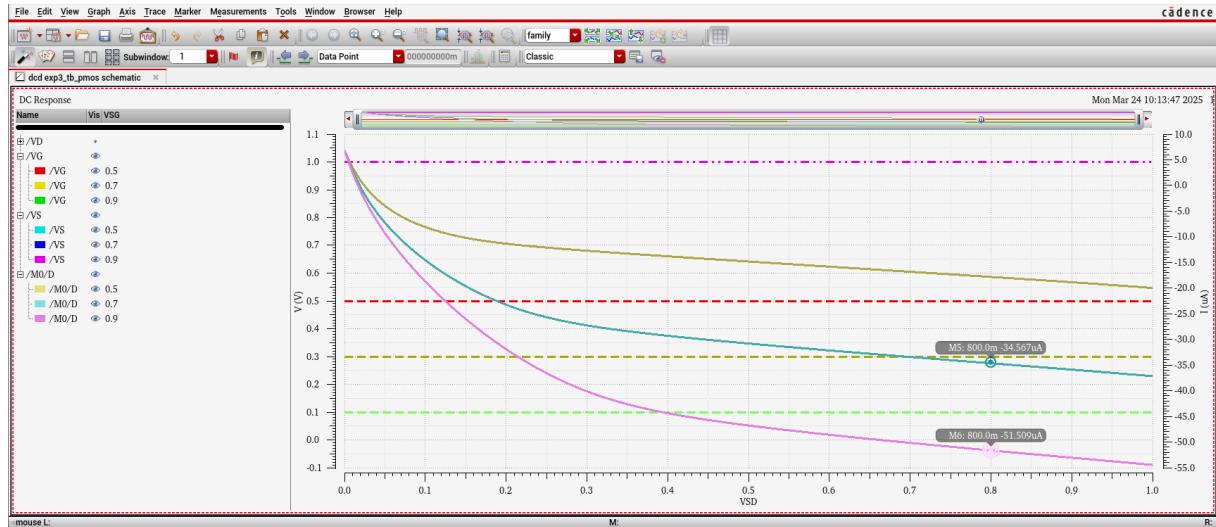


Figure 3.3.8: I_D vs V_{SD} @ $V_{SB} = 0.7V$, $V_{SG} = \{0.5,0.7,0.9\} V$ and sweeping $V_{SD} = [0,1] V$ step 10mV

EXPERIMENT 4: LAYOUT DESIGN FOR MOS TRANSISTOR

4.1 Requirements:

➤ Design the layout for a 120n/60n NMOS and a 50n/40n PMOS transistor.

➤ Verify the design by performing Design Rule Check (DRC) and ensuring Layout Versus Schematic (LVS) confirmation

4.2 Design Implementation:

To create the layout for NMOS and PMOS transistors, the first step is to determine the height of the active region, which corresponds to the transistor's width, and the width of the poly region, which corresponds to the transistor's length. Next, the respective terminals of the transistor are identified and connected through contacts. Finally, the design is verified using Design Rule Check (DRC) and Layout Versus Schematic (LVS).

For accurate and reliable design implementation, all required criteria must be met, and layout verification processes must be carried out to ensure the circuit meets design specifications.

4.2.1 Design NMOS's layout:

We will design the layout of the NMOS transistor according to the schematic below, including its terminals: **GATE**, **SOURCE**, **DRAIN**, and **BULK**. After completing the layout, **Design Rule Check (DRC)** and **Layout Versus Schematic (LVS)** will be used to verify the design accuracy and ensure compliance with fabrication constraints.

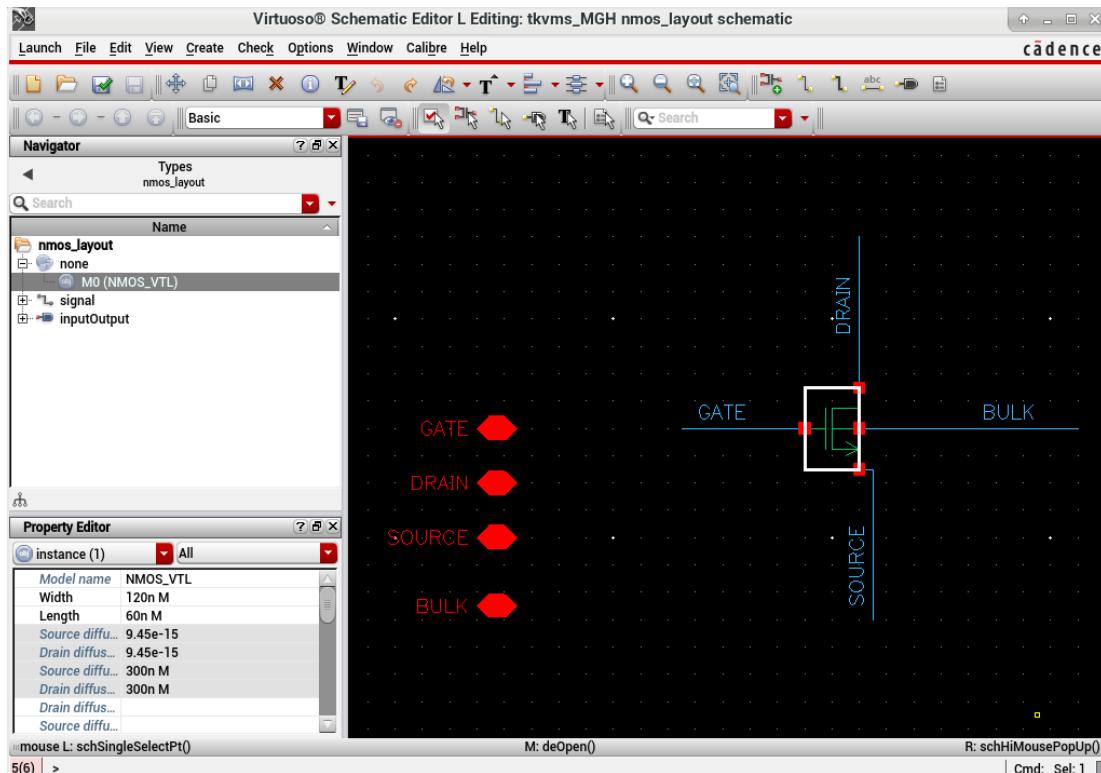


Figure 4.1: 120n/60n NMOS_VTL schematic

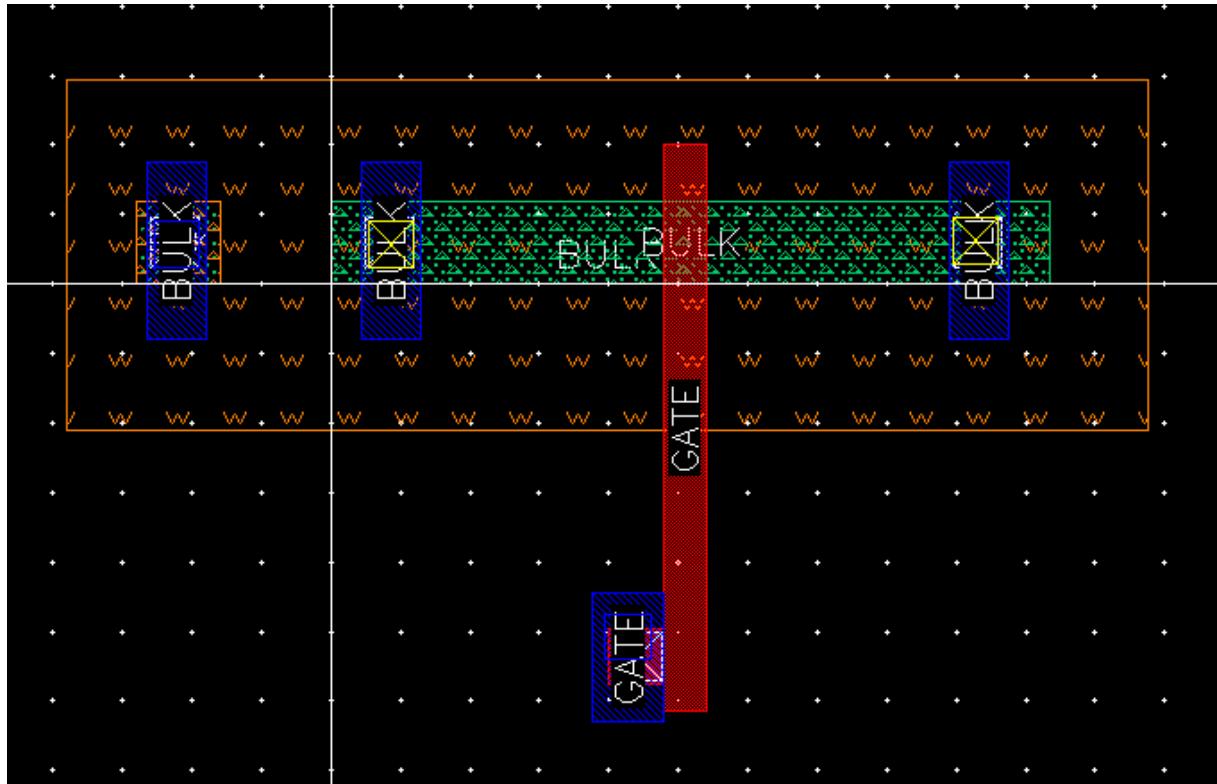


Figure 4.2: Layout of 120n/60n NMOS_VTL

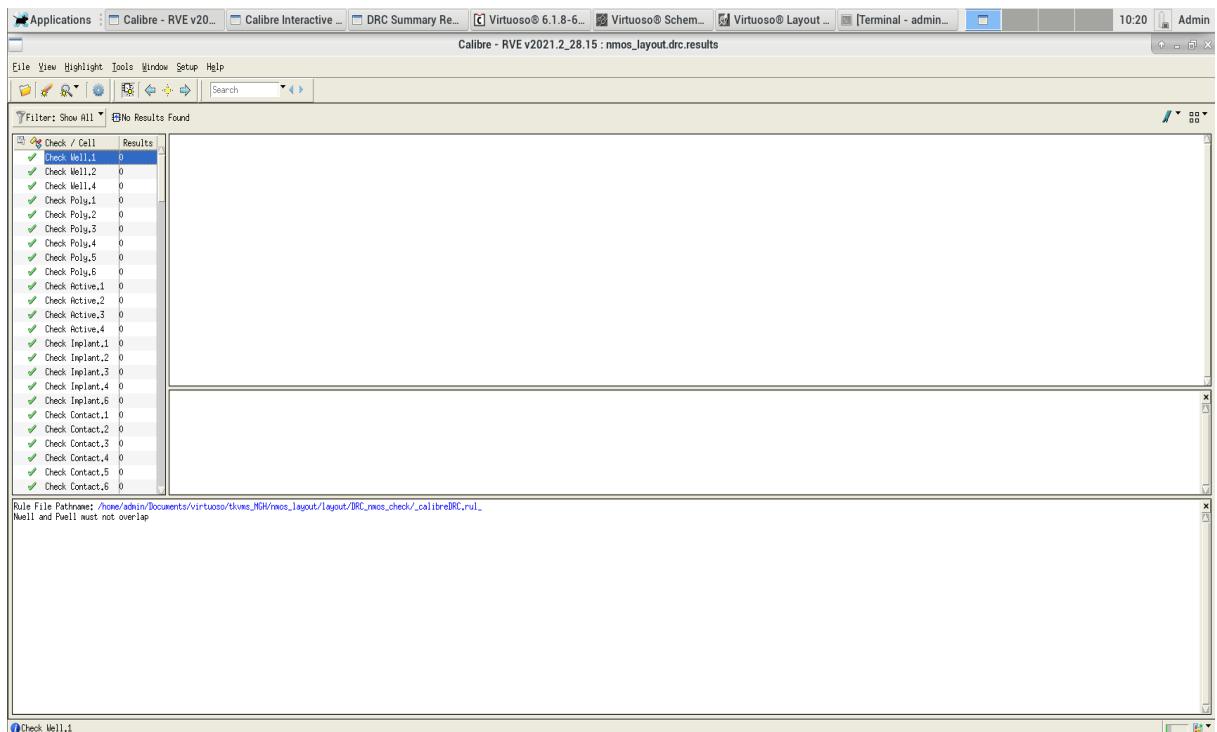


Figure 4.3: DRC Verification Results of NMOS_VTL

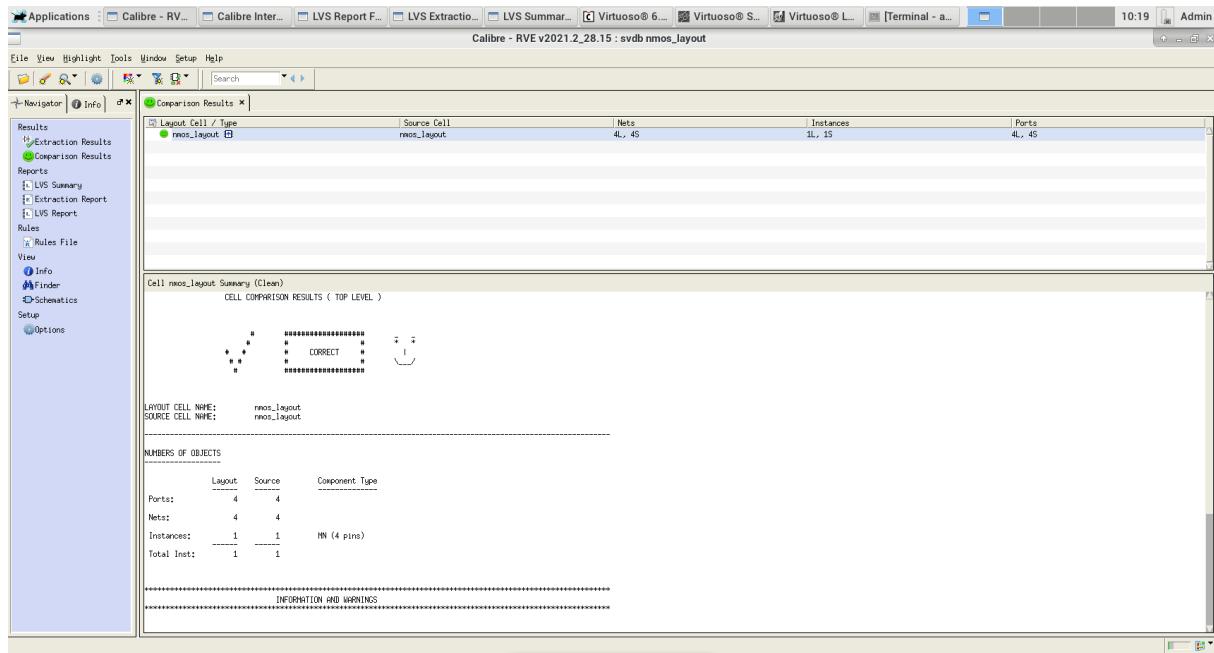


Figure 4.4: DRC Verification Results of NMOS_VTL

4.2.2 Design PMOS's layout:

Similarly to NMOS, we will design the layout of the **PMOS** transistor based on the schematic below, including its terminals: **GATE**, **SOURCE**, **DRAIN**, and **BULK**. After completing the layout, **Design Rule Check (DRC)** and **Layout Versus Schematic (LVS)** will be used to verify the design.

For PMOS, after performing the **DRC check**, it is necessary to adjust the **height of the active region** and the **width of the poly region** to match the **width and length of the PMOS transistor** accordingly.

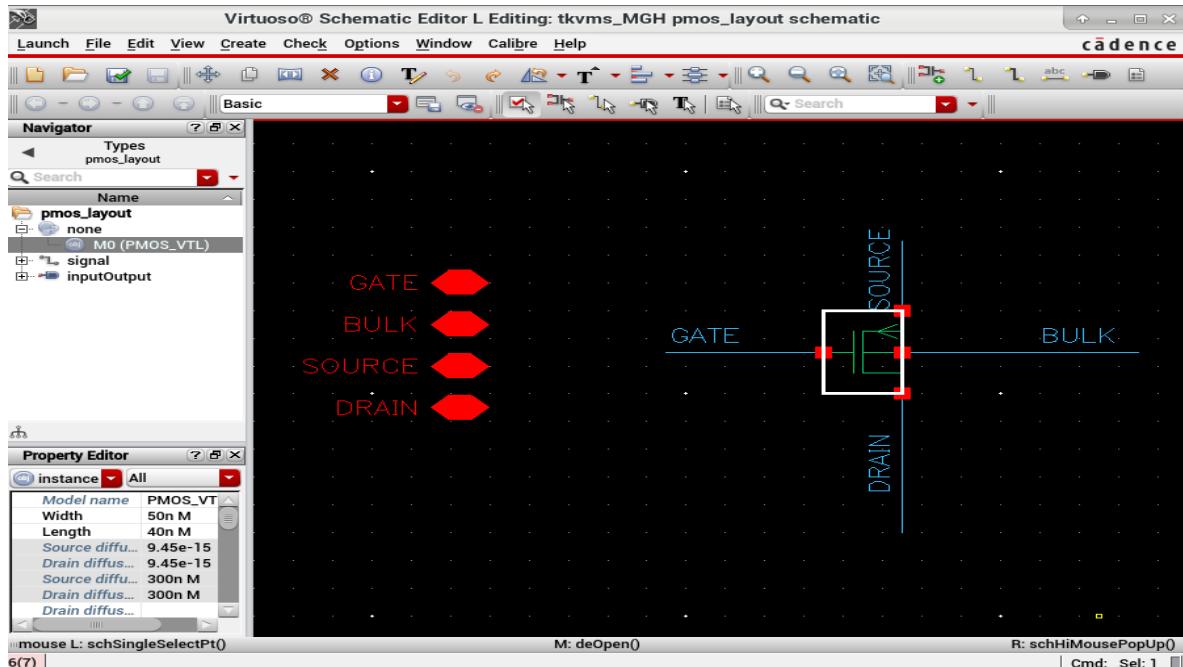


Figure 4.5: 50n/40n PMOS_VTL schematic

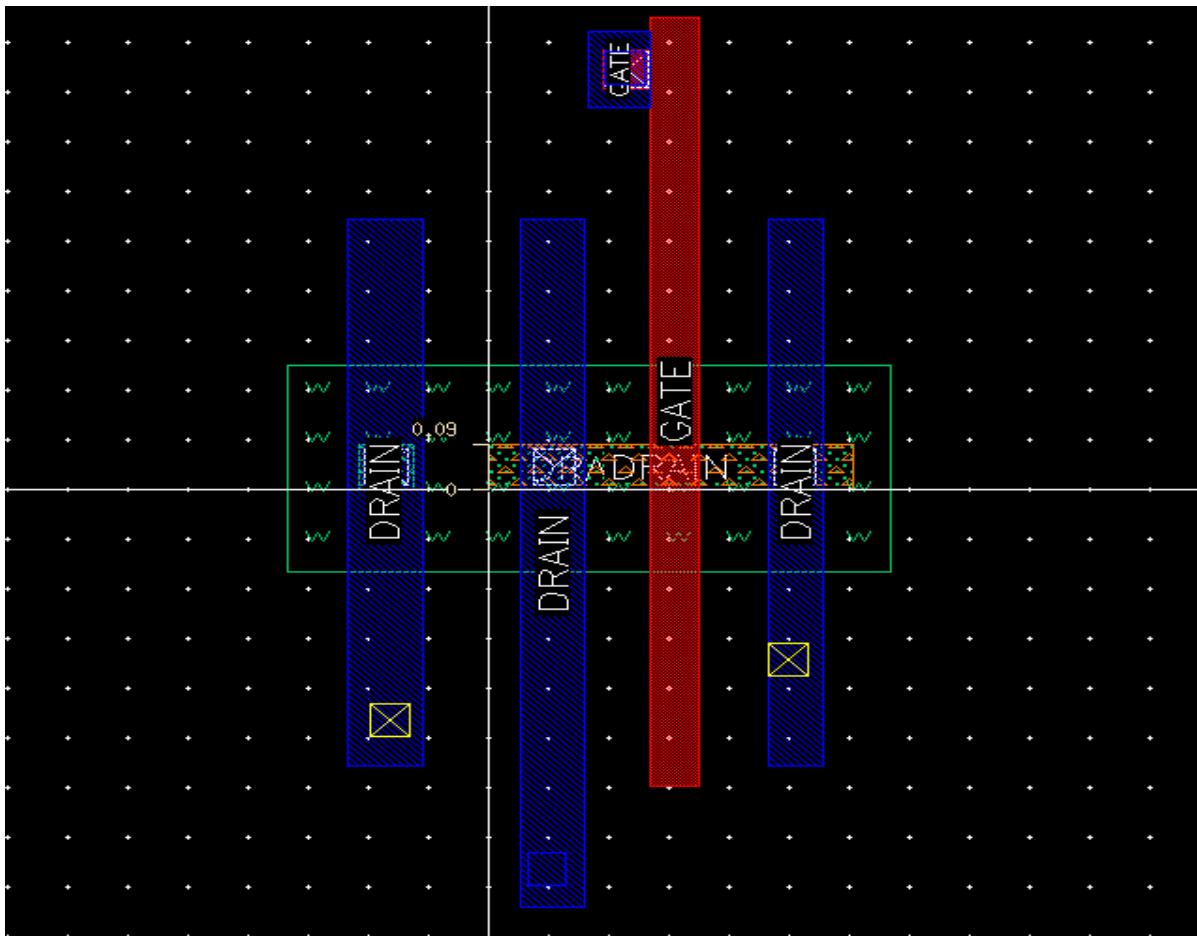


Figure 4.6: Layout of 50n/40n PMOS

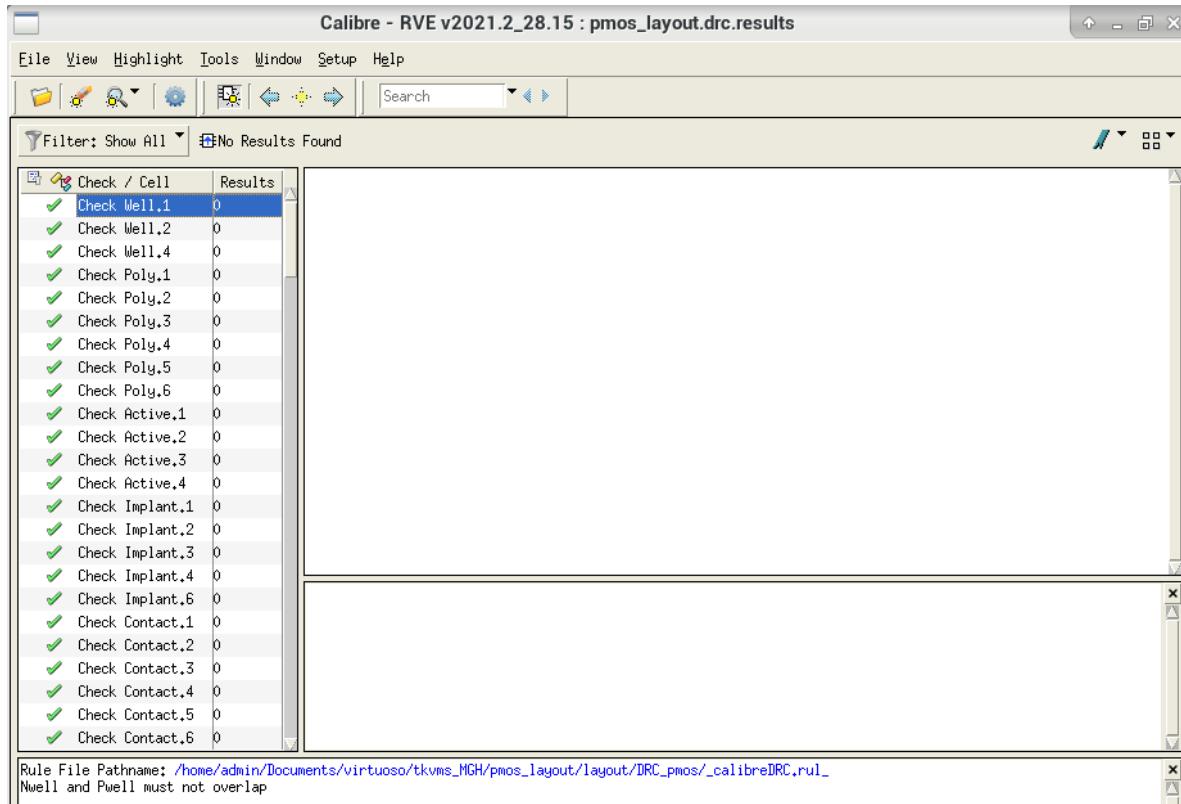


Figure 4.7: DRC Verification Results of PMOS

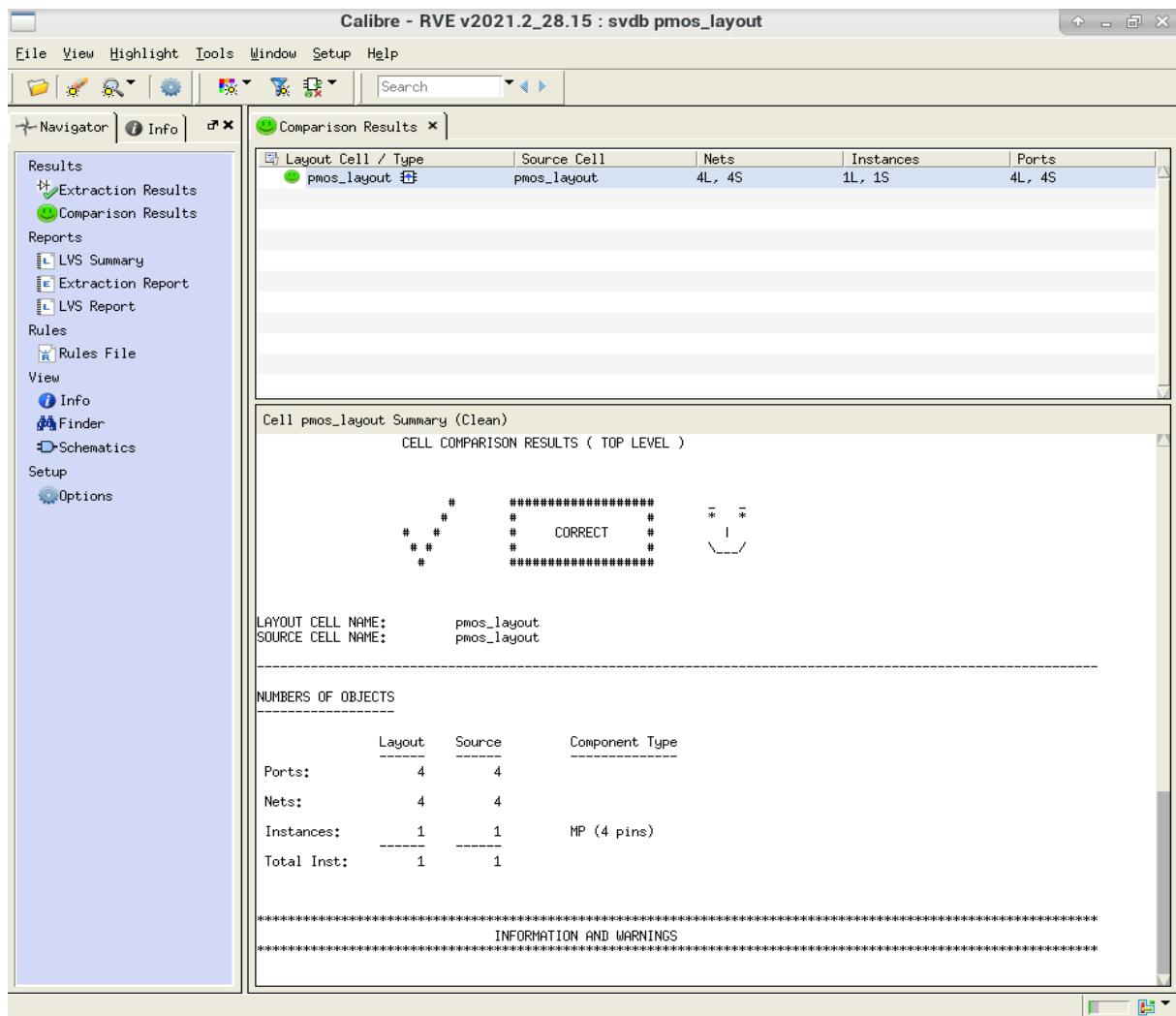


Figure 4.8: DRC Verification Results of PMOS