Vietnam National University Ho Chi Minh City
HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY

LAB 3: Design and synthesize ALU

Subject: Digital IC Design

Class L03 --- Semester 242

Group: 12

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Catalog

1. Mini project

Design and synthesize ALU specified in the previous RTL and verification lab(lab-3_1), use verification, plan in previous lab.
Get the maximum frequency (no violate on timing reports) and report.
Do not use (+, -, <<, >>, *, /, ...) operator in the design for arithmetic computation, each computational in the design must be structural, which mean arithmetic operator should not be used in the design (this will help the compute LUU module meet higher frequency).
Report resources usage (gates, area report can be found in 04_reports).
Post-synthesis netlist must meet all criteria in the verification plan.

1.1 Block diagrams of the design

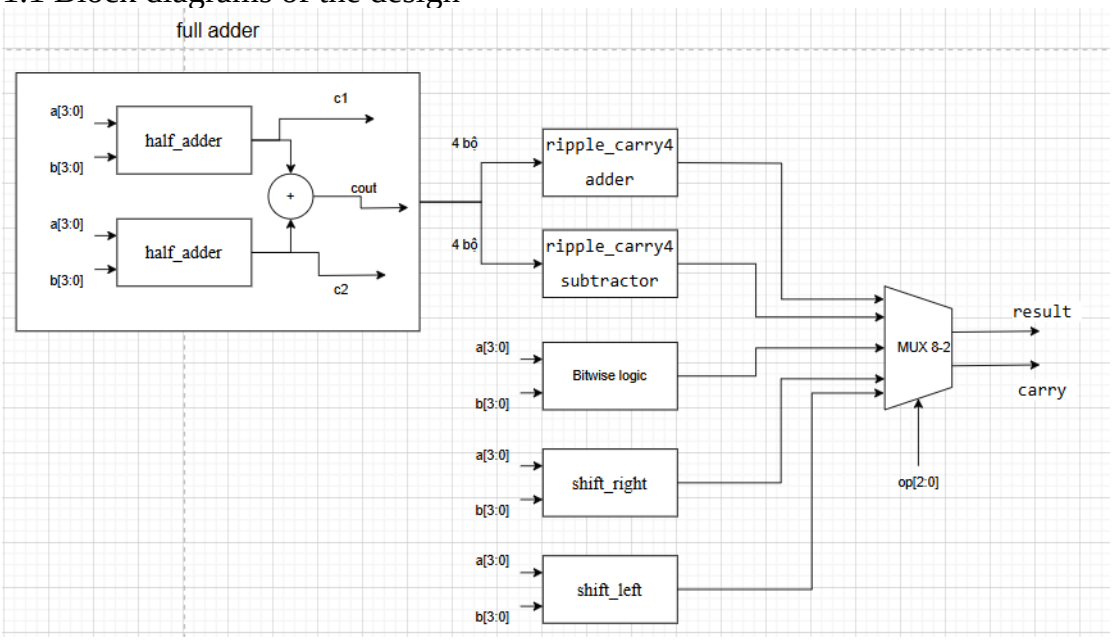


Figure 1.1.1 Block diagrams ALU

1.2 ALU Function Table and Port Description

Signal	Width	Direction Description
clk	1	input Clock signal
rst_n	1	input Asynchronous reset, active low
a	4	input First operand
b	4	input Second operand
op	3	input Operation selection
result	4	output Result of operation
carry	1	output Carry flag (for addition/subtraction only)

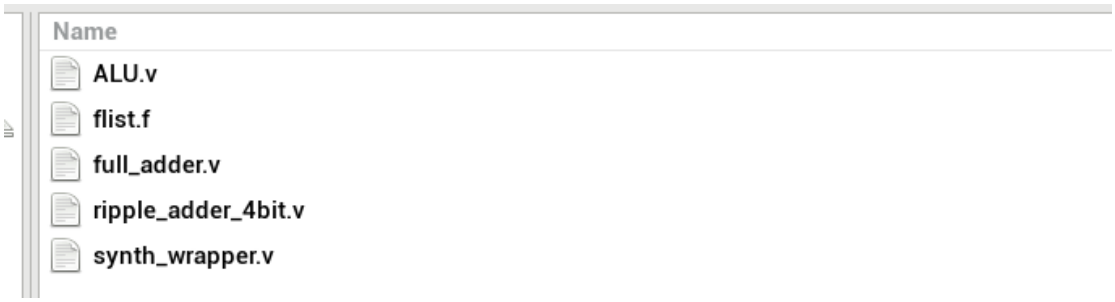
Table 1.2.1 Port Description

op (3 bit)	Operation	Description
000	Add	{carry, result} = a + b
001	Subtract	{carry, result} = a - b
010	AND	result = a & b; carry = 0
011	OR	result = a
100	XOR	result = a ^ b; carry = 0
101	NOT	result = ~a; carry = 0
110	Logical right	shift result = a >> b; carry = 0
111	Logical left	shift result = a << b; carry = 0

Table 1.2.2 Function Description

2. Report Mini project

2.1 Code module




```
module ALU( input clk, input rst_n, input [3:0] a, input [3:0] b, input [2:0] op, output reg [3:0] result, output reg carry );

// Internal signals
wire [3:0] adder_result;
wire [3:0] subtractor_result;
wire adder_carry;
wire subtractor_borrow;
wire [3:0] and_result;
wire [3:0] or_result;
wire [3:0] xor_result;
wire [3:0] not_result;
wire [3:0] shift_left_result;
wire [3:0] shift_right_result;

// Instantiate 4-bit adder
```

```
ripple_carry4 adder (
  .a(a),
  .b(b),
  .cin(1'b0),
  .s(adder_result),
  .cout(adder_carry)
);

// Instantiate 4-bit subtractor
ripple_carry4 subtractor (
  .a(a),
  .b(~b),
  .cin(1'b1),
  .s(subtractor_result),
  .cout(subtractor_borrow)
);

// Bitwise operations
assign and_result = a & b;
assign or_result = a | b;
assign xor_result = a ^ b;
assign not_result = ~a;

// Shift operations
shift_left sl (
  .a(a),
  .shift_amount(b[1:0]),  // Only use 2 LSBs for 4-bit shifts
  .result(shift_left_result)
);

shift_right sr (
  .a(a),
  .shift_amount(b[1:0]),  // Only use 2 LSBs for 4-bit shifts
  .result(shift_right_result)
);

always @(posedge clk or negedge rst_n) begin
  if (!rst_n) begin
     result <= 4'b0;
     carry <= 1'b0;
  end
  else begin
     case (op)
        3'b000: begin // Addition
           result <= adder_result;
           carry <= adder_carry;
```

```
        end
        3'b001: begin // Subtraction
            result <= subtractor_result;
            carry <= subtractor_borrow;
        end
        3'b010: begin // AND
            result <= and_result;
            carry <= 1'b0;
        end
        3'b011: begin // OR
            result <= or_result;
            carry <= 1'b0;
        end
        3'b100: begin // XOR
            result <= xor_result;
            carry <= 1'b0;
        end
        3'b101: begin // NOT
            result <= not_result;
            carry <= 1'b0;
        end
        3'b110: begin // Shift left
            result <= shift_left_result;
            carry <= 1'b0;
        end
        3'b111: begin // Shift right
            result <= shift_right_result;
            carry <= 1'b0;
        end
        default: begin
            result <= 4'b0;
            carry <= 1'b0;
        end
      endcase
  end
end


endmodule
```

// 4-bit ripple carry adder (from your original code) module ripple_carry4(input [3:0] a, b, input cin, output [3:0] s, output cout); wire c1, c2, c3; full_adder fa0 (.a(a[0]), .b(b[0]), .cin(cin), .s(s[0]), .cout(c1)); full_adder fa1 (.a(a[1]), .b(b[1]), .cin(c1), .s(s[1]), .cout(c2)); full_adder fa2 (.a(a[2]), .b(b[2]), .cin(c2), .s(s[2]), .cout(c3)); full_adder fa3 (.a(a[3]), .b(b[3]), .cin(c3), .s(s[3]), .cout(cout)); endmodule

// Full adder (from your original code) module full_adder(input a, b, cin, output s, cout); wire sum1, c1, c2; half_adder ha1 (.a(a), .b(b), .s(sum1), .c(c1)); half_adder ha2 (.a(sum1), .b(cin), .s(s), .c(c2)); or (cout, c1, c2); endmodule

// Half adder (from your original code) module half_adder(input a, b, output c, s); xor (s, a, b); and (c, a, b); endmodule

// Left shifter module module shift_left(input [3:0] a, input [1:0] shift_amount, output reg [3:0] result); always @(*) begin case (shift_amount) 2'b00: result = a; 2'b01: result = {a[2:0], 1'b0}; 2'b10: result = {a[1:0], 2'b0}; 2'b11: result = {a[0], 3'b0}; endcase end endmodule

// Right shifter module module shift_right(input [3:0] a, input [1:0] shift_amount, output reg [3:0] result); always @(*) begin case (shift_amount) 2'b00: result = a; 2'b01: result = {1'b0, a[3:1]}; 2'b10: result = {2'b0, a[3:2]}; 2'b11: result = {3'b0, a[3]}; endcase end endmodule

2.2 Simulation

2.2.1 Simulation testbench waveform window

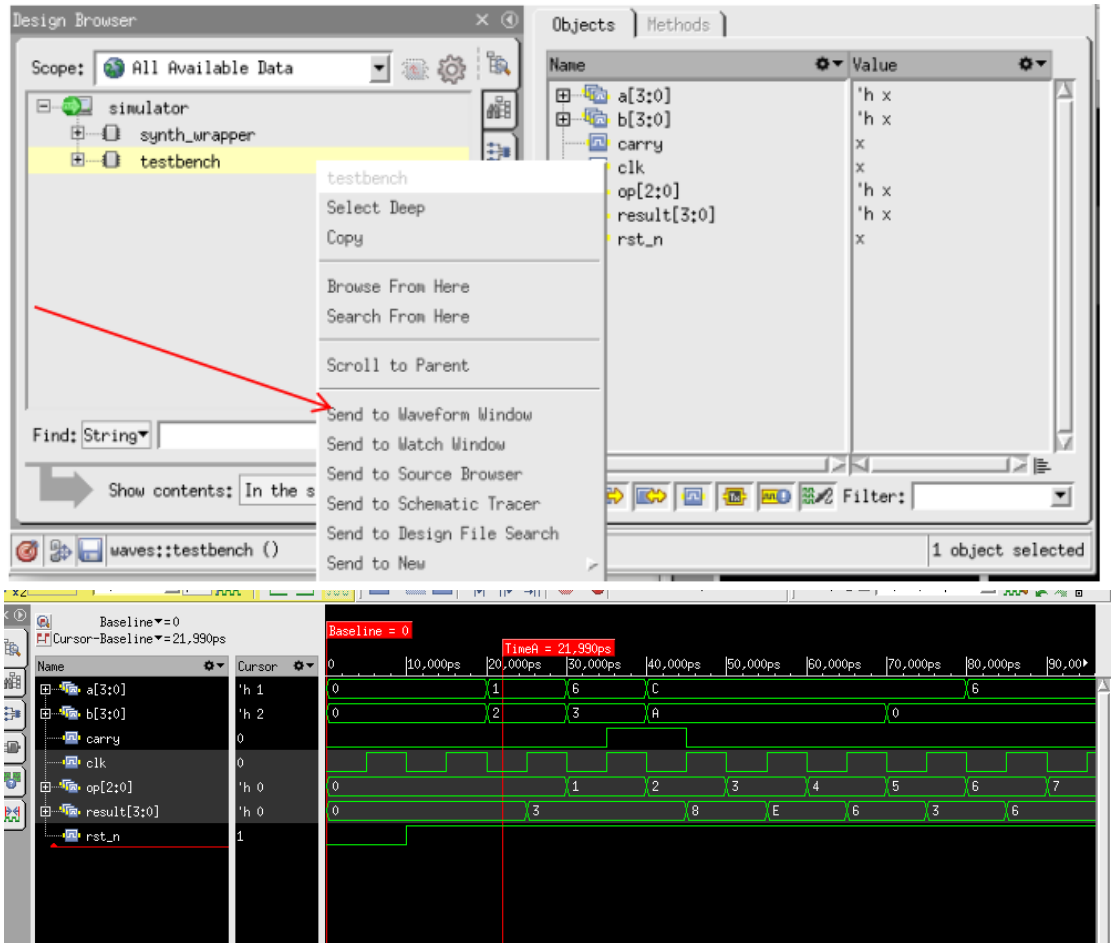


Figure 2.2.1.1 Waveform viewer Window

2.2.2 Simulation testbench schematic Tracer

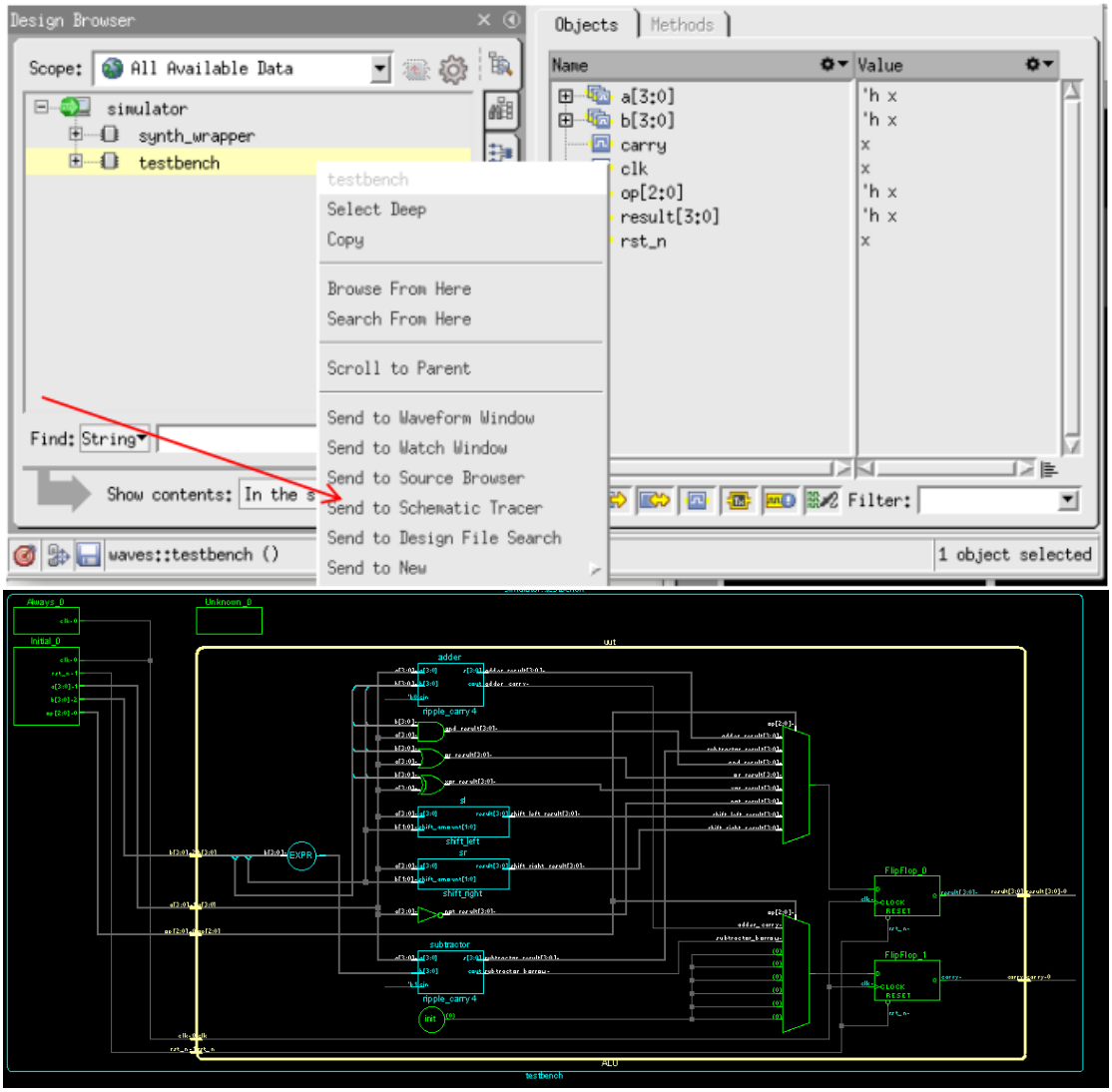


Figure 2.2.2.1 RTL viewer schematic

2.2.3 Simulation schematic of netlist

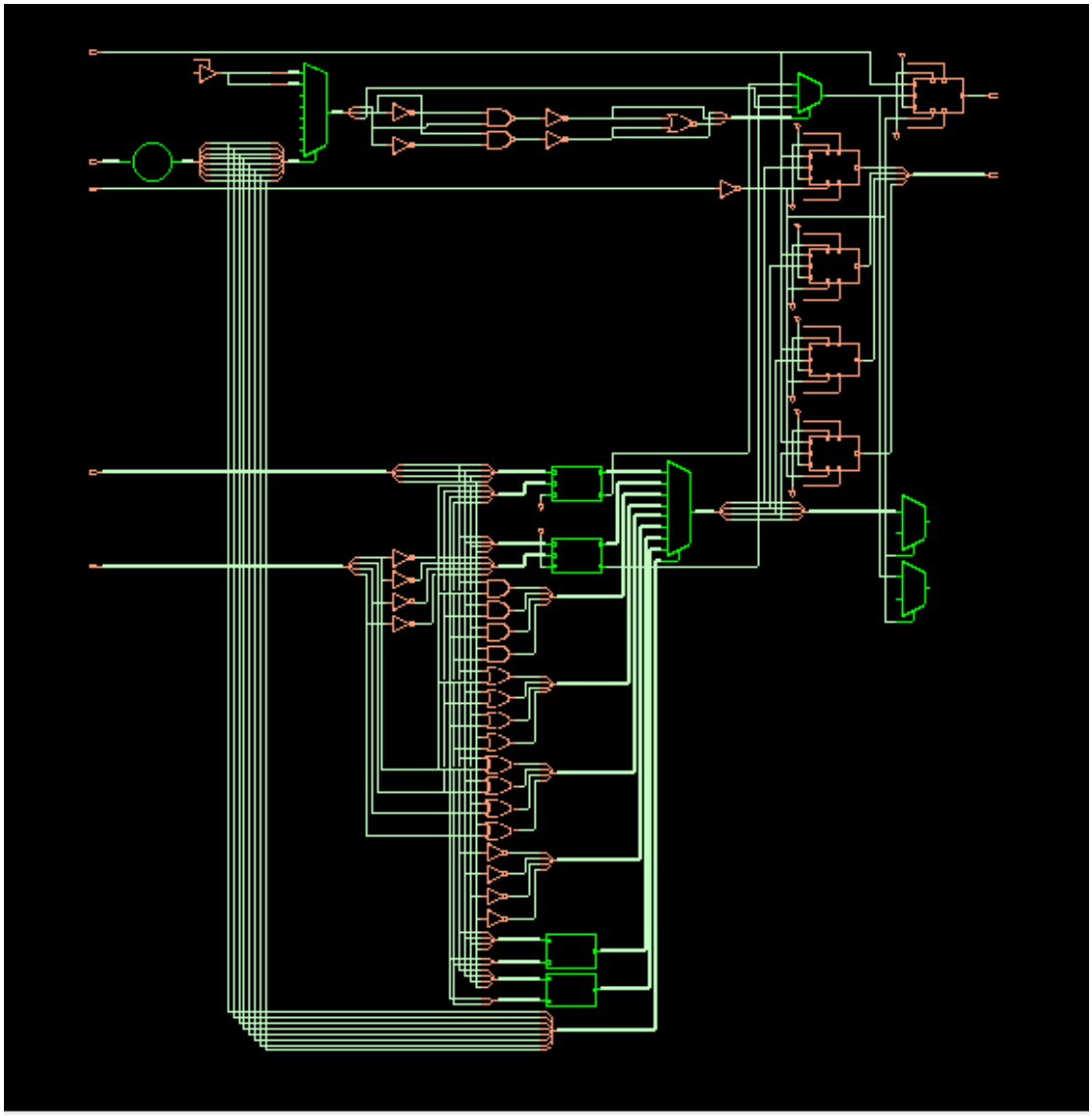


Figure 2.2.3.1 Schematic of netlist

2.2.4 Timing

Capture the reports of:

Highest frequency the design can be synthesized.

Timing report of the design like below (show that 10 paths printed from the command make report have no VIOLATE indication).

```
set FREQ_GHz 1.04
Path 1: VIOLATED (-19 ps) Setup Check with Pin S_reg[2]/CLK->D
Path 2: VIOLATED (-17 ps) Setup Check with Pin S_reg[3]/CLK->D
Path 3: VIOLATED (-10 ps) Setup Check with Pin Co_reg/CLK->D
Path 4: MET (27 ps) Setup Check with Pin S_reg[0]/CLK->D
Path 5: MET (60 ps) Setup Check with Pin S_reg[1]/CLK->D
Path 6: MET (146 ps) Late External Delay Assertion at pin Co
Path 7: MET (146 ps) Late External Delay Assertion at pin S[0]
Path 8: MET (146 ps) Late External Delay Assertion at pin S[1]
Path 9: MET (146 ps) Late External Delay Assertion at pin S[2]
Path 10: MET (146 ps) Late External Delay Assertion at pin S[3]
[admin@centos7 synthesis]$
```

Figure 2.2.4.1 The frequency at 1.04

```
set FREQ_GHz 1.03
Path 1: MET (0 ps) Setup Check with Pin S_reg[2]/CLK->D
Path 2: MET (4 ps) Setup Check with Pin S_reg[3]/CLK->D
Path 3: MET (4 ps) Setup Check with Pin Co_reg/CLK->D
Path 4: MET (37 ps) Setup Check with Pin S_reg[0]/CLK->D
Path 5: MET (69 ps) Setup Check with Pin S_reg[1]/CLK->D
Path 6: MET (151 ps) Late External Delay Assertion at pin Co
Path 7: MET (151 ps) Late External Delay Assertion at pin S[0]
Path 8: MET (151 ps) Late External Delay Assertion at pin S[1]
Path 9: MET (151 ps) Late External Delay Assertion at pin S[2]
Path 10: MET (151 ps) Late External Delay Assertion at pin S[3]
[admin@centos7 synthesis]$
```

Figure 2.2.4.1 The frequency at 1.03

The highest frequency at which a design can be synthesized is 1.03Ghz

Timing report of the design like below:

```
Path 1: MET (0 ps) Setup Check with Pin S_reg[2]/CLK->D
     Startpoint: (R) Cin_reg_reg/CLK
          Clock: (R) clk
       Endpoint: (F) S_reg[2]/D
          Clock: (R) clk

                    Capture       Launch
       Clock Edge:+     971            0
       Src Latency:+      0            0
       Net Latency:+      0 (I)        0 (I)
           Arrival:=    971            0

             Setup:-    120
       Uncertainty:-     10
     Required Time:=    840
      Launch Clock:-      0
         Data Path:-    840
             Slack:=      0

#-------------------------------------------------------------------------------------------------------
#  Timing Point   Flags    Arc   Edge           Cell             Fanout Load Trans Delay Arrival
#                                                                  (fF)  (ps)  (ps)   (ps)
#-------------------------------------------------------------------------------------------------------
  Cin_reg_reg/CLK -       -      R     (arrival)                    14    -     0     -       0
  Cin_reg_reg/Q   -       CLK->Q F     sky130_fd_sc_hd__dfrtp_1      3 11.1    77   380     380
  g16/Y           -       A->Y   R     sky130_fd_sc_hd__clkinv_2     1 10.6    50    71     451
  g15/Y           -       B->Y   F     sky130_fd_sc_hd__nand2_4      1  9.6    34    51     502
  g14/Y           -       A->Y   R     sky130_fd_sc_hd__nand2_4      1 10.1    56    55     556
  g419/Y          -       A->Y   F     sky130_fd_sc_hd__nand2_4      3 19.3    57    63     620
  g418/Y          -       A->Y   R     sky130_fd_sc_hd__nand2_2      2  8.8    66    74     694
  g79/Y           -       A->Y   F     sky130_fd_sc_hd__nand2_2      1  3.6    31    45     738
  g2456/Y         -       A->Y   R     sky130_fd_sc_hd__nand2_1      1  3.7    52    54     792
  g74/Y           -       A->Y   F     sky130_fd_sc_hd__nand2_1      1  3.2    36    49     840
  S_reg[2]/D      -       -      F     sky130_fd_sc_hd__dfrtp_1      1    -     -     0     840
#-------------------------------------------------------------------------------------------------------
```

```
Path 2: MET (4 ps) Setup Check with Pin S_reg[3]/CLK->D
     Startpoint: (R) Cin_reg_reg/CLK
          Clock: (R) clk
       Endpoint: (F) S_reg[3]/D
          Clock: (R) clk

                    Capture       Launch
       Clock Edge:+     971            0
       Src Latency:+      0            0
       Net Latency:+      0 (I)        0 (I)
           Arrival:=    971            0

             Setup:-    121
       Uncertainty:-     10
     Required Time:=    840
      Launch Clock:-      0
         Data Path:-    837
             Slack:=      4

#-------------------------------------------------------------------------------------------------------
#  Timing Point   Flags    Arc   Edge           Cell             Fanout Load Trans Delay Arrival
#                                                                  (fF)  (ps)  (ps)   (ps)
#-------------------------------------------------------------------------------------------------------
  Cin_reg_reg/CLK -       -      R     (arrival)                    14    -     0     -       0
  Cin_reg_reg/Q   -       CLK->Q F     sky130_fd_sc_hd__dfrtp_1      3 11.1    77   380     380
  g16/Y           -       A->Y   R     sky130_fd_sc_hd__clkinv_2     1 10.6    50    71     451
  g15/Y           -       B->Y   F     sky130_fd_sc_hd__nand2_4      1  9.6    34    51     502
  g14/Y           -       A->Y   R     sky130_fd_sc_hd__nand2_4      1 10.1    56    55     556
  g419/Y          -       A->Y   F     sky130_fd_sc_hd__nand2_4      3 19.3    57    63     620
  g395/Y          -       A->Y   R     sky130_fd_sc_hd__nand2_4      2  8.9    49    62     682
  g392/Y          -       A->Y   F     sky130_fd_sc_hd__nand2_2      2  6.5    38    49     731
  g390/Y          -       A->Y   R     sky130_fd_sc_hd__nand2_1      1  3.7    54    56     788
  g388/Y          -       A->Y   F     sky130_fd_sc_hd__nand2_1      1  3.2    36    49     837
  S_reg[3]/D      -       -      F     sky130_fd_sc_hd__dfrtp_1      1    -     -     0     837
#-------------------------------------------------------------------------------------------------------
```

```
Path 3: MET (4 ps) Setup Check with Pin Co_reg/CLK->D
     Startpoint: (R) Cin_reg_reg/CLK
          Clock: (R) clk
       Endpoint: (F) Co_reg/D
          Clock: (R) clk

                     Capture       Launch
        Clock Edge:+     971            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=     971            0

              Setup:-     120
       Uncertainty:-      10
     Required Time:=     841
      Launch Clock:-       0
         Data Path:-     836
             Slack:=       4

#-------------------------------------------------------------------------------------------------
#  Timing Point   Flags    Arc   Edge           Cell             Fanout Load Trans Delay Arrival
#                                                                  (fF)  (ps)  (ps)   (ps)
#-------------------------------------------------------------------------------------------------
  Cin_reg_reg/CLK -       -      R     (arrival)                    14    -     0     -       0
  Cin_reg_reg/Q   -       CLK->Q F     sky130_fd_sc_hd__dfrtp_1      3 11.1    77   380     380
  g16/Y           -       A->Y   R     sky130_fd_sc_hd__clkinv_2     1 10.6    50    71     451
  g15/Y           -       B->Y   F     sky130_fd_sc_hd__nand2_4      1  9.6    34    51     502
  g14/Y           -       A->Y   R     sky130_fd_sc_hd__nand2_4      1 10.1    56    55     556
  g419/Y          -       A->Y   F     sky130_fd_sc_hd__nand2_4      3 19.3    57    63     620
  g395/Y          -       A->Y   R     sky130_fd_sc_hd__nand2_4      2  8.9    49    62     682
  g392/Y          -       A->Y   F     sky130_fd_sc_hd__nand2_2      2  6.5    38    49     731
  g389/Y          -       A->Y   R     sky130_fd_sc_hd__nand2_1      1  3.7    53    56     788
  g31/Y           -       A->Y   F     sky130_fd_sc_hd__nand2_1      1  3.2    35    49     836
  Co_reg/D        -       -      F     sky130_fd_sc_hd__dfrtp_1      1    -     -     0     836
#-------------------------------------------------------------------------------------------------
```

```
Path 4: MET (37 ps) Setup Check with Pin S_reg[0]/CLK->D
     Startpoint: (R) X_reg_reg[0]/CLK
          Clock: (R) clk
       Endpoint: (F) S_reg[0]/D
          Clock: (R) clk

                     Capture       Launch
        Clock Edge:+     971            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=     971            0

              Setup:-     133
       Uncertainty:-      10
     Required Time:=     828
      Launch Clock:-       0
         Data Path:-     791
             Slack:=      37

#-------------------------------------------------------------------------------------------------
#  Timing Point    Flags    Arc   Edge           Cell             Fanout Load Trans Delay Arrival
#                                                                   (fF)  (ps)  (ps)   (ps)
#-------------------------------------------------------------------------------------------------
  X_reg_reg[0]/CLK -       -      R     (arrival)                   14    -     0     -       0
  X_reg_reg[0]/Q   -       CLK->Q F     sky130_fd_sc_hd__dfrtp_1     3 11.6    79   382     382
  g2426/X          -       A->X   F     sky130_fd_sc_hd__buf_1       1  5.5    42   116     498
  g2405/X          -       B->X   F     sky130_fd_sc_hd__xor2_1      1  5.5    68   148     645
  g2400/X          -       B->X   F     sky130_fd_sc_hd__xor2_1      1  3.2    64   146     791
  S_reg[0]/D       -       -      F     sky130_fd_sc_hd__dfrtp_1     1    -     -     0     791
#-------------------------------------------------------------------------------------------------
```

```
Path 5: MET (69 ps) Setup Check with Pin S_reg[1]/CLK->D
     Startpoint: (R) Cin_reg_reg/CLK
          Clock: (R) clk
       Endpoint: (F) S_reg[1]/D
          Clock: (R) clk

                     Capture       Launch
        Clock Edge:+     971            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=     971            0

              Setup:-     130
       Uncertainty:-      10
     Required Time:=     831
      Launch Clock:-       0
         Data Path:-     762
             Slack:=      69

#-------------------------------------------------------------------------------------------------
#  Timing Point   Flags    Arc   Edge           Cell              Fanout Load Trans Delay Arrival
#                                                                  (fF)  (ps)  (ps)   (ps)
#-------------------------------------------------------------------------------------------------
  Cin_reg_reg/CLK -       -      R     (arrival)                    14    -     0     -       0
  Cin_reg_reg/Q   -       CLK->Q F     sky130_fd_sc_hd__dfrtp_1      3 11.1    77   380     380
  g16/Y           -       A->Y   R     sky130_fd_sc_hd__clkinv_2     1 10.6    50    71     451
  g15/Y           -       B->Y   F     sky130_fd_sc_hd__nand2_4      1  9.6    34    51     502
  g14/Y           -       A->Y   R     sky130_fd_sc_hd__nand2_4      1 10.1    56    55     556
  g419/Y          -       A->Y   F     sky130_fd_sc_hd__nand2_4      3 19.3    57    63     620
  g57/X           -       B->X   F     sky130_fd_sc_hd__xor2_1       1  3.2    58   142     762
  S_reg[1]/D      -       -      F     sky130_fd_sc_hd__dfrtp_1      1    -     -     0     762
#-------------------------------------------------------------------------------------------------
```

```
Path 6: MET (151 ps) Late External Delay Assertion at pin Co
     Startpoint: (R) Co_reg/CLK
          Clock: (R) clk
       Endpoint: (F) Co
          Clock: (R) clk

                     Capture       Launch
        Clock Edge:+     971            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=     971            0

      Output Delay:-     485
       Uncertainty:-      10
     Required Time:=     476
      Launch Clock:-       0
         Data Path:-     325
             Slack:=     151

#-------------------------------------------------------------------------------------------------
# Timing Point   Flags    Arc   Edge           Cell            Fanout Load Trans Delay Arrival
#                                                                (fF)  (ps)  (ps)   (ps)
#-------------------------------------------------------------------------------------------------
  Co_reg/CLK     -       -      R     (arrival)                  14    -     0     -       0
  Co_reg/Q       -       CLK->Q F     sky130_fd_sc_hd__dfrtp_1    1  1.3    33   325     325
  Co             -       -      F     (port)                      -    -     -     0     325
#-------------------------------------------------------------------------------------------------
```

```
Path 7: MET (151 ps) Late External Delay Assertion at pin S[0]
     Startpoint: (R) S_reg[0]/CLK
          Clock: (R) clk
       Endpoint: (F) S[0]
          Clock: (R) clk

                     Capture       Launch
        Clock Edge:+     971            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=     971            0

      Output Delay:-     485
       Uncertainty:-      10
     Required Time:=     476
      Launch Clock:-       0
         Data Path:-     325
             Slack:=     151

#-------------------------------------------------------------------------------------------------
# Timing Point   Flags    Arc   Edge           Cell             Fanout Load Trans Delay Arrival
#                                                                 (fF)  (ps)  (ps)   (ps)
#-------------------------------------------------------------------------------------------------
  S_reg[0]/CLK   -        -      R     (arrival)                    14    -     0     -       0
  S_reg[0]/Q     -        CLK->Q F     sky130_fd_sc_hd__dfrtp_1      1  1.3    33   325     325
  S[0]           -        -      F     (port)                        -    -     -     0     325
#-------------------------------------------------------------------------------------------------
```

```
Path 8: MET (151 ps) Late External Delay Assertion at pin S[1]
     Startpoint: (R) S_reg[1]/CLK
          Clock: (R) clk
       Endpoint: (F) S[1]
          Clock: (R) clk

                     Capture       Launch
        Clock Edge:+     971            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=     971            0

      Output Delay:-     485
       Uncertainty:-      10
     Required Time:=     476
      Launch Clock:-       0
         Data Path:-     325
             Slack:=     151

#-------------------------------------------------------------------------------------------------
# Timing Point   Flags    Arc   Edge           Cell             Fanout Load Trans Delay Arrival
#                                                                 (fF)  (ps)  (ps)   (ps)
#-------------------------------------------------------------------------------------------------
  S_reg[1]/CLK   -        -      R     (arrival)                    14    -     0     -       0
  S_reg[1]/Q     -        CLK->Q F     sky130_fd_sc_hd__dfrtp_1      1  1.3    33   325     325
  S[1]           -        -      F     (port)                        -    -     -     0     325
#-------------------------------------------------------------------------------------------------
```

```
Path 9: MET (151 ps) Late External Delay Assertion at pin S[2]
     Startpoint: (R) S_reg[2]/CLK
          Clock: (R) clk
       Endpoint: (F) S[2]
          Clock: (R) clk

                     Capture       Launch
        Clock Edge:+     971            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=     971            0

      Output Delay:-     485
       Uncertainty:-      10
     Required Time:=     476
      Launch Clock:-       0
         Data Path:-     325
             Slack:=     151

#-------------------------------------------------------------------------------------------------
# Timing Point   Flags    Arc   Edge           Cell            Fanout Load Trans Delay Arrival
#                                                                 (fF)  (ps)  (ps)   (ps)
#-------------------------------------------------------------------------------------------------
  S_reg[2]/CLK   -       -      R     (arrival)                   14    -     0     -       0
  S_reg[2]/Q     -       CLK->Q F     sky130_fd_sc_hd__dfrtp_1     1  1.3    33   325     325
  S[2]           -       -      F     (port)                       -    -     -     0     325
#-------------------------------------------------------------------------------------------------
```

```
Path 10: MET (151 ps) Late External Delay Assertion at pin S[3]
     Startpoint: (R) S_reg[3]/CLK
          Clock: (R) clk
       Endpoint: (F) S[3]
          Clock: (R) clk

                     Capture       Launch
        Clock Edge:+     971            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=     971            0

      Output Delay:-     485
       Uncertainty:-      10
     Required Time:=     476
      Launch Clock:-       0
         Data Path:-     325
             Slack:=     151

#-------------------------------------------------------------------------------------------------
# Timing Point   Flags    Arc   Edge           Cell            Fanout Load Trans Delay Arrival
#                                                                 (fF)  (ps)  (ps)   (ps)
#-------------------------------------------------------------------------------------------------
  S_reg[3]/CLK   -       -      R     (arrival)                   14    -     0     -       0
  S_reg[3]/Q     -       CLK->Q F     sky130_fd_sc_hd__dfrtp_1     1  1.3    33   325     325
  S[3]           -       -      F     (port)                       -    -     -     0     325
#-------------------------------------------------------------------------------------------------
```

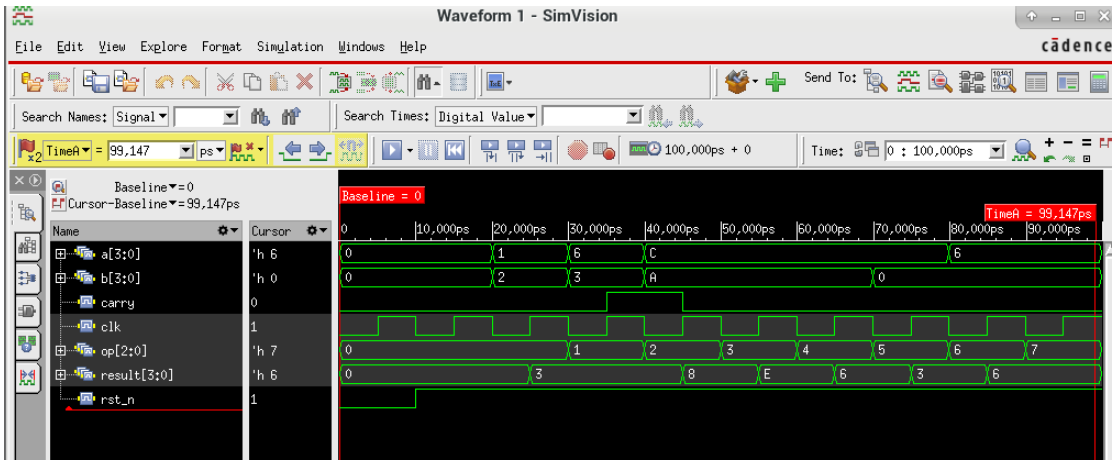
2.3 Waveform of RTL and netlist simulation
Waveform from both RTL and netlist simulation and gives

make verify GUI=”-gui”

```
[admin@centos7 synthesis]$ make verify GUI="-gui"
xrun -gui +xm64bit -sv \
03_synth/*_gate.v \
01_tb/testbench.v \
-vlogext .sv \
-f 02_sim/flist.f \
 \
-delay_mode punit \
-timescale 1ns/10ps \
+access+rcw
TOOL:    xrun(64)        20.09-s001: Started on May 12, 2025 at 00:49:34 ED
xrun(64): 20.09-s001: (c) Copyright 1995-2020 Cadence Design Systems, Inc.
xrun: *W,FMDEF: The default file type mapping of .sv is being overwritten.
xmsim: *W,DSEM2009: This SystemVerilog design is simulated as per IEEE 180
imulation semantics.

-----------------------------------
Relinquished control to SimVision...
xcelium>
xcelium> source /opt/cadence/XCELIUM2009/tools/xcelium/files/xmsimrc
```

we can also view the schematic and netlist
If we double-click into any cell-box it will show the model inside the standard cell model



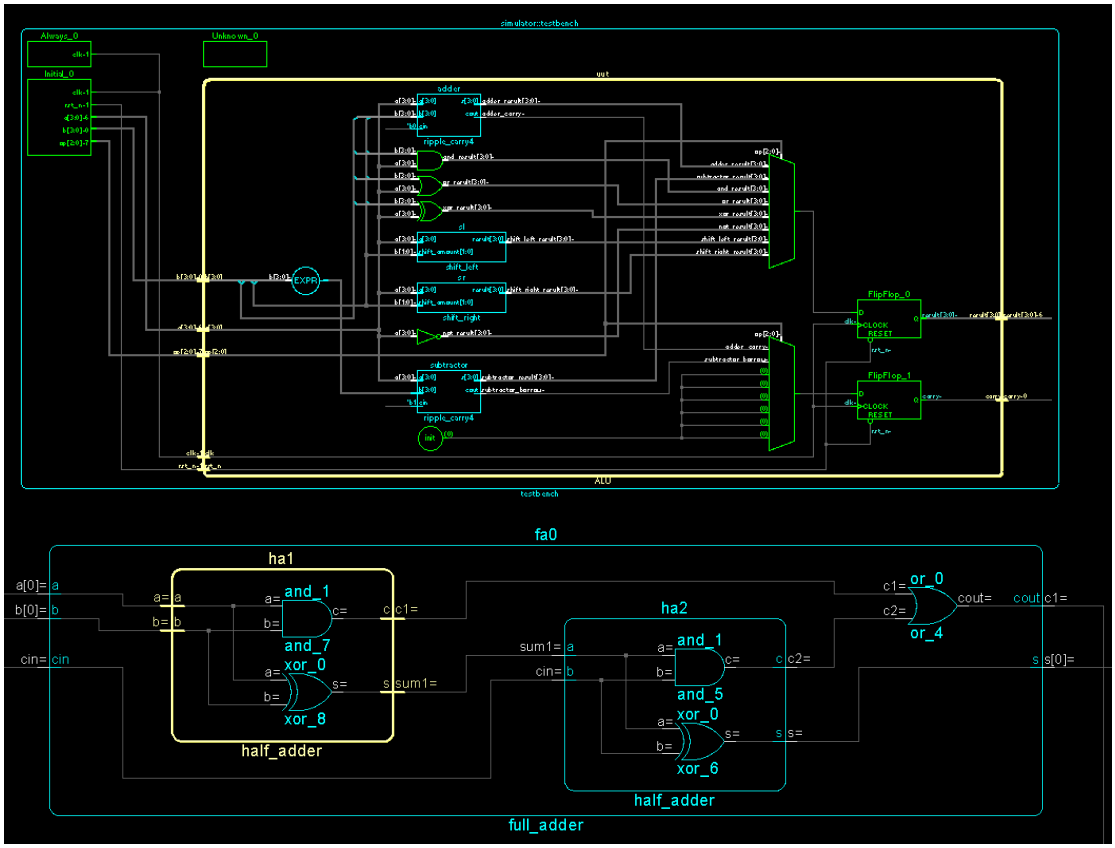


Figure 2.2.2.1 RTL viewer schematic and Waveform viewer