

**Vietnam National University Ho Chi Minh City**  
**HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY**



**LAB 2: DIGITAL LOGIC COMPONENTS**

**Subject: Digital IC Design**

**Class L03 --- Semester 242**

**Group: 12**

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## 1. EXPERIMENT 1

**Objective:** Implement CMOS-based logic gates.

**Requirements:**

- Complete the truth table, schematic, and symbol for each component.
- Run DC analysis and transient simulation.
- Create layouts for each logic gate, then show DRC confirmation and corresponding schematic with proof of LVS.

### INVERTER:

#### 1.1 Schematic

The schematic of a CMOS inverter

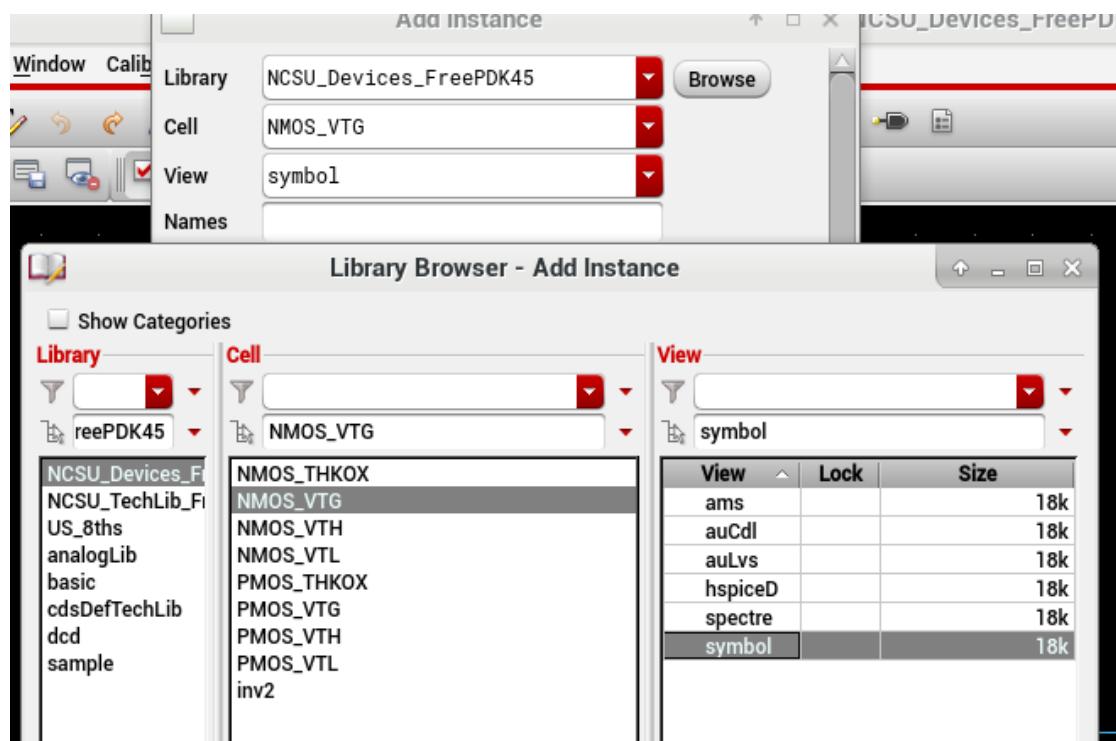
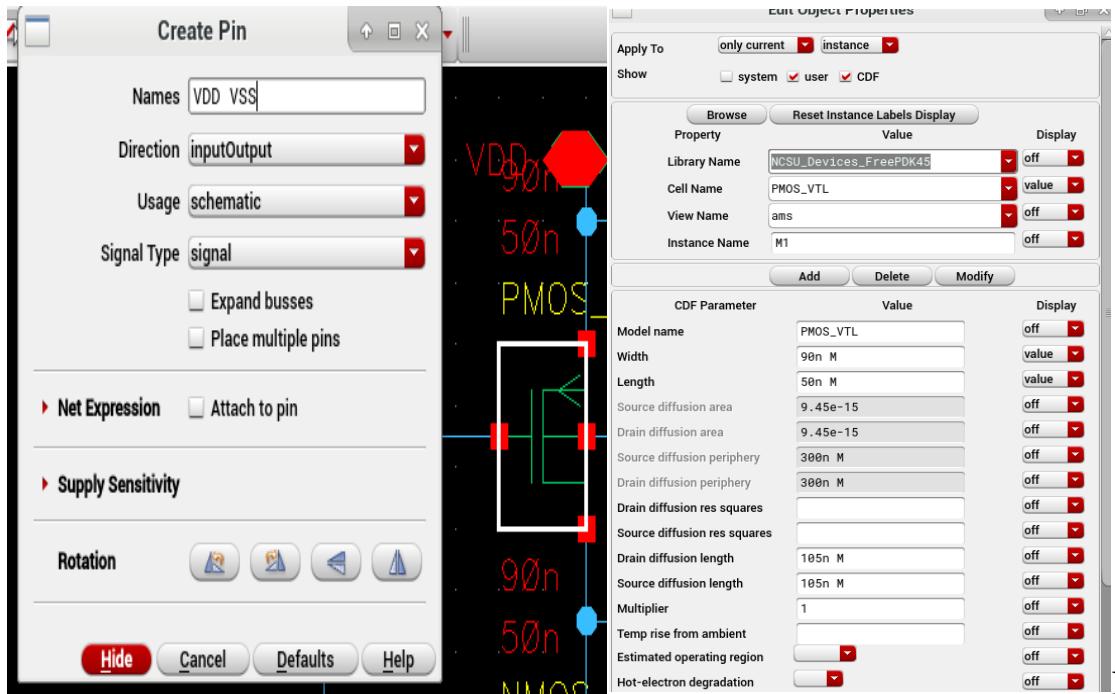


Figure 1.1.1 Take NMOS and PMOS on workspace



Figure

1.1.2 Connect components and add pins to the schematic.

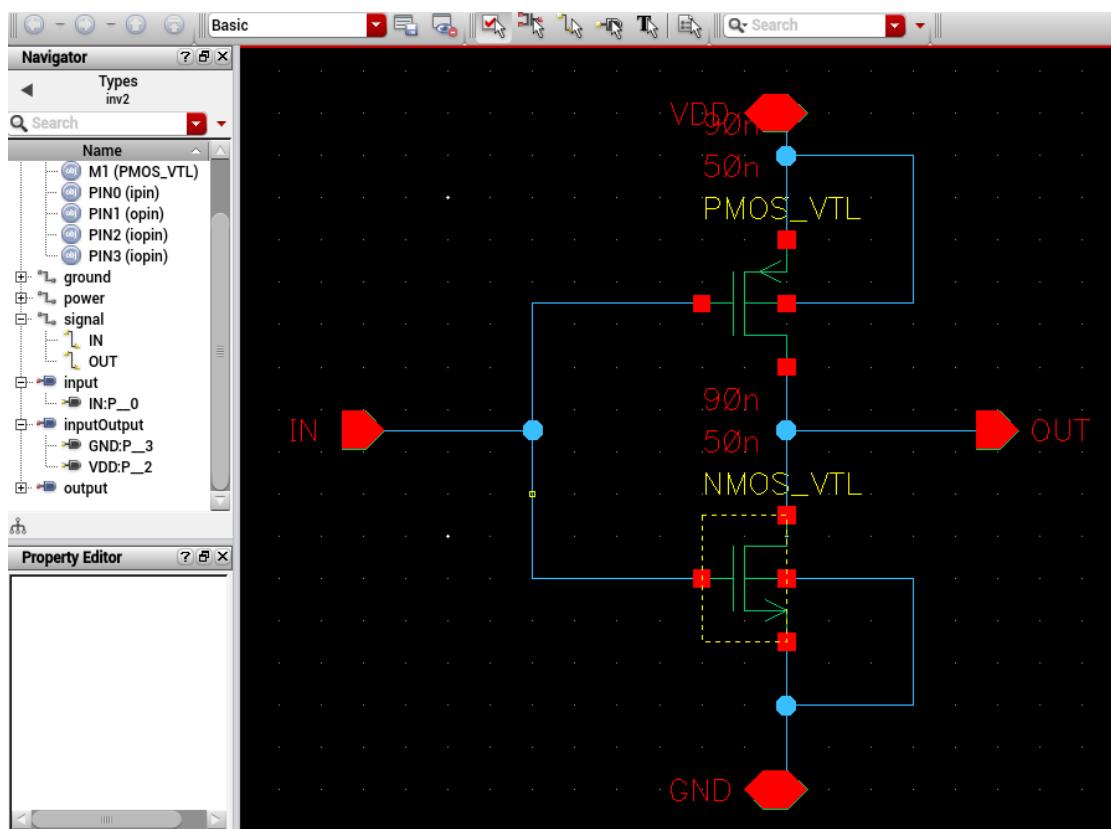
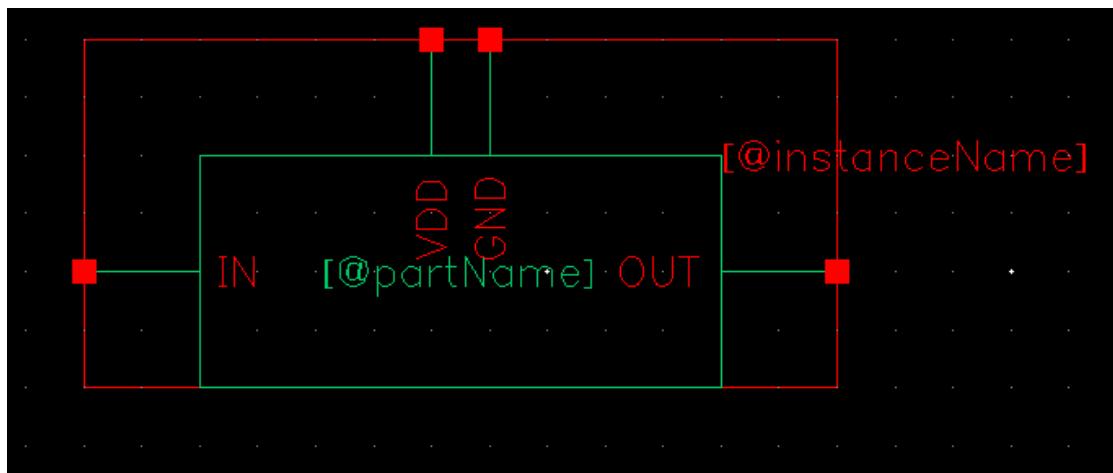
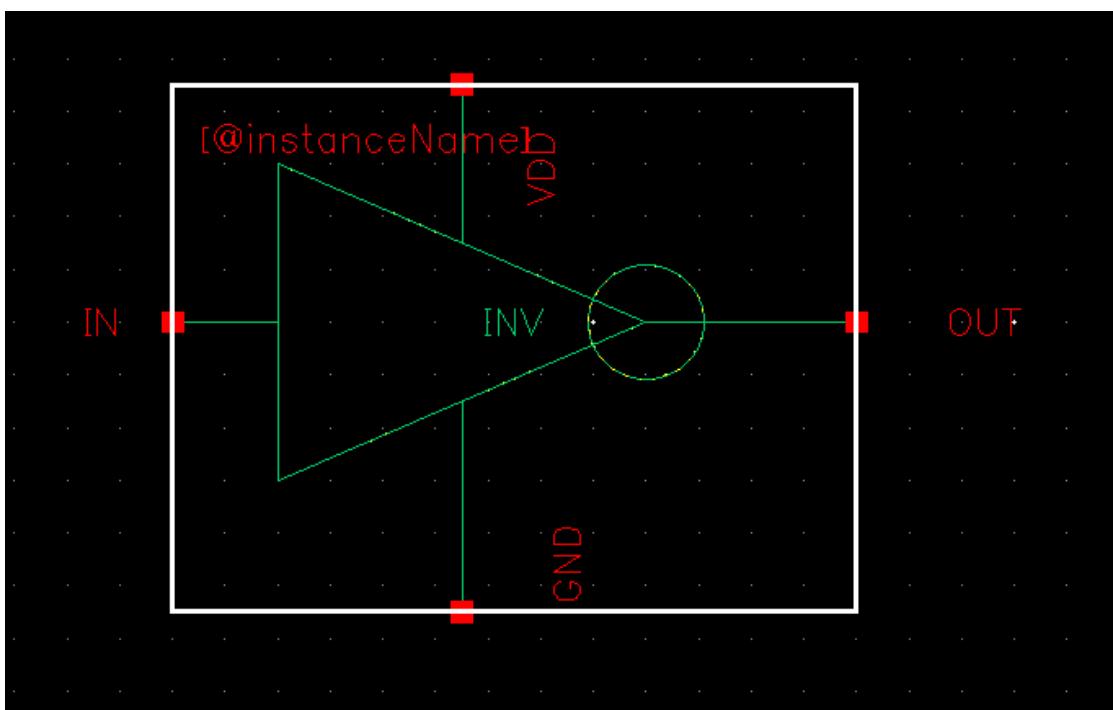


Figure 1.1.3 The schematic of a CMOS inverter

The symbol of intervert:

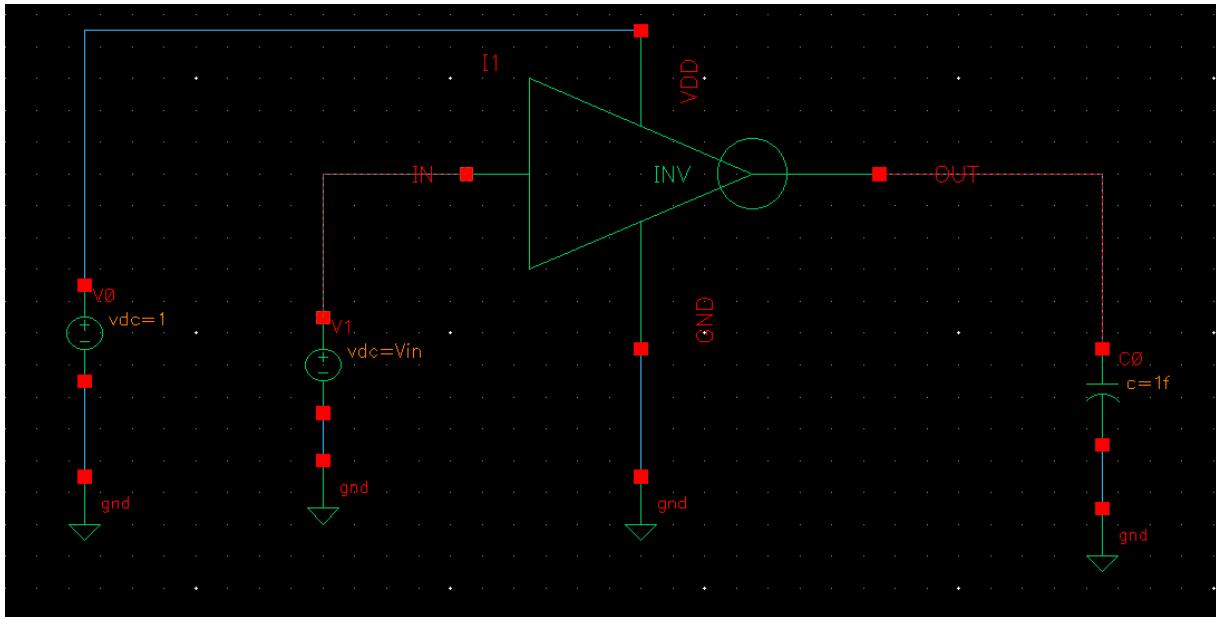


**Figure 1.1.4** Re-draw inverter's symbol

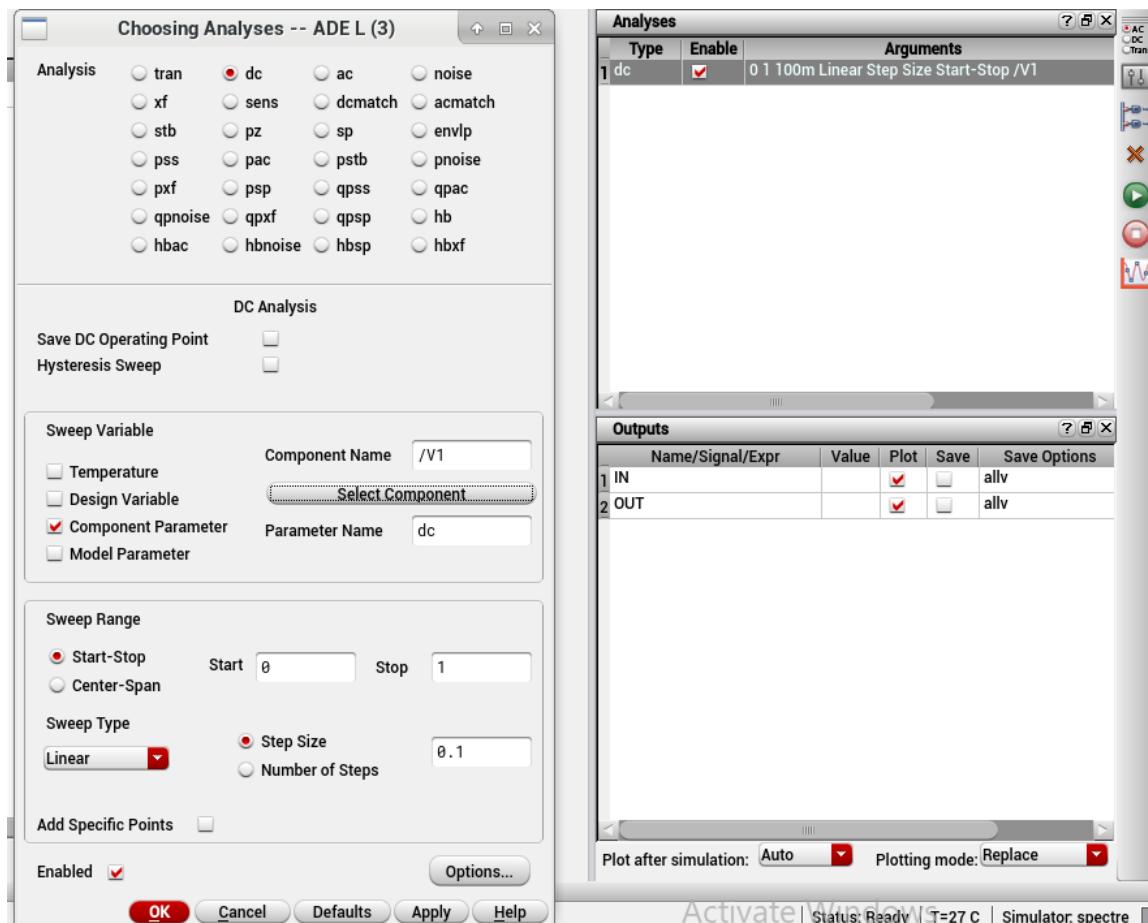


**Figure 1.1.5** Symbol of INV

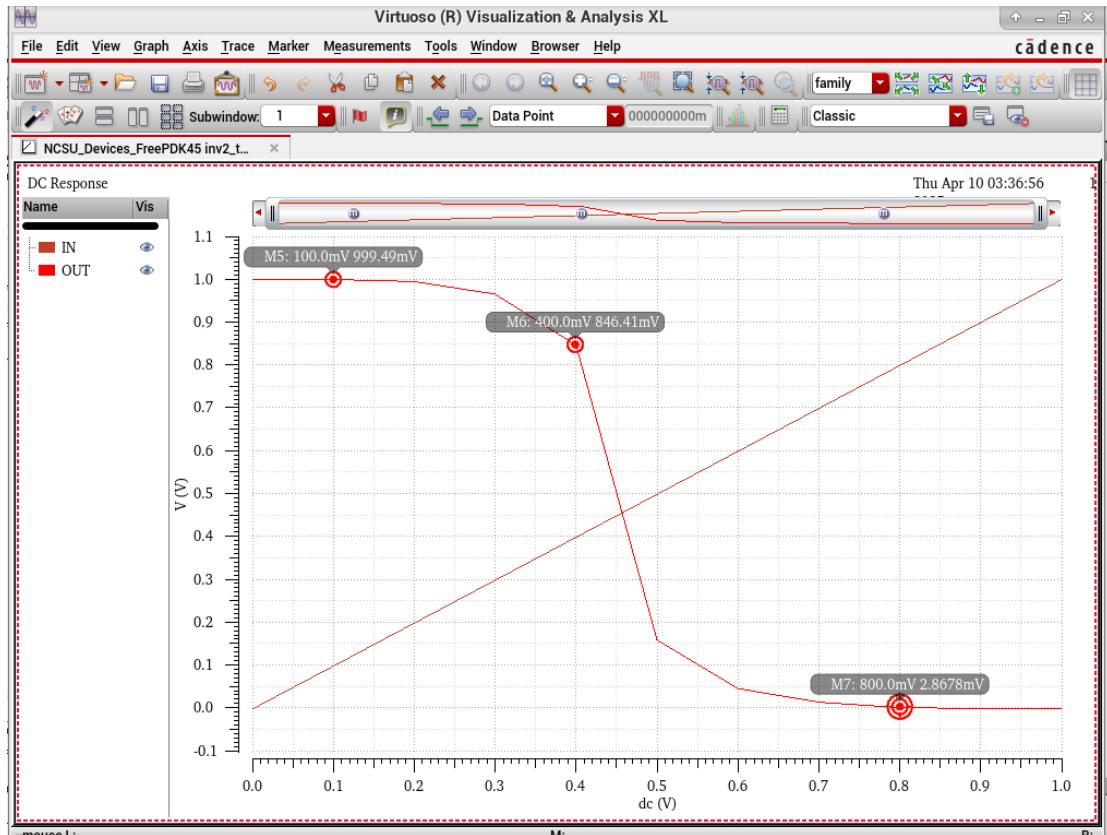
## 1.2 DC Analysis simulation:



**Figure 1.2.1 Insert vdc at the input of the inverter .**



**Figure 1.2.1 DC analysis setting instructions.**



**Figure 1.2.3** Voltage transfer curve (VTC) of CMOS inverter.

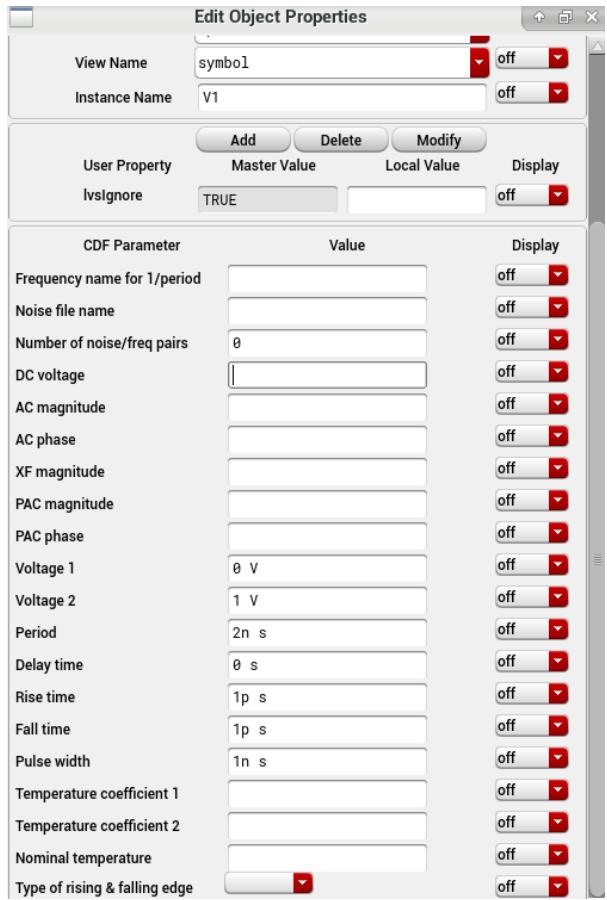
During the simulation process, students record the following two results: output voltage values at various values of Vin with a 0.1V step and plot the curve of Vout .

**Table 1.2.1** The output voltage values at various values of Vin with 0.1V step

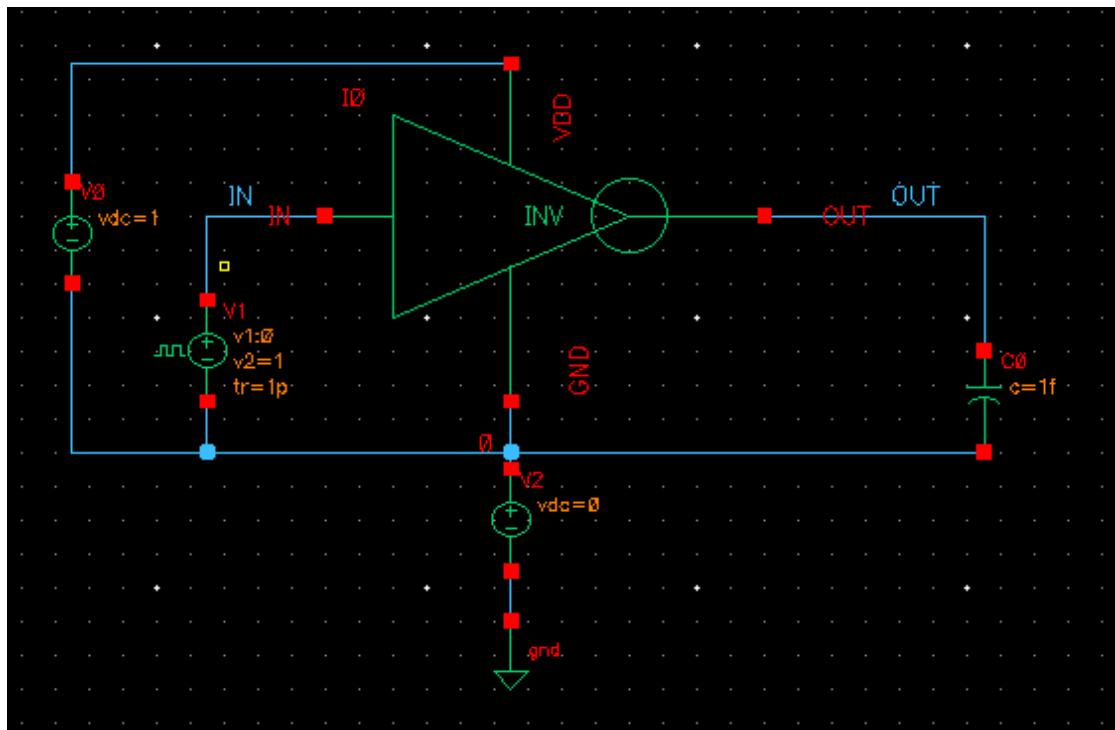
Vin	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0
Vout	0.999	0.994	0.965	0.846	0.16	0.047	0.015	0.028	308u	24u

### 1.3 Transient simulation

Use ADE-L to perform a time-domain simulation to verify the operation according to the truth table of the INV gate, represented in the form of an output waveform. To conduct this simulation, assemble a testbench circuit consisting of a pulse source (vpulse), an output capacitor, and provide power to the circuit (vdc). The circuit parameters are configured as follows:

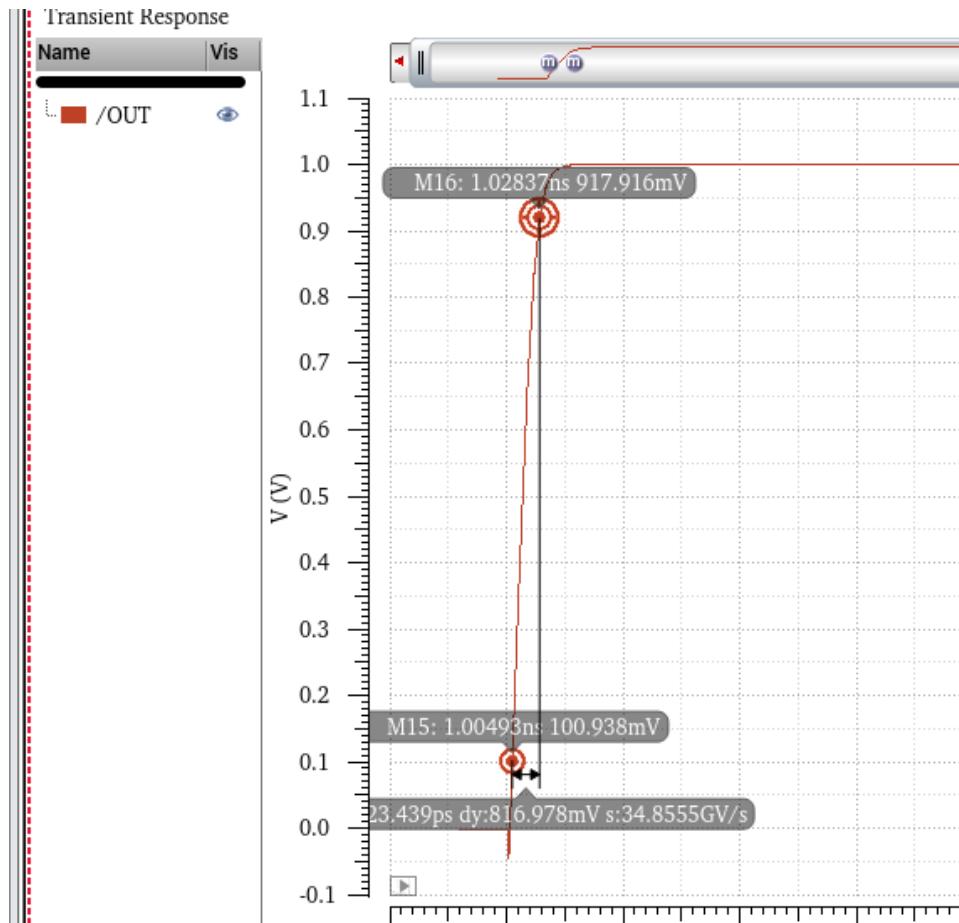


**Figure 1.3.1** Parameters for transient simulation

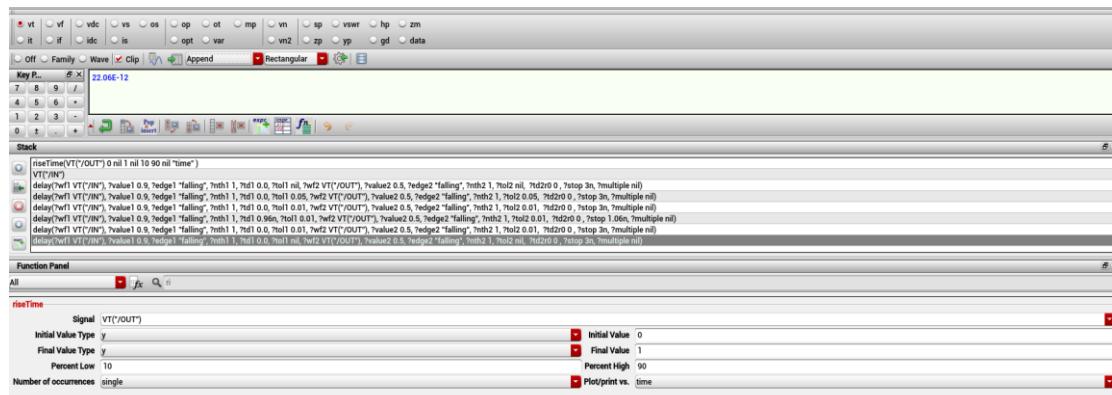


**Figure 1.3.2** The testbench of a CMOS inverter

## Parameters Rising time: (10%-90%)

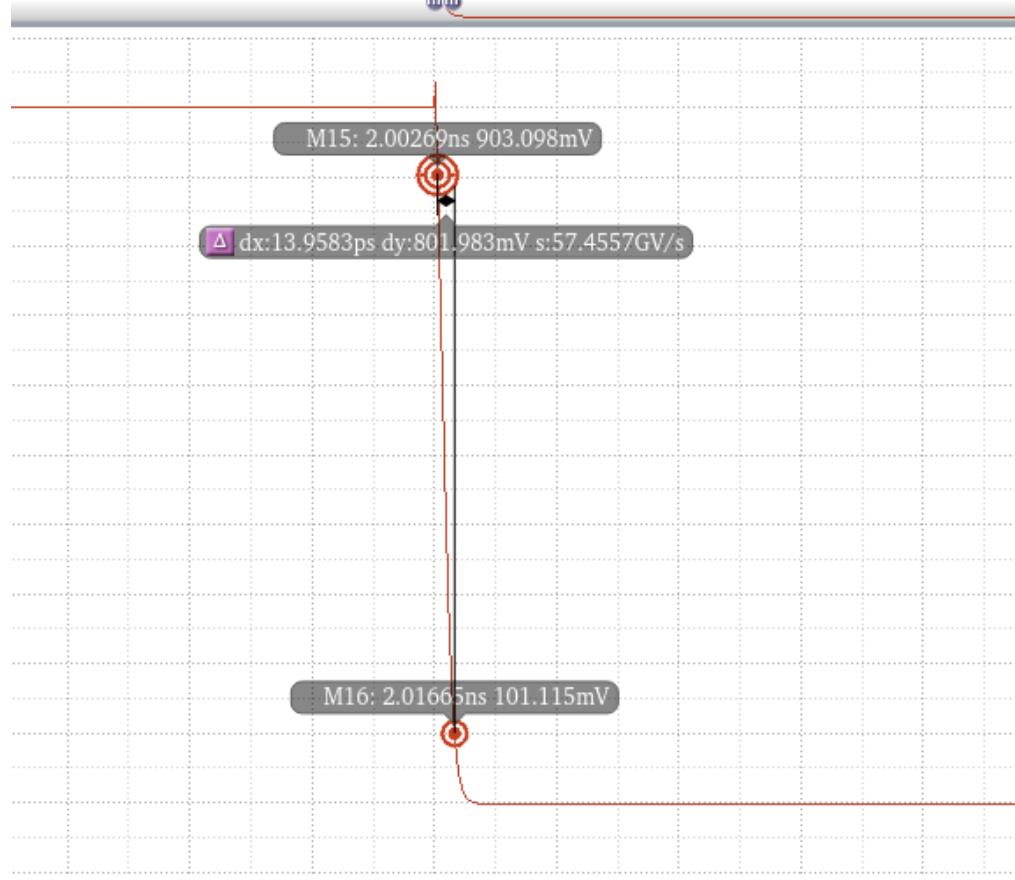


**Figure 1.3.3** The result of rising time using delta marker.

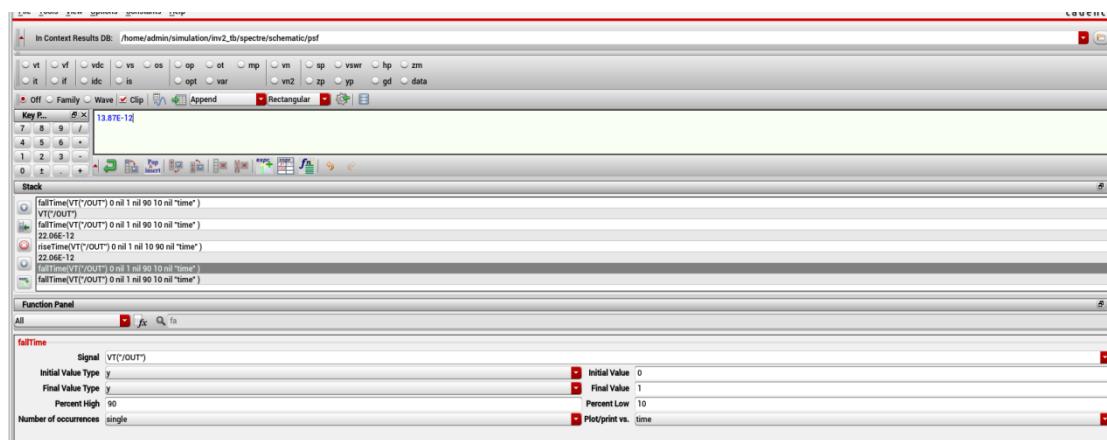


**Figure 1.3.4** The result of rising time using Calculator.

## Parameters Falling time: (90%-10%)

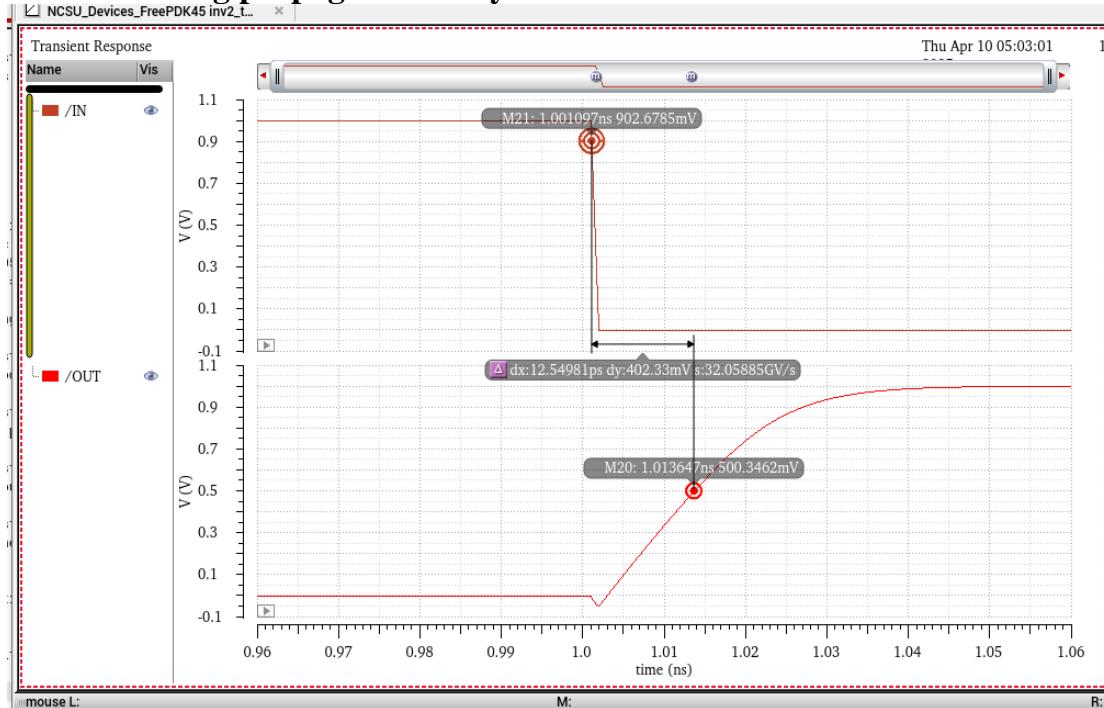


**Figure 1.3.5** The result of falling time using delta marker.

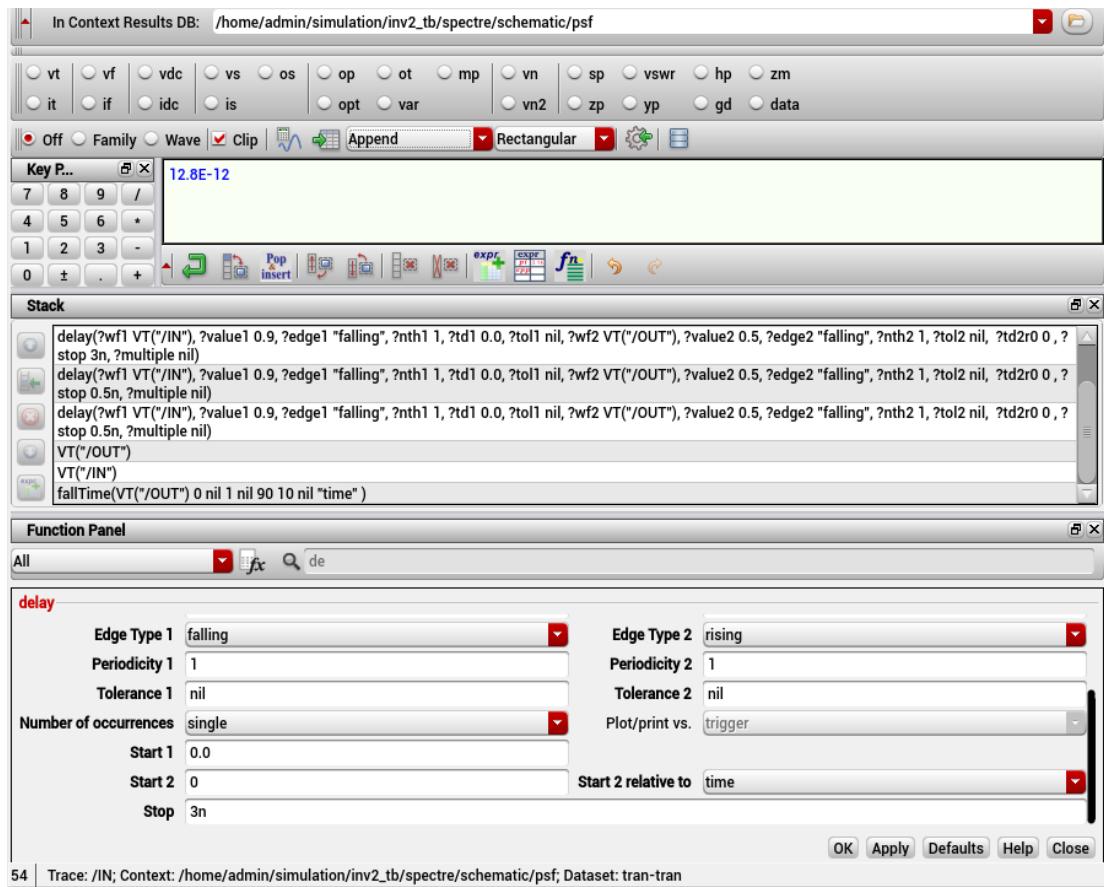


**Figure 1.3.6** The result of falling time using Calculator.

## Parameters Rising propagation delay

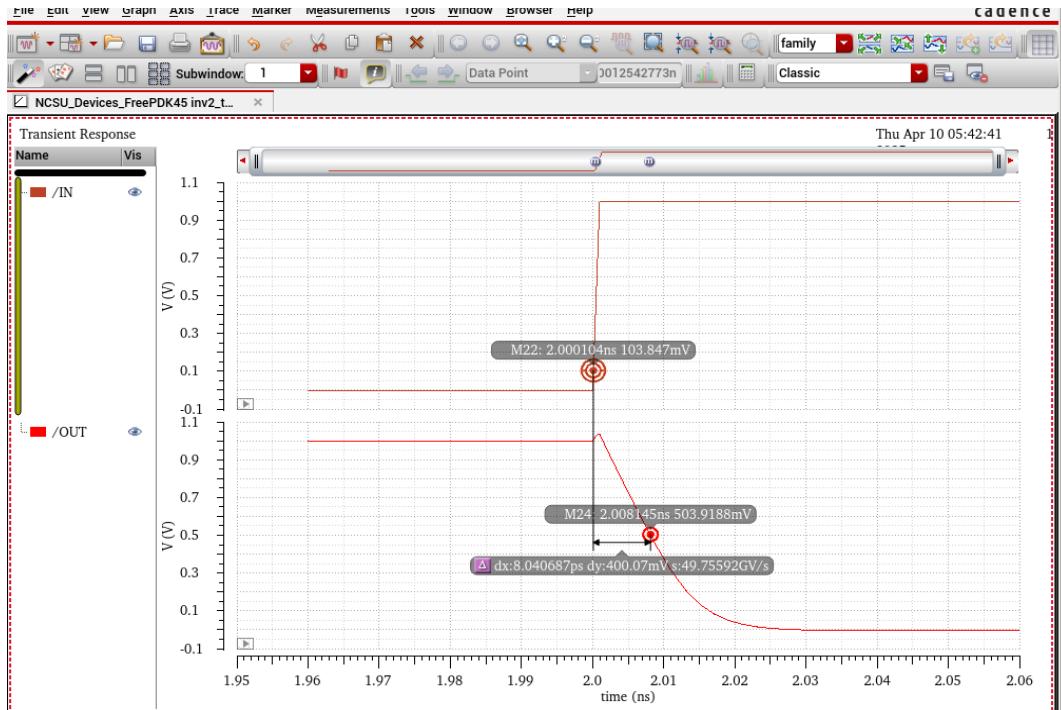


**Figure 1.3.7** The result of rising propagation delay using delta marker.

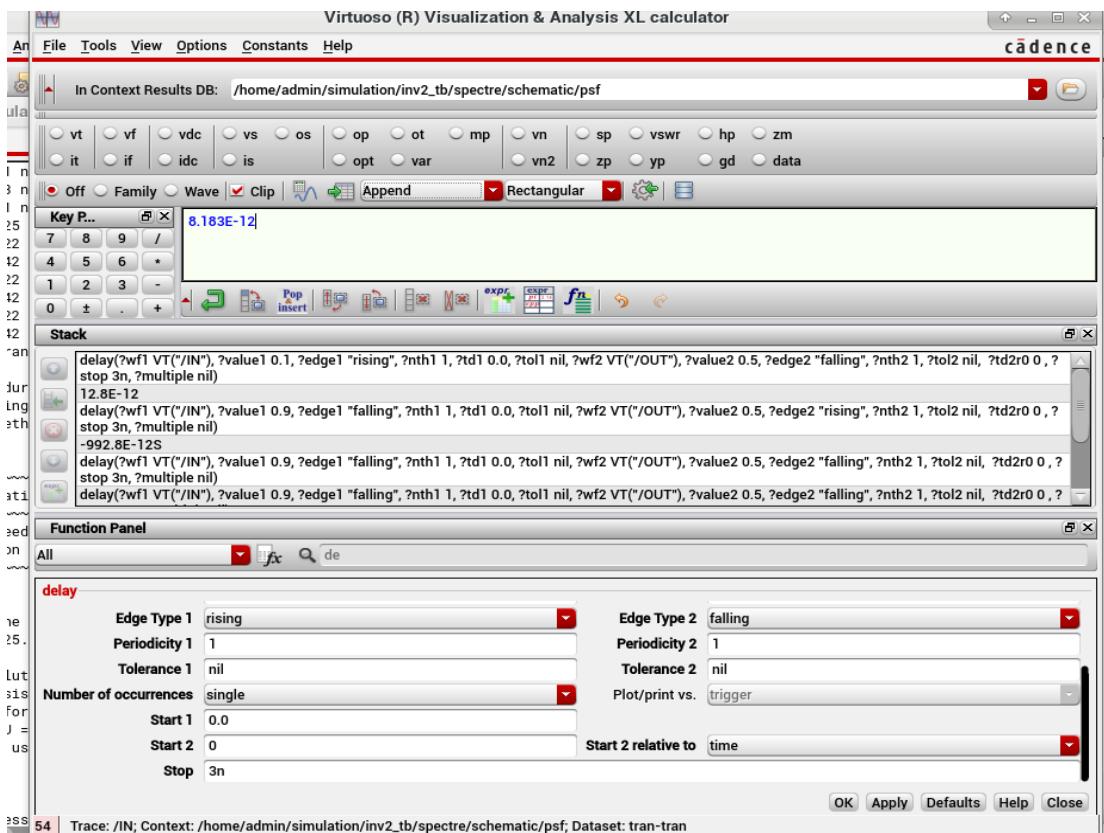


**Figure 1.3.8** The result of rising propagation delay using Calculator.

## Parameters Falling propagation delay



**Figure 1.3.9** The result of falling propagation delay using delta marker.



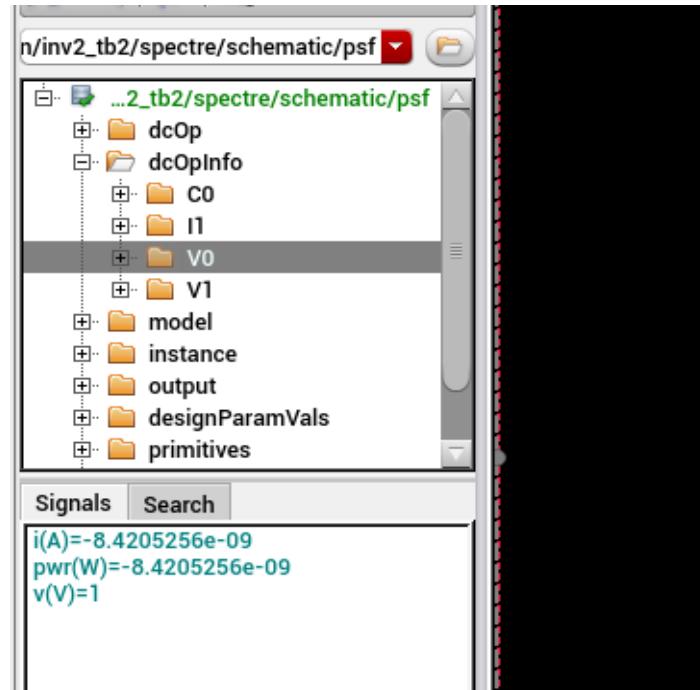
**Figure 1.3.10** The result of falling propagation delay using Calculator.

## Average propagation delay

$$t_{pd} = \frac{t_{PLH} + t_{PHL}}{2}$$

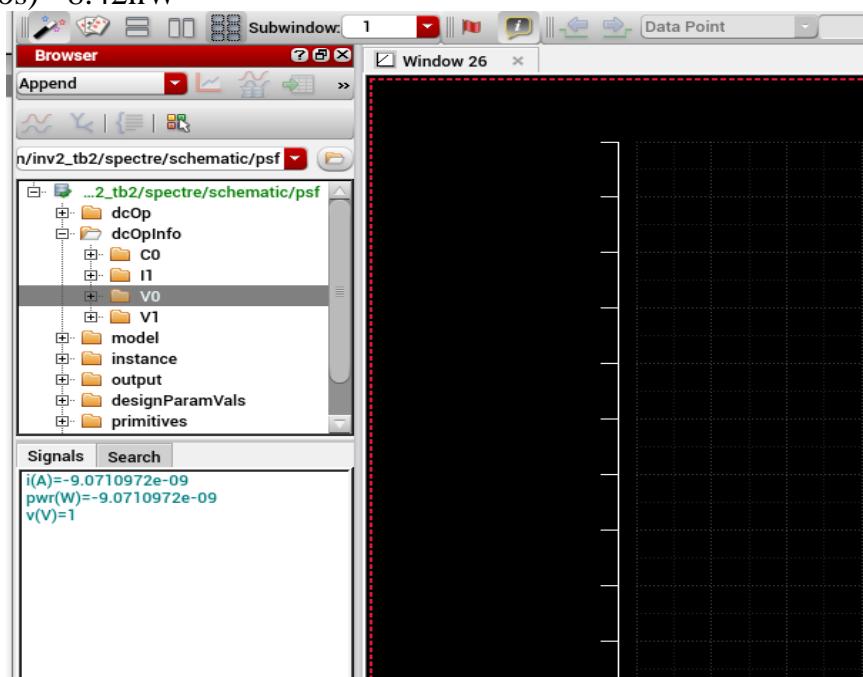
$$=(12.8\text{ps}+8.2\text{ps})/2=10.5 \text{ ps}$$

## Dynamic power



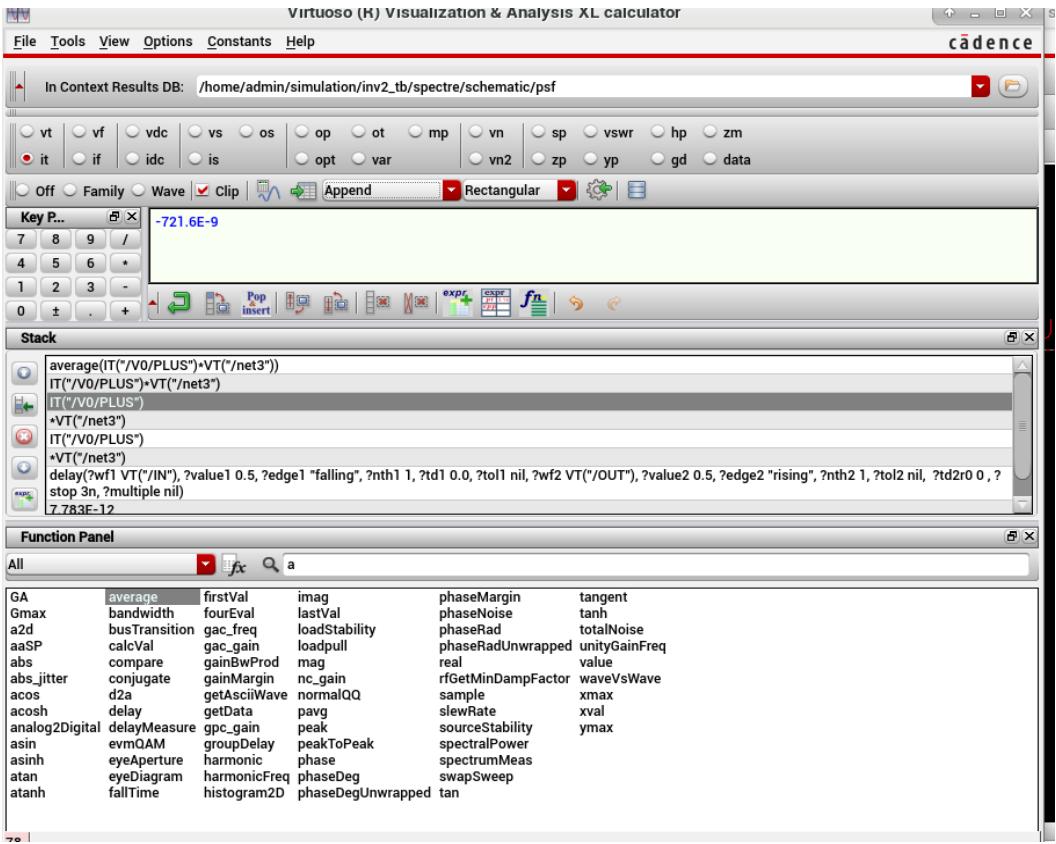
**Figure 1.3.11** The result of static power based on NMOS.

$$P_{\text{Static(Nmos)}} = 8.42 \text{nW}$$



**Figure 1.3.12** The result of static power based on PMOS

$$P_{\text{Static(Pmos)}} = 9.07 \text{nW}$$



**Figure 1.3.13** The result of total power consumption using Calculator

$$P_{total} = \text{average}(u(t) \times i(t)) = 721 \text{nW}$$

$$P_{dynamic} = P_{total} - P_{static} = 721 \times 10^{-9} - 9.1 \times 10^{-9} = 711.9 \text{nW}$$

Parameters	Result
Rising time: (10% - 90%)	22.1ps
Falling time: (90% - 10%)	13.9ps
Rising propagation delay	12.8ps
Falling propagation delay	8.2ps
Average propagation delay	10.5ps
Dynamic power	711.9nW
Static power	9.1nW

**Table 1.3.1:** Measurement results of CMOS

## NAND2 GATE:

### 1.4 Schematic

Input A	Input B	$Y = \bar{A}\bar{B}$
0	0	1
0	1	1
1	0	1
1	1	0

Table 1.4.1: Truth table of NAND

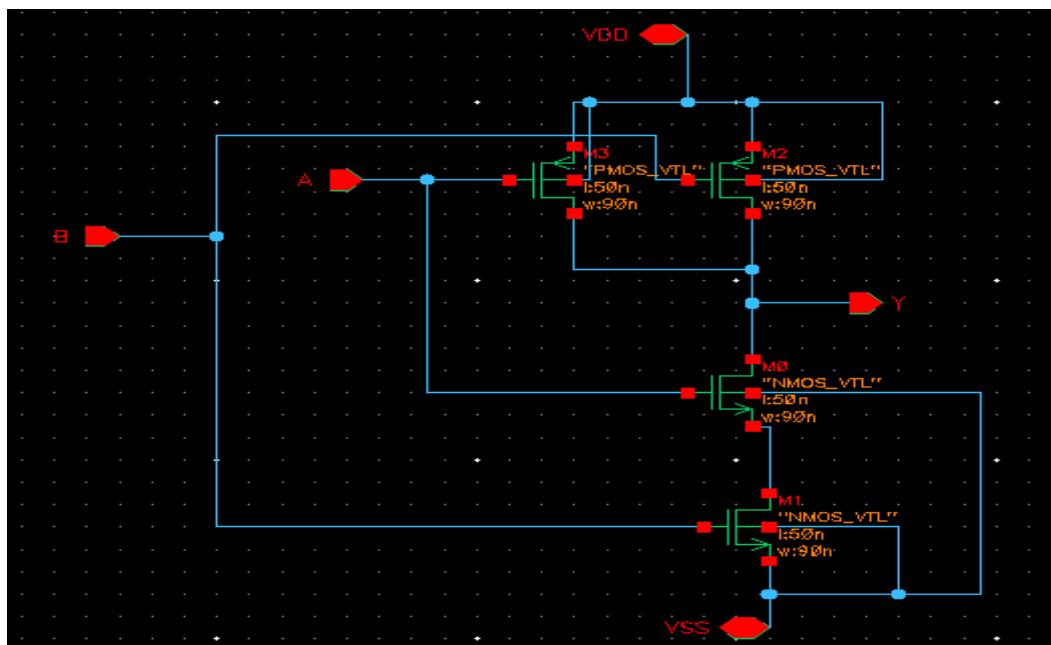


Figure 1.4.1 : Schematic of NAND

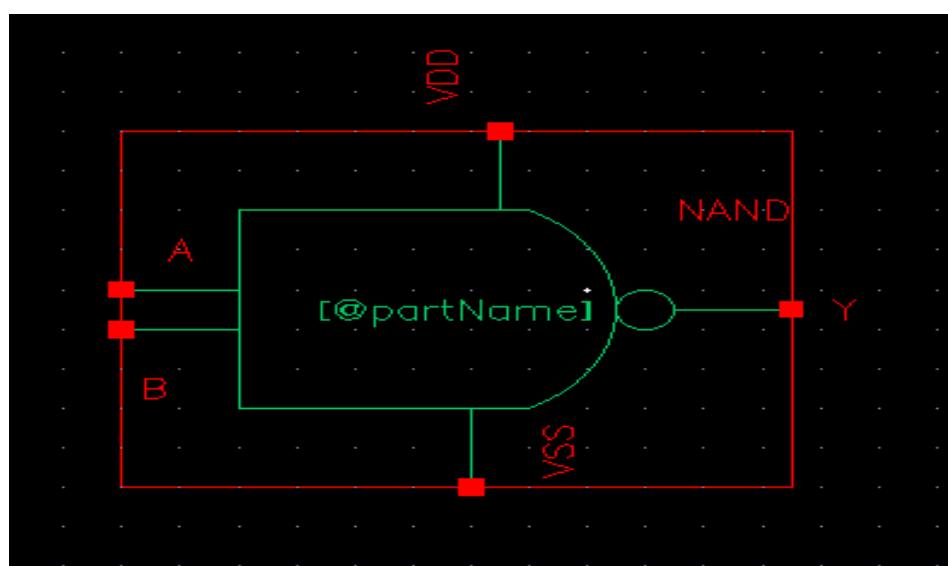


Figure 1.4.2: symbol of NAND

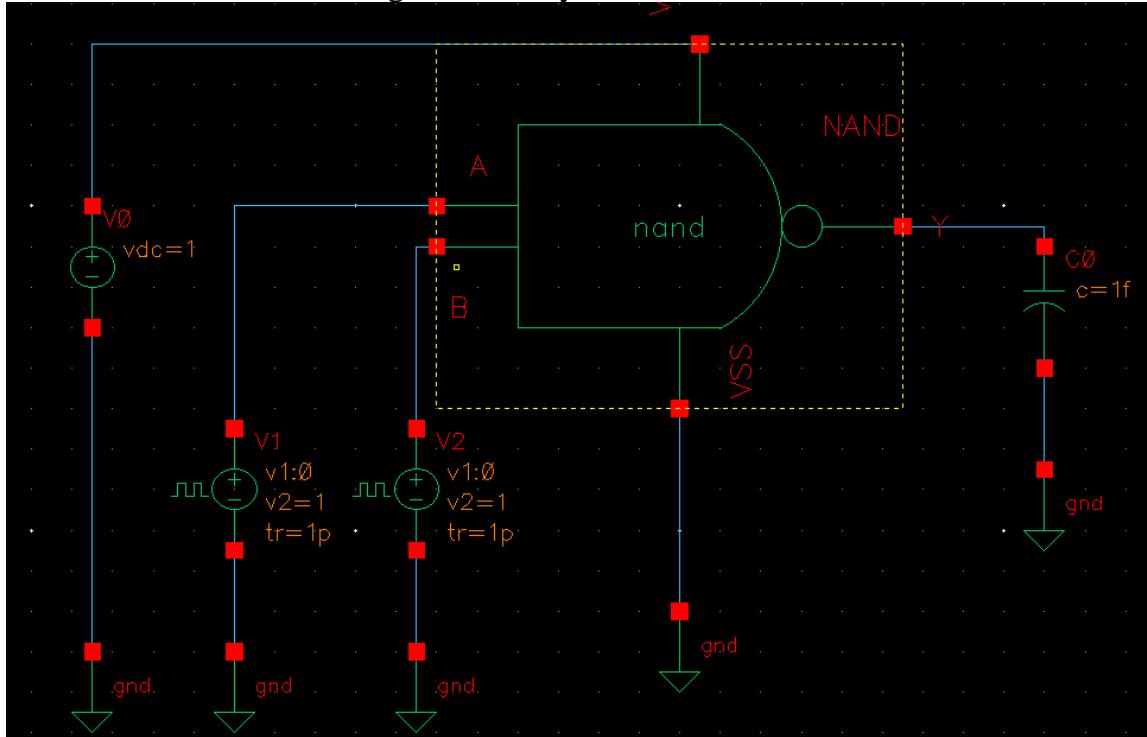


Figure 1.4.3: Testbench of NAND

## 1.5 DC analysis Simulation

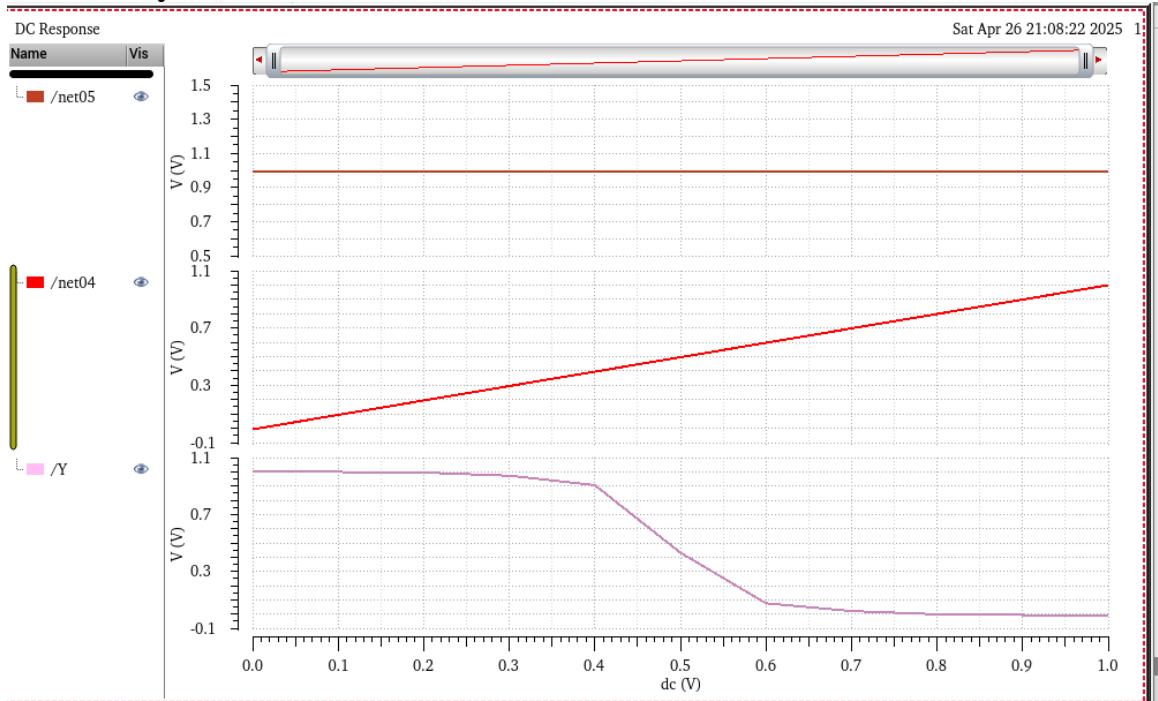


Figure 1.5.1 : A, B & Y DC analysis of EXOR2 when sweeping  $V_A$

## 1.6 Transient Analysis Simulation

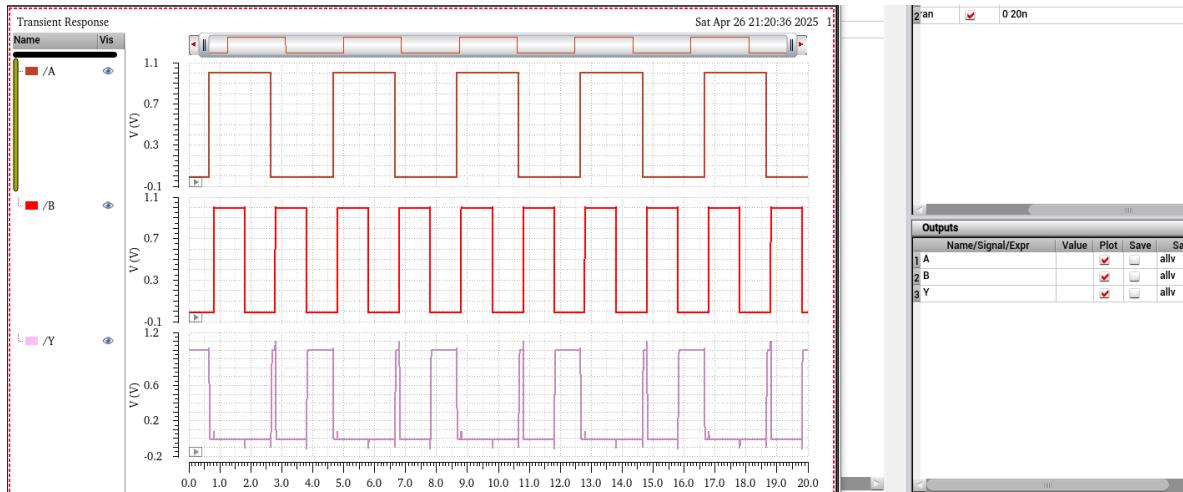
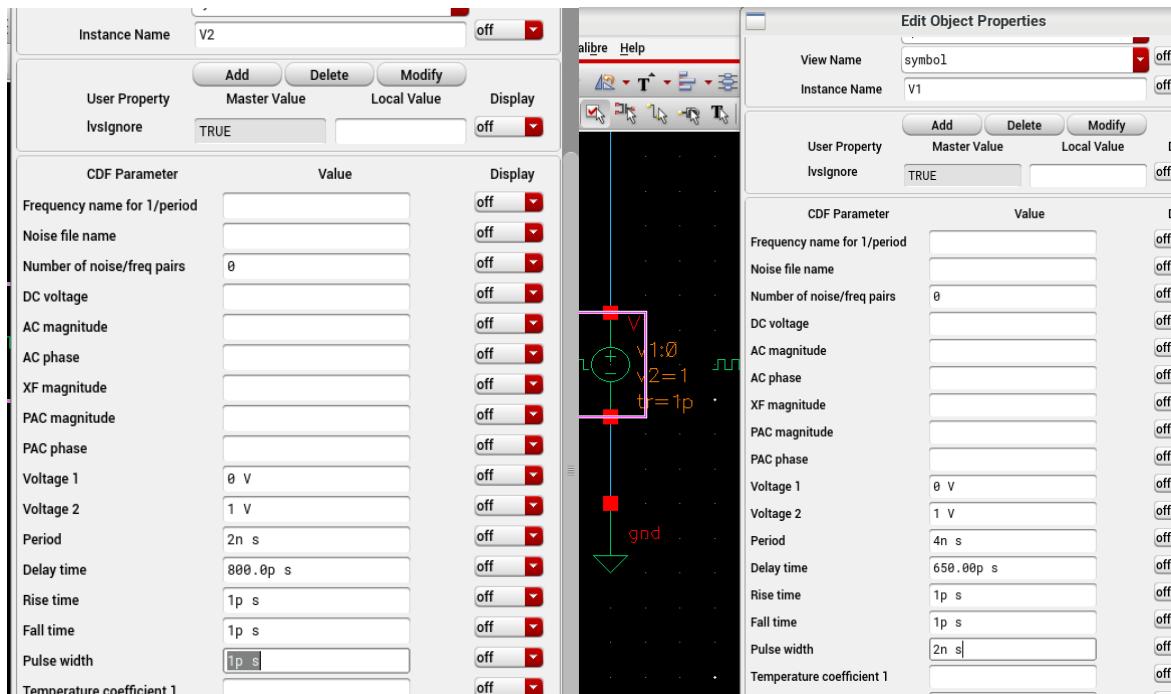


Figure 1.6.1: Transient of NAND

### - Use built-in functions in Calculator



**Key P...** 12.36E-12

**Stack**

```

riseTime(VT("/Y") 0 nil 1 nil 10 90 nil "time")
VT("/Y")
riseTime(riseTime(vT("/net4") 0 nil 1 nil 10 90 nil "time") 0 nil 1 nil 10 90 nil "time")
riseTime(riseTime(vT("/net4") 0 nil 1 nil 10 90 nil "time"))
fallTime(VT("/net4") 0 nil 1 nil 90 10 nil "time")
VT("/net4")
fallTime(vT("/net4") 0 nil 1 nil 90 10 nil "time")
VT("/net4")

```

**Function Panel**

All

**riseTime**

Signal VT("/Y")

Initial Value Type y Initial Value 0

Final Value Type y Final Value 1

Percent Low 10 Percent High 90

Number of occurrences single Plot/print vs. time

**Key P...** 10.37E-12

**Stack**

```

fallTime(VT("/Y") 0 nil 1 nil 90 10 nil "time")
VT("/Y")
12.36E-12
riseTime(VT("/Y") 0 nil 1 nil 10 90 nil "time")
VT("/Y")
riseTime(riseTime(vT("/net4") 0 nil 1 nil 10 90 nil "time") 0 nil 1 nil 10 90 nil "time")
riseTime(vT("/net4") 0 nil 1 nil 10 90 nil "time")
fallTime(VT("/net4") 0 nil 1 nil 90 10 nil "time")

```

**Function Panel**

All

**fallTime**

Signal VT("/Y")

Initial Value Type y Initial Value 0

Final Value Type y Final Value 1

Percent High 90 Percent Low 10

Number of occurrences single Plot/print vs. time

**Key P...** 8.182E-12

**Stack**

```

delay(?wf1 VT("/net3"), ?value1 0.9, ?edge1 "falling", ?nth1 1, ?td1 0.0, ?tol1 nil, ?wf2 VT("/Y"), ?value2 0.5, ?edge2 "rising", ?nth2 1, ?tol2 nil, ?td2r0 0, ?
stop 3n, ?multiple nil)
VT("/Y")
8.182E-12
delay(?wf1 VT("/net3"), ?value1 0.9, ?edge1 "falling", ?nth1 1, ?td1 0.0, ?tol1 nil, ?wf2 VT("/Y"), ?value2 0.5, ?edge2 "rising", ?nth2 1, ?tol2 nil, ?td2r0 0, ?
stop 3n, ?multiple nil)
1.008E-9
delay(?wf1 VT("/net3"), ?value1 0.9, ?edge1 "rising", ?nth1 1, ?td1 0.0, ?tol1 nil, ?wf2 VT("/Y"), ?value2 0.5, ?edge2 "rising", ?nth2 1, ?tol2 nil, ?td2r0 0, ?
stop 3n, ?multiple nil)

```

**Function Panel**

All

**delay**

Signal1 VT("/net3") Signal2 VT("/Y")

Threshold Value 1 0.9 Threshold Value 2 0.5

Edge Number 1 1 Edge Number 2 1

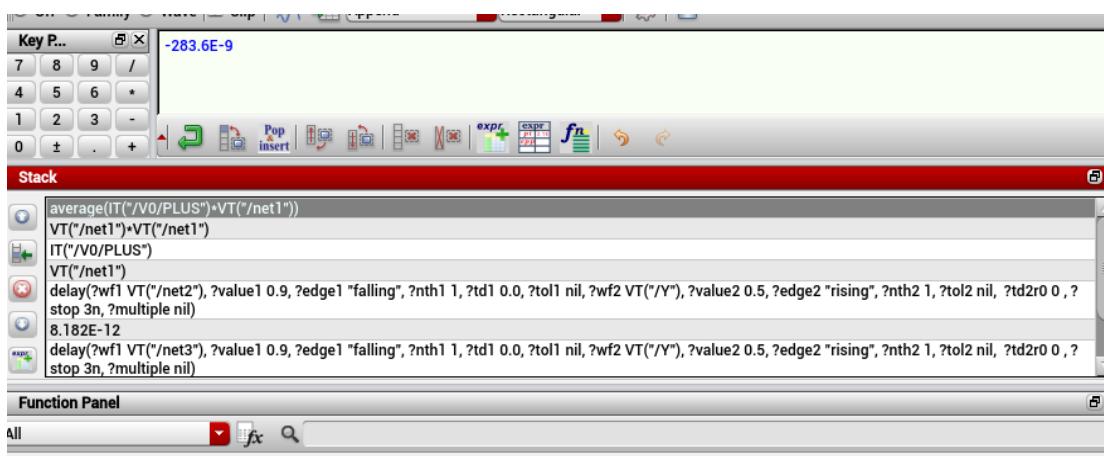
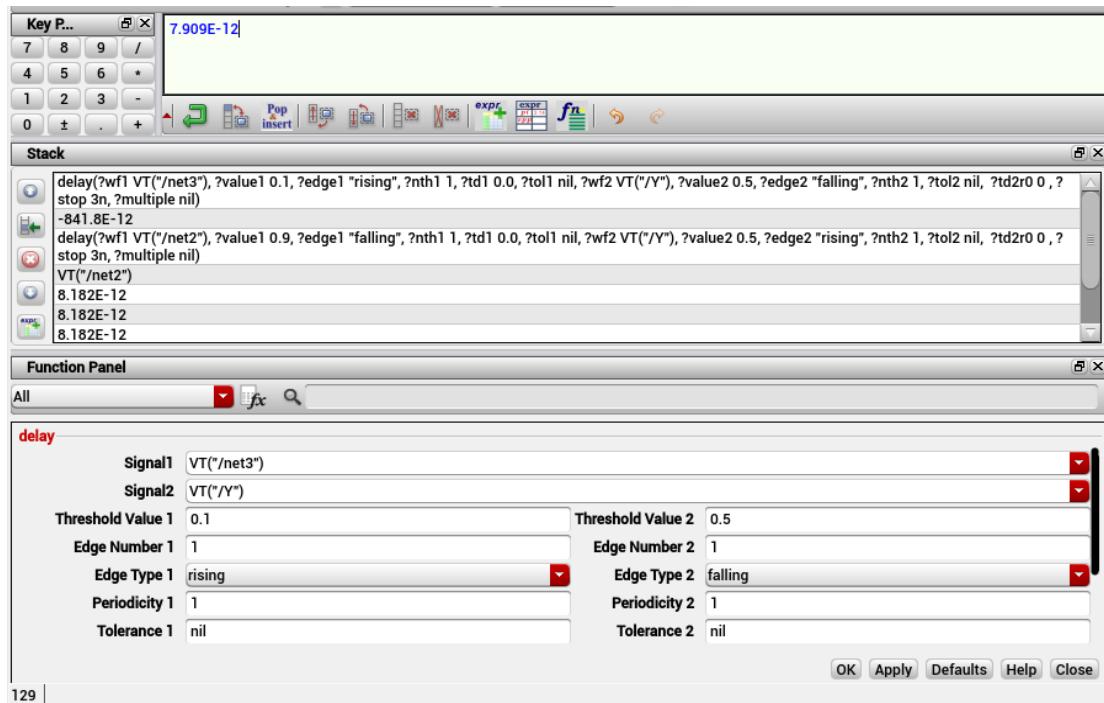
Edge Type 1 falling Edge Type 2 rising

Periodicity 1 1 Periodicity 2 1

Tolerance 1 nil Tolerance 2 nil

OK Apply Defaults Help Close

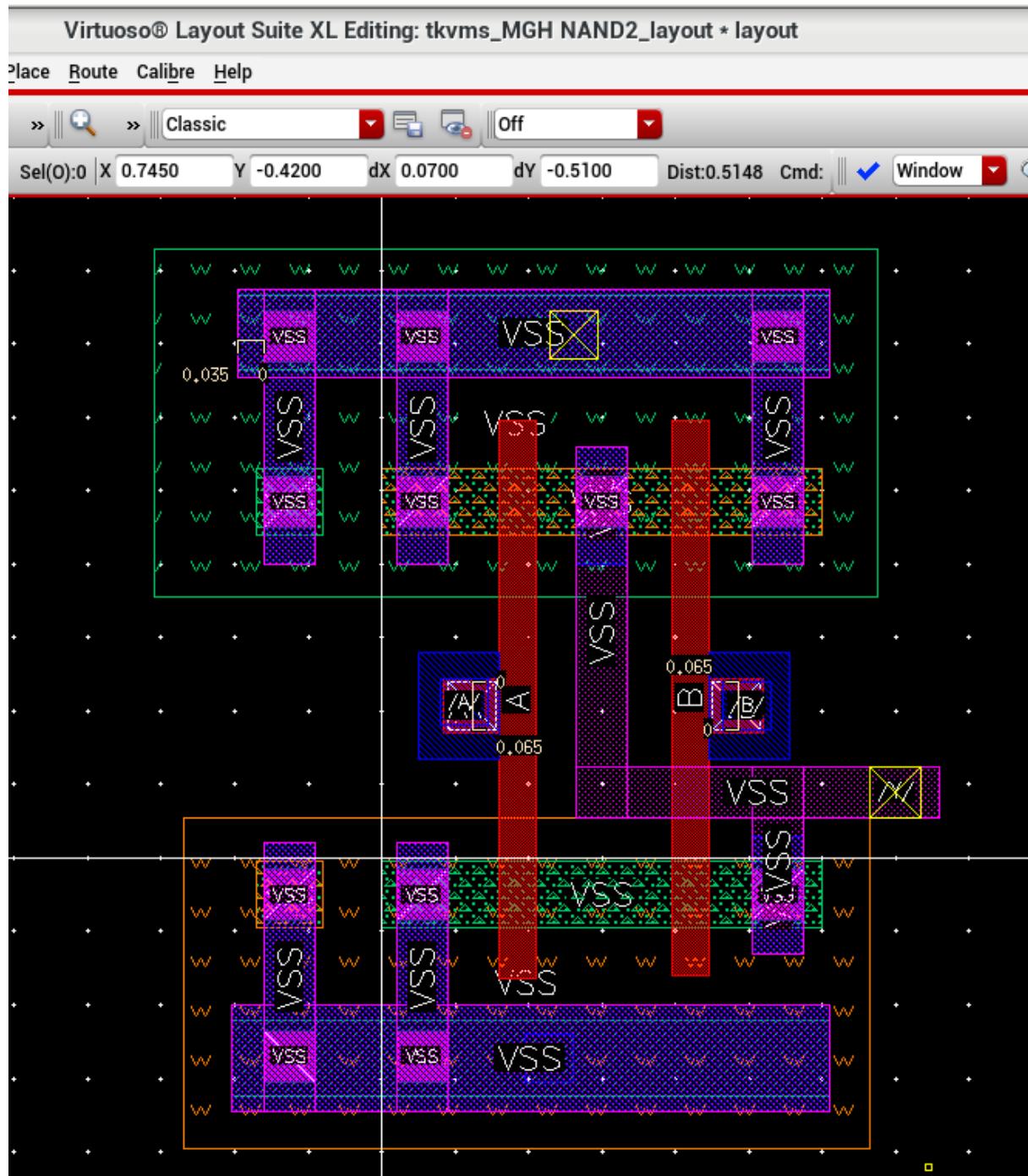
129



Parameters	Result
Rising time: (10%-90%)	12.36ps
Falling time: (90%-10%)	10.37ps
Rising propagation delay	8.18ps
Falling propagation delay	7.9ps
Average propagation delay	8.04ps
Power consumption	283.6nW

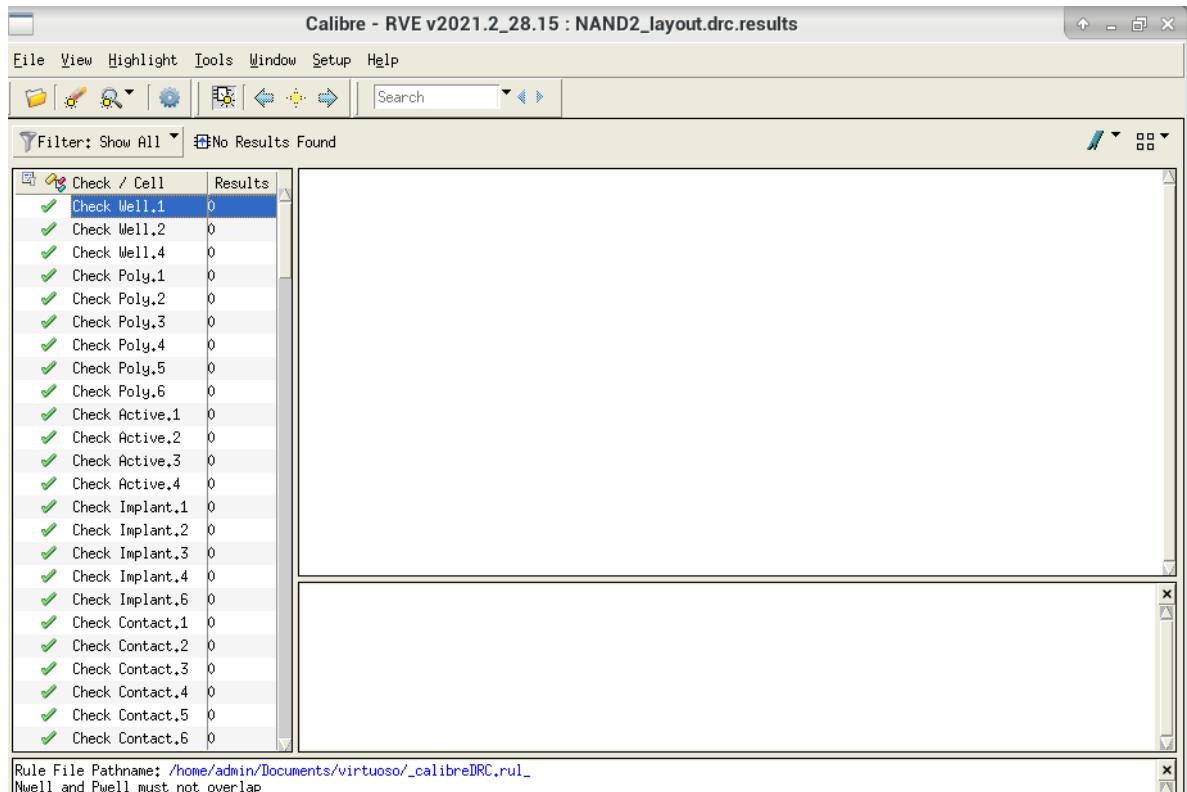
**Table 1.6.1:** Measurement results of NAND

- LAYOUT:



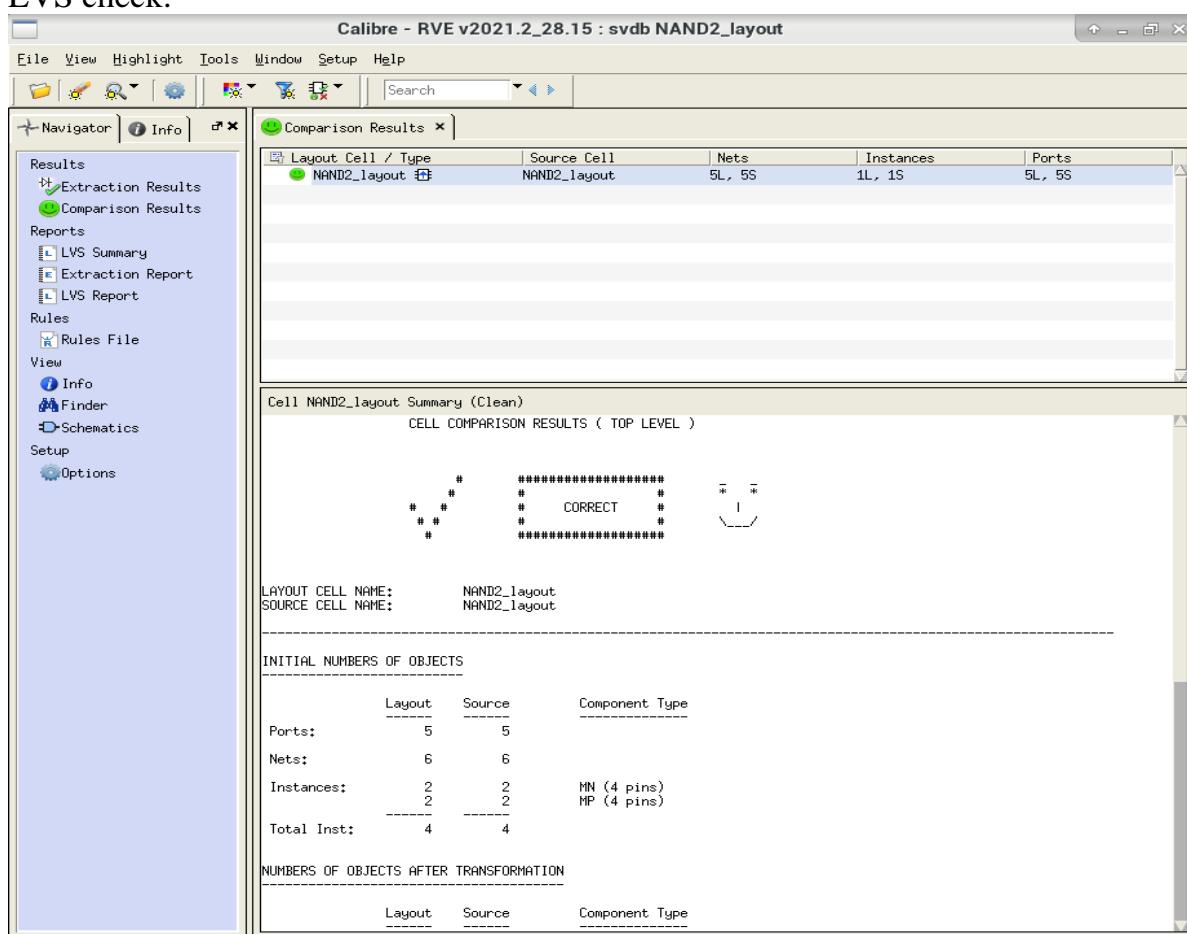
*Layout of NAND2*

DRC check:



The result of DRC

### LVS check:



The result of LVS

## NOR2 GATE:

### 1.7 Schematic

Input A	Input B	$0 = (A + B)'$
0	0	1
0	1	0
1	0	0
1	1	0

Table 1.7.1 : Truth table of NOR

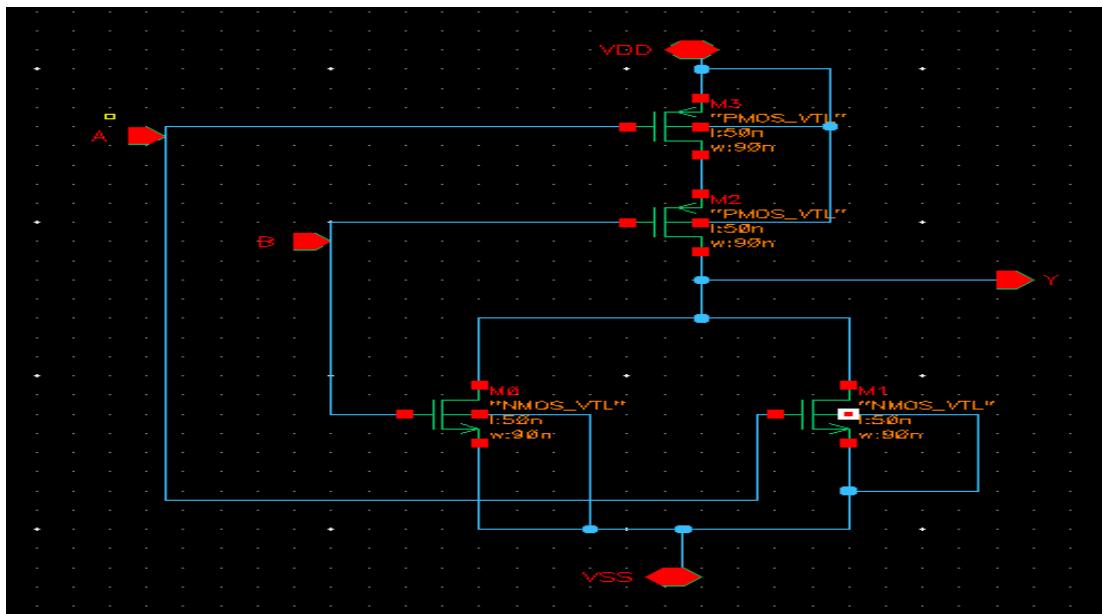


Figure 1.7.1: Schematic of NOR

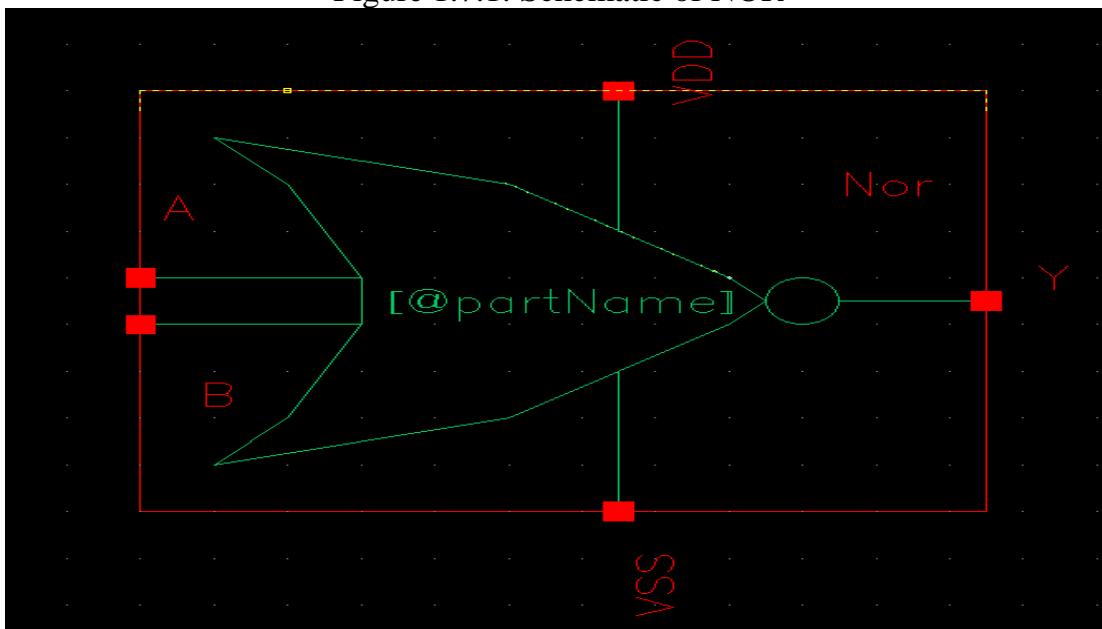


Figure 1.7.2: symbol of NOR

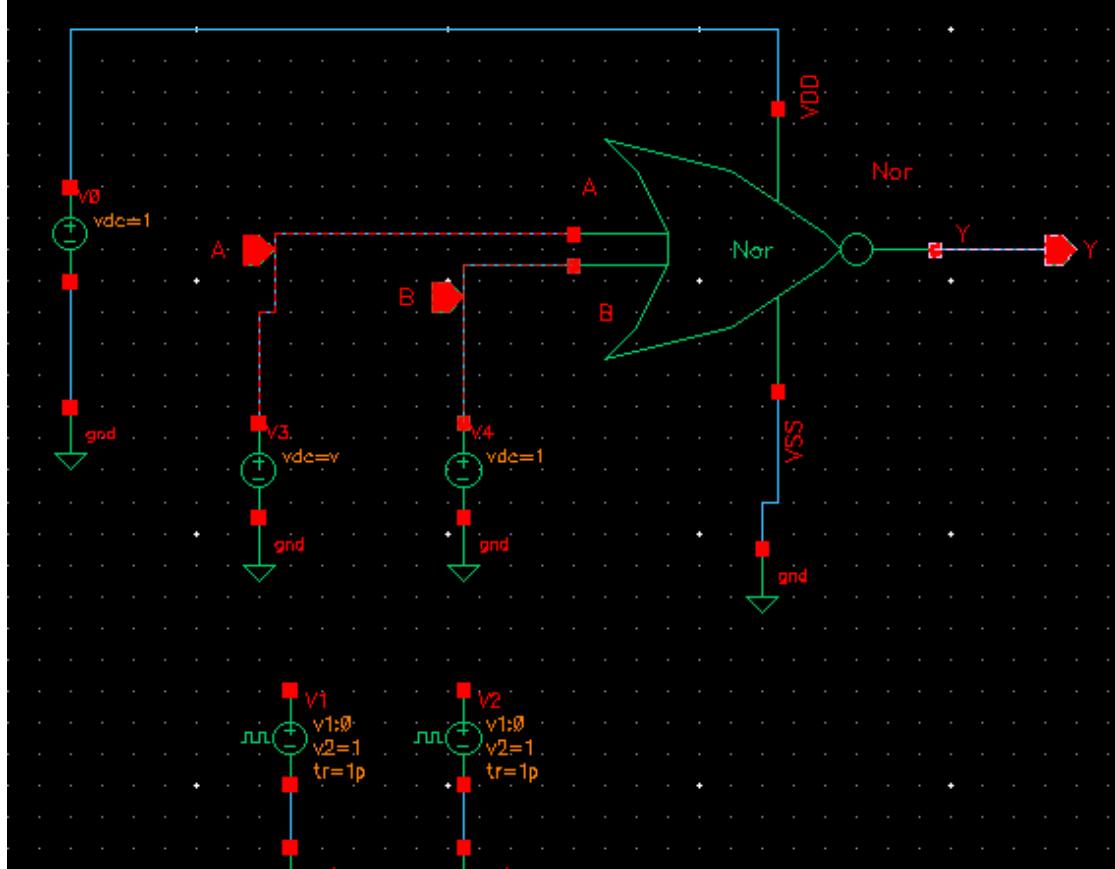


Figure 1.7.3 : Testbench of NOR

## 1.8 DC analysis Simulation

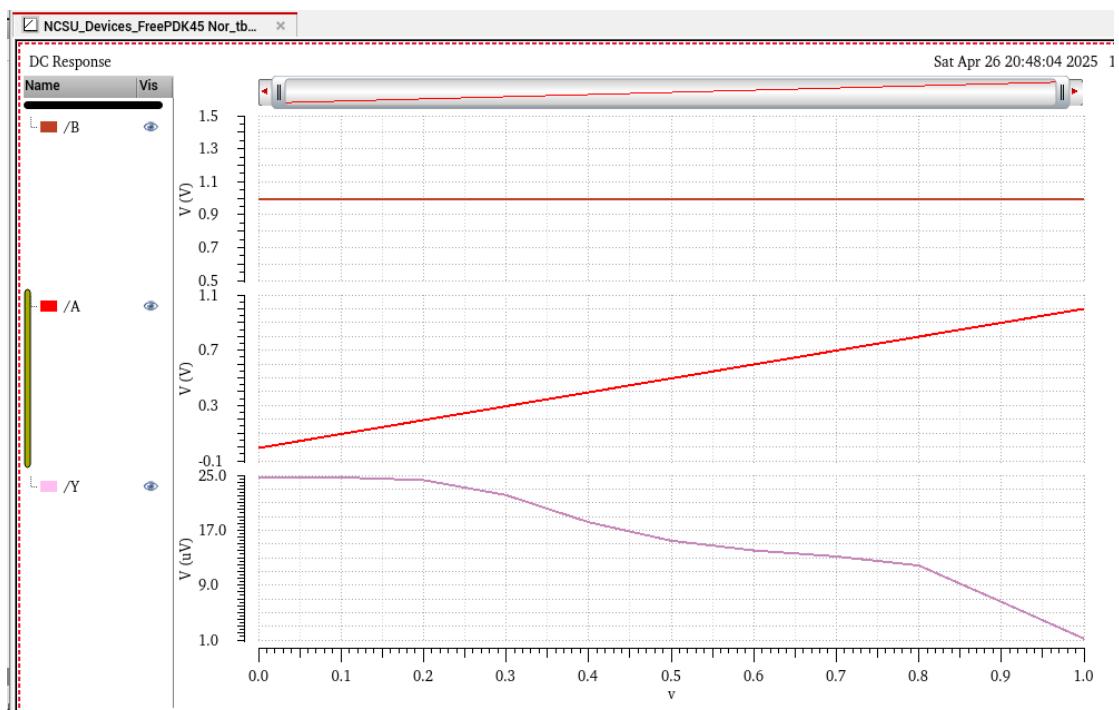


Figure 1.8.1 : A, B & Y DC analysis of EXOR2 when sweeping VA

## 1.9 Transient Analysis Simulation

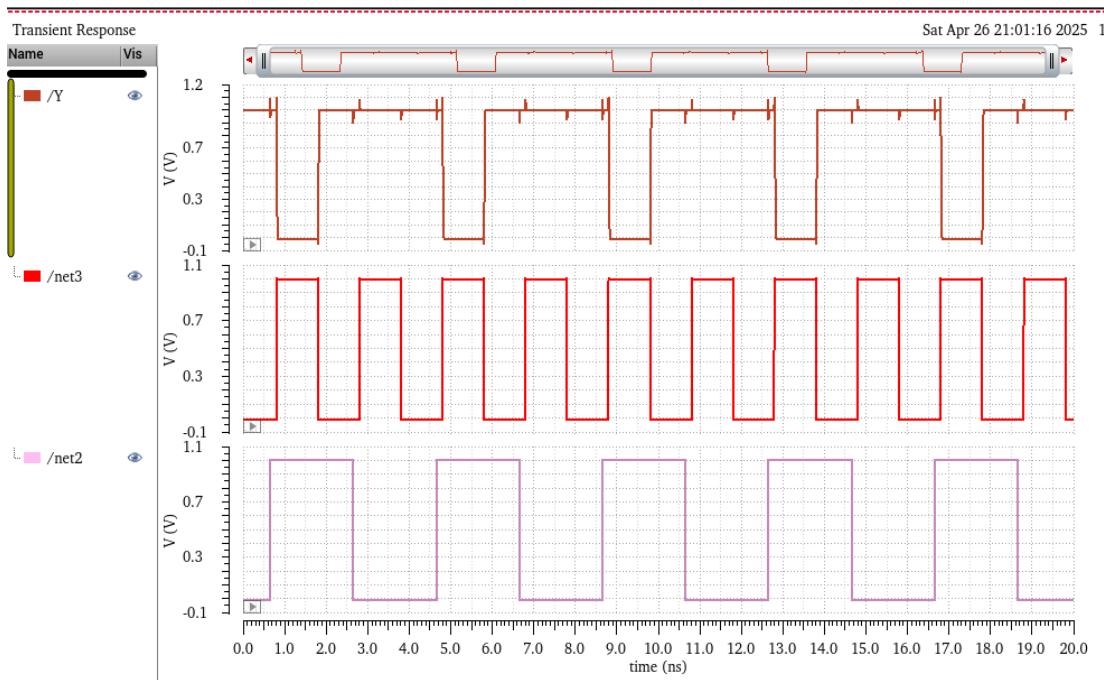
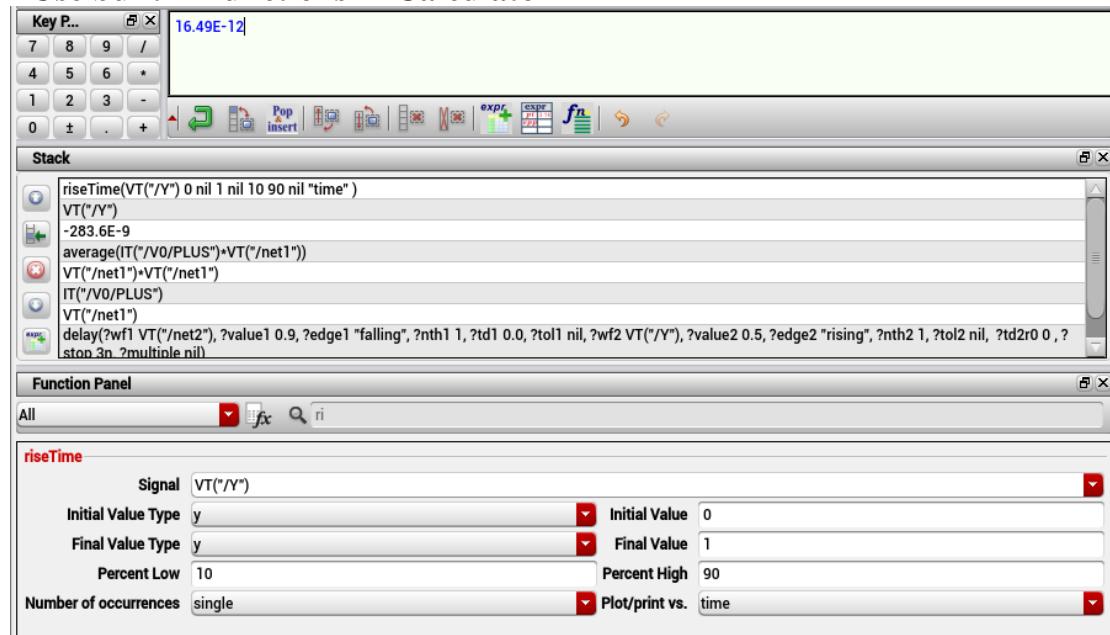


Figure 1.9.1 : Transient of XOR

### - Use built-in functions in Calculator



**Key P... 7.876E-12**

**Stack**

- fallTime(VT("/Y") 0 nil 1 nil 90 10 nil "time")
- VT("/Y")
- 16.49E-12
- riseTime(VT("/Y") 0 nil 1 nil 10 90 nil "time")
- VT("/Y")
- 283.6E-9
- average(IT("/V0/PLUS")+VT("/net1"))
- VT("/net1")\*VT("/net1")

**Function Panel**

**fallTime**

Signal	VT("/Y")
Initial Value Type	y
Final Value Type	y
Percent High	90
Percent Low	10
Number of occurrences	single
Plot/print vs.	time

**Key P... 12.59E-12**

**Stack**

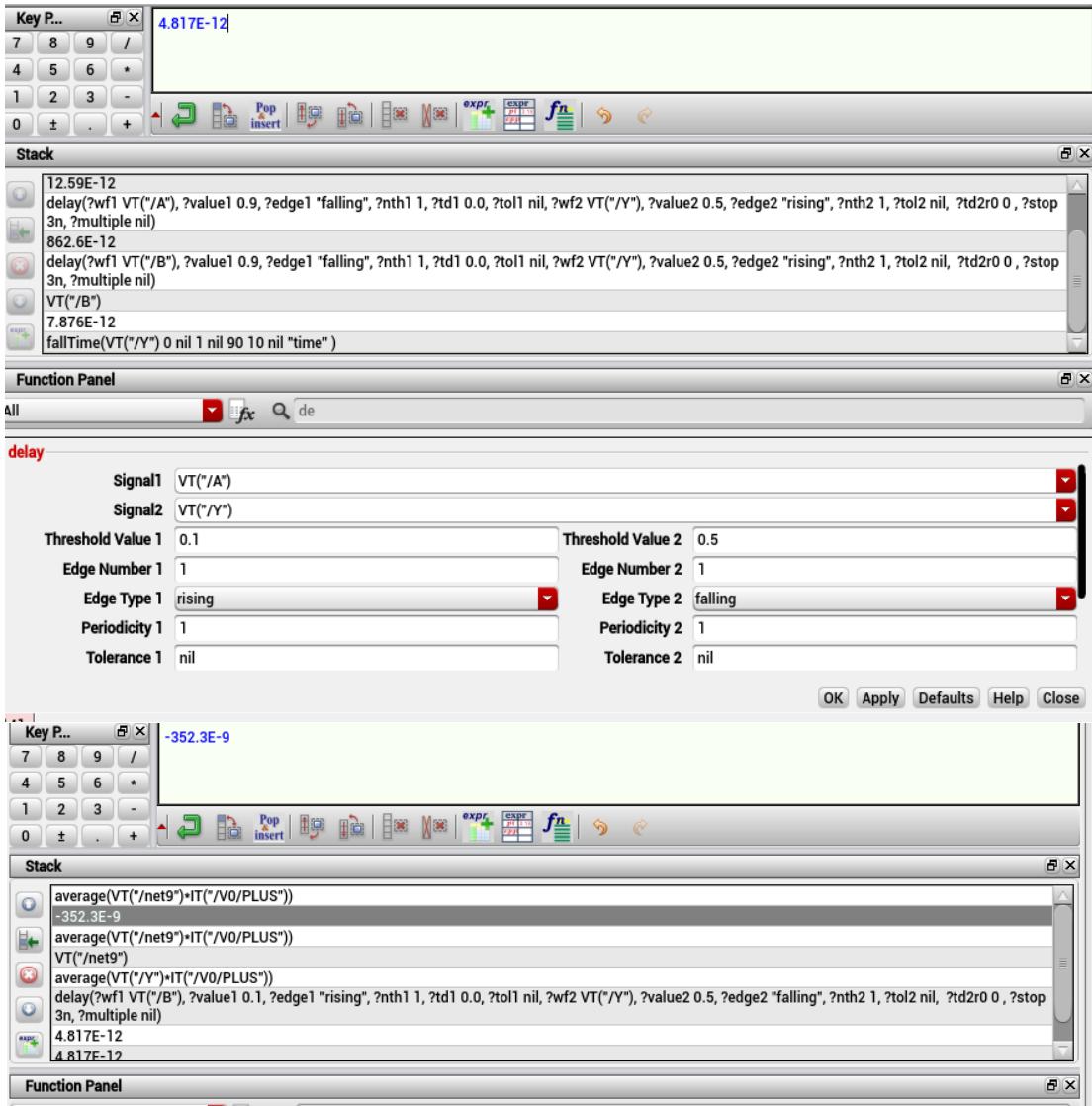
- 3n, ?multiple nil)
- 862.6E-12
- delay(?wf1 VT("/B"), ?value1 0.9, ?edge1 "falling", ?nth1 1, ?td1 0.0, ?tol1 nil, ?wf2 VT("/Y"), ?value2 0.5, ?edge2 "rising", ?nth2 1, ?tol2 nil, ?td2r0 0, ?stop 3n, ?multiple nil)
- VT("/B")
- 7.876E-12
- fallTime(VT("/Y") 0 nil 1 nil 90 10 nil "time")
- VT("/Y")
- 16.49E-12

**Function Panel**

**delay**

Signal1	VT("/A")
Signal2	VT("/Y")
Threshold Value 1	0.9
Edge Number 1	1
Edge Type 1	falling
Periodicity 1	1
Tolerance 1	nil
Threshold Value 2	0.5
Edge Number 2	1
Edge Type 2	rising
Periodicity 2	1
Tolerance 2	nil

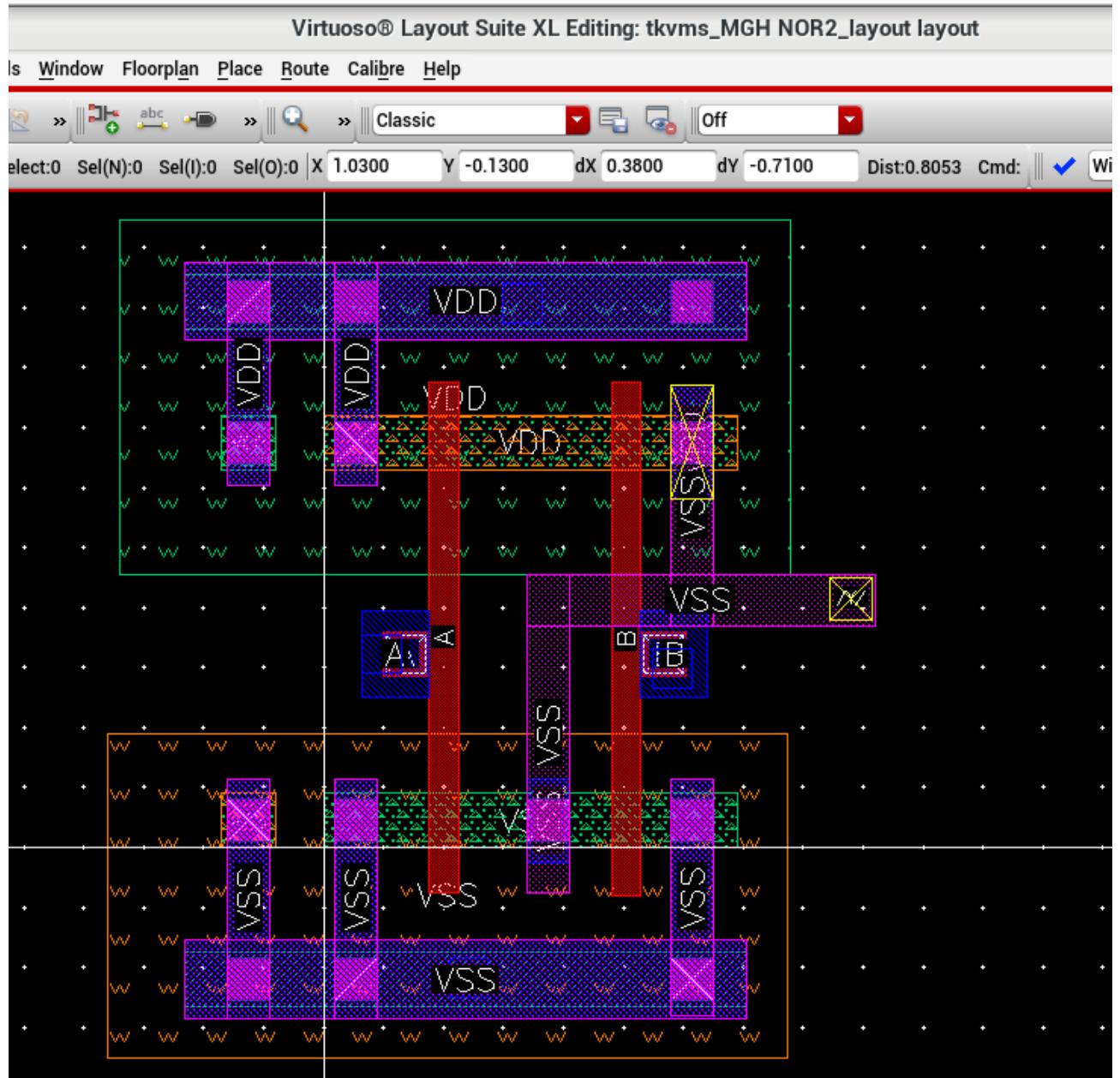
OK Apply Defaults Help Close



Parameters	Result
Rising time: (10%-90%)	16.49ps
Falling time: (90%-10%)	7.8ps
Rising propagation delay	12.59ps
Falling propagation delay	4.81ps
Average propagation delay	8.7ps
Power consumption	352.3nW

**Table 1.9.1: Measurement results of NOR**

- LAYOUT:



*Layout of NOR2*

## DRC:

The screenshot shows the Calibre DRC interface with the title "Calibre - RVE v2021.2\_28.15 : NOR2\_layout.drc.results". The menu bar includes File, View, Highlight, Tools, Window, Setup, and Help. The toolbar contains icons for file operations, search, and zoom. A search bar is present at the top right. The main window has a tree view on the left labeled "Check / Cell" with items like "Check Well.1", "Check Well.2", etc., all marked as "0". Below the tree is a large empty text area. At the bottom, a status bar displays "Rule File Pathname: /home/admin/Documents/virtuoso/\_calibreDRC.rul" and "Nwell and Pwell must not overlap".

*The result of DRC*

## LVS:

The screenshot shows the Calibre LVS interface with the title "Calibre - RVE v2021.2\_28.15 : svdb NOR2\_layout". The menu bar and toolbar are similar to the DRC interface. The left sidebar includes sections for Results (Extraction Results, Comparison Results), Reports (LVS Summary, Extraction Report, LVS Report), Rules (Rules File), View (Info, Finder, Schematics), and Setup (Options). The main area features a "Comparison Results" tab with a table showing one entry: "Layout Cell / Type" is NOR2\_layout, "Source Cell" is NOR2\_layout, "Nets" are 5L, 5S, "Instances" are 1L, 1S, and "Ports" are 5L, 5S. Below this is a "Cell NOR2\_layout Summary (Clean)" section with a "CELL COMPARISON RESULTS ( TOP LEVEL )" table:

Layout Cell Name	Source Cell Name	Net Count	Instance Count	Port Count
NOR2_layout	NOR2_layout	5L, 5S	1L, 1S	5L, 5S

Below the table is a graphical representation of layout objects using symbols like '#', '=', '|', and '/'. The summary also includes "INITIAL NUMBERS OF OBJECTS" tables:

	Layout	Source	Component	Type
Ports:	5	5		
Nets:	6	6		

*The result of LVS*

## EXOR2:

### 1.10 Schematic

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Table 1.10.1: Truth table of EXOR2

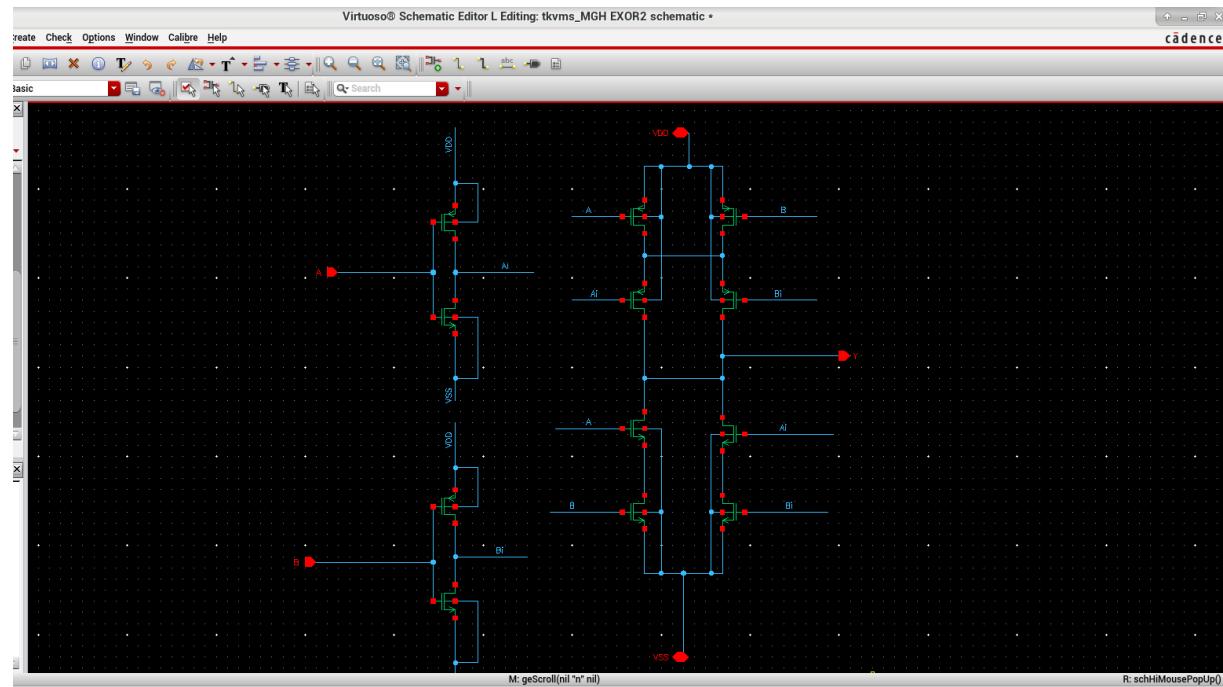


Figure 1.10.1 : Schematic of EXOR2

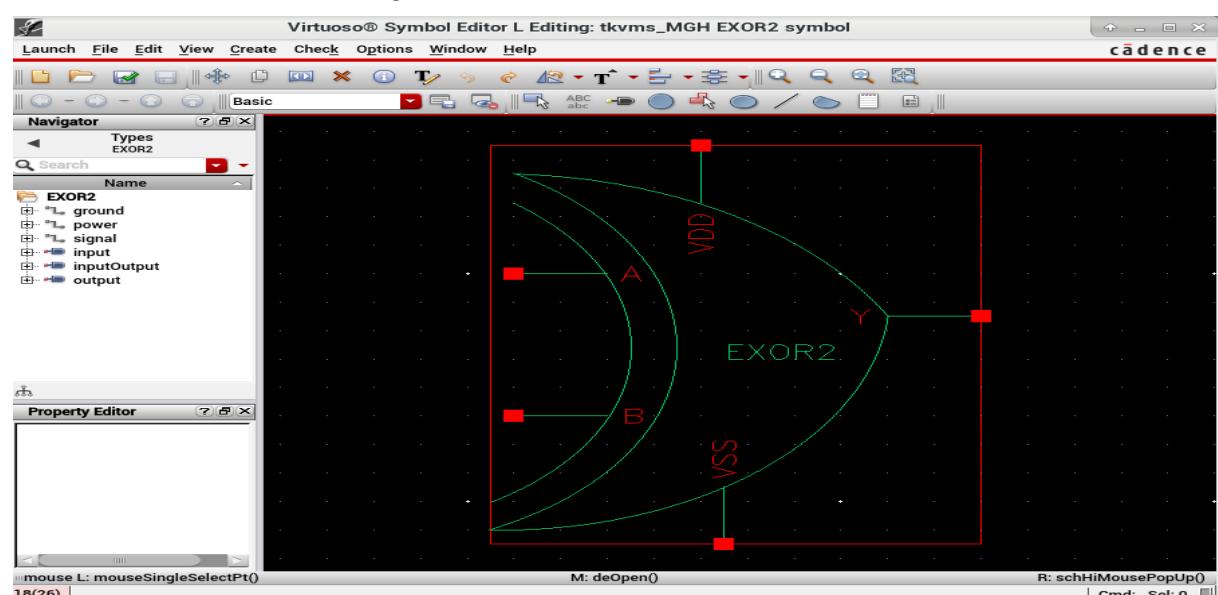


Figure 1.10.2: symbol of EXOR2

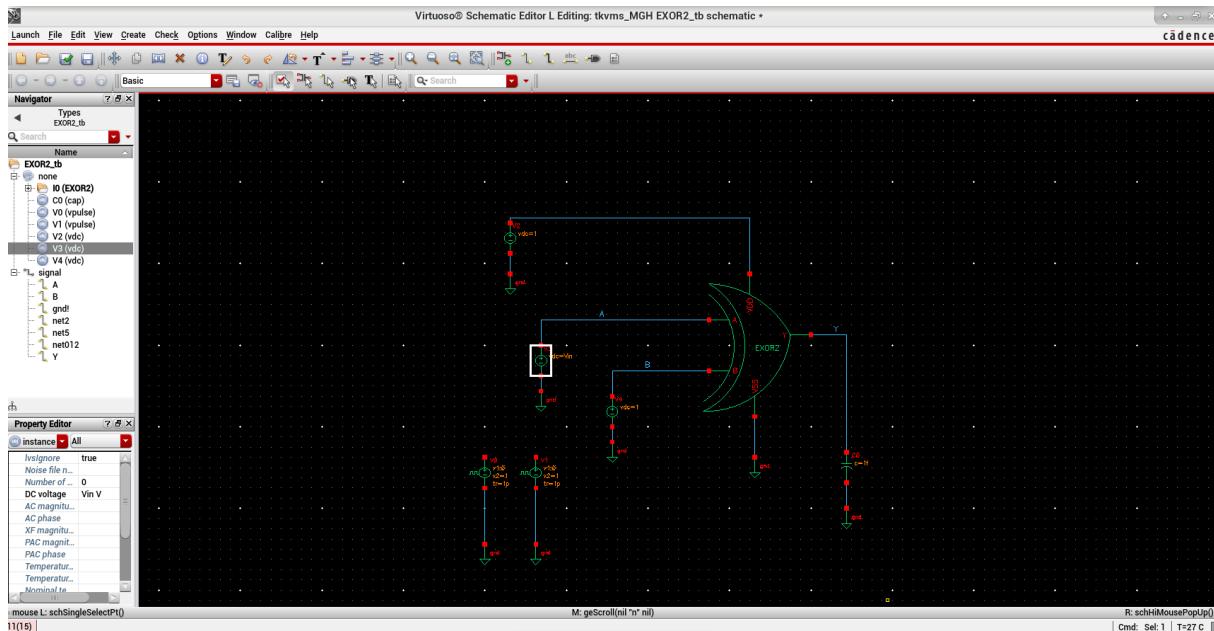


Figure 1.10.3 : Testbench of EXOR2

## 1.11 DC analysis Simulation

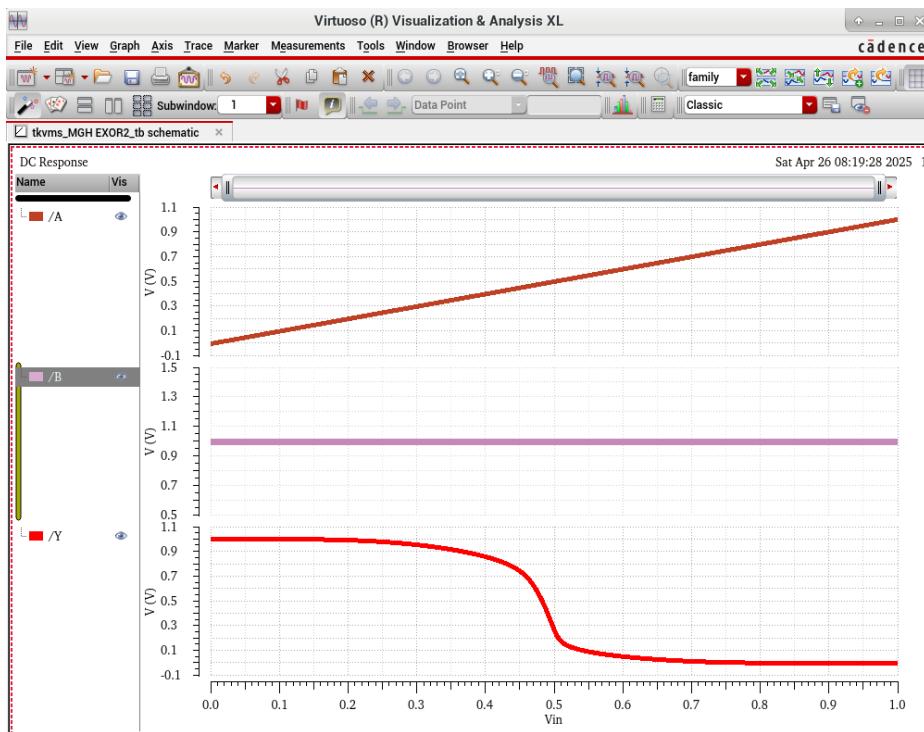


Figure 1.11.1: A, B & Y DC analysis of EXOR2 when sweeping  $V_A$

## 1.12 Transient Analysis Simulation

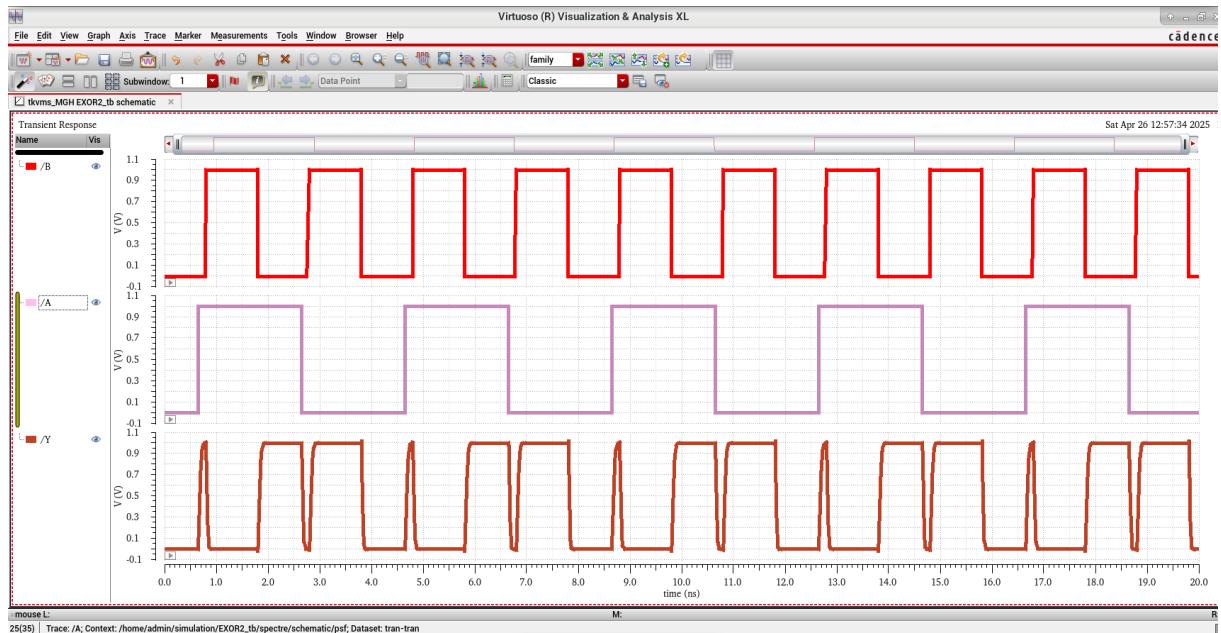


Figure 1.12.1 : Transient of Exor2

Parameter	result
$t_{pdr}$ – Rising Propagation Delay (90% - 50%)	31.54 ps
$t_{pdf}$ – Falling Propagation Delay (10% - 50%)	22.01 ps
$t_{pd}$ – Average Propagation Delay	26.775ps
Power consumption	18.81 uW
$t_{rise}$	58.55ps
$t_{fall}$	39.88ps

Table 1.12.1: Measurement results of EXOR2

### 1.13 Layout:

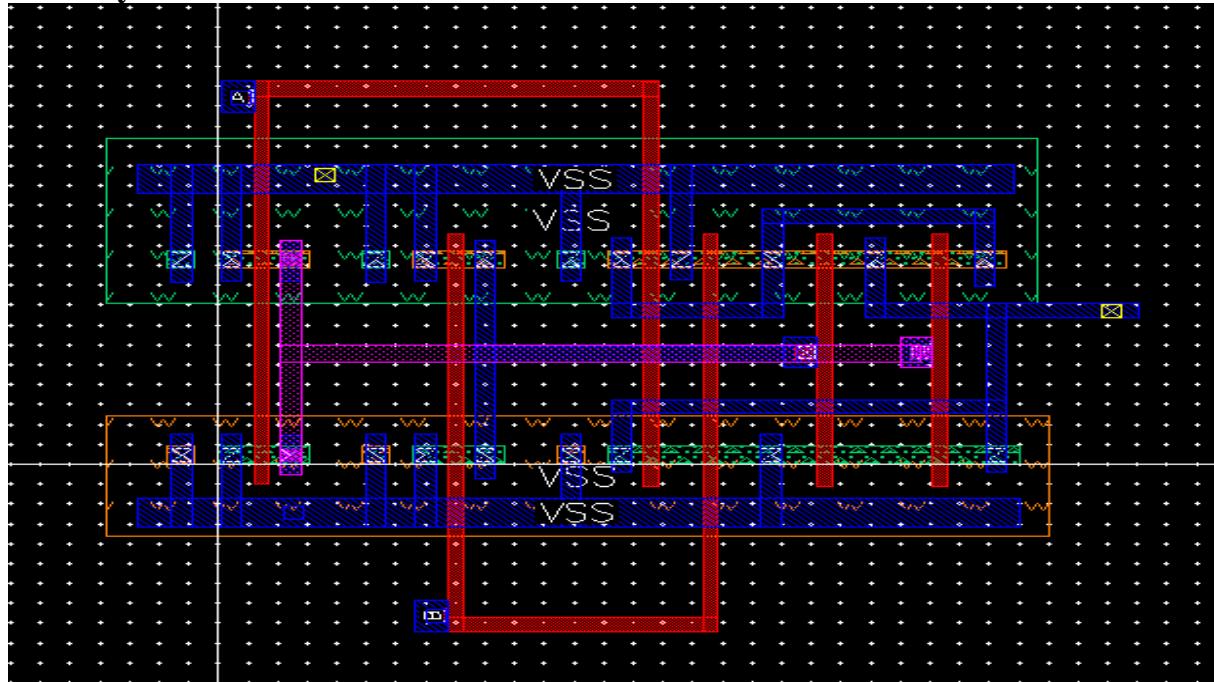


Figure 1.13.1: layout of EXOR2

## DRC check:

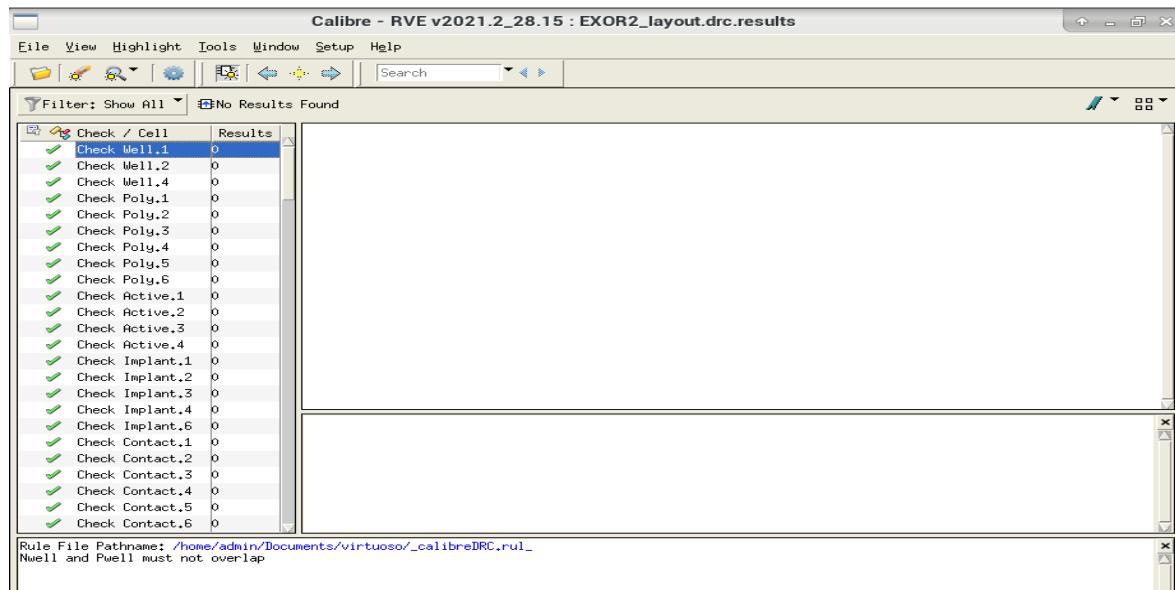


Figure 1.13.2 : DRC result of EXOR2 layout

## LVS check:

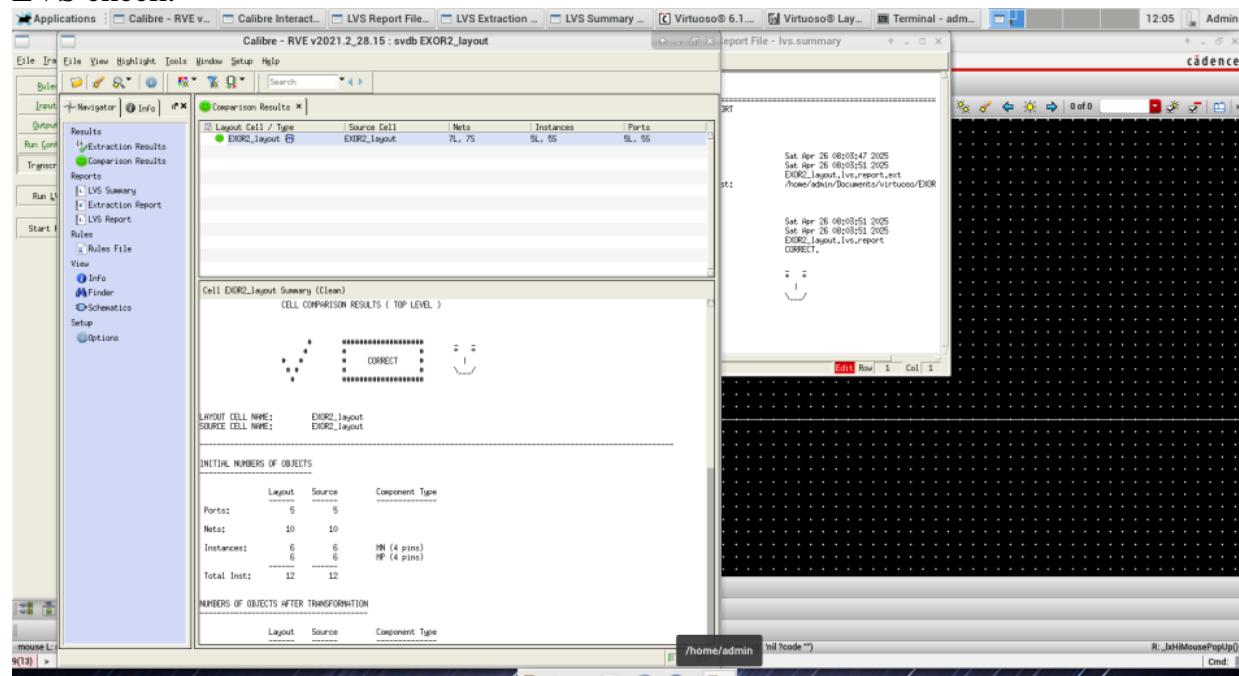


Figure 1.13.3: LVS check result of EXOR2 layout

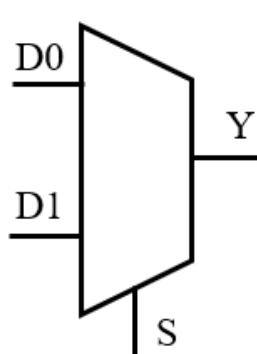
## 2. EXPERIMENT 2

**Objective:** Implement Basic CMOS Combinational Components.

**Requirements:**

- Complete the truth table, schematic, and symbol for a 2-to-1 channel multiplexer using compound gate.
- Run DC analysis and transient simulation.
- Create layouts for each logic gate, then show DRC confirmation and the corresponding schematic with proof of LVS.

**2.1 Truth table, schematic, and symbol for a 2-to-1 channel multiplexer using compound gate:**



Truth table of MUX 2-to-1:

S	D0	D1	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

- Draw the schematic of the compound gate for a 2-to-1 MUX:

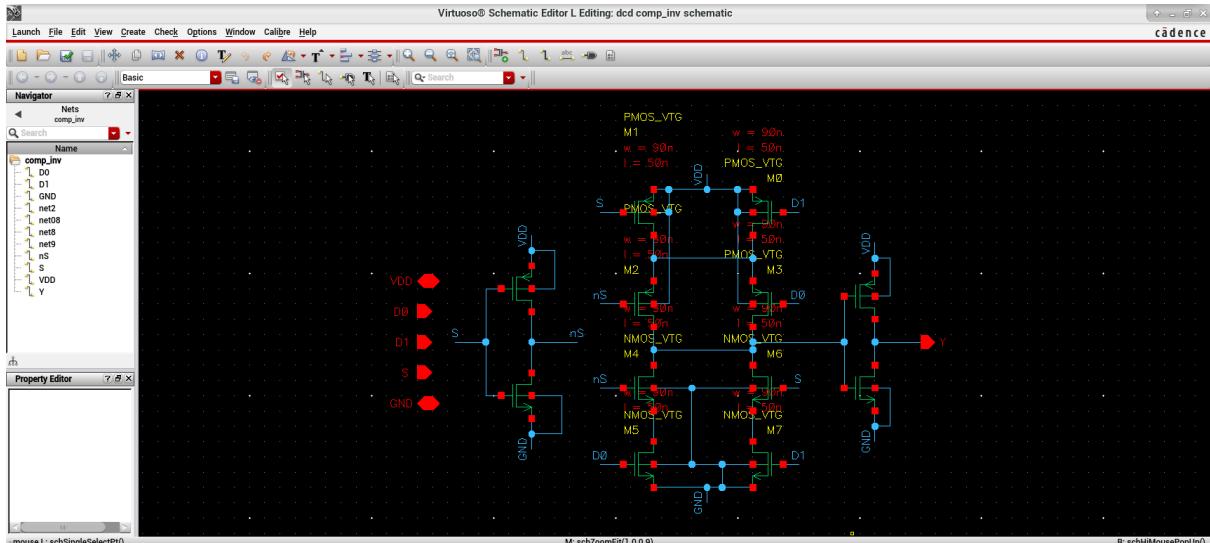


Figure 2.1: Schematic's MUX 2-to-1

- Create MUX 2-to-1's symbol:

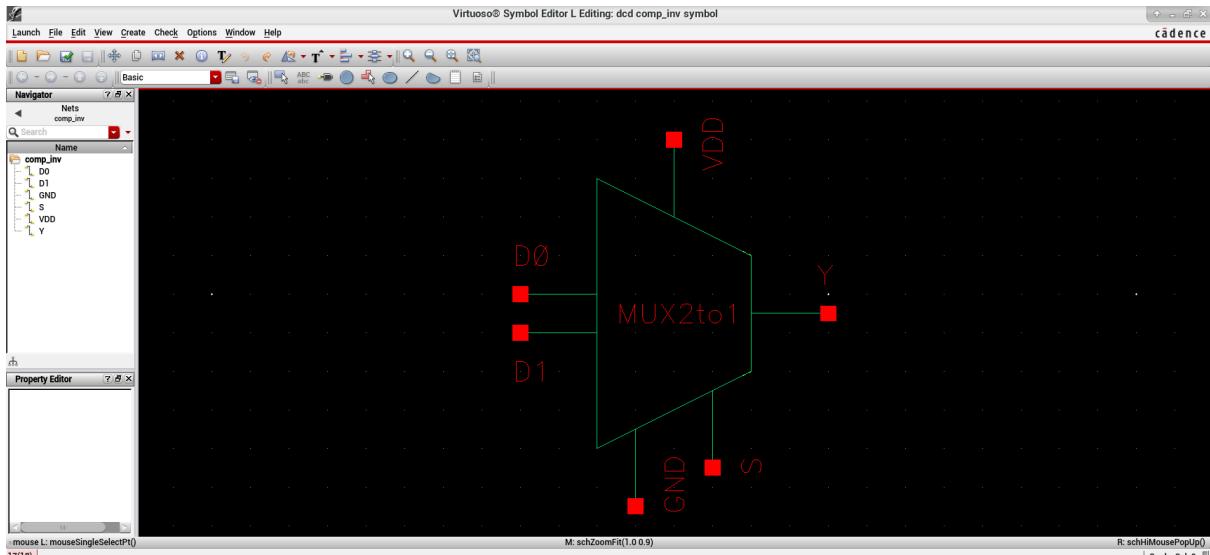


Figure 2.2: Symbol of MUX 2-to1

## 2.2 Simulated and Measured Parameters:

- Provide power to the signals for simulation purposes:

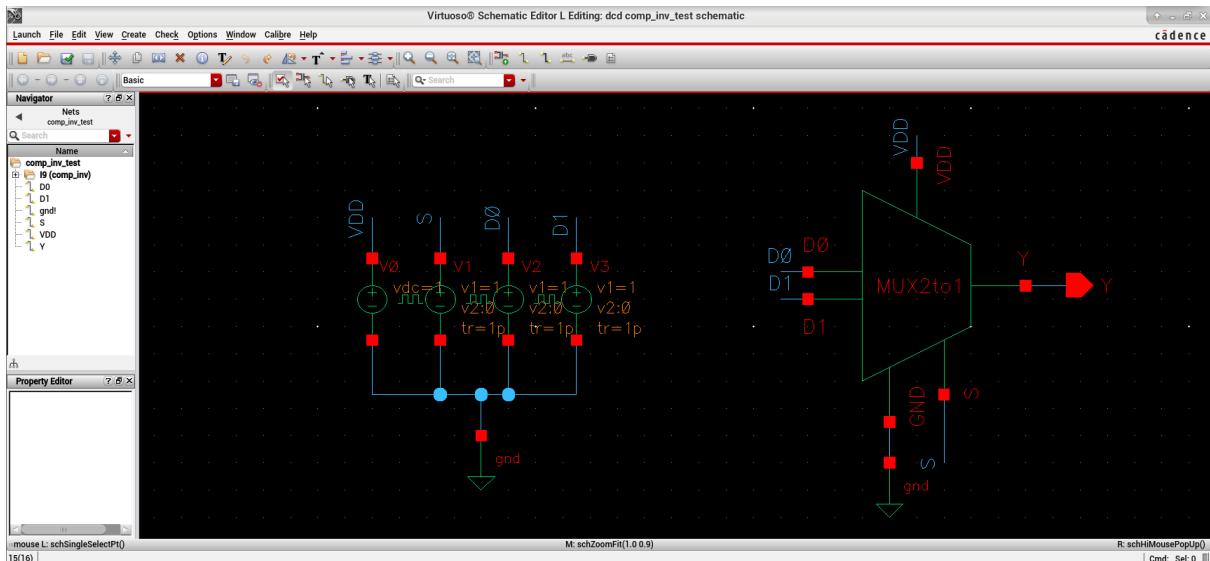
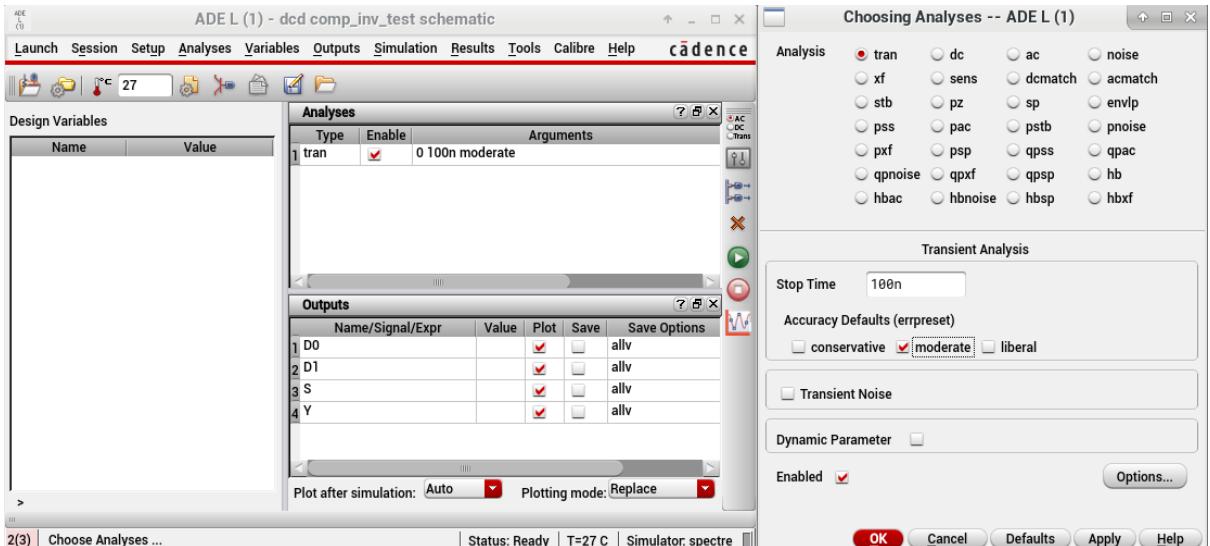


Figure 2.3: MUX 2-to-1's testbench

- Configure values to generate graphs of input and output signals:



- Simulation Results:

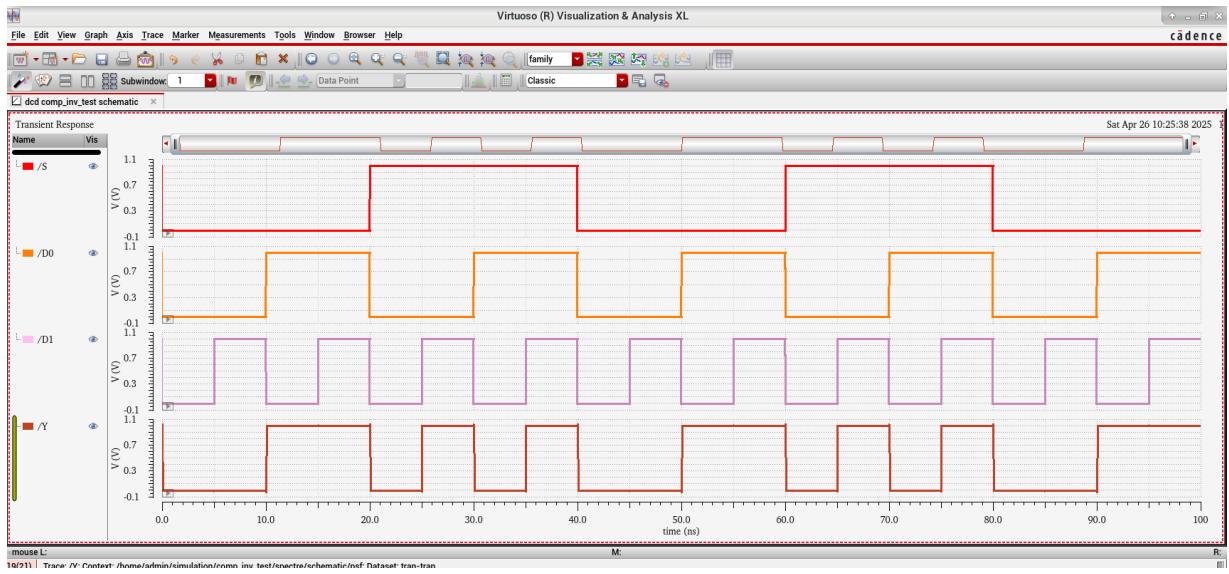


Figure 2.4: Waveform of MUX 2-to-1

=> This CMOS structure correctly performs the function of a 2-to-1 MUX.

#### - Measured parameters:

+ Based on the simulation waveform results using the calculator tool:

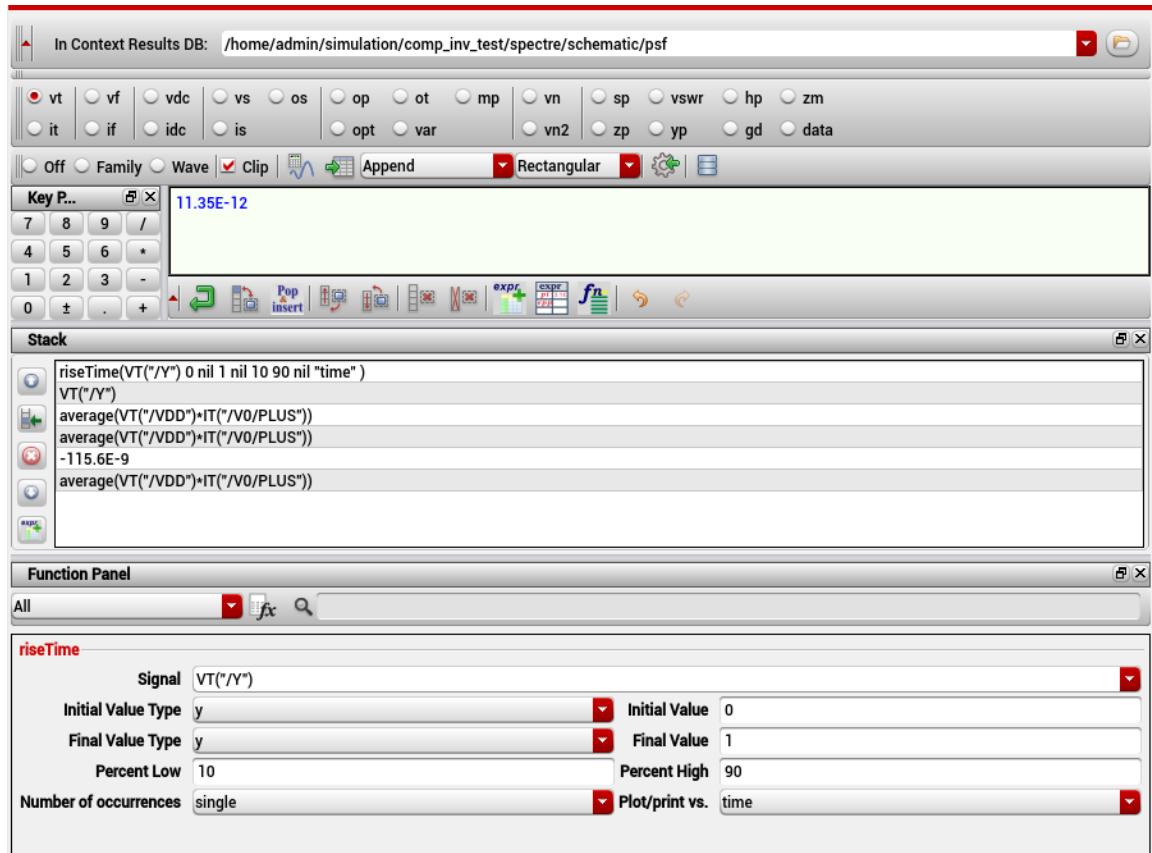


Figure 2.5: The result of total rising time using Calculator

=>  $t_r = 11.35 \text{ (ps)}$ .

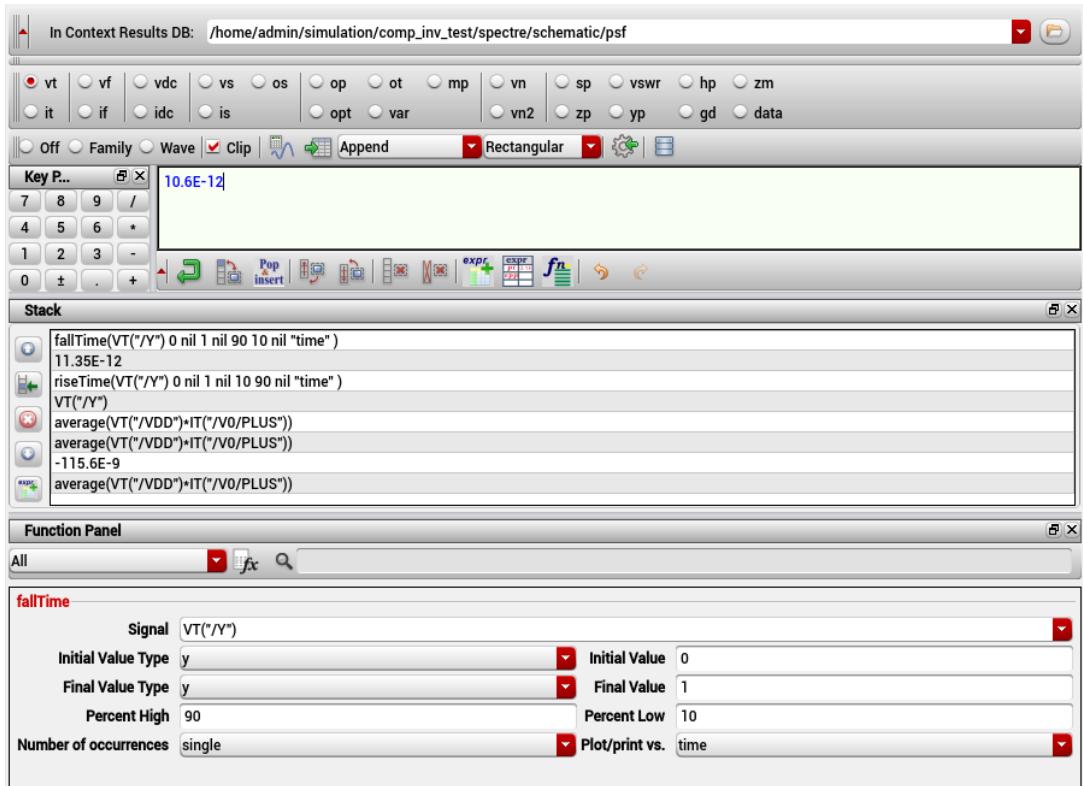


Figure 2.6: The result of falling time using Calculator

$$\Rightarrow t_f = 10.6 \text{ } (\mu\text{s}).$$

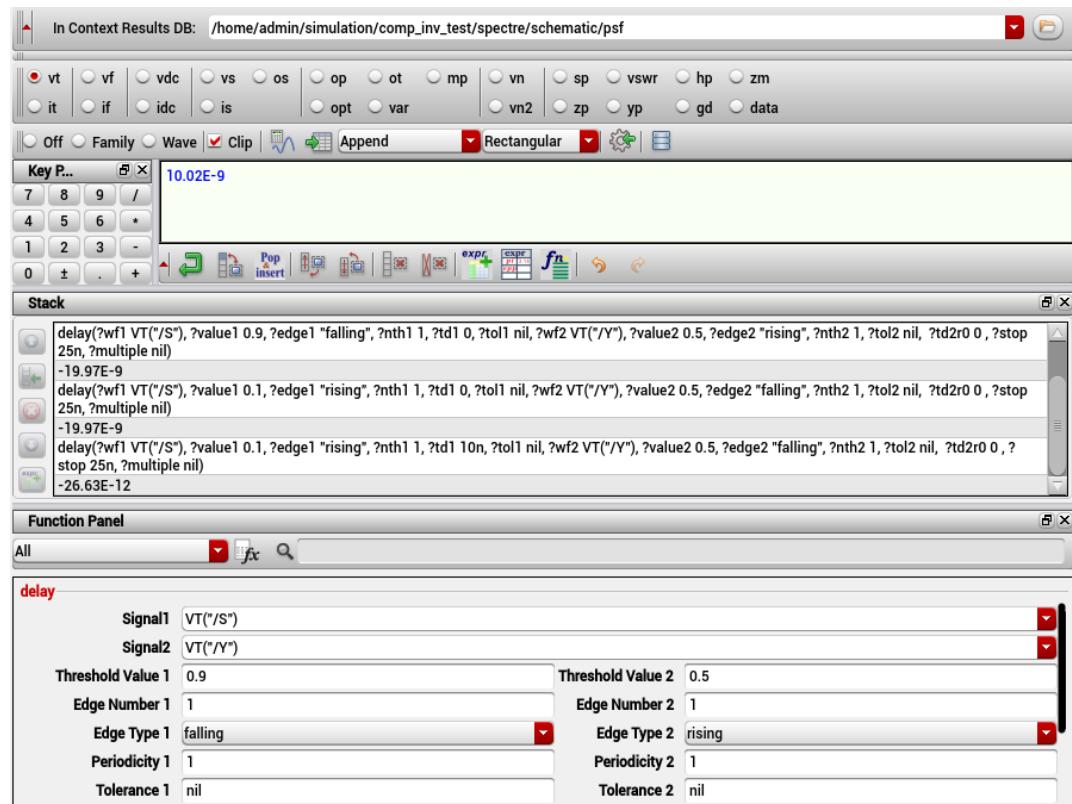


Figure 2.7: The result of rising propagation delay using Calculator

$$\Rightarrow t_{pdr} = 10.02 \text{ (ns).}$$

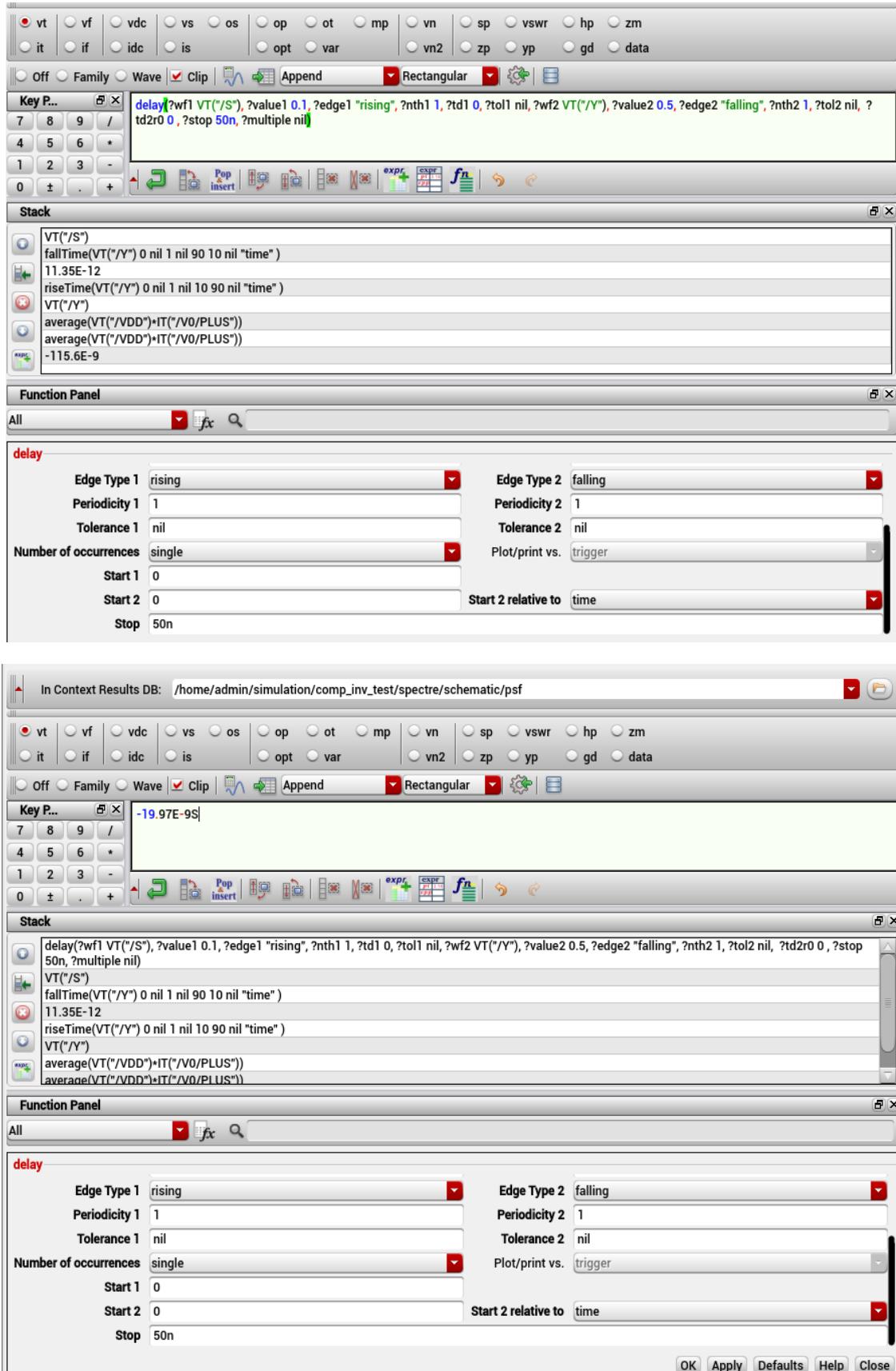


Figure 2.8+2.9: The result of falling propagation delay using Calculator

$$\Rightarrow t_{pdf} = 19.97 \text{ (ns).}$$

**- Power consumption:**

+ Static power based on NMOS – when  $V_{in} = 1$ :

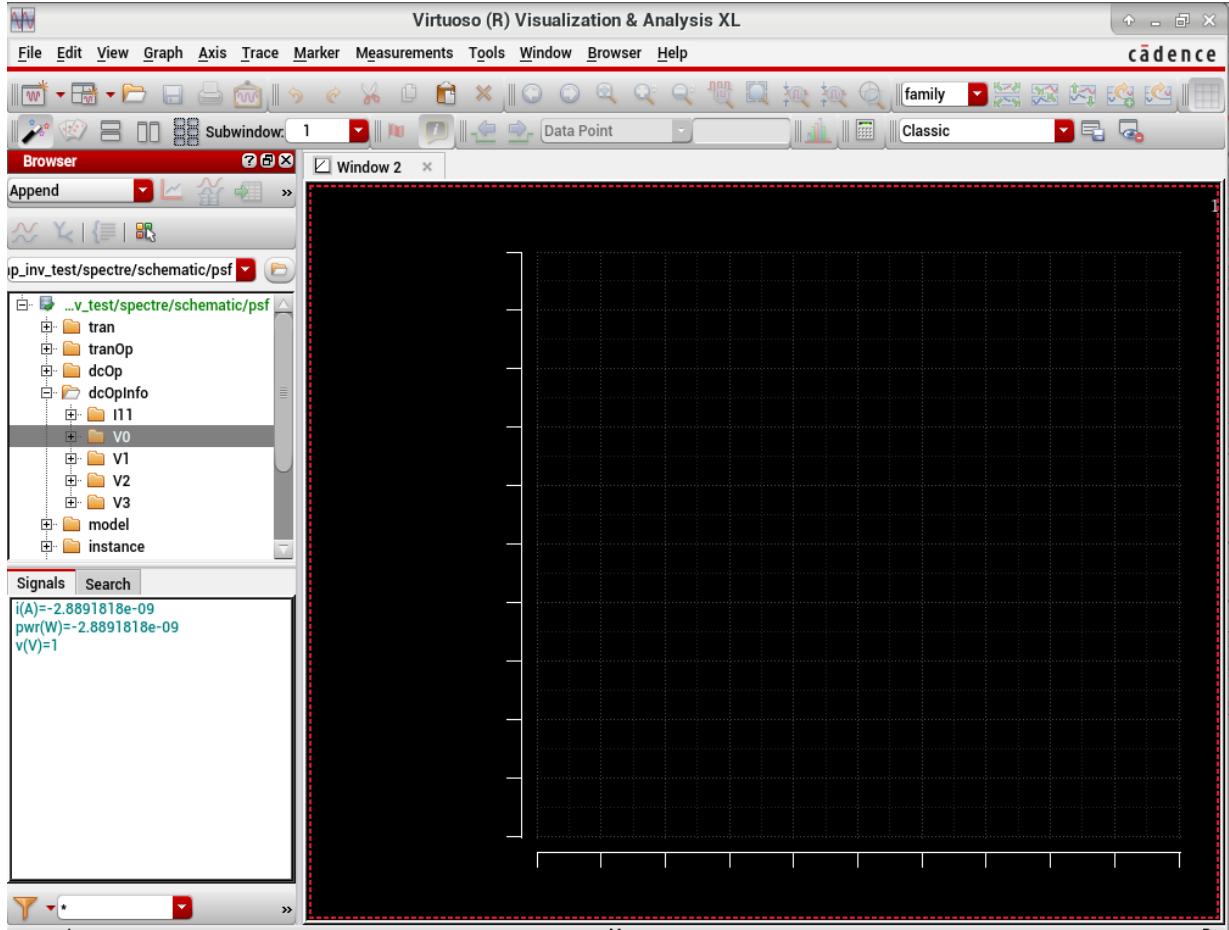


Figure 2.10: The result of static power based on NMOS

$$\Rightarrow P_{static} = 2.8892 \text{ nW.}$$

+ Static power based on PMOS – when  $V_{in} = 0$ .

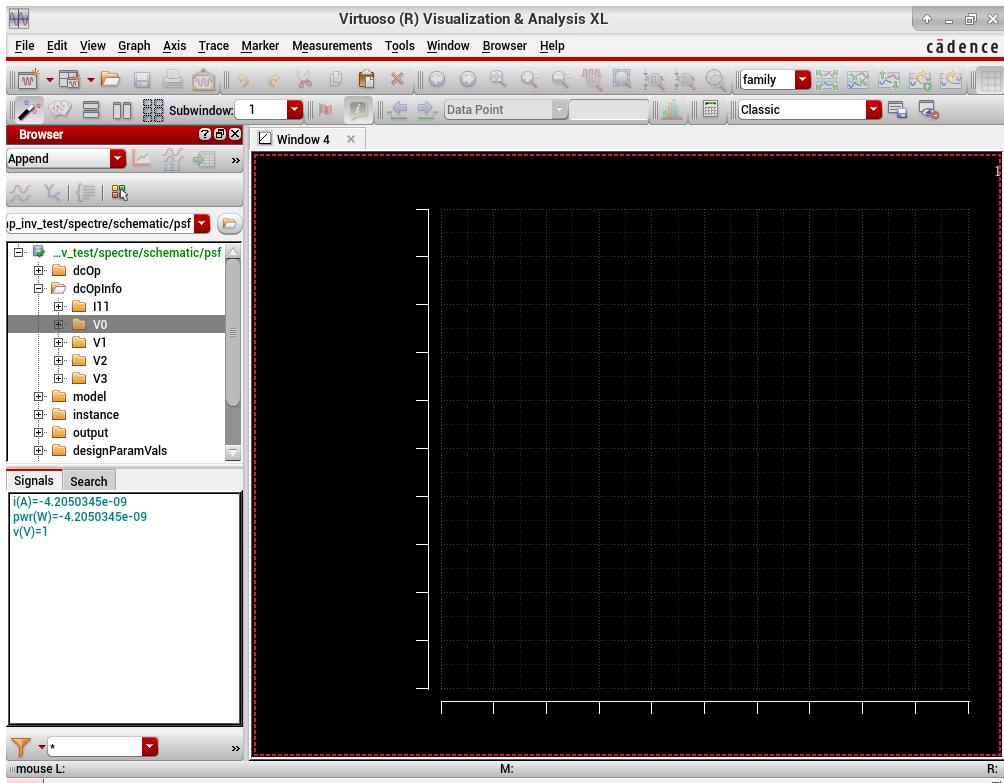
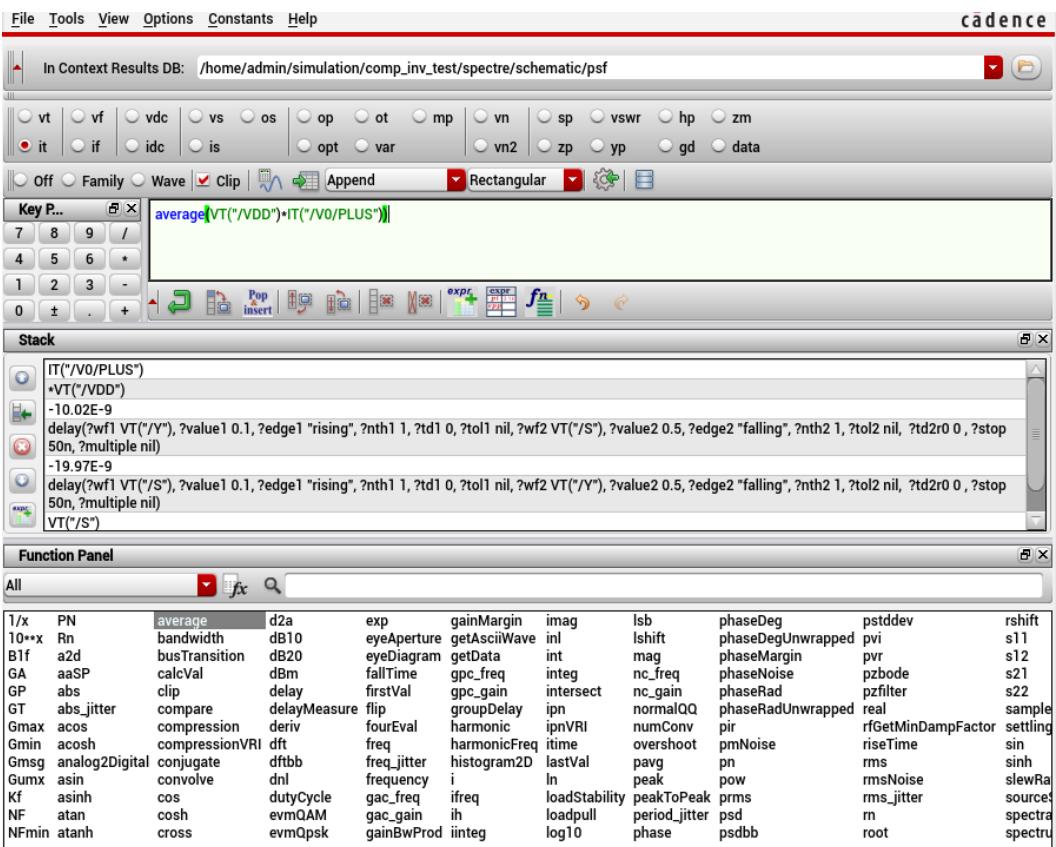


Figure 2.11: The result of static power based on PMOS

$$\Rightarrow P_{static} = 4.2050 \text{ nW.}$$

- Total power measurement:



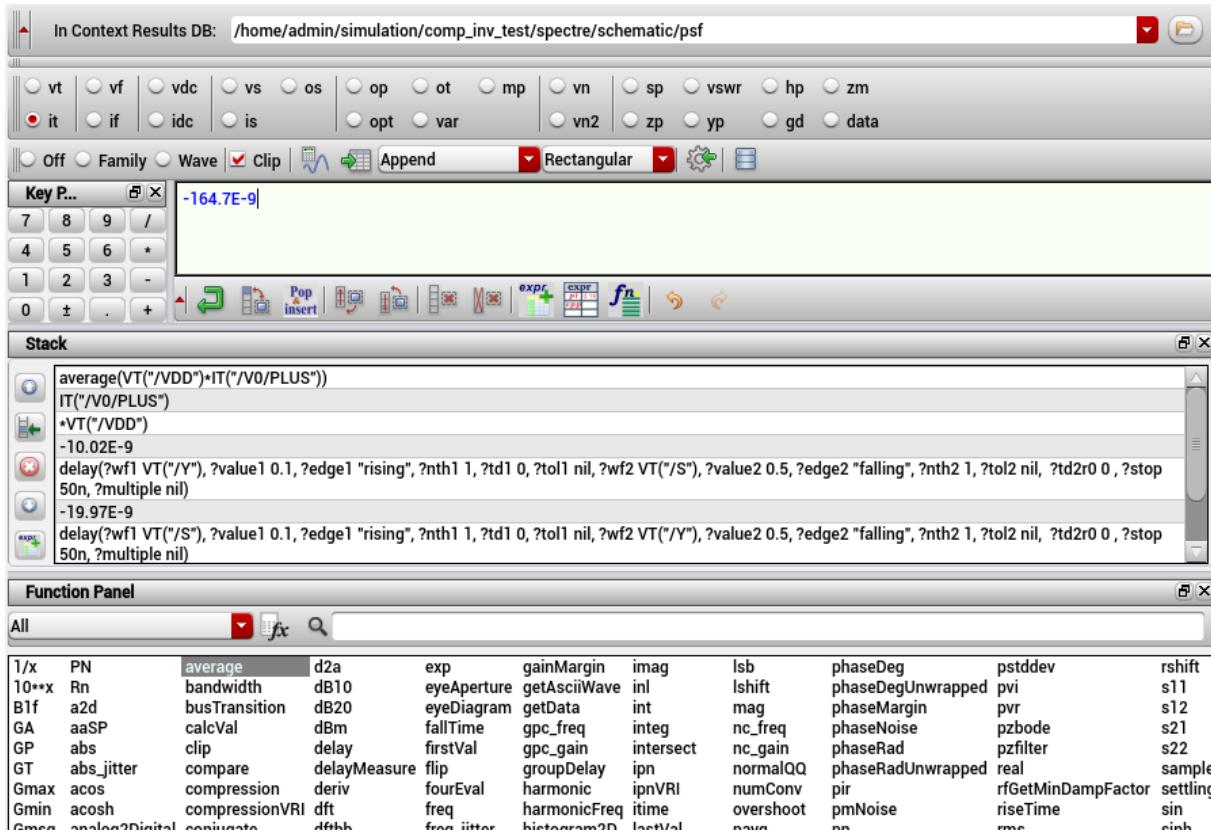


Figure 2.12+2.13: The result of total power consumption using Calculator

$$\Rightarrow P_{total} = 164.7 \text{ (nW)}.$$

- Measurement results of MUX 2-to-1:

Parameters	Result
$t_{rise}$ – Rising time (10% – 90%)	11.35 ( $\mu s$ )
$t_{fall}$ – Falling time (90% – 10%)	10.6 ( $\mu s$ )
$t_{pdr}$ – Rising propagation delay (90% – 50%)	10.02 ( $ns$ )
$t_{pdf}$ – Falling propagation delay (10% – 50%)	19.97 ( $ns$ )
$t_{pd}$ – Average propagation delay (50% - 50%)	14.995 ( $ns$ )
Power consumption	164.7 (nW)

$$(t_{pd} = \frac{t_{pdr} + t_{pdf}}{2} = 14.995 \text{ (ns)})$$

## 2.3 The layout of MUX 2-to-1 ‘s schematic:

The MUX 2-to-1 ‘s schematic:

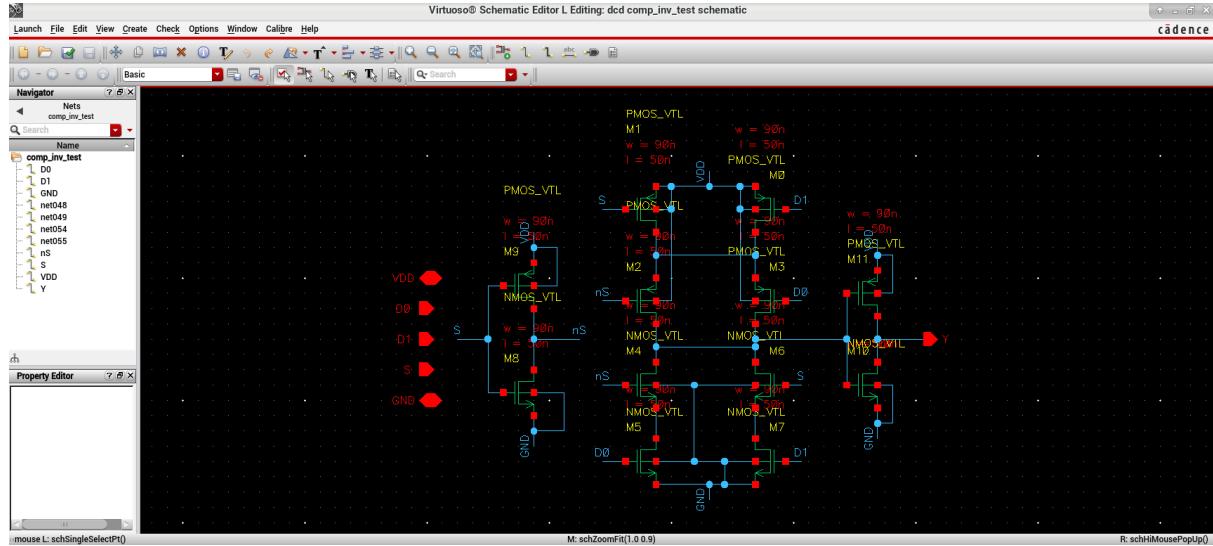


Figure 2.14: MUX 2-to-1 ‘s schematic

Layout of MUX 2-to-1 ‘s schematic:

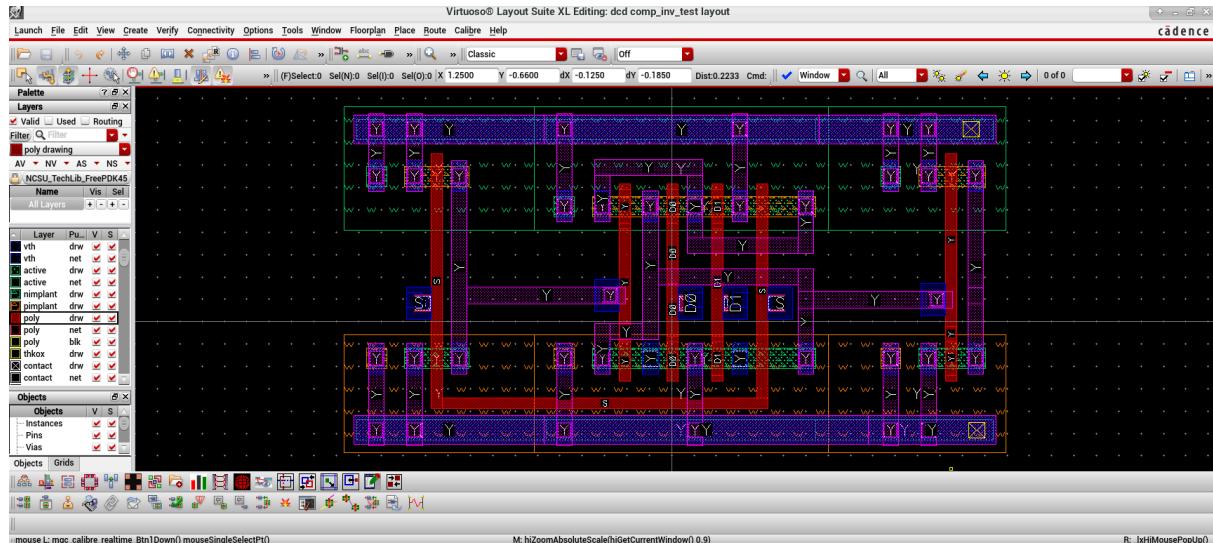


Figure 2.15: Layout of MUX 2-to-1

- Check DRC of layout:

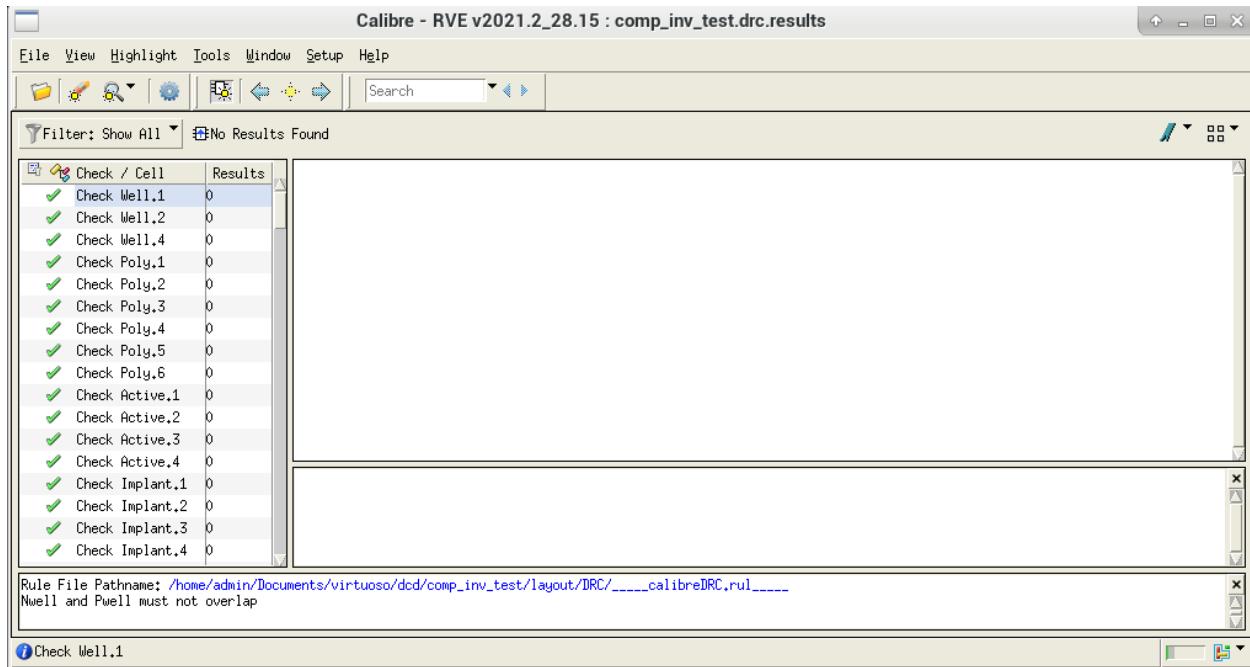


Figure 2.16: The result of DRC

=> PASS DRC

- Check LVS of layout:

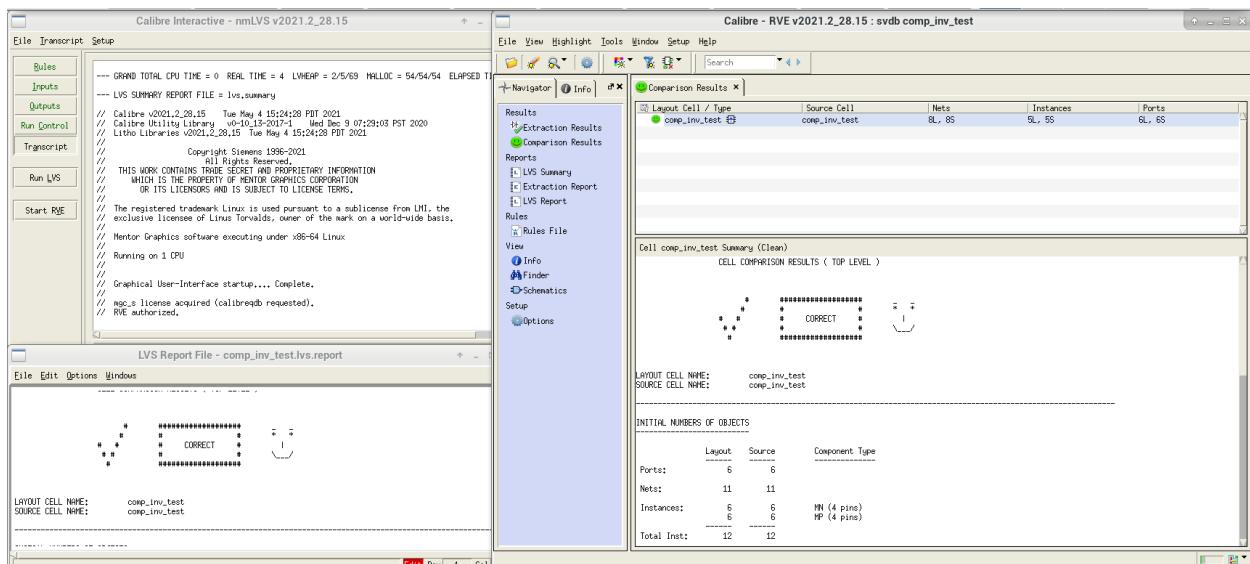


Figure 2.17: The result of LVS

=> PASS LVS.

### 3. EXPERIMENT 3

**Objective:** Implement simple storage elements - single-positive-edge-triggered Modified TSPC D flipflop.

**Requirements:**

- Demonstrate latch and flip-flop by studying a D latch and a D flip-flop using transmission gates.
- Complete the truth table, schematic, and symbol for each component, then run the transient simulation.
- Known definitions and how to measure setup time, propagation, and hold time.
- Find the clock frequency of this element.

A sequential logic circuit depends on the rising or falling edge of the single clock signal (CLK), its purpose is to capture and record the data input signal (D). The clock (CLK), data input (D), and output (Q) are commonly comprised in the truth table of a TSPC D flip-flop. As we have known that the output signal takes the value of the input Q only when the clock transition (rising or falling edge, depending on the design). Q stays in its prior state for the reverse case.

NMOS and PMOS are stacked in a Modified TSPC D flip-flop circuit to provide two or more stages of dynamic logic, while later stages employ additional transistors to transport and store the data, the commencing stage typically utilize an NMOS managed by the clock to sample the data input. Optimizing the transistor configuration in TSPC flip-flop is usually necessary to save power consumption, reduce propagation delay. The table below illustrate the truth table of a TSPC D flip flop:

Preset	D	CLK	Q
0	0	1	1
0	1	0	1
0	1	1	1
0	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1
1	0	0	0

Table 3.1: TSPC D Flip-flop Truth table

### 3.1 Schematic of the positive-edge-triggered TSPC D flip-flop:

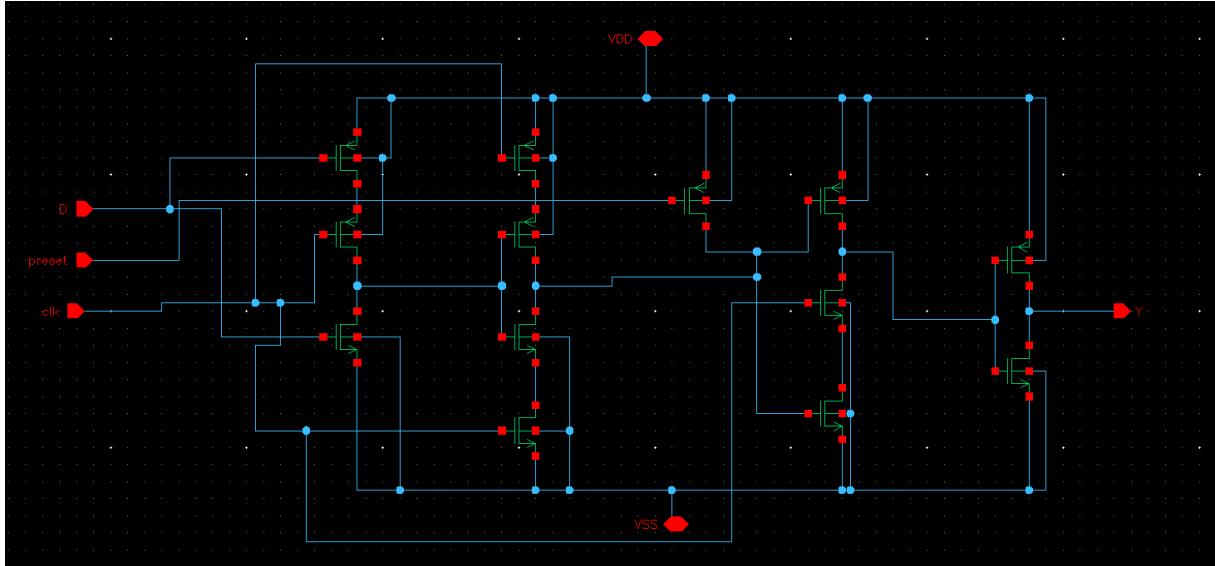


Figure 3.1: Schematic of TSPC D flip-flop

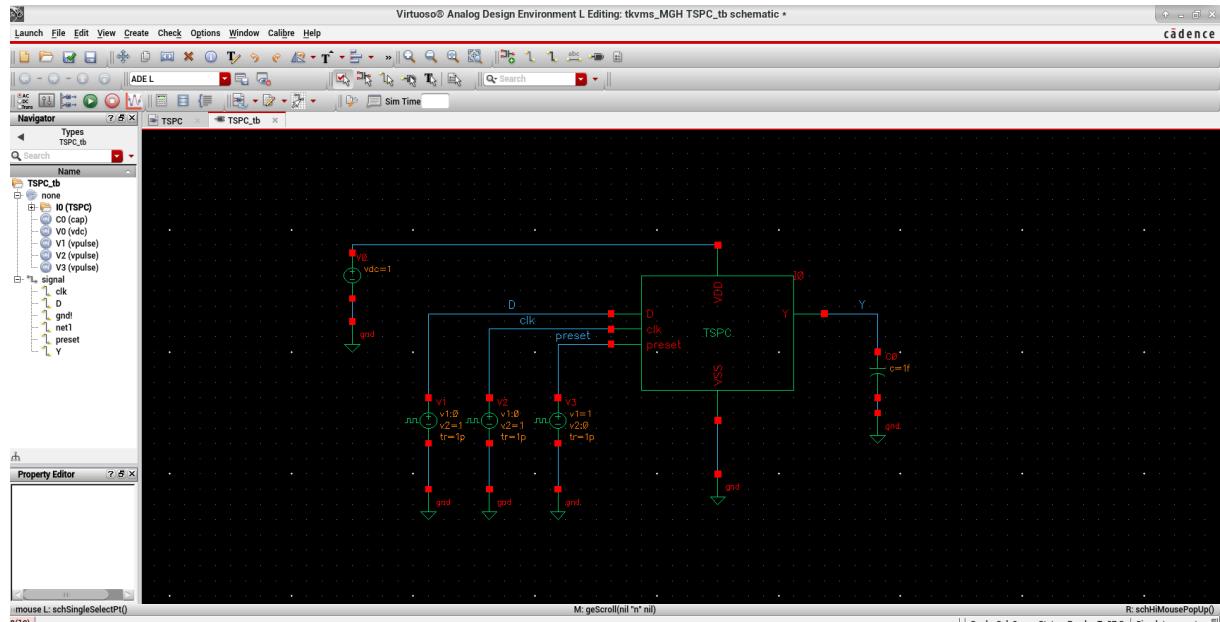


Figure 3.2: Testbench for TSPC D flip-flop

### 3.2 Transient Analysis Simulation:

The time dependence features of the flip flop's operation are captured in the simulation such as Cadence by focusing on how it switches between states in response to shifting clock and data inputs. A data input signal that varies at predetermined intervals is applied during the simulation, along with a clock signal with a given frequency and duty cycle. The transient response determines potential glitches or problems, set up and hold periods and propagation delays.

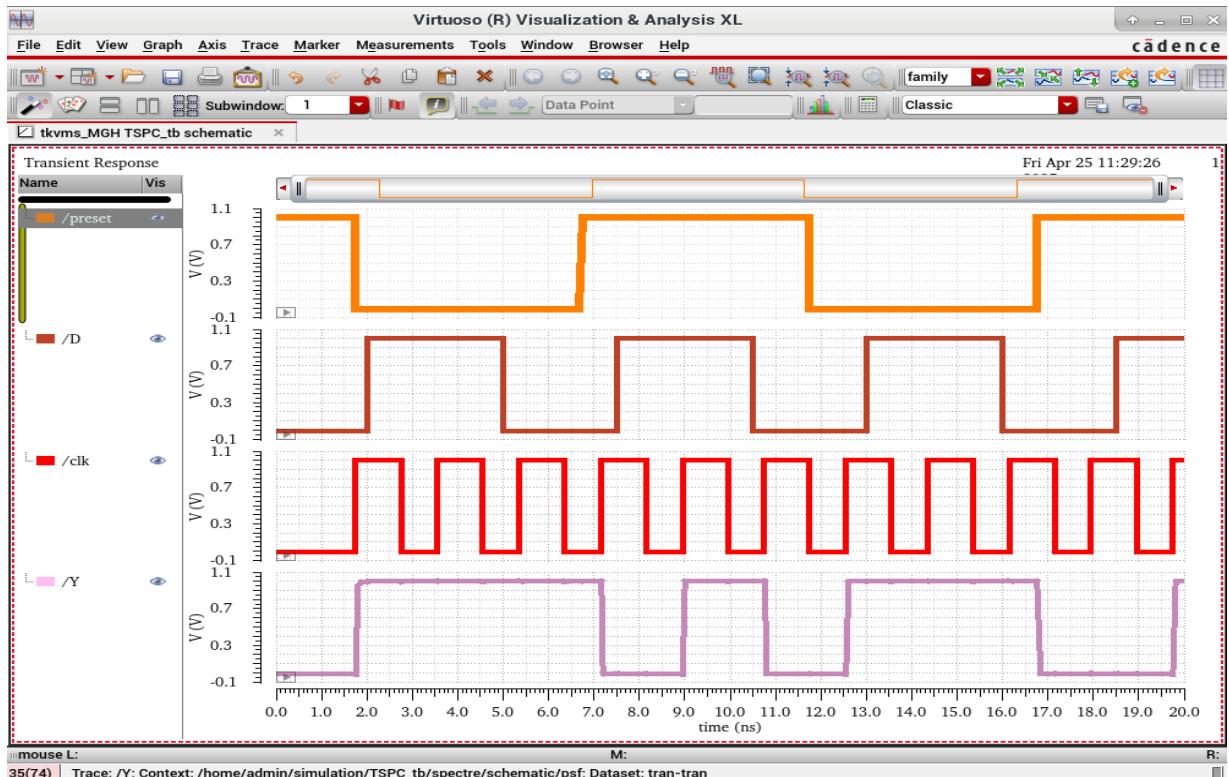


Figure 3.3: Transient Analysis of TSPC D flip flop

In the TSPC D flip flop, the vital measurements are the setup time and hold time. The set-up time responses the minimum of time before the clock edge that the data input (D) needs to be maintained steady to make the flip flop to sample it accurately. Meanwhile, the hold time illustrate the smallest time that follows the clock edge that the data input needs to stay untouched to be recorded accurately. The table below shows our results in determining required measurements.

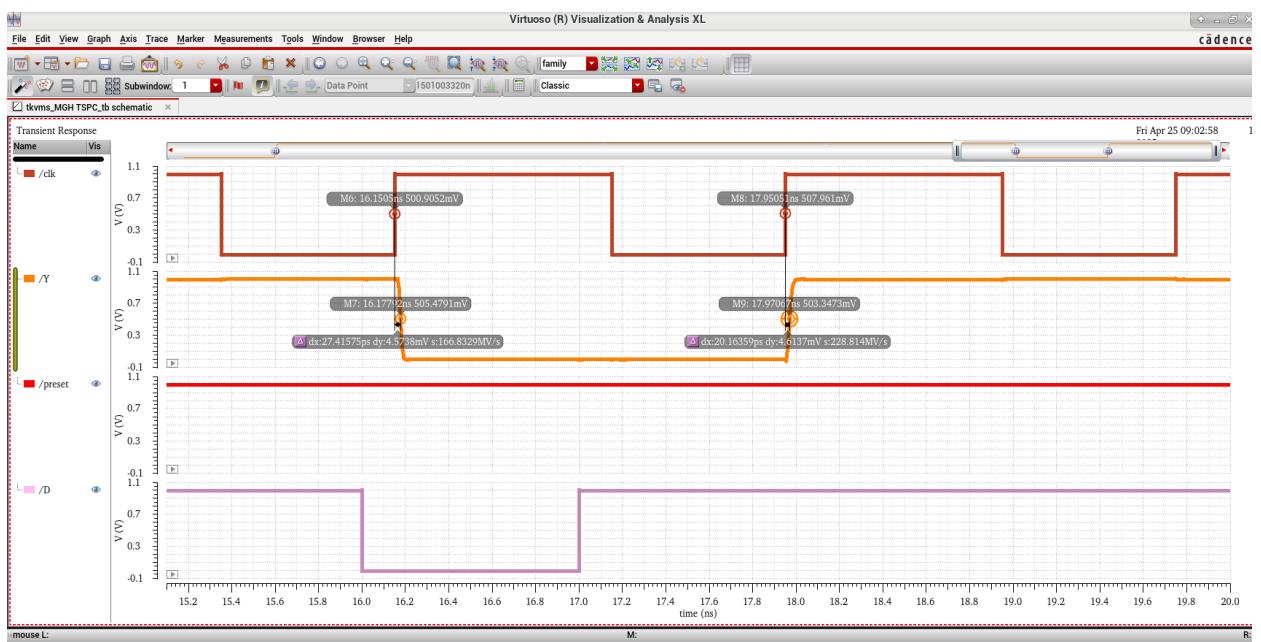


Figure 3.4: Flop Clock-to-Q Propagation Delay

Parameter	Result
$t_{pcqr}$ – Flop Clock-to-Q Propagation Delay (Low to High)	20.16 ps

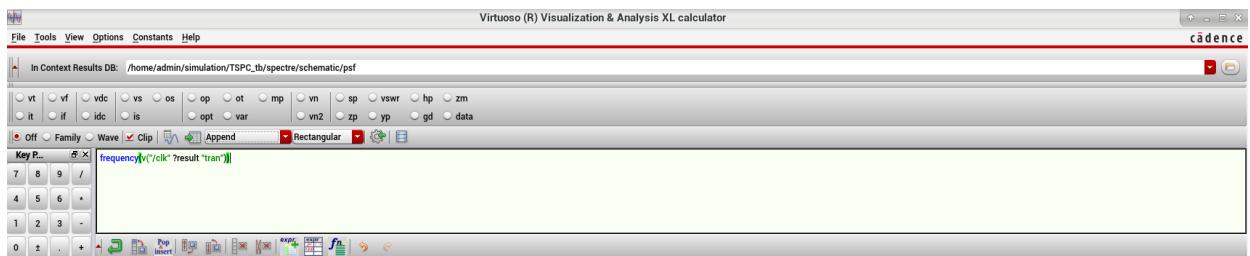
$t_{pdqf}$ – Flop Clock-to-Q Propagation Delay (High to Low)	27.4 ps
$t_{pd}$ – Flop Clock-to-Q Propagation Delay (average)	23.78 ps
Power consumption	9.7uW
$t_{hold}$	1.55 ns
$t_{setup}$	4.25 ns

**Table 3.2:** Delay time measurement of TSPC D flip-flop

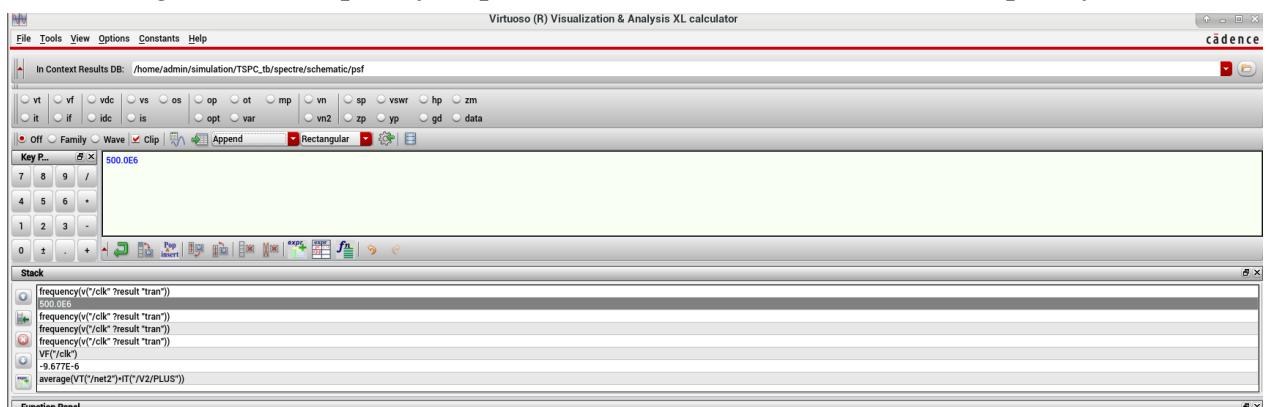
Moreover, we can measure the clock frequency base on the expression given in calculator:  $f_{clk} = 500.10^6$  Hz

CDF Parameter	Value	Display
Frequency name for 1/period		off ▾
Noise file name		off ▾
Number of noise/freq pairs	0	off ▾
DC voltage		off ▾
AC magnitude		off ▾
AC phase		off ▾
XF magnitude		off ▾
PAC magnitude		off ▾
PAC phase		off ▾
Voltage 1	0 V	off ▾
Voltage 2	1 V	off ▾
Period	2n s	off ▾
Delay time	650.00p s	off ▾
Rise time	400p s	off ▾
Fall time	400p s	off ▾
Pulse width	1n s	off ▾
Temperature coefficient 1		off ▾
Temperature coefficient 2		off ▾

**Figure 3.5:** testbench for calculating clock frequency



**Figure 3.6:** Frequency Expression is used to calculate clock frequency



**Figure 3.7:** Clock frequency result