

# Abdullah Giray Yağlıkçı

## Research Assistant at ETH Zurich

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Up-to-date version of CV is available at


<https://agyaglikci.github.io/onlineresume>

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I am a Ph.D. candidate in the Safari Research Group at ETH Zürich, working with Prof. Onur Mutlu. My current broader research interests are in computer architecture, systems, and hardware security with a special focus on DRAM robustness and performance. In particular, my PhD research focuses on understanding and solving the RowHammer vulnerability. I have published several works on this topic in major venues such as HPCA, MICRO, DSN, and ISCA. One of these works, BlockHammer, was named as a finalist by Intel in 2021 for the Intel Hardware Security Academic Award. My RowHammer research is in part supported by Google and the Microsoft Swiss Joint Research Center

## Professional Experience

1600 – 1601

### Twelfth Night

Viola finds herself shipwrecked in Illyria and, assuming that her brother Sebastian has died in the wreck, disguises herself as a man to gain a position in Duke Orsino's court. Orsino sends Viola (whom he knows as Cesario) to deliver a message to his love, Olivia. Olivia, however, dislikes the Duke. She falls in love with Viola, who she thinks is a man. Eventually, Viola's brother Sebastian, who in fact was unharmed in the wreck, reappears. At a critical moment, Viola's true identity is revealed when members of the court notice the similarities between her and Sebastian. Olivia quickly falls in love with Sebastian, and Viola confesses her love for the Duke.

comedy

love

1595–1596, with a possible early draft written in 1591

### The Tragedy of Romeo and Juliet

In Verona, Italy, two families, the Montagues and the Capulets, are in the midst of a bloody feud. Romeo, a Montague, and Juliet, a Capulet, fall in love and struggle to maintain their relationship in the face of familial hatred. After Romeo kills Juliet's cousin Tybalt in a fit of passion, things fall apart. Both lovers eventually commit suicide within minutes of each other, and the feuding families make peace over their recent grief.

tragedy

death

love

## Education

King Edward VI Grammar School in Stratford-upon-Avon [1571 - 1578]


## Selected Publications

in MICRO 2022




**Full Reference:** A. Giray Yaglikci, Ataberk Olgun, Minesh Patel, Haocong Luo, Hasan Hassan, Lois Orosa, Oguz Ergin, and Onur Mutlu, "HiRA: Hidden Row Activation for Reducing Refresh Latency of Off-the-Shelf DRAM Chips"

Proceedings of the 55th International Symposium on Microarchitecture (MICRO), Chicago, IL, USA, October 2022.

We propose a new operation, Hidden Row Activation (HiRA), and the HiRA Memory Controller (HiRA-MC) to perform HiRA operations. HiRA hides a refresh operation's latency by refreshing a row concurrently with accessing or refreshing another row within the same bank. Unlike prior works, HiRA achieves this parallelism without any modifications to off-the-shelf DRAM chips. To do so, it leverages the new observation that two rows in the same bank can be activated without data loss if the rows are connected to different charge restoration circuitry. HiRA reduces the time spent on refresh operations by 51.4%. HiRA-MC increases system performance by 12.6% and 3.73× as it reduces the performance degradation due to periodic refreshes and refreshes for RowHammer protection (preventive refreshes), respectively, for future DRAM chips with increased density and RowHammer vulnerability.

Full Paper: 

Live Talk Slides:  

Lecture (36 mins):   

rowhammer

defense

refresh

memory

dram

memory controller


subarray

parallelism


in DSN 2022




**Full Reference:** A. Giray Yağlıkcı, Haocong Luo, Geraldo F. de Oliveira, Ataberk Olgun, Minesh Patel, Jisung Park, Hasan Hassan, Jeremie S. Kim, Lois Orosa, and Onur Mutlu, **"Understanding RowHammer Under Reduced Wordline Voltage: An Experimental Study Using Real DRAM Devices"** Proceedings of the 52nd Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN), Baltimore, MD, USA, June 2022.

This is the first work to experimentally demonstrate on 272 real DRAM chips that lowering VPP reduces a DRAM chip's RowHammer vulnerability. We show that lowering VPP 1) increases the number of activate-precharge cycles needed to induce a RowHammer bit flip by up to 85.8 % with an average of 7.4 % across all tested chips and 2) decreases the RowHammer bit error rate by up to 66.9 % with an average of 15.2 % across all tested chips. At the same time, reducing VPP marginally worsens a DRAM cell's access latency, charge restoration, and data retention time within the guardbands of system-level nominal timing parameters for 208 out of 272 tested chips. We conclude that reducing VPP is a promising strategy for reducing a DRAM chip's RowHammer vulnerability without requiring modifications to DRAM chips.

Full Paper: 

arXiv: 

Lightning Talk (2 mins):   

Full Talk (34 mins incl. Q&A):   

rowhammer

characterization

real chips

memory

dram

voltage

wordline




in MICRO 2021




**Full Reference:** Lois Orosa, Abdullah Giray Yağlıkcı, Haocong Luo, Ataberk Olgun, Jisung Park, Hasan Hassan, Minesh Patel, Jeremie S. Kim, and Onur Mutlu, **"A Deeper Look into RowHammer's Sensitivities: Experimental Analysis of Real DRAM Chips and Implications on Future Attacks and Defenses"** Proceedings of the 54th International Symposium on Microarchitecture (MICRO), Virtual, October 2021.

We present an experimental characterization using 248 DDR4 and 24 DDR3 modern DRAM chips from four major DRAM manufacturers demonstrating how the RowHammer effects vary with three fundamental properties: 1) DRAM chip temperature, 2) aggressor row active time, and 3) victim DRAM cell's physical location. Among our 16 new observations, we highlight that a RowHammer bit flip 1) is very likely to occur in a bounded range, specific to each DRAM cell (e.g., 5.4% of the vulnerable DRAM cells exhibit errors in the range 70 °C to 90 °C), 2) is more likely to occur if the aggressor row is active for longer time (e.g., RowHammer vulnerability increases by 36% if we keep a DRAM row active for 15 column accesses), and 3) is more likely to occur in certain physical regions of the DRAM module under attack (e.g., 5% of the rows are 2x more vulnerable than the remaining 95% of the rows). Our study has important practical implications on future RowHammer attacks and defenses. We describe and analyze the implications of our new findings by proposing three future RowHammer attack and six future RowHammer defense improvements.

Full Paper: 

arXiv: 

Lightning Talk (1.5 mins):   

Full Talk (21 mins):   

rowhammer

characterization

real chips

memory

dram

temperature

access pattern

spatial variation

in HPCA 2021

**Full Reference:** A. Giray Yağlıkcı, Minesh Patel, Jeremie S. Kim, Roknoddin Azizi, Ataberk Olgun, Lois Orosa, Hasan Hassan, Jisung Park, Konstantinos Kanellopoulos, Taha Shahroodi, Saugata Ghose, and Onur Mutlu, **"BlockHammer: Preventing RowHammer at Low Cost by Blacklisting Rapidly-Accessed DRAM Rows,"** in Proceedings of the 27th International Symposium on High-Performance Computer Architecture (HPCA), Virtual, February-March 2021.

In this paper, we show that it is possible to efficiently and scalably prevent RowHammer bitflips without knowledge of or modification to DRAM internals. We introduce BlockHammer, a low-cost, effective, and easy-to-adopt RowHammer mitigation mechanism that prevents all RowHammer bitflips while overcoming the two key challenges: scalability with worsening RowHammer vulnerability and compatibility with commodity DRAM chips. BlockHammer selectively throttles memory accesses that may cause RowHammer bitflips. To our knowledge, this is the first work that prevents RowHammer bitflips efficiently and scalably without knowledge of or modifications to DRAM internals.

Full Paper: 

Short Talk (7 mins):  

Full Talk (22 mins):  

Intel HWSec Academic Awards Talk (2 mins):  

rowhammer

defense

throttling

memory

dram

memory controller

hardware

in ISCA, 2020

**Full Reference:** Jeremie S. Kim, Minesh Patel, A. Giray Yağlıkçı, Hasan Hassan, Roknoddin Azizi, Lois Orosa, and Onur Mutlu, "Revisiting RowHammer: An Experimental Analysis of Modern Devices and Mitigation Techniques," in Proceedings of the 47th International Symposium on Computer Architecture (ISCA), Valencia, Spain, June 2020.

In this paper, we first present an experimental characterization of RowHammer on 1580 DRAM chips (408× DDR3, 652× DDR4, and 520× LPDDR4) from 300 DRAM modules (60× DDR3, 110× DDR4, and 130× LPDDR4) with RowHammer protection mechanisms disabled, spanning multiple different technology nodes from across each of the three major DRAM manufacturers. Our studies definitively show that newer DRAM chips are more vulnerable to RowHammer: as device feature size reduces, the number of activations needed to induce a RowHammer bit flip also reduces, to as few as 9.6k (4.8k to two rows each) in the most vulnerable chip we tested.

Full Paper: 

Short Talk (7 mins):  

rowhammer

characterization

real chips

memory

dram

hardware