Curriculum Vitae

Abdullah Giray Yağlıkçı

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Google Scholar: https://scholar.google.com/citations?user=mt15O64AAAAJ&hl

Short Bio. I am a tenure-track faculty, leading the Secure and Sustainable System Scaling Lab at Helmholtz Institute Center of Information Security (CISPA). My current research aims enabling secure and sustainable system scaling as chips get denser and many users share chips. We push the boundaries of secure and sustainable system scaling via conducting research on high-performance, energy-efficient, and secure computer architectures and systems. Before joining CISPA, I was a postdoctoral researcher and lecturer at the Safari Research Group in ETH Zürich. My Ph.D. thesis, advised by Prof. Onur Mutlu, 1) builds a detailed understanding of DRAM read disturbance, a major limitation of main memory density scaling, and 2) builds mechanisms that efficiently and scalably mitigate DRAM read disturbance. I have published several works in this field in major venues, including HPCA, MICRO, DSN, ISCA, and USENIX Security. My Ph.D. dissertation received the W. C. Carter PhD Dissertation Award in Dependability and ACM SIGMICRO Phd Dissertation Award 2025. It also received an honorable mention by the ACM SIGARCH / IEEE CS TCCA Outstanding Dissertation Award, nominated for ETH Medal, chosen as a finalist by HOST PhD Dissertation Competition, and as a semi-finalist by IEEE TTTC E. J. McCluskey Best Doctoral Thesis Award. Among my first-author publications, BlockHammer (HPCA 2021) is chosen as a finalist by Intel Hardware Security Academic Award 2022, and an early version of Svärd (HPCA 2024) has won the ACM PACT Student Research Competition 2023. My Ph.D. research is in part supported by Google Security and Privacy Research Award and Microsoft Swiss Joint Research Center.

Education

PhD	ETH Zürich	Computer Engineering	2024
	Dissertation: *"Enabling Efficient and Scalable DRAM Read Disturbance Mitigation via New Experimental Insights into Modern DRAM Chips,"* ETH Zürich, 10.3929/ethz-b-000691009, August, 2024. Advisor: Onur Mutlu [Defense: ppt | pdf]		
	ACM SIGMICRO Dissertation Award 2025		
	IEEE/IFIP DSN W. C. Carter Doctoral Dissertation Award 2025 [ppt | pdf | video]		
	ACM SIGARCH Outstanding Dissertation Award (Honorable Mention) 2025		
	IEEE TTTC McCluskey Doctoral Dissertation Award (Semifinalist) 2025 [ppt | pdf | video]		
	ETH Medal for Outstanding Doctoral Thesis (Nominated) 2024		
	HOST Best Dissertation Award (Finalist) 2024 [ppt | pdf | video]		
	Dissertation reporting time: 6 years (2018 – 2024)		
MS	University of Notre Dame du Lac	Computer Engineering	2016
MS	TOBB ETU	Computer Engineering	2014
BS	TOBB ETU	Electrical Engineering	2011

Professional Experience

CISPA - Helmholtz Center for Information Security	Tenure-Track Faculty	2025 -
ETH Zürich	Postdoctoral Researcher and Lecturer	2024 - 2025
	Scientific Assistant (Research and Teaching Assistant)	2018 - 2024
Intel Labs	Research Intern	2017 - 2018
Carnegie Mellon University	Research Assistant	2016 - 2017
University of Notre Dame du Lac	Research Assistant	2014 - 2016
TOBB ETU	Research and Teaching Assistant	2012 - 2014

Honors and Recognitions

ACM SIGMICRO Dissertation Award, 2025:	Received the award
W. C. Carter PhD Dissertation Award in Dependability, 2025:	Received the award
ACM SIGARCH / IEEE CS TCCA Outstanding Dissertation Award, 2025:	Honorable Mention
IEEE TTTC E. J. McCluskey Best Doctoral Thesis Award, 2025:	Semi-finalist
HOST 2024 PhD Dissertation Competition:	One of five finalists - PhD Dissertation
ACM PACT 2023 Student Research Competition:	First place - Svärd (full version in HPCA'24)
ETH Medal, 2024:	Nominated by independent external experts
Intel Hardware Security Academic Award, 2022:	One of four finalists - BlockHammer (HPCA'21)
Distinguished Artifact Award at HPCA, 2025:	PaCRAM (HPCA'25)
Distinguished Artifact Award at ISCA, 2023:	One of 2 awardees - RowPress (ISCA'23)
IEEE Micro's Top Picks from Comp. Arch. Conferences:	One of 12 papers - RowPress (ISCA'23)

Invited Talks and Lectures

1. *"Chronus: Understanding and Securing the Cutting-Edge Industry Solutions to DRAM Read Disturbance,"* Future of Memory & Storage Summit, August 2025
2. *"Understanding Computational Capabilities of COTS DRAM Chips"* Future of Memory & Storage Summit, August 2025
3. *"Revisiting Memory Security for Emerging Data-Centric Computing Architectures"* SK Hynix Santa Clara, August 2025
4. *"Enabling Secure and Sustainable System Scaling"*
   UC Berkeley, August 2025
   SAFARI Live Workshop, July 2025
   CISPA, March 2025
   University of Edinburgh, March 2025
5. *"Scalable and Low Overhead Read Disturbance Mitigation,"* Future of Memory & Storage Summit, August 2024
6. *"Enabling Efficient and Scalable DRAM Read Disturbance Mitigation via New Experimental Insights into Modern DRAM Chips,"*
   Invited Lecture at Stanford University, August 2024 (40 mins)
   HOST PhD Dissertation Competition, May 2024 (23 mins)
   MICRO PhD Forum, October 2023 (3 mins)
   Invited Talk at Future of Memory & Storage Summit, August 2024
   Lectures at SK Hynix, Apple, and Rambus, August 2024
   Lectures at Univ. of Cambridge, King's College London, ARM, Huawei, and Microsoft, March 2024
   Lecture at AMD Research, Austin TX, November 2024
7. *"Memory Robustness,"* Lecture at ETHZ, May 2024 (1 hr 44 mins)
8. *"Fundamentally Understanding DRAM Reliability & Enabling Fast and Secure Memory,"* Microsoft Swiss Joint Research Center Spring Workshop, April 2024
9. "Efficiently and Scalably Mitigating RowHammer," [SAFARI Live Seminars, February 2024 (2 hrs)]
10. *"A Deeper Look into RowHammer's Characteristics,"* [SAFARI Live Seminars, January 2024 (2 hrs)]
11. *"Memory Security, Reliability, Safety Problems and Solutions"* [Lecture at ETHZ, October 2023 (3 hrs)]
12. *"Data Retention and Memory Refresh"* [Lecture at ETHZ, October 2023 (3 hrs)]
13. *"Memory Latency"* [Lecture at ETHZ, October 2023 (3 hrs)]
14. *"Fundamentally Understanding and Solving RowHammer"*
    28th Asia and South Pacific Design Automation Conference (ASP-DAC), Tokyo, Japan, January 2023 (26 mins)
    Microsoft Swiss Joint Research Center - Workshop, March 2022 (20 mins)

Conference Talks

1. *"Spatial Variation-Aware Read Disturbance Defenses: Experimental Analysis of Real DRAM Chips and Implications on Future Solutions,"* International Symposium on High-Performance Computer Architecture (HPCA-30), Edinburgh, UK, April 2024.
2. *"HiRA: Hidden Row Activation for Reducing Refresh Latency of Off-the-Shelf DRAM Chips,"* International Symposium on Microarchitecture (MICRO-55), Chicago, IL, USA, October 2022.

3. *"Understanding RowHammer Under Reduced Wordline Voltage: An Experimental Study Using Real DRAM Devices,"* Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN-52), Baltimore, MD, USA, June 2022.
4. *"A Deeper Look into RowHammer's Sensitivities: Experimental Analysis of Real DRAM Chips and Implications on Future Attacks and Defenses,"* International Symposium on Microarchitecture (MICRO-54), Virtual, October 2021.
5. *"BlockHammer: Preventing RowHammer at Low Cost by Blacklisting Rapidly-Accessed DRAM Rows,"* International Symposium on High-Performance Computer Architecture (HPCA-27), Virtual, February-March 2021.

Teaching Experience

- EFCL Summer School, June 2024: Lecturer in the Computer Architecture Track
- Dept. of Information Technologies and Electrical Engineering at ETH Zürich
  - FPGA-based Exploration of DRAM and RowHammer P&S Course
    Co-Instructor 2024
    Head teaching assistant 2023
    Teaching assistant 2020-2023
- Dept. of Computer Science at ETH Zürich
  - Teaching assistant in the Computer Architecture Course (MSc Level), 2018 - 2024.
  - Teaching assistant in the Seminar in Computer Architecture Course, 2018 - 2024.
  - Teaching assistant in the Digital Design and Computer Architecture Course, 2020 - 2025.
  - Teaching assistant in the Design of Digital Circuits Course, 2018 - 2019.
- Dept. of Computer Engineering, TOBB University of Economics and Technology, Türkiye
  - Teaching assistant in the Advanced Computer Architecture Course (MSc Level), 2012 - 2014.
  - Teaching assistant in the Computer Architecture Course, 2011 - 2014.
  - Teaching assistant in the Digital Design Course, 2011 - 2014.

Thesis Publications

[P1] **A. Giray Yağlıkçı**, Yahya Can Tugrul, Geraldo F. Oliveira, İsmail Yuksel, Ataberk Olgun, Haocong Luo, and Onur Mutlu, *"Spatial Variation-Aware Read Disturbance Defenses: Experimental Analysis of Real DRAM Chips and Implications on Future Solutions,"* International Symposium on High-Performance Computer Architecture (HPCA-30), Edinburgh, UK, April 2024. [Conference Talk: ppt | pdf | video] [ACM PACT 2023 Student Research Competition: pdf | video | poster]
First place at ACM PACT 2023 Student Research Competition

[P2] **A. Giray Yağlıkçı**, Ataberk Olgun, Minesh Patel, Haocong Luo, Hasan Hassan, Lois Orosa, Oguz Ergin, and Onur Mutlu, *"HiRA: Hidden Row Activation for Reducing Refresh Latency of Off-the-Shelf DRAM Chips,"* International Symposium on Microarchitecture (MICRO-55), Chicago, IL, USA, October 2022. [Conference Talk: ppt | pdf | video] [Invited Lecture: ppt | pdf | video]

[P3] **A. Giray Yağlıkçı**, Haocong Luo, Geraldo F. de Oliveira, Ataberk Olgun, Minesh Patel, Jisung Park, Hasan Hassan, Jeremie S. Kim, Lois Orosa, and Onur Mutlu, *"Understanding RowHammer Under Reduced Wordline Voltage: An Experimental Study Using Real DRAM Devices,"* Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN-52), Baltimore, MD, USA, June 2022. [Talk: ppt | pdf | video] [Lightning Talk: video]

[P4] **A. Giray Yağlıkçı***, Lois Orosa*, Haocong Luo, Ataberk Olgun, Jisung Park, Hasan Hassan, Minesh Patel, Jeremie S. Kim, and Onur Mutlu, *"A Deeper Look into RowHammer's Sensitivities: Experimental Analysis of Real DRAM Chips and Implications on Future Attacks and Defenses,"* International Symposium on Microarchitecture (MICRO-54), Virtual, October 2021. [Conference Talk: ppt | pdf | video] [Lightning Talk: ppt | pdf | video]

[P5] **A. Giray Yağlıkçı**, Minesh H. Patel, Jeremie S. Kim, Lois Orosa, Roknoddin Azizibarzoki, Hasan Hassan, Ataberk Olgun, Jisung Park, Konstantinos Kanellopoulos, Taha Shahroodi, Saugata Ghose, and Onur Mutlu, *"BlockHammer: Preventing RowHammer at Low Cost by Blacklisting Rapidly-Accessed DRAM Rows,"* International Symposium on High-Performance Computer Architecture (HPCA-27), Virtual, February-March 2021. [Conference Talk: ppt | pdf | video] [Short Talk: ppt | pdf | video] [Artifact]
[Intel Hardware Security Academic Awards Talk: ppt | pdf | video]
Intel Hardware Security Academic Award Finalist (one of 4 finalists out of 34 nominations)

Co-Supervised Publications

[P6] Oğuzhan Canpolat, **A. Giray Yağlıkçı**, Ataberk Olgun, İsmail Emir Yüksel, Yahya Can Tuğrul, Konstantinos Kanellopoulos, Oğuz Ergin, and Onur Mutlu, *"Chronus: Understanding and Securing the Cutting-Edge Industry Solutions to DRAM Read Disturbance,"* International Symposium on High-Performance Computer Architecture (HPCA-31), to appear, Las Vegas, NV, USA, April 2025.
Officially artifact evaluated as available, functional, and reproduced

[P7] Yahya Can Tuğrul, **A. Giray Yağlıkçı**, İsmail Emir Yüksel, Ataberk Olgun, Oğuzhan Canpolat, Nisa Bostancı, Mohammad Sadrosadati, Oğuz Ergin, and Onur Mutlu, *"Understanding RowHammer Under Reduced Refresh Latency: Experimental Analysis of Real DRAM Chips and Implications on Future Solutions,"* International Symposium on High-Performance Computer Architecture (HPCA-31), to appear, Las Vegas, NV, USA, April 2025.
Officially artifact evaluated as available, functional, and reproduced
Distinguished artifact award at HPCA 2025

[P8] Oğuzhan Canpolat, **A. Giray Yağlıkçı**, Ataberk Olgun, İsmail Emir Yuksel, Yahya Can Tuğrul, Konstantinos Kanellopoulos, Oğuz Ergin, and Onur Mutlu, *"BreakHammer: Enhancing RowHammer Mitigations by Carefully Throttling Suspect Threads,"* International Symposium on Microarchitecture (MICRO-57), to appear, Austin, TX, USA, October 2024. [Poster in FMS'24: ppt | pdf] [Artifact]
Officially artifact evaluated as available, functional, and reproduced.

[P9] Oğuzhan Canpolat, **A. Giray Yağlıkçı**, Geraldo F. Oliveira, Ataberk Olgun, Oğuz Ergin, and Onur Mutlu, *"Understanding the Security Benefits and Overheads of Emerging Industry Solutions to DRAM Read Disturbance,"* 4th Workshop on DRAM Security (DRAMsec), held with Annual International Symposium on Computer Architecture (ISCA-51), Buenos Aires, Argentina, July 2024. [Poster in FMS24: ppt | pdf] [Artifact]

Other Publications

[P10] İsmail Emir Yüksel, Ataberk Olgun, F. Nisa Bostancı, Oğuzhan Canpolat, Geraldo F. Oliveira, Mohammad Sadrosadati, A. Giray Yağlıkçı, Onur Mutlu, *"In-DRAM True Random Number Generation Using Simultaneous Multiple-Row Activation: An Experimental Study of Real DRAM Chips,"* Proceedings of the 43rd IEEE International Conference on Computer Design (ICCD), Dallas, TX, USA, 2025.

[P11] İsmail Emir Yüksel, Ataberk Olgun, F. Nisa Bostancı, Haocong Luo, A. Giray Yağlıkçı, Onur Mutlu, *"ColumnDisturb: Understanding Column-based Read Disturbance in Real DRAM Chips and Implications for Future Systems,"* Proceedings of the 58th International Symposium on Microarchitecture (MICRO), Seoul, South Korea, October 2025.

[P12] F. Nisa Bostancı, Oğuzhan Canpolat, Ataberk Olgun, İsmail Emir Yüksel, Konstantinos Kanellopoulos, Mohammad Sadrosadati, A. Giray Yağlıkçı, Onur Mutlu, *"Understanding and Mitigating Covert Channel and Side Channel Vulnerabilities Introduced by RowHammer Defenses,"* Proceedings of the 58th International Symposium on Microarchitecture (MICRO), Seoul, South Korea, 2025.

[P13] Carina Fiedler, Jonas Juffinger, Sudheendra Raghav Neela, Martin Heckel, Hannes Weissteiner, **A. Giray Yaglikci**, Florian Adamsky, Daniel Gruss, *"Memory Band-Aid: A Principled RowHammer Defense-in-Depth,"* Proceedings of the Network and Distributed System Security Symposium (NDSS), San Diego, CA, USA, 2026.

[P14] Ismail Emir Yuksel, Akash Sood, Ataberk Olgun, Oguzhan Canpolat, Haocong Luo, Nisa Bostanci, Mohammad Sadrosadati, **A. Giray Yaglikci**, and Onur Mutlu, *"PuDHammer: Experimental Analysis of Read Disturbance Effects of Processing-using-DRAM in Real DRAM Chips,"* Proceedings of the 52nd Annual International Symposium on Computer Architecture (ISCA), Tokyo, Japan, June 2025.

[P15] Geraldo Francisco, Mayank Kabra, Yuxin Guo, Kangqi Chen, **A. Giray Yaglikci**, Melina Soysal, Mohammad Sadrosadati, Joaquin Olivares, Saugata Ghose, Juan Gomez-Luna, and Onur Mutlu, *"Proteus: Achieving High-Performance Processing-Using-DRAM via Dynamic Precision Bit-Serial Arithmetic,"* Proceedings of the 37th ACM International Conference on Supercomputing (ICS), Salt Lake City, UT, USA, June 2025.

[P16] Nisa Bostanci, Konstantinos Kanellopoulos, Ataberk Olgun, **A. Giray Yaglikci**, Ismail Emir Yuksel, Nika Mansouri Ghiasi, Zulal Bingol, Mohammad Sadrosadati, and Onur Mutlu, *"Revisiting Main Memory-Based Covert and Side Channel Attacks in the Context of Processing-in-Memory,"* Proceedings of the 55th Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN), Naples, Italy, June 2025. [IMPACT Source Code]
Officially artifact evaluated as available, reviewed, and reproduced

[P17] Haocong Luo, Ismail Emir Yuksel, Ataberk Olgun, **Abdullah Giray Yaglikci**, and Onur Mutlu, *"Revisiting DRAM Read Disturbance: Identifying Inconsistencies Between Experimental Characterization with Device-Level Studies,"* Proceedings of the 43rd IEEE VLSI Test Symposium (VTS), Tempe, AZ, USA, April 2025. [Slides (pptx) (pdf)] [Source Code]

[P18] Ataberk Olgun, F. Nisa Bostanci, İsmail Emir Yuksel, **A. Giray Yağlıkçı**, Geraldo F. Oliveira, Haocong Luo, Oguzhan Canpolat, Minesh Patel, and Onur Mutlu, *"Variable Read Disturbance: An Experimental Analysis of Temporal Variation in DRAM Read Disturbance,"* International Symposium on High-Performance Computer Architecture (HPCA-31), Las Vegas, NV, USA, April 2025.

[P19] Hasan Hassan, Ataberk Olgun, **A. Giray Yağlıkçı**, Haocong Luo, and Onur Mutlu, *"Self-Managing DRAM: A Low-Cost Framework for Enabling Autonomous and Efficient in-DRAM Operations,"* International Symposium on Microarchitecture (MICRO-57), Austin, TX, USA, October 2024. [Artifact]

[P20] Minesh Patel, Taha Shahroodi, Aditya Manglik, **A. Giray Yağlıkçı**, Ataberk Olgun, Haocong Luo, and Onur Mutlu, *"Rethinking the Producer-Consumer Relationship in Modern DRAM-Based Systems,"* IEEE Access, 2024.

[P21] Ataberk Olgun, Yahya Can Tugrul, Nisa Bostanci, İsmail Emir Yuksel, Haocong Luo, Steve Rhyner, **A. Giray Yağlıkçı**, Geraldo F. Oliveira, and Onur Mutlu, *"ABACuS: All-Bank Activation Counters for Scalable and Low Overhead RowHammer Mitigation,"* USENIX Security Symposium (USENIX Security-33), Philadelphia, PA, USA, August 2024. [Artifact] [Poster FMS'24]
Officially artifact evaluated as available, functional, and reproduced.

[P22] Ataberk Olgun, Majd Osserian, **A. Giray Yağlıkçı**, Yahya Can Tugrul, Haocong Luo, Steve Rhyner, Behzad Salami, Juan Gomez-Luna, and Onur Mutlu, *"Read Disturbance in High Bandwidth Memory: A Detailed Experimental Study on HBM2 DRAM Chips,"* Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN-54), Brisbane, Australia, June 2024. [Slides: ppt | pdf] [Artifact]
Officially artifact evaluated as available, reviewed, and reproducible.

[P23] İsmail Emir Yuksel, Yahya Can Tugrul, F. Nisa Bostanci, Geraldo F. Oliveira, **A. Giray Yağlıkçı**, Ataberk Olgun, Melina Soysal, Haocong Luo, Juan Gomez-Luna, Mohammad Sadrosadati, and Onur Mutlu, *"Simultaneous Many-Row Activation in Off-the-Shelf DRAM Chips: Experimental Characterization and Analysis,"* Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN-54), Brisbane, Australia, June 2024. [Slides ppt | pdf] [Artifact]
Officially artifact evaluated as available, reviewed, and reproducible.

[P24] Haocong Luo, İsmail Emir Yüksel, Ataberk Olgun, **A. Giray Yağlıkçı**, Mohammad Sadrosadati, and Onur Mutlu, *"An Experimental Characterization of Combined RowHammer and RowPress Read Disturbance in Modern DRAM Chips,"* Annual IEEE/IFIP International Conference on Dependable Systems and Networks Disrupt Track (DSN-54 Disrupt), Brisbane, Australia, June 2024. [Slides ppt | pdf]

[P25] Ataberk Olgun, F. Nisa Bostanci, Geraldo F. Oliveira, Yahya Can Tugrul, Rahul Bera, **A. Giray Yağlıkçı**, Hasan Hassan, Oguz Ergin, and Onur Mutlu, *"Sectored DRAM: A Practical Energy-Efficient and High-Performance Fine-Grained DRAM Architecture,"* ACM Transactions on Architecture and Code Optimization (TACO), June, 2024.[ACM Digital Library version]

[P26] Lois Orosa, Ulrich Ruhrmair, **A. Giray Yağlıkçı**, Haocong Luo, Ataberk Olgun, Patrick Jattke, Minesh Patel, Jeremie S. Kim, Kaveh Razavi, and Onur Mutlu, *"SpyHammer: Understanding and Exploiting RowHammer Under Fine-Grained Temperature Variations,"* IEEE Access, June 2024.

[P27] F. Nisa Bostancı, İsmail E. Yüksel, Ataberk Olgun, Konstantinos Kanellopoulos, Yahya Can Tugrul, **A. Giray Yağlıkçı**, Mohammad Sadrosadati, and Onur Mutlu, *"CoMeT: Count-Min-Sketch-based Row Tracking to Mitigate RowHammer at Low Cost,"* International Symposium on High-Performance Computer Architecture (HPCA-30), Edinburgh, UK, April 2024.. [Slides ppt | pdf] [Artifact] [Poster FMS'24] Officially artifact evaluated as available, reviewed, and reproducible.

[P28] İsmail E. Yüksel, Yahya C. Tugrul, Ataberk Olgun, F. Nisa Bostancı, **A. Giray Yağlıkçı**, Geraldo F. Oliveira, Haocong Luo, Juan Gomez-Luna, Mohammad Sadrosadati, and Onur Mutlu, *"Functionally-Complete Boolean Logic in Real DRAM Chips: Experimental Characterization and Analysis,"* International Symposium on High-Performance Computer Architecture (HPCA-30), Edinburgh, UK, April 2024. [Slides ppt | pdf] [Artifact]

[P29] Geraldo F. Oliveira, Ataberk Olgun, **A. Giray Yağlıkçı**, F. Nisa Bostancı, Juan Gómez-Luna, Saugata Ghose, and Onur Mutlu, *"MIMDRAM: An End-to-End Processing-Using-DRAM System for High-Throughput, Energy-Efficient and Programmer- Transparent Multiple-Instruction Multiple-Data Computing,"* International Symposium on High-Performance Computer Architecture (HPCA-30), Edinburgh, UK, April 2024. [Slides ppt | pdf] [Artifact]

[P30] Haocong Luo, Yahya Can Tuğrul, F. Nisa Bostanci, Ataberk Olgun, **A. Giray Yağlıkçı**, and Onur Mutlu, *"Ramulator 2.0: A Modern, Modular, and Extensible DRAM Simulator,"* IEEE Computer Architecture Letters (CAL), 2024. [Ramulator 2.0 Source Code]

[P31] Haocong Luo, Ataberk Olgun, **A. Giray Yağlıkçı**, Yahya Can Tugrul, Steve Rhyner, M. Banu Cavlak, Joël Lindegger, Mohammad Sadrosadati, and Onur Mutlu, *"RowPress Vulnerability in Modern DRAM Chips,"* IEEE Micro, Special Issue: Micro's Top Picks from 2023 Computer Architecture Conferences (MICRO TOP PICKS), July/August 2024.

[P32] Haocong Luo, Ataberk Olgun, **A. Giray Yağlıkçı**, Yahya Can Tugrul, Steve Rhyner, Meryem Banu Cavlak, Joël Lindegger, Mohammad Sadrosadati, and Onur Mutlu, *"RowPress: Amplifying Read Disturbance in Modern DRAM Chips,"* International Symposium on Computer Architecture (ISCA-50), Orlando, FL, USA, June 2023. [Extended arxiv version] [Slides ppt | pdf | video] [Lightning Talk Slides ppt | pdf | video] [Artifact]
Officially artifact evaluated as available, reusable, and reproducible.
Distinguished artifact award at ISCA 2023.
One of the 12 computer architecture papers in Top Picks by IEEE Micro, 2024.

[P33] Ataberk Olgun, Majd Osseiran, **A. Giray Yağlıkçı**, Yahya Can Tugrul, Haocong Luo, Steve Rhyner, Behzad Salami, Juan Gomez Luna, and Onur Mutlu, *"An Experimental Analysis of RowHammer in HBM2 DRAM Chips,"* Annual IEEE/IFIP International Conference on Dependable Systems and Networks Disrupt Track (DSN-53 Disrupt), Porto, Portugal, June 2023. [Slides ppt | pdf | video]

[P34] Ataberk Olgun, Hasan Hassan, **A. Giray Yağlıkçı**, Yahya Can Tuğrul, Lois Orosa, Haocong Luo, Minesh Patel, Oğuz Ergin, and Onur Mutlu, *"DRAM Bender: An Extensible and Versatile FPGA-based Infrastructure to Easily Test State-of-the-art DRAM Chips,"* IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023. [Source Code] [Tutorial Video]

[P35] Onur Mutlu, Ataberk Olgun, and **A. Giray Yağlıkçı**, *"Fundamentally Understanding and Solving RowHammer,"* Invited Special Session Paper at the 28th Asia and South Pacific Design Automation Conference (ASP-DAC), Tokyo, Japan, January 2023. [Slides ppt | pdf | video (26 mins)]

[P36] F. Nisa Bostanci, Ataberk Olgun, Lois Orosa, **A. Giray Yağlıkçı**, Jeremie S. Kim, Hasan Hassan, Oguz Ergin, and Onur Mutlu, *"DR-STRaNGe: End-to-End System Design for DRAM-based True Random Number Generators,"* International Symposium on High-Performance Computer Architecture (HPCA-28), Virtual, April 2022. [Talk ppt | pdf | video] [Short Talk Slides ppt | pdf]

[P37] Jawad Haj Yahya, Jeremie S. Kim, **A. Giray Yağlıkçı**, Jisung Park, Efraim Rotem, Yanos Sazeides, and Onur Mutlu, *"DarkGates: A Hybrid Power-Gating Architecture to Mitigate the Performance Impact of Dark-Silicon in High Performance Processors,"* International Symposium on High-Performance Computer Architecture (HPCA-28), Virtual, April 2022. [Slides ppt | pdf] [Short Talk Slides ppt | pdf]

[P38] Jawad Haj-Yahya, Jeremie S. Kim, **A. Giray Yağlıkçı**, Ivan Puddu, Lois Orosa, Juan Gomez Luna, Mohammed Alser, and Onur Mutlu, *"IChannels: Exploiting Current Management Mechanisms to Create Covert Channels in Modern Processors,"* International Symposium on Computer Architecture (ISCA-48), Virtual, June 2021. [Talk ppt | pdf | video (21 minutes)] [Short Talk ppt | pdf]

[P39] Ataberk Olgun, Minesh Patel, **A. Giray Yağlıkçı**, Haocong Luo, Jeremie Kim, Nisa Bostanci, Nandita Vijaykumar, Oguz Ergin, and Onur Mutlu, *"QUAC-TRNG: High-Throughput True Random Number Generation Using Quadruple Row Activation in Commodity DRAM Chips,"* International Symposium on Computer Architecture (ISCA-48), Virtual, June 2021. [Talk ppt | pdf | video] [Short ppt | pdf]
[SAFARI Live Seminar]

[P40] Jeremie S. Kim, Minesh Patel, **A. Giray Yağlıkçı**, Hasan Hassan, Roknoddin Azizi, Lois Orosa, and Onur Mutlu, *"Revisiting RowHammer: An Experimental Analysis of Modern Devices and Mitigation Techniques,"* International Symposium on Computer Architecture (ISCA-47), Valencia, Spain, June 2020. [Slides ppt | pdf] [Lightning Talk ppt | pdf

| video] [Lecture ppt | pdf | video]
[ARM Research Summit ppt | pdf | video]

[P41] Jawad Haj-Yahya, Mohammed Alser, Jeremie S. Kim, **A. Giray Yağlıkçı**, Nandita Vijaykumar, Efraim Rotem, and Onur Mutlu, *"SysScale: Exploiting Multi-domain Dynamic Voltage and Frequency Scaling for Energy Efficient Mobile Processors,"* International Symposium on Computer Architecture (ISCA-47), Valencia, Spain, June 2020. [Full Talk ppt | pdf | video] [Lightning Talk ppt | pdf | video]

[P42] Haocong Luo, Taha Shahroodi, Hasan Hassan, Minesh Patel, **A. Giray Yağlıkçı**, Lois Orosa, Jisung Park, and Onur Mutlu, *"CLR-DRAM: A Low-Cost DRAM Architecture Enabling Dynamic Capacity-Latency Trade-Off,"* International Symposium on Computer Architecture (ISCA-47), Valencia, Spain, June 2020. [Talk ppt | pdf | video] [Lightning Talk ppt | pdf | video]

[P43] Skanda Koppula, Lois Orosa, **A. Giray Yağlıkçı**, Roknoddin Azizi, Taha Shahroodi, Konstantinos Kanellopoulos, and Onur Mutlu, *"EDEN: Enabling Energy-Efficient, High-Performance Deep Neural Network Inference Using Approximate DRAM,"* International Symposium on Microarchitecture (MICRO-52), Columbus, OH, USA, October 2019. [Slides ppt | pdf] [Lightning Talk ppt | pdf | video] [Poster ppt | pdf] [Full Talk Lecture]

[P44] Hasan Hassan, Minesh Patel, Jeremie S. Kim, **A. Giray Yağlıkçı**, Nandita Vijaykumar, Nika Mansourighiasi, Saugata Ghose, and Onur Mutlu, *"CROW: A Low-Cost Substrate for Improving DRAM Performance, Energy Efficiency, and Reliability,"* International Symposium on Computer Architecture (ISCA-46), Phoenix, AZ, USA, June 2019. [Talk ppt | pdf | video] [Lightning Talk ppt | pdf | video] [Poster ppt | pdf] [Lecture] [Artifact]

[P45] Saugata Ghose, **A. Giray Yağlıkçı**, Raghav Gupta, Donghyuk Lee, K. Kudrolli, William X. Liu, Hasan Hassan, Kevin K. Chang, Niladrish Chatterjee, Aditya Agrawal, Michael O'Connor, and Onur Mutlu, *"What Your DRAM Power Models Are Not Telling You: Lessons from a Detailed Experimental Study,"* International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS), Irvine, CA, USA, June 2018. [Abstract] [POMACS Version] [Talk ppt | pdf] [VAMPIRE DRAM Power Model]

[P46] Kevin Chang, **A. Giray Yağlıkçı**, Saugata Ghose, Aditya Agrawal, Niladrish Chatterjee, Abishek Kashyap, Donghyuk Lee, Michael O'Connor, Hasan Hassan, and Onur Mutlu, *"Understanding Reduced-Voltage Operation in Modern DRAM Devices: Experimental Characterization, Analysis, and Mechanisms,"* International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS), Urbana-Champaign, IL, USA, June 2017. [Abstract] [POMACS Version] [Talk ppt | pdf] [Full Lecture Video] [Full Data Sets and Circuit Model]

Preprints and Technical Reports

[P47] **A. Giray Yağlıkçı**, Jeremie S. Kim, Fabrice Devaux, and Onur Mutlu, *"Security Analysis of the Silver Bullet Technique for RowHammer Prevention,"* arXiv: 2106.07084 [cs.CR], 2021.

[P48] Konstantinos Kanellopoulos, F. Nisa Bostanci, Ataberk Olgun, **A. Giray Yağlıkçı**, İsmail Emir Yüksel, Nika Mansouri Ghiasi, Zülal Bingöl, Mohammad Sadrosadati, and Onur Mutlu, *"Amplifying Main Memory-Based Timing Covert and Side Channels using Processing-in-Memory Operations,"* arXiv: 2404.11284 [cs.CR], 2024.

[P49] İsmail Emir Yüksel, Ataberk Olgun, Behzad Salami, F. Nisa Bostancı, Yahya Can Tuğrul, **A. Giray Yağlıkçı**, Nika Mansouri Ghiasi, Onur Mutlu, and Oğuz Ergin, *"TuRaN: True Random Number Generation Using Supply Voltage Underscaling in SRAMs,"* arXiv: 2211.10894 [cs.AR], 2022.

[P50] Minesh Patel, Taha Shahroodi, Aditya Manglik, **A. Giray Yağlıkçı**, Ataberk Olgun, Haocong Luo, and Onur Mutlu, *"A Case for Transparent Reliability in DRAM Systems,"* arXiv: 2204.10378 [cs.AR], 2022.

Manuscripts Under Submission

[P51] **A. Giray Yağlıkçı**, Oğuzhan Canpolat, Prithvi Velicheti, Ataberk Olgun, Nisa Bostancı, Andreas Kosmas Kakolyris, İsmail Emir Yüksel,Geraldo F. de Oliveira, and Onur Mutlu, *"High Bandwidth Meets Low Latency: Understanding Access Latency of High Bandwidth Memory via Experimental Analyses Using Real HBM2 DRAM Chips,"* (Blinded).

[P52] İsmail Emir Yüksel, Akash Sood, Ataberk Olgun, Oğuzhan Canpolat, Haocong Luo, Nisa Bostanci, Mohammed Sadrosadati, **A. Giray Yağlıkçı**, and Onur Mutlu, *"PuDHammer: Experimental Analysis of Read Disturbance Effects of Processing-using-DRAM in Real DRAM Chips,"* (Blinded).

[P53] Nisa Bostanci, Oğuzhan Canpolat, Ataberk Olgun, İsmail Emir Yüksel, Mohammed Sadrosadati, **A. Giray Yağlıkçı**, and Onur Mutlu, *"Understanding Side and Covert Channel Vulnerabilities Introduced by RowHammer Mitigations,"* (Blinded).

[P54] Nisa Bostanci, Konstantinos Kanellopoulos, Ataberk Olgun, **A. Giray Yağlıkçı**, İsmail Emir Yuksel, Nika Mansouri Ghiasi, Zülal Bingöl, Mohammad Sadrosadati, and Onur Mutlu, *"Revisiting Main Memory-Based Covert and Side Channel Attacks in the Context of Processing-in-Memory,"* (Blinded).

Open-Source Tools and Infrastructure

- Ramulator 2.0: A modern, modular, and extensible DRAM simulator, including the implementations of several of our papers [P5–P9, P21]
  https://github.com/CMU-SAFARI/ramulator2
- DRAM Bender: The FPGA-based infrastructure in our TCAD 2023 paper [R22], which enabled many works, including [P1–P4, P10, P13–P15, P17, P19, P22–P25, P30, P31, P36, P37, P42]
  https://github.com/CMU-SAFARI/DRAM-Bender
- Self-Managing DRAM Simulator: Source code for the evaluation of our MICRO 2024 paper [P8]
  https://github.com/CMU-SAFARI/SelfManagingDRAM
- ABACuS Simulator: Source code for the evaluation of our USENIX Security 2024 paper [P9]
  https://github.com/CMU-SAFARI/ABACuS
- HBM-Read Disturbance Tests: Source code and scripts of our DSN 2024 paper [P10]
  https://github.com/CMU-SAFARI/HBM-Read-Disturbance
- SiMRA-DRAM: Source code of tests and demonstration in our DSN 2024 paper [P11]
  https://github.com/CMU-SAFARI/SiMRA-DRAM
- CoMeT Simulator: Source code for the evaluation of our HPCA 2024 paper [P18]
  https://github.com/CMU-SAFARI/CoMeT
- RowPress: Source code of the tests and real-system demonstration in our ISCA 2023 paper [P23]
  https://github.com/CMU-SAFARI/RowPress
- CROW Simulator: Source code for the evaluation of our ISCA 2019 paper [P35]
  https://github.com/CMU-SAFARI/CROW
- BlockHammer: Source code for the evaluation of our HPCA 2021 paper [P5]
  https://github.com/CMU-SAFARI/BlockHammer
- SoftMC: The FPGA-based DRAM testing infrastructure, which enabled many works, including [P1–P4, P7, P10, P13–P15, P17, P19, P22–P25, P30, P31, P34, P36, P37, P42]
  https://github.com/CMU-SAFARI/SoftMC
- VAMPIRE: The DRAM power model in our SIGMETRICS 2018 paper [P36]
  https://github.com/CMU-SAFARI/VAMPIRE
- Voltron: Experimental study and analysis of real DRAM chips in our SIGMETRICS 2017 paper [P37]
  https://github.com/CMU-SAFARI/DRAM-Voltage-Study

Service

- Reviewer for HPCA 2026, DSN 2026, ISCA 2026, DRAMSec 2025, TC 2024, DSN 2023, TODAES 2022, and IEEE CAL 2023
- Artifact Evaluation Committee Member for ASPLOS 2024 and DSN 2024
- Organizer of the 1st SAFARI Live Workshop (SaLWo) 2025
- Student Assistant to the PC chairs for DSN 2023
- Subreviewer for ASPLOS 2018, 2022, 2024, and 2025; DSN 2017, 2019, 2020; and 2022; HPCA 2018, 2021 and 2025; ISCA 2017, 2019, 2020; and 2022; MICRO 2017, and 2019-2024; TCAD 2019, 2021, and 2022.

Mentoring Experience

- Ataberk Olgun (PhD student in SAFARI Research Group, 2022 - ongoing)

  - Ataberk Olgun, Majd Osserian, **A. Giray Yağlıkçı**, Yahya Can Tugrul, Haocong Luo, Steve Rhyner, Behzad Salami, Juan Gomez-Luna, and Onur Mutlu, *"Read Disturbance in High Bandwidth Memory: A Detailed Experimental Study on HBM2 DRAM Chips,"* Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN-54), Brisbane, Australia, June 2024. [Slides: ppt | pdf] [Artifact] Officially artifact evaluated as available, reviewed, and reproducible.

- F. Nisa Bostanci (Phd Student in SAFARI Research Group, 2022 - ongoing)
  - F. Nisa Bostanci, Ataberk Olgun, Lois Orosa, **A. Giray Yağlıkçı**, Jeremie S. Kim, Hasan Hassan, Oguz Ergin, and Onur Mutlu, *"DR-STRaNGe: End-to-End System Design for DRAM-based True Random Number Generators,"* International Symposium on High-Performance Computer Architecture (HPCA-28), Virtual, April 2022. [Talk ppt | pdf | video] [Short Talk Slides ppt | pdf]
- İsmail Emir Yuksel (PhD Student in SAFARI Research Group, 2023 - ongoing)
  - İsmail Emir Yuksel, Yahya Can Tugrul, F. Nisa Bostanci, Geraldo F. Oliveira, **A. Giray Yağlıkçı**, Ataberk Olgun, Melina Soysal, Haocong Luo, Juan Gomez-Luna, Mohammad Sadrosadati, and Onur Mutlu, *"Simultaneous Many-Row Activation in Off-the-Shelf DRAM Chips: Experimental Characterization and Analysis,"* Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN-54), Brisbane, Australia, June 2024. [Slides ppt | pdf] [Artifact] Officially artifact evaluated as available, reviewed, and reproducible.
- Haocong Luo (PhD Student in SAFARI Research Group, 2023 - ongoing)
  - Haocong Luo, Ataberk Olgun, **A. Giray Yağlıkçı**, Yahya Can Tugrul, Steve Rhyner, M. Banu Cavlak, Joël Lindegger, Mohammad Sadrosadati, and Onur Mutlu, *"RowPress Vulnerability in Modern DRAM Chips,"* IEEE Micro, Special Issue: Micro's Top Picks from 2023 Computer Architecture Conferences (MICRO TOP PICKS), July/August 2024.
  - Haocong Luo, Ataberk Olgun, **A. Giray Yağlıkçı**, Yahya Can Tugrul, Steve Rhyner, Meryem Banu Cavlak, Joël Lindegger, Mohammad Sadrosadati, and Onur Mutlu, *"RowPress: Amplifying Read Disturbance in Modern DRAM Chips,"* International Symposium on Computer Architecture (ISCA-50), Orlando, FL, USA, June 2023. [Extended arxiv version] [Slides ppt | pdf | video] [Lightning Talk Slides ppt | pdf | video] [Artifact]
    Officially artifact evaluated as available, reusable, and reproducible.
    Distinguished artifact award at ISCA 2023.
    One of the 12 computer architecture papers in Top Picks by IEEE Micro, 2024.
- Oğuzhan Canpolat (Master's student and Intern in SAFARI Research Group, 2023 - ongoing)
  - Oğuzhan Canpolat, **A. Giray Yağlıkçı**, Ataberk Olgun, İsmail Emir Yüksel, Yahya Can Tuğrul, Konstantinos Kanellopoulos, Oğuz Ergin, and Onur Mutlu, *"Chronus: Understanding and Securing the Cutting-Edge Industry Solutions to DRAM Read Disturbance,"* International Symposium on High-Performance Computer Architecture (HPCA-31), to appear, Las Vegas, NV, USA, April 2025.
  - Oğuzhan Canpolat, **A. Giray Yağlıkçı**, Ataberk Olgun, İsmail Emir Yuksel, Yahya Can Tuğrul, Konstantinos Kanellopoulos, Oğuz Ergin, and Onur Mutlu, *"BreakHammer: Enhancing RowHammer Mitigations by Carefully Throttling Suspect Threads,"* International Symposium on Microarchitecture (MICRO-57), to appear, Austin, TX, USA, October 2024. [Poster in FMS'24: ppt | pdf] [Artifact] Officially artifact evaluated as available, functional, and reproduced.
- Yahya Can Tuğrul (Master's student and Intern in SAFARI Research Group, 2023 - ongoing)
  - Yahya Can Tuğrul, **A. Giray Yağlıkçı**, İsmail Emir Yüksel, Ataberk Olgun, Oğuzhan Canpolat, Nisa Bostancı, Mohammad Sadrosadati, Oğuz Ergin, and Onur Mutlu, *"Understanding RowHammer Under Reduced Refresh Latency: Experimental Analysis of Real DRAM Chips and Implications on Future Solutions,"* International Symposium on High-Performance Computer Architecture (HPCA-31), to appear, Las Vegas, NV, USA, April 2025.
- Prithvi Velicheti (Intern in SAFARI Research Group, 2023 - 2024)
  - **A. Giray Yağlıkçı**, Oğuzhan Canpolat, Prithvi Velicheti, Ataberk Olgun, Nisa Bostancı, Andreas Kosmas Kakolyris, İsmail Emir Yüksel,Geraldo F. de Oliveira, and Onur Mutlu, *"High Bandwidth Meets Low Latency: Understanding Access Latency of High Bandwidth Memory via Experimental Analyses Using Real HBM2 DRAM Chips,"* (Blinded).
- Eda Deniz Demirel (Visiting Bachelor Student in SAFARI Research Group, 2024 - ongoing)

– Eda Deniz Demirel, **A. Giray Yağlıkçı**, İsmail Emir Yuksel, Haocong Luo, Ataberk Olgun, Günhan Dündar, and Onur Mutlu, *"A Deeper Look into DRAM Read Disturbance under Unexplored Memory Access Patterns,"* ongoing work for a major conference submission. An early version will appear as a Bachelor's Thesis, Bogazici University, Turkey, 2024.