Abdullah Giray Yağlıkçı

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Up-to-date version of CV is available at https://agyaglikci.github.io/agyaglikci.github

I am a Ph.D. candidate in the Safari Research Group at ETH Zürich, working with Prof. Onur Mutlu. My current broader research interests are in computer architecture, systems, and hardware security with a special focus on DRAM robustness and performance. In particular, my PhD research focuses on understanding and solving the RowHammer vulnerability. I have published several works on this topic in major venues such as HPCA, MICRO, DSN, and ISCA. One of these works, BlockHammer, was named as a finalist by Intel in 2021 for the Intel Hardware Security Academic Award. My RowHammer research is in part supported by Google and the Microsoft Swiss Joint Research Center.

Education

2023 (expected)
PhD in Information Tech. and Electrical Engineering, ETH Zürich
2016
MSc in Computer Science, University of Notre Dame Du Lac (ND)
2014
MSc in Computer Engineering, TOBB University of Economics and Technology
2011
BSc in Electrical Engineering, TOBB University of Economics and Technology

First-Author Publications

HiRA: Hidden Row Activation for Reducing Refresh Latency of Off-the-Shelf DRAM Chips in MICRO 2022

Full Reference: A. Giray Yaglıkcı, Ataberk Olgun, Minesh Patel, Haocong Luo, Hasan Hassan, Lois Orosa, Oguz Ergin, and Onur Mutlu, "HiRA: Hidden Row Activation for Reducing Refresh Latency of Off-the-Shelf DRAM Chips" Proceedings of the 55th International Symposium on Microarchitecture (MICRO), Chicago, IL, USA, October 2022.

We propose a new operation, Hidden Row Activation (HiRA), and the HiRA Memory Controller (HiRA-MC) to perform HiRA operations. HiRA hides a refresh operation's latency by refreshing a row concurrently with accessing or refreshing another row within the same bank. Unlike prior works, HiRA achieves this parallelism without any modifications to off-the-shelf DRAM chips. To do so, it leverages the new observation that two rows in the same bank can be activated without data loss if the rows are connected to different charge restoration circuitry. HiRA reduces the time spent on refresh operations by 51.4%. HiRA-MC increases system performance by 12.6% and 3.73× as it reduces the performance degradation due to periodic refreshes and refreshes for RowHammer protection (preventive refreshes), respectively, for future DRAM chips with increased density and RowHammer vulnerability.

Full Paper: Live Talk Slides: Lecture (36 mins):
rowhammer defense refresh memory dram memory controller subarray parallelism

Understanding RowHammer Under Reduced Wordline Voltage in DSN 2022

Full Reference: A. Giray Yağlıkçı, Haocong Luo, Geraldo F. de Oliveira, Ataberk Olgun, Minesh Patel, Jisung Park, Hasan Hassan, Jeremie S. Kim, Lois Orosa, and Onur Mutlu, **"Understanding RowHammer Under Reduced Wordline Voltage: An Experimental Study Using Real DRAM Devices"** Proceedings of the 52nd Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN), Baltimore, MD, USA, June 2022.

This is the first work to experimentally demonstrate on 272 real DRAM chips that lowering VPP reduces a DRAM chip's RowHammer vulnerability. We show that lowering VPP 1) increases the number of activate-precharge cycles needed to induce a RowHammer bit flip by up to 85.8 % with an average of 7.4 % across all tested chips and 2) decreases the RowHammer bit error rate by up to 66.9 % with an average of

15.2 % across all tested chips. At the same time, reducing VPP marginally worsens a DRAM cell's access latency, charge restoration, and data retention time within the guardbands of system-level nominal timing parameters for 208 out of 272 tested chips. We conclude that reducing VPP is a promising strategy for reducing a DRAM chip's RowHammer vulnerability without requiring modifications to DRAM chips.

Full Paper: | arXiv: | Lightning Talk (2 mins): | Full Talk (34 mins incl. Q&A):

rowhammer | characterization | real chips | memory | dram | voltage | wordline

A Deeper Look into RowHammer in MICRO 2021

Full Reference: Lois Orosa, Abdullah Giray Yağlıkçı, Haocong Luo, Ataberk Olgun, Jisung Park, Hasan Hassan, Minesh Patel, Jeremie S. Kim, and Onur Mutlu, **"A Deeper Look into RowHammer's Sensitivities: Experimental Analysis of Real DRAM Chips and Implications on Future Attacks and Defenses"** Proceedings of the 54th International Symposium on Microarchitecture (MICRO), Virtual, October 2021.

We present an experimental characterization using 248 DDR4 and 24 DDR3 modern DRAM chips from four major DRAM manufacturers demonstrating how the RowHammer effects vary with three fundamental properties: 1) DRAM chip temperature, 2) aggressor row active time, and 3) victim DRAM cell's physical location. Among our 16 new observations, we highlight that a RowHammer bit flip 1) is very likely to occur in a bounded range, specific to each DRAM cell (e.g., 5.4% of the vulnerable DRAM cells exhibit errors in the range 70 °C to 90 °C), 2) is more likely to occur if the aggressor row is active for longer time (e.g., RowHammer vulnerability increases by 36% if we keep a DRAM row active for 15 column accesses), and 3) is more likely to occur in certain physical regions of the DRAM module under attack (e.g., 5% of the rows are 2x more vulnerable than the remaining 95% of the rows). Our study has important practical implications on future RowHammer attacks and defenses. We describe and analyze the implications of our new findings by proposing three future RowHammer attack and six future RowHammer defense improvements.

Full Paper: | arXiv: | Lightning Talk (1.5 mins): | Full Talk (21 mins):

rowhammer | characterization | real chips | memory | dram | temperature | access pattern | spatial variation

BlockHammer: Preventing RowHammer at Low Cost by Blacklisting Rapidly-Accessed DRAM Rows in HPCA 2021

Full Reference: A. Giray Yağlıkçı, Minesh Patel, Jeremie S. Kim, Roknoddin Azizi, Ataberk Olgun, Lois Orosa, Hasan Hassan, Jisung Park, Konstantinos Kanellopoulos, Taha Shahroodi, Saugata Ghose, and Onur Mutlu, **"BlockHammer: Preventing RowHammer at Low Cost by Blacklisting Rapidly-Accessed DRAM Rows,"** in Proceedings of the 27th International Symposium on High-Performance Computer Architecture (HPCA), Virtual, February-March 2021.

In this paper, we show that it is possible to efficiently and scalably prevent RowHammer bitflips without knowledge of or modification to DRAM internals. We introduce BlockHammer, a low-cost, effective, and easy-to-adopt RowHammer mitigation mechanism that prevents all RowHammer bitflips while overcoming the two key challenges: scalability with worsening RowHammer vulnerability and compatibility with commodity DRAM chips. BlockHammer selectively throttles memory accesses that may cause RowHammer bitflips. To our knowledge, this is the first work that prevents RowHammer bitflips efficiently and scalably without knowledge of or modifications to DRAM internals.

Full Paper: | Short Talk (7 mins): | Full Talk (22 mins): | Intel HWSec Academic Awards Talk (2 mins):

rowhammer | defense | throttling | memory | dram | memory controller | hardware

Security Analysis of the Silver Bullet Technique for RowHammer Prevention in arXiv 2021

Full Reference: A. Giray Yağlıkçı, Jeremie S. Kim, Fabrice Devaux, and Onur Mutlu, **""Security Analysis of the Silver Bullet Technique for RowHammer Prevention","** arXiv, 2021.

We mathematically demonstrate that Silver Bullet, when properly configured and implemented in a DRAM chip, can securely prevent RowHammer attacks. The demonstration focuses on the most representative implementation of Silver Bullet, the patent claiming many implementation possibilities not covered in this demonstration. Our study concludes that Silver Bullet is a promising RowHammer prevention mechanism that can be configured to operate securely against RowHammer attacks at various efficiency-area tradeoff points, supporting relatively small hammer count values (e.g., 1000) and Silver Bullet table sizes (e.g., 1.06KB).

Full Paper:

rowhammer defense refresh memory dram on-die hardware

Research Talks

ASP-DAC 2023

Fundamentally Understanding and Solving RowHammer
26 mins | Video: | Slides:

AMLD 2022

Fundamentally Understanding and Solving RowHammer
20 mins | Video: | Slides:

P&S DRAM Bender, ETH Zurich

A Deeper Look into RowHammer's Sensitivities
1 hour | Video: | Slides:

Service

2023
Student Assistant to PC chairs for DSN
Reviewer for DSN

2022
Reviewer for TODAES
Subreviewer for ASPLOS, DSN, ISCA, CAL, DRAMSec, TC, TCAD, and USENIX ATC

2021
Subreviewer for HPCA, MICRO, TCAD, and USENIX ATC

2020
Subreviewer for DSN, ISCA, MICRO, CCS, ISCAS, ISPASS, NVMW, and TCSI

2019
Subreviewer for DSN, ISCA, MICRO, MSST, TCAD, and TED

2018
Subreviewer for ASPLOS, HPCA, PACT, Nature Electronics, TC, and TVLSI

2017
Subreviewer for DSN, MICRO, ISCA, and PLDI

Employment

Feb 2018 - Present
Research and Teaching Assistant - ETH Zürich
Aug 2017 - Feb 2018
Research Intern - Intel Labs Santa Clara
Aug 2016 - Aug 2017
Research Intern - Carnegie Mellon University (CMU)
Aug 2014 - Aug 2016
Research Assistant - University of Notre Dame Du Lac (ND)

Jan 2012 - Aug 2014
Research and Teaching Assistant - TOBB University of Economics and Technology (TOBB ETÜ)
May 2011 - Dec 2011
Electrical Design Engineer - Kasirga Information Systems
May 2010 - Apr 2011
Electrical Design Engineer - Yumruk Space and Defense Industry

Other Publications

Haocong Luo, Ataberk Olgun, A. Giray Yaglikci, Yahya Can Tugrul, Steve Rhyner, M. Banu Cavlak, Joel Lindegger, Mohammad Sadrosadati, and Onur Mutlu, **"RowPress: Amplifying Read Disturbance in Modern DRAM Chips"** Proceedings of the 50th International Symposium on Computer Architecture (ISCA), Orlando, FL, USA, June 2023. Full Paper: Extended Version: Lightning Talk (3 mins): Full Talk (26 mins): Source Code:

Onur Mutlu, Ataberk Olgun, and A. Giray Yağlıkçı, **"Fundamentally Understanding and Solving RowHammer"** Invited Special Session Paper at the 28th Asia and South Pacific Design Automation Conference (ASP-DAC), Tokyo, Japan, January 2023. Full Paper: Recorded Talk (26 mins):

F. Nisa Bostanci, Ataberk Olgun, Lois Orosa, A. Giray Yağlıkçı, Jeremie S. Kim, Hasan Hassan, Oguz Ergin, and Onur Mutlu, **"DR-STRaNGe: End-to-End System Design for DRAM-based True Random Number Generators"** Proceedings of the 28th International Symposium on High-Performance Computer Architecture (HPCA), Virtual, April 2022. Full Paper: Full Talk (24 mins):

Jawad Haj Yahya, Jeremie S. Kim, A. Giray Yağlıkçı, Jisung Park, Efraim Rotem, Yanos Sazeides, and Onur Mutlu, **"DarkGates: A Hybrid Power-Gating Architecture to Mitigate the Performance Impact of Dark-Silicon in High Performance Processors"** Proceedings of the 28th International Symposium on High-Performance Computer Architecture (HPCA), Virtual, April 2022. Full Paper: Slides:

Ataberk Olgun, Minesh Patel, A. Giray Yağlıkçı, Haocong Luo, Jeremie S. Kim, F. Nisa Bostanci, Nandita Vijaykumar, Oguz Ergin, and Onur Mutlu, **"QUAC-TRNG: High-Throughput True Random Number Generation Using Quadruple Row Activation in Commodity DRAM Chips"** Proceedings of the 48th International Symposium on Computer Architecture (ISCA), Virtual, June 2021. Full Paper: Full Talk (25 mins): SAFARI Live Seminar (1hr 26 mins):

Jawad Haj-Yahya, Jeremie S. Kim, A. Giray Yağlıkçı, Ivan Puddu, Lois Orosa, Juan Gomez Luna, Mohammed Alser, and Onur Mutlu, **"IChannels: Exploiting Current Management Mechanisms to Create Covert Channels in Modern Processors"** Proceedings of the 48th International Symposium on Computer Architecture (ISCA), Virtual, June 2021. Full Paper: Full Talk (21 mins):

Jeremie S. Kim, Minesh Patel, A. Giray Yağlıkçı, Hasan Hassan, Roknoddin Azizi, Lois Orosa, and Onur Mutlu, **"Revisiting RowHammer: An Experimental Analysis of Modern Devices and Mitigation Techniques,"** in Proceedings of the 47th International Symposium on Computer Architecture (ISCA), Valencia, Spain, June 2020. Full Paper: Full Talk (20 mins): Lecture (55 mins):

Haocong Luo, Taha Shahroodi, Hasan Hassan, Minesh Patel, A. Giray Yağlıkçı, Lois Orosa, Jisung Park, and Onur Mutlu, **"CLR-DRAM: A Low-Cost DRAM Architecture Enabling Dynamic Capacity-Latency Trade-Off,"** in Proceedings of the 47th International Symposium on Computer Architecture (ISCA), Valencia, Spain, June 2020. Full Paper: Full Talk (20 mins):

Jawad Haj-Yahya, Mohammed Alser, Jeremie Kim, A. Giray Yağlıkçı, Nandita Vijaykumar, Efraim Rotem, and Onur Mutlu, **"SysScale: Exploiting Multi-domain Dynamic Voltage and Frequency Scaling for Energy Efficient Mobile Processors,"** in Proceedings of the 47th International Symposium on Computer Architecture (ISCA), Valencia, Spain, June 2020. Full Paper: Full Talk (17 mins):

Skanda Koppula, Lois Orosa, A. Giray Yağlıkçı, Roknoddin Azizi, Taha Shahroodi, Konstantinos Kanellopoulos, and Onur Mutlu, **"EDEN: Energy-Efficient, High-Performance Neural Network Inference Using Approximate DRAM,"** in Proceedings of the 52nd International Symposium on Microarchitecture (MICRO), Columbus, OH, USA, October 2019. Full Paper: Lecture (38 mins): Lightning Talk:

H. Hassan, M. Patel, J. S. Kim, A. Giray Yağlıkçı, N. Vijaykumar, N. Mansouri Ghiasi, S. Ghose, O. Mutlu, **"CROW: A Low-Cost Substrate for Improving DRAM Performance, Energy Efficiency, and Reliability,"** in Proceedings of the International Symposium on Computer Architecture (ISCA), June 2019. Full Paper: Full Talk: Lightning Talk:

S. Ghose, A. Giray Yağlıkçı, R. Gupta, D. Lee, K. Kudrolli, W. X. Liu, H. Hassan, K. K. Chang, N. Chatterjee, A. Agrawal, M. O'Connor, and O. Mutlu, **"What Your DRAM Power Models Are Not Telling You: Lessons from a Detailed Experimental Study,"** in Proceedings of the ACM International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS), Irvine, CA, USA, June 2018. Abstract: Full Paper: POMACS Journal Version: Slides:

K. Chang, A. Giray Yağlıkçı, S. Ghose, A. Agrawal, N. Chatterjee, A. Kashyap, D. Lee, M. O'Connor, H. Hassan, and O. Mutlu, **"Understanding Reduced-Voltage Operation in Modern DRAM Devices: Experimental Characterization, Analysis, and Mechanisms,"** in Proceedings of the ACM International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS), Urbana-Champaign, IL, USA, June 2017. Abstract: Full Paper: POMACS Journal Version: Slides:

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