TOSHIBA C²MOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TCM9001MD

Dec 12, 2008 **V0.21**

Preliminary

1/10" VGA size Camera Module

Features

General

Input Clock : 9.0 to 26MHz (with PLL, selectable)

Frame rate : 30fps (max.) @VGA output

Data formats : YUV422/RAW **Output format** : Parallel output

2.8V -/+ 0.2V Power supply : Analog

1.8V -/+ 0.1V Digital

I/O 1.8V -/+0.1V or 2.8V -/+0.2V

Operating temperature : -20 to +60 degree C Storage temperature : -30 to +85 degree C

Sensor

 Optical format : 1/10 inch • Effective pixel numbers : 648(H) x 492(V)

• Pixel pitch : 2.2µm(H) x 2.2µm(V) (square pixel) Image area size : $1425.6 \mu \text{ m(H)} \times 1082.4 \mu \text{ m(V)}$

: Primary color filter, Bayer arrangement Color filter

• Image sizer and window of interest (QVGA, QQVGA)

• Picture flip (Horizontal flip and Vertical flip)

• Picture effects (monochrome, negative, sepia, sketch, emboss)

• Fixed output format (VGA, QVGA, QQVGA)

• Auto luminance control (=Auto exposure)

• Auto white balance

• Blemish correction

· Auto flicker detection and correction

Gamma correction

· Lens shading correction

• Power down mode for low power consumption

V0.21 Dec. 12, 2008 1/40

Key Specifications

Item	Contents
Optical format	1/10 inch
Effective pixel numbers	648(H) x 492(V)
Image area size	1425.6 μ m(H) x 1082.4 μ m(V)
Pixel pitch	2.2 μ m(H) x 2.2 μ m(V)
Aspect ratio	4(H): 3(V)
Input clock frequency range	9 to 26 MHz (with PLL, selectable)
Signal output order	Progressive scanning
Color filter	RGB primary color filter
Color filter	Bayer arrangement (G checked, R/B in line sequence)
Output data	YUV422 or RAW parallel output
Frame rate	30fps (max.) @ VGA
Package	Camera Module

Table 1 Key specifications

V0.21 Dec. 12, 2008 2/40

Table of Contents

Featu	ures	1
Gei	neral	1
	nsor	
Key	y Specifications	2
Table	e of Contents	3
1.	List of Abbreviation	5
2.	Block Diagram	
2.1		
2.2	2. I/O circuits	
3.	Pin Layout	8
4.	I ² C Control Interface	
4.1		
4.2	2. Slave address	10
5.	Power supply	11
6.	Input clock frequency	12
6.1	1. Clock setting	12
7.	Frame rate	12
8.	Data Formats	12
_		
9.	Functions	
9.1		
9.2 9.3		
9.3 9.4		
9.5		
9.6	•	
9.7		
9.8	8. Analog gain control	14
9.9	9. White balance	
	10. Auto flicker detection and correction	14
	11. Statistical data output	
	12. Color separation	14
9.1	12. Color separation	14 14
9.1 9.1	12. Color separation	14 14 14
9.1 9.1 9.1	12. Color separation	14 14 14 15
9.1 9.1	12. Color separation	14 14 15 15
9.1 9.1 9.1 9.1	12. Color separation	
9.1 9.1 9.1 9.1 9.1	12. Color separation	
9.1 9.1 9.1 9.1 9.1	12. Color separation	
9.1 9.1 9.1 9.1 9.1 9.1	12. Color separation	
9.1 9.1 9.1 9.1 9.1 9.1 10.	12. Color separation	
9.1 9.1 9.1 9.1 9.1 9.1 10.	12. Color separation	
9.1 9.1 9.1 9.1 9.1 10. 10.	12. Color separation 13. Color matrix 14. Edge enhancement 15. Brightness and contrast 16. Lens shading correction 17. Blemish correction 18. Test charts 19. Test pattern output Timing Chart 11. Power management modes 12. Power on/off sequence 13. Power on sequence (w/ built-in regulator) 14. Power off sequence (w/ built-in regulator)	
9.1 9.1 9.1 9.1 9.1 9.1 10.	12. Color separation	

12	Electrical Characteristics	24
12	2.1. Absolute Maximum Ratings	31
12	2.2. Operating Conditions	31
12	2.3. DC Characteristics	32
12	2.4. AC Characteristics	33
:	12.4.1. EXTCLK input conditions	33
	12.4.2. SDA and SCL	34
:	12.4.3. DATA7 to DATA0, DCLK, HSYNC and VSYNC	35
13.	Reference of Application Circuit	36
14.	Characteristics of Lens	37
15.	Module dimensions	38
16.	Instruction for the Camera Module handling	39
RES	TRICTIONS ON PRODUCT USE	39
Revi	ision History	40

1. List of Abbreviation

Abbreviation	Description
ISP	Image Signal Processor
CDS	Correlated Double Sampling
ADC	Analog to Digital Converter
PLL	Phase Locked Loop
VCO	Variable Controlled Oscillator
PPRO	Pre PROcessor
MPRO	Main PROcessor
APRO	After signal PROcessor
ALC	Auto Luminance Control (≒AE)
AE	Auto Exposure
AF	Auto Focus
UXGA	Ultra XGA (1600 x 1200)
SXGA	Super XGA (1280 x 1024)
Quad VGA	Quad VGA (1280 x 960)
XGA	eXtended Graphics Array (1024 x 768)
SVGA	Super VGA (800 x 600)
VGA	Video Graph Array (640 x 480)
CIF	Common Intermediate Format (352 x 288)
QVGA	Quarter VGA (320 x 240)
QCIF	Quarter CIF (176 x 144)
QQVGA	Quarter Quarter VGA (160 x 120)
subQCIF	subQCIF (128 x96)
Image area	Aperture area of the sensor
Effective pixel area	It is the pixel area that is the signal output is available.

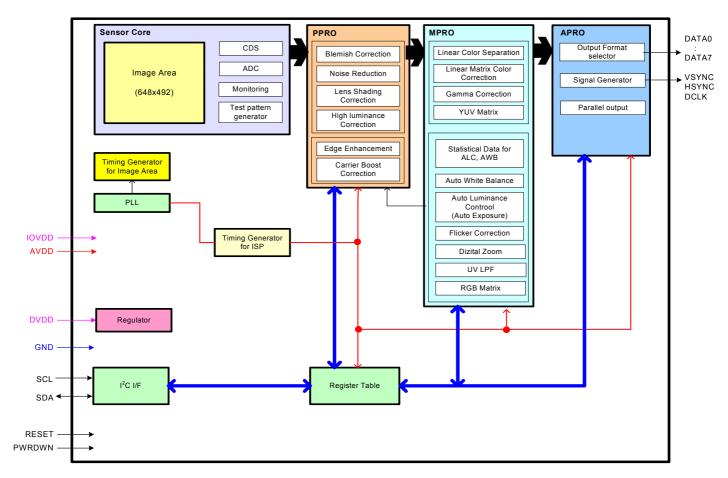
Preliminary

Table 2 Abbreviation

V0.21 Dec. 12, 2008 5/40

2. Block Diagram

2.1. Block Diagram



Some functional blocks, circuits or constants may be omitted or simplified in the block diagram for explanatory purposes.

Figure 1 Block diagram

V0.21 Dec. 12, 2008 6/40

2.2. I/O circuits

Pin No. / Pin name	I/O	Interface circuit
B5: EXTCLK	I	GND 777
C6: PWRDWN	I	GND ##
D3: RESET	I	GND 711 IOVDD
D6: SCL	I	GND ##
C5: SDA	I/O	GND 7 GND
A3: DCLK D1: HSYNC D2: VSYNC B1: DATA1 B2: DATA2 B3: DATA0 B4: DATA3 C1: DATA4 C2: DATA5 C3: DATA6 D4: DATA7	0	IOVDD GND 777

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Table 3 I/O circuits

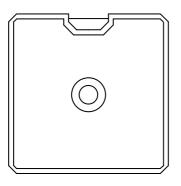
V0.21 Dec. 12, 2008 7/40

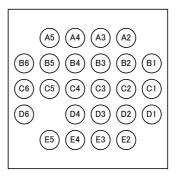
3. Pin Layout

<Top view>

Orientation







Pin No.	Pin name	I/O	Description
A2	IOVDD	-	Power supply for I/O circuits (1.7 to 3.0V)
A3	DCLK	0	Data clock output
A4	GND		System ground
A5	VDD15	-	Capacitor connection for internal regulator
B1	DATA1	0	Image data output 1
B2	DATA2	0	Image data output 2
B3	DATA0	0	Image data output 0
B4	DATA3	0	Image data output 3
B5	EXTCLK	I	External clock input
B6	DVDD	-	Power supply for digital circuits (1.8V -/+ 0.1V)
C1	DATA4	0	Image data output 4
C2	DATA5	0	Image data output 5
C3	DATA6	0	Image data output 6
C4	GND	-	System ground
C5	SDA	I/O	Serial data input/output for I ² C
C6	PWRDWN	I	System power down signal input
D1	HSYNC	0	Horizontal synchronization signal output
D2	VSYNC	0	Vertical synchronization signal output
D3	RESET	I	System reset signal input (Reset = L)
D4	DATA7	0	Image data output 7
D6	SCL	I	Serial data input/output for I ² C
E2	GND		System ground
E3	GND	-	System ground
E4	VDD15	-	Capacitor connection for internal regulator
E5	AVDD	-	Power supply for analog circuits (2.8V -/+ 0.2V)

Install the product correctly. Otherwise, it may result in break down, damage and/or degradation to the product or equipment.

Table 4 Pin description

V0.21 Dec. 12, 2008 8/40

4. I²C Control Interface

TCM9001MD controls interface configuration is based on fast mode I^2C bus. Register setting can be changed via I^2C bus. All register settings are readable via I^2C bus.

4.1. General

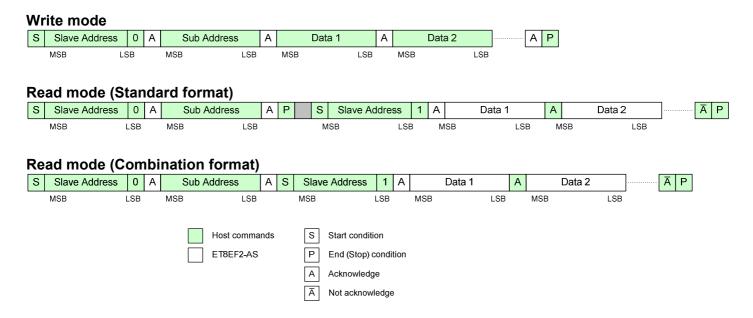


Figure 2 Write/Read mode

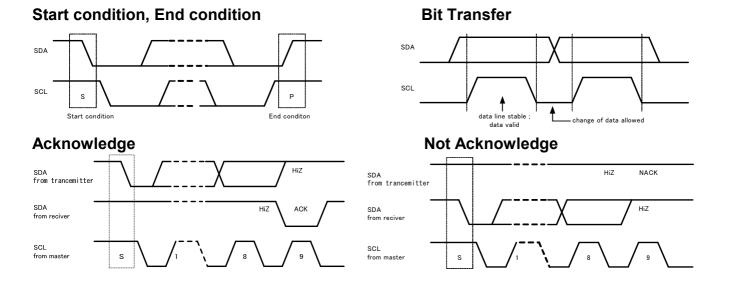


Figure 3 Start/End condition

Note:

The system conforms to the I²C Standard Specification as defined by Philips.

V0.21 Dec. 12, 2008 9/40

4.2. Slave address

TCM9001MD has one address table. Slave address is 7Ch.

W: 7Ch R: 7Dh

Bit	Data
A6	0
A5	1
A4	1
A3	1
A2	1
A1	1
A0	0
R/W	1/0

Table 5 Slave address

V0.21 Dec. 12, 2008 10/40

5. Power supply

TCM9001MD needs two power supplies, 2.8V and 1.8V. 2.8V is for Analog and 1.8V is for the build-in regulator (for Analog and digital circuits). And IOVDD also require a power supply, 1.8V or 2.8V, for I/F.

Pin name	I/O	Description
AVDD	-	Power supply for analog circuits (2.8V -/+ 0.2V)
IOVDD	-	Power supply for I/O circuits (1.8V -/+ 0.1V or 2.8V -/+ 0.2V)
DVDD	-	Power supply for regulator (1.8V -/+ 0.1V)

Table 6 Power supply pins

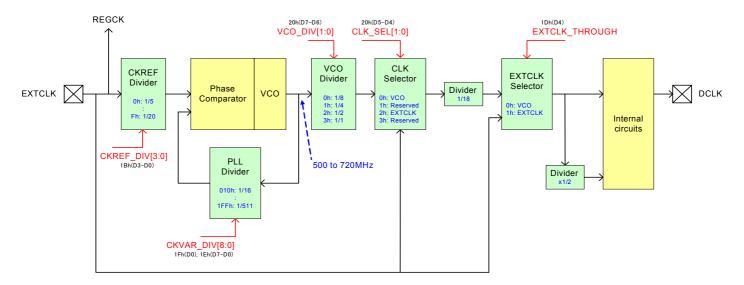
V0.21 Dec. 12, 2008 11/40

6. Input clock frequency

The input clock frequency between 9MHz and 26MHz is acceptable to TCM9001MD.

6.1. Clock setting

The clock system diagram is shown below.



Some functional blocks, circuits or constants may be omitted or simplified in the block diagram for explanatory purposes.

Figure 4 Clock diagram

7. Frame rate

TCM9001MD can operate 30 fps or less in VGA output mode.

8. Data Formats

The following data formats are available. Data format is selectable by I²C commands. The data output supports parallel.

Available parallel output: YUV422 and Raw

V0.21 Dec. 12, 2008 12/40

9. Functions

9.1. Window of interest

The window of interest function enables the user to select a part of the image from the whole image area with specified location (2 pixel step) and specified size (8 pixel step). The available maximum size is 648 x 492 in RAW output or 640 x 480 (VGA) in YUV output mode and the available minimum size is 128 x 96 (subQCIF).

9.2. Image sizer

The image sizer function enables the monitoring (sub sampling) mode on given image with scale factors of 1, 1/2, and 1/4. The available minimum image output is 128×96 (subQCIF). Monitoring (sub sampling) mode has a limited output format.

This function can be used like a zoom function. Digital x2 zoom is available under QVGA or less monitoring operation and digital x2 and x4 zoom is available under QQVGA or less monitoring operation.

9.3. Picture flip

Horizontal and vertical flip modes are controlled by I²C commands. Each flip mode is selectable separately as below.

No.	Mode
0	Original
1	Horizontal flip
2	Vertical flip
3	Vertical and Horizontal flip (180 deg rotation)

Table 7 Flip mode

9.4. Picture effects

The picture effect function supports some kind of pictures with special effects as below. It is controlled by I²C bus commands.

Normal / Monochrome / Negative / Sepia / Emboss / Sketch

9.5. Dynamic range adjustment

Dynamic range adjustment function supports programmable black level adjustment, high luminance level signal compression and others.

9.6. Gamma correction

Gamma correction function supports fixed gamma tables only. Fixed gamma table coefficients are 0.45, 0.55, and 0.65.

V0.21 Dec. 12, 2008 13/40

9.7. Auto luminance control

Auto luminance control (ALC) function is also called Auto Exposure (AE) control. It enables the system to adjust the electrical shutter speed, digital gain and analog gain to adapt to the ambient light automatically to achieve proper brightness of the image. The luminance convergence level, sampling location, EV shift and others can be controlled via I^2C bus. It also has manual mode.

9.8. Analog gain control

Analog gain control is used to adjust the gain of the amplifier of pixel cell. It is often used in dark environment to increase brightness of the image automatically. It also has manual mode.

9.9. White balance

Two modes are available for white balance control under different lighting conditions; manual white balance control and auto white balance control. In manual white balance control mode, it can specify the gain for each color to achieve special effects. In auto white balance control mode, the system supports the gain setting for the white balance based on limit conditions (such as sampling area and range of gain) specified by the user via I^2C bus.

9.10. Auto flicker detection and correction

Auto flicker detection and correction function can correct a fluorescent flicker for both AC 50Hz and 60Hz automatically. However, it is impossible to detect a flicker when shutter speed is faster than 1/100s (Very brighter condition).

9.11. Statistical data output

ALC statistical data are calculated in ISP every frame continuously. The region for calculating is selectable from all area, center only and center weighted mode. The statistical data can be read via I²C bus in read mode. AWB statistical data is also calculated in ISP every frame continuously.

9.12. Color separation

Color separation function separates color from sensor bayer arrangement.

9.13. Color matrix

Color matrix can adjust each color via I²C bus. It can control 6 factors.

9.14. Edge enhancement

Edge enhancement can emphasize edges in an image. It can be set V edge and H edge independently. It also can adjust an enhancement level via I²C bus.

V0.21 Dec. 12, 2008 14/40

9.15. Brightness and contrast

Brightness and Contrast can be adjusted via I²C bus.

9.16. Lens shading correction

The lens shading function can change the pixel gain of off center area to compensate the loss caused by lens shading effect. The correction gain and starting location are programmable across the shading area via I^2C bus. It can be set V and H separately.

9.17. Blemish correction

Blemish correction supports to correct fixed white and black pixels automatically.

9.18. Test charts

For connection test, it has built-in color bar charts, color/grayscale ramp charts and others.

9.19. Test pattern output

For connection test of input/output terminals, it is available to output 1/0 value via I²C bus.

V0.21 Dec. 12, 2008 15/40

10. Timing Chart

10.1. Power management modes

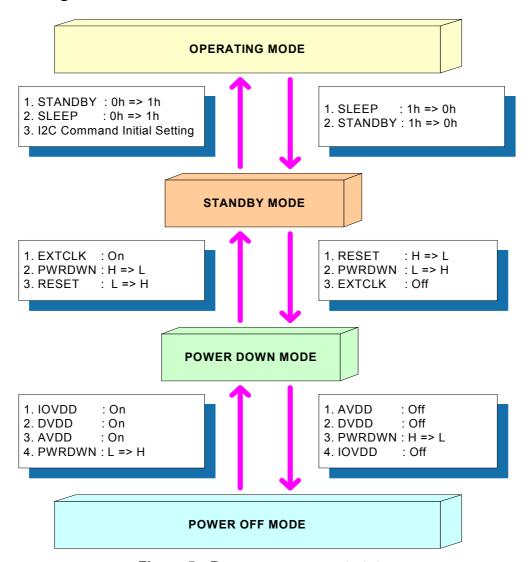


Figure 5 Power management states

Mode	Comment
OPERATING MDOE	All circuits are active.
STANDBY MODE	Internal digital circuits and clock control circuits are Disable for low power consumption while STANDBY and SLEEP registers are set to "0".
POWER DOWN MODE	All power are set. Clock is not provided.
POWER OFF MDOE	All power supplies are turned off .

Table 8 Power management mode

V0.21 Dec. 12, 2008 16/40

10.2. Power on/off sequence

10.2.1. Power on sequence (w/ built-in regulator)

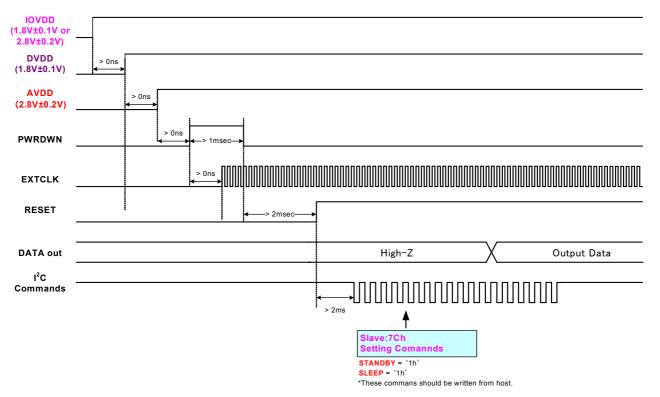


Figure 6.1 Power on sequence (w/ built-in regulator)

10.2.2. Power off sequence (w/ built-in regulator)

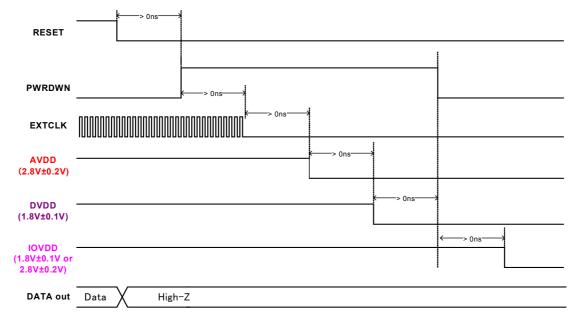
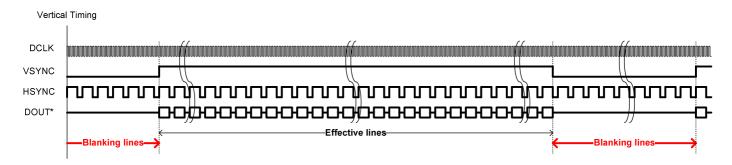


Figure 6.2 Power off sequence (w/ built-in regulator)

V0.21 Dec. 12, 2008 17/40

10.3. Output signal waveform

It can be output DCLK during blanking pulse low. It means DCLK is output continuously.



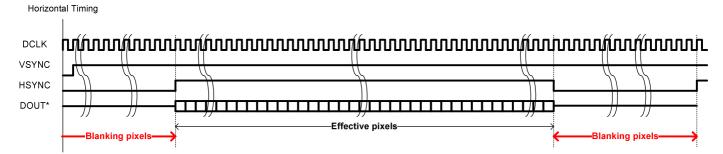


Figure 7 Example of output waveform (VGA output)

V0.21 Dec. 12, 2008 18/40

11. Register descriptions

Slave address = 7Ch/7Dh

Sub	141 00	s = 7Ch/7Dh		Read	
Add. (Hex)	bit	Register name	Description	only or R/W	Default (Hex)
00	D7-0	VER_NUM [7:0]	Chip version identification	R	48
01		VER NUM[15:8]		R	10
02		ALCDATA[7:0]	Shows internal ALC accumulated data. (Lower bits)	R	00
03		ALC_AC5060	Shows internal detection result on Flicker detection. Oh: 50Hz detected 1h: 60Hz detected	R	00
	D6-4	ALC_LES_MODE[2:0]	Shows current LES mode.		
		Reserved	Reserved		
	D1-0	ALCDATA[9:8]	Shows internal ALC accumulated data. (Upper bits)		
04		ALC_AGOUT[7:0]	Shows the analog gain status of ALC. (Lower bits)	R	00
05		Reserved	Reserved	R	00
		ALC_AGOUT[11:8]	Shows the analog gain status of ALC. (Upper bits)		
06		ALC_DGOUT[7:0]	Shows the digital gain status of ALC.	R	00
07		ALC_ESOUT[7:0]	Shows the accumulated number of electrical shutter lines. (Lower bits)	R	00
80	D7-6	Reserved	Reserved	R	00
	D5-0	ALC_ESOUT[13:8]	Shows the accumulated number of electrical shutter lines. (Upper bits)		
09	D7-0	AWB_UOUT[7:0]	Shows the accumulated value of U signal referred as AWB.	R	00
0A	D7-0	AWB_UOUT[15:8]	(Lower bits)	R	00
0B	D7-0	AWB_UOUT[23:16]		R	00
0C	D7-6	Reserved	Reserved	R	00
	D5-0	AWB_UOUT[29:24]	Shows the accumulated value of U signal referred as AWB. (Upper bits)		
0D	D7-0	AWB_VOUT[7:0]	Shows the accumulated value of V signal referred as AWB.	R	00
0E	D7-0	AWB_VOUT[15:8]	(Lower bits)	R	00
0F		AWB_VOUT[23:16]		R	00
10		Reserved	Reserved	R	00
	D5-0	AWB_VOUT[29:24]	Shows the accumulated value of V signal referred as AWB. (Upper bits)		
11	D7-0	AWB_PIXOUT[7:0]	Shows the number of pixels referred as AWB. (Lower bits)	R	00
12	D7-0	AWB_PIXOUT[15:8]		R	00
13	D7-3	Reserved	Reserved	R	00
	D2-0	AWB_PIXOUT[18:16]	Shows the number of pixels referred as AWB. (Upper bits)		
14	D7-0	AWB_RGOUT[7:0]	Shows the R gain for white balance.	R	00
15		AWB GGOUT[7:0]	Shows the G gain for white balance.	R	00
16	D7-0	AWB_BGOUT[7:0]	Shows the B gain for white balance.	R	00
17		Reserved	Reserved	R	00
18	D7	STANDBY	Software standby mode SW	R/W	9C
			0h: Standby 1h: Normal		
	D6-0	Reserved	Reserved		
19		Reserved	Reserved	R/W	04
1A	D7	VCO_STP_X	VCOPLL core SW Oh: Stop 1h: Active	R/W	90
	D6-0	Reserved	Reserved		
1B		Reserved	Reserved	R/W	00
		CKREF_DIV[3:0]	PLL divider control for reference clock (EXTCLK) 0h: 1/5 Fh: 1/20		
1C	D7-0	Reserved	Reserved	R/W	00

V0.21 Dec. 12, 2008 19/40

Sub Add. (Hex)	bit	Register name	Description	Read only or R/W	Default (Hex)
1D	D7-5	Reserved	Reserved	R/W	00
	D4	EXTCLK_THROUGH	EXTCLK through mode to MRCK and SPCK		
			0h: OFF 1h: ON (Through)		
	+	Reserved	Reserved		
1E	D7-0	CKVAR_DIV[7:0]	PLL divider control (Lower bits)	R/W	64
			000h-00Fh: Not available 010h: 1/16 1FFh: 1/511		
1F	D7 1	Reserved	010h: 1/16 1FFh: 1/511 Reserved	R/W	01
''		CKVAR_DIV[8]	PLL divider control (MSB). See Sub-address 1Eh.	I IN/VV	01
20		VCO DIV[1:0]	VCO clock divider control	R/W	C0
	D. 0	100_511[0]	0h: 1/8 1h: 1/4 2h: 1/2 3h: 1		
	D5-4	CLK_SEL[1:0]	Clock SW to MRCK divider		
		, ,	0h: VCO (Normal) 1h: Reserved		
			2h: EXTCLK (for test) 3h: Reserved		
	D3-0	Reserved	Reserved		
21	D7-0	Reserved	Reserved	R/W	0B
22	D7	VFLIP	Vertical flip mode SW	R/W	07
			0h: OFF 1h: ON		
	D6	HFLIP	Horizontal flip mode SW		
			0h: OFF 1h: ON		
		Reserved	Reserved		
	D2-0	HV_INTERMIT[2:0]	Horizontal and vertical resize setting		
	D7.0	LL COUNTIZ-01	0h-2h: x1/4 3h-6h: x1/2 7h: x1	DAM	00
23	D7-0	H_COUNT[7:0]	Total number of horizontal pixels per line, including effective	R/W	96
			and blanking pixels (Lower bits) [Total H-pix / line] = H_COUNT[8:0] x 8		
			000h-095h: Not available		
			096h: 1200 pixels (Default)		
			1FFh: 4088 pixels		
24	D7-1	Reserved	Reserved	R/W	00
	D0	H_COUNT[8]	Total number of horizontal pixels per line, including effective		
			and blanking pixels (MSB) See Sub-address 23h.		
25	D7-0	V_COUNT[7:0]	Total number of vertical lines per frame, including effective	R/W	42
			and blanking lines (Lower bits)		
			[Total V-line / frame] = V_COUNT[10:0] x 8		
			000h-041h: Not available		
			042h: 528 lines (Default)		
200	D7 0	Decemined	7FFh: 16376 lines	DAM	00
26		Reserved V_COUNT[10:8]	Reserved Total number of vertical lines per frame, including effective	R/W	00
	D2-0	V_COUNT[10.0]	and blanking lines (Upper bits) See Sub-address 25h.		
27	D7-0	Reserved	Reserved	R/W	00
28		Reserved	Reserved	R/W	00
29		Reserved	Reserved	R/W	83
2A		Reserved	Reserved	R/W	84
2B		Reserved	Reserved	R/W	AE
2C		Reserved	Reserved	R/W	21
2D	D7-0	Reserved	Reserved	R/W	00
2E	D7-0	Reserved	Reserved	R/W	04
2F	D7-0	Reserved	Reserved	R/W	7D
30		Reserved	Reserved	R/W	19
31		Reserved	Reserved	R/W	88
32		Reserved	Reserved	R/W	88
33		Reserved	Reserved	R/W	09
34	D7-0	Reserved	Reserved	R/W	6C

V0.21 Dec. 12, 2008 20/40

Sub				Read	Default
Add.	bit	Register name	Description	only or	(Hex)
(Hex)	DIC			R/W	(11621)
35	D7-0	Reserved	Reserved	R/W	00
36		Reserved	Reserved	R/W	0C
37		Reserved	Reserved	R/W	22
38		Reserved	Reserved	R/W	0B
39		Reserved	Reserved	R/W	AA
3A		Reserved	Reserved	R/W	0A
3B		Reserved	Reserved	R/W	84
3C		Reserved	Reserved	R/W	03
3D		Reserved	Reserved	R/W	10
3E		Reserved	Reserved	R/W	4C
3F		Reserved	Reserved	R/W	1D
40		Reserved	Reserved	R/W	14
41		Reserved	Reserved	R/W	05
42		Reserved	Reserved	R/W	12
43		Reserved	Reserved	R/W	B0
44		Reserved	Reserved	R/W	3F
45		Reserved	Reserved	R/W	7F
46		Reserved	Reserved	R/W	44
47		Reserved	Reserved	R/W	44
48		Reserved	Reserved	R/W	00
49		Reserved	Reserved	R/W	E8
4A		Reserved	Reserved	R/W	00
4B		Reserved	Reserved	R/W	9F
4C		Reserved	Reserved	R/W	C0
4D		Reserved	Reserved	R/W	24
4E		Reserved	Reserved	R/W	52
4F		Reserved	Reserved	R/W	71
50		Reserved	Reserved	R/W	0E
51		Reserved	Reserved	R/W	00
52 53		Reserved TP MODE[4:0]	Reserved Test pattern collection	R/W	00 0E
55	טו-3	TF_MODE[4.0]	Test pattern selection 00h : Normal 01h-06h : Normal picture + Cross line	R/W	OE
			07h : Reserved 08h : Frame		
			09h-10h : Color-bar		
			11h-17h : Gray scale (with color)		
			18h : Color-bar (Horizontal ramp)		
			19h-1Fh : Horizontal and vertical ramp		
		Reserved	Reserved		
		TPG_LINE_SW	Test pattern of Center cross line 0h: OFF 1h: ON		
54		Reserved	Reserved	R/W	08
55		Reserved	Reserved	R/W	14
56		Reserved	Reserved	R/W	84
57		Reserved	Reserved	R/W	30
58		Reserved	Reserved	R/W	80
59		Reserved	Reserved	R/W	80
5A		Reserved	Reserved	R/W	00
5B		Reserved	Reserved	R/W	06
5C		LINE_RLV[3:0]	Red level setting for Center cross test pattern Oh: Min. Ch-Fh: Max.	R/W	50
	D3-0	Reserved	Reserved		

V0.21 Dec. 12, 2008 21/40

Sub				Read	Default
Add. (Hex)	bit	Register name	Description		Default (Hex)
5D	D7-4	LINE_GLV[3:0]	Green level setting for Center cross test pattern 0h: Min. Ch-Fh: Max.	R/W R/W	A5
	D3-0	Reserved	Reserved		
5E	D7-4	LINE_BLV[3:0]	Blue level setting for Center cross test pattern Oh: Min. Ch-Fh: Max.	R/W	5A
	D3-0	Reserved	Reserved		
5F	D7-0	Reserved	Reserved	R/W	B0
60	D7-0	Reserved	Reserved	R/W	00
61		Reserved	Reserved	R/W	1B
62	D7-0	Reserved	Reserved	R/W	4E
63		Reserved	Reserved	R/W	04
64		LDNR_SW	Random noise reduction SW 0h: OFF 1h: ON	R/W	90
		Reserved	Reserved		
65	D7-0	AGMIN_LDNR_WIDTH[7:0]	Slice level setting for Noise reduction while Analog gain condition is min. (=under high light) 00h: Min. FFh: Max.	R/W	30
66	D7-0	AGMAX_LDNR_WIDTH[7:0]	Slice level setting for Noise reduction while Analog gain condition is max. (=under low light) 00h: Min. FFh: Max.	R/W	30
67	D7-0	AGMIN_LDNR_MP[7:0]	Gain setting for Noise reduction while Analog gain condition is min. (=under high light) 00h: Min. FFh: Max.	R/W	66
68	D7-0	AGMAX_LDNR_MP[7:0]	Gain setting for Noise reduction while Analog gain condition is max. (=under low light) 00h: Min. FFh: Max.	R/W	66
69	D7-0	Reserved	Reserved	R/W	C0
6A		Reserved	Reserved	R/W	30
6B		Reserved	Reserved	R/W	30
6C		Reserved	Reserved	R/W	10
6D		Reserved	Reserved	R/W	30
6E	+	Reserved	Reserved	R/W	AB
6F		Reserved	Reserved	R/W	30
70		AGMIN_BLACK_ADJ[7:0]	Fine setting for Black level while Analog gain condition is min. 00h: Min. FFh: Max.	R/W	80
71	D7-0	AGMAX_BLACK_ADJ[7:0]	Fine setting for Black level while Analog gain condition is max. 00h: Min. FFh: Max.	R/W	80
72	D7-0	IDR_SET[7:0]	Saturation level setting 00h: 100% 55h: 130% FFh: 200%	R/W	55
73	D7-0	PWB_RG[7:0]	Preset WB setting for R pixels 00h: x1 80h: x2 FFh: x3	R/W	00
74	D7-0	PWB_GRG[7:0]	Preset WB setting for Gr pixels 00h: x1 80h: x2 FFh: x3	R/W	04
75	D7-0	PWB_GBG[7:0]	Preset WB setting for Gb pixels 00h: x1 80h: x2 FFh: x3	R/W	04
76	D7-0	PWB_BG[7:0]	Preset WB setting for B pixels 00h: x1 80h: x2 FFh: x3	R/W	62
77	D7-0	Reserved	Reserved	R/W	00
78		LSSC_SW	Lens shading correction SW 0h: OFF 1h: ON	R/W	80
		Reserved	Reserved	_	
79		Reserved	Reserved	R/W	52
7A	D7-0	Reserved	Reserved	R/W	4F

V0.21 Dec. 12, 2008 22/40

Sub				Read	Default	
Add. (Hex)	bit	Register name	Description	only or R/W	(Hex)	
7B	D7-0	LSSC_LEFT_RG[7:0]	R gain on the left side for Lens shading correction 00h: Min. FFh: Max.	R/W	00	
7C	D7-0	LSSC_LEFT_GG[7:0]	G gain on the left side for Lens shading correction 00h: Min. FFh: Max.	R/W	00	
7D	D7-0	LSSC_LEFT_BG[7:0]	B gain on the left side for Lens shading correction 00h: Min. FFh: Max.	R/W	00	
7E	D7-0	LSSC_RIGHT_RG[7:0]	R gain on the right side for Lens shading correction 00h: Min. FFh: Max.	R/W	00	
7F	D7-0	LSSC_RIGHT_GG[7:0]	G gain on the right side for Lens shading correction 00h: Min. FFh: Max.	R/W	00	
80	D7-0	LSSC_RIGHT_BG[7:0]	B gain on the right side for Lens shading correction 00h: Min. FFh: Max.	R/W	00	
81	D7-0	LSSC_TOP_RG[7:0]	R gain on the top side for Lens shading correction 00h: Min. FFh: Max.	R/W	00	
82	D7-0	LSSC_TOP_GG[7:0]	G gain on the top side for Lens shading correction 00h: Min. FFh: Max.	R/W	00	
83	D7-0	LSSC_TOP_BG[7:0]	B gain on the top side for Lens shading correction 00h: Min. FFh: Max.	R/W	00	
84	D7-0	LSSC_BOTTOM_RG[7:0]	R gain on the bottom side for Lens shading correction 00h: Min. FFh: Max.	R/W	00	
85	D7-0	LSSC_BOTTOM_GG[7:0]	G gain on the bottom side for Lens shading correction 00h: Min. FFh: Max.	R/W	00	
86	D7-0	LSSC_BOTTOM_BG[7:0]	B gain on the bottom side for Lens shading correction 00h: Min. FFh: Max.	R/W	00	
87	D7-2	Reserved	Reserved	R/W	01	
	D1-0	LSSC_MP_MODE[1:0]	Gain setting for Lens shading correction Oh: x1/8 1h: x1/4 2h: x1/2 3h: x1			
88	D7-0	Reserved	Reserved	R/W	00	
89	D7-0	Reserved	Reserved	R/W	00	
8A	D7-0	PP_BLACK_ADJ[7:0]	Black level setting after Lens shading correction 00h: Min. FFh: Max.	R/W	40	
8B	D7-0	Reserved	Reserved	R/W	09	
8C	D7-0	Reserved	Reserved	R/W	E0	
8D	D7-0	Reserved	Reserved	R/W	C0	
8E	D7-0	Reserved	Reserved	R/W	80	
8F	D7-0	Reserved	Reserved	R/W	C0	
90	D7-0	Reserved	Reserved	R/W	80	
91		ANR_SW	Noise reduction SW 0h: OFF 1h: ON	R/W	80	
	D6-0	Reserved	Reserved			
92	D7-0	AGMIN_ANR_WIDTH[7:0]	Slice level setting for Noise reduction while Analog gain condition is min.	R/W	80	
93	D7-0	AGMAX_ANR_WIDTH[7:0]	00h: Min. FFh: Max. Slice level setting for Noise reduction while Analog gain condition is max.	R/W	80	
94	D7-0	AGMIN_ANR_MP[7:0]	O0h: Min. FFh: Max. Gain setting for Noise reduction while Analog gain condition is min.		40	
95	D7-0	AGMAX_ANR_MP[7:0]	O0h: Min. FFh: Max. Gain setting for Noise reduction while Analog gain condition is max. O0h: Min. FFh: Max.	R/W	40	
96	D7	DTL_SW	00h: Min. FFh: Max. Edge enhancement SW 0h: OFF 1h: ON	R/W	80	
	D6-0	Reserved	Reserved			
		1 10001 700	1.1000.100		l	

V0.21 Dec. 12, 2008 23/40

Sub Add. (Hex)	Register name Description			Read only or R/W	
97	D7-0	AGMIN_HDTL_NC[7:0]	Coring level setting for Horizontal edge enhancement while Analog gain condition is min. 00h: Min. FFh: Max.	R/W	07
98	D7-0	AGMIN_VDTL_NC[7:0]	Coring level setting for Vertical edge enhancement while Analog gain condition is min. 00h: Min. FFh: Max.	R/W	03
99	D7-0	AGMAX_HDTL_NC[7:0]	Coring level setting for Horizontal edge enhancement while Analog gain condition is max. 00h: Min. FFh: Max.	R/W	07
9A	D7-0	AGMAX_VDTL_NC[7:0]	Coring level setting for Vertical edge enhancement while Analog gain condition is max. 00h: Min. FFh: Max.	R/W	03
9B	D7-0	AGMIN_HDTL_MG[7:0]	Edge enhancement gain setting to Horizontal edges toward black while Analog gain condition is min. 00h: Min. FFh: Max.	R/W	80
9C	D7-0	AGMIN_HDTL_PG[7:0]	Edge enhancement gain setting for Horizontal edges toward white while Analog gain condition is min. 00h: Min. FFh: Max.	R/W	20
9D	D7-0	AGMIN_VDTL_MG[7:0]	Edge enhancement gain setting for Vertical edges toward black while Analog gain condition is min. 00h: Min. FFh: Max.	R/W	40
9E	D7-0	AGMIN_VDTL_PG[7:0]	Edge enhancement gain setting for Vertical edges toward white while Analog gain condition is min. 00h: Min. FFh: Max.	R/W	10
9F	D7-0	AGMAX_HDTL_MG[7:0]	Edge enhancement gain setting for Horizontal edges toward black while Analog gain condition is max. 00h: Min. FFh: Max.	R/W	80
A0	D7-0	AGMAX_HDTL_PG[7:0]	Edge enhancement gain setting for Horizontal edges toward white while Analog gain condition is max. 00h: Min. FFh: Max.	R/W	20
A1	D7-0	AGMAX_VDTL_MG[7:0]	Edge enhancement gain setting for Vertical edges toward black while Analog gain condition is max. 00h: Min. FFh: Max.	R/W	40
A2	D7-0	AGMAX_VDTL_PG[7:0]	Edge enhancement gain setting for Vertical edges toward white while Analog gain condition is max. 00h: Min. FFh: Max.	R/W	10
A3	D7-0	PE_HVDTL_G[7:0]	Edge enhancement gain setting for Picture effect mode. It's valid while PIC_EFFECT = 5h, 6h or 7h. 00h: Min. FFh: Max.	R/W	80
A4		HCBC_SW Reserved	Horizontal carrier boost correction SW Oh: OFF 1h: ON Reserved	R/W	82
A5		AGMIN_HCBC_G[7:0]	Gain setting for Horizontal carrier boost correction while Analog gain condition is min. 00h: Min. FFh: Max.	R/W	55
A6	D7-0	AGMAX_HCBC_G[7:0]	Gain setting for Horizontal carrier boost correction while Analog gain condition is max. 00h: Min. FFh: Max.	R/W	55
A7	D7-0	Reserved	Reserved	R/W	80
A8	D7-0	Reserved	Reserved	R/W	80
A9	D7-0	Reserved	Reserved	R/W	80

V0.21 Dec. 12, 2008 24/40

Sub	Bogistov name		Read	Default	
Add. (Hex)	bit	Register name	Description	only or R/W	(Hex)
AA	D7	LMCC_BMG_SEL	B-G coefficient polarity SW for Color matrix 0h: B-G 1h: G-B	R/W	09
	D6	LMCC_BMR_SEL	B-R coefficient polarity SW for Color matrix 0h: B-R 1h: R-B		
	D5	Reserved	Reserved		
	D4	LMCC_GMB_SEL	G-B coefficient polarity SW for Color matrix 0h: G-B 1h: B-G		
	D3	LMCC_GMR_SEL	G-R coefficient polarity SW for Color matrix 0h: G-R 1h: R-G		
	D2	Reserved	Reserved		
		LMCC_RMB_SEL	R-B coefficient polarity SW for Color matrix Oh: R-B 1h: B-R		
	D0	LMCC_RMG_SEL	R-G coefficient polarity SW for Color matrix 0h: R-G 1h: G-R		
AB	D7-0	LMCC_RMG_G[7:0]	R-G gain setting for Color matrix 00h: x0/256 FFh: x255/256	R/W	04
AC	D7-0	LMCC_RMB_G[7:0]	R-B gain setting for Color matrix 00h: x0/256 FFh: x255/256	R/W	10
AD	D7-0	LMCC_GMR_G[7:0]	G-R gain setting for Color matrix 00h: x0/256 FFh: x255/256	R/W	04
AE	D7-0	LMCC_GMB_G[7:0]	G-B gain setting for Color matrix 00h: x0/256 FFh: x255/256	R/W	08
AF	D7-0	LMCC_BMR_G[7:0]	B-R gain setting for Color matrix 00h: x0/256 FFh: x255/256	R/W	40
В0	D7-0	LMCC_BMG_G[7:0]	B-G gain setting for Color matrix 00h: x0/256 FFh: x255/256	R/W	40
B1	D7-6	GAM_SW[1:0]	Gamma correction SW and gain setting Oh: OFF 1h: 0.65 2h: 0.55 3h: 0.45	R/W	40
	D5-2	Reserved	Reserved		
	D1	YUVM_AWBDISP_SW	AWB test display SW. This register is used with IPIX_DISP_SW=1. Oh: OFF 1h: ON		
	D0	Reserved	Reserved		
B2	D7	Reserved	Reserved	R/W	4D
	D6-0	R_MATRIX[6:0]	R matrix coefficient for Y signal generating Y = (R_MATRIX[6:0] / 256) R + (B_MATRIX[6:0] / 256) B + ((256 - R_MATRIX[6:0] - B_MATRIX[6:0]) / 256) G The value When 00h is as same as one when 01h.		
В3	D7	Reserved	Reserved	R/W	1C
	D6-0	B_MATRIX[6:0]	B matrix coefficient for Y signal generating Y = (R_MATRIX[6:0] / 256) R + (B_MATRIX[6:0] / 256) B + ((256 - R_MATRIX[6:0] - B_MATRIX[6:0]) / 256) G		
B4	D7	UVG_SEL	The value When 00h is as same as one when 01h. UV gain SW 0h: x0.5 1h: x1.0	R/W	C8
	D6	BRIGHT_SEL	Brightness adjusting range SW Oh: -/+127/10bit 1h: -/+1016/10bit	1	
	D5-3	Reserved	Reserved	1	
		PIC_EFFECT[2:0]	Picture effect mode SW		
		10_211201	Oh: Normal 1h: Monochrome		
			2h: Sepia (Mono) 3h: Sepia (Color)		
			4h: Negative 5h: Emboss		
		OONTDACTIT OF	6h: Black board sketch 7h: White board sketch		
B5	ט7-0	CONTRAST[7:0]	Contrast setting for Y signal00h: x0 FFh: x4	R/W	40

V0.21 Dec. 12, 2008 25/40

Sub				Read	Default
Add. (Hex)	bit	Register name	Description	only or R/W	(Hex)
В6	D7-0	BRIGHT[7:0]	Brightness setting for Y signal 00h: -128 80h: -/+0 FFh: +127	R/W	80
B7	D7-0	Reserved	Reserved	R/W	00
B8	D7-0	Reserved	Reserved	R/W	FF
В9	D7-0	U_GAIN[7:0]	Gain setting for U signal U = (B - Y) / 128 x U_GAIN[7:0]	R/W	48
BA	D7-0	V_GAIN[7:0]	Gain setting for U signal V = (R - Y) / 128 x V_GAIN[7:0]	R/W	5B
BB	D7-0	SEPIA_US[7:0]	DC offset level setting for U signal for Sepia effect picture 00h: -128 80h: -/+0 FFh: +127	R/W	78
ВС	D7-0	SEPIA_VS[7:0]	DC offset level setting for V signal for Sepia effect picture 00h: -128 80h: -/+0 FFh: +127	R/W	90
BD	D7-0	U_CORING[7:0]	Coring level setting for U signal (small signal will be compressed) 00h: Min. FFh: Max.	R/W	03
BE	D7-0	V_CORING[7:0]	Coring level setting for V signal (small signal will be compressed) 00h: Min. FFh: Max.	R/W	03
BF	D7	YDTL_SW	Edge enhancement SW for high frequency components of Y signal Oh: OFF 1h: ON	R/W	C0
		UVLPF_SW	LPF SW for UV signals Oh: OFF 1h: ON		
		Reserved	Reserved		
C0	D7-0	YDTL_G[7:0]	Edge enhancement gain setting for high frequency components of Y signal 00h: Min. FFh: Max.	R/W	00
C1	D7-0	Reserved	Reserved	R/W	00
C2		ALC_SW	ALC SW Oh: OFF 1h: ON	R/W	80
		ALC_LOCK	Holds the exposure condition of ALC Oh: OFF 1h: ON (Lock)		
		Reserved	Reserved		
C3	D7-0	MES[7:0]	Manual exposure adjusting (Lower bits). It's valid while ALC_SW = OFF. 0000h: Min. 3FFFh: Max.	R/W	2C
C4	D7-6	Reserved	Reserved	R/W	01
		MES[13:8]	Manual exposure adjusting (Upper bits). See Sub-address C3h.		
C5	D7-0	MDG[7:0]	Manual Digital gain setting 00h: Min. FFh: Max.	R/W	00
C6	D7-0	MAG[7:0]	Manual Analog gain setting (Lower bits). It's valid while ALC_SW = OFF. 000h: Min. FFFh: Max	R/W	20
C7	D7-6	AGCONT_SEL[1:0]	Gain range setting for the changing gains according to AG condition. This setting affects AGMAX/MIN***G registers. Oh: Min. 3h: Max.	R/W	80
		Reserved	Reserved		
	D3-0	MAG[11:8]	Manual Analog gain setting (Upper bits). See Sub-address C6h.		
C8	D7-0	AG_MIN[7:0]	Min. limiter setting for Analog gain for ALC 00h: Min. FFh: Max.	R/W	20
C9	D7-0	AG_MAX[7:0]	Max. limiter setting for Analog gain for ALC 00h: Min. FFh: Max.	R/W	0F

V0.21 Dec. 12, 2008 26/40

Sub					
Add. (Hex)	bit	Register name	Description	only or R/W	Default (Hex)
CA	D7	AUTO_LES_SW	Auto long exposure SW	R/W	03
	D6-4	AUTO_LES_MODE[2:0]	Oh: OFF 1h: ON Time setting for Auto long exposure mode		
	D0-4	AOTO_LLS_WODL[2.0]	Oh: Min. (1V) 4h: Max. (16V)		
			5h-7h: Not available		
	D3-2	ALC_WEIGHT[1:0]	Weighted ALC measuring mode setting		
			0h: All pixels 1h: Central pixels only		
			2h: Not available 3h: Central pixels weighted		
	D1-0	FLCK_ADJ[1:0]	This register should be set according to the frame rate for		
			flicker less condition.		
			0h: Frame rate < 3.75 fps		
			1h: 3.75 =< Frame rate < 7.5 fps 2h: 7.5 =< Frame rate < 15 fps		
			3h: 15 =< Frame rate < 30 fps		
СВ	D7-0	ALC_LV[7:0]	ALC convergence level setting (Lower bits)	R/W	E0
CD	D1-0	ALO_LV[1.0]	000h: Min. 3FFh: Max.	17///	
CC	D7-2	Reserved	Reserved	R/W	11
		ALC_LV[9:8]	ALC convergence level setting (Upper bits) See		
			Sub-address CBh.		
CD	D7-0	ALC_LVW[7:0]	Insensitive range setting for ALC convergence level	R/W	0A
			00h: Min. FFh: Max.		
CE	D7-0	L64P600S[7:0]	Sets the number of lines for 8/100 sec. (for AC 50Hz) or	R/W	99
			8/120 sec (for AC 60Hz) (Lower bits)		
			866h: 2150 Line (Default)		
05	D.7	D I	867h–FFFh: Invalid	D 04/	00
CF		Reserved	Reserved	R/W	06
	D6-4	ALC_VWAIT[2:0]	Waiting time setting to stop ALC for a certain time at condition change		
			Oh: Min. 7h: Max.		
	D3-0	L64P600S[11:8]	Sets the number of lines for 8/100 sec. (Upper bits). See		
		2011 0000[11.0]	Sub-address CEh.		
D0	D7-0	UPDN_SPD[7:0]	ALC convergence speed setting	R/W	80
			00h: Min. FF Max.		
D1	D7-0	Reserved	Reserved	R/W	20
D2	D7-0	NEAR_SPD[7:0]	ALC convergence speed setting near the convergence level	R/W	80
			00h: Min. FF Max.		
D3		Reserved	Reserved	R/W	30
D4	D7	AC5060	Manual setting for AC50/60Hz. While ACFDET = ON, this	R/W	8A
			register is set as the initial AC mode setting for Auto flicker detection.		
			Oh: AC 50Hz mode 1h: AC 60Hz mode		
	D6	Reserved	Reserved		
		ALC_SAFETY[5:0]	Continuous alteration detection period setting to avoid ALC		
	50 0	7.20_0/11 21 1[0.0]	restarting for an instant luminance alternation		
			00h: Min. 3Fh: Max.		
D5	D7-0	Reserved	Reserved	R/W	02
D6	D7-0	Reserved	Reserved	R/W	4F
D7	D7-4	Reserved	Reserved	R/W	08
	D3	ACFDET	Auto flicker detection SW		
			0h: OFF (Manual setting by AC5060)		
			1h: ON (The initial condition is given by AC5060)		
D.*		Reserved	Reserved	5	
D8		Reserved	Reserved	R/W	08
D9		Reserved	Reserved	R/W	FF 01
DA		Reserved	Reserved	R/W	01
DB	D7-0	Reserved	Reserved	R/W	00

V0.21 Dec. 12, 2008 27/40

Sub					Default
Add. (Hex)	bit	Register name	Description	only or R/W	(Hex)
DC	D7-0	Reserved	Reserved	R/W	14
DD		Reserved	Reserved	R/W	00
DE	D7	AWB_SW	Auto white balance SW 0h: OFF 1h: ON	R/W	80
	D6	AWB_LOCK	Holds Auto white balance condition Oh: OFF (AWB active) 1h: ON (AWB freeze)		
		Reserved	Reserved		
DF	D7-0	WB_MRG[7:0]	R gain setting for manual WB 00h: Min. FFh: Max.	R/W	80
E0	D7-0	WB_MGG[7:0]	G gain setting for manual WB 00h: Min. FFh: Max.	R/W	80
E1	D7-0	WB_MBG[7:0]	B gain setting for manual WB 00h: Min. FFh: Max.	R/W	80
E2	D7-0	WB_RBMIN[7:0]	Lower limit gain setting for RB gain on AWB 00h: Min. FFh: Max.	R/W	40
E3	D7-0	WB_RBMAX[7:0]	Upper limit gain setting for RB gain on AWB 00h: Min. FFh: Max.	R/W	FF
E4	D7	HEXA_SW	Hexagonal color detection gate SW Oh: OFF 1h: ON (Hexagonal gate active)	R/W	90
	D6	Reserved	Reserved		
	D5-4	COLGATE_RANGE[1:0]	Range SW for Hexagonal color detection gate setting 0h: 1 pixel/step (total range: -127 to 127 pixels) 1h: 2 pixel/step (total range: -254 to 254 pixels) 2h: 4 pixel/step (total range: -508 to 508 pixels) 3h: 8 pixel/step (total range: -1016 to 1016 pixels)		
	D3-1	Reserved	Reserved		
	D0	COLGATE_OPEN	Opens the color detection gate Oh: OFF (Color gate active) 1h: ON (Opens gate, Color gate setting invalid)		
E5	D7	Reserved	Reserved	R/W	20
		RYCUTM[6:0]	Lower limit level setting for R-Y of Hexagonal color detection gate 00h: Narrowest FFh: Widest		
E6	D7	Reserved	Reserved	R/W	50
	D6-0	RYCUTP[6:0]	Upper limit level setting for R-Y of Hexagonal color detection gate 00h: Narrowest FFh: Widest		
E7	D7	Reserved	Reserved	R/W	38
		BYCUTM[6:0]	Lower limit level setting for B-Y of Hexagonal color detection gate 00h: Narrowest FFh: Widest		
E8	D7	Reserved	Reserved	R/W	20
		BYCUTP[6:0]	Upper limit level setting for B-Y of Hexagonal color detection gate 00h: Narrowest FFh: Widest		
E9	D7-0	RBCUTL[7:0]	Lower cross point on R-Y axis setting for Hexagonal color detection gate 80h: Widest 00h: Center 7Fh: Narrowest	R/W	F0
EA	D7-0	RBCUTH[7:0]	Upper cross point on R-Y axis setting for Hexagonal color detection gate 80h: Narrowest 00h: Center 77h: Narrowest 80h: Narrowest	R/W	18

V0.21 Dec. 12, 2008 28/40

Sub Add. (Hex)	bit	Register name	Description		Default (Hex)
EB	D7	SQ_SW	Square color detection gate SW	R/W R/W	01
		_	0h: OFF 1h: ON		
	D6	SQ_POL	Color detection mode SW for Square color detection gate		
			0h: Subtracts Square gate area from Hexagonal one		
			1h: Adds Square gate area to Hexagonal one		
	D5-1	Reserved	Reserved		
	D0	YGATE_SW	Luminance detection gate SW		
			0h: OFF (Opens gate) 1h: ON		
EC	D7-0	RYCUTL[7:0]	Lower R-Y level setting for Square color detection gate	R/W	00
			80h: Widest 00h: Center 7Fh: Narrowest		
ED	D7-0	RYCUTH[7:0]	Upper R-Y level setting for Square color detection gate	R/W	00
			80h: Narrowest 00h: Center 7Fh: Widest		
EE	D7-0	BYCUTL[7:0]	Lower B-Y level setting for Square color detection gate	R/W	00
			80h: Widest 00h: Center 7Fh: Narrowest		
EF	D7-0	BYCUTH[7:0]	Upper B-Y level setting for Square color detection gate	R/W	00
		<u> </u>	80h: Narrowest 00h: Center 7Fh: Widest		
F0	D7-0	YGATE_L[7:0]	Lower luminance level setting for Luminance detection gate	R/W	30
F4	D7.0	VOATE LITZO	00h: Lowest (Widest) FFh: Highest (Narrowest)	DAM	
F1	D7-0	YGATE_H[7:0]	Upper luminance level setting for Luminance detection gate	R/W	FF
F2	D7.6	Decembed	00h: Lowest (Narrowest) FFh: Highest (Widest)	DAM	00
F2		Reserved	Reserved	R/W	00
	D5	IPIX_DISP_SW	Displays the pixels for AWB accumulation. This register is		
			used with YUVM_AWBDISP_SW=1. 0h: OFF 1h: ON		
	D4-0	Reserved	Reserved		
F3		Reserved	Reserved	R/W	08
' "	—	AWB_U_UPDNLV[4:0]	Coring level setting for Up/Down detection on B gain of	1000	00
	D4-0	AVVB_0_01 BIVEV[4.0]	AWB		
			00h: Low level 1Fh High level		
F4	D7-5	Reserved	Reserved	R/W	08
		AWB V UPDNLV[4:0]	Coring level setting for Up/Down detection on R gain of		
			AWB		
			00h: Low level 1Fh High level		
F5	D7-0	AWB_WAIT[7:0]	Waiting time setting for Auto white balance	R/W	10
		[]	00h: No waiting time		
			80h: 128 frames FEh 254 frames		
			FFh: Not available		
F6	D7-0	AWB_SPDDLY[7:0]	Controls AWB convergence time.	R/W	00
			00h: Short FFh: Long		
F7	D7-6	Reserved	Reserved	R/W	20
	D5-0	AWB_SPD[5:0]	AWB convergence speed setting		
			00h: Slow FFh: Fast		
F8	D7	AWB_HUE_COR	Locks AWB to prevent WB from being unbalance when RB	R/W	86
			gain reach upper or lower limit.		
			0h: OFF 1h: ON		
	D6	Reserved	Reserved		
	D5	AWBSPD_FIX	Fixed AWB convergence speed SW		
			0h: Slower near convergence level		
			1h: Constant speed		
		Reserved	Reserved		
F9		Reserved	Reserved	R/W	00
FA	D7-0	H_START[7:0]	Horizontal picture start position setting	R/W	41
			[H start point] = H_START[7:0] x 2 + 1]	

V0.21 Dec. 12, 2008 29/40

Sub Add. (Hex)	bit	Register name	Description	Read only or R/W	Default (Hex)
FB	D7	Reserved	Reserved	R/W	50
	D6-0	H_WIDTH[6:0]	Horizontal picture size setting [H width] = H_WIDTH[6:0] x 8		
FC	D7-0	V_START[7:0]	Vertical picture start position setting [V start point] = V_START[7:0] x 2 + 1	R/W	0C
FD	D7-6	Reserved	Reserved	R/W	3C
	D5-0	V_HEIGHT[5:0]	Vertical picture size setting [V height] = V_HEIGHT[5:0] x 8		
FE	D7-4	PIC_FORMAT[3:0]	Picture output format setting 0h: Raw-6 (Time shared 10bit) 4h: Raw-8 (Time shared 10bit) 8h: Raw-8 (8bit) 2h, 3h, 6h, 7h, 9h-Fh: Reserved	R/W	50
	D3-0	Reserved	Reserved	1	
FF	D7	SLEEP	Software standby setting. Set this register with STANDBY. 0h: ON (Standby) 1h: OFF (Normal)	R/W	35
	D6	Reserved	Reserved		
	D5-4	PARALLEL_OUTSW[1:0]	Data output test mode SW Oh: Normal 2h: All H 3h: All High-Z		
	D3	DCLK_POL	DCLK output polarity SW Oh: Normal 1h: Inverted		
	D2-0	Reserved	Reserved		

V0.21 Dec. 12, 2008 30/40

12. Electrical Characteristics

12.1. Absolute Maximum Ratings

<u>Items</u>	Symbol	Rating	Unit
Power supply voltage	AVDD DVDD IOVDD	-0.3 to 3.6	>
	DVDD15 AVDD15		V
Input voltage	V _{in}	-0.3 to IOVDD+0.3	
Input current of protection diode	l _{in}	+/- 20	mA
Storage temperature	T _{stg}	-30 to 85	°C

The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant.

If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed.

Moreover, these operations with exceeded ratings may cause break down, damage and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions.

Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in this documents.

12.2. Operating Conditions

Itom	Symbol		Unit		
Item	Symbol	Min.	Тур.	Max.	UIIIL
	AVDD	2.6	2.8	3.0	
	DVDD		1.8	1.9	
Power supply voltage	IOVDD *3	1,7	1.8	1.9	V
		2.6	2.8	3.0	
	DVDD15 *4 AVDD15 *4	1.4	1.5	1.6	
Input voltage	V_{in}	0	-	IOVDD	
Operating temperature *1			°C		
Functional temperature *2	T _{func}		-30 to 70		

Notes:

V0.21 Dec. 12, 2008 31/40

^{*1:} Operating temperature is the temperature range that performance is guaranteed.

^{*2:} Functional temperature is the temperature range that function is guaranteed, however performance is not guaranteed.

^{*3:} The power supply for IOVDD is 1.8V -/+ 0.1V or 2.8V -/+ 0.2V.

^{*4} In case the build-in regulator is not used.

12.3. DC Characteristics

Condition: Ta=25 degree C

AVDD=2.8V, DVDD =1.8V, IOVDD=1.8V

	Items	Symbol	Conditions	Min.	Rating Typ.	Max.	Unit
	DVDD	I _{DVDD NORMAL}	Normani	-	-	30	mA
	IOVDD	${ m I}_{ m IOVDD~NORMAL}$	Normal, 30fps, VGA	-	-	5.1	mA
	AVDD	${ m I}_{\sf AVDD\ NORMAL}$	Julps, VGA	-	-	8	mA
. .	DVDD	I _{DVDD SW STBY}	Standby mode	-	-	500	μΑ
Current	IOVDD	I _{IOVDD} SW STBY	(Software	-	-	50	μΑ
consumption	AVDD	I _{AVDD SW STBY}	standby)	-	-	50	μΑ
	DVDD	$I_{ extsf{DVDD HW STBY}}$	Power down	-	-	10	μΑ
	IOVDD	I _{IOVDD HW STBY}	mode (Hardware	-	-	10	μΑ
	AVDD	I _{AVDD HW STBY}	standby)	-	-	10	μΑ
EXTCLK input voltage (sine wave)*	Peak to peak voltage	$V_{\sf pp\;CLK}$	-	0.5	-	1.2	V
EXTCLK input	Low level input voltage	$V_{\rm IL\;CLK}$	-	-	-	IOVDDx0.2	V
(square wave)	High level input voltage	V _{IH CLK}	-	IOVDDx0.8	-	-	V
	Low level output voltage	V _{OL DOUT}	-	-	-	IOVDDx0.2	V
DATA output	High level output voltage	$V_{OH\;DOUT}$	-	IOVDDx0.8	-	-	V
HSYNC,	Low level output voltage	$V_{OL\ SYNC}$	-	-	-	IOVDDx0.2	V
VSYNC output	High level output voltage	$V_{OH\;SYNC}$	-	IOVDDx0.8	-	-	V
DCLK output	Low level output voltage	V _{OL DCLK}	-	-	-	IOVDDx0.2	V
DCLK output	High level output voltage	V _{OH DCLK}	-	IOVDDx0.8	-	-	V
RESET input	Low level input voltage	$V_{IL\;RESET}$	-	-	-	IOVDDx0.2	V
KESET IIIput	High level input voltage	$V_{IH\;RESET}$	-	IOVDDx0.8	-	-	V
PWRDWN	Low level input voltage	$V_{IL\;PWRDWN}$	-	-	-	IOVDDx0.2	V
input	High level input voltage	$V_{IH\;PWRDWN}$	-	IOVDDx0.8	-	-	V
SCL input	Low level input voltage	$V_{IL\;SCL}$	-	-	-	IOVDDx0.2	V
	High level input voltage	V_{IHSCL}	-	IOVDDx0.8	-	-	V
SDA	Low level input voltage	$V_{IL\;SDA}$	-	-	-	IOVDDx0.2	V
input/output	High level input voltage	$V_{IH\;SDA}$	-	IOVDDx0.8	-	-	V
πρασσατρατ	Low level output voltage	$V_{OL\;SDA}$	-	-	-	0.4	V

^{*}Note:

In case of a sine wave using for EXTCLK, a coupling capacitor is required with the input terminal.

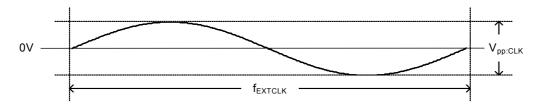
V0.21 Dec. 12, 2008 32/40

12.4. AC Characteristics

12.4.1. EXTCLK input conditions

Items	Symbol	Condition	Min.	Тур.	Max.	Unit
EXTCLK frequency	f _{EXTCLK}	With built-in PLL	9.0	1	26.0	MHz
Fall time	$t_{f;CLK}$	ı	-	-	5	ns
Clock duty	DUTY _{EXTCLK}	-	45/55	-	55/45	%

Table 9 EXTCLK input conditions



Note:

In case of a sine wave using for EXTCLK, a coupling capacitor is required with the input terminal.

Figure 8 EXTCLK waveform (Sine wave)

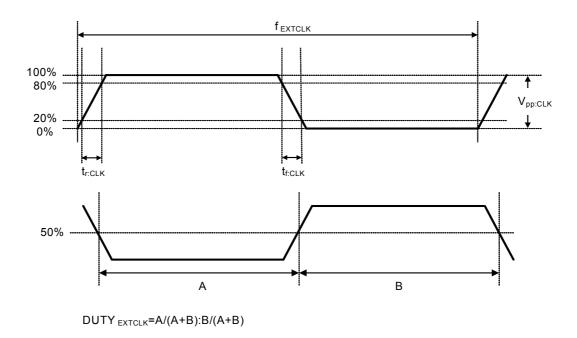


Figure 9 EXTCLK waveform (Square wave)

V0.21 Dec. 12, 2008 33/40

12.4.2. SDA and SCL

Items		Symbol	Min.	Max.	Unit	Notes
	Clock frequency	f _{SCL}	0	400	KHz	
	Low period	t _{LOW;SCL}	1.3	-	μs	
SCL	High period	t _{HIGH;SCL}	0.6	-	μs	
	Rise time	t _{r;SCL}	1	300	ns	
	Fall time	$t_{f;SCL}$	ı	300	ns	
SDA	Rise time	$t_{r;SDA}$	ı	300	ns	
SDA	Fall time	$t_{f;SDA}$	ı	300	ns	*1
Hold time(repeated) START condition After this period, the first clock pulse is generated		t _{HD;STA}	0.6	-	μs	
Setup time for a repeated START condition		t _{SU;STA}	0.6	-	μs	
Data hold time		t _{HD;DAT}	0	-	ns	
Data	t _{SU;DAT}	100	-	ns		
Setup time for STOP condition		$t_{SU;STO}$	0.6	-	μs	
Width of spike pulse	Normal	t_{SP1}	0	50	ns	
	Wake-up from sleep mode	t_{SP2}	0	20	ns	

^{*1)} All values referred to V_{IHmin} and V_{ILmax} levels

Table 10 SDA and SCL

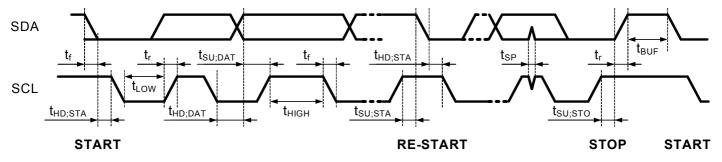


Figure 10 SDA and SCL

V0.21 Dec. 12, 2008 34/40

12.4.3. DATA7 to DATA0, DCLK, HSYNC and VSYNC

Items	Symble	Min.	Max.	Unit	Notes	
DCLK	Rise time	t _{r:DCLK}	ı	6	ns	
DOEK	Fall time	$t_{f:DCLK}$	1	6	ns	
DATA0 to 7	Rise time	$T_{r:DATA}$	ı	6	ns	*1
HSYNC and VSYNC Fall time		$t_{f:DATA}$	ı	6	ns	1
Setup time of data		t _{pd:SU}	10	-	ns	
Hold time of data		t _{pd:HD}	10	-	ns	

^{*1} All values referred to V_{OHmin} and V_{OLmax} levels.

Table 11 DCLK and DATA out

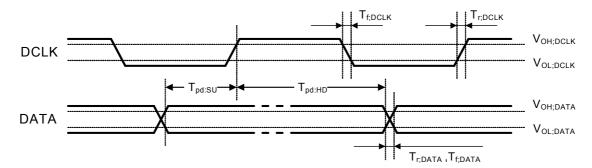


Figure 11 DCLK and DATA out

V0.21 Dec. 12, 2008 35/40

13. Reference of Application Circuit

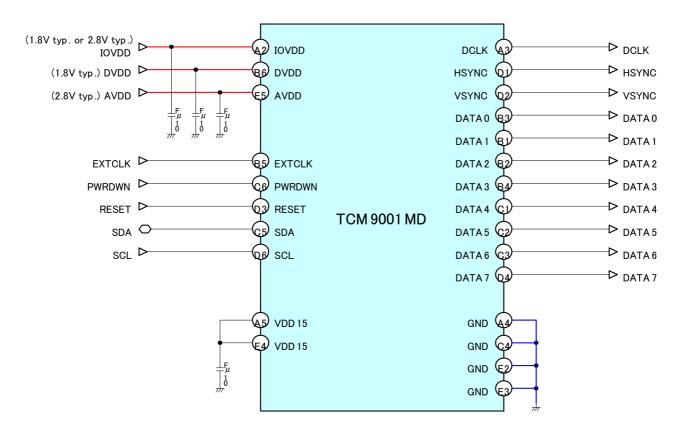


Figure 12 Reference of application circuit

V0.21 Dec. 12, 2008 36/40

14. Characteristics of Lens

Γ	TEM	VALUE	UNITS	
Optical format		1/10	inch	
	Horizontal	1	degree	
Field of view	Vertical	•	degree	
	Diagonal	67.0	degree	
F number		F2.8	-	
TV d	istortion	-0.6	%	
Focal length		1.3546	mm	
Manua	l focusing	Fixed focus	-	
Str	ucture	Doublet lens	-	

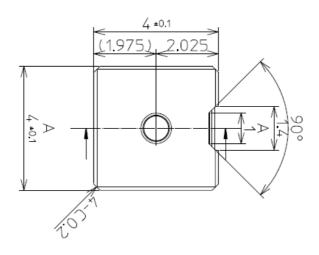
Note: The optical values are obtained by simulation.

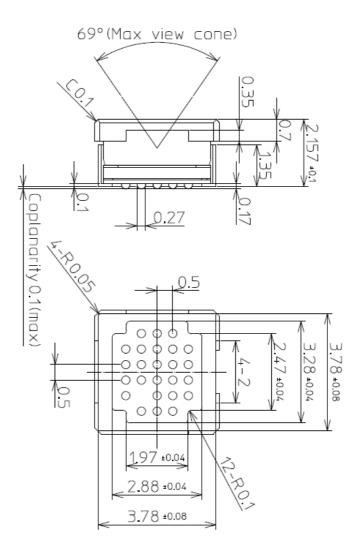
Table 12 Characteristics of Lens

V0.21 Dec. 12, 2008 37/40

15. Module dimensions

Unit: mm





V0.21 Dec. 12, 2008 38/40

16. Instruction for the Camera Module handling

- 1. Use a wrist strap for human body grounding while at work.
- 2. Do not touch the surface of lens with finger or hand to keep the lens clean.
- 3. Do not put stress on the lens block to keep optical performance.
- 5. Do not drop the camera module on the floor which causes breaking and flaw.
- 5. Pick up the edge of lens holder with fingers carefully if it is necessary for the assembly by direct handling.
- 6. Do not expose to strong light, such as the sun for long periods. These will be influence the optical characteristics.

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V0.21 Dec. 12, 2008 39/40

Revision History

Revision Date Comments

Sep 29, 2008 Dec 12, 2008 V0.1 New

Amended the Characteristics of Lens in page 37. Amended the Module dimensions in page 38. V0.21

V0.21 Dec. 12, 2008 40/40