Alexander R. Hankin

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Education

Ph.D Electrical Engineering (expected 2021) — Tufts University, Medford, MA
Adviser: Mark Hempstead — May 2017 - Present

M.S. Electrical Engineering, B.S. Computer Engineering — Tufts University, Medford, MA
Adviser: Mark Hempstead — September 2012 – May 2017

Publications

Accepted, pending publication

A. Hankin, T. Shapira, K. Sangaiah, M. Lui, M. Hempstead. Evaluation of Non-Volatile Memory Based Last Level Cache Given Modern Use Case Behavior. IEEE International Symposium on Workload Characterization (IISWC). 12 pages. Nov 3-5, 2019.

Research

Distributed Architecture for Mitigating Hotspots in Modern Chips — January 2019 – Present
Ph.D Dissertation
Funding: Google, Intel

- Drafting survey of hotspot mitigation techniques in the literature (packaging, architectural, and software based). Developing performance, power, and thermal simulation infrastructures for the target modern chip architectures. Will implement novel distributed architecture for mitigating hotspots in said chips and compare to existing techniques in the literature for different target use case behaviors

Non-Volatile Memory (NVM) Based Last Level Cache (LLC) — June 2016 – Present
M.S. research that was continued

- Evaluating NVM based LLC for Neural Networks (paper being developed)
- Conducted workload characterization study of NVM based LLC workloads including artificial intelligence workloads (led to publication). Collaborated with researchers at Drexel University.
- Conducted architectural simulations and analyzed trade-offs in performance, power, and area between many NVM based LLCs (Phase Change RAM, Spin-Torque Transfer RAM, Resistive RAM, and SRAM baseline)
- Developed NVM based LLC software models and toolchain for end-to-end architecture simulation and am releasing to the public with the publication

Industry

Google Inc. — January 2019 – July 2019
Mountain View, CA

- Hardware Engineering Intern
- Host: Qiuling (Jolin) Zhu. Co-Host: Andrea Di Blas

- Developed performance and power models of Image Signal Processing (ISP) kernel pipeline and neural network algorithm on processing elements in low-power, ambient computing processor
  - Developed general automated simulation flow for going from application code plus system RTL to detailed performance and power estimation
    - Ported C++ code to custom DSPs
    - Implemented scripts for compilation, linking, RTL simulation, and PrimeTime PX power simulation
    - Analyzed trade-offs in performance and power of image processing algorithms, especially ISP kernels, and deep learning algorithms on different processing elements using said developed flow
- Conducted memory optimization study for mobile image processing/machine learning accelerator (Pixel Visual Core)
  - Implemented caching hardware in a full-system simulator (implemented in C++/SystemC)
  - Analyzed trade-offs in performance and power across different caching architectures to determine optimal architecture for target use case memory access patterns

Teaching

Teaching assistant for the following computing courses at Tufts University in Department of Electrical and Computer Engineering (Fall 2017, Spring 2018, Fall 2018):

- Machine-centric Approach Programming (AKA Accelerated Programming for Graduate students)
- Advanced Computer Architecture
- Computer Organization and Design

Awards

Tufts University, Medford, MA
- Combined B.S. and M.S. degree program
- Dean's List 2 semesters
- Minor degree in Mathematics

Academic Activities

Tufts University, Medford, MA
- Undergraduate Admissions Interviewer
- Engineering Mentor for Undergraduates
- IEEE E-Board

IEEE student member

References

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Tufts University
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Additional references available upon request.