Cryogenic Classical Control System Architecture for Superconducting Quantum Computation

ABSTRACT

1. FRAMEWORK OVERVIEW

Of the various hardware implementations proposed to facilitate quantum computation, superconducting qubits have been gaining traction and popularity, as these systems benefit from solid state material implementations, and can leverage pre-existing research and tools surrounding planar electronic fabrication techniques.

To perform quantum computation with superconducting quantum circuitry, the entire system must be cooled to far below typical critical temperature for superconducting metals, so as to reduce external environment interference with the quantum device as much as possible. Dilution refrigerators are the current technology of choice required to perform this cooling, which presents a novel set of design constraints concerning electronic control system integration in such a system.

Typical dilution refrigerators cool materials in stages, proceeding from room temperature, to several intermediate stages, ultimately resulting in a small zone that arrives at the desired temperature. The temperature regions typically accessed along the cooling path are described in Figure 1 and ultimately utilize regions cooled to approximately 100K, 4K, along with a final region at the target 20mK temperature.

In such a system, wiring control signals to the supercooled quantum processor presents a series of design constraints. Namely, wiring the quantum processor to room temperature control electronics subjects the system to large thermal loads, difficult isolation from interference, large latency penalties, and lack of scalable compactness . To address these issues, classical control units can be located at one (or more) temperature level(s) of dilution refrigerator-based superconducting quantum computers. In moving to a system architecture involving internal classical control hardware, a series of tradeoffs is presented involving thermal computation costs and hardware constraints governing memory construction.

1.1 Dilution Refrigerator Constraints

The architecture of a dilution refrigerator being considered is a multi-stage cooling apparatus, using liquid nitrogen and liquid helium. Of interest right now are two characteristics: cooling capacity of temperature stages and latency of microwave links crossing these thermal boundaries. Using information from the specifications of a typical refrigerator (BlueFors XLD), these temperature levels and cooling capacities are shown in Table 1.

Temperature Zone	Capacity	Power Overhead
45K	40W	10X
4K	1.5W	200X
120mK	600μW	
100mK	400μW	
20mK	14 μW	50,000X

Table 1: Temperature Levels and Cooling Capacities

Additionally, there is a range of latencies introduced in passing microwave links through temperature interfaces. These seem to vary between 1-10ns approximately, growing longer as the gap widens between the target temperatures of the stages being crossed.

1.2 Hardware Characteristics

There are three primary types of hardware under consideration:

- RSFQ: Rapid Single Flux Quantum
- RQL: Reciprocal Quantum Logic
- CryoCMOS: Cryogenic CMOS

Each of these is characterized by a different energy usage to logic gate relationship. These values are typically characterized similarly to Table 2.

Hardware Type	Energy Required Per Gate (Joules)
RSFQ	10^{-19}
RQL	10^{-19}
CryoCMOS	10^{-15}

Table 2: Hardware Types and Energy Consumed Per Gate

It is also important to consider power consumption of memory systems under these types of conditions. Here, we will analyze power usage of cryogenic CMOS memory devices, and consider implementations of cryogenic persistent memory systems. Persistent memory could

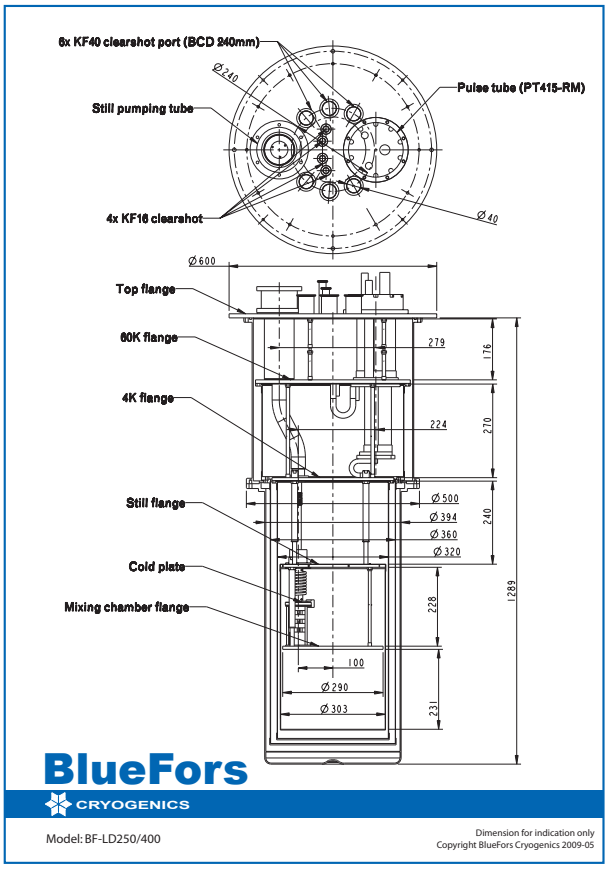

Figure 1: Dilution Refrigerator Schematic

potentially be useful in applications that rely upon a precomputed library of rotation decompositions, as memory may only need to be read only for long periods of computation. The qualification is that different applications often require different levels of precision in rotation decompositions, so these databases would potentially need to be changed between apps.

1.3 Classical Control Unit

An accurate model of a classical control system for a superconducting quantum processor contained within a dilution refrigerator is that of an instruction cache that requests code modules contained within an external memory. Code modules are compressed, transmitted to the microcontroller, decompressed and executed.

2. PROGRAM CODE GENERATION AND COMPILER OPTIMIZATIONS

A unique characteristic of quantum programs is a large amount of static compilation. Knowing this, quantum programs can be compiled in advance, and large amounts of optimization can be performed. Of interest to systems under the aforementioned hardware constraints are the tradeoffs between code flattening, parallelism extraction, and generated code size.

Due to the size of some large quantum programs, full code flattening for parallelism extraction can be rendered intractible or infeasible, given classical compiler resource constraints. Additionally, selectively flattening large quantum programs can generate flattened code modules of different size distributions, and will extract varying levels of parallelism from the application altogether. Of interest to this study is the application of specific flattening mechanisms, the parallelism that these mechanisms are able to extract, and the tradeoffs present within extracting this parallelism at the cost of a specific flattened module size distribution. One flattening mechanism may extract large amounts of parallelism, but may create modules of sizes that generate poor caching behavior by the classical control units located within the cryogenic system.

3. COMPRESSION TECHNIQUES

4. HARDWARE SCHEDULING TECHNIQUES

5. REFERENCES