Ali Hajiabadi

Postdoctoral Researcher
ETH Zürich

Contact Information

Address: ETZ G 78.2, Gloriastr. 35, 8092 Zürich, Switzerland
Email: ahajiabadi@ethz.ch
Homepage: ahajiabadi.github.io

Research Interests

Systems Security, Hardware/Software Co-design, Computer Architecture, Optimizing Compilers, Formal Methods, Trusted Execution Environments, Microarchitectural Attacks and Side Channels

Education

2019 - 2024 Doctor of Philosophy in Computer Science
National University of Singapore (NUS), Singapore
Thesis: *"Building Efficient and Secure Processors thorugh Hardware/Software Co-design"*
Advisor: Dr. Trevor E. Carlson

2014 - 2019 Bachelor of Science in Computer Engineering
Sharif University of Technology, Tehran, Iran
Thesis: *"High Concurrency Latency Tolerant Register Files for GPUs"*
Advisor: Dr. Hamid Sarbazi-Azad

2009 - 2013 Diploma in Physics and Mathematics Discipline
Shahid Beheshti High School, Birjand, Iran
Affiliated with the National Organization for the Development of Exceptional Talents (NODET)

Professional Experience

Jul. 2024 - Present | Postdoctoral Researcher at ETH Zürich, Switzerland
Computer Security (COMSEC) Group
Group Lead: Dr. Kaveh Razavi
Research: CPU and DRAM security, novel attacks and defenses for modern computing systems

Aug. 2019 - Jun. 2024 | Graduate Research Assistant at National University of Singapore, Singapore
NUS Computer Architecture (CompArch) Group
Group Lead: Dr. Trevor E. Carlson
Research: hardware/software co-design for efficient and secure modern processors

Jul. 2016 - Jun. 2019 | Research Assistant at Sharif University of Technology, Tehran, Iran
High Performance Computer Architectures and Networks (HPCAN) Lab
Group Lead: Prof. Hamid Sarbazi-Azad
Research: GPU register prefetching via HW/SW co-design and compiler optimizations

Summer 2018 | Research Intern at National University of Singapore, Singapore
Group Lead: Prof. Trevor E. Carlson
Research: exploring new implementations for out-of-order commit processors

Honors & Awards

Aug. 2024 Dean's Graduate Research Excellence Award (AY2023/2024).
Jul. 2024 School of Computing CS PhD Thesis Award (Honorable Mention), selected as top five theses.
Jun. 2024 Best Paper Award nomination at DAC '24.
Oct. 2023 Recipient of SoC Research Incentive Award from School of Computing, NUS (S$ 2,500 award).
Jan. 2022 Recipient of Student Travel Award from ASPLOS'22 conference.
Aug. 2021 Recipient of Research Achievement Award from School of Computing, NUS.
Mar. 2020 Invited talk and travel grant for the 2^{nd} Young Architect Workshop at ASPLOS'20, Switzerland.
Feb. 2019 Recipient of President's Graduate Fellowship, the most prestigious doctoral fellowship at National University of Singapore (NUS).

SEP. 2014 Ranked **164**th in Iranian National University Entrance Exam among more than 250,000 students.
2006/2009 Recognized as talented student in entry exam of NODET for middle school and high school.

IN-PROGRESS WORK

Ali Hajiabadi, Trevor E. Carlson
Providing High-Performance Execution with a Sequential Contract for Cryptographic Programs.
▶ *A hardware/software mechanism to protect constant-time cryptographic programs against Spectre-type attacks via disabling the branch predictor and redirecting fetch based on a strong and sequential security contract.*
arXiv Paper

Yun Chen*, **Ali Hajiabadi***, Romain Poussier, Andreas Diavastos, Shivam Bhasin, Trevor E. Carlson
Mitigating Power Attacks through Fine-Grained Instruction Reordering.
∗Joint first-authors with equal contribution.
▶ *Proposing a novel criticality-aware and non-deterministic instruction scheduling for out-of-order processors to resist power analysis attacks.*
arXiv Paper

PEER-REVIEWED PUBLICATIONS

DAC'24 | **Ali Hajiabadi**, Trevor E. Carlson
CONJURING*: Leaking Control Flow via Speculative Fetch Attacks.*
Proceedings of 61st ACM/IEEE Design Automation Conference (DAC 2024), June 2024. Acceptance rate: 337/1465 = 23.0%
★ *Best Paper Award Nominee* (5/337 = 1.5%)
▶ *Proposing a new and practical variant of speculative fetch attacks that enables unprivileged attackers to leak control flow information of victims, without requiring priming a side channel.*

DAC'24 | **Ali Hajiabadi**, Archit Agarwal, Andreas Diavastos, Trevor E. Carlson
LEVIOSO*: Efficient Compiler-Informed Secure Speculation.*
Proceedings of 61st ACM/IEEE Design Automation Conference (DAC 2024), June 2024. Acceptance rate: 337/1465 = 23.0%
▶ *Efficient and comprehensive mitigation for speculative execution attacks through compiler-informed hints about true branch dependencies to restrict execution of speculative instructions only if necessary.*

HPCA'24 | Yun Chen*, **Ali Hajiabadi***, Trevor E. Carlson
GADGETSPINNER*: A New Transient Execution Primitive using the Loop Stream Detector.*
Proceedings of 30th IEEE International Symposium on High-Performance Computer Architecture (HPCA 2024), March 2024. Acceptance rate: 75/410 = 18.3%
∗Joint first-authors with equal contribution.
▶ *Analyzing and discovering vulnerabilities of the Loop Stream Detector (LSD) in Intel CPUs that enables cross-core transient execution attacks without requiring branch mistraning/poisoning.*
Paper | Artifact

HPCA'24 | Yun Chen, **Ali Hajiabadi**, Lingfeng Pei, Trevor E. Carlson
PREFETCHX*: Cross-Core Cache-Agnostic Prefetcher-Based Side-Channel Attacks.*
Proceedings of 30th IEEE International Symposium on High-Performance Computer Architecture (HPCA 2024), March 2024. Acceptance rate: 75/410 = 18.3%
▶ *Extensive reverse-engineering of an undocumented Intel prefetcher, called XPT (an LLC miss predictor) that enables cross-core cache-agnostic side and covert channels.*
Paper | Artifact

ICCAD'23 | Arash Pashrashid, **Ali Hajiabadi**, Trevor E. Carlson
HIDFIX*: Efficient Mitigation of Cache-based Spectre Attacks through Hidden Rollbacks.*
Proceedings of 42nd IEEE/ACM International Conference on Computer-Aided Design (ICCAD 2023), November 2023. Acceptance rate: 172/768 = 22.4%
▶ *Co-designing detection and mitigation to defend cache-based Spectre with no performance overhead; extensive study of existing detection/mitigation combinations and proposing attacks to bypass them.*
Paper

ICCAD'22 | Arash Pashrashid, **Ali Hajiabadi**, Trevor E. Carlson
Fast, Robust and Accurate Detection of Cache-based Spectre Attack Phases.
Proceedings of 41st IEEE/ACM International Conference on Computer-Aided Design (ICCAD 2022), November 2022. Acceptance rate: 132/586 = 22.5%
▶ *(1) Demonstrating different attacks bypassing ML-based detectors for Spectre attacks; (2) proposing an efficient, accurate, robust, and timely mechanism to detect cache-based Spectre attack phases.*
Paper | Github

ASPLOS'21 | **Ali Hajiabadi**, Andreas Diavastos, Trevor E. Carlson
NOREBA: *A Compiler-Informed Non-speculative Out-of-Order Commit Processor*.
Proceedings of 26^{th} ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2021). April 2021. Acceptance rate: 75/398 = 18.8%
▶ *A hardware/software co-design that compiler informs the hardware about true branch dependencies enabling safe and non-speculative out-of-order commit of instructions improving efficiency.*
Paper | Extended Abstract | Short Slides | Short Talk | Slides | Full Talk

TOCS'21 | Mohammad Sadrosadati, Amirhossein Mirhosseini, **Ali Hajiabadi**, Seyed Borna Ehsani, Hajar Falahati, Hamid Sarbazi-Azad, Mario Drumond, Babak Falsafi, Rachata Ausavarungnirun, Onur Mutlu
Highly Concurrent Latency-tolerant Register Files for GPUs.
In ACM Transactions on Computer Systems (TOCS), 2021.
▶ *A hardware/software co-operative design for register prefetching in GPUs. The compiler constructs the prefetch sets and ensures minimal register bank conflicts via register renumbering.*
arXiv Paper

CGO'21 | Harish Patil, Alexander Isaev, Wim Heirman, Alen Sabu, **Ali Hajiabadi**, Trevor E. Carlson
ELFies: Executable Region Checkpoints for Performance Analysis and Simulation.
Proceedings of 19^{th} IEEE International Symposium on Code Generation and Optimization (CGO 2021), March 2021. Acceptance rate: 31/89 = 34.8%
▶ *Proposing a set of tools to generate checkpoint executables of the regions of interest of applications, called ELFies. ELFies run natively and can be used for detailed analysis in other tools and simulators.*
Paper | Github

TEACHING EXPERIENCE

▶ **ETH Zürich, Switzerland**

FALL 2024 — **Teaching Assistant**
Course: BSc Computer Engineering
Instructor: Prof. Kaveh Razavi

▶ **National University of Singapore, Singapore**

SPRING 2020 and SPRING 2021 — **Teaching Assistant**, Tutorial Instructor
Course: CS2106 Introduction to Operating Systems
Instructor: Prof. Djordje Jevdjic

▶ **Sharif University of Technology, Tehran, Iran**

SPRING 2017 — **Teaching Assistant**, Assignments/Projects Assistant
Course: CE323 Computer Architecture
Instructor: Prof. Hamid Sarbazi-Azad

FALL 2017 and FALL 2018 — **Teaching Assistant**, Tutorial Instructor, Assignments/Projects Assistant
Course: CE453 Real-Time Systems
Instructor: Prof. Amirhossein Jahangir

SERVICES

NOV. 2023 — **Heavy Shadow PC member** at 19^{th} European Conference on Computer Systems (EuroSys 2024).
OCT. 2022 — **Shadow PC member** at 18^{th} European Conference on Computer Systems (EuroSys 2023).
MAR. 2022 — **Mentor in the Meet-a-Senior-Student program** at 27^{th} International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2022), Lausanne.
JUN. 2021 — **Student Volunteer** at 42^{nd} International Conference on Programming Language Design and Implementation (PLDI 2021), Virtual.

RESEARCH MENTORING

2020 - 2024 — Yun Chen, PhD Student at NUS Advised by Trevor E. Carlson
2021 - 2023 — Arash Pashrashid, PhD Student at NUS Advised by Trevor E. Carlson
2021 - 2023 — Archit Agarwal, Research Assistant at NUS
2020 - 2021 — Vernon Pang, Undergraduate Student at NUS

TALKS

MAR. 2024 — **Will CPUs Be Free of Spectre? Dark Side and Light Side of the Battle**
ETH Zürich, COMSEC Group, Zürich, Switzerland.
MAR. 2024 — GADGETSPINNER: **A New Transient Execution Primitive using the Loop Stream Detector**
Int. Symposium on High-Performance Computer Architecture (HPCA 2024), Edinburgh, Scotland.

Aug. 2021 Noreba: **A Compiler-Informed Non-speculative Out-of-Order Commit Processor**
Computing Research Week, School of Computing (NUS), Virtual.

Apr. 2021 Noreba: **A Compiler-Informed Non-speculative Out-of-Order Commit Processor**
Int. Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2021), Virtual.

Feb. 2021 **Accelerating HPC applications with Out-of-Order Commit Processors**
Free and Open source Software Developers' European Meeting (FOSDEM 2021), HPC, Big Data, and Data Science track, Virtual.

Mar. 2020 **Speculation-Free Out-of-Order Commit**
2^{nd} Young Architect Workshop at the 25^{th} International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2020), Virtual.

Skills

Programming Languages:	C, C++, Python, bash, and familiar with Java, Matlab, Scala
Instruction Set Architectures:	x86, Arm, RISC-V
Scientific Tools:	LLVM Compiler Infrastructure, gem5 Simulator, Sniper Simulator, Intel Pin, DynamoRIO
Typesetting:	LaTeX, Microsoft Word