

Ali HAJIABADI

Postdoctoral Researcher and Lecturer
ETH Zürich

CONTACT INFORMATION

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RESEARCH INTERESTS

Systems Security, Hardware/Software Co-design, Computer Architecture, Optimizing Compilers, Formal Methods, Secure Architectures and Software, Microarchitectural Side Channels, Trusted Execution Environments

EDUCATION

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- 2019 - 2024 Doctor of Philosophy in Computer Science
National University of Singapore (NUS), Singapore
Thesis: "*Building Efficient and Secure Processors thorough Hardware/Software Co-design*"
Advisor: Prof. Trevor E. CARLSON
- 2014 - 2019 Bachelor of Science in Computer Engineering
Sharif University of Technology, Tehran, Iran
Thesis: "*High Concurrency Latency Tolerant Register Files for GPUs*"
Advisor: Prof. Hamid SARBAZI-AZAD
- 2009 - 2013 Diploma in Physics and Mathematics Discipline
Shahid Beheshti High School, Birjand, Iran
Affiliated with the National Organization for the Development of Exceptional Talents (NODET)

HONORS & AWARDS

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- AUG. 2024 DEAN'S GRADUATE RESEARCH EXCELLENCE AWARD.
- JUL. 2024 SCHOOL OF COMPUTING CS PHD THESIS AWARD (Honorable Mention), selected as top five theses.
- JUN. 2024 BEST PAPER AWARD nomination at DAC '24.
- OCT. 2023 NUSGS RESEARCH INCENTIVE AWARD from School of Computing, NUS (\$\$ 2,500 award).
- JAN. 2022 STUDENT TRAVEL AWARD from ASPLOS'22 conference.
- AUG. 2021 RESEARCH ACHIEVEMENT AWARD from School of Computing, NUS.
- MAR 2020 Invited talk and travel grant for the 2nd Young Architect Workshop at ASPLOS'20, Switzerland.
- FEB. 2019 PRESIDENT'S GRADUATE FELLOWSHIP, the most prestigious doctoral fellowship in Singapore.
- SEP. 2014 Ranked 164th in Iranian National University Entrance Exam among more than 250,000 students.
- 2006/2009 Recognized as talented student in entry exam of NODET for middle school and high school.

PROFESSIONAL EXPERIENCE

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- JUL. 2024 - PRESENT Postdoctoral Researcher at ETH ZÜRICH, Switzerland
Computer Security (COMSEC) Group
Group Lead: Prof. Kaveh RAZAVI
Research: CPU and DRAM security, novel attacks and defenses for computing systems
- AUG. 2019 - JUN. 2024 Graduate Research Assistant at NATIONAL UNIVERSITY OF SINGAPORE, Singapore
NUS Computer Architecture (CompArch) Group
Group Lead: Prof. Trevor E. CARLSON
Research: hardware/software co-design for efficient and secure modern processors
- JUL. 2016 - JUN. 2019 Research Assistant at SHARIF UNIVERSITY OF TECHNOLOGY, Tehran, Iran
High Performance Computer Architectures and Networks (HPCAN) Lab
Group Lead: Prof. Hamid SARBAZI-AZAD
Research: GPU register prefetching via HW/SW co-design and compiler optimizations
- SUMMER 2018 Research Intern at NATIONAL UNIVERSITY OF SINGAPORE, Singapore
Group Lead: Prof. Trevor E. CARLSON
Research: exploring new implementations for out-of-order commit processors

PEER-REVIEWED PUBLICATIONS

CCS'25	Ali Hajiabadi , Michele Marazzi, Kaveh Razavi <i>CHaRM: Checkpointed and Hashed Counters for Flexible and Efficient Rowhammer Mitigation.</i> Proceedings of 32 nd ACM Conference on Computer and Communications Security (CCS 2025), October 2025. ► Enabling a flexible in-CPU Rowhammer mitigation that secures any DRAM device, with arbitrary Rowhammer threshold, while using a fixed storage budget and efficient tagless SRAM counters. Paper Artifact GitHub Website
MICRO'25	Silvan Niederer, Sandro Rüegge, Ali Hajiabadi , Kaveh Razavi <i>One Flew over the Stack Engine's Nest: Practical Microarchitectural Attacks on the Stack Engine.</i> Proceedings of 58 th IEEE/ACM International Conference on Microarchitecture (MICRO 2025), October 2025. Acceptance rate: 124/597 = 20.8% ► Providing an extensive reverse engineering of the stack engine in modern AMD and Intel CPUs, and proposing novel and practical stack engine side channel attacks, leaking sensitive information. Paper Artifact Website
ISCA'25	Ali Hajiabadi , Trevor E. Carlson <i>CASSANDRA: Efficient Enforcement of Sequential Execution for Cryptographic Programs.</i> Proceedings of 52 nd ACM/IEEE International Symposium on Computer Architecture (ISCA 2025), June 2025. Acceptance rate: 132/570 = 23.1% ► A hardware/software mechanism to protect constant-time cryptographic code against Spectre by disabling speculation and recording and replaying sequential control flow. Paper
TACO'25	Yun Chen*, Ali Hajiabadi *, Romain Poussier, Yaswanth Tavva, Andreas Diavastos, Shivam Bhasin, Trevor E. Carlson <i>PARADISE: Criticality-Aware Instruction Reordering for Power Attack Resistance.</i> *Joint first-authors with equal contribution. In ACM Transactions on Architecture and Code Generation (TACO), 2024 ► Proposing a novel criticality-aware and non-deterministic instruction scheduling for out-of-order processors to resist power analysis attacks. Paper
DAC'24	Ali Hajiabadi , Trevor E. Carlson <i>CONJURING: Leaking Control Flow via Speculative Fetch Attacks.</i> Proceedings of 61 st ACM/IEEE Design Automation Conference (DAC 2024), June 2024. Acceptance rate: 337/1465 = 23.0% ★ Best Paper Award Nominee (5/337 = 1.5%) ► Proposing a new and practical variant of speculative fetch attacks that enables unprivileged attackers to leak control flow information of victims, without requiring priming a side channel. Paper Talk
DAC'24	Ali Hajiabadi , Archit Agarwal, Andreas Diavastos, Trevor E. Carlson <i>LEVIOSO: Efficient Compiler-Informed Secure Speculation.</i> Proceedings of 61 st ACM/IEEE Design Automation Conference (DAC 2024), June 2024. Acceptance rate: 337/1465 = 23.0% ► Efficient and comprehensive mitigation for speculative execution attacks through compiler-informed hints about true branch dependencies to restrict execution of speculative instructions only if necessary. Paper Github Talk
HPCA'24	Yun Chen*, Ali Hajiabadi *, Trevor E. Carlson <i>GADGETSPINNER: A New Transient Execution Primitive using the Loop Stream Detector.</i> Proceedings of 30 th IEEE International Symposium on High-Performance Computer Architecture (HPCA 2024), March 2024. Acceptance rate: 75/410 = 18.3% *Joint first-authors with equal contribution. ► Analyzing and discovering vulnerabilities of the Loop Stream Detector (LSD) in Intel CPUs that enables cross-core transient execution attacks without requiring branch mistraining/poisoning. Paper Artifact
HPCA'24	Yun Chen, Ali Hajiabadi , Lingfeng Pei, Trevor E. Carlson <i>PREFETCHX: Cross-Core Cache-Agnostic Prefetcher-Based Side-Channel Attacks.</i> Proceedings of 30 th IEEE International Symposium on High-Performance Computer Architecture (HPCA 2024), March 2024. Acceptance rate: 75/410 = 18.3% ► Extensive reverse-engineering of an undocumented Intel prefetcher, called XPT (an LLC miss predictor) that enables cross-core cache-agnostic side and covert channels. Paper Artifact

ICCAD'23	Arash Pashrashid, Ali Hajiabadi , Trevor E. Carlson <i>HIDFix: Efficient Mitigation of Cache-based Spectre Attacks through Hidden Rollbacks.</i> Proceedings of 42 nd IEEE/ACM International Conference on Computer-Aided Design (ICCAD 2023), November 2023. Acceptance rate: 172/768 = 22.4% ► Co-designing detection and mitigation to defend cache-based Spectre with no performance overhead; extensive study of existing detection/mitigation combinations and proposing attacks to bypass them. Paper
ICCAD'22	Arash Pashrashid, Ali Hajiabadi , Trevor E. Carlson <i>Fast, Robust and Accurate Detection of Cache-based Spectre Attack Phases.</i> Proceedings of 41 st IEEE/ACM International Conference on Computer-Aided Design (ICCAD 2022), November 2022. Acceptance rate: 132/586 = 22.5% ► (1) Demonstrating different attacks bypassing ML-based detectors for Spectre attacks; (2) proposing an efficient, accurate, robust, and timely mechanism to detect cache-based Spectre attack phases. Paper Github
ASPLOS'21	Ali Hajiabadi , Andreas Diavastos, Trevor E. Carlson <i>NOREBA: A Compiler-Informed Non-speculative Out-of-Order Commit Processor.</i> Proceedings of 26 th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2021). April 2021. Acceptance rate: 75/398 = 18.8% ► A hardware/software co-design that compiler informs the hardware about true branch dependencies enabling safe and non-speculative out-of-order commit of instructions improving efficiency. Paper Extended Abstract Short Slides Short Talk Slides Full Talk
TOCS'21	Mohammad Sadrosadati, Amirhossein Mirhosseini, Ali Hajiabadi , Seyed Borna Ehsani, Hajar Falahati, Hamid Sarbazi-Azad, Mario Drumond, Babak Falsafi, Rachata Ausavarungnirun, Onur Mutlu <i>Highly Concurrent Latency-tolerant Register Files for GPUs.</i> In ACM Transactions on Computer Systems (TOCS), 2021. ► A hardware/software co-operative design for register prefetching in GPUs. The compiler constructs the prefetch sets and ensures minimal register bank conflicts via register renumbering. arXiv Paper
CGO'21	Harish Patil, Alexander Isaev, Wim Heirman, Alen Sabu, Ali Hajiabadi , Trevor E. Carlson <i>ELFies: Executable Region Checkpoints for Performance Analysis and Simulation.</i> Proceedings of 19 th IEEE International Symposium on Code Generation and Optimization (CGO 2021), March 2021. Acceptance rate: 31/89 = 34.8% ► Proposing a set of tools to generate checkpoint executables of the regions of interest of applications, called ELFies. ELFies run natively and can be used for detailed analysis in other tools and simulators. Paper Github

TEACHING EXPERIENCE

► ETH Zürich, Switzerland

- FALL 2025 **Lecturer**, Computer Security (BSc)
 SPRING 2025 **Lecturer**, Capture the Flag – Introduction to Cybersecurity (P&S BSc)
 SPRING 2025 **Co-lecturer** with Prof. Kaveh Razavi, Computer Engineering (BSc)

► National University of Singapore, Singapore

- SPRING 2020/2021 **Teaching Assistant** (tutorial instructor), CS2106 Introduction to Operating Systems (BSc) by Prof. Djordje Jevdjic

► Sharif University of Technology, Tehran, Iran

- SPRING 2017 **Teaching Assistant** (assignments and projects), CE323 Computer Architecture (BSc) by Prof. Hamid Sarbazi-Azad
 FALL 2017/2018 **Teaching Assistant** (tutorial instructor, assignments and projects), CE453 Real-Time Systems (BSc) by Prof. Amirhossein Jahangir

PROFESSIONAL SERVICES

- Program Committee** HPCA 2026, MICRO 2025, EuroS&P 2026, AsiaCCS 2026
Sub-reviewer USENIX Security 2025
Reviewer (journals) IEEE CAL, ACM TACO, ACM TRETS
Shadow PC EuroSys 2024, EuroSys 2023
Student Volunteer PLDI 2021

RESEARCH MENTORING

MAR 2025 - PRESENT	<i>Maximilian Mosler</i>	Master thesis at ETH Zürich
MAR 2025 - JUN. 2025	<i>Jonas Buchholz</i>	Master semester project at ETH Zürich
DEC. 2024 - JUN. 2025	<i>Chenfei Liu</i>	Master thesis at ETH Zürich
SEP. 2024 - FEB. 2025	<i>Mounir Raki</i>	Master semester project at ETH Zürich
AUG. 2020 - MAR. 2024	<i>Yun Chen</i>	PhD thesis at NUS CompArch
JAN. 2021 - DEC. 2023	<i>Arash Pashrashid</i>	PhD thesis at NUS CompArch
JUL. 2021 - JUL. 2023	<i>Archit Agarwal</i>	Research assistant at NUS CompArch
SEP. 2020 - SEP. 2021	<i>Vernon Pang</i>	BSc final-year project at NUS

TALKS

JUN. 2025	CASSANDRA: Efficient Enforcement of Sequential Execution for Cryptographic Programs <i>Int. Symposium on Computer Architecture (ISCA 2025)</i> , Tokyo, Japan.
MAR. 2024	Will CPUs Be Free of Spectre? Dark Side and Light Side of the Battle <i>ETH Zürich, COMSEC Group</i> , Zürich, Switzerland.
MAR. 2024	GADGETSPINNER: A New Transient Execution Primitive using the Loop Stream Detector <i>Int. Symposium on High-Performance Computer Architecture (HPCA 2024)</i> , Edinburgh, Scotland.
AUG. 2021	NOREBA: A Compiler-Informed Non-speculative Out-of-Order Commit Processor <i>Computing Research Week, School of Computing (NUS)</i> , Virtual.
APR. 2021	NOREBA: A Compiler-Informed Non-speculative Out-of-Order Commit Processor <i>Int. Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2021)</i> , Virtual.
FEB. 2021	Accelerating HPC applications with Out-of-Order Commit Processors <i>Free and Open source Software Developers' European Meeting (FOSDEM 2021)</i> , HPC, Big Data, and Data Science track, Virtual.
MAR. 2020	Speculation-Free Out-of-Order Commit <i>2nd Young Architect Workshop at the 25th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2020)</i> , Virtual.

SKILLS

PROGRAMMING LANGUAGES:	C, C++, Python, bash, and familiar with Java, Matlab, Scala
INSTRUCTION SET ARCHITECTURES:	x86, Arm, RISC-V
SCIENTIFIC TOOLS:	LLVM Compiler Infrastructure, gem5 Simulator, Sniper Simulator, Ramulator, Intel Pin, Dynamorio
TYPESETTING:	L ^A T _E X, Microsoft Word