

Ali HAJIABADI

Postdoctoral Researcher
ETH Zürich

CONTACT INFORMATION

ADDRESS: ETZ G 78.2, Gloriastr. 35, 8092 Zürich, Switzerland
EMAIL: ahajiabadi@ethz.ch
HOMEPAGE: ahajiabadi.github.io

RESEARCH INTERESTS

Systems Security, Hardware/Software Co-design, Computer Architecture, Optimizing Compilers, Formal Methods, Secure Architectures and Software, Microarchitectural Side Channels, Trusted Execution Environments

EDUCATION

- 2019 - 2024 Doctor of Philosophy in Computer Science
National University of Singapore (NUS), Singapore
Thesis: *"Building Efficient and Secure Processors thorough Hardware/Software Co-design"*
Advisor: Prof. Trevor E. CARLSON
- 2014 - 2019 Bachelor of Science in Computer Engineering
Sharif University of Technology, Tehran, Iran
Thesis: *"High Concurrency Latency Tolerant Register Files for GPUs"*
Advisor: Prof. Hamid SARBAZI-AZAD
- 2009 - 2013 Diploma in Physics and Mathematics Discipline
Shahid Beheshti High School, Birjand, Iran
Affiliated with the National Organization for the Development of Exceptional Talents (NODET)

HONORS & AWARDS

- AUG. 2024 DEAN'S GRADUATE RESEARCH EXCELLENCE AWARD (AY2023/2024).
- JUL. 2024 SCHOOL OF COMPUTING CS PHD THESIS AWARD (Honorable Mention), selected as top five theses.
- JUN. 2024 BEST PAPER AWARD nomination at DAC '24.
- OCT. 2023 NUSGS RESEARCH INCENTIVE AWARD from School of Computing, NUS (S\$ 2,500 award).
- JAN. 2022 STUDENT TRAVEL AWARD from ASPLOS'22 conference.
- AUG. 2021 RESEARCH ACHIEVEMENT AWARD from School of Computing, NUS.
- MAR. 2020 Invited talk and travel grant for the 2nd Young Architect Workshop at ASPLOS'20, Switzerland.
- FEB. 2019 PRESIDENT'S GRADUATE FELLOWSHIP, the most prestigious doctoral fellowship in Singapore.
- SEP. 2014 Ranked 164th in Iranian National University Entrance Exam among more than 250,000 students.
- 2006/2009 Recognized as talented student in entry exam of NODET for middle school and high school.

PROFESSIONAL EXPERIENCE

- JUL. 2024 - PRESENT Postdoctoral Researcher at ETH ZÜRICH, Switzerland
Computer Security (COMSEC) Group
Group Lead: Prof. Kaveh RAZAVI
Research: CPU and DRAM security, novel attacks and defenses for computing systems
- AUG. 2019 - JUN. 2024 Graduate Research Assistant at NATIONAL UNIVERSITY OF SINGAPORE, Singapore
NUS Computer Architecture (CompArch) Group
Group Lead: Prof. Trevor E. CARLSON
Research: hardware/software co-design for efficient and secure modern processors
- JUL. 2016 - JUN. 2019 Research Assistant at SHARIF UNIVERSITY OF TECHNOLOGY, Tehran, Iran
High Performance Computer Architectures and Networks (HPCAN) Lab
Group Lead: Prof. Hamid SARBAZI-AZAD
Research: GPU register prefetching via HW/SW co-design and compiler optimizations
- SUMMER 2018 Research Intern at NATIONAL UNIVERSITY OF SINGAPORE, Singapore
Group Lead: Prof. Trevor E. CARLSON
Research: exploring new implementations for out-of-order commit processors

PEER-REVIEWED PUBLICATIONS

- ISCA'25 | **Ali Hajiabadi**, Trevor E. Carlson
CASSANDRA: Efficient Enforcement of Sequential Execution for Cryptographic Programs.
Proceedings of 52nd ACM/IEEE International Symposium on Computer Architecture (ISCA 2025), June 2025. Acceptance rate: 132/570 = 23.1%
► *A hardware/software mechanism to protect constant-time cryptographic programs against Spectre via disabling the branch predictor and redirecting fetch based on a sequential control-flow contract.*
- DAC'24 | **Ali Hajiabadi**, Trevor E. Carlson
CONJURING: Leaking Control Flow via Speculative Fetch Attacks.
Proceedings of 61st ACM/IEEE Design Automation Conference (DAC 2024), June 2024. Acceptance rate: 337/1465 = 23.0%
★ *Best Paper Award Nominee* (5/337 = 1.5%)
► *Proposing a new and practical variant of speculative fetch attacks that enables unprivileged attackers to leak control flow information of victims, without requiring priming a side channel.*
[Paper](#) | [Talk](#)
- DAC'24 | **Ali Hajiabadi**, Archit Agarwal, Andreas Diavastos, Trevor E. Carlson
LEVISO: Efficient Compiler-Informed Secure Speculation.
Proceedings of 61st ACM/IEEE Design Automation Conference (DAC 2024), June 2024. Acceptance rate: 337/1465 = 23.0%
► *Efficient and comprehensive mitigation for speculative execution attacks through compiler-informed hints about true branch dependencies to restrict execution of speculative instructions only if necessary.*
[Paper](#) | [Github](#) | [Talk](#)
- HPCA'24 | Yun Chen*, **Ali Hajiabadi***, Trevor E. Carlson
GADGETSPINNER: A New Transient Execution Primitive using the Loop Stream Detector.
Proceedings of 30th IEEE International Symposium on High-Performance Computer Architecture (HPCA 2024), March 2024. Acceptance rate: 75/410 = 18.3%
*Joint first-authors with equal contribution.
► *Analyzing and discovering vulnerabilities of the Loop Stream Detector (LSD) in Intel CPUs that enables cross-core transient execution attacks without requiring branch mistraining/poisoning.*
[Paper](#) | [Artifact](#)
- HPCA'24 | Yun Chen, **Ali Hajiabadi**, Lingfeng Pei, Trevor E. Carlson
PREFETCHX: Cross-Core Cache-Agnostic Prefetcher-Based Side-Channel Attacks.
Proceedings of 30th IEEE International Symposium on High-Performance Computer Architecture (HPCA 2024), March 2024. Acceptance rate: 75/410 = 18.3%
► *Extensive reverse-engineering of an undocumented Intel prefetcher, called XPT (an LLC miss predictor) that enables cross-core cache-agnostic side and covert channels.*
[Paper](#) | [Artifact](#)
- TACO'24 | Yun Chen*, **Ali Hajiabadi***, Romain Poussier, Yaswanth Tavva, Andreas Diavastos, Shivam Bhasin, Trevor E. Carlson
PARADISE: Criticality-Aware Instruction Reordering for Power Attack Resistance.
*Joint first-authors with equal contribution.
In ACM Transactions on Architecture and Code Generation (TACO), 2024
► *Proposing a novel criticality-aware and non-deterministic instruction scheduling for out-of-order processors to resist power analysis attacks.*
[Paper](#)
- ICCAD'23 | Arash Pashrashid, **Ali Hajiabadi**, Trevor E. Carlson
HIDFIX: Efficient Mitigation of Cache-based Spectre Attacks through Hidden Rollbacks.
Proceedings of 42nd IEEE/ACM International Conference on Computer-Aided Design (ICCAD 2023), November 2023. Acceptance rate: 172/768 = 22.4%
► *Co-designing detection and mitigation to defend cache-based Spectre with no performance overhead; extensive study of existing detection/mitigation combinations and proposing attacks to bypass them.*
[Paper](#)
- ICCAD'22 | Arash Pashrashid, **Ali Hajiabadi**, Trevor E. Carlson
Fast, Robust and Accurate Detection of Cache-based Spectre Attack Phases.
Proceedings of 41st IEEE/ACM International Conference on Computer-Aided Design (ICCAD 2022), November 2022. Acceptance rate: 132/586 = 22.5%
► *(1) Demonstrating different attacks bypassing ML-based detectors for Spectre attacks; (2) proposing an efficient, accurate, robust, and timely mechanism to detect cache-based Spectre attack phases.*
[Paper](#) | [Github](#)

ASPLOS'21	<p>Ali Hajiabadi, Andreas Diavastos, Trevor E. Carlson NOREBA: A Compiler-Informed Non-speculative Out-of-Order Commit Processor. Proceedings of 26th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2021). April 2021. Acceptance rate: 75/398 = 18.8% ► <i>A hardware/software co-design that compiler informs the hardware about true branch dependencies enabling safe and non-speculative out-of-order commit of instructions improving efficiency.</i> Paper Extended Abstract Short Slides Short Talk Slides Full Talk</p>
TOCS'21	<p>Mohammad Sadrosadati, Amirhossein Mirhosseini, Ali Hajiabadi, Seyed Borna Ehsani, Hajar Falahati, Hamid Sarbazi-Azad, Mario Drumond, Babak Falsafi, Rachata Ausavarungnirun, Onur Mutlu Highly Concurrent Latency-tolerant Register Files for GPUs. In ACM Transactions on Computer Systems (TOCS), 2021. ► <i>A hardware/software co-operative design for register prefetching in GPUs. The compiler constructs the prefetch sets and ensures minimal register bank conflicts via register renumbering.</i> arXiv Paper</p>
CGO'21	<p>Harish Patil, Alexander Isaev, Wim Heirman, Alen Sabu, Ali Hajiabadi, Trevor E. Carlson ELFies: Executable Region Checkpoints for Performance Analysis and Simulation. Proceedings of 19th IEEE International Symposium on Code Generation and Optimization (CGO 2021), March 2021. Acceptance rate: 31/89 = 34.8% ► <i>Proposing a set of tools to generate checkpoint executables of the regions of interest of applications, called ELFies. ELFies run natively and can be used for detailed analysis in other tools and simulators.</i> Paper Github</p>

TEACHING EXPERIENCE

► ETH Zürich, Switzerland

SPRING 2025	<p>Lecturer <i>Course: Capture the Flag – Introduction to Cybersecurity</i></p>
SPRING 2025	<p>Co-lecturer <i>Course: BSc Computer Engineering</i> <i>Co-lecturer: Prof. Kaveh Razavi</i></p>

► National University of Singapore, Singapore

SPRING 2020	<p>Teaching Assistant, Tutorial Instructor</p>
and SPRING 2021	<p><i>Course: CS2106 Introduction to Operating Systems</i> <i>Lecturer: Prof. Djordje Jevdjic</i></p>

► Sharif University of Technology, Tehran, Iran

SPRING 2017	<p>Teaching Assistant, Assignments/Projects Assistant <i>Course: CE323 Computer Architecture</i> <i>Lecturer: Prof. Hamid Sarbazi-Azad</i></p>
FALL 2017 and FALL 2018	<p>Teaching Assistant, Tutorial Instructor, Assignments/Projects Assistant <i>Course: CE453 Real-Time Systems</i> <i>Lecturer: Prof. Amirhossein Jahangir</i></p>

SERVICES

Program Committee	EuroSys 2024 (heavy Shadow PC), EuroSys 2023 (Shadow PC)
Reviewer	IEEE Computer Architecture Letters (CAL), ACM Transactions on Architecture and Code Optimizations (TACO), ACM Transactions on Reconfigurable Technology and Systems (TRETs)
Student Volunteer	PLDI 2021

RESEARCH MENTORING

MAR. 2025 -	PRESENT	<i>Jonas Buchholz</i>	Master semester project at ETH Zürich
FEB. 2025 -	PRESENT	<i>Maximilian Mosler</i>	Master thesis at ETH Zürich
DEC. 2024 -	PRESENT	<i>Chenfei Liu</i>	Master thesis at ETH Zürich
SEP. 2024 -	FEB. 2025	<i>Mounir Raki</i>	Master semester project at ETH Zürich
AUG. 2020 -	MAR. 2024	<i>Yun Chen</i>	PhD thesis at NUS CompArch
JAN. 2021 -	DEC. 2023	<i>Arash Pashrashid</i>	PhD thesis at NUS CompArch
JUL. 2021 -	JUL. 2023	<i>Archit Agarwal</i>	Research assistant at NUS CompArch
SEP. 2020 -	SEP. 2021	<i>Vernon Pang</i>	BSc final-year project at NUS

TALKS

- MAR. 2024 **Will CPUs Be Free of Spectre? Dark Side and Light Side of the Battle**
ETH Zürich, COMSEC Group, Zürich, Switzerland.
- MAR. 2024 **GADGETSPINNER: A New Transient Execution Primitive using the Loop Stream Detector**
Int. Symposium on High-Performance Computer Architecture (HPCA 2024), Edinburgh, Scotland.
- AUG. 2021 **NOREBA: A Compiler-Informed Non-speculative Out-of-Order Commit Processor**
Computing Research Week, School of Computing (NUS), Virtual.
- APR. 2021 **NOREBA: A Compiler-Informed Non-speculative Out-of-Order Commit Processor**
Int. Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2021), Virtual.
- FEB. 2021 **Accelerating HPC applications with Out-of-Order Commit Processors**
Free and Open source Software Developers' European Meeting (FOSDEM 2021), HPC, Big Data, and Data Science track, Virtual.
- MAR. 2020 **Speculation-Free Out-of-Order Commit**
2nd Young Architect Workshop at the 25th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2020), Virtual.

SKILLS

- PROGRAMMING LANGUAGES: C, C++, Python, bash, and familiar with Java, Matlab, Scala
- INSTRUCTION SET ARCHITECTURES: x86, Arm, RISC-V
- SCIENTIFIC TOOLS: LLVM Compiler Infrastructure, gem5 Simulator, Sniper Simulator, Ramulator, Intel Pin, DynamoRIO
- TYPESETTING: \LaTeX , Microsoft Word