

# Ali HAJIABADI

Postdoctoral Researcher and Lecturer  
ETH Zürich

## CONTACT INFORMATION

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## RESEARCH INTERESTS

Systems Security, Hardware/Software Co-design, Computer Architecture, Optimizing Compilers, Formal Methods, Secure Architectures and Software, Microarchitectural Side Channels, Trusted Execution Environments

## EDUCATION

- 2019 - 2024 Doctor of Philosophy in Computer Science  
**National University of Singapore (NUS)**, Singapore  
Thesis: *"Building Efficient and Secure Processors thorough Hardware/Software Co-design"*  
Advisor: Prof. Trevor E. CARLSON
- 2014 - 2019 Bachelor of Science in Computer Engineering  
**Sharif University of Technology**, Tehran, Iran  
Thesis: *"High Concurrency Latency Tolerant Register Files for GPUs"*  
Advisor: Prof. Hamid SARBAZI-AZAD
- 2009 - 2013 Diploma in Physics and Mathematics Discipline  
**Shahid Beheshti High School**, Birjand, Iran  
*Affiliated with the National Organization for the Development of Exceptional Talents (NODET)*

## HONORS & AWARDS

- AUG. 2024 DEAN'S GRADUATE RESEARCH EXCELLENCE AWARD.
- JUL. 2024 SCHOOL OF COMPUTING CS PHD THESIS AWARD (Honorable Mention), selected as top five theses.
- JUN. 2024 BEST PAPER AWARD nomination at DAC '24.
- OCT. 2023 NUSGS RESEARCH INCENTIVE AWARD from School of Computing, NUS (S\$ 2,500 award).
- JAN. 2022 STUDENT TRAVEL AWARD from ASPLOS'22 conference.
- AUG. 2021 RESEARCH ACHIEVEMENT AWARD from School of Computing, NUS.
- MAR. 2020 Invited talk and travel grant for the 2<sup>nd</sup> Young Architect Workshop at ASPLOS'20, Switzerland.
- FEB. 2019 PRESIDENT'S GRADUATE FELLOWSHIP, the most prestigious doctoral fellowship in Singapore.
- SEP. 2014 Ranked 164<sup>th</sup> in Iranian National University Entrance Exam among more than 250,000 students.
- 2006/2009 Recognized as talented student in entry exam of NODET for middle school and high school.

## PROFESSIONAL EXPERIENCE

- JUL. 2024 - PRESENT Postdoctoral Researcher at ETH ZÜRICH, Switzerland  
*Computer Security (COMSEC) Group*  
Group Lead: Prof. Kaveh RAZAVI  
Research: CPU and DRAM security, novel attacks and defenses for computing systems
- AUG. 2019 - JUN. 2024 Graduate Research Assistant at NATIONAL UNIVERSITY OF SINGAPORE, Singapore  
*NUS Computer Architecture (CompArch) Group*  
Group Lead: Prof. Trevor E. CARLSON  
Research: hardware/software co-design for efficient and secure modern processors
- JUL. 2016 - JUN. 2019 Research Assistant at SHARIF UNIVERSITY OF TECHNOLOGY, Tehran, Iran  
*High Performance Computer Architectures and Networks (HPCAN) Lab*  
Group Lead: Prof. Hamid SARBAZI-AZAD  
Research: GPU register prefetching via HW/SW co-design and compiler optimizations
- SUMMER 2018 Research Intern at NATIONAL UNIVERSITY OF SINGAPORE, Singapore  
Group Lead: Prof. Trevor E. CARLSON  
Research: exploring new implementations for out-of-order commit processors

## PEER-REVIEWED PUBLICATIONS

- S&P'26 | Jean-Claude Graf\*, Sandro Rüegge\*, **Ali Hajiabadi**, Kaveh Razavi  
*VMscape: Exposing and Exploiting Incomplete Branch Predictor Isolation in Cloud Environments*.  
Proceedings of 47<sup>th</sup> IEEE Symposium on Security and Privacy (S&P, Oakland 2026), May 2026.  
Acceptance rate: 118/925 = 12.8%  
► *A systematic analysis of Branch Target Injection (BTI) across virtualization boundaries, with the first attack on AMD CPUs where a KVM guest leaks secrets from an unmodified QEMU process on the host.*  
[Paper](#) | [GitHub](#) | [Website](#)
- HPCA'26 | Hritvik Taneja, **Ali Hajiabadi**, Michele Marazzi, Kaveh Razavi, Moinuddin K. Qureshi  
*MIRZA: Efficiently Mitigating Rowhammer with Randomization and ALERT*.  
Proceedings of 32<sup>nd</sup> IEEE International Symposium on High-Performance Computer Architecture (HPCA 2026), February 2026. Acceptance rate: 119/602 = 19.8%  
► *ALERT Is All You Need: proposing a reactive and efficient Rowhammer mitigation without per row activation counters, using probabilistic and securely filtered ALERTs.*
- CCS'25 | **Ali Hajiabadi**, Michele Marazzi, Kaveh Razavi  
*CHaRM: Checkpointed and Hashed Counters for Flexible and Efficient Rowhammer Mitigation*.  
Proceedings of 32<sup>nd</sup> ACM Conference on Computer and Communications Security (CCS 2025), October 2025. Acceptance rate: 316/2186 = 14.5%  
► *An in-CPU Rowhammer mitigation breaking counter-threshold dependency to protect DRAM devices with arbitrary threshold, while using a fixed storage budget and efficient tagless SRAM counters.*  
[Paper](#) | [Artifact](#) | [GitHub](#) | [Website](#)
- MICRO'25 | Silvan Niederer, Sandro Rüegge, **Ali Hajiabadi**, Kaveh Razavi  
*One Flew over the Stack Engine's Nest: Practical Microarchitectural Attacks on the Stack Engine*.  
Proceedings of 58<sup>th</sup> IEEE/ACM International Conference on Microarchitecture (MICRO 2025), October 2025. Acceptance rate: 124/597 = 20.8%  
► *Providing an extensive reverse engineering of the stack engine in modern AMD and Intel CPUs, and proposing novel and practical stack engine side channel attacks, leaking sensitive information.*  
[Paper](#) | [Artifact](#) | [Website](#)
- ISCA'25 | **Ali Hajiabadi**, Trevor E. Carlson  
*CASSANDRA: Efficient Enforcement of Sequential Execution for Cryptographic Programs*.  
Proceedings of 52<sup>nd</sup> ACM/IEEE International Symposium on Computer Architecture (ISCA 2025), June 2025. Acceptance rate: 132/570 = 23.1%  
► *A hardware/software mechanism to protect constant-time cryptographic code against Spectre by disabling speculation and recording-and-replaying sequential control flow.*  
[Paper](#)
- TACO'25 | Yun Chen\*, **Ali Hajiabadi\***, Romain Poussier, Yaswanth Tavva, Andreas Diavastos, Shivam Bhasin, Trevor E. Carlson  
*PARADISE: Criticality-Aware Instruction Reordering for Power Attack Resistance*.  
\*Joint first-authors with equal contribution.  
In ACM Transactions on Architecture and Code Generation (TACO), 2024  
► *Proposing a novel criticality-aware and non-deterministic instruction scheduling for out-of-order processors to resist power analysis attacks.*  
[Paper](#)
- DAC'24 | **Ali Hajiabadi**, Trevor E. Carlson  
*CONJURING: Leaking Control Flow via Speculative Fetch Attacks*.  
Proceedings of 61<sup>st</sup> ACM/IEEE Design Automation Conference (DAC 2024), June 2024. Acceptance rate: 337/1465 = 23.0%  
★ *Best Paper Award Nominee* (5/337 = 1.5%)  
► *Proposing a new and practical variant of speculative fetch attacks that enables unprivileged attackers to leak control flow information of victims, without requiring priming a side channel.*  
[Paper](#) | [Talk](#)
- DAC'24 | **Ali Hajiabadi**, Archit Agarwal, Andreas Diavastos, Trevor E. Carlson  
*LEVISO: Efficient Compiler-Informed Secure Speculation*.  
Proceedings of 61<sup>st</sup> ACM/IEEE Design Automation Conference (DAC 2024), June 2024. Acceptance rate: 337/1465 = 23.0%  
► *Efficient and comprehensive mitigation for speculative execution attacks through compiler-informed hints about true branch dependencies to restrict execution of speculative instructions only if necessary.*  
[Paper](#) | [Github](#) | [Talk](#)

HPCA'24	<p>Yun Chen*, <b>Ali Hajiabadi</b>*, Trevor E. Carlson  <b>GADGETSPINNER: A New Transient Execution Primitive using the Loop Stream Detector.</b>          Proceedings of 30<sup>th</sup> IEEE International Symposium on High-Performance Computer Architecture (HPCA 2024), March 2024. Acceptance rate: 75/410 = 18.3%          *Joint first-authors with equal contribution.          ► <i>Analyzing and discovering vulnerabilities of the Loop Stream Detector (LSD) in Intel CPUs that enables cross-core transient execution attacks without requiring branch prediction unit mistraining.</i>  <a href="#">Paper</a>   <a href="#">Artifact</a></p>
HPCA'24	<p>Yun Chen, <b>Ali Hajiabadi</b>, Lingfeng Pei, Trevor E. Carlson  <b>PREFETCHX: Cross-Core Cache-Agnostic Prefetcher-Based Side-Channel Attacks.</b>          Proceedings of 30<sup>th</sup> IEEE International Symposium on High-Performance Computer Architecture (HPCA 2024), March 2024. Acceptance rate: 75/410 = 18.3%          ► <i>Extensive reverse-engineering of an undocumented Intel prefetcher, called XPT (an LLC miss predictor) that enables cross-core cache-agnostic covert and side channels.</i>  <a href="#">Paper</a>   <a href="#">Artifact</a></p>
ICCAD'23	<p>Arash Pashrashid, <b>Ali Hajiabadi</b>, Trevor E. Carlson  <b>HIDFix: Efficient Mitigation of Cache-based Spectre Attacks through Hidden Rollbacks.</b>          Proceedings of 42<sup>nd</sup> IEEE/ACM International Conference on Computer-Aided Design (ICCAD 2023), November 2023. Acceptance rate: 172/768 = 22.4%          ► <i>Extensive study of existing detection/mitigation combinations and proposing attacks to bypass them; co-designing detection and mitigation to defend cache-based Spectre with no performance overhead.</i>  <a href="#">Paper</a></p>
ICCAD'22	<p>Arash Pashrashid, <b>Ali Hajiabadi</b>, Trevor E. Carlson  <b>Fast, Robust and Accurate Detection of Cache-based Spectre Attack Phases.</b>          Proceedings of 41<sup>st</sup> IEEE/ACM International Conference on Computer-Aided Design (ICCAD 2022), November 2022. Acceptance rate: 132/586 = 22.5%          ► <i>(1) Demonstrating different attacks bypassing ML-based detectors for Spectre attacks; (2) proposing an efficient, accurate, robust, and timely mechanism to detect cache-based Spectre attack phases.</i>  <a href="#">Paper</a>   <a href="#">Github</a></p>
ASPLOS'21	<p><b>Ali Hajiabadi</b>, Andreas Diavastos, Trevor E. Carlson  <b>NOREBA: A Compiler-Informed Non-speculative Out-of-Order Commit Processor.</b>          Proceedings of 26<sup>th</sup> ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2021). April 2021. Acceptance rate: 75/398 = 18.8%          ► <i>A hardware/software co-design that compiler informs the hardware about true branch dependencies enabling safe and non-speculative out-of-order commit of instructions improving efficiency.</i>  <a href="#">Paper</a>   <a href="#">Extended Abstract</a>   <a href="#">Short Slides</a>   <a href="#">Short Talk</a>   <a href="#">Slides</a>   <a href="#">Full Talk</a></p>
TOCS'21	<p>Mohammad Sadrosadati, Amirhossein Mirhosseini, <b>Ali Hajiabadi</b>, Seyed Borna Ehsani, Hajar Falahati, Hamid Sarbazi-Azad, Mario Drumond, Babak Falsafi, Rachata Ausavarungrun, Onur Mutlu  <b>Highly Concurrent Latency-tolerant Register Files for GPUs.</b>          In ACM Transactions on Computer Systems (TOCS), 2021.          ► <i>A hardware/software co-operative design for register prefetching in GPUs. The compiler constructs the prefetch sets and ensures minimal register bank conflicts via register renumbering.</i>  <a href="#">arXiv Paper</a></p>
CGO'21	<p>Harish Patil, Alexander Isaev, Wim Heirman, Alen Sabu, <b>Ali Hajiabadi</b>, Trevor E. Carlson  <b>ELFies: Executable Region Checkpoints for Performance Analysis and Simulation.</b>          Proceedings of 19<sup>th</sup> IEEE International Symposium on Code Generation and Optimization (CGO 2021), March 2021. Acceptance rate: 31/89 = 34.8%          ► <i>Proposing a set of tools to generate checkpoint executables of the regions of interest of applications, called ELFies. ELFies run natively and can be used for detailed analysis in other tools and simulators.</i>  <a href="#">Paper</a>   <a href="#">Github</a></p>

## TEACHING EXPERIENCE

### ► ETH Zürich, Switzerland

- SPRING 2026 **Co-lecturer**, Computer Engineering (BSc), with Prof. Kaveh Razavi and Dr. Patrick Jattke
- FALL 2025 **Lecturer**, Computer Security (BSc) [New Course]
- SPRING 2025 **Lecturer**, Capture the Flag – Introduction to Cybersecurity (P&S BSc) [New Course]
- SPRING 2025 **Co-lecturer**, Computer Engineering (BSc), with Prof. Kaveh Razavi

### ► National University of Singapore, Singapore

- SPRING 2020 **Teaching Assistant (tutorial instructor)**, CS2106 Introduction to Operating Systems (BSc)
- & SPRING 2021 **Lecturer**: Prof. Djordje Jevdjic

## ► Sharif University of Technology, Tehran, Iran

SPRING 2017 **Teaching Assistant** (*assignments & projects*), CE323 Computer Architecture (BSc)  
*Lecturer: Prof. Hamid Sarbazi-Azad*

FALL 2017 **Teaching Assistant** (*tutorial instructor, assignments & projects*), CE453 Real-Time Systems (BSc)  
& FALL 2018 *Lecturer: Prof. Amirhossein Jahangir*

## PROFESSIONAL SERVICES

<b>Program Committee</b>	ISCA ('26), MICRO ('25), HPCA ('26), uASC ('26), EuroS&P ('26), AsiaCCS ('26)
<b>Sub-reviewer</b>	USENIX Security ('25)
<b>Reviewer (journals)</b>	IEEE CAL, ACM TACO, ACM TRETs
<b>Session Chair</b>	uASC'26 ( <i>Brave New Defense</i> ), MICRO'25 ( <i>Security and Privacy - Memory</i> )
<b>Shadow PC</b>	EuroSys ('24, '23)
<b>Student Volunteer</b>	PLDI ('21)

## TALKS

NOV. 2025	<b>The Hidden and Ugly Faces of Spectre: Unexplored and Unmitigated Threat Models</b> <i>IC, EPFL, Lausanne, Switzerland.</i>
OCT. 2025	<b>CHaRM: Checkpointed and Hashed Counters for Flexible and Efficient Rowhammer Mitigation</b> <i>Conference on Computer and Communication Security (CCS 2025), Taipei, Taiwan.</i>
JUN. 2025	<b>CASSANDRA: Efficient Enforcement of Sequential Execution for Cryptographic Programs</b> <i>Int. Symposium on Computer Architecture (ISCA 2025), Tokyo, Japan.</i>
MAR. 2024	<b>Will CPUs Be Free of Spectre? Dark Side and Light Side of the Battle</b> <i>ETH Zürich, COMSEC Group, Zürich, Switzerland.</i>
MAR. 2024	<b>GADGETSPINNER: A New Transient Execution Primitive using the Loop Stream Detector</b> <i>Int. Symposium on High-Performance Computer Architecture (HPCA 2024), Edinburgh, Scotland.</i>
AUG. 2021	<b>NOREBA: A Compiler-Informed Non-speculative Out-of-Order Commit Processor</b> <i>Computing Research Week, School of Computing (NUS), Virtual.</i>
APR. 2021	<b>NOREBA: A Compiler-Informed Non-speculative Out-of-Order Commit Processor</b> <i>Int. Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2021), Virtual.</i>
FEB. 2021	<b>Accelerating HPC applications with Out-of-Order Commit Processors</b> <i>Free and Open source Software Developers' European Meeting (FOSDEM 2021), HPC, Big Data, and Data Science track, Virtual.</i>
MAR. 2020	<b>Speculation-Free Out-of-Order Commit</b> <i>2<sup>nd</sup> Young Architect Workshop at the 25<sup>th</sup> International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2020), Virtual.</i>

## RESEARCH MENTORING

JAN. 2026 - PRESENT	<i>Quentin Bordier</i>	PhD thesis at COMSEC, ETH Zürich
MAR. 2025 - PRESENT	<i>Jean-Claude Graf</i>	PhD thesis at COMSEC, ETH Zürich
MAR. 2025 - PRESENT	<i>Sandro Rüegg</i>	PhD thesis at COMSEC, ETH Zürich
MAR. 2025 - SEP. 2025	<i>Maximilian Mosler</i>	Master thesis at ETH Zürich
MAR. 2025 - JUN. 2025	<i>Jonas Buchholz</i>	Master semester project at ETH Zürich
DEC. 2024 - JUN. 2025	<i>Chenfei Liu</i>	Master thesis at ETH Zürich
SEP. 2024 - FEB. 2025	<i>Mounir Raki</i>	Master semester project at ETH Zürich
JUL. 2024 - PRESENT	<i>Silvan Niderer</i>	PhD thesis at COMSEC, ETH Zürich
JAN. 2021 - DEC. 2023	<i>Arash Pashrashid</i>	PhD thesis at NUS CompArch
JUL. 2021 - JUL. 2023	<i>Archit Agarwal</i>	Research assistant at NUS CompArch
SEP. 2020 - SEP. 2021	<i>Vernon Pang</i>	BSc final-year project at NUS
AUG. 2020 - MAR. 2024	<i>Yun Chen</i>	PhD thesis at NUS CompArch

## SKILLS

PROGRAMMING LANGUAGES:	C, C++, Python, bash, and familiar with Java, Matlab, Scala
INSTRUCTION SET ARCHITECTURES:	x86, Arm, RISC-V
SCIENTIFIC TOOLS:	LLVM Compiler Infrastructure, gem5 Simulator, Sniper Simulator, Rammulator, Intel Pin, DynamoRIO
TYPESETTING:	LaTeX, Microsoft Word