Marmara University Electrical-Electronics Eng. Dept.

CSE4117 Microprocessors Laboratory Assignment #4

Each group must submit their own study. The group members have to work together and each member must know each step of the study. The studies will be submitted until 12.08.2022. A report (pdf file) should explain the digital circuits, operational blocks and all necessary technical information (You may use screenshots in your report). A short video file (<2 mins and <10 MByte)must be prepared to present the study. Each group must upload these files to a cloud-drive. The drive link must be sent to cse4117@yaani.com email address.

For this laboratory assignment, you will use Altera Quartus II software and Altera DE2-115 FPGA Kit to design and demonstrate some simple CPU blocks working together. Please follow the items below to complete your study:

1. In this assignment, you will design the program counter, instruction register, stack and control unit blocks. You need to demonstrate the following J-type instructions are working properly: CALL, RETURN, JIN,JIZ,JIC and SIZ.
2. Step1: Design the stack module with the properties below:

    - It will have a memory module that have four addresses with 9-bit data area (each).
    - Address inputs of the memory module will be connected to a 2-bit stack pointer register, which will have 00 value at startup.
    - SP++ input will increase the stack pointer register by one.
    - SP-- input will decrease the stack pointer register by one.
    - R/W input defines the operation type: logic 0 value will store an address to the pointed(by SP) location. Logic 1 value will read an address from the pointed location.
    - Stack_EN will make the module operational. Logic1 the operaton will be realized in the next clock. Logic0, no operation.

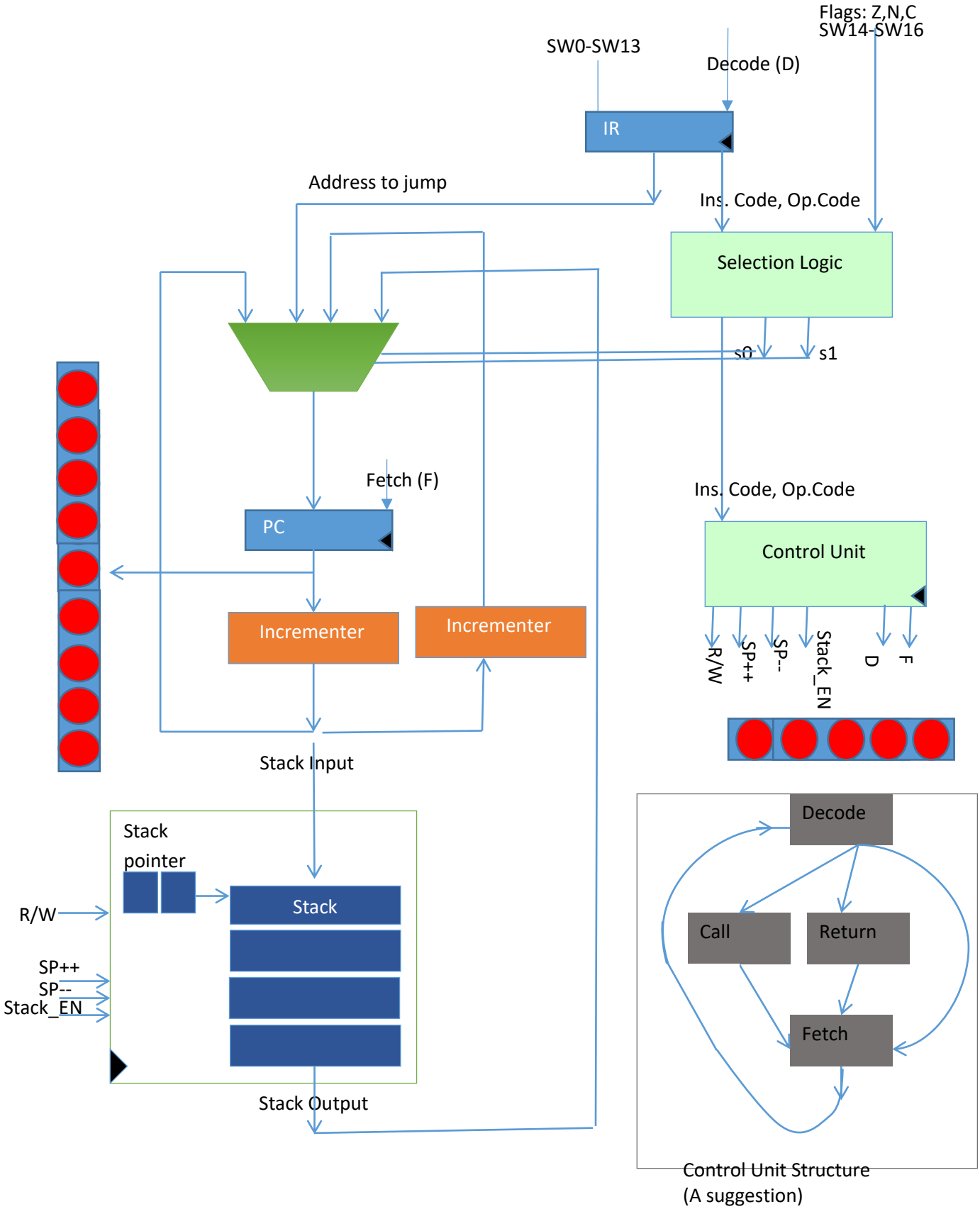
3. Step2: Design the counter

    - The program counter should choose the correct address value according the current instruction code, operation code and flag values.
    - The flags should be connected to SW14, SW15 and SW15 (Zero, Negative and Carry flags respectively).
    - The instruction should be read by Instruction register which has 14 inputs connected to SW0 to SW13. The instruction will be applied by the student using the switches.
    - Current program counter value should be followed by using the LEDs that are connected the the output of the program counter.

4. Step3: Control Unit

    - Control unit will have only the necessary states to enable the demonstration of the J-type instructions. A suggestion for the state diagram of the control unit can be seen in the figure below. The state diagram in the figure will give you an idea, NOTE THAT it is not completed and IT IS not correct It will give you a direction. You may need to add extra states or you can remove some states?
    - All Output signals shoud be connected to LEDs
    - Control unit must generate the necessary signals(SP++,Stack EN ,F,D etc) with the correct timing according to its inputs (Inst. Code, op codei clock).

5. Step5: Demonstrate the instructions: CALL, RETURN, JIN,JIZ,JIC and SIZ. Show they are working properly by applying the clock signal by hand an by following the LEDs.



Control Unit Structure
(A suggestion)