AMERICAN INTERNATIONAL UNIVERSITY BANGLADESH
Faculty of Engineering

Laboratory Report Cover Sheet

Students must complete all details except the faculty use part.

Please submit all reports to your subject supervisor or the office of the concerned faculty.

Laboratory Title: Designing Multiplexer and Demultiplexer, Encoder and Decoder circuit

Experiment Number: 04 Due Date: 26.10.22 Semester: _____

Subject Code: EEE____ Subject Name: Digital Logic and Circuits. Section: I

Course Instructor: Dr. Mohammad Shidujaman Degree Program: _____

Declaration and Statement of Authorship:

1. I/we hold a copy of this report, which can be produced if the original is lost/ damaged.
2. This report is my/our original work and no part of it has been copied from any other student's work or from any other source except where due acknowledgement is made.
3. No part of this report has been written for me/us by any other person except where such collaboration has been authorized by the lecturer/teacher concerned and is clearly acknowledged in the report.
4. I/we have not previously submitted or currently submitting this work for any other course/unit.
5. This work may be reproduced, communicated, compared and archived for the purpose of detecting plagiarism.
6. I/we give permission for a copy of my/our marked work to be retained by the School for review and comparison, including review by external examiners.

I/we understand that

7. Plagiarism is the presentation of the work, idea or creation of another person as though it is your own. It is a form of cheating and is a very serious academic offence that may lead to expulsion from the University. Plagiarized material can be drawn from, and presented in, written, graphic and visual form, including electronic data, and oral presentations. Plagiarism occurs when the origin of the material used is not appropriately cited.
8. Enabling plagiarism is the act of assisting or allowing another person to plagiarize or to copy your work

Group Number (if applicable): 04 ☐ Individual Submission ☑ Group Submission

No.	Student Name	Student Number	Student Signature	Date
Submitted by:				
1	Sakib Ahmed Sarwar	19-39375-1	Sarwar	26.10.22
Group Members: 7.	Akash Bhadra	19-39995-1	Akash	26.10.22
2	Rahman, Mohammed Mofizur	19-40120-1	M. Rahman	26.10.22
3	MD. Ahasanul Islam	19-40396-1	Ahasanul	26.10.22
4	Laila, Summya Akhter	20-42099-1	Summya	26.10.22
5	Rifat, Md. Johirul Islam	20-41888-1	Rifat	26.10.22
6.	Rowzatul Jannat	20-43976-2	Jannat	26.10.22

For faculty use only:

Total Marks: _____ **Marks Obtained:** _____

Faculty comments _____

Title: Designing Multiplexer (MUX) and Demultiplexer (Demux), Encoder and Decoder Circuits.

Introduction: In this experiment students will learn how to design and implement multiplexer (MUX) and demultiplexers (DeMUX) of different sizes using basic logic gates. They will also learn how to construct bigger multiplexer using smaller multiplexer. Students will also construct encoder and decoder circuits. Encoder and decoder circuits are very useful in information transmission, conversion, compression and maintaining the secrecy of any information.

Theory and Methodology:

Part 1: Multiplexer and Demultiplexer

A multiplexer (or mux) is a device that selects one of several inputs and forwards the selected input into a single line. A multiplexer of 2^n inputs has n selection lines, which are used to select which input has to be sent to the output. A multiplexer is also called a data selector.

A demultiplexer (or demux) is a device taking a single input and selecting one of many data-output-lines, which is connected to the single input.

Multiplexer :

In computer system, it is often necessary to choose data from exactly one of a number of possible sources. Suppose that there are four sources of data, provided as input signals D_0, D_1, D_2 and D_3. The values of these signals change in time, perhaps at regular intervals. We want to design a circuit that produces an output that has the same value as either D_0 or D_1 or D_2 or D_3. dependent on the values of two selection pins S_1 and S_0. Here the number of selection pin is two. Four combinations are possible using these two selection pins S_1 and S_0, such as $(S_1, S_0) = (0,0), (0,1), (1,0), (1,1)$. Each combination is dedicated for each input. Let us consider the output variable is f, Now if $S_1 = 0$ and $S_0 = 0$ then $f = D_0$, if $S_1 = 0$ and $S_0 = 1$ then $f = D_1$, if $S_1 = 1$ and $S_0 = 0$ then $f = D_2$ and if $S_1 = 1$ and $S_0 = 1$ then $f = D_3$.

It is important to know that there is a relationship between the number of input and the number of selection pin. If the number of selection pin of a Mux is n, then maximum 2^n inputs are possible for that Mux. And the Mux will be called as 2^n to 1 line Mux. The Mux we are going to design is a 4 to 1 Mux. There could be also 2 to 1 Mux, 8 to 1 Mux, 16 to 1 Mux etc.

For our design, there are 4 inputs and 2 selection pins. So actually we have 6 inputs. Now if we draw the truth table for 6 different inputs, there will be 64 input combinations. But fortunately we can do it in a more convenient way as given below.

Table : 1

S_1	S_0	f
0	0	D_0
0	1	D_1
1	0	D_2

1	0	0	0	Din	0
1	1	0	0	0	Din

From the above truth table we can write the functions for D_0, D_1, D_2 and D_3 as given below.

$D_0 = S_1 \bar{S_0} Din$ — (2)

$D_1 = S_1 S_0 Din$ — (3)

$D_2 = S_1 \bar{S_0} Din$ — (4)

$D_0 = \bar{S_1} \bar{S_0} Din$ — (5)

The circuit for 1 to 4 line demux is given below.

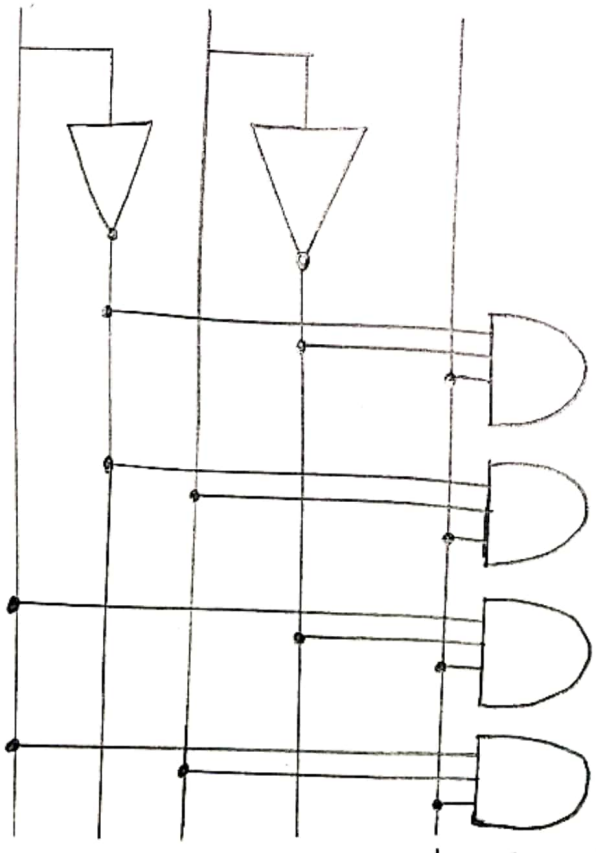


Fig2: 1 to 4 Demultiplexer

It is also possible to construct 4 to 1 multiplexer (and 1 to 4 demultiplexer) using 2 to 1 multiplexers (1 to 2 demultiplexers) only. Figure 3 and figure 4 show the construction of 4 to 1 multiplexer using 2 to 1 multiplexers and 1 to 4 demultiplexer using 1 to 2 demultiplexers only.

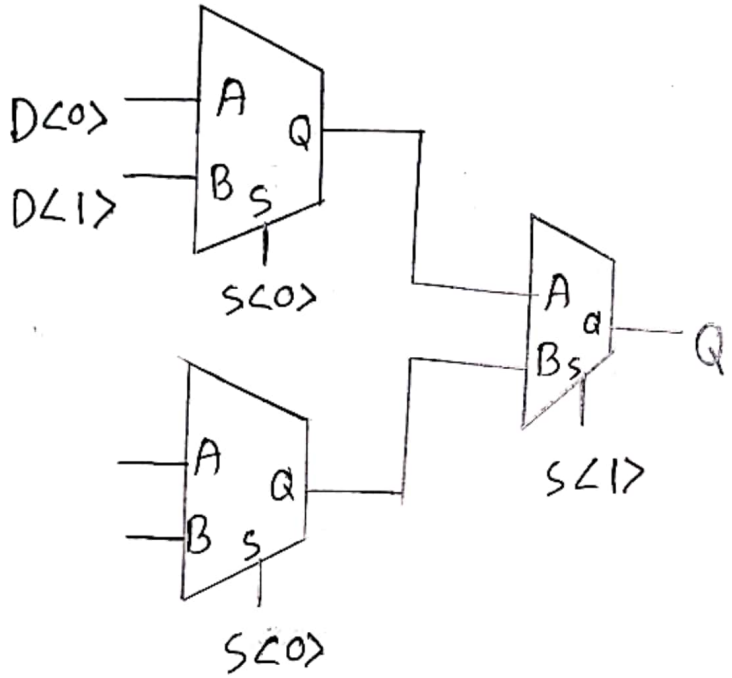


Figure 3: 4 to 1 multiplexer using 2 to 1 multiplexers

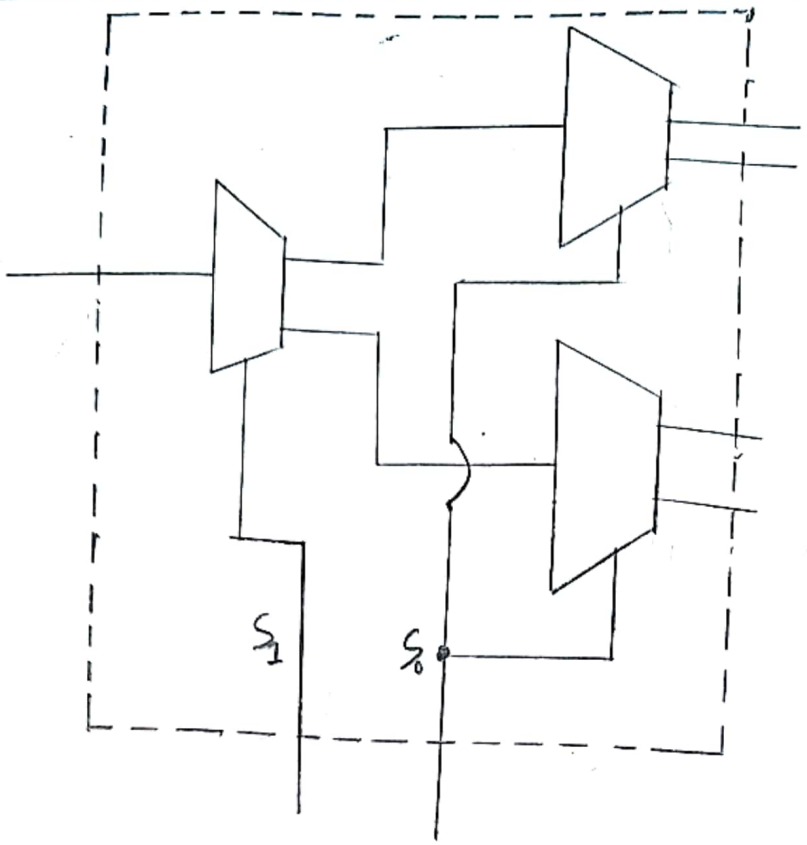


figure 4: 1 to 4 demultiplexer using 1 to 2 demultiplexers.

Part 2 : Encoder and Decoder:

An encoder is a device or a circuit that converts information from one formate or code to another. A decoder does the reverse operation of the encoder. It undoes the encoding so that the original information can be retrieved. Both the encoder and decoder are combinational circuits.

Encoding and decoding are very widely used ideas. They have applications in electronic circuits, software programs, medical devices, telecommunication and many others. In this experiment a very basic 2 to 4 line decoder and a decimal to BCD encoder will be constructed.

A decoder can convert binary information from n input lines to maximum of 2^n unique output lines. The 2 to 4 line decoder will take inputs from two lines and convert them to 4 lines.

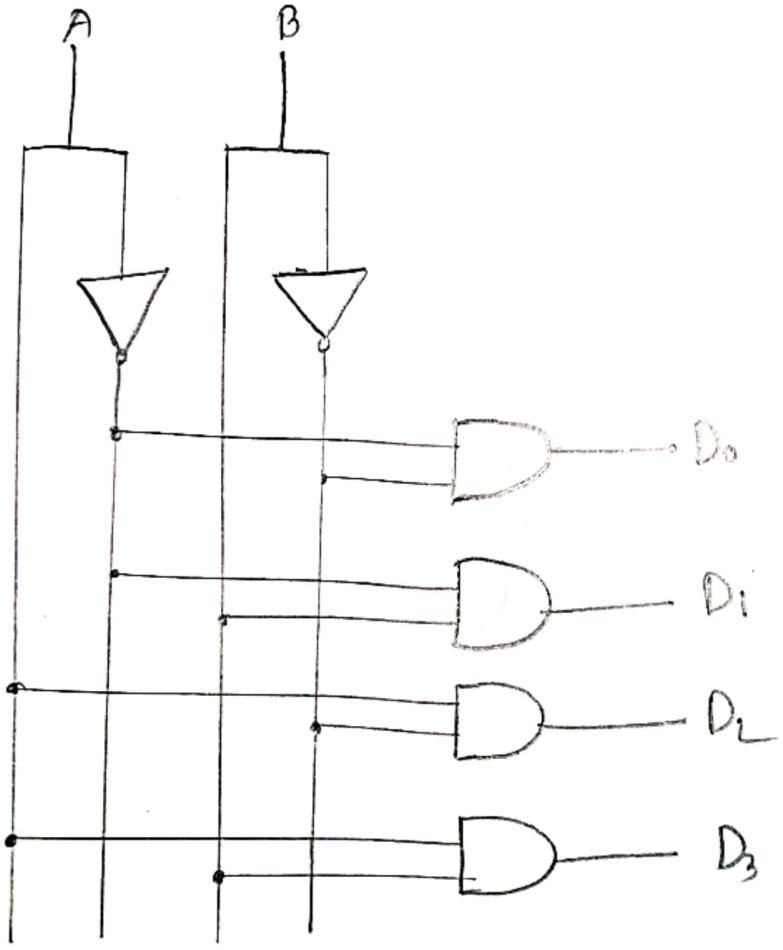


Fig 1 : 2 to 4 line decoder

The expressions for implementing 2-to-4 line decoder-

$D0 = A'B'$

$D1 = A'B$

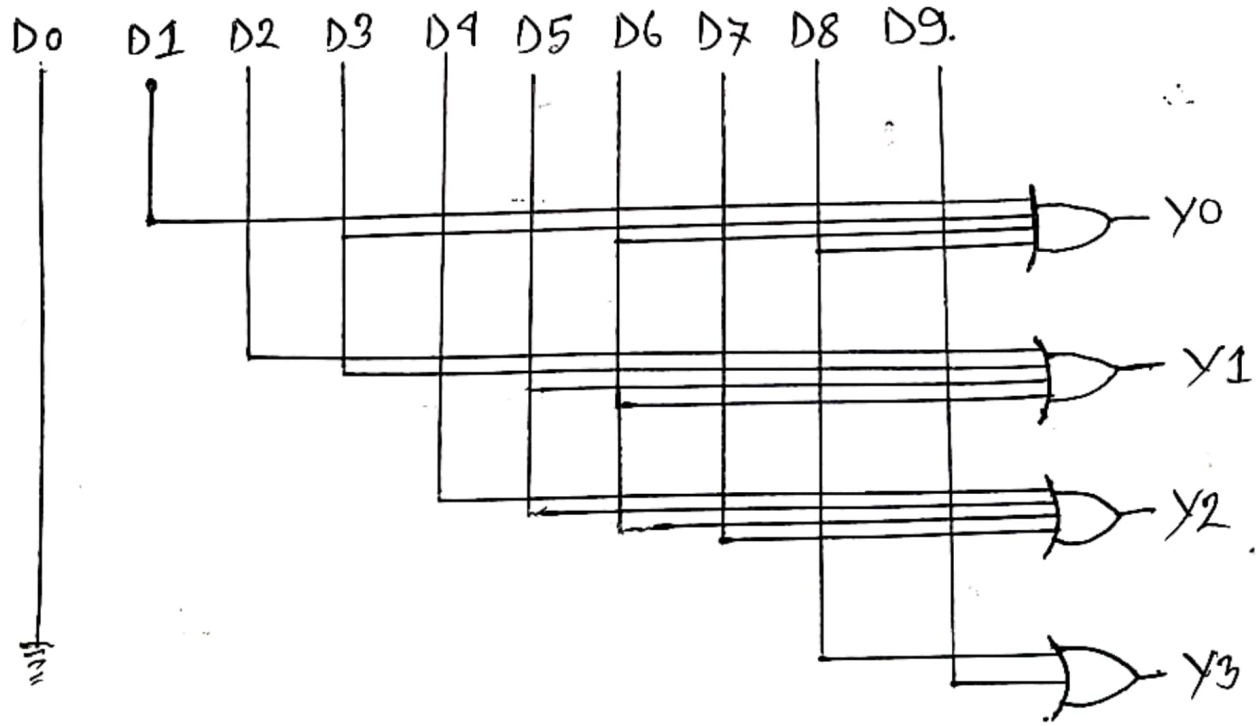
$D2 = AB'$

$D3 = AB$

Truth table for 2-4 line decoder is given below-

A	B	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

A decimal to BCD encoder converts a decimal number into Binary Coded Decimal (BCD).



The expressions for implementing the decimal to BCD encoder-

$Y0 = D1 + D3 + D5 + D7 + D9$

$Y1 = D2 + D3 + D6 + D7$

$Y2 = D4 + D5 + D6 + D7$

$Y3 = D8 + D9$

Truth table for decimal to BCD encoder is given below-

Dec.	Y3	Y2	Y1	Y0
D0	0	0	0	0
D1	0	0	0	1
D2	0	0	1	0
D3	0	0	1	1
D4	0	1	0	0
D5	0	1	0	1
D6	0	1	1	0
D7	0	1	1	1
D8	1	0	0	0
D9	1	0	0	1

Priority Encoder :

A priority encoder is a circuit or algorithm that compresses multiple binary inputs into a smaller number of outputs. The output of a priority encoder is the binary representation of the original number starting from zero of the most significant input bit. They are often used to control interrupts requests by acting on the highest priority request. If two or more inputs are given at the same time, the input having the highest priority will take precendence.

In this experiment a 4-to 2 priority encoder with a priority sequence of 2, 1, 3, 0 has been shown. It means, in this priority encoder 2 has the highest priority and 0 has the lowest. If 2 is high then other numbers are ignored and output would be binary representation of 2, i.e., $Y_1 Y_0 = 10$. If 2 is found to be low, then next priority is given no 1.

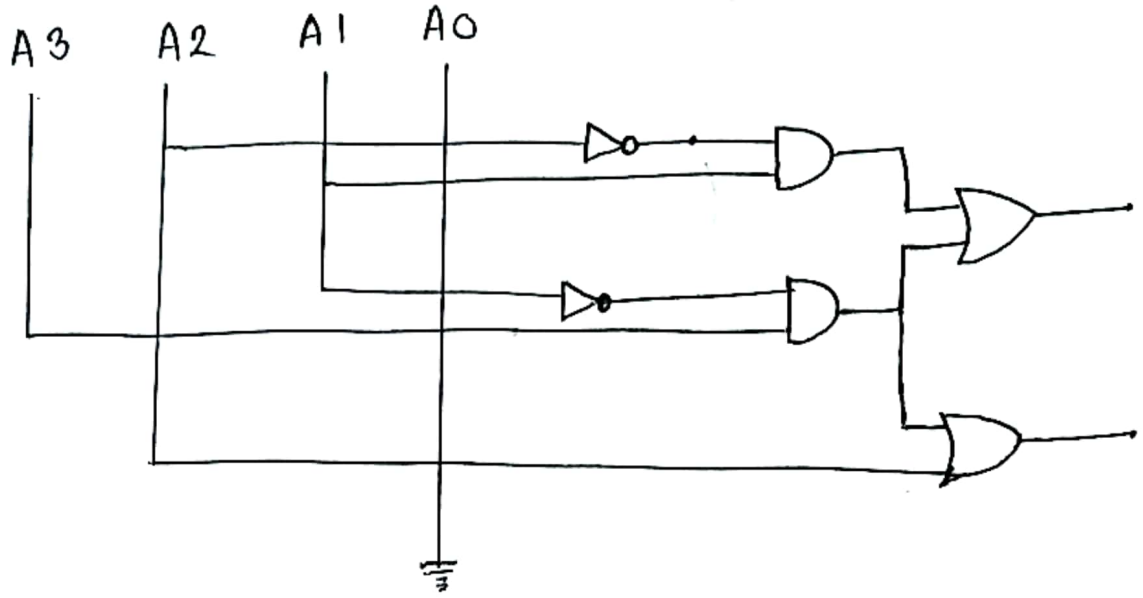


Fig 3: 4-to 2 priority encoder with a priority sequence of 2,1,3,0

The expressions for implementing the above priority encoder-

$Y0 = A2'.A1 + A3.A2'.A1'$

$Y1 = A2 + A3.A2'.A1'$

Truth table for this priority encoder is given below-

A3	A2	A1	A0	Y1	Y0
X	1	X	X	1	0
X	0	1	X	0	1
1	0	0	X	1	1
0	0	0	1	0	0

Apparatus:

1. NOT Gate - IC 7404
2. AND Gate - IC 7408
3. OR Gate - 5 input OR
   4 input OR
   2 input OR

Precautions:

1. Making sure that all the LED's and the toggle switches of the trainer board are working properly.
2. We have to be careful about shorting any connection.

Experimental Procedure:

1. Connect the circuit according to the figures.
2. Using the toggle switches on the trainer board for providing input signal to the circuits.
3. Apply the input signals and observe and note the corresponding output signals.

Results and Discussion:

In this experiment we have learned to design and implement multiplexers and demultiplexers using basic logic gates. The overall result was satisfactory but putting the circuit together was a bit tricky. To begin we had to understand multiplexer, demultiplexer, encoder and decoder. Then, ~~without~~ trying for a couple of times we have successfully constructed the circuit on bread board. finally the results were used to verify our truth-table, and they all matched

Reference:

http. www. tutorials point. com/ computer - logical - organization . htm.

lab manual - 4