Curriculum Vitae

Akihiro Hayashi

Contents

Summary

Dr. Hayashi is a senior research scientist at Georgia Institute of Technology. He has over ten years of experience in conducting and leading research in the programming languages and parallel computing areas. His research interests include:

- Parallel and Distributed Programming Models
- Automatic Parallelizing Compilers
- Just-In-Time Compilers
- Parallel and Distributed Runtime Systems
- Machine-learning for Compiler/Runtime Optimizations
- Resilience for Parallel and Distributed Systems
- GPUs
- Quantum Computing

Education

Ph.D., Computer Science, Waseda University, Tokyo, Japan - 2012

Thesis : *Studies on Automatic Parallelization for Heterogeneous and Homogeneous Multicore Processors*

Advisor : Professor Hironori Kasahara

M.E., Computer Science, Waseda University, Tokyo, Japan - 2008

Thesis : *Study on Compiler Cooperative Heterogeneous Multicore Architecture*

Advisor : Professor Hironori Kasahara

B.E., Computer Science, Waseda University, Tokyo, Japan - 2007

Thesis : *Parallel Code Generation Scheme for Hierarchical Multigrain Parallel Processing on Heterogeneous Multicore Processor*

Advisor : Professor Hironori Kasahara

Professional Experience

Professional

Senior Research Scientist, Georgia Institute of Technology, Atlanta, GA, USA - 2019-present Responsible for conducting and leading research on 1) enabling resiliency in asynchronous many-task (AMT) programming models, 2) an actor-based programming model for large-scale systems, 3) multi-level programming models for Graphics Processing Units (GPUs) and SIMD (Single-Instruction Multiple Data) units, 4) code generation and optimizations for Graphics Processing Units (GPUs), 5) automatic construction of compiler/runtime heuristics using machine-learning techniques, and 6) programming models for quantum classical systems.

Research Scientist, Rice University, Houston, TX, USA - 2015-2019 Responsible for conducting and leading research on 1) LLVM-based optimizations for large-scale systems, 2) code generation and optimizations for Graphics Processing Units (GPUs), 3) automatic construction of compiler/runtime heuristics using machine-learning techniques, and 4) enabling resiliency in asynchronous many-task (AMT) programming models.

Postdoctoral Researcher, Rice University, Houston, TX, USA - 2013-2015 Conducted research in the area of compiler and runtime support for parallel languages such as Habanero-Java. In particular, I worked on high-level language constructs and parallel code generation for GPUs while maintaining precise exception semantics on GPUs.

Assistant Professor, Waseda University, Tokyo, Japan - 2012-2013 Conducted research on automatic parallelizing compiler and compiler-directed power reduction techniques in collaboration with many companies in Japan. More specifically , I worked on parallelizing and optimizing 1) automotive engine control software with TOYOTA and Denso, 2) dose calculation software for heavy-ion therapy with Mitsubishi Electric, 3) smartphone applications on Android platforms with Fujitsu Ltd., and 4) multimedia applications with Olympus Corporation.

Instructor for freshman-level 1) computer literacy class and 2) programming class with C language in Spring/Fall 2012.

Research Associate, Waseda University, Tokyo, Japan - 2010-2012 Conducted research on automatic parallelization and power reduction techniques for embedded heterogeneous multi-core processors. In addition, I worked on the automatic parallelization and optimization of a clinically-used dose calculation program for heavy-ion therapy in collaboration with Mitsubishi Electric. Based on experimental results on an IBM POWER7 platform, our optimized version was over 50x faster than the conventional version.

Research Associate, Global COE Program, Waseda University, Tokyo, Japan - 2007-2010 Conducted research on automatic parallelization and power reduction techniques for embedded heterogeneous multi-core processors in collaboration with Hitachi Ltd. and Renesas Electronics Corporation (formerly known as Renesas Technology). This work was partially saupported by one of the global centers of excellence (GCOE) program named "International research and education center for Ambient SoC" established by Japan's Ministry of Education, Culture, Sports, Science, and Technology (MEXT).

Teaching

Courses

- Computer Literacy, Waseda University, Spring 2012. (English Course)
- C Programming, Waseda Univerisity, Fall 2012. (English Course)
- Science and Engineering Lab., Waseda Univerisity, Spring/Fall 2012. (Japanese Course)

Tutorials

- Fundamentals of CUDA Programming, Waseda University, Spring/Fall 2018
- Fundamentals of FPGA Programming, Waseda University, Spring 2018

Awards

- IEEE Senior Member, 2021
- Outstanding Paper award, The 2020 International Conference on High Performance Computing & Simulation (HPCS2020), Mar 2021. (Tiago Carneiro, Nouredine Melab, Akihiro Hayashi, Vivek Sarkar)
- Best Expo Exhibit, 28th Annual International Conference on Computer Science and Software Engineering (CASCON2018), November 2018 (1 best exhibit out of 72 exhibits). (Akihiro Hayashi, Gita Koblents, Max Grossman, Kazuaki Ishizaki, Alon Shalev Housfater, Jimmy Kwa, Vivek Sarkar)
- Best Expo Exhibit, 27th Annual International Conference on Computer Science and Software Engineering (CASCON2017), November 2017 (2 best exhibit out of 54 exhibits). (Akihiro Hayashi, Gita Koblents, Max Grossman, Kazuaki Ishizaki, Alon Shalev Housfater, Jimmy Kwa, Vivek Sarkar)
- Encouragement award, IPSJ Symposium on Embedded Systems, October 2013. (Dan Umeda, Yohei Kanehagi, Hiroki Mikami, Akihiro Hayashi, Mitsuhiro Tani, Hiroshi Mori,Keiji Kimura, Hironori Kasahara)
- Best feature award, COOL Chips XVI, IEEE Symposium on Low Power and High-Speed Chips, April 2013. (Yohei Kishimoto, Hiroki Mikami, Keiichi Nakano, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara,)
- Encouragement award, IPSJ Symposium on Embedded Systems, October 2012. (Yohei Kishimoto, Hiroki Mikami, Keiichi Nakano, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara)
- IPSJ SIG recommended Ph.D thesis, September 2012.
- Best presentation award, 5th GCOE Symposium, September 2009.

Professional Committees

Conference Committees

- Program Committee Member, The 9th Annual Chapel Implementers and Users Workshop (CHIUW), June 2022.
- External Review Committee Member, 27th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP), February 2022.
- Program Committee Member, 31st Annual International Conference on Computer Science and Software Engineering (CASCON), November 2021
- Program Committee Member, Workshop on Programming Environments for Heterogeneous Computing (PEHC), November 2021 (co-located with SC2021)
- Program Committee Member, 8th International Workshop on Large-scale HPC Application Modernization (LHAM), November 2021 (co-located with CANDAR2021)
- Program Committee Member, 2nd International Workshop on Parallel Optimization using/for Multi- and Many-core High Performance Computing (POMCO), December 2020 (co-located with HPCS2020)
- Program Committee Member, 29th Annual International Conference on Computer Science and Software Engineering (CASCON), November 2019

- Program Committee Member, 7th International Workshop on Computer Systems and Architectures (CSA), November 2019.
- Program Committee Member, 6th ACM SIGPLAN International Workshop on AI-Inspired and Empirical Methods for Software Engineering on Parallel Computing Systems (AI-SEPS2019, co-located with SPLASH2018).
- Program Committee Member, 32nd International Workshop on Languages and Compilers for Parallel Computing (LCPC), October 2019
- Program Committee Member, 33th IEEE International Parallel & DistributedProcessing Symposium (IPDPS), May 2019
- Program Committee Member, 6th International Workshop on Legacy-scale HPC Application Modernization (LHAM2018, co-located with CANDAR2018).
- Program Committee Member, 5th ACM SIGPLAN International Workshop on AI-Inspired and Empirical Methods for Software Engineering on Parallel Computing Systems (AI-SEPS2018, co-located with SPLASH2018).
- Program Committee Member, 28th Annual International Conference on Computer Science and Software Engineering (CASCON2018).
- External Review Committee Member, 23rd International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS2018).
- Program Committee Member, 5th International Workshop on Legacy HPC Application Migration(LHAM2017, co-located with CANDAR2017).
- Program Committee Member, 4th ACM SIGPLAN International Workshop on Software Engineering for Parallel Systems (SEPS2017, co-located with SPLASH2017).
- Program Committee Member, 22nd ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP2017).
- Program Committee Member, 22nd IEEE International Conference on Parallel and Distributed Systems (ICPADS2016).
- Program Committee Member, 3rd International Workshop on Software Engineering for Parallel Systems (SEPS2016, co-located with SPLASH2016).
- Technical Program Committee Member, 29th IEEE International Parallel & DistributedProcessing Symposium (IPDPS2015).
- Program Committee Member, IPSJ Symposium on Advanced Computing Systems and Infrastructures (SACSIS2013).
- Local arrangement Co-chair, 25th International Workshop on Languages and Compilers for Parallel Computing (LCPC2012).

Journal Reviewers

- IEEE Micro (2022)
- ACM Transactions on Architecture and Code Optimization (TACO) (2021, 2022)
- ACM Transactions on Programming Languages and Systems (TOPLAS) (2018)
- Arabian Journal for Science and Engineering (2017)
- Journal of Parallel and Distributed Computing (JDPC) (2017)
- ACM Transactions on Embedded Computing Systems (TECS)(2015)
- IEEE Transactions on Parallel and Distributed Systems (TPDS)(2015)
- IPSJ (Information Processing Society of Japan) Journals (2015, 2014)
- IEICE (The Institute of Electronics, Information and Communication Engineers) Transactions on Information and Systems (2020, 2013, 2012)

Journal Editors

- Guest Associate Editor, IEICE (The Institute of Electronics, Information and Communication Engineers) Special Section on Low-Power and High-Speed Chips (2022)

External Reviewers

- The IEEE Cluster Conference(IEEE Cluster 2017)
- International Conference on Network and Parallel Computing (NPC2017, NPC2016)
- International Conference on Parallel Processing (ICPP2016)
- International Conference on Parallel Architectures and Compilation Techniques (PACT2015)
- International Conference for High Performance Computing, Networking, Storage and Analysis (SC13)

- International Conference on Supercomputing (ICS2018, ICS2013)
- International Conference on Parallel and Distributed Systems (ICPADS2013)
- International Conference on Computer Design (ICCD2014, ICCD2013, ICCD2012)
- International Workshop on Languages and Compilers for Parallel Computing (LCPC2018, LCPC2015, LCPC2014, LCPC2013)

Specification Committees

- OpenSHMEM Application Programming Interface (2022-)

Publications

Ph.D Dissertation

- **Studies on Automatic Parallelization for Heterogeneous and Homogeneous Multicore Processors**. Akihiro Hayashi. Waseda University. February 2012.

Refereed Papers

Conference and Journal Publications

1. **Automatic Parallelization of Python programs for Distributed Heterogeneous Computing**. Jun Shirako, Akihiro Hayashi, Sri Raj Paul, Alexey Tumanov and Vivek Sarkar. 28th International European Conference on Parallel and Distributed Computing (Euro-Par2022), August 2022. DOI
2. **A Productive and Scalable Actor-based Programming System for PGAS Applications**. Sri Raj Paul, Akihiro Hayashi, Kun Chen, and Vivek Sarkar. 22th International Conference on Computational Science (ICCS2022), June 2022. DOI
3. **Qulacs: a fast and versatile quantum circuit simulator for research purpose**. Yasunari Suzuki, Yoshiaki Kawase, Yuya Masumura, Yuria Hiraga, Masahiro Nakadai, Jiabao Chen, Ken M. Nakanishi, Kosuke Mitarai, Ryosuke Imai, Shiro Tamiya, Takahiro Yamamoto, Tennin Yan, Toru Kawakubo, Yuya O. Nakagawa, Yohei Ibe, Youyuan Zhang, Hirotsugu Yamashita, Hikaru Yoshimura, Akihiro Hayashi, Keisuke Fujii. Quantum Journal (Quantum 5, 559). DOI
4. **Towards Chapel-based Exascale Tree Search Algorithms: dealing with multiple GPU accelerators**. Tiago Carneiro, Nouredine Melab, Akihiro Hayashi, Vivek Sarkar. 18th International Conference on High Performance Computing & Simulation (HPCS2020)
5. **Compiler-Support for Critical Data Persistence in NVM**. Reem Elkhouly, Mohammad Alshboul, Akihiro Hayashi, Yan Solihin, Keiji Kimura. ACM Transactions on Architecture and Code Optimization (TACO). DOI
6. **Enabling Resilience in Asynchronous Many-Task Programming Models**. Sri Raj Paul, Akihiro Hayashi, Nicole Slattengren, Hemanth Kolla, Matthew Whitlock, Seonmyeong Bak, Keita Teranishi, Jackson Mayo, Vivek Sarkar. 25th International European Conference on Parallel and Distributed Computing (Euro-Par2019), August 2019. DOI
7. **Performance Evaluation of OpenMP's Target Construct on GPUs**. Akihiro Hayashi, Jun Shirako, Ettore Tiotto, Robert Ho, Vivek Sarkar. International Journal of High Performance Computing and Networking (IJHPCN), Vol. 13, No. 1, 2019. DOI
8. **Optimized Two-level Parallelization for GPU Accelerators using the Polyhedral Model**. Jun Shirako, Akihiro Hayashi, Vivek Sarkar. 26th International Conference on Compiler Construction (CC2017), February 2017. DOI
9. **Compiling and Optimizing Java 8 Programs for GPU Execution**. Kazuaki Ishizaki, Akihiro Hayashi, Gita Koblents, Vivek Sarkar. 24th International Conference on Parallel Architectures and Compilation Techniques (PACT2015), October 2015. DOI
10. **Machine-Learning-based Performance Heuristics for Runtime CPU/GPU Selection**. Akihiro Hayashi, Kazuaki Ishizaki, Gita Koblents, Vivek Sarkar. 12th International Conference on the Principles and Practice of Programming in Java (PPPJ2015), September 2015. DOI

11. **Automatic Parallelization of Designed Engine Control C Codes by MATLAB/Simulink**. Dan Umeda, Yohei Kanehagi, Hiroki Mikami, Akihiro Hayashi, Mitsuhiro Tani, Hiroshi Mori, Keiji Kimura, Kasahara Hironori, IPSJ Journal, August, 2014. (in Japanese)
12. **Accelerating Habanero-Java Program with OpenCL Generation**. Akihiro Hayashi, Max Grossman, Jisheng Zhao, Jun Shirako, Vivek Sarkar. 10th International Conference on the Principles and Practice of Programming in Java (PPPJ2013), September 2013. DOI
13. **Automatic Parallelization, Performance Predictability and Power Control for Mobile-Applications**. Dominic Hillenbrand, Akihiro Hayashi, Hideo Yamamoto, Keiji Kimura, Hironori Kasahara. 16th IEEE Symposium on Low-Power and High-Speed Chips (CoolChips XVI), April 2013.
14. **Parallelization of Automotive Engine Control Software On Embedded Multi-core Processor Using OSCAR Compiler**. Yohei Kanehagi, Dan Umeda, Akihiro Hayashi, Keiji Kimura and Hironori Kasahara, 16th IEEE Symposium on Low-Power and High-Speed Chips (CoolChips XVI), April 2013.
15. **Parallel processing of multimedia applications on TILEPro64 using OSCAR API for embedded multicore**. Yohei Kishimoto, Hiroki Mikami, Keiichi Nakano, Akihiro Hayashi, Keiji Kimura and Hironori Kasahara, IPSJ Symposium on Embedded System (ESS2012), October 2012. (in Japanese)
16. **Automatic Parallelization of Dose Calculation Engine for A Particle Therapy**. Akihiro Hayashi, Takuji Matsumoto, Hiroki Mikami, Keiji Kimura, Keiji Yamamoto, Hironori Saki, Yasuyuki Takatani, Hironori Kasahara, IPSJ Symposium on High Performance Computing and Computer Science (HPCS2012), January 2012. (in Japanese)
17. **Parallelizing Compiler Framework and API for Heterogeneous Multicores**. Akihiro Hayashi, Yasutaka Wada, Takeshi Watanabe, Takeshi Sekiguchi, Masayoshi Mase, Jun Shirako, Keiji Kimura and Hironori Kasahara, IPSJ Transactions on Advanced Computing Systems (ACS), Vol.5, No.1, pp.68-79, November. 2011. (in Japanese)
18. **A Parallelizing Compiler Cooperative Heterogeneous Multicore Processor Architecture**. Yasutaka Wada, Akihiro Hayashi, Takeshi Masuura, Jun Shirako, Hirofumi Nakano, Hiroaki Shikano, Keiji Kimura, and Hironori Kasahara, Transactions on High-Performance Embedded Architectures and Compilers IV (HiPEAC IV), Lecture Note in Computer Science, Springer, Vol. 6760, pp. 215-233, November 2011.
19. **A 45nm Heterogeneous Multi-core SoC Supporting an over 32-bits Physical Address Space for Digital Appliance**. Takumi Nito, Yoichi Yuyama, Masayuki Ito, Yoshikazu Kiyoshige, Yusuke Nitta, Osamu Nishii, Atsushi Hasegawa, Makoto Ishikawa, Tetsuya Yamada, Junichi Miyakoshi, Koichi Terada, Tohru Nojiri, Masashi Takada, Makoto Satoh, Hiroyuki Mizuno, Kunio Uchiyama, Yasutaka Wada, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara, Hideo Maejima,13th IEEE Symposium on Low-power and High-Speed Chips (COOL Chips XIII), April 2010.
20. **Parallelization of MP3 Encoder using Static Scheduling on a Heterogeneous Multicore**. Yasutaka Wada, Akihiro Hayashi, Takeshi Masuura, Jun Shirako, Hirofumi Nakano, Hiroaki Shikano, Keiji Kimura, Hironori Kasahara, Transactions of IPSJ on Computing Systems, Vol. 49 (ACS), 2008 (in Japanese)
21. **Software-Cooperative Power-Efficient Heterogeneous Multi-Core for Media Processing**. Hiroaki Shikano, Masaki Ito, Kunio Uchiyama, Toshihiko Odaka,Akihiro Hayashi, Takeshi Masuura, Masayoshi Mase, Jun Shirako, Yasutaka Wada, Keiji Kimura, Hironori Kasahara, 13th Asia and South Pacific Design Automation Conference (ASP-DAC2008), January 2008.

Workshop Proceedings

1. **A Multi-Level Platform-Independent GPU API for High-Level Programming Models**. Akihiro Hayashi, Sri Raj Paul and Vivek Sarkar, HPC on Heterogeneous Hardware Workshop (H3), June 2022. (co-located with ISC22) DOI
2. **Integrating Inter-Node Communication with a Resilient Asynchronous Many-Task Runtime System**. Sri Raj Paul, Akihiro Hayashi, Matthew Whitlock, Seonmyeong Back, Keita Teranishi, Jackson Mayo, Max Grossman, Vivek Sarkar, International IEEE workshop on Exascale MPI (ExaMPI), November 2020. (co-located with SC20) DOI

3. **GPUIterator: bridging the gap between Chapel and native languages**. Akihiro Hayashi, Sri Raj Paul, Vivek Sarkar, The ACM SIGPLAN 6th Annual Chapel Implementers and Users Workshop (CHIUW), June 2019. (co-located with PLDI2019/ACM FCRC2019) DOI
4. **A Unified Runtime for PGAS and Event-Driven Programming**. Sri Raj Paul, Kun Chen, Akihiro Hayashi, Max Grossman, Vivek Sarkar, International IEEE Workshop on Extreme Scale Programming Models and Middleware (ESPM2), November 2018. (co-located with SC18) DOI
5. **Exploration of Supervised Machine Learning Techniques for Runtime Selection of CPU vs. GPU Execution in Java Programs**. Gloria Kim, Akihiro Hayashi, Vivek Sarkar. Fourth Workshop on Accelerator Programming Using Directives (WACCPD), November 2017. (co-located with SC17) DOI
6. **Chapel-on-X: Exploring Tasking Runtimes for PGAS Languages**. Akihiro Hayashi, Sri Raj Paul, Max Grossman, Jun Shirako, Vivek Sarkar. Third IEEE Workshop on Extreme Scale Programming Models and Middleware (ESPM2), November 2017. (co-located with SC17) DOI
7. **Exploring Compiler Optimization Opportunities for the OpenMP 4.x Accelerator Model on a POWER8+GPU Platform**. Akihiro Hayashi, Jun Shirako, Ettore Tiotto, Robert Ho, Vivek Sarkar. Third Workshop on Accelerator Programming Using Directives (WACCPD), November 2016. (co-located with SC16) DOI
8. **LLVM-based Communication Optimizations for PGAS Programs**. Akihiro Hayashi, Jisheng Zhao, Michael Ferguson, Vivek Sarkar. 2nd Workshop on the LLVM Compiler Infrastructure in HPC (LLVM), November, 2015. (co-located with SC15) DOI
9. **LLVM Optimizations for PGAS Programs -Case Study: LLVM Wide Optimization in Chapel-**. Akihiro Hayashi, Rishi Surendran, Jisheng Zhao, Michael Ferguson, Vivek Sarkar. 1st Chapel Implementers and Users Workshop (CHIUW2014), May 2014. (co-located with IPDPS)
10. **Speculative Execution of Parallel Programs with Precise Exception Semantics on GPUs**. Akihiro Hayashi, Max Grossman, Jisheng Zhao, Jun Shirako, Vivek Sarkar. 26th International Workshop on Languages and Compilers for Parallel Computing (LCPC2013), September 2013. (co-located with CnC) DOI
11. **Reconciling Application Power Control and Operating Systems for Optimal Power and Performance**. Dominic Hillenbrand, Yuuki Furuyama, Akihiro Hayashi, Mikami Hiroki, Keiji Kimura, Hironori Kasahara. 8th International Workshop on Reconfigurable Communication-centric Systemson-Chip (ReCoSoC2013), Germany, 2013.
12. **Automatic Parallelization of Hand Written Automotive Engine Control Codes Using OSCAR Compiler**. Dan Umeda, Yohei Kanehagi, Hiroki Mikami, Akihiro Hayashi, Keiji Kimura and Hironori Kasahara. 17th Workshop on Compilers for Parallel Computing (CPC2013), July 2013.
13. **OSCAR API v2.1: Extensions for an Advanced Accelerator Control Scheme to a Low-Power Multicore API**. Keiji Kimura, Cecilia Gonzales-Alvarez, Akihiro Hayashi, Hiroki Mikami, Mamoru Shimaoka, Jun Shirako, Hironori Kasahara, 17th Workshop on Compilers for Parallel Computing (CPC2013), July 2013.a
14. **Automatic Design Exploration Framework for Multicores with Reconfigurable Accelerators.** Cecilia Gonzalez-Alvarez, Haruku Ishikawa, Akihiro Hayashi, Daniel Jimenez-Gonzalez, Carlos Alvarez, Keiji Kimura and Hironori Kasahara. 7th HiPEAC Workshop on Reconfigurable Computing (WRC2013), January, 2013.
15. **OSCAR Parallelizing Compiler and API for Real-time Low Power Heterogeneous Multicores**. Akihiro Hayashi, Mamoru Shimaoka, Hiroki Mikmi, Masayoshi Mase, Yasutaka Wada, Jun Shirako, Keiji Kimura, and Hironori Kasahara, 16th Workshop on Compilers for Parallel Computing (CPC2012), January 2012.
16. **Evaluation of Power Consumption at Execution of Multiple Automatically Parallelized and Power Controlled Media Applications on the RP2 Low-power Multicore**. Hiroki Mikami, Shumpei Kitaki, Masayoshi Mase, Akihiro Hayashi, Mamoru Shimaoka, Keiji Kimura, Masato Edahiro, and Hironori Kasahara, 24th International Workshop on Languages and Compilers for Parallel Computing (LCPC2011), September 2011.
17. **Parallelizing Compiler Framework and API for Power Reduction and Software Productivity of Real-time Heterogeneous Multicores**. Akihiro Hayashi, Yasutaka Wada, Takeshi Watanabe, Takeshi

Sekiguchi, Masayoshi Mase, Jun Shirako, Keiji Kimura and Hironori Kasahara, 23rd International Workshop on Languages and Compilers for Parallel Computing (LCPC2010), October 2010.

18. **Performance of OSCAR Multigrain Parallelizing Compiler on Multicore Processors**. Hiroki Mikami, Jun Shirako, Masayoshi Mase, Takamichi Miyamoto, Hirofumi Nakano, Fumiyo Takano, Akihiro Hayashi, Yasutaka Wada, Keiji Kimura, Hironori Kasahara, 14th Workshop on Compilers for Parallel Computing(CPC2009), January 2009.
19. **Parallelizing Compiler Cooperative Heterogeneous Multicore**. Yasutaka Wada, Akihiro Hayashi, Takeshi Masuura, Jun Shirako, Hirofumi Nakano, Hiroaki Shikano, Keiji Kimura, Hironori Kasahara, Workshop on Software and Hardware Challenges of Manycore Platforms (SHCMP2008), June 2008. (co-located ISCA2008)

Refereed Posters

1. **How Java runtime can execute practical Java programs on GPU**. Kazuaki Ishizaki,Gita Koblents,Akihiro Hayashi,Vivek Sarkar,Hiroshi Inoue. Poster Session, IPSJ Symposium on High Performance Computing and Computer Science (HPCS2015), May 2015. (in Japanese)
2. **Parallel Processing of Multimedia Applications on TILEPro64**. Yohei Kishimoto, Hiroki Mikami, Keiichi Nakano, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara. 16th IEEE Symposium on Low Power and High-Speed Chips (COOL Chips XVI), April 2013.
3. **Opportunities and Challenges of Application-Power Control in the Age of Dark Silicon**. Dominic Hillenbrand, Yuuki Furuyama, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara. 8th international conference on High-Performance and Embedded Architectures and Compilers (HiPEAC2013), January 2013.
4. **OSCAR Parallelizing Compiler Cooperative Heterogeneous Multi-core Architecture**. Akihiro Hayashi, Yasutaka Wada, Hiroaki Shikano, Teruo Kamiayama, Takeshi Watanabe, Takeshi Sekiguchi, Masayoshi Mase, 18th International Conference on Parallel Architectures and Compilation Techniques (PACT2009), September 2009.

Patents (include applications)

1. **Parallelism extraction method and method for making program**. Hironori Kasahara, Keiji Kimura, Akihiro Hayashi, Hiroki Mikami, Yohei Kanehagi, Dan Umeda, Mitsuo Sawada. LINK
2. **Parallelizing compile method, parallelizing compiler, parallelizing compile apparatus, and on-board apparatus**. Hiroshi Mori, Mitsuhiro Tani, Hironori Kasahara, Keiji Kimura, Dan Umeda, Akihiro Hayashi, Hiroki Mikami, Yohei Kanehagi, LINK
3. **Runtime gpu/cpu selection**. Gita Koblents, Alon Shalev Housfater, Kazuaki Ishizaki, Akihiro Hayashi. LINK

Invited Talks

1. **How to design human actions by digital technology?** The National Convention of IPSJ, March 2013. (in Japanese)

Presentations

1. **GPUAPI: Multi-level Chapel Runtime API for GPUs**. Akihiro Hayashi, Sri Raj Paul, Vivek Sarkar, 8th Annual Chapel Implementers and Users Workshop (CHIUW), June 2021.
2. **Exploring a multi-resolution GPU programming model for Chapel**. Akihiro Hayashi, Sri Raj Paul, Vivek Sarkar, 7th Annual Chapel Implementers and Users Workshop (CHIUW), May 2020. (co-located with IPDPS2020)
3. **Resilience With Asynchronous Many Task (AMT) Programming Models**. SIAM Conference on Parallel Processing for Scientific Computing
4. **Machine-learning-based Performance Heuristics for Runtime CPU/GPU Selection in Java**. 10th Workshop on Challenges for Parallel Computing, November 2015. (co- located with CASCON2015)

5. **LLVM-based Communication Optimizations for Chapel**. Chapel Lightning Talks Birds-of-a-Feather at International Conference for High Performance Computing, Networking, Storage and Analysis (SC14), November 2014.

Technical Reports

1. **Resilient Asynchronous Many Task Programming Model**. Keita Teranishi, Hemanth Kolla, Nicole Lemaster Slattengren, Matthew Whitlock, Jackson Mayo, Robert L. Clay, Sri Raj Paul, Akihiro Hayashi, Vivek Sarkar, August, 2018.
2. **Performance Evaluation of Hierarchical Barrier Hardware with OSCAR API Analyzer**. Akihiro Kawashima, Yohei Kanehagi, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ. V0l.2013-ARC-206-16 (SWoPP2013), July 2013. (in Japanese)
3. **An Investigation of Parallelization and Evaluation on Commercial Multi-core Smart Device**. Hideo Yamamoto, Takashi Goto, Tomohiro Hirano, Kouhei Muto, Hiroki Mikami, Dominic Hillenbrand, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol. 2013-OS-124, February 2013. (in Japanese)
4. **Parallelization of Automobile Engine Control Software on Multicore Processor**. Yohei Kanehagi, Dan Umeda, Hiroki Mikami, Akihiro Hayashi, Mitsuo Sawada, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2013-ARC195-2, January 2013. (in Japanese)
5. **Automatic parallelization of the GMS Earthquake simulator with OSCAR Compiler**. Mamoru Shimaoka, Hiroki Mikami, Akihiro Hayashi, Yasutaka Wada, Keiji Kimura, Hidekazu Morita, Kunio Uchiyama, Hironori Kasahara. Technical Report of IPSJ, Vol.2012-ARC194HPC137-26 (HOKKE2012), December 2012.
6. **Automatic parallelization with OSCAR API Analyzer: a cross-platform performance evaluation**. Cecilia Gonzalez-Alvarez, Yohei Kanehagi, Kosei Takemoto, Yohei Kishimoto, Kohei Muto, Hiroki Mikami, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2012-ARC194HPC137-10 (HOKKE2012), December 2012.
7. **Opportunities and Challenges of Application-Power Control in the Age of Dark Silicon**. Dominic Hillenbrand, Yuuki Furuyama, Akihiro Hayashi, Hiroki Mikami, Keiji Kimura, Hironori Kasahara, Technical Report of IPSJ, Vol.2012- ARC194HPC137-11(HOKKE2012), December 2012.
8. **Realization of 1 Watt Web Service with RP-X Low-power Multicore Processor**. Yuuki Furuyama, Mamoru Shimaoka, Hiroki Mikami, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2012-ARC-201-24 (SWoPP2012), August 2012. (in Japanese)
9. **Parallelization of Basic Engine Control Software Model on Multicore Processor**. Dan Umeda, Yohei Kanehagi, Hiroki Mikami, Akihiro Hayashi, Mituhiro Tani, Yuji Mori, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2012-ARC-201-22 (SWoPP2012), August 2012. (in Japanese)
10. **Automatic Parallelization of Dose Calculation Engine for A Particle Therapy on SMP Servers**. Akihiro Hayashi, Takuji Matsumoto, Hiroki Mikami, Keiji Kimura, Keiji Ya- mamoto, Hironori Saki, Yasuyuki Takatani, Hironori Kasahara. Technical Report of IPSJ, Vol.2011-ARC189HPC132-2 (HOKKE2011), November 2011. (in Japanese)
11. **Hiding I/O overheads with Parallelizing Compiler for Media Applications**. Akihiro Hayashi, Takeshi Sekiguchi, Masayoshi Mase, Yasutaka Wada, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2011-ARC-195OS117-14, April 2011. (in Japanese)
12. **Evaluation of Parallelizable C Programs by the OSCAR API Standard Translator**. Takuya Sato, Hiroki Mikami, Akihiro Hayashi, Masayoshi Mase, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2010-ARC-191-2, October 2010. (in Japanese)
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