

Akihiro Hayashi, Ph.D.



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2008-2012: Ph.D., Computer Science, Waseda University, Tokyo, Japan	3
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2025-present: Principal Research Scientist, Georgia Institute of Technology, Atlanta, GA, USA	3
2019-2025: Senior Research Scientist, Georgia Institute of Technology, Atlanta, GA, USA	3
2015-2019: Research Scientist, Rice University, Houston, TX, USA	3
2013-2015: Postdoctoral Researcher, Rice University, Houston, TX, USA	4
2012-2013: Assistant Professor, Waseda University, Tokyo, Japan	4
2010-2012: Research Associate, Waseda University, Tokyo, Japan	4
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Executive Summary

A Brief Autobiography Dr. Akihiro Hayashi is a Principal Research Scientist at Georgia Tech. He earned his Ph.D. in Computer Science from Waseda University in 2012 under the supervision of Prof. Hironori Kasahara. He then joined Prof. Vivek Sarkar's group at Rice University as a Postdoctoral Researcher, was promoted to Research Scientist in 2015, and moved to Georgia Tech in 2019, where he advanced to Senior Research Scientist and subsequently to Principal Research Scientist. His research spans programming models, compiler and runtime systems, and optimizations for large-scale and heterogeneous computing systems.

Research Contributions Dr. Hayashi's work spans parallel computing, with contributions reflected in his publications, software artifacts, and awards. He has authored 8 refereed journal publications and over 60 refereed conference publications, including in top venues such as Quantum, CC, EuroPar, ISC, IPDPS, PACT, and SC. To date, according to Google Scholar, his research has received over 900 citations, with an h-index of 14 and an i10-index of 19.

Awards Dr. Hayashi has received several recognitions, including the 2024 Outstanding Research Scientist Award from Georgia Tech's College of Computing. His work has been honored with the Best SCALE Challenge Award (CCGRID, 2023 & 2024), the Outstanding Paper Award (IEEE HPCS, 2021), and the Best Expo Exhibit Award (IBM/ACM CASCON, 2017 & 2018).

Funding, Leadership, and Mentorship Dr. Hayashi has contributed to externally funded projects as a Co-PI, Lead, or Senior Personnel, collaborating with sponsors such as BAH, IARPA, IBM, ORNL, and SNL. He has worked with numerous academic/research faculty members, researchers, engineers, and students across various projects, mentoring Ph.D., master's, and undergraduate students, as well as postdoctoral fellows and research scientists.

Technical Engagement Dr. Hayashi is active in the research community, serving on program committees for top conferences and reviewing for leading journals. To date, he has reviewed over 20 journal and 120 conference/workshop papers. Additionally, since 2023, he has been an associate and guest editor for the IEICE Transactions on Information and Systems, and has been a member of the OpenSHMEM API specification committee since 2021.

Research Interests Dr. Hayashi's research interests include:

- Parallel and Distributed Programming Models
- Automatic Parallelizing Compilers
- Just-In-Time Compilers
- Parallel and Distributed Runtime Systems
- Machine-learning for Compiler/Runtime Optimizations
- Resilience for Parallel and Distributed Systems
- GPUs
- Quantum Computing

Education

2008-2012: Ph.D., Computer Science, Waseda University, Tokyo, Japan

Thesis: *Studies on Automatic Parallelization for Heterogeneous and Homogeneous Multicore Processors*

Advisor: Prof. Hironori Kasahara

2007-2008: M.E., Computer Science, Waseda University, Tokyo, Japan

Thesis: *Study on Compiler Cooperative Heterogeneous Multicore Architecture*

Advisor: Prof. Hironori Kasahara

2003-2007: B.E., Computer Science, Waseda University, Tokyo, Japan

Thesis: *Parallel Code Generation Scheme for Hierarchical Multigrain Parallel Processing on Heterogeneous Multi-core Processor*

Advisor: Prof. Hironori Kasahara

Professional Experience

Professional

2025-present: Principal Research Scientist, Georgia Institute of Technology, Atlanta, GA, USA

- Leading externally funded research projects as co-principal investigator, key personnel, and team lead
- Serving on conference organizing/program committees, journal editorial boards, and specification committees in high-performance computing and programming models

2019-2025: Senior Research Scientist, Georgia Institute of Technology, Atlanta, GA, USA

Led and conducted research on:

- An actor-based programming model and its runtime system for large-scale irregular applications
- Enabling resiliency in asynchronous many-task (AMT) programming models
- Multi-level programming models for Graphics Processing Units (GPUs) and SIMD units
- Code generation and optimizations for GPUs
- Automatic construction of compiler and runtime heuristics using machine-learning techniques
- Programming models for quantum-classical systems

Additional responsibilities:

- Led externally funded research projects such as IARPA AGILE as co-principal investigator, key personnel, and team lead
- Served on conference organizing/program committees, journal editorial boards, and specification committees in high-performance computing and programming models

2015-2019: Research Scientist, Rice University, Houston, TX, USA

Led and conducted research on:

- LLVM-based optimizations for large-scale systems
- Code generation and optimizations for GPUs
- Automatic construction of compiler/runtime heuristics with machine learning
- Resiliency in AMT programming models

2013-2015: Postdoctoral Researcher, Rice University, Houston, TX, USA

Conducted research on compiler and runtime support for parallel languages such as Habanero-Java, focusing on high-level language constructs and parallel GPU code generation while maintaining precise exception semantics.

2012-2013: Assistant Professor, Waseda University, Tokyo, Japan

Conducted research on automatic parallelizing compilers and compiler-directed power reduction techniques in collaboration with:

- TOYOTA and Denso (automotive engine control software)
- Mitsubishi Electric (dose calculation software for heavy-ion therapy)
- Fujitsu Ltd. (smartphone applications on Android)
- Olympus Corporation (multimedia applications)

Taught freshman-level courses in computer literacy and C programming (Spring/Fall 2012).

2010-2012: Research Associate, Waseda University, Tokyo, Japan

Conducted research on automatic parallelization and power reduction techniques for embedded heterogeneous multi-core processors. Most notably, optimized a clinically-used dose calculation program in collaboration with Mitsubishi Electric, achieving over 50x speedup on IBM POWER7 platforms.

2007-2010: Research Associate, Global COE Program, Waseda University, Tokyo, Japan

Conducted research on automatic parallelization and power reduction for embedded heterogeneous multi-core processors in collaboration with Hitachi Ltd. and Renesas Electronics Corporation. This work was supported by the Global COE program "International Research and Education Center for Ambient SoC," funded by Japan's Ministry of Education, Culture, Sports, Science, and Technology (MEXT).

Teaching**Courses**

- Computer Literacy, Waseda University, Spring 2012. (English Course)
- C Programming, Waseda University, Fall 2012. (English Course)
- Science and Engineering Lab., Waseda University, Spring/Fall 2012. (Japanese Course)

Tutorials

- Fundamentals of CUDA Programming, Waseda University, Spring/Fall 2018
- Fundamentals of FPGA Programming, Waseda University, Spring 2018

Awards

- Reproducibility Challenge Selection (SC25 Student Cluster Competition) at the International Conference for High Performance Computing, Networking, Storage, and Analysis (SC25), November, 2025. (Shubhendra Pal Singhal, Souvadra Hati, Jeffrey Young, Vivek Sarkar, Akihiro Hayashi, Richard Vuduc) [LINK](#)
- Best SCALE Challenge Award, IEEE TCSC International Scalable Computing Challenge at the 24th IEEE/ACM International Symposium on Cluster, Cloud and Internet Computing (CCGRID2024), May, 2024. (Youssef Elmougy, Akihiro Hayashi, Vivek Sarkar) [LINK](#)
- Outstanding Research Scientist Award, College of Computing, Georgia Institute of Technology, 2024 [LINK](#)
- Best SCALE Challenge Award, IEEE TCSC International Scalable Computing Challenge at the 23rd IEEE/ACM International Symposium on Cluster, Cloud and Internet Computing (CCGRID2023), May, 2023. (Youssef Elmougy, Akihiro Hayashi, Vivek Sarkar) [LINK](#)
- IEEE Senior Member, 2021
- Outstanding Paper award, The 2020 International Conference on High Performance Computing & Simulation (HPCS2020), Mar 2021. (Tiago Carneiro, Nouredine Melab, Akihiro Hayashi, Vivek Sarkar) [LINK](#)

- Best Expo Exhibit, 28th Annual International Conference on Computer Science and Software Engineering (CASCON2018), November 2018 (1 best exhibit out of 72 exhibits). (Akihiro Hayashi, Gita Koblents, Max Grossman, Kazuaki Ishizaki, Alon Shalev Housfater, Jimmy Kwa, Vivek Sarkar) [LINK](#) (A PDF File will open)
- Best Expo Exhibit, 27th Annual International Conference on Computer Science and Software Engineering (CASCON2017), November 2017 (2 best exhibit out of 54 exhibits). (Akihiro Hayashi, Gita Koblents, Max Grossman, Kazuaki Ishizaki, Alon Shalev Housfater, Jimmy Kwa, Vivek Sarkar) [LINK](#) (A PDF File will open)
- Encouragement award, IPSJ Symposium on Embedded Systems, October 2013. (Dan Umeda, Yohei Kanehagi, Hiroki Mikami, Akihiro Hayashi, Mitsuhiro Tani, Hiroshi Mori, Keiji Kimura, Hironori Kasahara)
- Best feature award, COOL Chips XVI, IEEE Symposium on Low Power and High-Speed Chips, April 2013. (Yohei Kishimoto, Hiroki Mikami, Keiichi Nakano, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara,) [LINK](#)
- Encouragement award, IPSJ Symposium on Embedded Systems, October 2012. (Yohei Kishimoto, Hiroki Mikami, Keiichi Nakano, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara)
- IPSJ SIG recommended Ph.D thesis, September 2012.
- Best presentation award, 5th GCOE Symposium, September 2009.

Selected Grants

- IARPA AGILE: Flow-Optimized Reconfigurable Zones of Acceleration (FORZA)". PI: Vivek Sarkar, co-PIs: Tom Conte, Alex Daglis, Akihiro Hayashi, Hyesoon Kim, Rich Vuduc (Georgia Tech), Scott Beamer (UC Santa Cruz), Peter Kogge (U. Notre Dame), Dean Chester, Gunnar Gunnarsson, Todd Inglett, Brian Smith (Cornelis Networks), Marty Deneroff, Tim Dysart (Lucata), Dave Donofrio, John Leidel (Tactical Computing Labs). Total Award Amount: \$15,847,862 (shared among six institutions).
- ORNL STAQC: "Software Stack and Algorithm for Automating Quantum-Classical Computing". PI: Jeffrey Young, co-PIs: Akihiro Hayashi, Tom Conte, Vivek Sarkar Total Award Amount: \$358,000

Professional Committees

Conference/Workshop Chairs

- Registration Chair, Social Media Co-Chair, 52nd International Symposium on Computer Architecture (ISCA2025), June 2025.
- Local arrangement Co-chair, 25th International Workshop on Languages and Compilers for Parallel Computing (LCPC2012), September 2012.

Conference/Workshop Committees

- Program Committee Member, 31st International Workshop on High-level Parallel Programming Models and Supportive Environments (HIPS, co-located with IPDPS26), May 2026.
- Program Committee Member, 28th Workshop on Advances in Parallel and Distributed Computational Models (APDCM, co-located with IPDPS26), May 2026.
- Program Committee Member, 31st ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP), January 2026.
- Program Committee Member, 35th Annual International Conference on Computer Science and Software Engineering (CASCON), November 2025.
- Program Committee Member, 34th Annual International Conference on Computer Science and Software Engineering (CASCON), November 2024.
- Reviewer, The Vivek Sarkar Festschrift Symposium (VIVEKFEST2024, co-located with SPLASH24). October 2024.
- Program Committee Member, 33rd Annual International Conference on Computer Science and Software Engineering (CASCON), September 2023.
- Program Committee Member, 29th International European Conference on Parallel and Distributed Computing (Euro-Par), August 2023.
- Program Committee Member, 10th Annual Chapel Implementers and Users Workshop (CHI UW), June 2023.
- Program Committee Member, 32nd Annual International Conference on Computer Science and Software Engineering (CASCON), November 2022.

- Program Committee Member, 9th Annual Chapel Implementers and Users Workshop (CHIUIW), June 2022.
- External Review Committee Member, 27th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP), February 2022.
- Program Committee Member, 31st Annual International Conference on Computer Science and Software Engineering (CASCON), November 2021
- Program Committee Member, Workshop on Programming Environments for Heterogeneous Computing (PEHC, co-located with SC21), November 2021
- Program Committee Member, 8th International Workshop on Large-scale HPC Application Modernization (LHAM), November 2021 (co-located with CANDAR2021)
- Program Committee Member, 2nd International Workshop on Parallel Optimization using/for Multi- and Many-core High Performance Computing (POMCO), December 2020 (co-located with HPCS2020).
- Program Committee Member, 29th Annual International Conference on Computer Science and Software Engineering (CASCON), November 2019
- Program Committee Member, 7th International Workshop on Computer Systems and Architectures (CSA), November 2019.
- Program Committee Member, 6th ACM SIGPLAN International Workshop on AI-Inspired and Empirical Methods for Software Engineering on Parallel Computing Systems (AI-SEPS2019, co-located with SPLASH2018).
- Program Committee Member, 32nd International Workshop on Languages and Compilers for Parallel Computing (LCPC), October 2019.
- Program Committee Member, 33rd IEEE International Parallel & Distributed Processing Symposium (IPDPS), May 2019.
- Program Committee Member, 6th International Workshop on Legacy-scale HPC Application Modernization (LHAM2018, co-located with CANDAR2018).
- Program Committee Member, 5th ACM SIGPLAN International Workshop on AI-Inspired and Empirical Methods for Software Engineering on Parallel Computing Systems (AI-SEPS2018, co-located with SPLASH2018).
- Program Committee Member, 28th Annual International Conference on Computer Science and Software Engineering (CASCON2018).
- External Review Committee Member, 23rd International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS2018).
- Program Committee Member, 5th International Workshop on Legacy HPC Application Migration (LHAM2017, co-located with CANDAR2017).
- Program Committee Member, 4th ACM SIGPLAN International Workshop on Software Engineering for Parallel Systems (SEPS2017, co-located with SPLASH2017).
- Program Committee Member, 22nd ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP2017).
- Program Committee Member, 22nd IEEE International Conference on Parallel and Distributed Systems (ICPADS2016).
- Program Committee Member, 3rd International Workshop on Software Engineering for Parallel Systems (SEPS2016, co-located with SPLASH2016).
- Technical Program Committee Member, 29th IEEE International Parallel & Distributed Processing Symposium (IPDPS2015).
- Program Committee Member, IPSJ Symposium on Advanced Computing Systems and Infrastructures (SAC-SIS2013).

Journal Reviewers

- ACM
 - Computing Surveys (CSUR) (2025)
 - Transactions on Mathematical Software (TOMS) (2025)
 - Transactions on Architecture and Code Optimization (TACO) (2025, 2022, 2021)
 - Transactions on Programming Languages and Systems (TOPLAS) (2018)
 - Transactions on Embedded Computing Systems (TECS)(2015)
- IEEE
 - Transactions on Parallel and Distributed Systems (TPDS)(2025, 2015)
 - Transactions on Mobile Computing (TMC) (2025)
 - Micro (2022)
- Wiley Concurrency and Computation: Practice and Experience (2024)

- PLOS ONE (2024, 2023)
- Journal of Cybersecurity and Privacy (JCP)(2023)
- Arabian Journal for Science and Engineering (2017)
- Journal of Parallel and Distributed Computing (JDPC) (2017)
- IPSJ (Information Processing Society of Japan) Journals (2024, 2015, 2014)
- IEICE (The Institute of Electronics, Information and Communication Engineers) Transactions on Information and Systems (2020, 2013, 2012)

Journal Editors

- Associate Editor, IEICE Transactions on Information and Systems (2023-)
- Guest Associate Editor, IEICE (The Institute of Electronics, Information and Communication Engineers) Special Section on Low-Power and High-Speed Chips (2022-)

External Reviewers

- The IEEE Cluster Conference(IEEE Cluster 2017)
- International Conference on Network and Parallel Computing (NPC2017, NPC2016)
- International Conference on Parallel Processing (ICPP2016)
- International Conference on Parallel Architectures and Compilation Techniques (PACT2015)
- International Conference for High Performance Computing, Networking, Storage and Analysis (SC13)
- International Conference on Supercomputing (ICS2018, ICS2013)
- International Conference on Parallel and Distributed Systems (ICPADS2013)
- International Conference on Computer Design (ICCD2014, ICCD2013, ICCD2012)
- International Workshop on Languages and Compilers for Parallel Computing (LCPC2018, LCPC2015, LCPC2014, LCPC2013)

Specification Committees

- OpenSHMEM Application Programming Interface (2022-)

Publications

Ph.D Dissertation

- **Studies on Automatic Parallelization for Heterogeneous and Homogeneous Multicore Processors.** Akihiro Hayashi. Waseda University. February 2012.

Refereed Papers

Journal Publications

1. **A Fine-grained Asynchronous Bulk Synchronous parallelism model for PGAS applications.** Sri Raj Paul, Akihiro Hayashi, Kun Chen, Youssef Elmougy, Vivek Sarkar. Journal of Computational Science, April 2023. DOI
2. **Qulacs: a fast and versatile quantum circuit simulator for research purpose.** Yasunari Suzuki, Yoshiaki Kawase, Yuya Masumura, Yuria Hiraga, Masahiro Nakadai, Jiabao Chen, Ken M. Nakanishi, Kosuke Mitarai, Ryosuke Imai, Shiro Tamiya, Takahiro Yamamoto, Tennin Yan, Toru Kawakubo, Yuya O. Nakagawa, Yohei Ibe, Youyuan Zhang, Hirotsugu Yamashita, Hikaru Yoshimura, Akihiro Hayashi, Keisuke Fujii. Quantum Journal (Quantum 5, 559). DOI
3. **Compiler-Support for Critical Data Persistence in NVM.** Reem Elkhoully, Mohammad Alshboul, Akihiro Hayashi, Yan Solihin, Keiji Kimura. ACM Transactions on Architecture and Code Optimization (TACO). DOI

4. **Performance Evaluation of OpenMP's Target Construct on GPUs.** Akihiro Hayashi, Jun Shirako, Ettore Tiotto, Robert Ho, Vivek Sarkar. International Journal of High Performance Computing and Networking (IJH-PCN), Vol. 13, No. 1, 2019. DOI
5. **Automatic Parallelization of Designed Engine Control C Codes by MATLAB/Simulink.** Dan Umeda, Yohei Kanehagi, Hiroki Mikami, Akihiro Hayashi, Mitsuhiro Tani, Hiroshi Mori, Keiji Kimura, Kasahara Hironori, IPSJ Journal, August, 2014. LINK (in Japanese)
6. **Parallelizing Compiler Framework and API for Heterogeneous Multicores.** Akihiro Hayashi, Yasutaka Wada, Takeshi Watanabe, Takeshi Sekiguchi, Masayoshi Mase, Jun Shirako, Keiji Kimura and Hironori Kasahara, IPSJ Transactions on Advanced Computing Systems (ACS), Vol.5, No.1, pp.68-79, November. 2011. LINK (in Japanese)
7. **A Parallelizing Compiler Cooperative Heterogeneous Multicore Processor Architecture.** Yasutaka Wada, Akihiro Hayashi, Takeshi Masuura, Jun Shirako, Hirofumi Nakano, Hiroaki Shikano, Keiji Kimura, and Hironori Kasahara, Transactions on High-Performance Embedded Architectures and Compilers IV (HiPEAC IV), Lecture Note in Computer Science, Springer, Vol. 6760, pp. 215-233, November 2011. DOI
8. **Parallelization of MP3 Encoder using Static Scheduling on a Heterogeneous Multicore.** Yasutaka Wada, Akihiro Hayashi, Takeshi Masuura, Jun Shirako, Hirofumi Nakano, Hiroaki Shikano, Keiji Kimura, Hironori Kasahara, Transactions of IPSJ on Computing Systems, Vol. 49 (ACS), 2008. LINK (in Japanese)

Conference/Workshop Publications

1. **Asynchronous Distributed-Memory Parallel Algorithm for k-mer Counting.** Souvadra Hati, Akihiro Hayashi, Richard Vuduc. 39th IEEE International Parallel & Distributed Processing Symposium (IPDPS25). June 2025. DOI
2. **Enhancing Productivity and Performance of HCLib-Actor with Efficient Task Termination.** Youssef Elmougy, Nirjhar Deb, Akihiro Hayashi, Vivek Sarkar. 27th Workshop on Advances in Parallel and Distributed Computational Models (APDCM, co-located with IPDPS25). DOI
3. **Divide, Conquer, and Match: A Distributed and Asynchronous Approach for Subgraph Isomorphism.** Youssef Elmougy, Akihiro Hayashi, Vivek Sarkar. Workshop on Graphs, Architectures, Programming, and Learning (GrAPL, co-located with IPDPS25). DOI
4. **ActorISx: Exploiting Asynchrony for Scalable High-Performance Integer Sort.** Youssef Elmougy, Shubhendra Pal Singhal, Akihiro Hayashi, Vivek Sarkar. IEEE TCSC International Scalable Computing Challenge (SCALE 2025, co-located with CCGRID25). DOI
5. **Asynchronous Distributed-Memory Parallel Algorithms for Influence Maximization.** Shubhendra Pal Singhal, Souvadra Hati, Jeffrey Young, Vivek Sarkar, Akihiro Hayashi, Richard Vuduc. International Conference for High Performance Computing, Networking, Storage, and Analysis (SC24). November 2024. DOI
6. **ActorProf: A Framework for Profiling and Visualizing Fine-grained Asynchronous Bulk Synchronous Parallel Execution.** Jiawei Yang, Shubhendra Pal Singhal, Jun Shirako, Akihiro Hayashi, Vivek Sarkar. Workshop on Programming and Performance Visualization Tools (ProTools2024, co-located with SC24). DOI
7. **Enabling User-level Asynchronous Tasking in the FA-BSP Model - Case Study: Distributed Triangle Counting.** Akihiro Hayashi, Shubhendra Pal Singhal, Youssef Elmougy, Jiawei Yang. The Vivek Sarkar Festschrift Symposium (VIVEKFEST2024, co-located with SPLASH24). October 2024. DOI
8. **Intrepydd: Toward Performance, Productivity, and Portability for Massive Heterogeneous Parallelism.** Jun Shirako, Tong Zhou, Akihiro Hayashi. The Vivek Sarkar Festschrift Symposium (VIVEKFEST2024, co-located with SPLASH24). October 2024. DOI
9. **On the Cloud We Can't Wait: Asynchronous Actors Perform Even Better on the Cloud.** Aniruddha Mysore, Youssef Elmougy, Akihiro Hayashi. The Vivek Sarkar Festschrift Symposium (VIVEKFEST2024, co-located with SPLASH24). October 2024. DOI
10. **Asynchronous Distributed Actor-based Approach to Jaccard Similarity for Genome Comparisons.** Youssef Elmougy, Akihiro Hayashi, Vivek Sarkar. International Conference on High Performance Computing (ISC High Performance). May 2024. DOI

11. **A Distributed, Asynchronous Algorithm for Large-Scale Internet Network Topology Analysis.** Youssef Elmougy, Akihiro Hayashi, Vivek Sarkar. IEEE TCSC International Scalable Computing Challenge (SCALE 2024, co-located with CCGRID24), May 2024. Recipient of Best SCALE Challenge Award. DOI
12. **Towards Safe HPC: Productivity and Performance via Rust interfaces for a Distributed C++ Actors library.** John T. Parrish, Nicole Wren, Tsz Hang Kiang, Akihiro Hayashi, Jeffrey Young, Vivek Sarkar. 20th International Conference on Managed Programming Languages & Runtimes (MPLR, co-located with SPLASH24). October 2023. DOI
13. **Enabling Multi-threading in Heterogeneous Quantum-Classical Programming Models.** Akihiro Hayashi, Austin Adams, Jeffrey Young, Alexander McCaskey, Eugene Dumitrescu, Vivek Sarkar, Thomas M. Conte, IPDPS Workshop on Quantum Computing Algorithms, Systems, and Applications (Q-CASA, co-located with IPDPS23). May 2023. DOI
14. **Highly Scalable Large-Scale Asynchronous Graph Processing using Actors.** Youssef Elmougy, Akihiro Hayashi, Vivek Sarkar. IEEE TCSC International Scalable Computing Challenge (SCALE 2023, co-located with CCGRID23), May 2023. Recipient of Best SCALE Challenge Award. DOI
15. **Automatic Parallelization of Python programs for Distributed Heterogeneous Computing.** Jun Shirako, Akihiro Hayashi, Sri Raj Paul, Alexey Tumanov and Vivek Sarkar. 28th International European Conference on Parallel and Distributed Computing (Euro-Par2022), August 2022. DOI
16. **A Multi-Level Platform-Independent GPU API for High-Level Programming Models.** Akihiro Hayashi, Sri Raj Paul and Vivek Sarkar, HPC on Heterogeneous Hardware Workshop (H3), June 2022. (co-located with ISC22) DOI
17. **A Productive and Scalable Actor-based Programming System for PGAS Applications.** Sri Raj Paul, Akihiro Hayashi, Kun Chen, and Vivek Sarkar. 22th International Conference on Computational Science (ICCS2022), June 2022. DOI
18. **Towards Chapel-based Exascale Tree Search Algorithms: dealing with multiple GPU accelerators.** Tiago Carneiro, Nouredine Melab, Akihiro Hayashi, Vivek Sarkar. 18th International Conference on High Performance Computing & Simulation (HPCS2020), March 2021. Recipient of Outstanding Paper Award. [LINK]
19. **Integrating Inter-Node Communication with a Resilient Asynchronous Many-Task Runtime System.** Sri Raj Paul, Akihiro Hayashi, Matthew Whitlock, Seonmyeong Back, Keita Teranishi, Jackson Mayo, Max Grossman, Vivek Sarkar, International IEEE workshop on Exascale MPI (ExaMPI), November 2020. (co-located with SC20) DOI
20. **Exploring a multi-resolution GPU programming model for Chapel.** Akihiro Hayashi, Sri Raj Paul, Vivek Sarkar, 7th Annual Chapel Implementers and Users Workshop (CHI UW), May 2020. (co-located with IPDPS2020) DOI
21. **Enabling Resilience in Asynchronous Many-Task Programming Models.** Sri Raj Paul, Akihiro Hayashi, Nicole Slattengren, Hemanth Kolla, Matthew Whitlock, Seonmyeong Bak, Keita Teranishi, Jackson Mayo, Vivek Sarkar. 25th International European Conference on Parallel and Distributed Computing (Euro-Par2019), August 2019. DOI
22. **GPUerator: bridging the gap between Chapel and native languages.** Akihiro Hayashi, Sri Raj Paul, Vivek Sarkar, The ACM SIGPLAN 6th Annual Chapel Implementers and Users Workshop (CHI UW), June 2019. (co-located with PLDI2019/ACM FCRC2019) DOI
23. **A Unified Runtime for PGAS and Event-Driven Programming.** Sri Raj Paul, Kun Chen, Akihiro Hayashi, Max Grossman, Vivek Sarkar, International IEEE Workshop on Extreme Scale Programming Models and Middleware (ESPM2), November 2018. (co-located with SC18) DOI
24. **Exploration of Supervised Machine Learning Techniques for Runtime Selection of CPU vs. GPU Execution in Java Programs.** Gloria Kim, Akihiro Hayashi, Vivek Sarkar. Fourth Workshop on Accelerator Programming Using Directives (WACCPD), November 2017. (co-located with SC17) DOI
25. **Chapel-on-X: Exploring Tasking Runtimes for PGAS Languages.** Akihiro Hayashi, Sri Raj Paul, Max Grossman, Jun Shirako, Vivek Sarkar. Third IEEE Workshop on Extreme Scale Programming Models and Middleware (ESPM2), November 2017. (co-located with SC17) DOI

26. **Optimized Two-level Parallelization for GPU Accelerators using the Polyhedral Model.** Jun Shirako, Akihiro Hayashi, Vivek Sarkar. 26th International Conference on Compiler Construction (CC2017), February 2017. DOI
27. **Exploring Compiler Optimization Opportunities for the OpenMP 4.x Accelerator Model on a POWER8+GPU Platform.** Akihiro Hayashi, Jun Shirako, Ettore Tiotto, Robert Ho, Vivek Sarkar. Third Workshop on Accelerator Programming Using Directives (WACCPD), November 2016. (co-located with SC16) DOI
28. **LLVM-based Communication Optimizations for PGAS Programs.** Akihiro Hayashi, Jisheng Zhao, Michael Ferguson, Vivek Sarkar. 2nd Workshop on the LLVM Compiler Infrastructure in HPC (LLVM), November, 2015. (co-located with SC15) DOI
29. **Compiling and Optimizing Java 8 Programs for GPU Execution.** Kazuaki Ishizaki, Akihiro Hayashi, Gita Koblents, Vivek Sarkar. 24th International Conference on Parallel Architectures and Compilation Techniques (PACT2015), October 2015. DOI
30. **Machine-Learning-based Performance Heuristics for Runtime CPU/GPU Selection.** Akihiro Hayashi, Kazuaki Ishizaki, Gita Koblents, Vivek Sarkar. 12th International Conference on the Principles and Practice of Programming in Java (PPPJ2015), September 2015. DOI
31. **Accelerating Habanero-Java Program with OpenCL Generation.** Akihiro Hayashi, Max Grossman, Jisheng Zhao, Jun Shirako, Vivek Sarkar. 10th International Conference on the Principles and Practice of Programming in Java (PPPJ2013), September 2013. DOI
32. **Speculative Execution of Parallel Programs with Precise Exception Semantics on GPUs.** Akihiro Hayashi, Max Grossman, Jisheng Zhao, Jun Shirako, Vivek Sarkar. 26th International Workshop on Languages and Compilers for Parallel Computing (LCPC2013), September 2013. (co-located with CnC) DOI
33. **Reconciling Application Power Control and Operating Systems for Optimal Power and Performance.** Dominic Hillenbrand, Yuuki Furuyama, Akihiro Hayashi, Mikami Hiroki, Keiji Kimura, Hironori Kasahara. 8th International Workshop on Reconfigurable Communication-centric System-on-Chip (ReCoSoC2013), Germany, 2013. DOI
34. **Automatic Parallelization, Performance Predictability and Power Control for Mobile-Applications.** Dominic Hillenbrand, Akihiro Hayashi, Hideo Yamamoto, Keiji Kimura, Hironori Kasahara. 16th IEEE Symposium on Low-Power and High-Speed Chips (CoolChips XVI), April 2013. DOI
35. **Parallelization of Automotive Engine Control Software On Embedded Multi-core Processor Using OSCAR Compiler.** Yohei Kanehagi, Dan Umeda, Akihiro Hayashi, Keiji Kimura and Hironori Kasahara, 16th IEEE Symposium on Low-Power and High-Speed Chips (CoolChips XVI), April 2013. DOI
36. **Automatic Design Exploration Framework for Multicores with Reconfigurable Accelerators.** Cecilia Gonzalez-Alvarez, Haruku Ishikawa, Akihiro Hayashi, Daniel Jimenez-Gonzalez, Carlos Alvarez, Keiji Kimura and Hironori Kasahara. 7th HiPEAC Workshop on Reconfigurable Computing (WRC2013), January, 2013.
37. **Parallel processing of multimedia applications on TILEPro64 using OSCAR API for embedded multi-core.** Yohei Kishimoto, Hiroki Mikami, Keiichi Nakano, Akihiro Hayashi, Keiji Kimura and Hironori Kasahara, IPSJ Symposium on Embedded System (ESS2012), October 2012. (in Japanese)
38. **Automatic Parallelization of Dose Calculation Engine for A Particle Therapy.** Akihiro Hayashi, Takuji Matsumoto, Hiroki Mikami, Keiji Kimura, Keiji Yamamoto, Hironori Saki, Yasuyuki Takatani, Hironori Kasahara, IPSJ Symposium on High Performance Computing and Computer Science (HPCS2012), January 2012. (in Japanese)
39. **Evaluation of Power Consumption at Execution of Multiple Automatically Parallelized and Power Controlled Media Applications on the RP2 Low-power Multicore.** Hiroki Mikami, Shumpei Kitaki, Masayoshi Mase, Akihiro Hayashi, Mamoru Shimaoka, Keiji Kimura, Masato Eda, and Hironori Kasahara, 24th International Workshop on Languages and Compilers for Parallel Computing (LCPC2011), September 2011. DOI
40. **Parallelizing Compiler Framework and API for Power Reduction and Software Productivity of Real-time Heterogeneous Multicores.** Akihiro Hayashi, Yasutaka Wada, Takeshi Watanabe, Takeshi Sekiguchi, Masayoshi Mase, Jun Shirako, Keiji Kimura and Hironori Kasahara, 23rd International Workshop on Languages and Compilers for Parallel Computing (LCPC2010), October 2010. DOI

41. **A 45nm Heterogeneous Multi-core SoC Supporting an over 32-bits Physical Address Space for Digital Appliance.** Takumi Nito, Yoichi Yuyama, Masayuki Ito, Yoshikazu Kiyoshige, Yusuke Nitta, Osamu Nishii, Atsushi Hasegawa, Makoto Ishikawa, Tetsuya Yamada, Junichi Miyakoshi, Koichi Terada, Tooru Nojiri, Masashi Takada, Makoto Satoh, Hiroyuki Mizuno, Kunio Uchiyama, Yasutaka Wada, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara, Hideo Maejima, 13th IEEE Symposium on Low-power and High-Speed Chips (COOL Chips XIII), April 2010.
42. **Parallelizing Compiler Cooperative Heterogeneous Multicore.** Yasutaka Wada, Akihiro Hayashi, Takeshi Masuura, Jun Shirako, Hirofumi Nakano, Hiroaki Shikano, Keiji Kimura, Hironori Kasahara, Workshop on Software and Hardware Challenges of Manycore Platforms (SHCMP2008), June 2008. (co-located ISCA2008)
43. **Software-Cooperative Power-Efficient Heterogeneous Multi-Core for Media Processing.** Hiroaki Shikano, Masaki Ito, Kunio Uchiyama, Toshihiko Odaka, Akihiro Hayashi, Takeshi Masuura, Masayoshi Mase, Jun Shirako, Yasutaka Wada, Keiji Kimura, Hironori Kasahara, 13th Asia and South Pacific Design Automation Conference (ASP-DAC2008), January 2008. DOI

Refereed Posters

1. **Bottleneck Scenarios in use of the Conveyors Message Aggregation Library.** Shubhendra Pal Singhal, Akihiro Hayashi, Vivek Sarkar. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS24). May 2024. DOI
2. **Accelerating Actor-Based Distributed Triangle Counting.** Aniruddha Mysore, Kaushik Ravichandran, Youssef Elmougy, Akihiro Hayashi, Vivek Sarkar**. International Conference for High Performance Computing, Networking, Storage, and Analysis (SC23). November 2023. LINK
3. **Extending OMR with Explicit and Automatic Runtime SIMD/GPU Parallelization.** Akihiro Hayashi, Tong Zhou, Gita Koblenz, Jimmy Kwa, Kazuaki Ishizaki, Vivek Sarkar. 30th Annual International Conference on Computer Science and Software Engineering (CASCON), November 2020
4. **Kokkos-HClib: enabling high-performance and resiliency for HPC systems.** Akihiro Hayashi, Sri Raj Paul, Matthew Whitlock, Nicolas Morales, Jeff Miles, Keita Teranishi, Vivek Sarkar. 2020 DOE Performance, Portability, and Productivity in HPC Forum (P3HPC 2020), September 2020
5. **Runtime Automatic Parallelization of JVM and OMR Applications.** Akihiro Hayashi, Gita Koblenz, Kazuaki Ishizaki, Jimmy Kwa, Vivek Sarkar. 29th Annual International Conference on Computer Science and Software Engineering (CASCON), November 2019
6. **Runtime Automatic Parallelization of JVM Applications.** Akihiro Hayashi, Gita Koblenz, Max Grossman, Kazuaki Ishizaki, Alon Housfater, Jimmy Kwa, Vivek Sarkar. 28th Annual International Conference on Computer Science and Software Engineering (CASCON), November 2018 (Won the best exhibit out of 72 exhibits)
7. **Runtime Automatic Parallelization of JVM Applications.** Akihiro Hayashi, Gita Koblenz, Max Grossman, Kazuaki Ishizaki, Alon Housfater, Jimmy Kwa, Vivek Sarkar. 27th Annual International Conference on Computer Science and Software Engineering (CASCON), November 2017 (Won the best exhibit out of 68 exhibits)
8. **Tackling GPU Programmability and Profitability Using IBM JIT Code Generation and Performance Prediction.** Akihiro Hayashi, Gita Koblenz, Max Grossman, Kazuaki Ishizaki, Alon Housfater, Jimmy Kwa, Vivek Sarkar. 26th Annual International Conference on Computer Science and Software Engineering (CASCON), November 2016
9. **How Java runtime can execute practical Java programs on GPU.** Kazuaki Ishizaki, Gita Koblenz, Akihiro Hayashi, Vivek Sarkar, Hiroshi Inoue. Poster Session, IPSJ Symposium on High Performance Computing and Computer Science (HPCS2015), May 2015. (in Japanese)
10. **Parallel Processing of Multimedia Applications on TILEPro64.** Yohei Kishimoto, Hiroki Mikami, Keiichi Nakano, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara. 16th IEEE Symposium on Low Power and High-Speed Chips (COOL Chips XVI), April 2013.
11. **Opportunities and Challenges of Application-Power Control in the Age of Dark Silicon.** Dominic Hillenbrand, Yuuki Furuyama, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara. 8th International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC2013), January 2013.

12. **OSCAR Parallelizing Compiler Cooperative Heterogeneous Multi-core Architecture.** Akihiro Hayashi, Yasutaka Wada, Hiroaki Shikano, Teruo Kamiyama, Takeshi Watanabe, Takeshi Sekiguchi, Masayoshi Mase, 18th International Conference on Parallel Architectures and Compilation Techniques (PACT2009), September 2009.

Patents (include applications)

1. **Parallelism extraction method and method for making program.** Hironori Kasahara, Keiji Kimura, Akihiro Hayashi, Hiroki Mikami, Yohei Kanehagi, Dan Umeda, Mitsuo Sawada. LINK
2. **Parallelizing compile method, parallelizing compiler, parallelizing compile apparatus, and onboard apparatus.** Hiroshi Mori, Mitsuhiro Tani, Hironori Kasahara, Keiji Kimura, Dan Umeda, Akihiro Hayashi, Hiroki Mikami, Yohei Kanehagi, LINK
3. **Runtime gpu/cpu selection.** Gita Koblents, Alon Shalev Housfater, Kazuaki Ishizaki, Akihiro Hayashi. LINK

Invited Talks

1. **A Fine-grained Asynchronous Bulk Synchronous Parallelism Model for Large-scale Applications** Advanced Computer Science and Engineering Seminar, Waseda University, 2024.
2. **How to design human actions by digital technology?** The National Convention of IPSJ, March 2013. (in Japanese)

Refereed Presentations/Papers without Precedings

1. **Fine-grained-Asynchronous Bulk-Synchronous Processing for Graph Analytics.** Vivek Sarkar and Akihiro Hayashi. 2024 SIAM Conference on Parallel Processing for Scientific Computing (SIAM-PP24), March 2024.
2. **Enabling CHIP-SPV in Chapel GPUAPI module.** Jisheng Zhao, Akihiro Hayashi, Brice Videau, Vivek Sarkar. The 10th Annual Chapel Implementers and Users Workshop (CHI UW 2023), June 2023.
3. **Accelerating CHAMPS on GPUs.** Akihiro Hayashi, Sri Raj Paul and Vivek Sarkar. The 9th Annual Chapel Implementers and Users Workshop (CHI UW 2022), June 2022.
4. **A Cooperative Compiler and Runtime Checkpoint/Restart Approach for Kokkos.** Akihiro Hayashi, Matthew Whitlock, Sri Raj Paul, Nicolas Morales, Keita Teranishi, Vivek Sarkar, 2022 SIAM Conference on Parallel Processing for Scientific Computing (SIAM-PP22), February 2022.
5. **GPUAPI: Multi-level Chapel Runtime API for GPUs.** Akihiro Hayashi, Sri Raj Paul, Vivek Sarkar, 8th Annual Chapel Implementers and Users Workshop (CHI UW), June 2021.
6. **Composing Asynchrony, Communication and Resilience.** Sri Raj Paul, Akihiro Hayashi, Nicole Slattengren, Hemanth Kolla, Seonmyeong Bak, Matthew Whitlock, Jackson Mayo, Keita Teranishi, Vivek Sarkar and Max Grossman. 2020 SIAM Conference on Parallel Processing for Scientific Computing (SIAM-PP20)
7. **Scalable Efficient Fault Tolerance in Asynchronous Many Task (AMT) Programming Models.** Keita Teranishi, Hemanth Kolla, Nicole Slattengren, Mayo Jackson, Sri Raj Paul, Akihiro Hayashi, Vivek Sarkar, Seonmyeong Bak. 2019 SIAM Conference on Parallel Processing for Scientific Computing (SIAM-PP19)
8. **Fault Tolerance in AMT Programming Models & Runtimes.** Hemanth Kolla, Keita Teranishi, Nicole Slattengren, Matthew Whitlock, Jackson Mayo, Sri Raj Paul, Akihiro Hayashi, Vivek Sarkar. 2018 ACM Conference on Platform for Advanced Scientific Computing (PASC2018)
9. **Resilience With Asynchronous Many Task (AMT) Programming Models.** Sanjay Chatterjee, Keita Teranishi, Vivek Sarkar, Akihiro Hayashi. 2018 SIAM Conference on Parallel Processing for Scientific Computing (SIAM-PP18)
10. **Machine-learning-based Performance Heuristics for Runtime CPU/GPU Selection in Java.** 10th Workshop on Challenges for Parallel Computing, November 2015. (co- located with CASCON2015)

11. **LLVM-based Communication Optimizations for Chapel.** Chapel Lightning Talks Birds-of-a-Feather at International Conference for High Performance Computing, Networking, Storage and Analysis (SC14), November 2014.
12. **LLVM Optimizations for PGAS Programs -Case Study: LLVM Wide Optimization in Chapel-**. Akihiro Hayashi, Rishi Surendran, Jisheng Zhao, Michael Ferguson, Vivek Sarkar. 1st Chapel Implementers and Users Workshop (CHI UW2014), May 2014. (co-located with IPDPS)
13. **Automatic Parallelization of Hand Written Automotive Engine Control Codes Using OSCAR Compiler.** Dan Umeda, Yohei Kanehagi, Hiroki Mikami, Akihiro Hayashi, Keiji Kimura and Hironori Kasahara. 17th Workshop on Compilers for Parallel Computing (CPC2013), July 2013.
14. **OSCAR API v2.1: Extensions for an Advanced Accelerator Control Scheme to a Low-Power Multicore API.** Keiji Kimura, Cecilia Gonzales-Alvarez, Akihiro Hayashi, Hiroki Mikami, Mamoru Shimaoka, Jun Shirako, Hironori Kasahara, 17th Workshop on Compilers for Parallel Computing (CPC2013), July 2013
15. **OSCAR Parallelizing Compiler and API for Real-time Low Power Heterogeneous Multicores.** Akihiro Hayashi, Mamoru Shimaoka, Hiroki Mikami, Masayoshi Mase, Yasutaka Wada, Jun Shirako, Keiji Kimura, and Hironori Kasahara, 16th Workshop on Compilers for Parallel Computing (CPC2012), January 2012.
16. **Performance of OSCAR Multigrain Parallelizing Compiler on Multicore Processors.** Hiroki Mikami, Jun Shirako, Masayoshi Mase, Takamichi Miyamoto, Hirofumi Nakano, Fumiyo Takano, Akihiro Hayashi, Yasutaka Wada, Keiji Kimura, Hironori Kasahara, 14th Workshop on Compilers for Parallel Computing(CPC2009), January 2009.

Technical Reports

1. **Resilient Asynchronous Many Task Programming Model.** Keita Teranishi, Hemanth Kolla, Nicole Lemaster Slattengren, Matthew Whitlock, Jackson Mayo, Robert L. Clay, Sri Raj Paul, Akihiro Hayashi, Vivek Sarkar, August, 2018. DOI
2. **Performance Evaluation of Hierarchical Barrier Hardware with OSCAR API Analyzer.** Akihiro Kawashima, Yohei Kanehagi, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ. Vol.2013-ARC-206-16 (SWoPP2013), July 2013. (in Japanese)
3. **An Investigation of Parallelization and Evaluation on Commercial Multi-core Smart Device.** Hideo Yamamoto, Takashi Goto, Tomohiro Hirano, Kouhei Muto, Hiroki Mikami, Dominic Hillenbrand, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol. 2013-OS-124, February 2013. (in Japanese)
4. **Parallelization of Automobile Engine Control Software on Multicore Processor.** Yohei Kanehagi, Dan Umeda, Hiroki Mikami, Akihiro Hayashi, Mitsuo Sawada, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2013-ARC195-2, January 2013. (in Japanese)
5. **Automatic parallelization of the GMS Earthquake simulator with OSCAR Compiler.** Mamoru Shimaoka, Hiroki Mikami, Akihiro Hayashi, Yasutaka Wada, Keiji Kimura, Hidekazu Morita, Kunio Uchiyama, Hironori Kasahara. Technical Report of IPSJ, Vol.2012-ARC194HPC137-26 (HOKKE2012), December 2012.
6. **Automatic parallelization with OSCAR API Analyzer: a cross-platform performance evaluation.** Cecilia Gonzalez-Alvarez, Yohei Kanehagi, Kosei Takemoto, Yohei Kishimoto, Kohei Muto, Hiroki Mikami, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2012-ARC194HPC137-10 (HOKKE2012), December 2012.
7. **Opportunities and Challenges of Application-Power Control in the Age of Dark Silicon.** Dominic Hillenbrand, Yuuki Furuyama, Akihiro Hayashi, Hiroki Mikami, Keiji Kimura, Hironori Kasahara, Technical Report of IPSJ, Vol.2012- ARC194HPC137-11(HOKKE2012), December 2012.
8. **Realization of 1 Watt Web Service with RP-X Low-power Multicore Processor.** Yuuki Furuyama, Mamoru Shimaoka, Hiroki Mikami, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2012-ARC-201-24 (SWoPP2012), August 2012. (in Japanese)
9. **Parallelization of Basic Engine Control Software Model on Multicore Processor.** Dan Umeda, Yohei Kanehagi, Hiroki Mikami, Akihiro Hayashi, Mituhiro Tani, Yuji Mori, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2012-ARC-201-22 (SWoPP2012), August 2012. (in Japanese)

10. **Automatic Parallelization of Dose Calculation Engine for A Particle Therapy on SMP Servers.** Akihiro Hayashi, Takuji Matsumoto, Hiroki Mikami, Keiji Kimura, Keiji Yamamoto, Hironori Saki, Yasuyuki Takatani, Hironori Kasahara. Technical Report of IPSJ, Vol.2011-ARC189HPC132-2 (HOKKE2011), November 2011. (in Japanese)
11. **Hiding I/O overheads with Parallelizing Compiler for Media Applications.** Akihiro Hayashi, Takeshi Sekiguchi, Masayoshi Mase, Yasutaka Wada, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2011-ARC-195OS117-14, April 2011. (in Japanese)
12. **Evaluation of Parallelizable C Programs by the OSCAR API Standard Translator.** Takuya Sato, Hiroki Mikami, Akihiro Hayashi, Masayoshi Mase, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2010-ARC-191-2, October 2010. (in Japanese)
13. **A Compiler Framework for Heterogeneous Multicores for Consumer Electronics.** Akihiro Hayashi, Yasutaka Wada, Takeshi Watanabe, Takeshi Sekiguchi, Masayoshi Mase, Keiji Kimura, Masayuki Ito, Jun Hasegawa, Makoto Sato, Toru Nojiri, Kunio Uchiyama, Hironori Kasahara. Technical Report of IPSJ, Vol.2010-ARC-190-7 (SWoPP2010), August 2010. (in Japanese)
14. **Performance of Power Reduction Scheme by a Compiler on Heterogeneous Multicore for Consumer Electronics RP-X.** Yasutaka Wada, Akihiro Hayashi, Takeshi Watanabe, Takeshi Sekiguchi, Masayoshi Mase, Jun Shirako, Keiji Kimura, Masayuki Ito, Jun Hasegawa, Makoto Sato, Toru Nojiri, Kunio Uchiyama, Hironori Kasahara, Technical Report of IPSJ, Vol.2010-ARC-190-8 (SWoPP2010), August 2010. (in Japanese)
15. **Performance Evaluation of Parallelizing Compiler Cooperated Heterogeneous Multicore Architecture Using Media Applications.** Teruo Kamiyama, Yasutaka Wada, Akihiro Hayashi, Masayoshi Mase, Hirofumi Nakano, Takeshi Watanabe, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2009-ARC-173, Jan. 2009. (in Japanese)
16. **A Hierarchical Coarse Grain Task Static Scheduling Scheme on a Heterogeneous Multicore.** Yasutaka Wada, Akihiro Hayashi, Taketo Iyoku, Jun Shirako, Hirofumi Nakano, Hiroaki Shikano, Keiji Kimura, Hironori Kasahara, Technical Report of IPSJ, Vol. 2007-ARC-174-17 (SWoPP2007), August 2007. (in Japanese)
17. **Compiler Control Power Saving for Heterogeneous Multicore Processor.** Akihiro Hayashi, Taketo Iyoku, Ryo Nakagawa, Shigeru Matsumoto, Kaito Yamada, Naoto Oshiyama, Jun Shirako, Yasutaka Wada, Hirofumi Nakano, Hiroaki Shikano, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2007-ARC-174-18 (SWoPP2007), August 2007. (in Japanese)