Marco Spaziani Brunella

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Education

University of Rome Tor Vergata — *Rome, IT*
PhD in Electronics Engineering, First Place at the admissions — *Present*

University of Rome Tor Vergata — *Rome, IT*
Master of Science in Electronics Engineering, 110/110 — *October 2019*

University of Rome Tor Vergata — *Rome, IT*
Bachelor of Science in Electronics Engineering, 106/110 — *July 2017*

J. T. Schwartz International School for Scientific Research — *Lipari, IT*
Lipari PhD School on Network and Computer Sciences, A+ ECTS — *July 2017*

Skills

Languages	C, VHDL, (System)Verilog, Python, Visual C#, SPICE, Java, JavaScript, TypeScript, HTML
Development Fileds	FPGAs, ASICs, Linux Kernel, Embedded Systems, CPU Architectures, RISC-V
Frameworks and EDAs	Xilinx Vivado, Intel Quartus, Cadence, Synopsis, Angular, Django

Experience

GenomeUp — *Rome, IT*
Front End Developer — *April 2020 - Present*
- Developed an Anhular + Angular Material frontend foa a microbiome database

University of Rome Tor Vergata — *Rome, IT*
Lecturer — *March 2020 - Present*
- ICT Infrastructure Security Course at the BSc in ICT Engineering
- Provide the basics of Computer Architecture to address recent transient execution attacks

Docunque — *Rome, IT*
Back End Developer — *Feb. 2020 - Present*
- Responsible for the Italian Health Service Integration and Communication
- Used Django framework to manage patients, doctors and pharmaceutics

Axbryd — *Rome, IT*
Hardware Architect — *Oct. 2019 - Present*
- Implemented an complete offload system for eBPF from Linux Kernel to a NetFPGA-SUME

University of Rome La Sapienza — *Rome, IT*
Lecturer — *Oct. 2017 - Present*
- Network Infrastructures Course
- Enterprise network organization and management on Unix-like OSs
- c.a. 200 Students from the MSc in: Artificial Intelligence and Robotics, Cybersecurity and Computer Science

BMD S.p.A — *Tivoli Terme, IT*
Application Developer — *Feb. 2019 - Feb. 2020*
- Bug Fixing on an third-party management application written in Angular+Electron for the Sampling and Identification of Biological, Chemical and Radiological Agents, made for the Italian Army
- Re-Writing of the entire application in Visual C# to improve robustness in a mission critical environment

GatesAir — *Brescia, IT*
Embedded System Engineer — *Sept. 2018 - Dec. 2018*
- Porting of the software of their DVB-T Modulator from a STMicroelectronics MCU running Linux Kernel 2.6 on a newly-created board equipped with a Variscite DART-6UL, powered by an NXP i.MX 6UltraLite running kernel 4.9.11

C.N.I.T. *Rome, IT*

HARDWARE RESEARCHER *Sept. 2016 - Oct. 2019*

- Developed a VLIW CPU architecture called Sephirot to efficiently perform packet processing at 100+ Gbps
- Developed the exploit for the Foreshadow-VMM Transient Execution Attack

Projects

eBPF4FPGA

- Hardware facility that allows the offload of eBPF applications to an FPGA
- Comprises an eBPF VLIW Core, HW-implemented maps and HW-implemented helper functions
- Validated on a NetFPGA-SUME

Sephirot

FORMERLY V-PMP

- An extensible and customizable Very-Long Instruction Word Processor
- Supports many Instruction Set Architectures: MIPS, RISC-V RV32I and eBPF
- Design validated at +200MHz on a Xilinx Virtex-7 FPGA

Foreshadow-VMM Exploit

- Exploit that runs both on the kernel and on the user space of the attacker machine
- Breaks the isolation between two VMs running on the same host
- Validated on the KVM hypervisor and on VirtualBox
- Demo here «–

Publications

● M. S. Brunella, G. Bianchi, S. Turco, F. Quaglia, and N. Blefari-Melazzi, "Foreshadow-VMM: Feasibility and Network Perspective," in *2019 IEEE Conference on Network Softwarization (NetSoft)*, pp. 257–259, IEEE, 2019

● M. S. Brunella, S. Turco, G. Bianchi, and N. B. Melazzi, "Foreshadow-VMM: on the practical feasibility of L1 cache Terminal Fault attacks," in *ITASEC 2019*, 2019

● S. Pontarelli, R. Bifulco, M. Bonola, C. Cascone, M. Spaziani, V. Bruschi, D. Sanvito, G. Siracusano, A. Capone, M. Honda, *et al.*, "Flowblaze: Stateful packet processing in hardware," in *16th {USENIX} Symposium on Networked Systems Design and Implementation ({NSDI} 19)*, pp. 531–548, 2019

● M. S. Brunella, S. Pontarelli, M. Bonola, and G. Bianchi, "V-PMP: A VLIW Packet Manipulator Processor," in *2018 European Conference on Networks and Communications (EuCNC)*, pp. 1–9, IEEE, 2018

● M. S. Brunella, S. Pontarelli, F. Marrese, M. Bonola, and G. Bianchi, "Packet Manipulator Processor: A RISC-V VLIW core for networking applications," in *7th RISC-V Workshop*, 2017

● A. Nannarelli, M. Re, G.-C. Cardarilli, L. Di Nunzio, M. S. Brunella, R. Fazzolari, and F. Carbonari, "Robust throughput boosting for low latency dynamic partial reconfiguration," in *2017 30th IEEE International System-on-Chip Conference (SOCC)*, pp. 86–90, IEEE, 2017