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Revision History

Revision Number	Description	Revision Date
001	• initial Release	November 2011

§

Intel® X79 Express Chipset Features

- **Direct Media Interface**
  - NEW: Up to 20 Gb/s each direction, full duplex
  - Lane reversal supported
  - Transparent to software
- **PCI Express* Root Ports**
  - 8 PCI Express* root ports
  - NEW: Supports PCI Express 2.0 running at up to 5.0 GT/s
  - Ports 1-4 and ports 5-8 can independently be configured to support eight x1s, two x4s, two x2s, and four x1s, or one x4 and four x1 port widths.
  - Module based hot-plug supported (that is, ExpressCard*)
  - Lane reversal supported on x4 configuration
- **SGPIO Ports**
  - Serial GPIO controller for SATA only ports
- **Integrated Serial ATA Host Controller**
  - Up to six SATA ports
  - NEW: Data transfer rates up to 6.0 Gb/s (600 MB/s) on up to 2 ports.
  - Data transfer rates up to 3.0 Gb/s (300 MB/s) on up to 1.5 Gb/s (150 MB/s) all ports.
  - Integrated AHCI controller
- **External SATA support**
  - 3.0 Gb/s / 1.5 Gb/s support
  - Port Disable Capability
- **Intel® Rapid Storage Technology enterprise**
  - Configures the PCH chipset SATA ports as a RAID controller supporting RAID 0/1/5/10
- **Intel® High Definition Audio Interface**
  - PCI Express endpoint
  - Independent Bus Master logic for eight general purpose streams: four input and four output
  - Support four external Codecs
  - Supports variable length stream slots
  - Supports multichannel, 32-bit sample depth, 192 kHz sample rate output
  - Provides mic array support
  - Allows for non-48 kHz sampling output
  - Support for ACPI Device States
  - Four PWM signals and Eight TACH signals
- **Simple Serial Transport (SST) 1.0 Bus and Platform Environmental Control Interface (PECI)**
- **USB**
  - Two EHCI Host Controllers, supporting up to fourteen external USB 2.0 ports
  - New: Two USB 2.0 Rate Matching Hubs (RMH) to replace functionality of UHCI controllers
  - Per-Port-Disable Capability
  - Includes up to two USB 2.0 High-speed Debug Ports
  - Supports wake-up from sleeping states S1-S4
  - Supports legacy Keyboard/Mouse software
- **Integrated Gigabit LAN Controller**
  - NEW: Connection utilizes PCI Express pins
  - Integrated ASF Management Controller
  - Network security with System Defense
  - Supports IEEE 802.3
  - 10/100/1000 Mbps Ethernet Support
  - Jumbo Frame Support
- **Power Management Logic**
  - Supports ACPI 4.0a
  - ACPI-defined power states (processor driven C states)
  - ACPI Power Management Timer
  - SMI# generation
  - All registers readable/restorable for proper resume from 0 V core well suspend states
  - Support for APM-based legacy power management for non-ACPI implementations
- **External Glue Integration**
  - Integrated Pull-up, Pull-down and Series Termination resistors on processor I/F
  - Integrated Pull-down and Series resistors on USB
- **Enhanced DMA Controller**
  - Two cascaded 8237 DMA controllers
  - Supports LPC DMA
- **Interrupt Controller**
  - Supports up to eight PCI interrupt pins
  - Supports PCI 2.3 Message Signaled Interrupts
  - Two cascaded 8259 with 15 interrupts
  - Integrated I/O APIC capability with 24 interrupts
  - Supports Processor System Bus interrupt delivery
- **Serial Peripheral Interface (SPI)**
  - Supports up to two SPI devices
  - Supports 20 MHz, 33 MHz SPI devices
  - Support up to two different erase granularities

- **PCI Bus Interface**
  - Supports PCI Rev 2.3 specification at 33 MHz
  - Four available PCI REQ/GNT pairs (shared with GPIO serial expander signals)
  - Support for 64-bit addressing on PCI using DAC protocol
- **SMBus**
  - Interface speeds greater than 100 kbps
  - SMBus/SMLink architecture provides flexibility and optimizes the interface performance
  - Provides independent manageability bus through SMLink interface
  - Supports SMBus 2.0 Specification
  - Host interface allows processor to communicate using SMBus
  - Slave interface allows an external Microcontroller to communicate with PCH
  - Compatible with most two-wire components that are also I^2C* compatible
- **High Precision Event Timers**
  - Advanced operating system interrupt scheduling
- **Timers Based on 8254**
  - System timer, Refresh request, Speaker tone output
- **Real-Time Clock**
  - 256-byte battery-backed CMOS RAM
  - Integrated oscillator components
  - Lower Power DC/DC Converter implementation
- **System TCO Reduction Circuits**
  - Timers to generate SMI# and Reset upon detection of system hang
  - Timers to detect improper processor reset
  - Integrated processor frequency strap logic
  - Supports ability to disable external devices
- **Low Pin Count (LPC) I/F**
  - Supports two Master/DMA devices.
  - Support for Security Device (Trusted Platform Module) connected to LPC.
- **GPIO**
  - TTL, Open-Drain, Inversion
  - GPIO lock down
  - NEW: Additional GPIOs using GPIO Serial Expander
- **JTAG**
  - Boundary Scan for testing during board manufacturing
- **Technologies supported**
  - Intel® Anti-Theft Technology
  - NEW: Network Outbreak Containment Heuristics
- **Miscellaneous**
  - Thermal sensor for die temp tracking
  - 27x27 mm FCBGA package
  - 901 pins (498 signals, 387 power and ground)
  - 1.1 V operation with 1.5 and 3.3 V I/O
  - 1.1 V Core Voltage
  - Five Integrated Voltage Regulators for different power rails
  - Firmware Hub I/F supports BIOS Memory size up to 8 MBytes

Note: This platform does not support Intel® Active Management Technology (Intel® AMT).

§

1 Introduction

1.1 About This Manual

This manual is intended for Original Equipment Manufacturers and BIOS vendors creating Intel®X79 Express Chipset family-based products This manual assumes a working knowledge of the vocabulary and principles of PCI Express*, USB, AHCI, SATA, Intel® High Definition Audio (Intel® HD Audio), SMBus, PCI, ACPI and LPC. Although some details of these features are described within this manual, refer to the individual industry specifications listed in Table 1-1 for the complete details.

Note: The Intel® X79 Express Chipset is also known as the PCH (Platform Controller Hub). In this document, Intel® X79 Express Chipset and PCH are used interchangeably.

Table 1-1. Industry Specifications

Specification	Location
PCI Express* Base Specification, Revision 1.1	http://www.pcisig.com/specifications
PCI Express* Base Specification, Revision 2.0	http://www.pcisig.com/specifications
PCI Express* Base Specification, Revision 3.0 (draft)	http://www.pcisig.com/specifications
Low Pin Count Interface Specification, Revision 1.1 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
System Management Bus Specification, Version 2.0 (SMBus)	http://www.smbus.org/specs/
PCI Local Bus Specification, Revision 2.3 (PCI)	http://www.pcisig.com/specifications
PCI Power Management Specification, Revision 1.2	http://www.pcisig.com/specifications
Universal Serial Bus Specification (USB), Revision 2.0	http://www.usb.org/developers/docs
Advanced Configuration and Power Interface, Version 4.0a (ACPI)	http://www.acpi.info/spec.htm
Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0 (EHCI)	http://developer.intel.com/technology/usb/ehcispec.htm
Serial ATA Specification, Revision 3.0	http://www.serialata.org/specifications.asp
Serial ATA II: Extensions to Serial ATA 1.0, Revision 1.0	http://www.serialata.org/specifications.asp
Serial ATA II Cables and Connectors Volume 2 Gold	http://www.serialata.org/specifications.asp
Alert Standard Format Specification, Version 2.0	http://www.dmtf.org/standards/documents/ASF/DSP0136.pdf
Desktop and mobile Architecture for System Hardware (DASH) Specification 1.1	http://www.dmtf.org/standards/published_documents/DSP2014_1.1.0.pdf
IEEE 802.3 Fast Ethernet	http://standards.ieee.org/getieee802/
AT Attachment - 6 with Packet Interface (ATA/ATAPI - 6)	http://T13.org (T13 1410D)
IA-PC HPET (High Precision Event Timers) Specification, Revision 1.0a	http://www.intel.com/hardwaredesign/hpetspec_1.pdf
TPM Specification 1.02, Level 2 Revision 103	http://www.trustedcomputinggroup.org/specs/TPM
SFF-8485 Specification for Serial GPIO (SGPIO) Bus, Revision 0.7	ftp://ftp.seagate.com/sff/SFF-8485.PDF
Advanced Host Controller Interface specification for Serial ATA, Revision 1.3	http://www.intel.com/technology/serialata/ahci.htm
Intel® High Definition Audio Specification, Revision 1.0a	http://www.intel.com/standards/hdaudio/
MultiProcessor Specification	http://www.intel.com/design/pentium/datashts/242016.HTM

Chapter 1. Introduction
Chapter 1 introduces the Intel® X79 Express Chipset and provides information on manual organization and gives a general overview of the PCH.

Chapter 2. Signal Description
Chapter 2 provides a block diagram of the PCH and a detailed description of each signal. Signals are arranged according to interface and details are provided as to the drive characteristics (Input/Output, Open Drain, and so forth) of all signals.

Chapter 3. PCH **Pin States**
Chapter 3 provides a complete list of signals, their associated power well, their logic level in each suspend state, and their logic level before and after reset.

Chapter 4. PCH **and System Clock Domains**
Chapter 4 provides a list of each clock domain associated with the PCH in an Intel® X79 Express Chipset-based system.

Chapter 5. Functional Description
Chapter 5 provides a detailed description of the functions in the PCH. All PCI buses, devices and functions in this manual are abbreviated using the following nomenclature; Bus:Device:Function. This manual abbreviates buses as B*n*, devices as D*n*, and functions as F*n*. For example Device 31 Function 0 is abbreviated as D31:F0, Bus 1 Device 8 Function 0 is abbreviated as B1:D8:F0. Generally, the bus number will not be used, and can be considered to be Bus 0. The Intel® X79 Express Chipset's external PCI bus is typically Bus 1, but may be assigned a different number depending upon system configuration.

Chapter 6. Ballout Definition
Chapter 6 provides a table of each signal and its ball assignment in the PCH package.

Chapter 7. Package Information
Chapter 7 provides drawings of the physical dimensions and characteristics of the 676-mBGA package.

Chapter 8. Electrical Characteristics
Chapter 8 provides all AC and DC characteristics including detailed timing diagrams.

Chapter 9. Register and Memory Mappings
Chapter 9 provides an overview of the registers, fixed I/O ranges, variable I/O ranges and memory ranges decoded by the PCH.

Chapter 10. Chipset Configuration Registers
Chapter 10 provides a detailed description of all registers and base functionality that is related to chipset configuration and not a specific interface (such as LPC, PCI, or PCI Express). It contains the root complex register block, which describes the behavior of the upstream internal link.

Chapter 11. PCI-to-PCI Bridge Registers
Chapter 11 provides a detailed description of all registers that reside in the PCI-to-PCI bridge. This bridge resides at Device 30, Function 0 (D30:F0).

Chapter 12. Integrated LAN Controller Registers
Chapter 12 provides a detailed description of all registers that reside in the PCH's integrated LAN controller. The integrated LAN Controller resides at Device 25, Function 0 (D25:F0).

Chapter 13. LPC Bridge Registers
Chapter 13 provides a detailed description of all registers that reside in the LPC bridge. This bridge resides at Device 31, Function 0 (D31:F0). This function contains registers for many different units within the PCH including DMA, Timers, Interrupts, Processor Interface, GPIO, Power Management, System Management and RTC.

Chapter 14. SATA Controller Registers
Chapter 14 provides a detailed description of all registers that reside in the SATA controller #1. This controller resides at Device 31, Function 2 (D31:F2).

Chapter 15. SATA Controller Registers
Chapter 15 provides a detailed description of all registers that reside in the SATA controller #2. This controller resides at Device 31, Function 5 (D31:F5).

Chapter 16. EHCI Controller Registers
Chapter 16 provides a detailed description of all registers that reside in the two EHCI host controllers. These controllers reside at Device 29, Function 7 (D29:F7) and Device 26, Function 7 (D26:F7).

Chapter 17. Intel® High Definition Audio Controller Registers
Chapter 17 provides a detailed description of all registers that reside in the Intel® High Definition Audio (Intel® HD Audio) controller. This controller resides at Device 27, Function 0 (D27:F0).

Chapter 18. SMBus Controller Registers
Chapter 18 provides a detailed description of all registers that reside in the SMBus controller. This controller resides at Device 31, Function 3 (D31:F3).

Chapter 19. PCI Express* Port Controller Registers
Chapter 19 provides a detailed description of all registers that reside in the PCI Express controller. This controller resides at Device 28, Functions 0 to 5 (D30:F0-F5).

Chapter 20. High Precision Event Timers Registers
Chapter 20 provides a detailed description of all registers that reside in the multimedia timer memory mapped register space.

Chapter 21. Serial Peripheral Interface Registers
Chapter 21 provides a detailed description of all registers that reside in the SPI memory mapped register space.

Chapter 22. Thermal Sensors
Chapter 22 provides a detailed description of all registers that reside in the thermal sensors PCI configuration space. The registers reside at Device 31, Function 6 (D31:F6).

Chapter 23. Intel® Management Engine (Intel® ME)

Chapter 23 provides a detailed description of all registers that reside in the thermal sensors PCI configuration space. The registers reside at Device 31, Function 6 (D31:F6).

Chapter 24. PCIe* Virtual Root Interface Registers
Chapter 24 provides a detailed description of all registers that reside in the virtual Root port of the PCI Express controller. For virtual root port, this controller resides at Device 17, Function 0 (D17:F0).

1.2 Overview

The PCH provides extensive I/O support. Functions and capabilities include:

- *PCI Express* Base Specification*, Revision 2.0 support for up to eight ports with transfers up to 5 GT/s.
- *PCI Local Bus Specification*, Revision 2.3 support for 33 MHz PCI operations (supports up to four Req/Gnt pairs).
- ACPI Power Management Logic Support, Revision 4.0a
- Enhanced DMA controller, interrupt controller, and timer functions

- Integrated Serial ATA host controllers with independent DMA operation on up to six ports.
- USB host interface with two EHCI high-speed USB 2.0 Host controllers and 2 rate matching hubs provide support for support for up to fourteen USB 2.0 ports
- Integrated 10/100/1000 Gigabit Ethernet MAC with System Defense
- *System Management Bus (SMBus) Specification*, Version 2.0 with additional support for I^2C* devices
- Supports Intel® High Definition Audio
- Supports Intel® Rapid Storage Technology enterprise (Intel® RSTe)
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support
- Serial Peripheral Interface (SPI) support
- Intel® Anti-Theft Technology (Intel® AT)
- JTAG Boundary Scan support

The PCH incorporates a variety of PCI devices and functions. Refer to Table 9-1 for details.

1.2.1 Capability Overview

The following sub-sections provide an overview of the PCH capabilities.

Digital Media Interface (DMI)

Digital Media Interface (DMI) is the chip-to-chip connection between the processor and PCH. This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities. Base functionality is completely software-transparent, permitting current and legacy software to operate normally.

PCI Express* Root Port

The PCH provides up to 8 PCI Express Root Ports, supporting the *PCI Express Base Specification*, Revision 2.0. Each Root Port x1 lane supports up to 5 Gb/s bandwidth in each direction (10 Gb/s concurrent). PCI Express Root Ports 1–4 or Ports 5–8 can independently be configured to support four x1s, two x2s, one x2 and two x1s, or one x4 port widths.

Serial ATA (SATA) Controller

The PCH has two integrated SATA host controllers that support independent DMA operation on up to six ports and supports data transfer rates of up to 6.0 Gb/s (600 MB/s) on up to two ports (Port 0 and 1 Only) while all ports support rates up to 3.0 Gb/s (300 MB/s) and up to 1.5 Gb/s (150 MB/s). The SATA controller contains two modes of operation – a legacy mode using I/O space, and an AHCI mode using memory space. Software that uses legacy mode will not have AHCI capabilities.

The PCH supports the *Serial ATA Specification*, Revision 3.0. The PCH also supports several optional sections of the Serial ATA II: Extensions to *Serial ATA 1.0 Specification*, Revision 1.0 (AHCI support is required for some elements).

AHCI

The PCH provides hardware support for Advanced Host Controller Interface (AHCI), a standardized programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave

designation for SATA devices—each device is treated as a master—and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug. AHCI requires appropriate software support (for example, an AHCI driver) and for some features, hardware support in the SATA device or additional platform hardware.

Intel® Rapid Storage Technology enterprise (RSTe)

The PCH provides support for Intel® Rapid Storage Technology enterprise, providing both AHCI (see above for details on AHCI) and integrated RAID functionality. The industry-leading RAID capability provides high-performance RAID 0, 1, 5, and 10 functionality on up to 6 SATA ports of the PCH. Matrix RAID support is provided to allow multiple RAID levels to be combined on a single set of hard drives, such as RAID 0 and RAID 1 on two disks. Other RAID features include hot-spare support, SMART alerting, and RAID 0 auto replace. Software components include an Option ROM for pre-boot configuration and boot functionality, a Microsoft Windows* compatible driver, and a user interface for configuration and management of the RAID capability of the PCH.

PCI Interface

The PCH PCI interface provides a 33 MHz, Revision 2.3 implementation. The PCH integrates a PCI arbiter that supports up to four external PCI bus masters in addition to the internal PCH requests. This allows for combinations of up to four PCI down devices and PCI slots.

Low Pin Count (LPC) Interface

The PCH implements an LPC Interface as described in the *LPC 1.1 Specification*. The Low Pin Count (LPC) bridge function of the PCH resides in PCI Device 31:Function 0. In addition to the LPC bridge interface function, D31:F0 contains other functional units including DMA, interrupt controllers, timers, power management, system management, GPIO, and RTC.

Serial Peripheral Interface (SPI)

The PCH implements an SPI Interface as an alternative interface for the BIOS flash device. An SPI flash device can be used as a replacement for the FWH, and is required to support Gigabit Ethernet. The PCH supports up to two SPI flash devices with speeds up to 50 MHz, using two chip select pins.

Compatibility Modules (DMA Controller, Timer/Counters, Interrupt Controller)

The DMA controller incorporates the logic of two 8237 DMA controllers, with seven independently programmable channels. Channels 0–3 are hardwired to 8-bit, count-by-byte transfers, and channels 5–7 are hardwired to 16-bit, count-by-word transfers. Any two of the seven DMA channels can be programmed to support fast Type-F transfers. Channel 4 is reserved as a generic bus master request.

The PCH supports LPC DMA, which is similar to ISA DMA, through the PCH's DMA controller. LPC DMA is handled through the use of the LDRQ# lines from peripherals and special encoding on LAD[3:0] from the host. Single, Demand, Verify, and Increment modes are supported on the LPC interface.

The timer/counter block contains three counters that are equivalent in function to those found in one 8254 programmable interval timer. These three counters are combined to provide the system timer function, and speaker tone. The 14.31818 MHz oscillator input provides the clock source for these three counters.

The PCH provides an ISA-Compatible Programmable Interrupt Controller (PIC) that incorporates the functionality of two 8259 interrupt controllers. The two interrupt controllers are cascaded so that 14 external and two internal interrupts are possible. In addition, the PCH supports a serial interrupt scheme.

All of the registers in these modules can be read and restored. This is required to save and restore system state after power has been removed and restored to the platform.

Advanced Programmable Interrupt Controller (APIC)

In addition to the standard ISA compatible Programmable Interrupt controller (PIC) described in the previous section, the PCH incorporates the Advanced Programmable Interrupt Controller (APIC).

Universal Serial Bus (USB) Controllers

The PCH has up to two Enhanced Host Controller Interface (EHCI) host controllers that support USB high-speed signaling. High-speed USB 2.0 allows data transfers up to 480 Mb/s which is 40 times faster than full-speed USB. The PCH supports up to fourteen USB 2.0 ports. All fourteen ports are high-speed, full-speed, and low-speed capable.

Gigabit Ethernet Controller

The Gigabit Ethernet Controller provides a system interface using a PCI function. The controller provides a full memory-mapped or IO mapped interface along with a 64-bit address master support for systems using more than 4 GB of physical memory and DMA (Direct Memory Addressing) mechanisms for high performance data transfers. Its bus master capabilities enable the component to process high-level commands and perform multiple operations; this lowers processor utilization by off-loading communication tasks from the processor. Two large configurable transmit and receive FIFOs (up to 20 KB each) help prevent data underruns and overruns while waiting for bus accesses. This enables the integrated LAN controller to transmit data with minimum interframe spacing (IFS).

The LAN controller can operate at multiple speeds (10/100/1000 MB/s) and in either full duplex or half duplex mode. In full duplex mode the LAN controller adheres with the *IEEE 802.3x Flow Control* Specification. Half duplex performance is enhanced by a proprietary collision reduction mechanism. See Section 5.4 for details.

RTC

The PCH contains a Motorola MC146818B-compatible real-time clock with 256 bytes of battery-backed RAM. The real-time clock performs two key functions – keeping track of the time of day and storing system data, even when the system is powered down. The RTC operates on a 32.768 KHz crystal and a 3 V battery.

The RTC also supports two lockable memory ranges. By setting bits in the configuration space, two 8-byte ranges can be locked to read and write accesses. This prevents unauthorized reading of passwords or other system security information.

The RTC also supports a date alarm that allows for scheduling a wake up event up to 30 days in advance, rather than just 24 hours in advance.

GPIO

Various general purpose inputs and outputs are provided for custom system design. The number of inputs and outputs varies depending on the PCH configuration.

Enhanced Power Management

The PCH's power management functions include enhanced clock control and various low-power (suspend) states (for example, Suspend-to-RAM and Suspend-to-Disk). A hardware-based thermal management circuit permits software-independent entrance to low-power states. The PCH contains full support for the *Advanced Configuration and Power Interface (ACPI) Specification*, Revision 4.0a.

Manageability

The PCH integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

- **TCO Timer.** The PCH's integrated programmable TCO timer is used to detect system locks. The first expiration of the timer generates an SMI# that the system can use to recover from a software lock. The second expiration of the timer causes a system reset to recover from a hardware lock.
- **Processor Present Indicator.** The PCH looks for the processor to fetch the first instruction after reset. If the processor does not fetch the first instruction, the PCH will reboot the system.
- **ECC Error Reporting.** When detecting an ECC error, the host controller has the ability to send one of several messages to the PCH. The host controller can instruct the PCH to generate either an SMI#, NMI, SERR#, or TCO interrupt.
- **Function Disable.** The PCH provides the ability to disable the following integrated functions: LAN, USB, LPC, Intel HD Audio, SATA, PCI Express or SMBus. Once disabled, these functions no longer decode I/O, memory, or PCI configuration space. Also, no interrupts or power management events are generated from the disabled functions.
- **Intruder Detect.** The PCH provides an input signal (INTRUDER#) that can be attached to a switch that is activated by the system case being opened. The PCH can be programmed to generate an SMI# or TCO interrupt due to an active INTRUDER# signal.

System Management Bus (SMBus 2.0)

The PCH contains an SMBus Host interface that allows the processor to communicate with SMBus slaves. This interface is compatible with most I^2C devices. Special I^2C commands are implemented.

The PCH's SMBus host controller provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves). Also, the PCH supports slave functionality, including the Host Notify protocol. Hence, the host controller supports eight command protocols of the SMBus interface (see *System Management Bus (SMBus) Specification*, Version 2.0) – Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, Block Read/Write, and Host Notify.

The PCH's SMBus also implements hardware-based Packet Error Checking for data robustness and the Address Resolution Protocol (ARP) to dynamically provide address to all SMBus devices.

Intel HD Audio Controller

The *Intel® High Definition Audio Specification* defines a digital interface that can be used to attach different types of codecs, such as audio and modem codecs. The PCH Intel HD Audio controller supports up to 4 codecs. The link can operate at either 3.3 V or 1.5 V.

With the support of multi-channel audio stream, 32-bit sample depth, and sample rate up to 192 kHz, the Intel® HD Audio controller provides audio quality that can deliver CE levels of audio experience. On the input side, the PCH adds support for an array of microphones.

Fan Speed Control

The PCH integrates four fan speed sensors (four TACH signals) and four fan speed controllers (three Pulse Width Modulator signals), which enables monitoring and controlling up to four fans on the system. With the new implementation of the single-wire Simple Serial Transport (SST) 1.0 bus and Platform Environmental Control Interface (PECI), the PCH provides an easy way to connect to SST-based thermal sensors and access the processor thermal data.

JTAG Boundary-Scan

The PCH adds the industry standard JTAG interface and enables Boundary-Scan in place of the XOR chains used in previous generations of chipsets. Boundary-Scan can be used to ensure device connectivity during the board manufacturing process. The JTAG interface allows system manufacturers to improve efficiency by using industry available tools to test the PCH on an assembled board. Since JTAG is a serial interface, it eliminates the need to create probe points for every pin in an XOR chain. This eases pin breakout and trace routing and simplifies the interface between the system and a bed-of-nails tester.

Note: Contact your local Intel Field Sales Representative for additional information about JTAG usage on the PCH.

§ §

2 Signal Description

This chapter provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

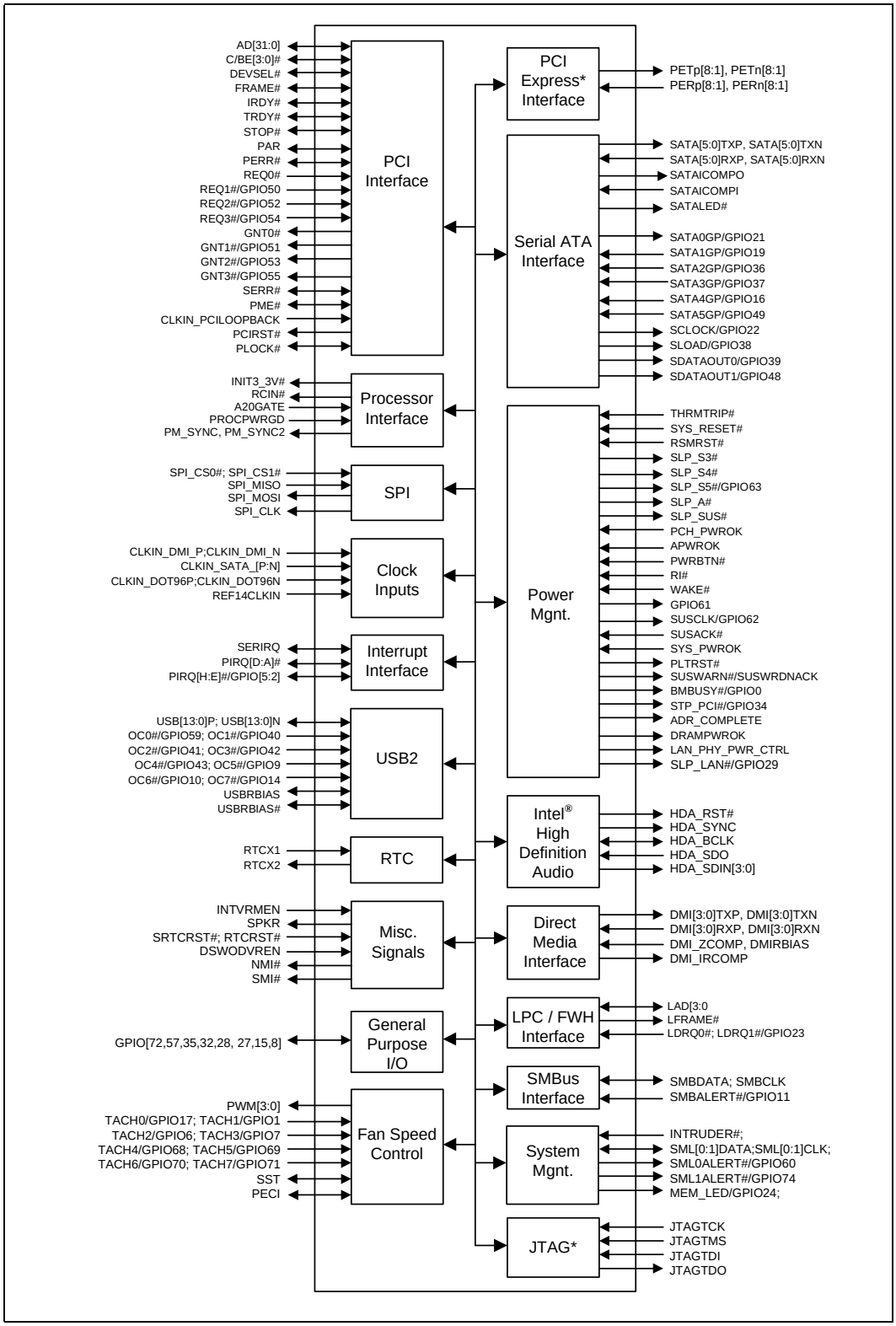
The "#" symbol at the end of the signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at the high voltage level.

The following notations are used to describe the signal type:

I	Input Pin
O	Output Pin
OD O	Open Drain Output Pin.
I / OD	Bi-directional Input/Open Drain Output Pin.
I / O	Bi-directional Input / Output Pin.
CMOS	CMOS buffers. 1.5 V tolerant.
COD	CMOS Open Drain buffers. 3.3 V tolerant.
HVCMOS	High Voltage CMOS buffers. 3.3 V tolerant.
A	Analog reference or output.

The "Type" for each signal is indicative of the functional operating mode of the signal. Unless otherwise noted in Section 3.2 or Section 3.3, a signal is considered to be in the functional operating mode after RTCRST# deasserts for signals in the RTC well, after RSMRST# deasserts for signals in the suspend well, and after PCH_PWROK asserts for signals in the core well, after DPWROK asserts for Signals in the Deep Sleep well, after APWROK asserts for Signals in the Active Sleep well.

Figure 2-1. PCH Chipset Interface Signals Block Diagram



2.1 Direct Media Interface (DMI) to Host Controller

Table 2-1. Direct Media Interface Signals

Name	Type	Description
DMI_TXP_0, DMI_TXN_0	O	**Direct Media Interface Differential Transmit Pair 0**
DMI_RXP_0, DMI_RXN_0	I	**Direct Media Interface Differential Receive Pair 0**
DMI_TXP_1, DMI_TXN_1	O	**Direct Media Interface Differential Transmit Pair 1**
DMI_RXP_1, DMI_RXN_1	I	**Direct Media Interface Differential Receive Pair 1**
DMI_TXP_2, DMI_TXN_2	O	**Direct Media Interface Differential Transmit Pair 2**
DMI_RXP_2, DMI_RXN_2	I	**Direct Media Interface Differential Receive Pair 2**
DMI_TXP_3, DMI_TXN_3	O	**Direct Media Interface Differential Transmit Pair 3**
DMI_RXP_3, DMI_RXN_3	I	**Direct Media Interface Differential Receive Pair 3**
DMI_ZCOMP	I	**Impedance Compensation Input:** Determines DMI input impedance.
DMI_IRCOMP	O	**Impedance/Current Compensation Output:** Determines DMI output impedance and bias current.
DMIRBIAS	I/O	**DMIRBIAS:** Analog connection point for 750 Ω ±1% external precision resistor

2.2 PCI Express*

Table 2-2. PCI Express* Signals

Name	Type	Description
PETp1, PETn1	O	**PCI Express* Differential Transmit Pair 1**
PERp1, PERn1	I	**PCI Express Differential Receive Pair 1**
PETp2, PETn2	O	**PCI Express Differential Transmit Pair 2**
PERp2, PERn2	I	**PCI Express Differential Receive Pair 2**
PETp3, PETn3	O	**PCI Express Differential Transmit Pair 3**
PERp3, PERn3	I	**PCI Express Differential Receive Pair 3**
PETp4, PETn4	O	**PCI Express Differential Transmit Pair 4**
PERp4, PERn4	I	**PCI Express Differential Receive Pair 4**
PETp5, PETn5	O	**PCI Express Differential Transmit Pair 5**
PERp5, PERn5	I	**PCI Express Differential Receive Pair 5**
PETp6, PETn6	O	**PCI Express Differential Transmit Pair 6**
PERp6, PERn6	I	**PCI Express Differential Receive Pair 6**
PETp7, PETn7	O	**PCI Express Differential Transmit Pair 7**
PERp7, PERn7	I	**PCI Express Differential Receive Pair 7**
PETp8, PETn8	O	**PCI Express Differential Transmit Pair 8**
PERp8, PERn8	I	**PCI Express Differential Receive Pair 8**

2.3 PCI Express 8GT/s Uplink

Note: These signals are not used on the PCH. They are reserved for future use.

Table 2-3. PCI Express* Uplink Signals

Name	Type	Description
PEG0_Tp[3:0], PEG0_Tn[3:0]	O	Reserved for future use. ***Note:*** These signals should be no connects.
PEG0_Rp[3:0], PEG0_Rn[3:0]	I	Reserved for future use. ***Note:*** These signals should be no connects.
PEG0_RBIASP, PEG0_RBIASN	I	Reserved for future use. ***Note:*** These signals should be no connects.

2.4 PCI Interface

Table 2-4. PCI Interface Signals (Sheet 1 of 3)

Name	Type	Description
AD[31:0]	I/O	**PCI Address/Data**: AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical address (32 bits). During subsequent clocks, AD[31:0] contain data. The PCH will drive all 0s on AD[31:0] during the address phase of all PCI Special Cycles.
C/BE[3:0]#	I/O	**Bus Command and Byte Enables**: The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase, C/BE[3:0]# define the Byte Enables. **C/BE[3:0]#** — **Command Type** 0000b — Interrupt Acknowledge 0001b — Special Cycle 0010b — I/O Read 0011b — I/O Write 0110b — Memory Read 0111b — Memory Write 1010b — Configuration Read 1011b — Configuration Write 1100b — Memory Read Multiple 1110b — Memory Read Line 1111b — Memory Write and Invalidate All command encodings not shown are reserved. The PCH does not decode reserved values, and therefore will not respond if a PCI master generates a cycle using one of the reserved values.
DEVSEL#	I/O	**Device Select**: The PCH asserts DEVSEL# to claim a PCI transaction. As an output, the PCH asserts DEVSEL# when a PCI master peripheral attempts an access to an internal PCH address or an address destined for DMI (main memory or graphics). As an input, DEVSEL# indicates the response to a PCH -initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PLTRST#. DEVSEL# remains tri-stated by the PCH until driven by a target device.
FRAME#	I/O	**Cycle Frame:** The current initiator drives FRAME# to indicate the beginning and duration of a PCI transaction. While the initiator asserts FRAME#, data transfers continue. When the initiator negates FRAME#, the transaction is in the final data phase. FRAME# is an input to the PCH when the PCH is the target, and FRAME# is an output from the PCH when the PCH is the initiator. FRAME# remains tri-stated by the PCH until driven by an initiator.

Table 2-4. PCI Interface Signals (Sheet 2 of 3)

Name	Type	Description
IRDY#	I/O	**Initiator Ready**: IRDY# indicates the PCH 's ability, as an initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the PCH has valid data present on AD[31:0]. During a read, it indicates the PCH is prepared to latch data. IRDY# is an input to the PCH when the PCH is the target and an output from the PCH when the PCH is an initiator. IRDY# remains tri-stated by the PCH until driven by an initiator.
TRDY#	I/O	**Target Ready**: TRDY# indicates the PCH 's ability as a target to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the PCH, as a target, has placed valid data on AD[31:0]. During a write, TRDY# indicates the PCH, as a target is prepared to latch data. TRDY# is an input to the PCH when the PCH is the initiator and an output from the PCH when the PCH is a target. TRDY# is tri-stated from the leading edge of PLTRST#. TRDY# remains tri-stated by the PCH until driven by a target.
STOP#	I/O	**Stop**: STOP# indicates that the PCH, as a target, is requesting the initiator to stop the current transaction. STOP# causes the PCH, as an initiator, to stop the current transaction. STOP# is an output when the PCH is a target and an input when the PCH is an initiator.
PAR	I/O	**Calculated/Checked Parity:** PAR uses "even" parity calculated on 36 bits, AD[31:0] plus C/BE[3:0]#. "Even" parity means that the PCH counts the number of ones within the 36 bits plus PAR and the sum is always even. The PCH always calculates PAR on 36 bits regardless of the valid byte enables. The PCH generates PAR for address and data phases and only ensures PAR to be valid one PCI clock after the corresponding address or data phase. The PCH drives and tri-states PAR identically to the AD[31:0] lines except that the PCH delays PAR by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all PCH initiated transactions. PAR is an output during the data phase (delayed one clock) when the PCH is the initiator of a PCI write transaction, and when it is the target of a read transaction. PCH checks parity when it is the target of a PCI write transaction. If a parity error is detected, the PCH will set the appropriate internal status bits, and has the option to generate an NMI# or SMI#.
PERR#	I/O	**Parity Error**: An external PCI device drives PERR# when it receives data that has a parity error. The PCH drives PERR# when it detects a parity error. The PCH can either generate an NMI# or SMI# upon detecting a parity error (either detected internally or reported using the PERR# signal).
REQ0# **REQ1#/** GPIO50 / GSXCLK **REQ2#/** GPIO52 / GSXSLOAD **REQ3#/**GPIO54 / GSXRESET#	I	**PCI Requests**: The PCH supports up to 4 masters on the PCI bus. REQ[3:1]# pins can instead be used as GPIO. REQ[3:1]# pins can also be use as GSX signals. (See Section 2.23 for details.) ***Notes:*** External pull-up resistor is required. When used as native functionality, the pull-up resistor may be to either 3.3 V or 5.0 V per PCI specification. When used as GPIO or not used at all, the pull-up resistor should be to the Vcc3_3 rail.
GNT0# **GNT1#/** GPIO51 / GSXDOUT **GNT2#**/ GPIO53 / GSXDIN **GNT3#**/GPIO55	O	**PCI Grants**: The PCH supports up to 4 masters on the PCI bus. GNT[3:1]# pins can instead be used as GPIO. GNT[2:1]# pins can also be use as GSX signals. (See Section 2.23 for details.) Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail. ***Note:*** GNT[3:1]#/GPIO[55,53,51] are sampled as a functional strap. See Section 2.26.1 for details.
PCIRST#	O	**PCI Reset:** This is the Secondary PCI Bus reset signal. It is a logical OR of the primary interface PLTRST# signal and the state of the Secondary Bus Reset bit of the Bridge Control register (D30:F0:3Eh, bit 6).
PLOCK#	I/O	**PCI Lock**: This signal indicates an exclusive bus operation and may require multiple transactions to complete. PCH asserts PLOCK# when it performs non-exclusive transactions on the PCI bus. PLOCK# is ignored when PCI masters are granted the bus.
SERR#	I/OD	**System Error**: SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the PCH has the ability to generate an NMI, SMI#, or interrupt.

Table 2-4. PCI Interface Signals (Sheet 3 of 3)

Name	Type	Description
PME#	I/OD	**PCI Power Management Event**: PCI peripherals drive PME# to wake the system from low-power states S1–S5. PME# assertion can also be enabled to generate an SCI from the S0 state. In some cases the PCH may drive PME# active due to an internal wake event. The PCH will not drive PME# high, but it will be pulled up to VccSus3_3 by an internal pull-up resistor.

2.5 Serial ATA Interface

Table 2-5. Serial ATA Interface Signals (Sheet 1 of 2)

Name	Type	Description
SATA0TXP **SATA0TXN**	O	**Serial ATA 0 Differential Transmit Pairs:** These are outbound high-speed differential signals to Port 0. In compatible mode, SATA Port 0 is the primary master of SATA Controller 1. Supports up to 6 Gb/s, 3 Gb/s, and 1.5 Gb/s.
SATA0RXP **SATA0RXN**	I	**Serial ATA 0 Differential Receive Pair:** These are inbound high-speed differential signals from Port 0. In compatible mode, SATA Port 0 is the primary master of SATA Controller 1. Supports up to 6 Gb/s, 3 Gb/s, and 1.5 Gb/s.
SATA1TXP **SATA1TXN**	O	**Serial ATA 1 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 1. In compatible mode, SATA Port 1 is the secondary master of SATA Controller 1. Supports up to 6 Gb/s, 3 Gb/s, and 1.5 Gb/s.
SATA1RXP **SATA1RXN**	I	**Serial ATA 1 Differential Receive Pair:** These are inbound high-speed differential signals from Port 1. In compatible mode, SATA Port 1 is the secondary master of SATA Controller 1. Supports up to 6 Gb/s, 3 Gb/s, and 1.5 Gb/s.
SATA2TXP **SATA2TXN**	O	**Serial ATA 2 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 2. In compatible mode, SATA Port 2 is the primary slave of SATA Controller 1. Supports up to 3 Gb/s and 1.5 Gb/s.
SATA2RXP **SATA2RXN**	I	**Serial ATA 2 Differential Receive Pair:** These are inbound high-speed differential signals from Port 2. In compatible mode, SATA Port 2 is the primary slave of SATA Controller 1 Supports up to 3 Gb/s and 1.5 Gb/s.
SATA3TXP **SATA3TXN**	O	**Serial ATA 3 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 3 In compatible mode, SATA Port 3 is the secondary slave of SATA Controller 1 Supports up to 3 Gb/s and 1.5 Gb/s.
SATA3RXP **SATA3RXN**	I	**Serial ATA 3 Differential Receive Pair:** These are inbound high-speed differential signals from Port 3 In compatible mode, SATA Port 3 is the secondary slave of SATA Controller 1 Supports up to 3 Gb/s and 1.5 Gb/s.
SATA4TXP **SATA4TXN**	O	**Serial ATA 4 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 4. In compatible mode, SATA Port 4 is the primary master of SATA Controller 2. Supports up to 3 Gb/s and 1.5 Gb/s.
SATA4RXP **SATA4RXN**	I	**Serial ATA 4 Differential Receive Pair:** These are inbound high-speed differential signals from Port 4. In compatible mode, SATA Port 4 is the primary master of SATA Controller 2. Supports up to 3 Gb/s and 1.5 Gb/s.
SATA5TXP **SATA5TXN**	O	**Serial ATA 5 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 5. In compatible mode, SATA Port 5 is the secondary master of SATA Controller 2. Supports up to 3 Gb/s and 1.5 Gb/s.

Table 2-5. Serial ATA Interface Signals (Sheet 2 of 2)

Name	Type	Description
SATA5RXP **SATA5RXN**	I	**Serial ATA 5 Differential Receive Pair:** These are inbound high-speed differential signals from Port 5. In compatible mode, SATA Port 5 is the secondary master of SATA Controller 2. Supports up to 3 Gb/s and 1.5 Gb/s.
SATAICOMPO	O	**Serial ATA Compensation Output:** Connected to an external precision resistor to VccCore. Must be connected to **SATAICOMPI** on the board.
SATAICOMPI	I	**Serial ATA Compensation Input:** Connected to **SATAICOMPO** on the board.
SATA0GP / GPIO21	I	**Serial ATA 0 General Purpose:** This is an input pin which can be configured as an interlock switch corresponding to SATA Port 0. When used as an interlock switch status indication, this signal should be drive to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. If interlock switches are not required, this pin can be configured as GPIO21.
SATA1GP / GPIO19	I	**Serial ATA 1 General Purpose:** Same function as SATA0GP, except for SATA Port 1. If interlock switches are not required, this pin can be configured as GPIO19.
SATA2GP / GPIO36	I	**Serial ATA 2 General Purpose:** Same function as SATA0GP, except for SATA Port 2. If interlock switches are not required, this pin can be configured as GPIO36.
SATA3GP / GPIO37	I	**Serial ATA 3 General Purpose:** Same function as SATA0GP, except for SATA Port 3. If interlock switches are not required, this pin can be configured as GPIO37.
SATA4GP / GPIO16	I	**Serial ATA 4 General Purpose:** Same function as SATA0GP, except for SATA Port 4. If interlock switches are not required, this pin can be configured as GPIO16.
SATA5GP / GPIO49 / TEMP_ALERT#	I	**Serial ATA 5 General Purpose:** Same function as SATA0GP, except for SATA Port 5. If interlock switches are not required, this pin can be configured as GPIO49 or TEMP_ALERT#.
SATALED#	OD O	**Serial ATA LED:** This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc3_3 is required.
SCLOCK/GPIO22	OD O	**SGPIO Reference Clock:** The SATA controller uses rising edges of this clock to transmit serial data, and the target uses the falling edge of this clock to latch data. The SCLOCK frequency supported is 32 kHz. If SGPIO interface is not used, this signal can be used as a GPIO22.
SLOAD/GPIO38	OD O	**SGPIO Load:** The controller drives a '1' at the rising edge of SCLOCK to indicate either the start or end of a bit stream. A 4-bit vendor specific pattern will be transmitted right after the signal assertion. If SGPIO interface is not used, this signal can be used as a GPIO.
SDATAOUT0/ GPIO39 **SDATAOUT1**/ GPIO48	OD O	**SGPIO Dataout:** Driven by the controller to indicate the drive status in the following sequence: drive 0, 1, 2, 3, 4, 5, 0, 1, 2... If SGPIO interface is not used, the signals can be used as GPIO.
SATA3RBIAS	I/O	**DMI RBIAS:** Analog connection point for an external precision resistor.
SATA3COMPI	I	**Impedance Compensation Input:** Connected to a 50 ohm (1%) precision external pull-up resistor to vccsata3.
SATA3COMPO	O	**Impedance/Current Compensation Output:** Connected to a 50 ohm (1%) precision external pull-up resistor.to vccsata3.

2.6 SAS Interface

Note: These signals are not used on the PCH. They are reserved for future use.

Table 2-6. SAS Interface Signals (Sheet 1 of 2)

Name	Type	Description
SAS0TXP **SAS0TXN**	O	Reserved for future use. ***Note:*** These signals should be no connects.
SAS0RXP **SAS0RXN**	I	Reserved for future use. ***Note:*** These signals should be no connects.
SAS1TXP **SAS1TXN**	O	Reserved for future use. ***Note:*** These signals should be no connects.
SAS1RXP **SAS1RXN**	I	Reserved for future use. ***Note:*** These signals should be no connects.
SAS2TXP **SAS2TXN**	O	Reserved for future use. ***Note:*** These signals should be no connects.
SAS2RXP **SAS2RXN**	I	Reserved for future use. ***Note:*** These signals should be no connects.
SAS3TXP **SAS3TXN**	O	Reserved for future use. ***Note:*** These signals should be no connects.
SAS3RXP **SAS3RXN**	I	Reserved for future use. ***Note:*** These signals should be no connects.
SAS4TXP **SAS4TXN**	O	Reserved for future use. ***Note:*** These signals should be no connects.
SAS4RXP **SAS4RXN**	I	Reserved for future use. ***Note:*** These signals should be no connects.
SAS5TXP **SAS5TXN**	O	Reserved for future use. ***Note:*** These signals should be no connects.
SAS5RXP **SAS5RXN**	I	Reserved for future use. ***Note:*** These signals should be no connects.
SAS6TXP **SAS6TXN**	O	Reserved for future use. ***Note:*** These signals should be no connects.
SAS6RXP **SAS6RXN**	I	Reserved for future use. ***Note:*** These signals should be no connects.
SAS7TXP **SAS7TXN**	O	Reserved for future use. ***Note:*** These signals should be no connects.
SAS7RXP **SAS7RXN**	I	Reserved for future use. ***Note:*** These signals should be no connects.
SAS_CLOCK1	O	Reserved for future use. ***Note:*** This signal should be connected.
SAS_LOAD1	O	Reserved for future use. ***Note:*** This signal should be a no connect.
SAS_DATAIN1	O	Reserved for future use. ***Note:*** This signal should be a no connect.
SAS_DATAOUT1	O	Reserved for future use. ***Note:*** This signal should be a no connect.
SAS_CLOCK2	O	Reserved for future use. ***Note:*** This signal should be a no connect.
SAS_LOAD2	O	Reserved for future use. ***Note:*** This signal should be a no connect.
SAS_DATAIN2	O	Reserved for future use. ***Note:*** This signal should be a no connect.

Table 2-6. SAS Interface Signals (Sheet 2 of 2)

Name	Type	Description
SAS_DATAOUT2	O	Reserved for future use. ***Note:*** This signal should be a no connect.
SAS_LED#	O	Reserved for future use. ***Note:*** This signal should be a no connect.
SAS_RBIASP0	I	Reserved for future use. ***Note:*** This signal tied to SAS_RBIASN0 through a 6.0 KΩ ±1% resistor. SAS_RBIASNO should be connected to V_{SS} at the resistor.
SAS_RBIASN0	I	Reserved for future use. ***Note:*** This signal tied to SAS_RBIASN0 through a 6.0 KΩ ±1% resistor. SAS_RBIASNO should be connected to V_{SS} at the resistor.
SAS_RBIASP1	I	Reserved for future use. ***Note:*** This signal should be a no connect.
SAS_RBIASN1	I	Reserved for future use. ***Note:*** This signal should be a no connect.

2.7 LPC Interface

Table 2-7. LPC Interface Signals

Name	Type	Description
LAD[3:0]	I/O	**LPC Multiplexed Command, Address, Data:** For LAD[3:0], internal pull-ups are provided.
LFRAME#	O	**LPC Frame:** LFRAME# indicates the start of an LPC cycle, or an abort.
LDRQ0#, LDRQ1# / GPIO23	I	**LPC Serial DMA/Master Request Inputs:** LDRQ[1:0]# are used to request DMA or bus master access. These signals are typically connected to an external Super I/O device. An internal pull-up resistor is provided on these signals. LDRQ1# may optionally be used as GPIO.

2.8 Interrupt Interface

Table 2-8. Interrupt Signals

Name	Type	Description
SERIRQ	I/OD	**Serial Interrupt Request:** This pin implements the serial interrupt protocol.
PIRQ[D:A]#	I/OD	**PCI Interrupt Requests:** In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, or 15 as described in Section 5.9.6. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQA# is connected to IRQ16, PIRQB# to IRQ17, PIRQC# to IRQ18, and PIRQD# to IRQ19. This frees the legacy interrupts. These signals are 5 V tolerant.
PIRQ[H:E]# / GPIO[5:2]	I/OD	**PCI Interrupt Requests:** In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, or 15 as described in Section 5.9.6. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQE# is connected to IRQ20, PIRQF# to IRQ21, PIRQG# to IRQ22, and PIRQH# to IRQ23. This frees the legacy interrupts. If not needed for interrupts, these signals can be used as GPIO. These signals are 5 V tolerant.

Note: PIRQ Interrupts can only be shared if it is configured as level sensitive. They cannot be shared if configured as edge triggered.

2.9 USB 2.0 Interface

Table 2-9. USB 2.0 Interface Signals (Sheet 1 of 2)

Name	Type	Description
USBP0P, USBP0N, USBP1P, USBP1N	I/O	**Universal Serial Bus Port [1:0] Differential**: These differential pairs are used to transmit Data/Address/Command signals for ports 0 and 1. These ports can be routed to EHCI controller #1. ***Note:*** No external resistors are required on these signals. The PCH integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP2P, USBP2N, USBP3P, USBP3N	I/O	**Universal Serial Bus Port [3:2] Differential**: These differential pairs are used to transmit data/address/command signals for ports 2 and 3. These ports can be routed to EHCI controller #1. ***Note:*** No external resistors are required on these signals. The PCH integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP4P, USBP4N, USBP5P, USBP5N	I/O	**Universal Serial Bus Port [5:4] Differential**: These differential pairs are used to transmit Data/Address/Command signals for ports 4 and 5. These ports can be routed to EHCI controller #1. ***Note:*** No external resistors are required on these signals. The PCH integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP6P, USBP6N, USBP7P, USBP7N	I/O	**Universal Serial Bus Port [7:6] Differential**: These differential pairs are used to transmit Data/Address/Command signals for ports 6 and 7. These ports can be routed to EHCI controller #1. ***Note:*** No external resistors are required on these signals. The PCH integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.

Table 2-9. USB 2.0 Interface Signals (Sheet 2 of 2)

Name	Type	Description
USBP8P, USBP8N, USBP9P, USBP9N	I/O	**Universal Serial Bus Port [9:8] Differential**: These differential pairs are used to transmit Data/Address/Command signals for ports 8 and 9. These ports can be routed to EHCI controller #2. ***Note:*** No external resistors are required on these signals. The PCH integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP10P, USBP10N, USBP11P, USBP11N	I/O	**Universal Serial Bus Port [11:10] Differential**: These differential pairs are used to transmit Data/Address/Command signals for ports 10 and 11. These ports can be routed to EHCI controller #2. ***Note:*** No external resistors are required on these signals. The PCH integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP12P, USBP12N, USBP13P, USBP13N	I/O	**Universal Serial Bus Port [13:12] Differential**: These differential pairs are used to transmit Data/Address/Command signals for ports 13 and 12. These ports can be routed to EHCI controller #2. ***Note:*** No external resistors are required on these signals. The PCH integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
OC0# / GPIO59 **OC1#** / GPIO40 **OC2#** / GPIO41 **OC3#** / GPIO42 **OC4#** / GPIO43 **OC5#** / GPIO9 **OC6#** / GPIO10 **OC7#** / GPIO14	I	**Overcurrent Indicators**: These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred. OC[7:0]# may optionally be used as GPIOs. ***Notes:*** 1. OC# pins are not 5 V tolerant. 2. OC# pins must be shared between ports 3. OC#[3:0] can only be used for EHCI controller #1 4. OC#[4:7] can only be used for EHCI controller #2
USBRBIAS	O	**USB Resistor Bias:** Analog connection point for an external resistor. Used to set transmit currents and internal load resistors.
USBRBIAS#	I	**USB Resistor Bias Complement:** Analog connection point for an external resistor. Used to set transmit currents and internal load resistors.

2.10 Power Management Interface

Table 2-10. Power Management Interface Signals (Sheet 1 of 3)

Name	Type	Description
APWROK	I	**Active Sleep Well (ASW) Power OK:** When asserted, indicates that power to the ASW sub-system is stable.
BMBUSY# / GPIO0	I	**Bus Master Busy:** Generic bus master activity indication driven into the PCH. Can be configured to set the PM1_STS.BM_STS bit. Can also be configured to assert indications transmitted from the PCH to the Processor using the PM_SYNC pin.
DPWROK	I	**DPWROK:** Power OK Indication for the VccDSW3_3 voltage rail. This input is tied together with RSMRST# on platforms that do not support DeepSx. This signal is in the RTC well.
DRAMPWROK	OD O	**DRAM Power OK:** This signal should connect to the Processor's SM_DRAMPWROK pin. The PCH asserts this pin to indicate when DRAM power is stable. This pin requires an external pull-up.
LAN_PHY_PWR_CTRL / GPIO12	O	**LAN PHY Power Control:** LAN_PHY_PWR_CTRL should be connected to LAN_DISABLE_N on the PHY. The PCH will drive LAN_PHY_PWR_CTRL low to put the PHY into a low power state when functionality is not needed. ***Note:*** LAN_PHY_PWR_CTRL can only be driven low if SLP_LAN# is deasserted. Signal can instead be used as GPIO12.

Table 2-10. Power Management Interface Signals (Sheet 2 of 3)

Name	Type	Description
PLTRST#	O	**Platform Reset:** The PCH asserts PLTRST# to reset devices on the platform (for example, SIO, FWH, LAN, Processor, and so on). The PCH asserts PLTRST# during power-up and when software initiates a hard reset sequence through the Reset Control register (I/O Register CF9h). The PCH drives PLTRST# active a minimum of 1 ms when initiated through the Reset Control register (I/O Register CF9h). ***Note:*** PLTRST# is in the VccSus3_3 well.
PWRBTN#	I	**Power Button:** The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S1–S4 states. This signal has an internal pull-up resistor and has an internal 16 ms de-bounce on the input. This signal is in the DSW well.
PCH_PWROK	I	**Power OK:** When asserted, PCH_PWROK is an indication to the PCH that all of its core powerrails have been stable for at least 10 ms. PCH_PWROK can be driven asynchronously. When PCH_PWROK is negated, the PCH asserts PLTRST#. ***Note:*** It is required that the powerrails associated with PCI/PCIe* (typically the 3.3 V, 5 V, and 12 V core well rails) have been valid for 99 ms prior to PCH_PWROK assertion in order to comply with the 100 ms PCI 2.3/ PCIe 1.1 specification on PLTRST# deassertion. PCH_PWROK must not glitch, even if RSMRST# is low.
RI#	I	**Ring Indicate:** This signal is an input from a modem. It can be enabled as a wake event, and this is preserved across power failures.
RSMRST#	I	**Resume Well Reset:** This signal is used for resetting the resume power plane logic. This signal must remain asserted for at least 10 ms after the suspend power wells are valid. When deasserted, this signal is an indication that the suspend power wells are stable.
SLP_A#	O	**SLP_A#:** Used to control power to the active sleep well (ASW) of the PCH.
SLP_LAN# / GPIO29	O	**LAN Sub-System Sleep Control:** When SLP_LAN# is deasserted it indicates that the PHY device must be powered. When SLP_LAN# is asserted, power can be shut off to the PHY device. SLP_LAN# will always be deasserted in S0 and anytime SLP_A# is deasserted. A SLP_LAN#/GPIO Select Soft-Strap can be used for systems NOT using SLP_LAN# functionality to revert to GPIO29 usage. When soft-strap is 0 (default), pin function will be SLP_LAN#. When soft-strap is set to 1, the pin returns to its regular GPIO mode. The pin behavior is summarized in Section 5.14.9.4
SLP_S3#	O	**S3 Sleep Control:** SLP_S3# is for power plane control. This signal shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S4#	O	**S4 Sleep Control:** Power plane control. Shuts power to non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state. This pin must be used to control the DRAM power in order to use the PCH's DRAM power-cycling feature. ***Note:*** This pin must be used to control the DRAM power in order to use the PCH's DRAM power-cycling feature. Refer to Section 5.14.9.2 for details
SLP_S5# / GPIO63	O	**S5 Sleep Control:** SLP_S5# is for power plane control. This signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states. Pin may also be used as GPIO63.
SLP_SUS#	O	**Deep Sleep Indication:** When asserted low, this signal indicates PCH is in deep sleep state where internal Sus power is shut off for enhanced power saving. If DeepSx is not supported, then this pin can be left unconnected. This pin is in the DSW power well.
SUSACK#	I	**SUSACK#:** If DeepSx is supported, the EC must change SUSACK# to match SUSWARN# once the EC has completed the preparations discussed in the description for the SUSWARN# pin. ***Note:*** SUSWARN# must only change in response to SUSACK# if DeepSx is supported by the platform. This pin is in the Sus power well.

Table 2-10. Power Management Interface Signals (Sheet 3 of 3)

Name	Type	Description
SUSCLK /GPIO62	O	**Suspend Clock:** This clock is an output of the RTC generator circuit to use by other chips for refresh clock. Pin may also be used as GPIO62.
SUSWARN# GPIO30 /	O	**SUSWARN#:** This pin asserts low when the PCH is planning to enter the DeepSx power state and remove Suspend power (using SLP_SUS#). The EC must observe edges on this pin, preparing for SUS well power loss on a falling edge and preparing for SUS well related activity (host/Intel ME wakes and runtime events) on a rising edge. SUSACK# should be asserted within a minimal amount of time from SUSWARN# assertion, as no wake events are supported if SUSWARN# is asserted, but SUSACK# is not asserted. Platforms supporting Deep S4/S5, but not wishing to participate in the handshake during wake and Deep S4/S5 entry may tie SUSACK# to SUSWARN#. This pin may be muxed with a GPIO for use in systems that do not support Deep S4/S5. Reset type: RSMRST# This signal is muxed with GPIO30
SYS_PWROK	I	**System Power OK:** This generic power good input to the PCH is driven and utilized in a platform-specific manner. While PCH_PWROK always indicates that the CORE well of the PCH is stable, SYS_PWROK is used to inform the PCH that power is stable to some other system component(s) and the system is ready to start the exit from reset. ***Note:*** Consult the Platform Design Guide for instructions on how to connect SYS_PWROK for that platform.
SYS_RESET#	I	**System Reset**: This pin forces an internal reset after being debounced. The PCH will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms ± 2 ms for the SMBus to idle before forcing a reset on the system.
WAKE#	I	**PCI Express* Wake Event:** Sideband wake signal on PCI Express asserted by components requesting wake up.
ADR_COMPLETE	O	This pin is not used for High-End Desktop (HEDT) designs.

2.11 Processor Interface

Table 2-11. Processor Interface Signals

Name	Type	Description
RCIN#	I	**Keyboard Controller Reset CPU:** The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the PCH's other sources of INIT#. When the PCH detects the assertion of this signal, INIT# is generated for 16 PCI clocks. ***Note:*** The PCH will ignore RCIN# assertion during transitions to the S3, S4, and S5 states.
A20GATE	I	**A20 Gate:** A20GATE is from the keyboard controller. The signal acts as an alternative method to force the A20M# signal active. It saves the external OR gate needed with various other copyists.
PROCPWRGD	O	**Processor Power Good:** This signal should be connected to the processor's PWRGOOD input to indicate when the processor power is valid.
PM_SYNC	O	**Power Management Sync:** Provides state information from the PCH to the processor relevant to C-state transitions.
PM_SYNC2	O	**Power Management Sync 2:** Provides state information from the PCH to the processor relevant to C-state transitions. Not used for HEDT.
THRMTRIP#	I	**Thermal Trip**: When low, this signal indicates that a thermal trip from the processor occurred, and the PCH will immediately transition to a S5 state. The PCH will not wait for the processor stop grant cycle since the processor has overheated.

2.12 SMBus Interface

Table 2-12. SM Bus Interface Signals

Name	Type	Description
SMBDATA	I/OD	**SMBus Data:** External pull-up resistor is required.
SMBCLK	I/OD	**SMBus Clock:** External pull-up resistor is required.
SMBALERT# / GPIO11	I	**SMBus Alert:** This signal is used to wake the system or generate SMI#. This signal may be used as GPIO11.

2.13 System Management Interface

Table 2-13. System Management Interface Signals

Name	Type	Description
INTRUDER#	I	**Intruder Detect:** This signal can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPI if the Intruder Detection is not needed.
SML0DATA	I/OD	**System Management Link 0 Data:** SMBus link to external PHY. External pull-up is required.
SML0CLK	I/OD	**System Management Link 0 Clock:** SMBus link to external PHY. External pull-up is required.
SML0ALERT# / GPIO60	O OD	**SMLink Alert 0:** Output of the integrated LAN controller to external PHY. External pull-up resistor is required. This signal can instead be used as a GPIO60.
SML1ALERT# / PCHHOT#/GPIO74	O OD	PCHHOT#: This signal is used to indicate a PCH temperature out of bounds condition to an external EC, when PCH temperature is greater than value programmed by BIOS. An external pull-up resistor is required on this signal. ***Note:*** A soft-strap determines the native function SML1ALERT# or PCHHOT# usage. When soft-strap is 0, function is SML1ALERT#, when soft-strap is 1, function is PCHHOT#.
SML1CLK / GPIO58	I/OD	**System Management Link 1 Clock:** SMBus link to optional Embedded Controller or BMC. External pull-up resistor is required.
SML1DATA / GPIO75	I/OD	**System Management Link 1 Data:** SMBus link to optional Embedded Controller or BMC. External pull-up resistor is required.

2.14 SAS System Management Interface

Note: These signals are not used on the PCH. They are reserved for future use.

Table 2-14. SAS System Management Interface Signals

Name	Type	Description
SASSMBDATA0	I/O	Reserved for future use. ***Note:*** This signal should be a no connect.
SASSMBCLK0	O	Reserved for future use. ***Note:*** This signal should be a no connect.
SASSMBDATA1	I/O	Reserved for future use. ***Note:*** This signal should be a no connect.
SASSMBCL0K1	O	Reserved for future use. ***Note:*** This signal should be a no connect.
SASSMBDATA2	I/O	Reserved for future use. ***Note:*** This signal should be a no connect.
SASSMBCLK2	O	Reserved for future use. ***Note:*** This signal should be a no connect.

2.15 Real Time Clock Interface

Table 2-15. Real Time Clock Interface

Name	Type	Description
RTCX1	Special	**Crystal Input 1:** This signal is connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX1 can be driven with the desired clock rate.
RTCX2	Special	**Crystal Input 2:** This signal is connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX2 should be left floating.

2.16 Miscellaneous Signals

Table 2-16. Miscellaneous Signals

Name	Type	Description
INTVRMEN	I	**Internal Voltage Regulator Enable:** This signal enables the internal 1.5 V regulators. This signal must be always pulled-up to VccRTC. ***Note:*** See VccCore signal description for behavior when INTVRMEN is sampled low (external VR mode).
DSWODVREN	I	**Deep Sleep Well Internal Voltage Regulator Enable:** This signal enables the internal Deep Sleep 1.1 V regulators. This signal must be always pulled-up to VccRTC.
SPKR	O	**Speaker:** The SPKR signal is the output of counter 2 and is internally "ANDed" with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon PLTRST#, its output state is 0. ***Note:*** SPKR is sampled as a functional strap. See Section 2.26.1 for more details. There is a weak integrated pull-down resistor on SPKR pin.
RTCRST#	I	**RTC Reset:** When asserted, this signal resets register bits in the RTC well. ***Notes:*** 1. Unless CMOS is being cleared (only to be done in the G3 power state), the RTCRST# input must always be high when all other RTC power planes are on. 2. In the case where the RTC battery is dead or missing on the platform, the RTCRST# pin must rise before the RSMRST# pin.
SRTCRST#	I	**Secondary RTC Reset:** This signal resets the manageability register bits in the RTC well when the RTC battery is removed. ***Notes:*** 1. The SRTCRST# input must always be high when all other RTC power planes are on. 2. In the case where the RTC battery is dead or missing on the platform, the SRTCRST# pin must rise before the RSMRST# pin.
SML1ALERT# / PCHHOT# / GPIO74	OD	PCHHOT#: This signal is used to indicate a PCH temperature out of bounds condition to an external EC, when PCH temperature is greater than value programmed by BIOS. An external pull-up resistor is required on this signal. ***Note:*** A soft-strap determines the native function SML1ALERT# or PCHHOT# usage. When soft-strap is 0, function is SML1ALERT#, when soft-strap is 1, function is PCHHOT#.
INIT3_3V#	O	**Initialization 3.3 V:** INIT3_3V# is asserted by the PCH for 16 PCI clocks to reset the processor. This signal is intended for Firmware Hub.
NMI#/ GPIO35	O	**Non-Maskable Interrupt:** NMI# is used to force a non-Maskable interrupt to the processor. ***Note:*** The NMI # function is enabled using softstrap.
SMI# / GPIO20	O	**System Management Interrupt:** SMI# is an active low output synchronous to PCICLK. It is asserted by the PCH in response to one of many enabled hardware or software events. ***Note:*** The SMI# function is enabled using softstrap.

2.17 Intel® High Definition Audio (Intel® HD Audio) Link

Table 2-17. Intel® High Definition Audio (Intel® HD Audio) Link Signals

Name	Type	Description
HDA_RST#	O	**Intel HD Audio Reset:** Master hardware reset to external codec(s).
HDA_SYNC	O	**Intel HD Audio Sync:** 48 kHz fixed rate sample sync to the codec(s). Also used to encode the stream number. ***Note:*** This signal is sampled as a functional strap. See Section 2.26.1 for more details. There is a weak integrated pull-down resistor on this pin.
HDA_BCLK	O	**Intel HD Audio Bit Clock Output:** 24.000 MHz serial data clock generated by the Intel High Definition Audio controller (the PCH). This signal has a weak internal pull-down resistor.
HDA_SDO	O	**Intel HD Audio Serial Data Out:** Serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel High Definition Audio. ***Note:*** This signal is sampled as a functional strap. See Section 2.26.1 for more details. There is a weak integrated pull-down resistor on this pin.
HDA_SDIN[3:0]	I	**Intel HD Audio Serial Data In [3:0]**: Serial TDM data inputs from the codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel High Definition Audio. These signals have integrated pull-down resistors, which are always enabled. ***Note:*** During enumeration, the PCH will drive this signal. During normal operation, the CODEC will drive it.

2.18 Serial Peripheral Interface (SPI)

Table 2-18. Serial Peripheral Interface (SPI) Signals

Name	Type	Description
SPI_CS0#	O	**SPI Chip Select 0**: Used as the SPI bus request signal.
SPI_CS1#	O	**SPI Chip Select 1**: Used as the SPI bus request signal.
SPI_MISO	I	**SPI Master IN Slave OUT**: Data input pin for PCH.
SPI_MOSI	I/O	**SPI Master OUT Slave IN**: Data output pin for PCH.
SPI_CLK	O	**SPI Clock**: SPI clock signal, during idle the bus owner will drive the clock signal low. 17.86 MHz and 31.25 MHz.

2.19 Thermal Signals

Table 2-19. Thermal Signals

Signal Name	Type	Description
PWM[3:0]	OD O	**Fan Pulse Width Modulation Outputs:** Pulse Width Modulated duty cycle output signal that is used for Intel® Quiet System Technology (Intel® QST). When controlling a 3-wire fan, this signal controls a power transistor that, in turn, controls power to the fan. When controlling a 4-wire fan, this signal is connected to the "Control" signal on the fan. The polarity of this signal is programmable. The output default is low. These signals are 5 V tolerant.
TACH0 / GPIO17 **TACH1** / GPIO1 **TACH2** / GPIO6 **TACH3** / GPIO7 **TACH4** / GPIO68 **TACH5** / GPIO69 **TACH6** / GPIO70 **TACH7** / GPIO71	I	**Fan Tachometer Inputs:** Tachometer pulse input signal that is used to measure fan speed. This signal is connected to the "Sense" signal on the fan. Can instead be used as a GPIO.
SST	I/O	**Simple Serial Transport:** Single-wire, serial bus. This signal connect to SST compliant devices such as SST thermal sensors or voltage sensors.
PECI	I/O	**Platform Environment Control Interface:** Single-wire, serial bus. This signal connect to corresponding pin of the processor for accessing processor digital thermometer.

2.20 JTAG Signals

Table 2-20. JTAG Signals

Name	Type	Description
JTAG_TCK	I	**Test Clock Input (TCK):** The test clock input provides the clock for the JTAG test logic.
JTAG_TMS	I	**Test Mode Select (TMS):** The signal is decoded by the Test Access Port (TAP) controller to control test operations.
JTAG_TDI	I	**Test Data Input (TDI):** Serial test instructions and data are received by the test logic at TDI.
JTAG_TDO	OD	**Test Data Output (TDO):** TDO is the serial output for test instructions and data from the test logic defined in this standard.

Note: JTAG Pin definitions are from IEEE Standard Test Access Port and Boundary-Scan Architecture (IEEE Std. 1149.1-2001)

2.21 Clock Signals

Table 2-21. Clock Interface Signals

Name	Type	Description
CLKIN_DMI_P, CLKIN_DMI_N	I	100 MHz differential reference clock from CK505 and used by DMI.
CLKIN_SATA_P, CLKIN_SATA_N	I	100 MHz differential reference clock from CK505, provided separately from CLKIN_DMI, for use only as a 100 MHz source for SATA.
CLKIN_DOT96P, CLKIN_DOT96N	I	96 MHz differential reference clock from CK505.
REFCLK14IN	I	Single-ended 14.31818 MHz reference clock driven by CK505. Used for 8254 Timer, ACPI Timer and HPET.
CLKIN_SAS0_P, CLKIN_SAS0_N	I	100 MHz differential reference clock from CK505. Reserved for future use. ***Note:*** These signals must be tied to 100 MHz differential reference clock.
CLKIN_SAS1_P, CLKIN_SAS1_N	I	100 MHz differential reference clock from CK505. Reserved for future use. ***Note:*** These signals should be no connects.
CLKIN_SPCIE0_P, CLKIN_SPCIE0_N	I	Reserved for future use. ***Note:*** These signals should be no connects.
CLKIN_PCI	I	**PCI Clock**: This is a 33 MHz clock feedback input to reduce skew between PCH PCI clock and clock observed by connected PCI devices.

2.22 General Purpose I/O Signals

1. GPIO Configuration registers within the Core Well are reset whenever PCH_PWROK is deasserted.
2. GPIO Configuration registers within the Suspend Well are reset when RSMRST# is asserted, CF9h reset (06h or 0Eh) event occurs, or SYS_RESET# is asserted. However, CF9h reset and SYS_RESET# events can be masked from resetting the Suspend well GPIO by programming appropriate GPIO Reset Select (GPIO_RST_SEL) registers.
3. GPIO24 is an exception to the other GPIO Signals in the Suspend Well and is not reset by CF9h reset (06h or 0Eh).

Table 2-22. General Purpose I/O Signals (Sheet 1 of 3)

Name	Type	Tolerance	Power Well	Default	Blink Capability	Description
GPIO75	I/O	3.3 V	Suspend	Native	No	Multiplexed with SML1DATA (Note 10)
GPIO74	I/O	3.3 V	Suspend	Native	No	Multiplexed with SML1ALERT#/ PCHHOT# (Note 10)
GPIO73	I/O	3.3 V	Suspend	GPI	No	Unmultiplexed
GPIO72	I/O	3.3 V	Suspend	Native	No	Unmultiplexed (note 4) This signal must not be low prior to ASW well being valid; Requires pull-up resistor.
GPIO71	I/O	3.3 V	Core	Native	No	Multiplexed with Tach7
GPIO70	I/O	3.3 V	Core	Native	No	Multiplexed with Tach6
GPIO69	I/O	3.3 V	Core	GPI	No	Multiplexed with Tach5
GPIO68	I/O	3.3 V	Core	GPI	No	Multiplexed with Tach4

Table 2-22. General Purpose I/O Signals (Sheet 2 of 3)

Name	Type	Tolerance	Power Well	Default	Blink Capability	Description
GPIO67	I/O	3.3 V	Core	GPO	No	Unmultiplexed
GPIO66	I/O	3.3 V	Core	GPO	No	Unmultiplexed
GPIO65	I/O	3.3 V	Core	GPO	No	Unmultiplexed
GPIO64	I/O	3.3 V	Core	GPO	No	Unmultiplexed
GPIO63	I/O	3.3 V	Suspend	Native	No	Multiplexed with SLP_S5#
GPIO62	I/O	3.3 V	Suspend	Native	No	Multiplexed with SUSCLK
GPIO61	I/O	3.3 V	Suspend	GPO	No	Unmultiplexed (note 4)
GPIO60	I/O	3.3 V	Suspend	Native	No	Multiplexed with SML0ALERT#
GPIO59	I/O	3.3 V	Suspend	Native	No	Multiplexed with OC0# (Note 10)
GPIO58	I/O	3.3 V	Suspend	Native	No	Multiplexed with SML1CLK
GPIO57	I/O	3.3 V	Suspend	GPI	No	Unmultiplexed
GPIO56	I/O	3.3 V	Suspend	GPI	No	Unmultiplexed
GPIO55	I/O	3.3 V	Core	Native	No	Multiplexed with GNT3#
GPIO54	I/O	5.0 V	Core	Native	No	Multiplexed with REQ3#/ GSXRESET#.(Note 10)
GPIO53	I/O	3.3 V	Core	Native	No	Multiplexed with GNT2#/GSXDIN
GPIO52	I/O	5.0 V	Core	Native	No	Multiplexed with REQ2#/GSXSLOAD. (Note 10)
GPIO51	I/O	3.3 V	Core	Native	No	Multiplexed with GNT1#/GSXDOUT
GPIO50	I/O	5.0 V	Core	Native	No	Multiplexed with REQ1#/GSXCLK. (Note 10)
GPIO49	I/O	3.3 V	Core	GPI	No	Multiplexed with SATA5GP and TEMP_ALERT#
GPIO48	I/O	3.3 V	Core	GPI	No	Multiplexed with SDATAOUT1.
GPIO47	I/O	3.3 V	Suspend	GPI	No	Unmultiplexed
GPIO46	I/O	3.3 V	Suspend	GPI	No	Unmultiplexed
GPIO45	I/O	3.3 V	Suspend	GPI	No	Unmultiplexed
GPIO44	I/O	3.3 V	Suspend	GPI	No	Unmultiplexed
GPIO[43:40]	I/O	3.3 V	Suspend	Native	No	Multiplexed with OC[4:1]#. (Note 10)
GPIO39	I/O	3.3 V	Core	GPI	No	Multiplexed with SDATAOUT0.
GPIO38	I/O	3.3 V	Core	GPI	No	Multiplexed with SLOAD.
GPIO37	I/O	3.3 V	Core	GPI	No	Multiplexed with SATA3GP.
GPIO36	I/O	3.3 V	Core	GPI	No	Multiplexed with SATA2GP.
GPIO35	I/O	3.3 V	Core	GPO	No	Multiplexed with NMI#.
GPIO34	I/O	3.3 V	Core	GPI	No	Unmultiplexed (Note 4)
GPIO33	I/O	3.3 V	Core	GPO	No	Unmultiplexed (Note 4)
GPIO32	I/O	3.3 V	Core	GPO	No	Unmultiplexed (Note 4)
GPIO31	I/O	3.3 V	DSW	GPI	Yes	Unmultiplexed (Note 4)
GPIO30	I/O	3.3 V	Suspend	Native	Yes	Multiplexed with SUSWARN#. Can be used as SUSWARN# and GPIO30 only.
GPIO29	I/O	3.3 V	Suspend	GPI	No	Multiplexed with SLP_LAN# (Note 9)

Table 2-22. General Purpose I/O Signals (Sheet 3 of 3)

Name	Type	Tolerance	Power Well	Default	Blink Capability	Description
GPIO28	I/O	3.3 V	Suspend	GPO	Yes	Unmultiplexed
GPIO27	I/O	3.3 V	DSW	GPI	Yes	Unmultiplexed Can be configured as wake input to allow wakes from Deep S4/S5.
GPIO26	I/O	3.3 V	Suspend	GPO	Yes	Unmultiplexed
GPIO25	I/O	3.3 V	Suspend	GPO	Yes	Unmultiplexed
GPIO24	I/O	3.3 V	Suspend	GPO	Yes	Unmultiplexed ***Note:*** GPIO24 configuration register bits are not cleared by CF9h reset event.
GPIO23	I/O	3.3 V	Core	Native	Yes	Multiplexed with LDRQ1#.
GPIO22	I/O	3.3 V	Core	GPI	Yes	Multiplexed with SCLOCK
GPIO21	I/O	3.3 V	Core	GPI	Yes	Multiplexed with SATA0GP
GPIO20	I/O	3.3 V	Core	GPO	Yes	Multiplexed with SMI#
GPIO19	I/O	3.3 V	Core	GPI	Yes	Multiplexed with SATA1GP
GPIO18	I/O	3.3 V	Core	GPO	Yes (Note 6)	Unmultiplexed
GPIO17	I/O	3.3 V	Core	GPI	Yes	Multiplexed with TACH0.
GPIO16	I/O	3.3 V	Core	GPI	Yes	Multiplexed with SATA4GP.
GPIO15	I/O	3.3 V	Suspend	GPO	Yes	Unmultiplexed
GPIO14	I/O	3.3 V	Suspend	Native	Yes	Multiplexed with OC7#
GPIO13	I/O	3.3 V or 1.5 V	Suspend	GPI	Yes	Unmultiplexed (Note 4) ***Note:*** GPIO13 is powered by VccSusHDA (either 3.3 V or 1.5 V). Voltage tolerance on the signal is the same as VccSusHDA.
GPIO12	I/O	3.3 V	Suspend	Native	Yes	Multiplexed with LAN_PHY_PWR_CTRL. GPIO / Native functionality controlled using soft strap (Note 7)
GPIO11	I/O	3.3 V	Suspend	Native	Yes	Multiplexed with SMBALERT#. (Note 10)
GPIO10	I/O	3.3 V	Suspend	Native	Yes	Multiplexed with OC6# (Note 10)
GPIO9	I/O	3.3 V	Suspend	Native	Yes	Multiplexed with OC5# (Note 10)
GPIO8	I/O	3.3 V	Suspend	GPO	Yes	Unmultiplexed
GPIO[7:6]	I/O	3.3 V	Core	GPI	Yes	Multiplexed with TACH[3:2].
GPIO[5:2]	I/OD	5 V	Core	GPI	Yes	Multiplexed with PIRQ[H:E]# (Note 5).
GPIO1	I/O	3.3 V	Core	GPI	Yes	Multiplexed with TACH1.
GPIO0	I/O	3.3 V	Core	GPI	Yes	Multiplexed with BMBUSY#

Notes:

1. All GPIOs can be configured as either input or output.
2. GPI[15:0] can be configured to cause a SMI# or SCI. A GPI can be routed to either an SMI# or an SCI, but not both.
3. Some GPIOs exist in the VccSus3_3 power plane. Care must be taken to make sure GPIO signals are not driven high into powered-down planes. Also, external devices should not be driving powered down GPIOs high. Some GPIOs may be connected to pins on devices that exist in the core well. If these GPIOs are outputs, there is a danger that a loss of core power (PCH_PWROK low) or a Power Button Override event will result in the PCH driving a pin to a logic 1 to another device that is powered down.
4. The functionality that is multiplexed with the GPIO is not utilized in the PCH.
5. When this signal is configured as GPO the output stage is an open drain.

6. GPIO18 will toggle at a frequency of approximately 1 Hz when the signal is programmed as a GPIO (when configured as an output) by BIOS.
7. For GPIOs where GPIO versus Native Mode is configured using SPI Soft Strap, the corresponding GPIO_USE_SEL bits for these GPIOs have no effect. The GPIO_USE_SEL bits for these GPIOs may change to reflect the Soft-Strap configuration even though GPIO Lockdown Enable (GLE) bit is set.
8. These pins are used as Functional straps. See Section 2.26.1 for more details.
9. Once Soft-strap is set to GPIO mode, this pin will default to GP Input. When Soft-strap is SLP_LAN# usage and if Host BIOS does not configure as GP Output for SLP_LAN# control, SLP_LAN# behavior will be based on the setting of the RTC backed SLP_LAN# Default Bit(D31:F0:A4h:Bit 8).
10. When the multiplexed GPIO is used as GPIO functionality, care should be taken to ensure the signal is stable in its inactive state of the native functionality, immediately after reset until it is initialized to GPIO functionality.

2.23 GPIO Serial Expander Signals

Table 2-23. GPIO Serial Expander Interface

Name	Type	Description
GSXCLK	O	GPIO Serial Expansion clock input. GSXCLK may optionally be used as REQ1# or GPIO50
GSXSLOAD	O	GPIO Serial Expansion data load select. GSXSLOAD may optionally be used as REQ2# or GPIO52
GSXSRESET#	O	GPIO Serial Expansion reset. GSXSRESET# may optionally be used as REQ3# or GPIO54
GSXDOUT	O	GPIO Serial Expansion serial data out. GSXDOUT may optionally be used as GNT1# or GPIO51
GSXDIN	I	GPIO Serial Expansion serial data in. GSXDIN may optionally be used as GNT2# or GPIO53

Note: GSX (GPIO Serial Expander) signal functions are enabled using softstrap.

2.24 Manageability Signals

The following signals can be optionally used by PCH Intel ME supported applications and appropriately configured by Intel ME firmware. When configured and used as a Manageability function, the associated host GPIO functionality is no longer available. If the Manageability function is not utilized in a platform, the signal can be used as a host General Purpose I/O or a native function.

Table 2-24. Manageability Signals

Name	Type	Description
MGPIO0/ PROC_MISSING/ GPIO24	I/O	MGPIO0 can be used to connect to upgrade ROM. It is also used to indicate Processor Missing to the Intel® Management Engine (Intel® ME). ***Note:*** This signal is in the Suspend power well.
MGPIO1/GPIO30	I/O	MGPIO1 can be used as an alternative for MGPIO2 or MGPIO5 when neither pins are available for Intel ME. ***Note:*** This signal is in the Suspend power well.
MGPIO2 / GPIO31	I/O	MGPIO2 can be used as a SMBALERT# signal from PSU to PCH ***Note:*** This signal is in the Suspend power well.
MGPIO3 / SLP_LAN# / GPIO29	I/O	Intel ME General Purpose I/O 3. ***Note:*** This signal is in the Suspend power well.
MGPIO4 / SML0ALERT# / GPIO60	I/O	MGPIO4 can be used as an alternative for MGPIO2 or MGPIO5 when neither pins are available for Intel ME. ***Note:*** This signal is in the Suspend power well.
MGPIO5 / GPIO57	I/O	MGPIO5 can be used as Intel ME firmware recovery mode strap. MGPIO5 can be used as an alternative for MGPIO2 when it is not available for Intel ME. ***Note:*** This signal is in the Suspend power well.
MGPIO6 / GPIO27	I/O	MGPIO6 can be used as an alternative for MGPIO2 or MGPIO5 when neither pins are available for Intel ME. ***Note:*** This signal is in the Deep S4/S5(DSW) power well.
MGPIO7 / GPIO28	I/O	MGPIO7 can be used as an alternative for MGPIO2 or MGPIO5 when neither pins are available for Intel ME. ***Note:*** This signal is in the Suspend power well.
MGPIO8 / SML1ALERT# / GPIO74	I/O	MGPIO8 can be used as an alternative for MGPIO2 or MGPIO5 when neither pins are available for Intel ME. ***Note:*** This signal is in the Suspend power well.
MGPIO9 / SATA4GP / GPIO16	I/O	Intel ME General Purpose I/O 9. ***Note:*** This signal is in the Core power well.
MGPIO10/ TEMP_ALERT/ SATA5GP / GPIO49	I/O	Used as an alert (active low) to indicate to the external controller (for example, EC or SIO) that temperatures are out of range for the PCH or Graphics/Memory Controller or the processor core. ***Note:*** This signal is in the Core power well.
MGPIO11 / SML1CLK / GPIO58	I/O	ME General Purpose I/O 11. ***Note:*** This signal is in the Suspend power well.
MGPIO12 / SML1DATA / GPIO75	I/O	ME General Purpose I/O 12. ***Note:*** This signal is in the Suspend power well.

Note: SLP_LAN#/GPIO29 may also be configured by Intel ME FW in Sx/Moff. Please refer to SLP_LAN#/ GPIO29 signal description for details.

2.25 Power and Ground Signals

Table 2-25. Power and Ground Signals (Sheet 1 of 2)

Name	Description
DcpRTC	**Decoupling:** This signal is for RTC decoupling only. This signal requires decoupling.
DcpSST	**Decoupling:** Internally generated 1.5 V powered off of Suspend Well. This signal requires decoupling. Decoupling is required even if this feature is not used.
DcpSus	1.1 V Suspend well supply that is supplied internally by Internal VRs.
DcpSusByp	Internally generated 1.1 V Deep S4/S5 well power. This rail should not be supplied externally. ***Note:*** No decoupling capacitors should be used on this rail.
V5REF	Reference for 5 V tolerance on core well inputs. This power may be shut off in S3, S4, S5 or G3 states.
V5REF_Sus	Reference for 5 V tolerance on suspend well inputs. This power is not expected to be shut off unless the system is unplugged.
VccCore	1.1 V supply for core well logic. This power may be shut off in S3, S4, S5 or G3 states. ***Note:*** In external VR mode (INTVRMEN sampled low), the voltage level of VccCore may be indeterminate while DcpSus (1.1 V Suspend Well Power) supply ramps and prior to PWROK assertion.
VccIO	1.1 V supply for core well I/O buffers. This power may be shut off in S3, S4, S5 or G3 states.
Vcc3_3	3.3 V supply for core well I/O buffers. This power may be shut off in S3, S4, S5 or G3 states.
VccASW	1.1 V supply for Active Sleep Well. This plane must be on in S0 and other times the Intel ME is used or integrated LAN is used.
VccDMI	Power supply for DMI. 1.0 to 1.1 V based on the processor VTT voltage. Please refer to the respective processor documentation to find the appropriate voltage level.
VccRTC	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well. This power is not expected to be shut off unless the RTC battery is removed or completely drained. ***Note:*** Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS in a PCH based platform can be done by using a jumper on RTCRST# or GPI.
VccSus3_3	3.3 V supply for suspend well I/O buffers. This power is not expected to be shut off unless the system is unplugged.
VccAUBG	3.3 V supply for suspend well USB reference. ***Note:*** This pin may require external filtering.
VccAUPLL	1.1 V supply for core well USB PLL. ***Notes:*** This pin may require external filtering.
VccSusHDA	Suspend supply for Intel HD Audio. This pin can be either 1.5 or 3.3 V.
VccVRM	1.5 V / 1.8 V supply for internal PLL and VRMs
VccDFTERM	1.8 V or 3.3 V supply for DF_TVS. Can be pulled up to 1.8 V or 3.3 V core.
VccAPLLSATA	1.1 V Analog power supply for SATA. This signal is used for the analog power for SATA. This requires an LC filter and is supplied by the core well. Must be powered even if SATA is not used. ***Note:*** This pin can be left as no connect in On-Die VR enabled mode (default).
VccAPLLEXP	1.1 V Analog Power for DMI. This power is supplied by the core well. This requires an LC filter. ***Note:*** This pin can be left as no connect in On-Die VR enabled mode (default).
VccAPLLDMI2	1.1 V Analog Power for internal PLL. This power is supplied by the core well. This requires an LC filter. ***Note:*** This pin can be left as no connect in On-Die VR enabled mode (default).
V_PROC_IO	Powered by the same supply as the processor I/O voltage. This supply is used to drive the processor interface signals. Please refer to the respective processor documentation to find the appropriate voltage level.

Table 2-25. Power and Ground Signals (Sheet 2 of 2)

Name	Description
VccDSW3_3	3.3 V supply for Deep Sleep wells. If platform does not support Deep S4/S5, then tie to VccSus3_3.
VccSPI	3.3 V supply for SPI controller logic. This must be powered when VccASW is powered. ***Note:*** This rail can be optionally powered on 3.3-V Suspend power (VccSus3_3) based on platform needs.
VccXUS	1.1 V supply Can be tied to Vss for SKUs not supporting PCI Express Uplink. Reserved for future use. ***Note:*** This signal can be tied to V_{SS} or V_{CC}, but must be tied to the same power plane as VccSCUS.
VccSCUS	1.1 V supply for SAS switch wells. Can be tied to Vss for SKUs not supporting SAS. Reserved for future use. ***Note:*** This signal can be tied to V_{SS} or V_{CC}, but must be tied to the same power plane as VccXUS.
VccPLLSAS0	1.1 V supply for x4 SAS port. This signal requires an LC filter and is supplied by the core well. Reserved for future use. This signal must be connected.
VccPLLSAS1	1.1 V supply for x4 SAS port. This signal requires an LC filter and is supplied by the core well. Reserved for future use. This signal must be connected.
VccPLLEXPU	1.1 V supply. This requires an LC filter and is supplied by the core well. Reserved for future use. ***Note:*** Must be tied to Vss if VccXUS is tied to Vss on PCH SKUs.
VccRBIAS_SAS0	1.1 V supply for x4 SAS port RBIAS. This is supplied by the core well. Reserved for future use. ***Note:*** This signal must be connected.
VccRBIAS_SAS1	1.1 V supply for x4 SAS port RBIAS. This is supplied by the core well. Reserved for future use. ***Note:*** This signal must be connected.
VccRBIAS_PU	1.1 V supply. This is signal is supplied by the core well. Reserved for future use. ***Note:*** This signal must be tied to Vss if VccXUS is tied to Vss on.
VccSAS1_5	1.5 V supply for x4 SAS port. This signal is supplied by the core well. Reserved for future use. ***Note:*** This signal must be connected.
Vss	Grounds.

2.26 Pin Straps

2.26.1 Functional Straps

The following signals are used for static configuration. They are sampled at the rising edge of PCH_PWROK to select configurations (except as noted), and then revert later to their normal usage. To invoke the associated mode, the signal should be driven at least four PCI clocks prior to the time it is sampled.

PCH has implemented Soft Straps. Soft Straps are used to configure specific functions within the PCH and processor very early in the boot process before BIOS or software intervention. When Descriptor Mode is enabled, the PCH will read Soft Strap data out of the SPI device prior to the de-assertion of reset to both the Intel ME and the Host system.

Table 2-26. Functional Strap Definitions (Sheet 1 of 3)

Signal	Usage	When Sampled	Comment
SPKR	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. ***Note:*** The internal pull-down is disabled after PLTRST# de-asserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). The status of this strap is readable using the NO REBOOT bit (Chipset Config Registers: Offset 3410h:bit 5).
INIT3_3V#	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-up. ***Note:*** The internal pull-up is disabled after PLTRST# de-asserts. ***Note:*** This signal should not be pulled low
GNT3#/GPIO55	Top-Block Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-up. If the signal is sampled low, this indicates that the system is strapped to the "top-block swap" mode. The status of this strap is readable using the Top Swap bit (Chipset Config Registers: Offset 3414h:Bit 0). **NOTES:** 1. The internal pull-up is disabled after PLTRST# deasserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted without GNT3#/GPIO55 being pulled down.
INTVRMEN	Integrated 1.1 V VRM Enable / Disable	Always	Integrated 1.1 V VRMs is enabled when high ***Note:*** This signal should always be pulled high.

Table 2-26. Functional Strap Definitions (Sheet 2 of 3)

Signal	Usage	When Sampled	Comment
GNT1#/GPIO51	Boot BIOS Strap bit [1] BBS[1]	Rising edge of PCH_PWROK	This Signal has a weak internal pull-up. ***Note:*** The internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. **Bit11 / Bit 10 / Boot BIOS Destination** 0 / 1 / Reserved 1 / 0 / PCI 1 / 1 / SPI 0 / 0 / LPC ***Note:*** If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. ***Note:*** Booting to PCI is intended for debut/ testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN.
SATA1GP/ GPIO19	Boot BIOS Strap bit[0] BBS[0]	Rising edge of PCH_PWROK	This Signal has a weak internal pull-up. ***Note:*** The internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. **Bit11 / Bit 10 / Boot BIOS Destination** 0 / 1 / Reserved 1 / 0 / PCI 1 / 1 / SPI 0 / 0 / LPC ***Note:*** If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. ***Note:*** Booting to PCI is intended for debut/ testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN.
GNT2#/ GPIO53	DMI AC Coupling	Rising edge of PCH_PWROK	This Signal has a weak internal pull-up. ***Note:*** The internal pull-up is disabled after PLTRST# de-asserts. Tying this strap low enables DMI full voltage AC coupling.

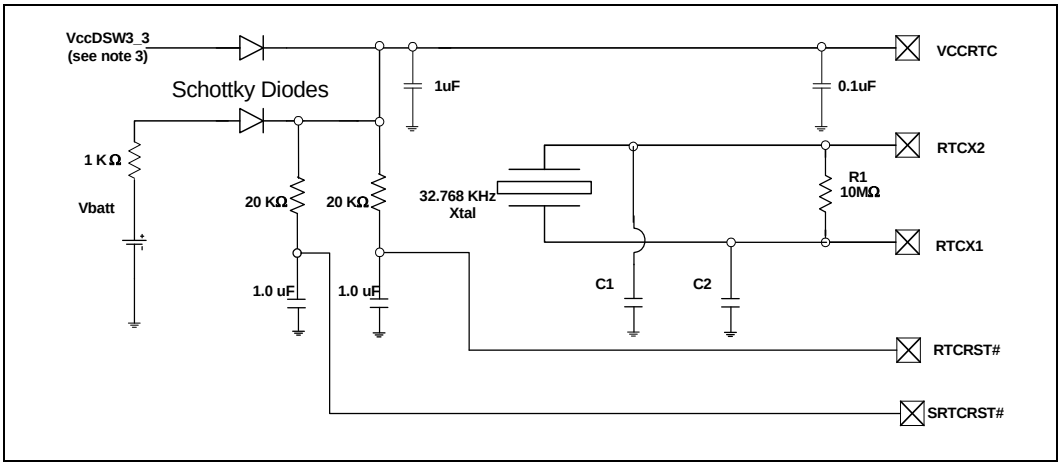
Table 2-26. Functional Strap Definitions (Sheet 3 of 3)

Signal	Usage	When Sampled	Comment
HDA_SDO	Flash Descriptor Security Override/ Intel ME Debug Mode	Rising edge of PCH_PWROK	Signal has a weak internal pull-down. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default). If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. ***Note:*** The weak internal pull-down is disabled after PLTRST# de-asserts. ***Note:*** Asserting the HDA_SDO high on the rising edge of PCH_PWROK will also halt Intel ME after chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug.
DF_TVS	DMI Tx /Rx Termination Voltage	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. ***Note:*** The internal pull-down is disabled after PLTRST# de-asserts.
GPIO28	On-Die PLL Voltage Regulator	Rising edge of RSMRST# pin	This signal has a weak internal pull-up. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled. ***Note:*** The internal pull-up is disabled after RSMRST# deasserts.
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V from VccVRM when sampled high, 1.8 V from VccVRM when sampled low.
GPIO15	TLS Confidentiality	Rising edge of RSMRST# pin	Low = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel ME Crypto TLS cipher suite with confidentiality This signal has a weak internal pull down. ***Notes:*** 1. A strong pull up may be needed for GPIO functionality. 2. This signal must be pulled up to support Intel RPAT with TLS. Intel ME configuration parameters also need to be set correctly to enable TLS.
DSWODVREN	Deep S4/S5 Well On-Die Voltage Regulator Enable	Always	If strap is sampled high, the integrated Deep S4/ S5 Well (DSW) On-Die VR mode is enabled.
SATA2GP/GPIO36	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. ***Note:*** The internal pull-down is disabled after PLTRST# de-asserts. ***Note:*** This signal should not be pulled high when strap is sampled.

2.26.2 External RTC Circuitry

The PCH implements an internal oscillator circuit that is sensitive to step voltage changes in VccRTC. Figure 2-2 shows an example schematic recommended to ensure correct operation of the PCH RTC.

Figure 2-2. Example External RTC Circuit



Notes:

1. The exact capacitor values for C1 and C2 must be based on the crystal maker recommendations.
2. Reference designators are arbitrarily assigned.
3. For platforms not supporting Deep S4/S5, the VccDSW3_3 pins will be connected to the VccSus3_3 pins.
4. Vbatt is voltage provided by the RTC battery (for example, coin cell).
5. VccRTC, RTCX1, RTCX2, RTCRST#, and SRTCRST# are PCH pins.
6. VccRTC powers PCH RTC well.
7. RTCX1 is the input to the internal oscillator.
8. RTCX2 is the amplified feedback for the external crystal.

§

3 PCH Pin States

3.1 Integrated Pull-Ups and Pull-Downs

Table 3-1. Integrated Pull-Up and Pull-Down Resistors

Signal	Resistor	Nominal	Notes
GPIO[67:64]	Pull-down	20K	1, 10
GPIO15	Pull-down	20K	3
HDA_SDIN[3:0]	Pull-down	20K	2
HDA_SYNC, HDA_SDO	Pull-down	20K	2, 5
GNT[3:1]#/GPIO[55,53,51],	Pull-up	20K	3, 6, 7
GPIO8	Pull-up	20K	3, 12
LAD[3:0]#	Pull-up	20K	3
LDRQ0#, LDRQ1# / GPIO23	Pull-up	20K	3
DF_TVS	Pull-down	20k	8
PME#	Pull-up	20K	3
INIT3_3V#	Pull-up	20K	3
PWRBTN#	Pull-up	20K	3
SPI_MOSI	Pull-down	20K	3
SPI_MISO	Pull-up	20K	3
SPKR	Pull-down	20K	3, 9
TACH[7:0]/GPIO[71:68,7,6,1,17]	Pull-up	20K	3 (only on TACH[7:0])
USB[13:0] [P,N]	Pull-down	20K	4
GPIO72	Pull-up	20K	3
GPIO27	Pull-up	20K	3, 14
JTAG_TDI, JTAG_TMS	Pull-up	20K	1, 11
JTAG_TCK	Pull-down	20K	1, 11
GPIO28	Pull-up	20K	3, 12
SATA[3:2]GP/GPIO[37:36]	Pull-down	20K	3, 9
GPIO31/MGPIO2	Pull-down	20K	3, 15
GPIO44	Pull-up	20K	1, 12
SST	Pull-down	10K	16
GPIO46	Pull-up	20K	1, 12
SATA1GP/GPIO19	Pull-up	20K	3, 9
SUSACK#	Pull-up	20K	3
PECI	Pull-down	350	17

Notes:
1. Simulation data shows that these resistor values can range from 10 kΩ to 40 kΩ.
2. Simulation data shows that these resistor values can range from 9 kΩ to 50 kΩ.
3. Simulation data shows that these resistor values can range from 15 kΩ to 40 kΩ.
4. Simulation data shows that these resistor values can range from 14.25 kΩ to 24.8 kΩ
5. The pull-up or pull-down on this signal is only enabled at boot/reset for strapping function.
6. The pull-up on this signal is not enabled when PCIRST# is high.
7. The pull-up on this signal is not enabled when PCH_PWROK is low.
8. Simulation data shows that these resistor values can range from 15 kΩ to 31 kΩ.

9. The Pull-up or pull down is not active when PLTRST# is NOT asserted.
10. The pull-down is enabled when PCH_PWROK is low.
11. External termination is also required on these signals for JTAG enabling.
12. Pull-up is disabled after RSMRST# is deasserted.
13. Not applicable for PCH.
14. Pull-up is enabled only in Deep-S4/5 state.
15. Pull-down is enabled only in Deep-S4/5 state.
16. When the interface is in BUS IDLE, the Internal Pull-down of 10K is enabled. In normal transmission, a 400 ohm pull down takes effect, the signal will be override to logic 1 with pull-up resistor (37 ohms) to VCC 1.5 V.
17. This is a 350-Ω normal pull-down, signal will be overridden to logic 1 with pull-up resistor (31 Ω) to VCC 1.1 V.

3.2 Output and I/O Signals Planes and States

Table 3.2 shows the power plane associated with the output and I/O signals, as well as the state at various times. Within the table, the following terms are used:

"High-Z"	Tri-state. PCH not driving the signal high or low.
"High"	PCH is driving the signal to a logic 1.
"Low"	PCH is driving the signal to a logic 0.
"Defined"	Driven to a level that is defined by the function or external pull-up/pull-down resistor (will be high or low).
"Undefined"	PCH is driving the signal, but the value is indeterminate.
"Running"	Clock is toggling or signal is transitioning because function not stopping.
"Off"	The power plane is off; PCH is not driving when configured as an output or sampling when configured as an input.
"Input"	PCH is sampling and signal state determined by external driver.

Note: Signal levels are the same in S4 and S5, except as noted.

PCH suspend well signal states are indeterminate and undefined and may glitch prior to RSMRST# deassertion. This does not apply to SLP_S3#, SLP_S4# and SLP_S5#. These signals are determinate and defined prior to RSMRST# deassertion.

PCH core well signal states are indeterminate and undefined and may glitch prior to PCH_PWROK assertion. This does not apply to THRMTRIP#. This signal is determinate and defined prior to PCH_PWROK assertion.

DSW indicates PCH Deep Sleep Well.This state provides a few wake events and critical context context to allow system to draw minimal power in S4 or S5 states.

ASW indicates PCH Active Sleep Well. This power well contains functionality associated with active usage models while the host system is in Sx.

Table 3-2. Power Plane and States for Output and I/O Signals (Sheet 1 of 4)

Signal Name	Power Plane	During Reset[2]	Immediately after Reset[2]	S0/S1	S3	S4/S5
PCI Express						
PET[8:1]p, PET[8:1]n	Core	Low	Low[4]	Defined	OFF	OFF
DMI						
DMI_TXP[3:0], DMI_TXN[3:0]	Core	Low	Low	Defined	Off	Off

Table 3-2. Power Plane and States for Output and I/O Signals (Sheet 2 of 4)

Signal Name	Power Plane	During Reset[2]	Immediately after Reset[2]	S0/S1	S3	S4/S5
PCI Bus						
AD[31:0]	Core	Low	Low	Low	Off	Off
C/BE[3:0]#	Core	Low	Low	Low	Off	Off
DEVSEL#	Core	High-Z	High-Z	High-Z	Off	Off
FRAME#	Core	High-Z	High-Z	High-Z	Off	Off
GNT0#[7], GNT[3:1]#[7]/ GPIO[55, 53, 51]	Core	High	High	High	Off	Off
IRDY#, TRDY#	Core	High-Z	High-Z	High-Z	Off	Off
PAR	Core	Low	Low	Low	Off	Off
PCIRST#	Suspend	Low	High	High	Low	Low
PERR#	Core	High-Z	High-Z	High-Z	Off	Off
PLOCK#	Core	High-Z	High-Z	High-Z	Off	Off
STOP#	Core	High-Z	High-Z	High-Z	Off	Off
LPC/FWH Interface						
LAD[3:0]	Core	High	High	High	Off	Off
LFRAME#	Core	High	High	High	Off	Off
INIT3_3V#[7]	Core	High	High	High	Off	Off
SATA Interface						
SATA[5:0]TXP, SATA[5:0]TXN	Core	High-Z	High-Z	Defined	Off	Off
SATALED#	Core	High-Z	High-Z	Defined	Off	Off
SATAICOMPO	Core	High	High	Defined	Off	Off
SCLOCK/GPIO22	Core	High-Z (Input)	High-Z (Input)	Defined	Off	Off
SLOAD/GPIO38	Core	High-Z (Input)	High-Z (Input)	Defined	Off	Off
SDATAOUT[1:0]/ GPIO[48,39]	Core	High-Z	High-Z	High-Z	Off	Off
SATA3RBIAS	Core	Terminated to Vss	Terminated to Vss	Terminated to Vss	Off	Off
SATA3ICOMPO	Core	High-Z	High-Z	High-Z	Off	Off
SATA3RCOMPO	Core	High-Z	High-Z	High-Z	Off	Off
Interrupts						
PIRQ[A:D]#,	Core	High-Z	High-Z	High-Z	Off	Off
PIRQ[H:E]# / GPIO[5:2]	Core	High-Z (Input)	High-Z (Input)	Defined	Off	Off
SERIRQ	Core	High-Z	High-Z	High-Z	Off	Off
USB Interface						
USB[13:0][P,N]	Suspend	Low	Low	Defined	Defined	Defined
USBRBIAS	Suspend	High-Z	High-Z	High	High	High
Power Management						
LAN_PHY_PWR_CTRL[10]/ GPIO12	Suspend	Low	Low	Defined	Defined	Defined
PLTRST#	Suspend	Low	High	High	Low	Low

Table 3-2. Power Plane and States for Output and I/O Signals (Sheet 3 of 4)

Signal Name	Power Plane	During Reset[2]	Immediately after Reset[2]	S0/S1	S3	S4/S5
SLP_A#[5]	Suspend	Low	High	High	Defined	Defined
SLP_S3#	Suspend	Low	High	High	Low	Low
SLP_S4#	Suspend	Low	High	High	High	Defined
SLP_S5#/GPIO63	Suspend	Low	High	High	High	Defined[2]
SUSCLK	Suspend	Low	Running			
DRAMPWROK	Suspend	Low	High-Z	High-Z	High-Z	Low
PM_SYNC	Core	Low	Low	Defined	Off	Off
PM_SYNC2	Core	Low	Low	Defined	Off	Off
SLP_LAN#/GPIO29[8] SLP_LAN# (using soft-strap) GPIO29 (using soft-strap)	Suspend	Low High-z	Low[8] High-z	High High-z	Defined High-z	Defined High-z
Processor Interface						
PROCPWRGD	Processor	Low	High	High	Off	Off
SMBus Interface						
SMBCLK, SMBDATA	Suspend	High-Z	High-Z	Defined	Defined	Defined
System Management Interface						
SML0ALERT# / GPIO60	Suspend	High-Z	High-Z[12]	Defined	Defined	Defined
SML0DATA	Suspend	High-Z	High-Z	Defined	Defined	Defined
SML0CLK	Suspend	High-Z	High-Z	Defined	Defined	Defined
GPIO58/SML1CLK	Suspend	High-Z	High-Z	Defined	Defined	Defined
SML1ALERT#/ PCH_HOT#/GPIO74	Suspend	High-Z	High-Z	Defined	Defined	Defined
SML1DATA/GPIO75	Suspend	High-Z	High-Z	Defined	Defined	Defined
Miscellaneous Signals						
SPKR[7]	Core	Low	Low	Defined	Off	Off
JTAG_TDO	Suspend	High-Z	High-Z	High-Z	High-Z	High-Z
Intel HD Audio Interface						
HDA_RST#	Suspend	Low	Low[3]	Defined	Low	Low
HDA_SDO[7]	Suspend	Low	Low	Defined	Low	Low
HDA_SYNC[7]	Suspend	Low	Low	Defined	Low	Low
HDA_BCLK[13]	Suspend	Low	Low	Low	Low	Low
UnMultiplexed GPIO Signals						
GPIO8	Suspend	High	High	Defined	Defined	Defined
GPIO15[7]	Suspend	Low	Low	Defined	Defined	Defined
GPIO24	Suspend	Low	Low	Defined	Defined	Defined
GPIO27 (Non-Deep S4/ S5 mode)	DSW	High-Z	High-Z	High-Z	High-Z	High-Z
GPIO27 (Deep S4/S5 mode)	DSW	High-Z	High-Z	High-Z	High-Z	High-Z
GPIO28[12]	Suspend	High	Low	Low	Low	Low

Table 3-2. Power Plane and States for Output and I/O Signals (Sheet 4 of 4)

Signal Name	Power Plane	During Reset[2]	Immediately after Reset[2]	S0/S1	S3	S4/S5
GPIO32	Core	High	High	Defined	Off	Off
GPIO57	Suspend	High-Z (Input)	High-Z (Input)	Defined	Defined	Defined
GPIO72[9]	Suspend	High	High	Defined	Defined	Defined
Multiplexed GPIO Signals used as GPIO only						
GPIO0	Core	High-Z (Input)	High-Z (Input)	Defined	Off	Off
GPIO13[9, 14]	Suspend	High-Z	High-Z	High-Z	High-Z	High-Z
GPIO20	Core	High-Z (Input)	High-Z (Input)	Defined	Off	Off
GPIO30[9]	Suspend	High-Z (Input)	High-Z (Input)	Defined	Defined	Defined
GPIO31[9] (Non Deep-S4/ S5 mode)	DSW	High-Z (Input)	High-Z (Input)	Defined	Defined	Defined
GPIO31[9] (Deep-S4/S5 mode)	DSW	High-Z (Input)	High-Z (Input)	Defined	Defined	Defined
GPIO33[9]	Core	High	High	High	Off	Off
GPIO34	Core	High-Z (Input)	High-Z (Input)	Defined	Off	Off
GPIO35/NMI#	Core	Low	Low	Defined	Off	Off
GPIO[46:44]	Suspend	High-Z (Input)	High-Z (Input)	Defined	Defined	Defined
GPIO61	Suspend	Low	High	High	Low	Low
SPI Interface						
SPI_CS0#	ASW	High[12]	High	Defined	Defined	Defined
SPI_CS1#	ASW	High[12]	High	Defined	Defined	Defined
SPI_MOSI	ASW	Low[12]	Low	Defined	Defined	Defined
SPI_CLK	ASW	Low[12]	Low	Running	Defined	Defined
Thermal Reporting						
PWM[3:0]	Core	Low	Low	Defined	Off	Off
SST	Suspend	Low	Low	Defined	Off	Off
PECI	Processor	Low	Low	Defined	Off	Off
SAS Interface						
SAS[3:0]TXN, SAS[3:0]TXP	CORE	High-Z	High-Z	Defined	Off	Off
SAS_CLOCK1	CORE	High-Z (Input)	High-Z (Input)	Defined	Off	Off
SAS_LOAD1	CORE	High-Z (Input)	High-Z (Input)	Defined	Off	Off
SAS_DATAIN1	CORE	High-Z (Input)	High-Z (Input)	Defined	Off	Off
SAS_DATAOUT1	CORE	High-Z	High-Z	High-Z	Off	Off
SAS_RBIASN0, SAS_RBIASP0	Core	Terminated to Vss	Terminated to Vss	Terminated to Vss	Off	Off

Notes:

1. The states of Core and processor signals are evaluated at the times During PLTRST# and Immediately after PLTRST#. The states of the Suspend signals are evaluated at the times During RSMRST# and Immediately after RSMRST#, with an exception to GPIO signals; refer to Section 2.23 for more details on GPIO state after reset. The states of the HDA signals are evaluated at the times During HDA_RST# and Immediately after HDA_RST#
2. SLP_S5# signals will be high in the S4 state and low in the S5 state.
3. Low until Intel HD Audio Controller Reset bit set (D27:F0:Offset HDBAR+08h:bit 0), at which time HDA_RST# will be High and HDA_BIT_CLK will be Running.
4. PETp/n[8:1] low until port is enabled by software.
5. The SLP_A# state will be determined by Intel ME Policies.
6. The state of signals in S3-5 will be defined by Intel ME Policies.

7. This signal is sampled as a functional strap during reset. Refer to Table 2-26, "Functional Strap Definitions" on page 70 for usage.
8. SLP_LAN# behavior after reset is dependent on value of SLP_LAN# default value bit. A soft-strap is used to select between SLP_LAN# and GPIO usage. When strap is set to 0 (default), pin is used as SLP_LAN#, when soft-strap is set to 1, pin is used as GPIO29.
9. Native functionality multiplexed with these GPIOs are not used in the PCH.
10. Native/GPIO functionality controlled using soft straps. Default to Native functionality until soft straps are loaded.
11. State of the pins depend on the source of VccASW power.
12. Pin is tri-stated prior to APWROK assertion during Reset.
13. When Controller Reset Bit of Global Control Register (D27:F0 Offset HDBAR 08h bit 0) gets set, this pin will start toggling.
14. GPIO13 is powered by VccSusHDA (either 3.3 V or 1.5 V). Voltage tolerance on the signal is the same as VccSusHDA.

3.3 Power Planes for Input Signals

Table 3-3 shows the power plane associated with each input signal, as well as what device drives the signal at various times. Valid states include:

High
Low
Static: Will be high or low, but will not change
Driven: Will be high or low, and is allowed to change
Running: For input clocks

PCH suspend well signal states are indeterminate and undefined and may glitch prior to RSMRST# deassertion. This does not apply to SLP_S3#, SLP_S4# and SLP_S5#. These signals are determinate and defined prior to RSMRST# deassertion.

PCH core well signal states are indeterminate and undefined and may glitch prior to PCH_PWROK assertion. This does not apply to FERR# and THRMTRIP#. These signals are determinate and defined prior to PCH_PWROK assertion.

Table 3-3. Power Plane for Input Signals (Sheet 1 of 3)

Signal Name	Power Well	Driver During Reset	S0/S1	S3	S4/S5
DMI					
DMI_RXP[3:0], DMI_RXN[3:0]	Core	Processor	Driven	Off	Off
PCI Express					
PER[8:1]p, PER[8:1]n	Core	PCI Express Device	Driven	Off	Off
PCI Bus					
REQ0#, REQ1# / GPIO50 [1] REQ2# / GPIO52[1] REQ3# / GPIO54[1]	Core	External Pull-up	Driven	Off	Off
PME#	Suspend	Internal Pull-up	Driven	Driven	Driven
SERR#	Core	PCI Bus Peripherals	Driven	Off	Off
LPC Interface					
LDRQ0#	Core	LPC Devices	Driven	Off	Off
LDRQ1# / GPIO23[1]	Core	LPC Devices	Driven	Off	Off
SATA Interface					
SATA[5:0]RXP, SATA[5:0]RXN	Core	SATA Drive	Driven	Off	Off
SATAICOMPI	Core	High-Z	Driven	Off	Off
SATA[5:4]GP/ GPIO[49,16][1]	Core	External Device or External Pull-up/Pull-down	Driven	Off	Off

Table 3-3. Power Plane for Input Signals (Sheet 2 of 3)

Signal Name	Power Well	Driver During Reset	S0/S1	S3	S4/S5
SATA0GP / GPIO[21][1]	Core	External Device or External Pull-up/Pull-down	Driven	Off	Off
SATA1GP/GPIO19	Core	Internal Pull-up	Driven	Off	Off
SATA[3:2]GP/GPIO[37:36]	Core	Internal Pull-down	Driven	Off	Off
SATA3COMPI	Core	External Pull-up	Driven	Off	Off
USB Interface					
OC[7:0]#/ GPIO[14,10,9,43:40,59][1]	Suspend	External Pull-ups	Driven	Driven	Driven
USBRBIAS#	Suspend	External Pull-down	Driven	Driven	Driven
Power Management					
APWROK	Suspend	External Circuit	High	Driven	Driven
PWRBTN#	DSW	Internal Pull-up	Driven	Driven	Driven
PCH_PWROK	RTC	External Circuit	Driven	Driven	Driven
DPWROK	RTC	External Circuit	Driven	Driven	Driven
RI#	Suspend	Serial Port Buffer	Driven	Driven	Driven
RSMRST#	RTC	External RC Circuit	High	High	High
SYS_RESET#	Core	External Circuit	Driven	Off	Off
SYS_PWROK	Suspend	External Circuit	High	Driven	Driven
THRMTRIP#	Core (Processor)	External Thermal Sensor	Driven	Off	Off
WAKE#	Suspend	External Pull-up	Driven	Driven	Driven
Processor Interface					
A20GATE	Core	External Micro controller	Static	Off	Off
RCIN#	Core	External Micro controller	High	Off	Off
System Management Interface					
SMBALERT# / GPIO11	Suspend	External Pull-up	Driven	Driven	Driven
INTRUDER#	RTC	External Switch	Driven	Driven	Driven
JTAG Interface					
JTAG_TDI[3]	Suspend	Internal Pull-up	High	High	High
JTAG_TMS[3]	Suspend	Internal Pull-up	High	High	High
JTAG_TCK[3]	Suspend	Internal Pull down	Low	Low	Low
Miscellaneous Signals					
INTVRMEN[2]	RTC	External Pull-up	High	High	High
RTCRST#	RTC	External RC Circuit	High	High	High
SRTCRST#	RTC	External RC Circuit	High	High	High
Clock Interface					
CLKIN_SATA_N, CLKIN_SATA_P	Core	Clock Generator	Running	Off	Off
CLKIN_DOT_96P, CLKIN_DOT_96N	Core	Clock Generator	Running	Off	Off
CLKIN_PCI	Core	Clock Generator	Running	Off	Off

Table 3-3. Power Plane for Input Signals (Sheet 3 of 3)

Signal Name	Power Well	Driver During Reset	S0/S1	S3	S4/S5
CLKIN_SAS0_N, CLKIN_SAS0_P	Core	Clock Generator	Running	Off	Off
REFCLK14IN	Core	Clock Generator	Running	Off	Off
CLKIN_SAS1_N, CLKIN_SAS1_P	Core	Clock Generator	Running	Off	Off
Intel HD Audio Interface					
HDA_SDIN[3:0]	Suspend	Internal Pull-down	Driven	Low	Low
SPI Interface					
SPI_MISO	ASW	Internal Pull-up	Driven	Driven	Driven
Thermal Control					
TACH[7:0]/ GPIO[71:68,7,6,1,17][1]	Core	Internal Pull-up	Driven	Off	Off
SAS[3:0]RXP, SAS[3:0]RXN	Core	Internal Pull-down	Driven	Off	Off

Notes:
1. These signals can be configured as outputs in GPIO mode.
2. This signal is sampled as a functional strap during Reset. Refer to Table 2-26, "Functional Strap Definitions" on page 70 for usage.
3. External termination is also required for JTAG enabling.

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4 System Clock Domains

The PCH uses clock source inputs provided by CK505, an external clock chip. The inputs to the PCH include:

- 100 MHz differential, PCI Express 2.0 specification compliant, SSC capable
- 100 MHz differential isolated for SATA, SSC capable
- 100 MHz differential for PCIe 8GT/s ports, SSC capable
- 96 MHz differential, non SSC
- 14.318 MHz single-ended non SSC

4.1 System Clock Domains

Table 4-1 shows the system clock input to the PCH. Table 4-1 shows system clock domains generated by the PCH.

Table 4-1. PCH Clock Inputs

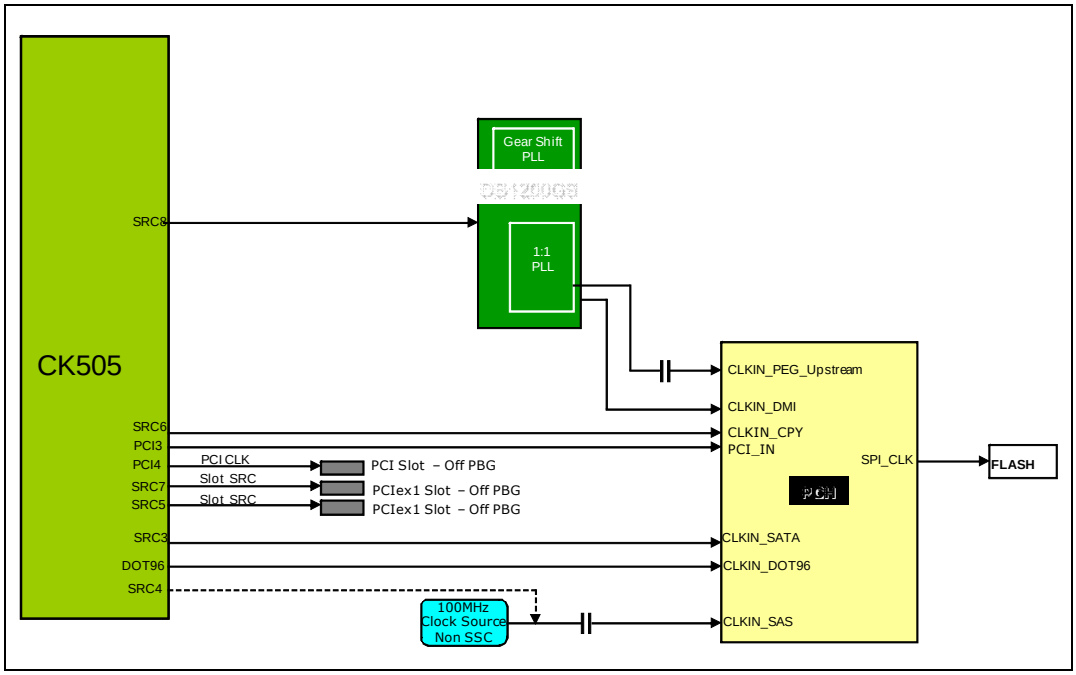
Signal	Frequency	Usage
CLKIN_DMI_P, CLKIN_DMI_N	100 MHz	100 MHz differential reference clock from CK505. Used for DMI and PCIe Gen 2.0 when clock isolation is disabled. Used for DMI only when clock isolation is enabled
CLKIN_SATA_P, CLKIN_SATA_N	100 MHz	100 MHz differential reference clock from CK505. Used for SATA.
CLKIN_DOT96_P, CLKIN_DOT96_N	96 MHz	96 MHz differential reference clock from CK505
CLKIN_PCI	33.3 MHz	33.3 MHZ PCI reference clock
REFCLK14IN	14.31818 MHz	Single-ended 14.31818 MHz reference clock from CK505. Used for 8254 Timer, ACPI Timer and HPET.
RTCX1	32.768 KHz	Reference input for RTC Oscillator
RTCX2	32.768 KHz	See above

Table 4-2. PCH Clock Outputs

Signal	Frequency	Usage
GP22_SCLOCK	32.768 KHz	SCLOCK is SATA SGPIO Reference Clock. Can also be used as GPIO22
SUSCLK_GP62	32.768 KHz	SUSCLK is a suspend clock output from RTC generator circuit. Can also be used as GPIO62
SPI_CLK	17.86 MHz/ 20.83 MHz/ 31.25 MHz	SPI Flash clock output

Figure 4-1 shows the high level block diagram of PCH clocking.

Figure 4-1. PCH High-Level Clock Diagram



4.2 Functional Blocks

Table 4-3 describes the PLLs on the PCH and the clock domains that are driven from the PLLs.

Table 4-3. PCH PLLs

PLL	Outputs Frequency	Description / Usage
DMI PLL	2.5 GHz/625 MHz/250 MHz	Source clock is 100 MHz from DB1200. The PLL resource to generate the DMI port clocks when clock isolation is enabled. Uses CLKIN_DMI input. This PLL is shut down when clock isolation is disabled. Resides in core power well and is not powered in S3 and below states.
PCIe2 PLL	2.5 GHz/625 MHz/250 MHz	PCIe2 PLL 2.5 GHz/625 MHz/250 MHz Source clock is 100 MHz from CK505. PCIe2 PLL drives clocks to PCIe 2.0 ports, Intel ME/VE engines2 (in S0 state) and the NAND interface logic2 (in S0 state). It is also used to supply DMI clocks when clock isolation is disabled. Can be configured to use CLKIN_DMI (when clock isolation is disabled) or optional CLKIN_CPY input (when clock isolation is enabled). Resides in core power well and is not powered in S3 and below states.
SATA PLL	3.0 GHz/1.5 GHz/300 MHz/ 150 MHz	Source clock is 100 MHz from CK505. This PLL generates clocks for SATA Gen2 and SATA Gen3 ports. Uses CLKIN_SATA input. Resides in core power well and is not powered in S3 and below states.
USB PLL	24 MHz/48 MHz/240 MHz/ 480 MHz	Source clock is 96 MHz from CK505. Uses CLKIN_DOT96 input. Used for USB 2.0/1.0 logic. Resides in core power well and is not powered in S3 and below states.
PCIe3 PLL	4.0 GHz/500 MHz/250 MHz	Source clock is 100 MHz from DB1200. There are two PCIe 8GT/s PLLs in the PCH. They generate clocks for PCIe 8GT/s ports. Uses CLKIN_SPCIE0 input. Resides in core power well and is not powered in S3 and below states.

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5 Functional Description

This chapter describes the functions and interfaces of the PCH family.

5.1 PCI-to-PCI Bridge (D30:F0)

The PCI-to-PCI bridge resides in PCI Device 30, Function 0 on bus #0. This portion of the PCH implements the buffering and control logic between PCI and Direct Media Interface (DMI). The arbitration for the PCI bus is handled by this PCI device. The PCI decoder in this device must decode the ranges for the DMI. All register contents are lost when core well power is removed.

DMI is the chip-to-chip connection between the Processor and PCH. This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities. Base functionality is completely software transparent permitting current and legacy software to operate normally. New for PCH the DMI interface operates at 5.0 GT/s.

To provide for true isochronous transfers and configurable Quality of Service (QoS) transactions, the PCH supports two virtual channels on DMI — VC0 and VC1. These two channels provide a fixed arbitration scheme where VC1 is always the highest priority. VC0 is the default conduit of traffic for DMI and is always enabled. VC1 must be specifically enabled and configured at both ends of the DMI link (that is, the PCH and processor).

Configuration registers for DMI, virtual channel support, and DMI active state power management (ASPM) are in the RCRB space in the Chipset Config Registers (Chapter 10.1).

DMI is also capable of operating in the AC terminated mode for HEDTs. A hardware strap is used to configure DMI in AC terminated mode, see Section 2.26 for details.

5.1.1 PCI Bus Interface

The PCH PCI interface supports *PCI Local Bus Specification*, Revision 2.3, at 33 MHz. The PCH integrates a PCI arbiter that supports up to four external PCI bus masters in addition to the internal PCH requests.

See Section 5.2 for alternative methods for supporting PCI devices.

5.1.2 PCI Bridge As an Initiator

The bridge initiates cycles on the PCI bus when granted by the PCI arbiter. The bridge generates the cycle types shown in Table 5-1.

Table 5-1. PCI Bridge Initiator Cycle Types

Command	C/BE#	Notes
I/O Read/Write	2h/3h	Non-posted
Memory Read/Write	6h/7h	Writes are posted
Configuration Read/Write	Ah/Bh	Non-posted
Special Cycles	1h	Posted

5.1.2.1 Memory Reads and Writes

The bridge bursts memory writes on PCI that are received as a single packet from DMI.

5.1.2.2 I/O Reads and Writes

The bridge generates single DW I/O read and write cycles. When the cycle completes on the PCI bus, the bridge generates a corresponding completion on DMI. If the cycle is retried, the cycle is kept in the down bound queue and may be passed by a postable cycle.

5.1.2.3 Configuration Reads and Writes

The bridge generates single DW configuration read and write cycles. When the cycle completes on the PCI bus, the bridge generates a corresponding completion. If the cycle is retried, the cycle is kept in the down bound queue and may be passed by a postable cycle.

5.1.2.4 Locked Cycles

The bridge propagates locks from DMI per the *PCI Local Bus Specification*. The PCI bridge implements bus lock, which means the arbiter will not grant to any agent except DMI while locked.

If a locked read results in a target or master abort, the lock is not established (as per the *PCI Local Bus Specification*). Agents north of the PCH must not forward a subsequent locked read to the bridge if they see the first one finish with a failed completion.

5.1.2.5 Target / Master Aborts

When a cycle initiated by the bridge is master/target aborted, the bridge will not re-attempt the same cycle. For multiple DW cycles, the bridge increments the address and attempts the next DW of the transaction. For all non-postable cycles, a target abort response packet is returned for each DW that was master or target aborted on PCI. The bridge drops posted writes that abort.

5.1.2.6 Secondary Master Latency Timer

The bridge implements a Master Latency Timer using the SMLT register which, upon expiration, causes the deassertion of FRAME# at the next legal clock edge when there is another active request to use the PCI bus.

5.1.2.7 Dual Address Cycle (DAC)

The bridge will issue full 64-bit dual address cycles for device memory-mapped registers above 4 GB.

5.1.2.8 Memory and I/O Decode to PCI

The PCI bridge in the PCH is a **subtractive decode agent**, which follows the following rules when forwarding a cycle from DMI to the PCI interface:

- The PCI bridge will **positively** decode any memory/IO address within its window registers, assuming PCICMD.MSE (D30:F0:Offset 04h:bit 1) is set for memory windows and PCICMD.IOSE (D30:F0:Offset 04h:bit 0) is set for I/O windows.
- The PCI bridge will **subtractively** decode any 64-bit memory address not claimed by another agent, assuming PCICMD.MSE (D30:F0:Offset 04h:bit 1) is set.
- The PCI bridge will **subtractively** decode any 16-bit I/O address not claimed by another agent assuming PCICMD.IOSE (D30:F0:Offset 04h:bit 0) is set.

- If BCTRL.IE (D30:F0:Offset 3Eh:bit 2) is set, the PCI bridge will **not positively** forward from primary to secondary called out ranges in the I/O window per *PCI Local Bus Specification* (I/O transactions addressing the last 768 bytes in each, 1 KB block: offsets 100h to 3FFh). The PCI bridge will still take them subtractively assuming the above rules.
- If BCTRL.VGAE (D30:F0:Offset 3Eh:bit 3) is set, the PCI bridge will **positively** forward from primary to secondary I/O and memory ranges as called out in the *PCI Bridge Specification*, assuming the above rules are met.

5.1.3 Parity Error Detection and Generation

PCI parity errors can be detected and reported. The following behavioral rules apply:

- When a parity error is detected on PCI, the bridge sets the SECSTS.DPE (D30:F0:Offset 1Eh:Bit 15).
- If the bridge is a master and BCTRL.PERE (D30:F0:Offset 3Eh:Bit 0) is set and one of the parity errors defined below is detected on PCI, then the bridge will set SECSTS.DPD (D30:F0:Offset 1Eh:Bit 8) and will also generate an internal SERR#.
  - During a write cycle, the PERR# signal is active, or
  - A data parity error is detected while performing a read cycle
- If an address or command parity error is detected on PCI and PCICMD.SEE (D30:F0:Offset 04h:bit 8), BCTRL.PERE, and BCTRL.SEE (D30:F0:Offset 3Eh:Bit 1) are all set, the bridge will set PSTS.SSE (D30:F0:Offset 06h:Bit 14) and generate an internal SERR#.
- If the PSTS.SSE is set because of an address parity error and the PCICMD.SEE is set, the bridge will generate an internal SERR#.
- When bad parity is detected from DMI, bad parity will be driven on all data from the bridge.
- When an address parity error is detected on PCI, the PCI bridge will never claim the cycle. This is a slight deviation from the PCI bridge spec, which says that a cycle should be claimed if BCTRL.PERE is not set. However, DMI does not have a concept of address parity error, so claiming the cycle could result in the rest of the system seeing a bad transaction as a good transaction.

5.1.4 PCIRST#

The PCIRST# pin is generated under two conditions:

- PLTRST# active
- BCTRL.SBR (D30:F0:Offset 3Eh:Bit 6) set to 1

The PCIRST# pin is in the suspend well. PCIRST# should be tied to PCI bus agents, but not other agents in the system.

5.1.5 Peer Cycles

The PCI bridge may be the initiator of peer cycles. Peer cycles include memory, I/O, and configuration cycle types. Peer cycles are only allowed through VC0, and are enabled with the following bits:

- BPC.PDE (D30:F0:Offset 4Ch:Bit 2) – Memory and I/O cycles
- BPC.CDE (D30:F0:Offset 4Ch:Bit 1) – Configuration cycles

When enabled for peer for one of the above cycle types, the PCI bridge will perform a peer decode to see if a peer agent can receive the cycle. When not enabled, memory cycles (posted and/or non-posted) are sent to DMI, and I/O and/or configuration cycles are not claimed.

Configuration cycles have special considerations. Under the *PCI Local Bus Specification*, these cycles are not allowed to be forwarded upstream through a bridge. However, to enable things such as manageability, BPC.CDE can be set. When set, type 1 cycles are allowed into the part. The address format of the type 1 cycle is slightly different from a standard PCI configuration cycle to allow addressing of extended PCI space. The format is shown as in Table 5-2.

Table 5-2. Type 1 Address Format

Bits	Definition
31:27	Reserved (same as the *PCI Local Bus Specification*)
26:24	Extended Configuration Address – allows addressing of up to 4K. These bits are combined with Bits 7:2 to get the full register.
23:16	Bus Number (same as the *PCI Local Bus Specification*)
15:11	Device Number (same as the *PCI Local Bus Specification*)
10:8	Function Number (same as the *PCI Local Bus Specification*)
7:2	Register (same as the *PCI Local Bus Specification*)
1	0
0	Must be 1 to indicate a type 1 cycle. Type 0 cycles are not decoded.

Note: The PCH's USB controllers cannot perform peer-to-peer traffic.

5.1.6 PCI-to-PCI Bridge Model

From a software perspective, the PCH contains a PCI-to-PCI bridge. This bridge connects DMI to the PCI bus. By using the PCI-to-PCI bridge software model, the PCH can have its decode ranges programmed by existing plug-and-play software such that PCI ranges do not conflict with graphics aperture ranges in the Host controller.

5.1.7 IDSEL to Device Number Mapping

When addressing devices on the external PCI bus (with the PCI slots), the PCH asserts one address signal as an IDSEL. When accessing Device 0, the PCH asserts AD16. When accessing Device 1, the PCH asserts AD17. This mapping continues all the way up to Device 15 where the PCH asserts AD31. The PCH internal functions (Intel High Definition Audio, USB, SATA and PCI Bridge) are enumerated like they are off of a separate PCI bus (DMI) from the external PCI bus.

5.1.8 Standard PCI Bus Configuration Mechanism

The PCI Bus defines a slot based "configuration space" that allows each device to contain up to eight functions with each function containing up to 256, 8-bit configuration registers. The *PCI Local Bus Specification*, Revision 2.3 defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the processor. Configuration space is supported by a mapping mechanism implemented within the PCH. The *PCI Local Bus Specification*, Revision 2.3 defines two mechanisms to access configuration space, Mechanism 1 and Mechanism 2. The PCH only supports Mechanism 1.

Warning: Configuration writes to internal devices, when the devices are disabled, are illegal and may cause undefined results.

5.2 PCI Legacy Mode

The PCH may optionally use PCIe-to-PCI bridges to enable external PCI I/O devices. To be able to use PCIe-to-PCI bridges and attached legacy PCI devices, the PCH provides PCI Legacy Mode. PCI Legacy Mode allows both the PCI Express root port and PCIe-to-PCI bridge look like subtractive PCI-to-PCI bridges. This allows the PCI Express root port to subtractively decode and forward legacy cycles to the bridge, and the PCIe-to-PCI bridge continues forwarding legacy cycles to downstream PCI devices. For designs that would like to utilize PCI Legacy Mode, BIOS must program registers in the PCI-to-PCI bridge (Device 30:Function 0) and in the desired PCI Express Root Port (Device 28:Functions 0-7) to enable subtractive decode.

Note: Software must ensure that only one PCH device is enabled for Subtractive decode at a time.

5.3 PCI Express*

The PCH contains up to 8 PCI Express* root ports.

In all configurations, the SMBus, SGPIO controllers are part of a multifunction device. In the PCH, the SCU, SGPIO and SMBus controllers are connected to a virtual root port that is connected to the PCH's backbone. This is Device 31 off of Bus0.

5.4 Gigabit Ethernet Controller (B0:D25:F0)

The PCH integrates a Gigabit Ethernet (GbE) controller. The integrated GbE controller is compatible with the Intel® 82579 Platform LAN Connect device. The integrated GbE controller provides two interfaces for 10/100/1000 Mb/s and manageability operation:

- Based on PCI Express – A high-speed SerDes interface using PCI Express electrical signaling at half speed while keeping the logical protocol for active state operation mode.
- System Management Bus (SMBus) – A very low speed connection for low power state mode for manageability communication only. At this low power state mode the Ethernet link speed is reduced to 10 Mb/s.

The Intel 82579 can be connected to any available downstream PCI Express port in the PCH. The Intel 82579 Phy only runs at a speed of 1250 Mb/s, which is 1/2 of the gen1 2.5 Gb/s PCI Express frequency. Each of the PCI Express root ports in the PCH chipset have the ability to run at the 1250 Mb/s rate. There is no need to implement a mechanism to detect that the Intel 82579 LAN device is connected. The port configuration (if any), attached to the Intel 82579 LAN device, is pre-loaded from the SPI flash. The selected port adjusts the transmitter to run at the 1250 Mb/s rate and does not need to be PCI Express compliant.

Note: For more detailed information about Intel 82579 LAN Connect device, refer to *Intel® 82579 Gigabit Ethernet PHY Datasheet*.

Note: PCIe validation tools cannot be used for electrical validation of this interface; however, PCIe layout rules apply for on-board routing.

The integrated GbE controller operates at full-duplex at all supported speeds or half-duplex at 10/100 Mb/s. It also adheres to the *IEEE 802.3x Flow Control Specification.*

Note: GbE operation (1000 Mb/s) is only supported in S0 mode. In Sx modes, SMBus is the only active bus and is used to support manageability/remote wake-up functionality.

The integrated GbE controller provides a system interface using a PCI Express function. A full memory-mapped or I/O-mapped interface is provided to the software, along with DMA mechanisms for high performance data transfer.

The integrated GbE controller features are:

- Network Features
  - Compliant with the 1 Gb/s Ethernet 802.3 802.3u 802.3ab specifications
  - Multi-speed operation: 10/100/1000 Mb/s
  - Full-duplex operation at 10/100/1000 Mb/s: Half-duplex at 10/100 Mb/s
  - Flow control support compliant with the 802.3X specification
  - VLAN support compliant with the 802.3q specification
  - MAC address filters: perfect match unicast filters; multicast hash filtering, broadcast filter and promiscuous mode
  - PCI Express/SMBus interface to GbE PHYs
- Host Interface Features
  - 64-bit address master support for systems using more than 4 GB of physical memory
  - Programmable host memory receive buffers (256 Bytes to 16 KB)
  - Intelligent interrupt generation features to enhance driver performance
  - Descriptor ring management hardware for transmit and receive
  - Software controlled reset (resets everything except the configuration space)
  - Message Signaled Interrupts
- Performance Features
  - Configurable receive and transmit data FIFO, programmable in 1 KB increments
  - TCP segmentation capability compatible with Windows NT* 5.x off loading features
  - Fragmented UDP checksum offload for packet reassembly
  - IPv4 and IPv6 checksum offload support (receive, transmit, and TCP segmentation offload)
  - Split header support to eliminate payload copy from user space to host space
  - Receive Side Scaling (RSS) with two hardware receive queues
  - Supports 9018 bytes of jumbo packets
  - Packet buffer size 32k bytes
  - LinkSec offload compliant with 802.3ae specification
  - TimeSync offload compliant with 802.1as specification
- Power Management Features
  - Magic Packet wake-up enable with unique MAC address
  - ACPI register set and power down functionality supporting D0 and D3 states
  - Full wake up support (APM, ACPI)
  - MAC power down at Sx, DMoff with and without WoL

5.4.1 GbE PCI Express* Bus Interface

The GbE controller has a PCI Express interface to the host processor and host memory. The following sections detail the bus transactions.

5.4.1.1 Transaction Layer

The upper layer of the host architecture is the transaction layer. The transaction layer connects to the device core using an implementation specific protocol. Through this core-to-transaction-layer protocol, the application-specific parts of the device interact with the subsystem and transmit and receive requests to or from the remote agent, respectively.

5.4.1.2 Data Alignment

5.4.1.2.1 4-KB Boundary

PCI requests must never specify an address/length combination that causes a memory space access to cross a 4-KB boundary. It is hardware's responsibility to break requests into 4-KB-aligned requests (if needed). This does not pose any requirement on software. However, if software allocates a buffer across a 4-KB boundary, hardware issues multiple requests for the buffer. Software should consider aligning buffers to 4-KB boundary in cases where it improves performance.

The alignment to the 4-KB boundaries is done in the core. The transaction layer does not do any alignment according to these boundaries.

5.4.1.2.2 64 Bytes

PCI requests are multiples of 64 bytes and aligned to make better use of memory controller resources. Writes, however, can be on any boundary and can cross a 64-byte alignment boundary.

5.4.1.3 Configuration Request Retry Status

The integrated GbE controller might have a delay in initialization due to an NVM read. If the NVM configuration read operation is not completed and the device receives a configuration request, the device responds with a configuration request retry completion status to terminate the request; this effectively stalls the configuration request until such time that the sub-system has completed local initialization and is ready to communicate with the host.

5.4.2 Error Events and Error Reporting

5.4.2.1 Data Parity Error

The PCI host bus does not provide parity protection, but it does forward parity errors from bridges. The integrated GbE controller recognizes parity errors through the internal bus interface and sets the *Parity Error* bit in PCI configuration space. If parity errors are enabled in configuration space, a system error is indicated on the PCI host bus. The offending cycle with a parity error is dropped and not processed by the integrated GbE controller.

5.4.2.2 Completion with Unsuccessful Completion Status

A completion with unsuccessful completion status (any status other than 000) is dropped and not processed by the integrated GbE controller. Furthermore, the request that corresponds to the unsuccessful completion is not retried. When this unsuccessful

completion status is received, the *System Error* bit in the PCI configuration space is set. If the system errors are enabled in configuration space, a system error is indicated on the PCI host bus.

5.4.3 Ethernet Interface

The integrated GbE controller provides a complete CSMA/CD function supporting IEEE 802.3 (10 Mb/s), 802.3u (100 Mb/s) implementations. It also supports the IEEE 802.3z and 802.3ab (1000 Mb/s) implementations. The device performs all of the functions required for transmission, reception, and collision handling called out in the standards.

The mode used to communicate between the PCH and the Intel 82579 PHY supports 10/100/1000 Mb/s operation, with both half- and full-duplex operation at 10/100 Mb/s, and full-duplex operation at 1000 Mb/s.

5.4.3.1 Intel® 82579 LAN PHY Interface

The integrated GbE controller and the Intel 82579 PHY communicate through the PCIe and SMBus interfaces. All integrated GbE controller configuration is performed using device control registers mapped into system memory or I/O space. The Intel 82579 device is configured using the PCI Express or SMBus interface.

The integrated GbE controller supports various modes as listed in Table 5-3.

Table 5-3. LAN Mode Support

Mode	System State	Interface Active	Connections
Normal 10/100/1000 Mb/s	S0	PCI Express or SMBus[1]	Intel 82579
Manageability and Remote Wake-up	Sx	SMBus	Intel 82579

1. GbE operation is not supported in Sx states.

5.4.4 PCI Power Management

The integrated GbE controller supports the Advanced Configuration and Power Interface (ACPI) specification as well as Advanced Power Management (APM). This enables the network-related activity (using an internal host wake signal) to wake up the host. For example, from Sx (S3–S5) to S0.

The integrated GbE controller contains power management registers for PCI and supports D0 and D3 states. PCIe transactions are only allowed in the D0 state, except for host accesses to the integrated GbE controller's PCI configuration registers.

5.4.4.1 Wake Up

The integrated GbE controller supports two types of wake-up mechanisms:

1. Advanced Power Management (APM) Wake Up
2. ACPI Power Management Wake Up

Both mechanisms use an internal logic signal to wake the system up. The wake-up steps are as follows:

1. Host wake event occurs (packet is not delivered to host).
2. The Intel 82579 receives a WoL packet/link status change.
3. The Intel 82579 wakes up the integrated GbE controller using an SMBus message.
4. The integrated GbE controller sets the *PME_STATUS* bit.
5. System wakes from Sx state to S0 state.
6. The host LAN function is transitioned to D0.
7. The host clears the *PME_STATUS* bit.

5.4.4.1.1 Advanced Power Management Wake Up

Advanced Power Management Wake Up or APM Wake Up was previously known as Wake on LAN (WoL). It is a feature that has existed in the 10/100 Mb/s NICs for several generations. The basic premise is to receive a broadcast or unicast packet with an explicit data pattern and then to assert a signal to wake up the system. In earlier generations, this was accomplished by using a special signal that ran across a cable to a defined connector on the motherboard. The NIC would assert the signal for approximately 50 ms to signal a wake up. The integrated GbE controller uses (if configured to) an in-band PM_PME message for this.

At power up, the integrated GbE controller reads the *APM Enable* bits from the NVM PCI Init Control Word into the APM Enable (APME) bits of the Wake Up Control (WUC) register. These bits control enabling of APM wake up.

When APM wake up is enabled, the integrated GbE controller checks all incoming packets for Magic Packets.

Once the integrated GbE controller receives a matching Magic Packet, it:

- Sets the Magic Packet *Received* bit in the Wake Up Status (WUS) register.
- Sets the *PME_Status* bit in the Power Management Control/Status Register (PMCSR).

APM wake up is supported in all power states and only disabled if a subsequent NVM read results in the *APM Wake Up* bit being cleared or the software explicitly writes a 0b to the *APM Wake Up* (APM) bit of the WUC register.

Note: APM wake up settings will be restored to NVM default by the PCH when LAN connected Device (PHY) power is turned off and subsequently restored. Some example host WOL flows are:

- When system transitions to G3 after WOL is disabled from the BIOS, APM host WOL would get enabled.
- Anytime power to the LAN Connected Device (PHY) is cycled while in S4/S5 after WOL is disabled from the BIOS, APM host WOL would get enabled. Anytime power to the LAN Connected Device (PHY) is cycled while in S3, APM host WOL configuration is lost.

5.4.4.1.2 ACPI Power Management Wake Up

The integrated GbE controller supports ACPI Power Management based Wake ups. It can generate system wake-up events from three sources:

- Receiving a Magic Packet.
- Receiving a Network Wake Up Packet.
- Detecting a link change of state.

Activating ACPI Power Management Wakeup requires the following steps:

- The software device driver programs the Wake Up Filter Control (WUFC) register to indicate the packets it needs to wake up from and supplies the necessary data to the IPv4 Address Table (IP4AT) and the Flexible Filter Mask Table (FFMT), Flexible Filter Length Table (FFLT), and the Flexible Filter Value Table (FFVT). It can also set the *Link Status Change Wake Up Enable* (LNKC) bit in the Wake Up Filter Control (WUFC) register to cause wake up when the link changes state.
- The operating system (at configuration time) writes a 1b to the *PME_EN* bit of the Power Management Control/Status Register (PMCSR.8).

Normally, after enabling wake up, the operating system writes a 11b to the lower two bits of the PMCSR to put the integrated GbE controller into low-power mode.

Once wake up is enabled, the integrated GbE controller monitors incoming packets, first filtering them according to its standard address filtering method, then filtering them with all of the enabled wake-up filters. If a packet passes both the standard address filtering and at least one of the enabled wake-up filters, the integrated GbE controller:

- Sets the *PME_Status* bit in the PMCSR
- Sets one or more of the *Received* bits in the Wake Up Status (WUS) register. (More than one bit is set if a packet matches more than one filter.)

If enabled, a link state change wake up causes similar results, setting the *Link Status Changed* (LNKC) bit in the Wake Up Status (WUS) register when the link goes up or down.

After receiving a wake-up packet, the integrated GbE controller ignores any subsequent wake-up packets until the software device driver clears all of the *Received* bits in the Wake Up Status (WUS) register. It also ignores link change events until the software device driver clears the *Link Status Changed* (LNKC) bit in the Wake Up Status (WUS) register.

Note: ACPI wake up settings are not preserved when the LAN Connected Device (PHY) power is turned off and subsequently restored. Some example host WOL flows are:

- Anytime power to the LAN Connected Device (PHY) is cycled while in S3 or S4, ACPI host WOL configuration is lost.

5.4.5 Configurable LEDs

The integrated GbE controller supports three controllable and configurable LEDs that are driven from the Intel 82579 LAN device. Each of the three LED outputs can be individually configured to select the particular event, state, or activity, which is indicated on that output. In addition, each LED can be individually configured for output polarity as well as for blinking versus non-blinking (steady-state) indication.

The configuration for LED outputs is specified using the LEDCTL register. Furthermore, the hardware-default configuration for all the LED outputs, can be specified using NVM fields, thereby supporting LED displays configurable to a particular OEM preference.

Each of the three LEDs might be configured to use one of a variety of sources for output indication. The MODE bits control the LED source:

- LINK_100/1000 is asserted when link is established at either 100 or 1000 Mb/s.
- LINK_10/1000 is asserted when link is established at either 10 or 1000 Mb/s.
- LINK_UP is asserted when any speed link is established and maintained.
- ACTIVITY is asserted when link is established and packets are being transmitted or received.
- LINK/ACTIVITY is asserted when link is established AND there is NO transmit or receive activity.
- LINK_10 is asserted when a 10 Mb/ps link is established and maintained.
- LINK_100 is asserted when a 100 Mb/s link is established and maintained.
- LINK_1000 is asserted when a 1000 Mb/s link is established and maintained.
- FULL_DUPLEX is asserted when the link is configured for full duplex operation.
- COLLISION is asserted when a collision is observed.
- PAUSED is asserted when the device's transmitter is flow controlled.
- LED_ON is always asserted; LED_OFF is always deasserted.

The *IVRT* bits enable the LED source to be inverted before being output or observed by the blink-control logic. LED outputs are assumed to normally be connected to the negative side (cathode) of an external LED.

The *BLINK* bits control whether the LED should be blinked while the LED source is asserted, and the blinking frequency (either 200 ms on and 200 ms off or 83 ms on and 83 ms off). The blink control can be especially useful for ensuring that certain events, such as ACTIVITY indication, cause LED transitions, which are sufficiently visible to a human eye. The same blinking rate is shared by all LEDs.

5.5 LPC Bridge (with System and Management Functions) (D31:F0)

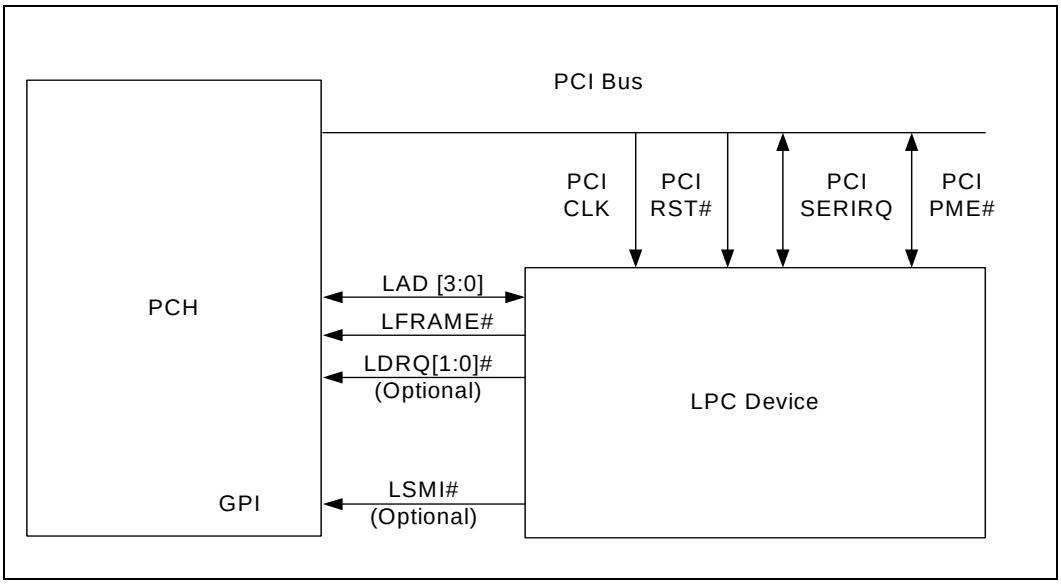
The LPC bridge function of the PCH resides in PCI Device 31:Function 0. In addition to the LPC bridge function, D31:F0 contains other functional units including DMA, Interrupt controllers, Timers, Power Management, System Management, GPIO, and RTC. In this chapter, registers and functions associated with other functional units (power management, GPIO, USB, and so forth) are described in their respective sections.

Note: The LPC bridge cannot be configured as a subtractive decode agent.

5.5.1 LPC Interface

The PCH implements an LPC interface as described in the *Low Pin Count Interface Specification*, Revision 1.1. The LPC interface to the PCH is shown in Figure 5-1. The PCH implements all of the signals that are shown as optional, but peripherals are not required to do so.

Figure 5-1. LPC Interface Diagram



5.5.1.1 LPC Cycle Types

The PCH implements all of the cycle types described in the *Low Pin Count Interface Specification*, Revision 1.1. Table 5-4 shows the cycle types supported by the PCH.

Table 5-4. LPC Cycle Types Supported

Cycle Type	Comment
Memory Read	1 byte only. (See Note 1 below)
Memory Write	1 byte only. (See Note 1 below)
I/O Read	1 byte only. The PCH breaks up 16- and 32-bit processor cycles into multiple 8-bit transfers.
I/O Write	1 byte only. The PCH breaks up 16- and 32-bit processor cycles into multiple 8-bit transfers.
DMA Read	Can be 1, or 2 bytes
DMA Write	Can be 1, or 2 bytes
Bus Master Read	Can be 1, 2, or 4 bytes. (See Note 2 below)
Bus Master Write	Can be 1, 2, or 4 bytes. (See Note 2 below)

Notes:

1. The PCH provides a single generic memory range (LGMR) for decoding memory cycles and forwarding them as LPC Memory cycles on the LPC bus. The LGMR memory decode range is 64 KB in size and can be defined as being anywhere in the 4 GB memory space. This range needs to be configured by BIOS during POST to provide the necessary memory resources. BIOS should advertise the LPC Generic Memory Range as Reserved to the operating system in order to avoid resource conflict. For larger transfers, the PCH performs multiple 8-bit transfers. If the cycle is not claimed by any peripheral, it is subsequently aborted, and the PCH returns a value of all 1s to the processor. This is done to maintain compatibility with ISA memory cycles where pull-up resistors would keep the bus high if no device responds.
2. Bus Master Read or Write cycles must be naturally aligned. For example, a 1-byte transfer can be to any address. However, the 2-byte transfer must be word-aligned (that is, with an address where A0=0). A DWord transfer must be DWord-aligned (that is, with an address where A1 and A0 are both 0).

5.5.1.2 Start Field Definition

Table 5-5. Start Field Bit Definitions

Bits[3:0] Encoding	Definition
0000	Start of cycle for a generic target
0010	Grant for bus master 0
0011	Grant for bus master 1
1111	Stop/Abort: End of a cycle for a target.

Note: All other encodings are RESERVED.

5.5.1.3 Cycle Type / Direction (CYCTYPE + DIR)

The PCH always drives Bit 0 of this field to 0. Peripherals running bus master cycles must also drive Bit 0 to 0. Table 5-6 shows the valid bit encodings.

Table 5-6. Cycle Type Bit Definitions

Bits[3:2]	Bit1	Definition
00	0	I/O Read
00	1	I/O Write
01	0	Memory Read
01	1	Memory Read
10	0	DMA Read
10	1	DMA Write
11	x	Reserved. If a peripheral performing a bus master cycle generates this value, the PCH aborts the cycle.

5.5.1.4 Size

Bits[3:2] are reserved. The PCH always drives them to 00. Peripherals running bus master cycles are also supposed to drive 00 for Bits 3:2; however, the PCH ignores those bits. Bits[1:0] are encoded as listed in Table 5-7.

Table 5-7. Transfer Size Bit Definition

Bits[1:0]	Size
00	8-bit transfer (1 byte)
01	16-bit transfer (2 bytes)
10	Reserved. The PCH never drives this combination. If a peripheral running a bus master cycle drives this combination, the PCH may abort the transfer.
11	32-bit transfer (4 bytes)

5.5.1.5 SYNC

Valid values for the SYNC field are shown in Table 5-8.

Table 5-8. SYNC Bit Definition

Bits[3:0]	Indication
0000	**Ready:** SYNC achieved with no error. For DMA transfers, this also indicates DMA request deassertion and no more transfers desired for that channel.
0101	**Short Wait:** Part indicating wait-states. For bus master cycles, the PCH does not use this encoding. Instead, the PCH uses the Long Wait encoding (see next encoding below).
0110	**Long Wait:** Part indicating wait-states, and many wait-states will be added. This encoding driven by the PCH for bus master cycles, rather than the Short Wait (0101).
1001	**Ready More (Used only by peripheral for DMA cycle):** SYNC achieved with no error and more DMA transfers desired to continue after this transfer. This value is valid only on DMA transfers and is not allowed for any other type of cycle.
1010	**Error:** Sync achieved with error. This is generally used to replace the SERR# or IOCHK# signal on the PCI/ISA bus. It indicates that the data is to be transferred, but there is a serious error in this transfer. For DMA transfers, this not only indicates an error, but also indicates DMA request deassertion and no more transfers desired for that channel.

Notes:
1. All other combinations are RESERVED.
2. If the LPC controller receives any SYNC returned from the device other than short (0101), long wait (0110), or ready (0000) when running a FWH cycle, indeterminate results may occur. A FWH device is not allowed to assert an Error SYNC.

5.5.1.6 SYNC Time-Out

There are several error cases that can occur on the LPC interface. The PCH responds as defined in section 4.2.1.9 of the *Low Pin Count Interface Specification*, Revision 1.1 to the stimuli described therein. There may be other peripheral failure conditions; however, these are not handled by the PCH.

5.5.1.7 SYNC Error Indication

The PCH responds as defined in section 4.2.1.10 of the *Low Pin Count Interface Specification*, Revision 1.1.

Upon recognizing the SYNC field indicating an error, the PCH treats this as a SERR by reporting this into the Device 31 Error Reporting Logic.

5.5.1.8 LFRAME# Usage

The PCH follows the usage of LFRAME# as defined in the *Low Pin Count Interface Specification*, Revision 1.1.

The PCH performs an abort for the following cases (possible failure cases):

- The PCH starts a Memory, I/O, or DMA cycle, but no device drives a valid SYNC after four consecutive clocks.
- The PCH starts a Memory, I/O, or DMA cycle, and the peripheral drives an invalid SYNC pattern.
- A peripheral drives an illegal address when performing bus master cycles.
- A peripheral drives an invalid value.

5.5.1.9 I/O Cycles

For I/O cycles targeting registers specified in the PCH's decode ranges, the PCH performs I/O cycles as defined in the *Low Pin Count Interface Specification*, Revision 1.1. These are 8-bit transfers. If the processor attempts a 16-bit or 32-bit transfer, the PCH breaks the cycle up into multiple 8-bit transfers to consecutive I/O addresses.

Note: If the cycle is not claimed by any peripheral (and subsequently aborted), the PCH returns a value of all 1s (FFh) to the processor. This is to maintain compatibility with ISA I/O cycles where pull-up resistors would keep the bus high if no device responds.

5.5.1.10 Bus Master Cycles

The PCH supports Bus Master cycles and requests (using LDRQ#) as defined in the *Low Pin Count Interface Specification*, Revision 1.1. The PCH has two LDRQ# inputs, and thus supports two separate bus master devices. It uses the associated START fields for Bus Master 0 (0010b) or Bus Master 1 (0011b).

Note: The PCH does not support LPC Bus Masters performing I/O cycles. LPC Bus Masters should only perform memory read or memory write cycles.

5.5.1.11 Configuration and PCH Implications

LPC I/F Decoders

To allow the I/O cycles and memory mapped cycles to go to the LPC interface, the PCH includes several decoders. During configuration, the PCH must be programmed with the same decode ranges as the peripheral. The decoders are programmed using the Device 31:Function 0 configuration space.

Note: The PCH cannot accept PCI write cycles from PCI-to-PCI bridges or devices with similar characteristics (specifically those with a "Retry Read" feature which is enabled) to an LPC device if there is an outstanding LPC read cycle towards the same PCI device or bridge. These cycles are not part of normal system operation, but may be encountered as part of platform validation testing using custom test fixtures.

Bus Master Device Mapping and START Fields

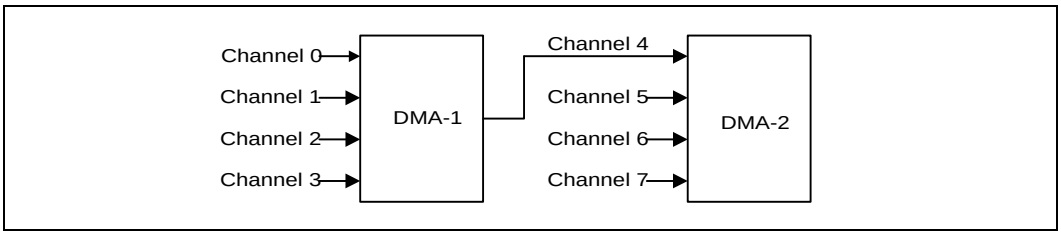
Bus Masters must have a unique START field. In the case of the PCH that supports two LPC bus masters, it drives 0010 for the START field for grants to Bus Master 0 (requested using LDRQ0#) and 0011 for grants to Bus Master 1 (requested using LDRQ1#.). Thus, no registers are needed to configure the START fields for a particular bus master.

5.6 DMA Operation (D31:F0)

The PCH supports LPC DMA using the PCH's DMA controller. The DMA controller has registers that are fixed in the lower 64 KB of I/O space. The DMA controller is configured using registers in the PCI configuration space. These registers allow configuration of the channels for use by LPC DMA.

The DMA circuitry incorporates the functionality of two 8237 DMA controllers with seven independently programmable channels (Figure 5-2). DMA Controller 1 (DMA-1) corresponds to DMA Channels 0–3 and DMA Controller 2 (DMA-2) corresponds to Channels 5–7. DMA Channel 4 is used to cascade the two controllers and defaults to cascade mode in the DMA Channel Mode (DCM) Register. Channel 4 is not available for any other purpose. In addition to accepting requests from DMA slaves, the DMA controller also responds to requests that software initiates. Software may initiate a DMA service request by setting any bit in the DMA Channel Request Register to a 1.

Figure 5-2. PCH DMA Controller



Each DMA channel is hardwired to the compatible settings for DMA device size: Channels [3:0] are hardwired to 8-bit, count-by-bytes transfers, and Channels [7:5] are hardwired to 16-bit, count-by-words (address shifted) transfers.

The PCH provides 24-bit addressing in compliance with the ISA-Compatible specification. Each channel includes a 16-bit ISA-Compatible Current Register which holds the 16 least-significant bits of the 24-bit address, an ISA-Compatible Page Register which contains the eight next most significant bits of address.

The DMA controller also features refresh address generation, and auto-initialization following a DMA termination.

5.6.1 Channel Priority

For priority resolution, the DMA consists of two logical channel groups: Channels 0–3 and Channels 4–7. Each group may be in either fixed or rotate mode, as determined by the DMA Command Register.

DMA I/O slaves normally assert their DREQ line to arbitrate for DMA service. However, a software request for DMA service can be presented through each channel's DMA Request Register. A software request is subject to the same prioritization as any hardware request. See the detailed register description for Request Register programming information in Section 13.2.

5.6.1.1 Fixed Priority

The initial fixed priority structure is as follows:

High priority	Low priority
0, 1, 2, 3	5, 6, 7

The fixed priority ordering is 0, 1, 2, 3, 5, 6, and 7. In this scheme, channel 0 has the highest priority, and Channel 7 has the lowest priority. Channels [3:0] of DMA-1 assume the priority position of Channel 4 in DMA-2, thus taking priority over Channels 5, 6, and 7.

5.6.1.2 Rotating Priority

Rotation allows for “fairness” in priority resolution. The priority chain rotates so that the last channel serviced is assigned the lowest priority in the channel group (0–3, 5–7).

Channels 0–3 rotate as a group of 4. They are always placed between Channel 5 and Channel 7 in the priority list.

Channel 5–7 rotate as part of a group of 4. That is, Channels (5–7) form the first three positions in the rotation, while Channel Group (0–3) comprises the fourth position in the arbitration.

5.6.2 Address Compatibility Mode

When the DMA is operating, the addresses do not increment or decrement through the High and Low Page Registers. Therefore, if a 24-bit address is 01FFFFh and increments, the next address is 010000h, not 020000h. Similarly, if a 24-bit address is 020000h and decrements, the next address is 02FFFFh, not 01FFFFh. However, when the DMA is operating in 16-bit mode, the addresses still do not increment or decrement through the High and Low Page Registers but the page boundary is now 128 K. Therefore, if a 24-bit address is 01FFFEh and increments, the next address is 000000h, not 0100000h. Similarly, if a 24-bit address is 020000h and decrements, the next address is 03FFFEh, not 02FFFEh. This is compatible with the 8237 and Page Register implementation used in the PC-AT. This mode is set after CPURST is valid.

5.6.3 Summary of DMA Transfer Sizes

Table 5-9 lists each of the DMA device transfer sizes. The column labeled “Current Byte/Word Count Register” indicates that the register contents represents either the number of bytes to transfer or the number of 16-bit words to transfer. The column labeled “Current Address Increment/Decrement” indicates the number added to or taken from the Current Address register after each DMA transfer cycle. The DMA Channel Mode Register determines if the Current Address Register will be incremented or decremented.

5.6.3.1 Address Shifting When Programmed for 16-Bit I/O Count by Words

Table 5-9. DMA Transfer Size

DMA Device Date Size And Word Count	Current Byte/Word Count Register	Current Address Increment/Decrement
8-Bit I/O, Count By Bytes	Bytes	1
16-Bit I/O, Count By Words (Address Shifted)	Words	1

The PCH maintains compatibility with the implementation of the DMA in the PC AT that used the 8237. The DMA shifts the addresses for transfers to/from a 16-bit device count-by-words.

Note: The least significant bit of the Low Page Register is dropped in 16-bit shifted mode. When programming the Current Address Register (when the DMA channel is in this mode), the Current Address must be programmed to an even address with the address value shifted right by one bit.

The address shifting is shown in Table 5-10.

Table 5-10. Address Shifting in 16-Bit I/O DMA Transfers

Output Address	8-Bit I/O Programmed Address (Ch 0–3)	16-Bit I/O Programmed Address (Ch 5–7) (Shifted)
A0 A[16:1] A[23:17]	A0 A[16:1] A[23:17]	0 A[15:0] A[23:17]

Note: The least significant bit of the Page Register is dropped in 16-bit shifted mode.

5.6.4 Autoinitialize

By programming a bit in the DMA Channel Mode Register, a channel may be set up as an autoinitialize channel. When a channel undergoes autoinitialization, the original values of the Current Page, Current Address and Current Byte/Word Count Registers are automatically restored from the Base Page, Address, and Byte/Word Count Registers of that channel following TC. The Base Registers are loaded simultaneously with the Current Registers by the microprocessor when the DMA channel is programmed and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in autoinitialize. Following autoinitialize, the channel is ready to perform another DMA service, without processor intervention, as soon as a valid DREQ is detected.

5.6.5 Software Commands

There are three additional special software commands that the DMA controller can execute. The three software commands are:

- Clear Byte Pointer Flip-Flop
- Master Clear
- Clear Mask Register

They do not depend on any specific bit pattern on the data bus.

5.7 LPC DMA

DMA on LPC is handled through the use of the LDRQ# lines from peripherals and special encodings on LAD[3:0] from the host. Single, Demand, Verify, and Increment modes are supported on the LPC interface. Channels 0–3 are 8-bit channels. Channels 5–7 are 16-bit channels. Channel 4 is reserved as a generic bus master request.

5.7.1 Asserting DMA Requests

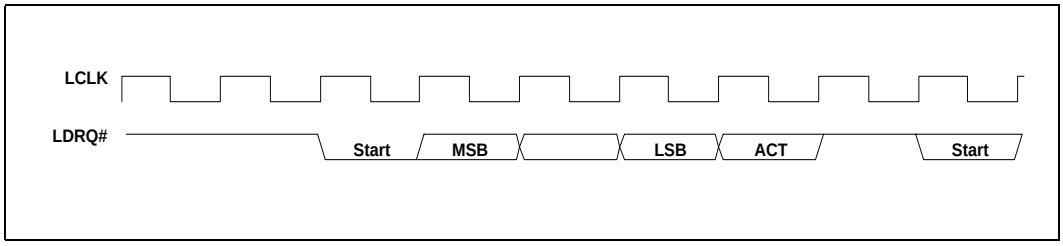
Peripherals that need DMA service encode their requested channel number on the LDRQ# signal. To simplify the protocol, each peripheral on the LPC I/F has its own dedicated LDRQ# signal (they may not be shared between two separate peripherals). The PCH has two LDRQ# inputs, allowing at least two devices to support DMA or bus mastering.

LDRQ# is synchronous with LCLK (PCI clock). As shown in Figure 5-3, the peripheral uses the following serial encoding sequence:

- Peripheral starts the sequence by asserting LDRQ# low (start bit). LDRQ# is high during idle conditions.
- The next three bits contain the encoded DMA channel number (MSB first).
- The next bit (ACT) indicates whether the request for the indicated DMA channel is active or inactive. The ACT bit is 1 (high) to indicate if it is active and 0 (low) if it is inactive. The case where ACT is low is rare, and is only used to indicate that a previous request for that channel is being abandoned.
- After the active/inactive indication, the LDRQ# signal must go high for at least 1 clock. After that one clock, LDRQ# signal can be brought low to the next encoding sequence.

If another DMA channel also needs to request a transfer, another sequence can be sent on LDRQ#. For example, if an encoded request is sent for Channel 2, and then Channel 3 needs a transfer before the cycle for Channel 2 is run on the interface, the peripheral can send the encoded request for Channel 3. This allows multiple DMA agents behind an I/O device to request use of the LPC interface, and the I/O device does not need to self-arbitrate before sending the message.

Figure 5-3. DMA Request Assertion through LDRQ#



5.7.2 Abandoning DMA Requests

DMA Requests can be deasserted in two fashions: on error conditions by sending an LDRQ# message with the 'ACT' bit set to 0, or normally through a SYNC field during the DMA transfer. This section describes boundary conditions where the DMA request needs to be removed prior to a data transfer.

There may be some special cases where the peripheral desires to abandon a DMA transfer. The most likely case of this occurring is due to a floppy disk controller which has overrun or underrun its FIFO, or software stopping a device prematurely.

In these cases, the peripheral wishes to stop further DMA activity. It may do so by sending an LDRQ# message with the ACT bit as 0. However, since the DMA request was seen by the PCH, there is no assurance that the cycle has not been granted and will shortly run on LPC. Therefore, peripherals must take into account that a DMA cycle may still occur. The peripheral can choose not to respond to this cycle, in which case the host will abort it, or it can choose to complete the cycle normally with any random data.

This method of DMA deassertion should be prevented whenever possible, to limit boundary conditions both on the PCH and the peripheral.

5.7.3 General Flow of DMA Transfers

Arbitration for DMA channels is performed through the 8237 within the host. Once the host has won arbitration on behalf of a DMA channel assigned to LPC, it asserts LFRAME# on the LPC I/F and begins the DMA transfer. The general flow for a basic DMA transfer is as follows:

1. The PCH starts transfer by asserting 0000b on LAD[3:0] with LFRAME# asserted.
2. The PCH asserts 'cycle type' of DMA, direction based on DMA transfer direction.
3. The PCH asserts channel number and, if applicable, terminal count.
4. The PCH indicates the size of the transfer: 8 or 16 bits.
5. If a DMA read…
   - The PCH drives the first 8 bits of data and turns the bus around.
   - The peripheral acknowledges the data with a valid SYNC.
   - If a 16-bit transfer, the process is repeated for the next 8 bits.
6. If a DMA write:
   - The PCH turns the bus around and waits for data.
   - The peripheral indicates data ready through SYNC and transfers the first byte.
   - If a 16-bit transfer, the peripheral indicates data ready and transfers the next byte.
7. The peripheral turns around the bus.

5.7.4 Terminal Count

Terminal count is communicated through LAD[3] on the same clock that DMA channel is communicated on LAD[2:0]. This field is the CHANNEL field. Terminal count indicates the last byte of transfer, based upon the size of the transfer.

For example, on an 8-bit transfer size (SIZE field is 00b), if the TC bit is set, then this is the last byte. On a 16-bit transfer (SIZE field is 01b), if the TC bit is set, then the second byte is the last byte. The peripheral, therefore, must internalize the TC bit when the CHANNEL field is communicated, and only signal TC when the last byte of that transfer size has been transferred.

5.7.5 Verify Mode

Verify mode is supported on the LPC interface. A verify transfer to the peripheral is similar to a DMA write, where the peripheral is transferring data to main memory. The indication from the host is the same as a DMA write, so the peripheral will be driving data onto the LPC interface. However, the host will not transfer this data into main memory.

5.7.6 DMA Request Deassertion

An end of transfer is communicated to the PCH through a special SYNC field transmitted by the peripheral. An LPC device must not attempt to signal the end of a transfer by deasserting LDREQ#. If a DMA transfer is several bytes (for example, a transfer from a demand mode device) the PCH needs to know when to deassert the DMA request based on the data currently being transferred.

The DMA agent uses a SYNC encoding on each byte of data being transferred, which indicates to the PCH whether this is the last byte of transfer or if more bytes are requested. To indicate the last byte of transfer, the peripheral uses a SYNC value of 0000b (ready with no error), or 1010b (ready with error). These encodings tell the PCH that this is the last piece of data transferred on a DMA read (PCH to peripheral), or the byte that follows is the last piece of data transferred on a DMA write (peripheral to the PCH).

When the PCH sees one of these two encodings, it ends the DMA transfer after this byte and deasserts the DMA request to the 8237. Therefore, if the PCH indicated a 16-bit transfer, the peripheral can end the transfer after one byte by indicating a SYNC value of 0000b or 1010b. The PCH does not attempt to transfer the second byte, and deasserts the DMA request internally.

If the peripheral indicates a 0000b or 1010b SYNC pattern on the last byte of the indicated size, then the PCH only deasserts the DMA request to the 8237 since it does not need to end the transfer.

If the peripheral wishes to keep the DMA request active, then it uses a SYNC value of 1001b (ready plus more data). This tells the 8237 that more data bytes are requested after the current byte has been transferred, so the PCH keeps the DMA request active to the 8237. Therefore, on an 8-bit transfer size, if the peripheral indicates a SYNC value of 1001b to the PCH, the data will be transferred and the DMA request will remain active to the 8237. At a later time, the PCH will then come back with another START–CYCTYPE–CHANNEL–SIZE, and so forth, combination to initiate another transfer to the peripheral.

The peripheral must not assume that the next START indication from the PCH is another grant to the peripheral if it had indicated a SYNC value of 1001b. On a single mode DMA device, the 8237 will re-arbitrate after every transfer. Only demand mode DMA devices can be assured that they will receive the next START indication from the PCH.

Note: Indicating a 0000b or 1010b encoding on the SYNC field of an odd byte of a 16-bit channel (first byte of a 16-bit transfer) is an error condition.

Note: The host stops the transfer on the LPC bus as indicated, fills the upper byte with random data on DMA writes (peripheral to memory), and indicates to the 8237 that the DMA transfer occurred, incrementing the 8237's address and decrementing its byte count.

5.7.7 SYNC Field / LDRQ# Rules

Since DMA transfers on LPC are requested through an LDRQ# assertion message, and are ended through a SYNC field during the DMA transfer, the peripheral must obey the following rule when initiating back-to-back transfers from a DMA channel.

The peripheral must not assert another message for eight LCLKs after a deassertion is indicated through the SYNC field. This is needed to allow the 8237, that typically runs off a much slower internal clock, to see a message deasserted before it is re-asserted so that it can arbitrate to the next agent.

Under default operation, the host only performs 8-bit transfers on 8-bit channels and 16-bit transfers on 16-bit channels.

The method by which this communication between host and peripheral through system BIOS is performed is beyond the scope of this specification. Since the LPC host and LPC peripheral are motherboard devices, no “plug-n-play” registry is required.

The peripheral must not assume that the host is able to perform transfer sizes that are larger than the size allowed for the DMA channel, and be willing to accept a SIZE field that is smaller than what it may currently have buffered.

To that end, it is recommended that future devices that may appear on the LPC bus, that require higher bandwidth than 8-bit or 16-bit DMA allow, do so with a bus mastering interface and not rely on the 8237.

5.8 8254 Timers (D31:F0)

The PCH contains three counters that have fixed uses. All registers and functions associated with the 8254 timers are in the core well. The 8254 unit is clocked by a 14.31818 MHz clock.

Counter 0, System Timer

This counter functions as the system timer by controlling the state of IRQ0 and is typically programmed for Mode 3 operation. The counter produces a square wave with a period equal to the product of the counter period (838 ns) and the initial count value. The counter loads the initial count value 1 counter period after software writes the count value to the counter I/O address. The counter initially asserts IRQ0 and decrements the count value by two each counter period. The counter negates IRQ0 when the count value reaches 0. It then reloads the initial count value and again decrements the initial count value by two each counter period. The counter then asserts IRQ0 when the count value reaches 0, reloads the initial count value, and repeats the cycle, alternately asserting and negating IRQ0.

Counter 1, Refresh Request Signal

This counter provides the refresh request signal and is typically programmed for Mode 2 operation and only impacts the period of the REF_TOGGLE bit in Port 61. The initial count value is loaded one counter period after being written to the counter I/O address. The REF_TOGGLE bit will have a square wave behavior (alternate between 0 and 1) and will toggle at a rate based on the value in the counter. Programming the counter to anything other than Mode 2 will result in undefined behavior for the REF_TOGGLE bit.

Counter 2, Speaker Tone

This counter provides the speaker tone and is typically programmed for Mode 3 operation. The counter provides a speaker frequency equal to the counter clock frequency (1.193 MHz) divided by the initial count value. The speaker must be enabled by a write to port 061h (see NMI Status and Control ports).

5.8.1 Timer Programming

The counter/timers are programmed in the following fashion:

1. Write a control word to select a counter.
2. Write an initial count for that counter.
3. Load the least and/or most significant bytes (as required by Control Word Bits 5, 4) of the 16-bit counter.
4. Repeat with other counters.

Only two conventions need to be observed when programming the counters. First, for each counter, the control word must be written before the initial count is written. Second, the initial count must follow the count format specified in the control word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

A new initial count may be written to a counter at any time without affecting the counter's programmed mode. Counting is affected as described in the mode definitions. The new count must follow the programmed count format.

If a counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same counter. Otherwise, the counter will be loaded with an incorrect count.

The Control Word Register at port 43h controls the operation of all three counters. Several commands are available:

- **Control Word Command.** Specifies which counter to read or write, the operating mode, and the count format (binary or BCD).
- **Counter Latch Command.** Latches the current count so that it can be read by the system. The countdown process continues.
- **Read Back Command.** Reads the count value, programmed mode, the current state of the OUT pins, and the state of the Null Count Flag of the selected counter.

Table 5-11 lists the six operating modes for the interval counters.

Table 5-11. Counter Operating Modes

Mode	Function	Description
0	Out signal on end of count (=0)	Output is 0. When count goes to 0, output goes to 1 and stays at 1 until counter is reprogrammed.
1	Hardware retriggerable one-shot	Output is 0. When count goes to 0, output goes to 1 for one clock time.
2	Rate generator (divide by n counter)	Output is 1. Output goes to 0 for one clock time, then back to 1 and counter is reloaded.
3	Square wave output	Output is 1. Output goes to 0 when counter rolls over, and counter is reloaded. Output goes to 1 when counter rolls over, and counter is reloaded, and so forth.
4	Software triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.
5	Hardware triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.

5.8.2 Reading from the Interval Timer

It is often desirable to read the value of a counter without disturbing the count in progress. There are three methods for reading the counters: a simple read operation, counter Latch command, and the Read-Back command. Each is explained below.

With the simple read and counter latch command methods, the count must be read according to the programmed format; specifically, if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other. Read, write, or programming operations for other counters may be inserted between them.

5.8.2.1 Simple Read

The first method is to perform a simple read operation. The counter is selected through port 40h (Counter 0), 41h (Counter 1), or 42h (Counter 2).

Note: Performing a direct read from the counter does not return a determinate value, because the counting process is asynchronous to read operations. However, in the case of Counter 2, the count can be stopped by writing to the GATE bit in Port 61h.

5.8.2.2 Counter Latch Command

The Counter Latch command, written to Port 43h, latches the count of a specific counter at the time the command is received. This command is used to ensure that the count read from the counter is accurate, particularly when reading a two-byte count. The count value is then read from each counter's Count register as was programmed by the Control register.

The count is held in the latch until it is read or the counter is reprogrammed. The count is then unlatched. This allows reading the contents of the counters on the fly without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one counter. Counter Latch commands do not affect the programmed mode of the counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch command is ignored. The count read is the count at the time the first Counter Latch command was issued.

5.8.2.3 Read Back Command

The Read Back command, written to Port 43h, latches the count value, programmed mode, and current states of the OUT pin and Null Count flag of the selected counter or counters. The value of the counter and its status may then be read by I/O access to the counter address.

The Read Back command may be used to latch multiple counter outputs at one time. This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read or reprogrammed. Once read, a counter is unlatched. The other counters remain latched until they are read. If multiple count Read Back commands are issued to the same counter without reading the count, all but the first are ignored.

The Read Back command may additionally be used to latch status information of selected counters. The status of a counter is accessed by a read from that counter's I/O port address. If multiple counter status latch operations are performed without reading the status, all but the first are ignored.

Both count and status of the selected counters may be latched simultaneously. This is functionally the same as issuing two consecutive, separate Read Back commands. If multiple count and/or status Read Back commands are issued to the same counters without any intervening reads, all but the first are ignored.

If both count and status of a counter are latched, the first read operation from that counter returns the latched status, regardless of which was latched first. The next one or two reads, depending on whether the counter is programmed for one or two type counts, returns the latched count. Subsequent reads return unlatched count.

5.9 8259 Interrupt Controllers (PIC) (D31:F0)

The PCH incorporates the functionality of two 8259 interrupt controllers that provide system interrupts for the ISA compatible interrupts. These interrupts are: system timer, keyboard controller, serial ports, parallel ports, floppy disk, mouse, and DMA channels. In addition, this interrupt controller can support the PCI based interrupts, by mapping the PCI interrupt onto the compatible ISA interrupt line. Each 8259 core supports eight interrupts, numbered 0–7. Table 5-12 shows how the cores are connected.

Table 5-12. Interrupt Controller Core Connections

8259	8259 Input	Typical Interrupt Source	Connected Pin / Function
Master	0	Internal	Internal Timer / Counter 0 output / HPET #0
	1	Keyboard	IRQ1 using SERIRQ
	2	Internal	Slave controller INTR output
	3	Serial Port A	IRQ3 using SERIRQ, PIRQ#
	4	Serial Port B	IRQ4 using SERIRQ, PIRQ#
	5	Parallel Port / Generic	IRQ5 using SERIRQ, PIRQ#
	6	Floppy Disk	IRQ6 using SERIRQ, PIRQ#
	7	Parallel Port / Generic	IRQ7 using SERIRQ, PIRQ#
Slave	0	Internal Real Time Clock	Internal RTC / HPET #1
	1	Generic	IRQ9 using SERIRQ, SCI, TCO, or PIRQ#
	2	Generic	IRQ10 using SERIRQ, SCI, TCO, or PIRQ#
	3	Generic	IRQ11 using SERIRQ, SCI, TCO, or PIRQ#, or HPET #2
	4	PS/2 Mouse	IRQ12 using SERIRQ, SCI, TCO, or PIRQ#, or HPET #3
	5	Internal	State Machine output based on processor FERR# assertion. May optionally be used for SCI or TCO interrupt if FERR# not needed.
	6	SATA	SATA Primary (legacy mode), or using SERIRQ or PIRQ#
	7	SATA	SATA Secondary (legacy mode) or using SERIRQ or PIRQ#

The PCH cascades the slave controller onto the master controller through master controller interrupt input 2. This means there are only 15 possible interrupts for the PCH's PIC.

Interrupts can individually be programmed to be edge or level, except for IRQ0, IRQ2, IRQ8, and IRQ13.

Note: Active-low interrupt sources (for example, the PIRQ#s) are inverted inside the PCH. In the following descriptions of the 8259s, the interrupt levels are in reference to the signals at the internal interface of the 8259s, after the required inversions have occurred. Therefore, the term "high" indicates "active," which means "low" on an originating PIRQ#.

5.9.1 Interrupt Handling

5.9.1.1 Generating Interrupts

The PIC interrupt sequence involves three bits, from the IRR, ISR, and IMR, for each interrupt level. These bits are used to determine the interrupt vector returned, and status of any other pending interrupts. Table 5-13 defines the IRR, ISR, and IMR.

Table 5-13. Interrupt Status Registers

Bit	Description
IRR	**Interrupt Request Register.** This bit is set on a low to high transition of the interrupt line in edge mode, and by an active high level in level mode. This bit is set whether or not the interrupt is masked. However, a masked interrupt will not generate INTR.
ISR	**Interrupt Service Register.** This bit is set, and the corresponding IRR bit cleared, when an interrupt acknowledge cycle is seen, and the vector returned is for that interrupt.
IMR	**Interrupt Mask Register.** This bit determines whether an interrupt is masked. Masked interrupts will not generate INTR.

5.9.1.2 Acknowledging Interrupts

The processor generates an interrupt acknowledge cycle that is translated by the host bridge into a PCI Interrupt Acknowledge Cycle to the PCH. The PIC translates this command into two internal INTA# pulses expected by the 8259 cores. The PIC uses the first internal INTA# pulse to freeze the state of the interrupts for priority resolution. On the second INTA# pulse, the master or slave sends the interrupt vector to the processor with the acknowledged interrupt code. This code is based upon bits [7:3] of the corresponding ICW2 register, combined with three bits representing the interrupt within that controller.

Table 5-14. Content of Interrupt Vector Byte

Master, Slave Interrupt	Bits [7:3]	Bits [2:0]
IRQ7,15	ICW2[7:3]	111
IRQ6,14		110
IRQ5,13		101
IRQ4,12		100
IRQ3,11		011
IRQ2,10		010
IRQ1,9		001
IRQ0,8		000

5.9.1.3 Hardware/Software Interrupt Sequence

1. One or more of the Interrupt Request lines (IRQ) are raised high in edge mode, or seen high in level mode, setting the corresponding IRR bit.
2. The PIC sends INTR active to the processor if an asserted interrupt is not masked.
3. The processor acknowledges the INTR and responds with an interrupt acknowledge cycle. The cycle is translated into a PCI interrupt acknowledge cycle by the host bridge. This command is broadcast over PCI by the PCH.
4. Upon observing its own interrupt acknowledge cycle on PCI, the PCH converts it into the two cycles that the internal 8259 pair can respond to. Each cycle appears as an interrupt acknowledge pulse on the internal INTA# pin of the cascaded interrupt controllers.
5. Upon receiving the first internally generated INTA# pulse, the highest priority ISR bit is set and the corresponding IRR bit is reset. On the trailing edge of the first pulse, a slave identification code is broadcast by the master to the slave on a private, internal three bit wide bus. The slave controller uses these bits to determine if it must respond with an interrupt vector during the second INTA# pulse.
6. Upon receiving the second internally generated INTA# pulse, the PIC returns the interrupt vector. If no interrupt request is present because the request was too short in duration, the PIC returns vector 7 from the master controller.
7. This completes the interrupt cycle. In Automatic End of Interrupt (AEOI) mode the ISR bit is reset at the end of the second INTA# pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

5.9.2 Initialization Command Words (ICWx)

Before operation can begin, each 8259 must be initialized. In the PCH, this is a four byte sequence. The four initialization command words are referred to by their acronyms: ICW1, ICW2, ICW3, and ICW4.

The base address for each 8259 initialization command word is a fixed location in the I/O memory space: 20h for the master controller, and A0h for the slave controller.

5.9.2.1 ICW1

An I/O write to the master or slave controller base address with data bit 4 equal to 1 is interpreted as a write to ICW1. Upon sensing this write, the PCH PIC expects three more byte writes to 21h for the master controller, or A1h for the slave controller, to complete the ICW sequence.

A write to ICW1 starts the initialization sequence during which the following automatically occur:

1. Following initialization, an interrupt request (IRQ) input must make a low-to-high transition to generate an interrupt.
2. The Interrupt Mask Register is cleared.
3. IRQ7 input is assigned priority 7.
4. The slave mode address is set to 7.
5. Special mask mode is cleared and Status Read is set to IRR.

5.9.2.2 ICW2

The second write in the sequence (ICW2) is programmed to provide bits [7:3] of the interrupt vector that will be released during an interrupt acknowledge. A different base is selected for each interrupt controller.

5.9.2.3 ICW3

The third write in the sequence (ICW3) has a different meaning for each controller.

- For the master controller, ICW3 is used to indicate which IRQ input line is used to cascade the slave controller. Within the PCH, IRQ2 is used. Therefore, bit 2 of ICW3 on the master controller is set to a 1, and the other bits are set to 0s.
- For the slave controller, ICW3 is the slave identification code used during an interrupt acknowledge cycle. On interrupt acknowledge cycles, the master controller broadcasts a code to the slave controller if the cascaded interrupt won arbitration on the master controller. The slave controller compares this identification code to the value stored in its ICW3, and if it matches, the slave controller assumes responsibility for broadcasting the interrupt vector.

5.9.2.4 ICW4

The final write in the sequence (ICW4) must be programmed for both controllers. At the very least, bit 0 must be set to a 1 to indicate that the controllers are operating in an Intel Architecture-based system.

5.9.3 Operation Command Words (OCW)

These command words reprogram the Interrupt controller to operate in various interrupt modes.

- OCW1 masks and unmasks interrupt lines.
- OCW2 controls the rotation of interrupt priorities when in rotating priority mode, and controls the EOI function.
- OCW3 sets up ISR/IRR reads, enables/disables the special mask mode (SMM), and enables/disables polled interrupt mode.

5.9.4 Modes of Operation

5.9.4.1 Fully Nested Mode

In this mode, interrupt requests are ordered in priority from 0 through 7, with 0 being the highest. When an interrupt is acknowledged, the highest priority request is determined and its vector placed on the bus. Additionally, the ISR for the interrupt is set. This ISR bit remains set until: the processor issues an EOI command immediately before returning from the service routine; or if in AEOI mode, on the trailing edge of the second INTA#. While the ISR bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels generate another interrupt. Interrupt priorities can be changed in the rotating priority mode.

5.9.4.2 Special Fully-Nested Mode

This mode is used in the case of a system where cascading is used, and the priority has to be conserved within each slave. In this case, the special fully-nested mode is programmed to the master controller. This mode is similar to the fully-nested mode with the following exceptions:

- When an interrupt request from a certain slave is in service, this slave is not locked out from the master's priority logic and further interrupt requests from higher priority interrupts within the slave are recognized by the master and initiate interrupts to the processor. In the normal-nested mode, a slave is masked out when its request is in service.
- When exiting the Interrupt Service routine, software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a Non-

Specific EOI command to the slave and then reading its ISR. If it is 0, a non-specific EOI can also be sent to the master.

5.9.4.3 Automatic Rotation Mode (Equal Priority Devices)

In some applications, there are a number of interrupting devices of equal priority. Automatic rotation mode provides for a sequential 8-way rotation. In this mode, a device receives the lowest priority after being serviced. In the worst case, a device requesting an interrupt has to wait until each of seven other devices are serviced at most once.

There are two ways to accomplish automatic rotation using OCW2; the Rotation on Non-Specific EOI Command (R=1, SL=0, EOI=1) and the rotate in automatic EOI mode which is set by (R=1, SL=0, EOI=0).

5.9.4.4 Specific Rotation Mode (Specific Priority)

Software can change interrupt priorities by programming the bottom priority. For example, if IRQ5 is programmed as the bottom priority device, then IRQ6 is the highest priority device. The Set Priority Command is issued in OCW2 to accomplish this, where: R=1, SL=1, and LO–L2 is the binary priority level code of the bottom priority device.

In this mode, internal status is updated by software control during OCW2. However, it is independent of the EOI command. Priority changes can be executed during an EOI command by using the Rotate on Specific EOI Command in OCW2 (R=1, SL=1, EOI=1 and LO–L2=IRQ level to receive bottom priority.

5.9.4.5 Poll Mode

Poll mode can be used to conserve space in the interrupt vector table. Multiple interrupts that can be serviced by one interrupt service routine do not need separate vectors if the service routine uses the poll command. Poll mode can also be used to expand the number of interrupts. The polling interrupt service routine can call the appropriate service routine, instead of providing the interrupt vectors in the vector table. In this mode, the INTR output is not used and the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P=1 in OCW3. The PIC treats its next I/O read as an interrupt acknowledge, sets the appropriate ISR bit if there is a request, and reads the priority level. Interrupts are frozen from the OCW3 write to the I/O read. The byte returned during the I/O read contains a 1 in bit 7 if there is an interrupt, and the binary code of the highest priority level in bits 2:0.

5.9.4.6 Edge and Level Triggered Mode

In ISA systems this mode is programmed using bit 3 in ICW1, which sets level or edge for the entire controller. In the PCH, this bit is disabled and a new register for edge and level triggered mode selection, per interrupt input, is included. This is the Edge/Level control Registers ELCR1 and ELCR2.

If an ELCR bit is 0, an interrupt request will be recognized by a low-to-high transition on the corresponding IRQ input. The IRQ input can remain high without generating another interrupt. If an ELCR bit is 1, an interrupt request will be recognized by a high level on the corresponding IRQ input and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued to prevent a second interrupt from occurring.

In both the edge and level triggered modes, the IRQ inputs must remain active until after the falling edge of the first internal INTA#. If the IRQ input goes inactive before this time, a default IRQ7 vector is returned.

5.9.4.7 End of Interrupt (EOI) Operations

An EOI can occur in one of two fashions: by a command word write issued to the PIC before returning from a service routine, the EOI command; or automatically when AEOI bit in ICW4 is set to 1.

5.9.4.8 Normal End of Interrupt

In normal EOI, software writes an EOI command before leaving the interrupt service routine to mark the interrupt as completed. There are two forms of EOI commands: Specific and Non-Specific. When a Non-Specific EOI command is issued, the PIC clears the highest ISR bit of those that are set to 1. Non-Specific EOI is the normal mode of operation of the PIC within the PCH, as the interrupt being serviced currently is the interrupt entered with the interrupt acknowledge. When the PIC is operated in modes that preserve the fully nested structure, software can determine which ISR bit to clear by issuing a Specific EOI. An ISR bit that is masked is not cleared by a Non-Specific EOI if the PIC is in the special mask mode. An EOI command must be issued for both the master and slave controller.

5.9.4.9 Automatic End of Interrupt Mode

In this mode, the PIC automatically performs a Non-Specific EOI operation at the trailing edge of the last interrupt acknowledge pulse. From a system standpoint, this mode should be used only when a nested multi-level interrupt structure is not required within a single PIC. The AEOI mode can only be used in the master controller and not the slave controller.

5.9.5 Masking Interrupts

5.9.5.1 Masking on an Individual Interrupt Request

Each interrupt request can be masked individually by the Interrupt Mask Register (IMR). This register is programmed through OCW1. Each bit in the IMR masks one interrupt channel. Masking IRQ2 on the master controller masks all requests for service from the slave controller.

5.9.5.2 Special Mask Mode

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The special mask mode enables all interrupts not masked by a bit set in the Mask register. Normally, when an interrupt service routine acknowledges an interrupt without issuing an EOI to clear the ISR bit, the interrupt controller inhibits all lower priority requests. In the special mask mode, any interrupts may be selectively enabled by loading the Mask Register with the appropriate pattern. The special mask mode is set by OCW3 where: SSMM=1, SMM=1, and cleared where SSMM=1, SMM=0.

5.9.6 Steering PCI Interrupts

The PCH can be programmed to allow PIRQA#-PIRQH# to be routed internally to interrupts 3–7, 9–12, 14 or 15. The assignment is programmable through the PIRQx Route Control registers, located at 60–63h and 68–6Bh in Device 31:Function 0. One or more PIRQx# lines can be routed to the same IRQx input. If interrupt steering is not required, the Route registers can be programmed to disable steering.

The PIRQx# lines are defined as active low, level sensitive to allow multiple interrupts on a PCI board to share a single line across the connector. When a PIRQx# is routed to specified IRQ line, software must change the IRQ's corresponding ELCR bit to level sensitive mode. The PCH internally inverts the PIRQx# line to send an active high level to the PIC. When a PCI interrupt is routed onto the PIC, the selected IRQ can no longer be used by an active high device (through SERIRQ). However, active low interrupts can share their interrupt with PCI interrupts.

Internal sources of the PIRQs, including SCI and TCO interrupts, cause the external PIRQ to be asserted. The PCH receives the PIRQ input, like all of the other external sources, and routes it accordingly.

5.10 Advanced Programmable Interrupt Controller (APIC) (D31:F0)

In addition to the standard ISA-compatible PIC described in the previous chapter, the PCH incorporates the APIC. While the standard interrupt controller is intended for use in a uni-processor system, APIC can be used in either a uni-processor or multi-processor system.

5.10.1 Interrupt Handling

The I/O APIC handles interrupts very differently than the 8259. Briefly, these differences are:

- **Method of Interrupt Transmission.** The I/O APIC transmits interrupts through memory writes on the normal datapath to the processor, and interrupts are handled without the need for the processor to run an interrupt acknowledge cycle.
- **Interrupt Priority.** The priority of interrupts in the I/O APIC is independent of the interrupt number. For example, interrupt 10 can be given a higher priority than interrupt 3.
- **More Interrupts.** The I/O APIC in the PCH supports a total of 24 interrupts.
- **Multiple Interrupt Controllers.** The I/O APIC architecture allows for multiple I/O APIC devices in the system with their own interrupt vectors.

5.10.2 Interrupt Mapping

The I/O APIC within the PCH supports 24 APIC interrupts. Each interrupt has its own unique vector assigned by software. The interrupt vectors are mapped as follows, and match "Config 6" of the *Multi-Processor Specification* (see Table 1-1, "Industry Specifications").

Table 5-15. APIC Interrupt Mapping[1] (Sheet 1 of 2)

IRQ #	Using SERIRQ	Direct from Pin	Using PCI Message	Internal Modules
0	No	No	No	Cascade from 8259 #1
1	Yes	No	Yes	
2	No	No	No	8254 Counter 0, HPET #0 (legacy mode)
3	Yes	No	Yes	
4	Yes	No	Yes	
5	Yes	No	Yes	
6	Yes	No	Yes	
7	Yes	No	Yes	
8	No	No	No	RTC, HPET #1 (legacy mode)
9	Yes	No	Yes	Option for SCI, TCO
10	Yes	No	Yes	Option for SCI, TCO
11	Yes	No	Yes	HPET #2, Option for SCI, TCO (Note2)
12	Yes	No	Yes	HPET #3 (Note 3)
13	No	No	No	FERR# logic
14	Yes	No	Yes	SATA Primary (legacy mode)
15	Yes	No	Yes	SATA Secondary (legacy mode)

Table 5-15. APIC Interrupt Mapping[1] (Sheet 2 of 2)

IRQ #	Using SERIRQ	Direct from Pin	Using PCI Message	Internal Modules
16	PIRQA#	PIRQA#	Yes	Internal devices are routable; see Section 10.1.20 though Section 10.1.29.
17	PIRQB#	PIRQB#		
18	PIRQC#	PIRQC#		
19	PIRQD#	PIRQD#		
20	N/A	PIRQE#[4]	Yes	Option for SCI, TCO, HPET #0,1,2, 3. Other internal devices are routable; see Section 10.1.20 though Section 10.1.29.
21	N/A	PIRQF#[4]		
22	N/A	PIRQG#[4]		
23	N/A	PIRQH#[4]		

Notes:
1. When programming the polarity of internal interrupt sources on the APIC, interrupts 0 through 15 receive active-high internal interrupt sources, while interrupts 16 through 23 receive active-low internal interrupt sources.
2. If IRQ 11 is used for HPET #2, software should ensure IRQ 11 is not shared with any other devices to ensure the proper operation of HPET #2. PCH hardware does not prevent sharing of IRQ 11.
3. If IRQ 12 is used for HPET #3, software should ensure IRQ 12 is not shared with any other devices to ensure the proper operation of HPET #3. PCH hardware does not prevent sharing of IRQ 12.
4. PIRQ[E:H]# are Multiplexed with GPIO pins. Interrupts PIRQ[E:H]# will not be exposed if they are configured as GPIOs.

5.10.3 PCI / PCI Express* Message-Based Interrupts

When external devices through PCI / PCI Express wish to generate an interrupt, they will send the message defined in the *PCI Express* Base Specification*, Revision 1.0a for generating INTA# – INTD#. These will be translated internal assertions/deassertions of INTA# – INTD#.

5.10.4 External Interrupt Controller Support

The PCH supports external APICs off of PCI Express ports, and does not support APICs on the PCI bus. The EOI special cycle is only forwarded to PCI Express ports.

5.11 Serial Interrupt (D31:F0)

The PCH supports a serial IRQ scheme. This allows a single signal to be used to report interrupt requests. The signal used to transmit this information is shared between the host, the PCH, and all peripherals that support serial interrupts. The signal line, SERIRQ, is synchronous to PCI clock, and follows the sustained tri-state protocol that is used by all PCI signals. This means that if a device has driven SERIRQ low, it will first drive it high synchronous to PCI clock and release it the following PCI clock. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S – Sample Phase.** Signal driven low
- **R** – **Recovery Phase.** Signal driven high
- **T** – **Turn-around Phase.** Signal released

The PCH supports a message for 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0–1, 3–15), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20–23).

Note: When the SATA controller is configured for legacy IDE mode, IRQ14 and IRQ15 are expected to behave as ISA legacy interrupts that cannot be shared (that is, through the Serial Interrupt pin). If IRQ14 and IRQ15 are shared with Serial Interrupt pin then abnormal system behavior may occur. For example, IRQ14/15 may not be detected by PCH's interrupt controller. When the SATA controller is not running in Native IDE mode, IRQ14 and IRQ15 are used as special interrupts. If the SATA controller is in native modes, these interrupts can be mapped to other devices accordingly.

5.11.1 Start Frame

The serial IRQ protocol has two modes of operation which affect the start frame. These two modes are: Continuous, where the PCH is solely responsible for generating the start frame; and Quiet, where a serial IRQ peripheral is responsible for beginning the start frame.

The mode that must first be entered when enabling the serial IRQ protocol is continuous mode. In this mode, the PCH asserts the start frame. This start frame is 4, 6, or 8 PCI clocks wide based upon the Serial IRQ Control Register, bits 1:0 at 64h in Device 31:Function 0 configuration space. This is a polling mode.

When the serial IRQ stream enters quiet mode (signaled in the Stop Frame), the SERIRQ line remains inactive and pulled up between the Stop and Start Frame until a peripheral drives the SERIRQ signal low. The PCH senses the line low and continues to drive it low for the remainder of the Start Frame. Since the first PCI clock of the start frame was driven by the peripheral in this mode, the PCH drives the SERIRQ line low for 1 PCI clock less than in continuous mode. This mode of operation allows for a quiet, and therefore lower power, operation.

5.11.2 Data Frames

Once the Start frame has been initiated, all of the SERIRQ peripherals must start counting frames based on the rising edge of SERIRQ. Each of the IRQ/DATA frames has exactly 3 phases of 1 clock each:

- **Sample Phase.** During this phase, the SERIRQ device drives SERIRQ low if the corresponding interrupt signal is low. If the corresponding interrupt is high, then the SERIRQ devices tri-state the SERIRQ signal. The SERIRQ line remains high due to pull-up resistors (there is no internal pull-up resistor on this signal, an external pull-up resistor is required). A low level during the IRQ0–1 and IRQ2–15 frames indicates that an active-high ISA interrupt is not being requested, but a low level

during the PCI INT[A:D], SMI#, and IOCHK# frame indicates that an active-low interrupt is being requested.

- **Recovery Phase.** During this phase, the device drives the SERIRQ line high if in the Sample Phase it was driven low. If it was not driven in the sample phase, it is tri-stated in this phase.
- **Turn-around Phase.** The device tri-states the SERIRQ line.

5.11.3 Stop Frame

After all data frames, a Stop Frame is driven by the PCH. The SERIRQ signal is driven low by the PCH for 2 or 3 PCI clocks. The number of clocks is determined by the SERIRQ configuration register. The number of clocks determines the next mode.

Table 5-16. Stop Frame Explanation

Stop Frame Width	Next Mode
2 PCI clocks	**Quiet Mode.** Any SERIRQ device may initiate a Start Frame
3 PCI clocks	**Continuous Mode.** Only the host () may initiate a Start Frame

5.11.4 Specific Interrupts Not Supported using SERIRQ

There are three interrupts seen through the serial stream that are not supported by the PCH. These interrupts are generated internally, and are not sharable with other devices within the system. These interrupts are:

- IRQ0. Heartbeat interrupt generated off of the internal 8254 counter 0.
- IRQ8#. RTC interrupt can only be generated internally.
- IRQ13. Floating point error interrupt generated off of the processor assertion of FERR#.

The PCH ignores the state of these interrupts in the serial stream, and does not adjust their level based on the level seen in the serial stream.

5.11.5 Data Frame Format

Table 5-17 shows the format of the data frames. For the PCI interrupts (A–D), the output from the PCH is AND'd with the PCI input signal. This way, the interrupt can be signaled using both the PCI interrupt input signal and using the SERIRQ signal (they are shared).

Table 5-17. Data Frame Format

Data Frame #	Interrupt	Clocks Past Start Frame	Comment
1	IRQ0	2	Ignored. IRQ0 can only be generated using the internal 8524
2	IRQ1	5	
3	SMI#	8	Causes SMI# if low. Will set the SERIRQ_SMI_STS bit.
4	IRQ3	11	
5	IRQ4	14	
6	IRQ5	17	
7	IRQ6	20	
8	IRQ7	23	
9	IRQ8	26	Ignored. IRQ8# can only be generated internally.
10	IRQ9	29	
11	IRQ10	32	
12	IRQ11	35	
13	IRQ12	38	
14	IRQ13	41	Ignored. IRQ13 can only be generated from FERR#
15	IRQ14	44	Not attached to SATA logic
16	IRQ15	47	Not attached to SATA logic
17	IOCHCK#	50	Same as ISA IOCHCK# going active.
18	PCI INTA#	53	Drive PIRQA#
19	PCI INTB#	56	Drive PIRQB#
20	PCI INTC#	59	Drive PIRQC#
21	PCI INTD#	62	Drive PIRQD#

5.12 Real Time Clock (D31:F0)

The Real Time Clock (RTC) module provides a battery backed-up date and time keeping device with two banks of static RAM with 128 bytes each, although the first bank has 114 bytes for general purpose usage. Three interrupt features are available: time of day alarm with once a second to once a month range, periodic rates of 122 µs to 500 ms, and end of update cycle notification. Seconds, minutes, hours, days, day of week, month, and year are counted. Daylight savings compensation is no longer supported. The hour is represented in twelve or twenty-four hour format, and data can be represented in BCD or binary format. The design is functionally compatible with the Motorola MS146818B. The time keeping comes from a 32.768 kHz oscillating source, which is divided to achieve an update every second. The lower 14 bytes on the lower RAM block has very specific functions. The first ten are for time and date information. The next four (0Ah to 0Dh) are registers, which configure and report RTC functions.

The time and calendar data should match the data mode (BCD or binary) and hour mode (12 or 24 hour) as selected in register B. It is up to the programmer to make sure that data stored in these locations is within the reasonable values ranges and represents a possible date and time. The exception to these ranges is to store a value of C0–FFh in the Alarm bytes to indicate a don't care situation. All Alarm conditions must match to trigger an Alarm Flag, which could trigger an Alarm Interrupt if enabled. The SET bit must be 1 while programming these locations to avoid clashes with an update cycle. Access to time and date information is done through the RAM locations. If a RAM read from the ten time and date bytes is attempted during an update cycle, the value read do not necessarily represent the true contents of those locations. Any RAM writes under the same conditions are ignored.

Note: The leap year determination for adding a 29th day to February does not take into account the end-of-the-century exceptions. The logic simply assumes that all years divisible by 4 are leap years. According to the Royal Observatory Greenwich, years that are divisible by 100 are typically not leap years. In every fourth century (years divisible by 400, like 2000), the 100-year-exception is over-ridden and a leap-year occurs. The year 2100 will be the first time in which the current RTC implementation would incorrectly calculate the leap-year.

The PCH does not implement month/year alarms.

5.12.1 Update Cycles

An update cycle occurs once a second, if the SET bit of register B is not asserted and the divide chain is properly configured. During this procedure, the stored time and date are incremented, overflow is checked, a matching alarm condition is checked, and the time and date are rewritten to the RAM locations. The update cycle will start at least 488 µs after the UIP bit of register A is asserted, and the entire cycle does not take more than 1984 µs to complete. The time and date RAM locations (0–9) are disconnected from the external bus during this time.

To avoid update and data corruption conditions, external RAM access to these locations can safely occur at two times. When a updated-ended interrupt is detected, almost 999 ms is available to read and write the valid time and date data. If the UIP bit of Register A is detected to be low, there is at least 488 µs before the update cycle begins.

Warning: The overflow conditions for leap years adjustments are based on more than one date or time item. To ensure proper operation when adjusting the time, the new time and data values should be set at least two seconds before leap year occurs.

5.12.2 Interrupts

The real-time clock interrupt is internally routed within the PCH both to the I/O APIC and the 8259. It is mapped to interrupt vector 8. This interrupt does not leave the PCH, nor is it shared with any other interrupt. IRQ8# from the SERIRQ stream is ignored. However, the High Performance Event Timers can also be mapped to IRQ8#; in this case, the RTC interrupt is blocked.

5.12.3 Lockable RAM Ranges

The RTC battery-backed RAM supports two 8-byte ranges that can be locked using the configuration space. If the locking bits are set, the corresponding range in the RAM will not be readable or writable. A write cycle to those locations will have no effect. A read cycle to those locations will not return the location's actual value (resultant value is undefined).

Once a range is locked, the range can be unlocked only by a hard reset, which will invoke the BIOS and allow it to relock the RAM range.

5.12.4 Century Rollover

The PCH detects a rollover when the Year byte (RTC I/O space, index Cffset 09h) transitions form 99 to 00. Upon detecting the rollover, the PCH sets the NEWCENTURY_STS bit (TCOBASE + 04h, bit 7). If the system is in an S0 state, this causes an SMI#. The SMI# handler can update registers in the RTC RAM that are associated with century value. If the system is in a sleep state (S1–S5) when the century rollover occurs, the PCH also sets the NEWCENTURY_STS bit, but no SMI# is generated. When the system resumes from the sleep state, BIOS should check the NEWCENTURY_STS bit and update the century value in the RTC RAM.

5.12.5 Clearing Battery-Backed RTC RAM

Clearing CMOS RAM in an PCH-based platform can be done by using a jumper on RTCRST# or GPI. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low.

Using RTCRST# to Clear CMOS

A jumper on RTCRST# can be used to clear CMOS values, as well as reset to default, the state of those configuration bits that reside in the RTC power well. When the RTCRST# is strapped to ground, the RTC_PWR_STS bit (D31:F0:A4h bit 2) will be set and those configuration bits in the RTC power well will be set to their default state. BIOS can monitor the state of this bit, and manually clear the RTC CMOS array once the system is booted. The normal position would cause RTCRST# to be pulled up through a weak pull-up resistor. Table 5-18 shows which bits are set to their default state when RTCRST# is asserted. This RTCRST# jumper technique allows the jumper to be moved and then replaced—all while the system is powered off. Then, once booted, the RTC_PWR_STS can be detected in the set state.

Table 5-18. Configuration Bits Reset by RTCRST# Assertion

Bit Name	Register	Location	Bit(s)	Default State
Alarm Interrupt Enable (AIE)	Register B (General Configuration) (RTC_REGB)	I/O space (RTC Index + 0Bh)	5	X
Alarm Flag (AF)	Register C (Flag Register) (RTC_REGC)	I/O space (RTC Index + 0Ch)	5	X
SWSMI_RATE_SEL	General PM Configuration 3 Register GEN_PMCON_3	D31:F0:A4h	7:6	0
SLP_S4# Minimum Assertion Width	General PM Configuration 3 Register GEN_PMCON_3	D31:F0:A4h	5:4	0
SLP_S4# Assertion Stretch Enable	General PM Configuration 3 Register GEN_PMCON_3	D31:F0:A4h	3	0
RTC Power Status (RTC_PWR_STS)	General PM Configuration 3 Register GEN_PMCON_3	D31:F0:A4h	2	0
Power Failure (PWR_FLR)	General PM Configuration 3 Register (GEN_PMCON_3)	D31:F0:A4h	1	0
AFTERG3_EN	General PM Configuration 3 Register GEN_PMCON_3	D31:F0:A4h	0	0
Power Button Override Status (PRBTNOR_STS)	Power Management 1 Status Register (PM1_STS)	PMBase + 00h	11	0
RTC Event Enable (RTC_EN)	Power Management 1 Enable Register (PM1_EN)	PMBase + 02h	10	0
Sleep Type (SLP_TYP)	Power Management 1 Control (PM1_CNT)	PMBase + 04h	12:10	0
PME_EN	General Purpose Event 0 Enables Register (GPE0_EN)	PMBase + 2Ch	11	0
BATLOW_EN	General Purpose Event 0 Enables Register (GPE0_EN)	PMBase + 2Ch	10	0
RI_EN	General Purpose Event 0 Enables Register (GPE0_EN)	PMBase + 2Ch	8	0
NEWCENTURY_STS	TCO1 Status Register (TCO1_STS)	TCOBase + 04h	7	0
Intruder Detect (INTRD_DET)	TCO2 Status Register (TCO2_STS)	TCOBase + 06h	0	0
Top Swap (TS)	Backed Up Control Register (BUC)	Chipset Config Registers:Offset 3414h	0	X

Using a GPI to Clear CMOS

A jumper on a GPI can also be used to clear CMOS values. BIOS would detect the setting of this GPI on system boot-up, and manually clear the CMOS array.

Note: The GPI strap technique to clear CMOS requires multiple steps to implement. The system is booted with the jumper in new position, then powered back down. The jumper is replaced back to the normal position, then the system is rebooted again.

Warning: Do not implement a jumper on VccRTC to clear CMOS.

5.13 Processor Interface (D31:F0)

The PCH interfaces to the processor with following pin-based signals other than DMI:

- Standard Outputs to processor: PROCPWRGD, PM_SYNC, PM_SYNC2, PECI
- Standard Input from processor: THRMTRIP#

Most PCH outputs to the processor use standard buffers. The PCH has separate V_PROC_IO signals that are pulled up at the system level to the processor voltage, and thus determines VOH for the outputs to the processor.

The following Processor interface legacy pins were removed from the PCH:

- IGNNE#, STPCLK#, DPSLP#, are DPRSLPVR are no longer required on PCH based systems.
- A20M#, SMI#, NMI, INIT#, INTR, FERR#: Functionality has been replaced by in-band Virtual Legacy Wire (VLW) messages. See Section 5.13.3.

5.13.1 Processor Interface Signals and VLW Messages

This section describes each of the signals that interface between the PCH and the processor(s). The behavior of some signals may vary during processor reset, as the signals are used for frequency strapping.

5.13.1.1 A20M# (Mask A20) / A20GATE

The A20M# VLW message is asserted when both of the following conditions are true:

- The ALT_A20_GATE bit (Bit 1 of PORT92 register) is a 0
- The A20GATE input signal is a 0

The A20GATE input signal is expected to be generated by the external microcontroller (KBC).

5.13.1.2 INIT (Initialization)

The INIT# VLW Message is asserted based on any one of several events described in Table 5-19. When any of these events occur, INIT# is asserted for 16 PCI clocks, then driven high.

Note: INIT3_3V# is functionally identical to INIT# VLW but it is a physical signal at 3.3 V.

Table 5-19. INIT# Going Active (Sheet 1 of 2)

Cause of INIT3_3V# Going Active	Comment
Shutdown special cycle from processor observed on PCH-Processor interconnect.	INIT assertion based on value of Shutdown Policy Select register (SPS)
PORT92 write, where INIT_NOW (bit 0) transitions from a 0 to a 1.	
PORTCF9 write, where SYS_RST (bit 1) was a 0 and RST_CPU (bit 2) transitions from 0 to 1.	

Table 5-19. INIT# Going Active (Sheet 2 of 2)

Cause of INIT3_3V# Going Active	Comment
RCIN# input signal goes low. RCIN# is expected to be driven by the external microcontroller (KBC).	0 to 1 transition on RCIN# must occur before the PCH will arm INIT3_3V# to be generated again. ***Note:*** RCIN# signal is expected to be low during S3, S4, and S5 states. Transition on the RCIN# signal in those states (or the transition to those states) may not necessarily cause the INIT3_3V# signal to be generated to the processor.
Processor BIST	To enter BIST, software sets CPU_BIST_EN bit and then does a full processor reset using the CF9 register.

5.13.1.3 FERR# (Numeric Coprocessor Error)

The PCH supports the coprocessor error function with the FERR# message. The function is enabled using the CEN bit. If FERR# is driven active by the processor, IRQ13 goes active (internally). When it detects a write to the COPROC_ERR register (I/O Register F0h), the PCH negates the internal IRQ13 and IGNNE# will be active. IGNNE# remains active until FERR# is driven inactive. IGNNE# is never driven active unless FERR# is active.

Note: IGNNE# – Ignore Numeric Error is now internally generated by the processor.

5.13.1.4 NMI (Non-Maskable Interrupt)

Non-Maskable Interrupts (NMIs) can be generated by several sources, as described in Table 5-20.

Table 5-20. NMI Sources

Cause of NMI	Comment
SERR# goes active (either internally, externally using SERR# signal, or using message from Processor)	Can instead be routed to generate an SCI, through the NMI2SCI_EN bit (Device 31:Function 0, TCO Base + 08h, bit 11).
IOCHK# goes active using SERIRQ# stream (ISA system Error)	Can instead be routed to generate an SCI, through the NMI2SCI_EN bit (Device 31:Function 0, TCO Base + 08h, bit 11).
SECSTS Register Device 31: Function F0 Offset 1Eh, bit 8.	This is enabled by the Parity Error Response Bit (PER) at Device 30: Function 0 Offset 04, bit 6.
DEV_STS Register Device 31:Function F0 Offset 06h, bit 8	This is enabled by the Parity Error Response Bit (PER) at Device 30: Function 0 Offset 04, bit 6.
GPIO[15:0] when configured as a General Purpose input and routed as NMI (by GPIO_ROUT at Device 31: Function 0 Offset B8)	This is enabled by GPI NMI Enable (GPI_NMI_EN) bits at Device 31: Function 0 Offset: GPIOBASE + 28h bits 15:0

5.13.1.5 Processor Power Good (PROCPWRGD)

This signal is connected to the processor's PRWGOOD input to indicate when the processor power is valid.

5.13.2 Dual-Processor Issues

5.13.2.1 Usage Differences

In dual-processor designs, some of the processor signals are unused or used differently than for uniprocessor designs.

- A20M#/A20GATE and FERR# are generally not used, but still supported.
- I/O APIC and SMI# are assumed to be used.

5.13.3 Virtual Legacy Wire (VLW) Messages

The PCH supports VLW messages as alternative method of conveying the status of the following legacy sideband interface signals to the Processor:

- A20M#, INTR, SMI#, INIT#, NMI

Note: IGNNE# VLW message is not required to be generated by the PCH as it is internally emulated by the Processor.

VLW are inbound messages to the Processor. They are communicated using Vendor Defined Message over the DMI link.

Legacy processor signals can only be delivered using VLW in PCH. Delivery of legacy processor signals (A20M#, INTR, SMI#, INIT# or NMI) using I/O APIC controller is not supported.

5.14 Power Management

5.14.1 Features

- Support for *Advanced Configuration and Power Interface, Version 3.0b (ACPI)* providing power and thermal management
  - ACPI 24-Bit Timer SCI and SMI# Generation
- PCI PME# signal for Wake Up from Low-Power states
- System Sleep State Control
  - ACPI S3 state — Suspend to RAM (STR)
  - ACPI S4 state — Suspend-to-Disk (STD)
  - ACPI G2/S5 state — Soft Off (SOFF)
  - Power Failure Detection and Recovery
  - Deep S4/S5
- Intel ME Power Management Support
  - Wake events from the Intel ME (enabled from all S-States including Catastrophic S5 conditions)

5.14.2 PCH and System Power States

Table 5-21 shows the power states defined for PCH-based platforms. The state names generally match the corresponding ACPI states.

Table 5-21. General Power States for Systems Using the PCH

State/ Substates	Legacy Name / Description
G0/S0/C0	**Full On:** Processor operating. Individual devices may be shut down or be placed into lower power states to save power.
G0/S0/Cx	**Cx State:** Cx states are processor power states within the S0 system state that provide for various levels of power savings. The Processor initiates C-state entry and exit while interacting with the PCH through DMI messaging. The PCH will base its behavior on the Processor state.
G1/S1	**S1:** PCH provides the S1 messages and the S0 messages on a wake event. It is much preferred for systems to use C-states than S1.
G1/S3	**Suspend-To-RAM (STR):** The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained and refreshes continue. All external clocks stop except RTC.
G1/S4	**Suspend-To-Disk (STD):** The context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
G2/S5	**Soft Off (SOFF):** System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.
Deep S4/S5	**Deep S4/S5:** An optional low power state where system context may or may not be maintained depending upon entry condition. All power is shut off except for minimal logic that allows exiting Deep S4/S5. If Deep S4/S5 state was entered from S4 state, then the resume path will place system back into S4. If Deep S4/S5 state was entered from S5 state, then the resume path will place system back into S5.
G3	**Mechanical OFF (MOFF):** System context not maintained. All power is shut off except for the RTC. No "Wake" events are possible. This state occurs if the user turns off a mechanical switch or if the system power supply is at a level that is insufficient to power the "waking" logic. When system power returns, transition will depend on the state just prior to the entry to G3 and the AFTERG3 bit in the GEN_PMCON3 register (D31:F0, offset A4). Refer to Table 5-28 for more details.

Table 5-22 shows the transitions rules among the various states. Transitions among the various states may appear to temporarily transition through intermediate states. For example, in going from S0 to S3, it may appear to pass through the G1/S1 states. These intermediate transitions and states are not listed in the table.

Table 5-22. State Transition Rules for the PCH (Sheet 1 of 2)

Present State	Transition Trigger	Next State
G0/S0/C0	• DMI Msg • SLP_EN bit set • Power Button Override2[2] • Mechanical Off/Power Failure	• G0/S0/Cx • G1/Sx or G2/S5 state • G2/S5 • G3
G0/S0/Cx	• DMI Msg • Power Button Override[2] • Mechanical Off/Power Failure	• G0/S0/C0 • G2/S5 • G3
G1/S1 or G1/S3	• Any Enabled Wake Event • Power Button Override[2] • Mechanical Off/Power Failure	• G0/S0/C0 • G2/S5 • G3

Table 5-22. State Transition Rules for the PCH (Sheet 2 of 2)

Present State	Transition Trigger	Next State
G1/S4	• Any Enabled Wake Event • Power Button Override[2] • Conditions met as described in Section 5.14.6.6.1 and Section 5.14.6.6.2 • Mechanical Off/Power Failure	• G0/S0/C0 • G2/S5 • Deep S4/S5 • G3
G2/S5	• Any Enabled Wake Event • Conditions met as described in Section 5.14.6.6.1 and Section 5.14.6.6.2 • Mechanical Off/Power Failure	• G0/S0/C0[2] • Deep S4/S5 • G3
G2/Deep S4/S5	• Any Enabled Wake Event • Mechanical Off/Power Failure	• G0/S0/C0 • G1/S4 or G2/S5 (see Section 5.14.6.6.2) • G3
G3	• Power Returns	• Optional to go to S0/C0 (reboot) or G2/S5 (stay off until power button pressed or other wake event). (See Note 1)

Notes:
1. Some wake events can be preserved through power failure.
2. Includes all other applicable types of events that force the host into and stay in G2/S5.
3. If the system was in G1/S4 before G3 entry, then the system will go to S0/C0 or G1/S4.

5.14.3 System Power Planes

The system has several independent power planes, as described in Table 5-23. When a particular power plane is shut off, it should go to a 0 V level.

Table 5-23. System Power Plane

Plane	Controlled By	Description
Processor	SLP_S3# signal	The SLP_S3# signal can be used to cut the power to the processor completely.
Main	SLP_S3# signal	When SLP_S3# goes active, power can be shut off to any circuit not required to wake the system from the S3 state. Since the S3 state requires that the memory context be preserved, power must be retained to the main memory. The processor, devices on the PCI bus, LPC I/F, and graphics will typically be shut off when the Main power plane is off, although there may be small subsections powered.
Memory	SLP_S4# signal SLP_S5# signal	When SLP_S4# goes active, power can be shut off to any circuit not required to wake the system from the S4. Since the memory context does not need to be preserved in the S4 state, the power to the memory can also be shut down. When SLP_S5# goes active, power can be shut off to any circuit not required to wake the system from the S5 state. Since the memory context does not need to be preserved in the S5 state, the power to the memory can also be shut.
Intel ME	SLP_A#	This signal is asserted when the manageability platform goes to MOff. Depending on the platform, this pin may be used to control the Intel ME power planes, LAN subsystem power, and the SPI flash power.
LAN	SLP_LAN#	This signal is asserted in Sx/Moff when both host and Intel ME WOL are not supported. This signal can be use to control power to the Intel GbE PHY.
Deep S4/S5 Well	SLP_SUS#	This signal that the Sus rails externally can be shut off for enhanced power saving.
DEVICE[n]	GPIO	Individual subsystems may have their own power plane. For example, GPIO signals may be used to control the power to disk drives, audio amplifiers, or the display screen.

5.14.4 SMI#/SCI Generation

Upon any enabled Intel SMI event taking place while the End of Intel SMI (EOS) bit is set, the PCH will clear the EOS bit and assert Intel SMI to the processor, which will cause it to enter SMM space. Intel SMI assertion is performed using a Virtual Legacy Wire (VLW) message. Prior system generations (those based upon legacy processors) used an actual SMI# pin.

Once the Intel SMI VLW has been delivered, the PCH takes no action on behalf of active Intel SMI events until Host software sets the End of Intel SMI (EOS) bit. At that point, if any Intel SMI events are still active, the PCH will send another Intel SMI VLW.

The SCI is a level-mode interrupt that is typically handled by an ACPI-aware operating system. In non-APIC systems (which is the default), the SCI IRQ is routed to one of the 8259 interrupts (IRQ 9, 10, or 11). The 8259 interrupt controller must be programmed to level mode for that interrupt.

In systems using the APIC, the SCI can be routed to interrupts 9, 10, 11, 20, 21, 22, or 23. The interrupt polarity changes depending on whether it is on an interrupt shareable with a PIRQ or not (see Section 13.1.14). The interrupt remains asserted until all SCI sources are removed.

Table 5-24 shows which events can cause an Intel SMI and SCI. Some events can be programmed to cause either an Intel SMI or SCI. The usage of the event for SCI (instead of Intel SMI) is typically associated with an ACPI-based system. Each Intel SMI or SCI source has a corresponding enable and status bit.

Table 5-24. Causes of Intel® Scalable Memory Interconnect (Intel® SMI) and SCI (Sheet 1 of 3)

Cause	SCI	SMI	Additional Enables	Where Reported
PME#	Yes	Yes	PME_EN=1	PME_STS
PME_B0 (Internal, Bus 0, PME-Capable Agents)	Yes	Yes	PME_B0_EN=1	PME_B0_STS
PCI Express PME Messages	Yes	Yes	PCI_EXP_EN=1 (Not enabled for SMI)	PCI_EXP_STS
PCI Express Hot-Plug Message	Yes	Yes	HOT_PLUG_EN=1 (Not enabled for SMI)	HOT_PLUG_STS
Power Button Press	Yes	Yes	PWRBTN_EN=1	PWRBTN_STS
Power Button Override (Note 7)	Yes	No	None	PRBTNOR_STS
RTC Alarm	Yes	Yes	RTC_EN=1	RTC_STS
Ring Indicate	Yes	Yes	RI_EN=1	RI_STS
USB#1 wakes	Yes	Yes	USB1_EN=1	USB1_STS
USB#2 wakes	Yes	Yes	INTEL_USB2_EN=1	INTEL_USB2_STS
USB#3 wakes	Yes	Yes	USB3_EN=1	USB3_STS
USB#4 wakes	Yes	Yes	USB4_EN=1	USB4_STS
USB#5 wakes	Yes	Yes	USB5_EN=1	USB5_STS
USB#6 wakes	Yes	Yes	USB6_EN=1	USB6_STS
USB#9 wakes	Yes	Yes	USB9_EN=1	USB9_STS
ACPI Timer overflow (2.34 sec.)	Yes	Yes	TMROF_EN=1	TMROF_STS
Any GPI[15:0]	Yes	Yes	GPI[x]_Route=10; GPI[x]_EN=1 (SCI) GPI[x]_Route=01; ALT_GPI_SMI[x]_EN=1 (SMI)	GPI[x]_STS ALT_GPI_SMI[x]_STS

Table 5-24. Causes of Intel® Scalable Memory Interconnect (Intel® SMI) and SCI (Sheet 2 of 3)

Cause	SCI	SMI	Additional Enables	Where Reported
GPIO[27]	Yes	Yes	GP27_EN=1	GP27_STS
TCO SCI Logic	Yes	No	TCOSCI_EN=1	TCOSCI_STS
TCO SCI message from MCH	Yes	Yes	none	MCHSCI_STS MCHSMI_STS
TCO SMI Logic	No	Yes	TCO_EN=1	TCO_STS
TCO SMI — Year 2000 Rollover	No	Yes	none	NEWCENTURY_STS
TCO SMI — TCO TIMEROUT	No	Yes	none	TIMEOUT
TCO SMI — operating system writes to TCO_DAT_IN register	No	Yes	none	SW_TCO_SMI
TCO SMI — Message from processor	No	Yes	none	DMISMI_STS
TCO SMI — NMI occurred (and NMIs mapped to SMI)	No	Yes	NMI2SMI_EN=1	NMI2SMI_STS
TCO SMI — INTRUDER# signal goes active	No	Yes	INTRD_SEL=10	INTRD_DET
TCO SMI — Change of the BIOSWE (D31:F0:DCh, bit 0) bit from 0 to 1	No	Yes	BCLE=1	BIOSWR_STS
TCO SMI — Write attempted to BIOS	No	Yes	BC.WPD =0 (Write Protect Disable)	BIOSWR_STS
NMI (and NMI's mapped to SMI) See NMI section for causes of NMI	No	Yes	NMI2SMI_EN=1	TCO_STS_NMI2SMI_STS
BIOS_RLS written to	Yes	No	GBL_EN=1	GBL_STS
GBL_RLS written to	No	Yes	BIOS_EN=1	BIOS_STS
Write to B2h register	No	Yes	APMC_EN = 1	APM_STS
Periodic timer expires	No	Yes	PERIODIC_EN=1	PERIODIC_STS
64 ms timer expires	No	Yes	SWSMI_TMR_EN=1	SWSMI_TMR_STS
Enhanced USB Legacy Support Event	No	Yes	LEGACY_USB2_EN = 1	LEGACY_USB2_STS
Enhanced USB Intel Specific Event	No	Yes	INTEL_USB2_EN = 1	INTEL_USB2_STS
Serial IRQ Intel SMI reported	No	Yes	none	SERIRQ_SMI_STS
Device monitors match address in its range	No	Yes	See DEVTRAP_STS register description	DEVTRAP_STS
SMBus Host Controller	No	Yes	SMB_SMI_EN Host Controller Enabled	SMBus host status reg.
SMBus Slave Intel SMI message	No	Yes	none	SMBUS_SMI_STS
SMBus SMBALERT# signal active	No	Yes	none	SMBUS_SMI_STS
SMBus Host Notify message received	No	Yes	HOST_NOTIFY_INTREN	SMBUS_SMI_STS HOST_NOTIFY_STS
Access microcontroller 62h/66h	No	Yes	MCSMI_EN	MCSMI_STS
SLP_EN bit written to 1	No	Yes	SLP_SMI_EN=1	SLP_SMI_STS
SPI Command Completed	No	Yes	See SPI section	SPI_STS
Software Generated GPE	Yes	Yes	SWGPE_EN=1	SWGPE_STS
USB Per-Port Registers Write Enable bit changes to 1	No	Yes	INTEL_USB2_EN=1, Write_Enable_SMI_Enable=1	INTEL_USB2_STS, Write Enable Status

Table 5-24. Causes of Intel® Scalable Memory Interconnect (Intel® SMI) and SCI (Sheet 3 of 3)

Cause	SCI	SMI	Additional Enables	Where Reported
GPIO Lockdown Enable bit changes from '1' to '0'	No	Yes	GPIO_UNLOCK_SMI_EN=1	GPIO_UNLOCK_SMI_STS
VE Host Interface	Yes	Yes	VEHCI_SCI_EN = 1 VEHCI_SMI_EN = 1	VEHCI_SCI_STS VEHCI_SMI_STS
VE Intel ME Interface	Yes	Yes	VEMCI_SCI_EN = 1 VEMCI_SMI_EN = 1	VEMCI_SCI_STS VEMCI_SMI_STS
Intel ME Interface	Yes	Yes	ME_SCI_EN = 1 ME_SMI_EN = 1	ME_SCI_STS ME_SMI_STS
Classic USB Legacy logic (Port 64/60 rd/wr, End of pass-through)	No	Yes	LEGACY_USB_EN = 1	LEGACY_USB_STS
RTC Update-in-progress	No	Yes	see I/O Trap Register section	RTC_UIP_SMI_STS

Notes:
1. SCI_EN must be 1 to enable SCI, except for BIOS_RLS. SCI_EN must be 0 to enable SMI.
2. SCI can be routed to cause interrupt 9:11 or 20:23 (20:23 only available in APIC mode).
3. GBL_SMI_EN must be 1 to enable SMI.
4. EOS must be written to 1 to re-enable Intel SMI for the next 1.
5. PCH must have Intel SMI fully enabled when PCH is also enabled to trap cycles. If Intel SMI is not enabled in conjunction with the trap enabling, then hardware behavior is undefined.
6. Only GPI[15:0] may generate an Intel SMI or SCI.
7. When a power button override first occurs, the system will transition immediately to S5. The SCI will only occur after the next wake to S0 if the residual status bit (PRBTNOR_STS) is not cleared prior to setting SCI_EN.
8. GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place.

5.14.4.1 PCI Express* SCI

PCI Express ports and the Processor (using DMI) have the ability to cause PME using messages. When a PME message is received, PCH will set the PCI_EXP_STS bit. If the PCI_EXP_EN bit is also set, the PCH can cause an SCI using the GPE1_STS register.

5.14.4.2 PCI Express* Hot-Plug

PCI Express has a Hot-Plug mechanism and is capable of generating a SCI using the GPE1 register. It is also capable of generating an Intel SMI. However, it is not capable of generating a wake event.

5.14.5 C-States

PCH-based systems implement C-states by having the Processor control the states. The chipset exchanges messages with the Processor as part of the C-state flow, but the chipset does not directly control any of the Processor impacts of C-states, such as voltage levels or Processor clocking. In addition to the new messages, the PCH also provides additional information to the Processor using a sideband pin (PM_SYNC). All of the legacy C-state related pins (STPCLK#, STP_CPU#, DPRSLP#, DPRSLPVR#, and so forth) do not exist on PCH.

5.14.6 Sleep States

5.14.6.1 Sleep State Overview

The PCH directly supports different sleep states (S1–S5), which are entered by methods such as setting the SLP_EN bit, or due to a Power Button press. The entry to the Sleep states is based on several assumptions:

- The G3 state cannot be entered using any software mechanism. The G3 state indicates a complete loss of power.

5.14.6.2 Initiating Sleep State

Sleep states (S1–S5) are initiated by:

- Masking interrupts, turning off all bus master enable bits, setting the desired type in the SLP_TYP field, and then setting the SLP_EN bit. The hardware then attempts to gracefully put the system into the corresponding Sleep state.
- Pressing the PWRBTN# Signal for more than 4 seconds to cause a Power Button Override event. In this case the transition to the S5 state is less graceful, since there are no dependencies on DMI messages from the processor or on clocks other than the RTC clock.
- Assertion of the THRMTRIP# signal will cause a transition to the S5 state. This can occur when system is in S0 or S1 state.
- Shutdown by integrated manageability functions (ASF)
- Internal watchdog timer timeout events

Table 5-25. Sleep Types

Sleep Type	Comment
S1	System lowers the processor's power consumption. No snooping is possible in this state.
S3	Asserts SLP_S3#. The SLP_S3# signal controls the power to non-critical circuits. Power is only retained to devices needed to wake from this sleeping state, as well as to the memory.
S4	Asserts SLP_S3# and SLP_S4#. The SLP_S4# signal shuts off the power to the memory subsystem. Only devices needed to wake from this state should be powered.
S5	Same power state as S4. asserts SLP_S3#, SLP_S4# and SLP_S5#.

5.14.6.3 Exiting Sleep States

Sleep states (S1–S5) are exited based on Wake events. The Wake events forces the system to a full on state (S0), although some non-critical subsystems might still be shut off and have to be brought back manually. For example, the hard disk may be shut off during a sleep state, and have to be enabled using a GPIO pin before it can be used.

Upon exit from software entered sleep states (that is, those initiated using the SLP_EN bit) the WAK_STS bit is set. The possible causes of Wake Events (and their restrictions) are shown in Table 5-26.

Table 5-26. Causes of Wake Events (Sheet 1 of 2)

Cause	How Enabled	Wake from S1, Sx	Wake from Deep S4/S5	Wake from S1, Sx After Power Loss (Note 1)	Wake from "Reset" Types (Note 2)
RTC Alarm	Set RTC_EN bit in PM1_EN register.	Y	Y	Y	
Power Button	Always enabled as Wake event.	Y	Y	Y	Y
GPI[15:0]	GPE0_EN register ***Note:*** GPI's that are in the core well are not capable of waking the system from sleep states when the core well is not powered.	Y			
GPIO27	Set GP27_EN in GPE0_EN Register.	Y	Y	Y	Y
LAN	Will use PME#. Wake enable set with LAN logic.	Y		Y	
RI#	Set RI_EN bit in GPE0_EN register.	Y		Y	
Intel® High Definition Audio	Event sets PME_B0_STS bit; PM_B0_EN must be enabled. Can not wake from S5 state if it was entered due to power failure or power button override.	Y		Y	
Primary PME#	PME_B0_EN bit in GPE0_EN register.	Y		Y	
Secondary PME#	Set PME_EN bit in GPE0_EN register.	Y		Y	
PCI_EXP_WAKE#	PCI_EXP_WAKE bit. (Note 3)	Y		Y	
SATA	Set PME_EN bit in GPE0_EN register. (Note 4)	S1		S1	
PCI_EXP PME Message	Must use the PCI Express* WAKE# pin rather than messages for wake from S3, S4, or S5.	S1		S1	
SMBALERT#	Always enabled as Wake event.	Y		Y	Y
SMBus Slave Wake Message (01h)	Wake/SMI# command always enabled as a Wake event. ***Note:*** SMBus Slave Message can wake the system from S1–S5, as well as from S5 due to Power Button Override.	Y		Y	Y

Table 5-26. Causes of Wake Events (Sheet 2 of 2)

Cause	How Enabled	Wake from S1, Sx	Wake from Deep S4/S5	Wake from S1, Sx After Power Loss (Note 1)	Wake from "Reset" Types (Note 2)
SMBus Host Notify message received	HOST_NOTIFY_WKEN bit SMBus Slave Command register. Reported in the SMB_WAK_STS bit in the GPEO_STS register.	Y		Y	Y
Intel® ME Non-Maskable Wake	Always enabled as a wake event.	Y		Y	Y
Integrated WOL Enable Override	WOL Enable Override bit (in Configuration Space).	Y		Y	Y

Notes:
1. This column represents what the PCH would honor as wake events but there may be enabling dependencies on the device side which are not enabled after a power loss.
2. Reset Types include: Power Button override, Intel ME initiated power button override, Intel ME initiated host partition reset with power down, Intel ME Watchdog Timer, SMBus unconditional power down, processor thermal trip, PCH catastrophic temperature event.
3. When the WAKE# pin is active and the PCI Express device is enabled to wake the system, the PCH will wake the platform.
4. SATA can only trigger a wake event in S1, but if PME is asserted prior to S3/S4/S5 entry and software does not clear the PME_B0_STS, a wake event would still result.

It is important to understand that the various GPIs have different levels of functionality when used as wake events. The GPIs that reside in the core power well can only generate wake events from sleep states where the core well is powered. Also, only certain GPIs are "ACPI Compliant," meaning that their Status and Enable bits reside in ACPI I/O space. Table 5-27 summarizes the use of GPIs as wake events.

Table 5-27. GPI Wake Events

GPI	Power Well	Wake From	Notes
GPI[7:0]	Core	S1	ACPI Compliant
GPI[15:8]	Suspend	S1–S5	ACPI Compliant

The latency to exit the various Sleep states varies greatly and is heavily dependent on power supply design, so much so that the exit latencies due to the PCH are insignificant.

5.14.6.4 PCI Express* WAKE# Signal and PME Event Message

PCI Express ports can wake the platform from any sleep state (S1, S3, S4, or S5) using the WAKE# pin. WAKE# is treated as a wake event, but does not cause any bits to go active in the GPE_STS register.

PCI Express ports and the processor (using DMI) have the ability to cause PME using messages. When a PME message is received, PCH will set the PCI_EXP_STS bit.

5.14.6.5 Sx-G3-Sx, Handling Power Failures

Depending on when the power failure occurs and how the system is designed, different transitions could occur due to a power failure.

The AFTERG3_EN bit provides the ability to program whether or not the system should boot once power returns after a power loss event. If the policy is to not boot, the system remains in an S5 state (unless previously in S4). There are only three possible events that will wake the system after a power failure.

1. **PWRBTN#:** PWRBTN# is always enabled as a wake event. When RSMRST# is low (G3 state), the PWRBTN_STS bit is reset. When the PCH exits G3 after power returns (RSMRST# goes high), the PWRBTN# signal is already high (because V_{CC}-standby goes high before RSMRST# goes high) and the PWRBTN_STS bit is 0.
2. **RI#:** RI# does not have an internal pull-up. Therefore, if this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit is set and the system interprets that as a wake event.
3. **RTC Alarm:** The RTC_EN bit is in the RTC well and is preserved after a power loss. Like PWRBTN_STS the RTC_STS bit is cleared when RSMRST# goes low.

The PCH monitors both PCH_PWROK and RSMRST# to detect for power failures. If PCH_PWROK goes low, the PWROK_FLR bit is set. If RSMRST# goes low, PWR_FLR is set.

Note: Although PME_EN is in the RTC well, this signal cannot wake the system after a power loss. PME_EN is cleared by RTCRST#, and PME_STS is cleared by RSMRST#.

Table 5-28. Transitions Due to Power Failure

State at Power Failure	AFTERG3_EN bit	Transition When Power Returns
S0, S1, S3	1 0	S5 S0
S4	1 0	S4 S0
S5	1 0	S5 S0
Deep S4/S5	1 0	Deep S4/S5[1] S0

Notes:
1. Entry state to Deep S4/S5 is preserved through G3 allowing resume from Deep S4/S5 to take appropriate path (that is, return to S4 or S5).

5.14.6.6 Deep S4/S5

To minimize power consumption while in S4/S5, the PCH supports a lower power, lower featured version of these power states known as Deep S4/S5. In these Deep S4/S5 states, the Suspend wells are powered off, while the new Deep S4/S5 Well (DSW) remains powered. A limited set of wake events are supported by the logic located in the DSW.

5.14.6.6.1 Entry Into Deep S4/S5

A combination of conditions is required for entry into Deep S4/S5.

All of the following must be met:

— Intel ME in Moff

— AND ((DPS4_EN_AC AND S4) OR (DPS5_EN_AC AND S5)

Table 5-29. Supported Deep S4/S5 Policy Configurations

Configuration	DPS4_EN_DC	DPS4_EN_AC	DPS5_EN_DC	DPS5_EN_AC
1: Enabled in S5	0	0	1	1
2: Enabled in S4 and S5	1	1	1	1
3: Deep S4 / S5 disabled	0	0	0	0

The PCH also performs a SUSWARN#/SUSACK# handshake to ensure the platform is ready to enter Deep S4/S5. The PCH asserts SUSWARN# as notification that it is about to enter Deep S4/S5. Before the PCH proceeds and asserts SLP_SUS#, the PCH waits for SUSACK# to assert.

5.14.6.6.2 Exit from Deep S4/S5

While in Deep S4/S5, the PCH monitors and responds to a limited set of wake events (RTC Alarm, Power Button, and GPIO27). Upon sensing an enabled Deep S4/S5 wake event, the PCH brings up the Suspend well by deasserting SLP_SUS#.

Table 5-30. Deep S4/S5 Wake Events

Event	Enable
RTC Alarm	RTC_DS_WAKE_DIS (RCBA+3318h:Bit 21)
Power Button	Always enabled
GPIO27	GPIO27_EN (PMBASE+28h:Bit 35)

5.14.7 Event Input Signals and Their Usage

The PCH has various input signals that trigger specific events. This section describes those signals and how they should be used.

5.14.7.1 PWRBTN# (Power Button)

The PCH PWRBTN# signal operates as a "Fixed Power Button" as described in the *Advanced Configuration and Power Interface, Version 2.0b.* PWRBTN# signal has a 16 ms de-bounce on the input. The state transition descriptions are included in Table 5-31. The transitions start as soon as the PWRBTN# is pressed (but after the debounce logic), and does not depend on when the Power Button is released.

Note: During the time that the SLP_S4# signal is stretched for the minimum assertion width (if enabled), the Power Button is not a wake event. Refer to the following Power Button Override Function section for further detail.

Table 5-31. Transitions Due to Power Button

Present State	Event	Transition / Action	Comment
S0/Cx	PWRBTN# goes low	Intel SMI or SCI generated (depending on SCI_EN, PWRBTN_EN and GLB_SMI_EN)	Software typically initiates a Sleep state
S1–S5	PWRBTN# goes low	Wake Event. Transitions to S0 state	Standard wakeup
G3	PWRBTN# pressed	None	No effect since no power Not latched nor detected
S0–S4	PWRBTN# held low for at least 4 consecutive seconds	Unconditional transition to S5 state	No dependence on processor (DMI Messages) or any other subsystem

Power Button Override Function

If PWRBTN# is observed active for at least four consecutive seconds, the state machine should unconditionally transition to the G2/S5 state, regardless of present state (S0–S4), even if the PCH_PWROK is not active. In this case, the transition to the G2/S5 state should not depend on any particular response from the processor (such as, a DMI Messages), nor any similar dependency from any other subsystem.

The PWRBTN# status is readable to check if the button is currently being pressed or has been released. The status is taken after the de-bounce, and is readable using the PWRBTN_LVL bit.

Note: The 4-second PWRBTN# assertion should only be used if a system lock-up has occurred. The 4-second timer starts counting when the PCH is in a S0 state. If the PWRBTN# signal is asserted and held active when the system is in a suspend state (S1–S5), the assertion causes a wake event. Once the system has resumed to the S0 state, the 4-second timer starts.

Note: During the time that the SLP_S4# signal is stretched for the minimum assertion width (if enabled by D31:F0:A4h bit 3), the Power Button is not a wake event. As a result, it is conceivable that the user will press and continue to hold the Power Button waiting for the system to awake. Since a 4-second press of the Power Button is already defined as an Unconditional Power down, the power button timer will be forced to inactive while the power-cycle timer is in progress. Once the power-cycle timer has expired, the Power Button awakes the system. Once the minimum SLP_S4# power cycle expires, the Power Button must be pressed for another 4 to 5 seconds to create the Override condition to S5.

Sleep Button

The *Advanced Configuration and Power Interface, Version 2.0b* defines an optional Sleep button. It differs from the power button in that it only is a request to go from S0 to S1–S4 (not S5). Also, in an S5 state, the Power Button can wake the system, but the Sleep Button cannot.

Although the PCH does not include a specific signal designated as a Sleep Button, one of the GPIO signals can be used to create a "Control Method" Sleep Button. See the *Advanced Configuration and Power Interface, Version 2.0b* for implementation details.

5.14.7.2 RI# (Ring Indicator)

The Ring Indicator can cause a wake event (if enabled) from the S1–S5 states. Table 5-32 shows when the wake event is generated or ignored in different states. If in the G0/S0/Cx states, the PCH generates an interrupt based on RI# active, and the interrupt will be set up as a Break event.

Table 5-32. Transitions Due to RI# Signal

Present State	Event	RI_EN	Event
S0	RI# Active	X	Ignored
S1–S5	RI# Active	0 1	Ignored Wake Event

Note: Filtering/Debounce on RI# will not be done in PCH. Can be in modem or external.

5.14.7.3 PME# (PCI Power Management Event)

The PME# signal comes from a PCI device to request that the system be restarted. The PME# signal can generate an SMI#, SCI, or optionally a Wake event. The event occurs when the PME# signal goes from high to low. No event is caused when it goes from low to high.

There is also an internal PME_B0 bit. This is separate from the external PME# signal and can cause the same effect.

5.14.7.4 SYS_RESET# Signal

When the SYS_RESET# pin is detected as active after the 16 ms debounce logic, the PCH attempts to perform a "graceful" reset, by waiting up to 25 ms for the SMBus to go idle. If the SMBus is idle when the pin is detected active, the reset occurs immediately; otherwise, the counter starts. If at any point during the count the SMBus goes idle the reset occurs. If, however, the counter expires and the SMBus is still active, a reset is forced upon the system even though activity is still occurring.

Once the reset is asserted, it remains asserted for 5 to 6 ms regardless of whether the SYS_RESET# input remains asserted or not. It cannot occur again until SYS_RESET# has been detected inactive after the debounce logic, and the system is back to a full S0 state with PLTRST# inactive. If bit 3 of the CF9h I/O register is set then SYS_RESET# will result in a full power cycle reset.

5.14.7.5 THRMTRIP# Signal

If THRMTRIP# goes active, the processor is indicating an overheat condition, and the PCH immediately transitions to an S5 state, driving SLP_S3#, SLP_S4#, SLP_S5# low, and setting the CTS bit. The transition looks like a power button override.

When a THRMTRIP# event occurs, the PCH will power down immediately without following the normal S0 -> S5 path. The PCH will immediately drive SLP_S3#, SLP_S4#, and SLP_S5# low after sampling THRMTRIP# active.

If the processor is running extremely hot and is heating up, it is possible (although very unlikely) that components around it, such as the PCH, are no longer executing cycles properly. Therefore, if THRMTRIP# goes active, and the PCH is relying on state machine logic to perform the power down, the state machine may not be working, and the system will not power down.

The PCH provides filtering for short low glitches on the THRMTRIP# signal in order to prevent erroneous system shut downs from noise. Glitches shorter than 25 nsec are ignored.

During boot, THRMTRIP# is ignored until SLP_S3#, PCH_PWROK, and PLTRST# are all '1'. During entry into a powered-down state (due to S3, S4, S5 entry, power cycle reset, etc.) THRMTRIP# is ignored until either SLP_S3# = 0, or PCH_PWROK = 0, or SYS_PWROK= 0.

Note: A thermal trip event will:

- Clear the PWRBTN_STS bit
- Clear all the GPE0_EN register bits
- Clear the SMB_WAK_STS bit only if SMB_SAK_STS was set due to SMBus slave receiving message and not set due to SMBAlert

5.14.8 ALT Access Mode

Before entering a low power state, several registers from powered down parts may need to be saved. In the majority of cases, this is not an issue, as registers have read and write paths. However, several of the ISA compatible registers are either read only or write only. To get data out of write-only registers, and to restore data into read-only registers, the PCH implements an ALT access mode.

If the ALT access mode is entered and exited after reading the registers of the PCH timer (8254), the timer starts counting faster (13.5 ms). The following steps listed below can cause problems:

1. BIOS enters ALT access mode for reading the PCH timer related registers.
2. BIOS exits ALT access mode.
3. BIOS continues through the execution of other needed steps and passes control to the operating system.

After getting control in step #3, if the operating system does not reprogram the system timer again, the timer ticks may be happening faster than expected. For example Microsoft MS-DOS* and its associated software assume that the system timer is running at 54.6 ms and as a result the time-outs in the software may be happening faster than expected.

Operating systems (for example, Microsoft Windows* 98 and Windows* 2000) reprogram the system timer and therefore do not encounter this problem.

For other operating systems (for example, Microsoft MS-DOS*) the BIOS should restore the timer back to 54.6 ms before passing control to the operating system. If the BIOS is entering ALT access mode before entering the suspend state it is not necessary to restore the timer contents after the exit from ALT access mode.

5.14.8.1 Write Only Registers with Read Paths in ALT Access Mode

The registers described in Table 5-33 have read paths in ALT access mode. The access number field in the table indicates which register will be returned per access to that port.

Table 5-33. Write Only Registers with Read Paths in ALT Access Mode (Sheet 1 of 2)

Restore Data				Restore Data			
I/O Addr	# of Rds	Access	Data	I/O Addr	# of Rds	Access	Data
00h	2	1	DMA Chan 0 base address low byte	40h	7	1	Timer Counter 0 status, bits [5:0]
		2	DMA Chan 0 base address high byte			2	Timer Counter 0 base count low byte
01h	2	1	DMA Chan 0 base count low byte			3	Timer Counter 0 base count high byte
		2	DMA Chan 0 base count high byte			4	Timer Counter 1 base count low byte
02h	2	1	DMA Chan 1 base address low byte			5	Timer Counter 1 base count high byte
		2	DMA Chan 1 base address high byte			6	Timer Counter 2 base count low byte
03h	2	1	DMA Chan 1 base count low byte			7	Timer Counter 2 base count high byte
		2	DMA Chan 1 base count high byte	41h	1		Timer Counter 1 status, bits [5:0]
04h	2	1	DMA Chan 2 base address low byte	42h	1		Timer Counter 2 status, bits [5:0]
		2	DMA Chan 2 base address high byte	70h	1		Bit 7 = NMI Enable, Bits [6:0] = RTC Address
05h	2	1	DMA Chan 2 base count low byte	C4h	2	1	DMA Chan 5 base address low byte
		2	DMA Chan 2 base count high byte			2	DMA Chan 5 base address high byte
06h	2	1	DMA Chan 3 base address low byte	C6h	2	1	DMA Chan 5 base count low byte
		2	DMA Chan 3 base address high byte			2	DMA Chan 5 base count high byte
07h	2	1	DMA Chan 3 base count low byte	C8h	2	1	DMA Chan 6 base address low byte
		2	DMA Chan 3 base count high byte			2	DMA Chan 6 base address high byte
08h	6	1	DMA Chan 0–3 Command[2]	CAh	2	1	DMA Chan 6 base count low byte
		2	DMA Chan 0–3 Request			2	DMA Chan 6 base count high byte
		3	DMA Chan 0 Mode: Bits(1:0) = 00	CCh	2	1	DMA Chan 7 base address low byte
		4	DMA Chan 1 Mode: Bits(1:0) = 01			2	DMA Chan 7 base address high byte
		5	DMA Chan 2 Mode: Bits(1:0) = 10	CEh	2	1	DMA Chan 7 base count low byte
		6	DMA Chan 3 Mode: Bits(1:0) = 11.			2	DMA Chan 7 base count high byte

Table 5-33. Write Only Registers with Read Paths in ALT Access Mode (Sheet 2 of 2)

Restore Data				Restore Data			
I/O Addr	# of Rds	Access	Data	I/O Addr	# of Rds	Access	Data
20h	12	1	PIC ICW2 of Master controller	D0h	6	1	DMA Chan 4–7 Command[2]
		2	PIC ICW3 of Master controller			2	DMA Chan 4–7 Request
		3	PIC ICW4 of Master controller			3	DMA Chan 4 Mode: Bits(1:0) = 00
		4	PIC OCW1 of Master controller[1]			4	DMA Chan 5 Mode: Bits(1:0) = 01
		5	PIC OCW2 of Master controller			5	DMA Chan 6 Mode: Bits(1:0) = 10
		6	PIC OCW3 of Master controller			6	DMA Chan 7 Mode: Bits(1:0) = 11.
		7	PIC ICW2 of Slave controller				
		8	PIC ICW3 of Slave controller				
		9	PIC ICW4 of Slave controller				
		10	PIC OCW1 of Slave controller[1]				
		11	PIC OCW2 of Slave controller				
		12	PIC OCW3 of Slave controller				

Notes:
1. The OCW1 register must be read before entering ALT access mode.
2. Bits 5, 3, 1, and 0 return 0.

5.14.8.2 PIC Reserved Bits

Many bits within the PIC are reserved, and must have certain values written in order for the PIC to operate properly. Therefore, there is no need to return these values in ALT access mode. When reading PIC registers from 20h and A0h, the reserved bits shall return the values listed in Table 5-34.

Table 5-34. PIC Reserved Bits Return Values

PIC Reserved Bits	Value Returned
ICW2(2:0)	000
ICW4(7:5)	000
ICW4(3:2)	00
ICW4(0)	0
OCW2(4:3)	00
OCW3(7)	0
OCW3(5)	Reflects bit 6
OCW3(4:3)	01

5.14.8.3 Read Only Registers with Write Paths in ALT Access Mode

The registers described in Table 5-35 have write paths to them in ALT access mode. Software restores these values after returning from a powered down state. These registers must be handled special by software. When in normal mode, writing to the base address/count register also writes to the current address/count register. Therefore, the base address/count must be written first, then the part is put into ALT access mode and the current address/count register is written.

Table 5-35. Register Write Accesses in ALT Access Mode

I/O Address	Register Write Value
08h	DMA Status Register for channels 0–3.
D0h	DMA Status Register for channels 4–7.

5.14.9 System Power Supplies, Planes, and Signals

5.14.9.1 Power Plane Control with SLP_S3#, SLP_S4#, SLP_S5#, SLP_A# and SLP_LAN#

The SLP_S3# output signal can be used to cut power to the system core supply, since it only goes active for the Suspend-to-RAM state (typically mapped to ACPI S3). Power must be maintained to the PCH suspend well, and to any other circuits that need to generate Wake signals from the Suspend-to-RAM state. During S3 (Suspend-to-RAM) all signals attached to powered down plans will be tri-stated or driven low, unless they are pulled using a pull-up resistor.

Cutting power to the core may be done using the power supply, or by external FETs on the motherboard.

The SLP_S4# or SLP_S5# output signal can be used to cut power to the system core supply, as well as power to the system memory, since the context of the system is saved on the disk. Cutting power to the memory may be done using the power supply, or by external FETs on the motherboard.

The SLP_S4# output signal is used to remove power to additional subsystems that are powered during SLP_S3#.

SLP_S5# output signal can be used to cut power to the system core supply, as well as power to the system memory, since the context of the system is saved on the disk. Cutting power to the memory may be done using the power supply, or by external FETs on the motherboard.

SLP_A# output signal can be used to cut power to the Intel ME, Clock chip and SPI flash on a platform that supports the M3 state.

SLP_LAN# output signal can be used to cut power to the external Intel 82579 Gbe PHY device.

5.14.9.2 SLP_S4# and Suspend-To-RAM Sequencing

The system memory suspend voltage regulator is controlled by the Glue logic. The SLP_S4# signal should be used to remove power to system memory rather than the SLP_S5# signal. The SLP_S4# logic in the PCH provides a mechanism to fully cycle the power to the DRAM and/or detect if the power is not cycled for a minimum time.

Note: To utilize the minimum DRAM power-down feature that is enabled by the SLP_S4# Assertion Stretch Enable bit (D31:F0:A4h bit 3), the DRAM power must be controlled by the SLP_S4# signal.

5.14.9.3 PCH_PWROK Signal

When asserted, PCH_PWROK is an indication to the PCH that its core well power rails have been powered and stable. PCH_PWROK can be driven asynchronously. When PCH_PWROK is low, the PCH asynchronously asserts PLTRST#. PCH_PWROK must not glitch, even if RSMRST# is low.

It is required that the power associated with PCI/PCIe have been valid for 99 ms prior to PCH_PWROK assertion in order to comply with the 100 ms PCI 2.3 / PCIe 1.1 specification on PLTRST# deassertion.

Note: SYS_RESET# is recommended for implementing the system reset button. This saves external logic that is needed if the PCH_PWROK input is used. Additionally, it allows for better handling of the SMBus and processor resets and avoids improperly reporting power failures.

5.14.9.4 SLP_LAN# Pin Behavior

The following table summarizes SLP_LAN# pin behavior.

Table 5-36. SLP_LAN# Pin Behavior

Pin Functionality (Determined by soft strap)	SLP_LAN Default Value Bit	GPIO29 Input / Output (Determined by GP_IO_SEL bit)	Pin Value In S0 or M3	Value in S3-S5/ Moff
SLP_LAN#	0 (Default)	In (Default)	1	0
		Out	1	Depends on GPIO29 output data value
	1	In (Default)	1	1
		Out	1	Depends on GPIO29 output data value
GPIO29	0 (Default)	In	Z (tri-state)	0
	1	In	Z (tri-state)	1
	N/A	Out	Depends on GPIO29 output data value	Depends on GPIO29 output data value

5.14.9.5 RTCRST# and SRTCRST#

RTCRST# is used to reset PCH registers in the RTC Well to their default value. If a jumper is used on this pin, it should only be pulled low when system is in the G3 state and then replaced to the default jumper position. Upon booting, BIOS should recognize that RTCRST# was asserted and clear internal PCH registers accordingly. It is imperative that this signal not be pulled low in the S0 to S5 states.

SRTCRST# is used to reset portions of the Intel Manageability Engine and should not be connected to a jumper or button on the platform. The only time this signal gets asserted (driven low in combination with RTCRST#) should be when the coin cell battery is removed or not installed and the platform is in the G3 state. Pulling this signal low independently (without RTCRST# also being driven low) may cause the platform to enter an indeterminate state. Similar to RTCRST#, it is imperative that SRTCRST# not be pulled low in the S0 to S5 states.

See Table 2-2 that demonstrates the proper circuit connection of these pins.

5.14.10 Legacy Power Management Theory of Operation

Instead of relying on ACPI software, legacy power management uses BIOS and various hardware mechanisms. The scheme relies on the concept of detecting when individual subsystems are idle, detecting when the whole system is idle, and detecting when accesses are attempted to idle subsystems.

However, the operating system is assumed to be at least APM enabled. Without APM calls, there is no quick way to know when the system is idle between keystrokes. The PCH does not support burst modes.

5.14.10.1 APM Power Management

The PCH has a timer that, when enabled by the 1MIN_EN bit in the Intel SMI Control and Enable register, generates an Intel SMI once per minute. The Intel SMI handler can check for system activity by reading the DEVTRAP_STS register. If none of the system bits are set, the Intel SMI handler can increment a software counter. When the counter reaches a sufficient number of consecutive minutes with no activity, the Intel SMI handler can then put the system into a lower power state.

If there is activity, various bits in the DEVTRAP_STS register will be set. Software clears the bits by writing a 1 to the bit position.

The DEVTRAP_STS register allows for monitoring various internal devices, or Super I/O devices (SP, PP, FDC) on LPC or PCI, keyboard controller accesses, or audio functions on LPC or PCI. Other PCI activity can be monitored by checking the PCI interrupts.

5.14.11 Reset Behavior

When a reset is triggered, the PCH will send a warning message to the Processor to allow the Processor to attempt to complete any outstanding memory cycles and put memory into a safe state before the platform is reset. When the Processor is ready, it will send an acknowledge message to the PCH. Once the message is received the PCH asserts PLTRST#.

The PCH does not require an acknowledge message from the processor to trigger PLTRST#. A global reset will occur after 4 seconds if an acknowledge from the processor is not received.

When the PCH causes a reset by asserting PLTRST# its output signals will go to their reset states as defined in Chapter 3.

A reset in which the host platform is reset and PLTRST# is asserted is called a Host Reset or Host Partition Reset. Depending on the trigger a host reset may also result in power cycling see Table 5-37 for details. If a host reset is triggered and the PCH times out before receiving an acknowledge message from the Processor a Global Reset with power cycle will occur.

A reset in which the host and Intel ME partitions of the platform are reset is called a Global Reset. During a Global Reset, all PCH functionality is reset except RTC Power Well backed information and Suspend well status, configuration, and functional logic for controlling and reporting the reset. Intel ME and Host power back up after the power cycle period.

Straight to S5 is another reset type where all power wells that are controlled by the SLP_S3#, SLP_S4#, and SLP_A# pins, as well as SLP_S5# and SLP_LAN# (if pins are not configured as GPIOs), are turned off. All PCH functionality is reset except RTC Power Well backed information and Suspend well status, configuration, and functional logic for controlling and reporting the reset. The host stays there until a valid wake event occurs.

Table 5-37 shows the various reset triggers:

Table 5-37. Causes of Host and Global Resets

Trigger	Host Reset without Power Cycle[1]	Host Reset with Power Cycle[2]	Global Reset with Power Cycle[3]	Straight to S5 (Host Stays there)
Write of 0Eh to CF9h (RST_CNT Register) when CF9h Global Reset Bit=0b	No	Yes	No (Note 4)	
Write of 06h to CF9h (RST_CNT Register) when CF9h Global Reset Bit=0b	Yes	No	No (Note 4)	
Write of 06h or 0Eh to CF9h (RST_CNT Register) when CF9h Global Reset Bit=1b	No	No	Yes	
SYS_RESET# Asserted and CF9h (RST_CNT Register) Bit 3 = 0	Yes	No	No (Note 4)	
SYS_RESET# Asserted and CF9h (RST_CNT Register) Bit 3 = 1	No	Yes	No (Note 4)	
SMBus Slave Message received for Reset with Power Cycle	No	Yes	No (Note 4)	
SMBus Slave Message received for Reset without Power Cycle	Yes	No	No (Note 4)	
SMBus Slave Message received for unconditional Power Down	No	No	No	Yes
TCO Watchdog Timer reaches zero two times	Yes	No	No (Note 4)	
Power Failure: PWROK signal goes inactive in S0/S1 or DPWROK drops	No	No	Yes	
SYS_PWROK Failure: SYS_PWROK signal goes inactive in S0/S1	No	No	Yes	
Processor Thermal Trip (THRMTRIP#) causes transition to S5 and reset asserts	No	No	No	Yes
PCH internal thermal sensors signals a catastrophic temperature condition	No	No	No	Yes
Power Button 4 second override causes transition to S5 and reset asserts	No	No	No	Yes
Special shutdown cycle from processor causes CF9h-like PLTRST# and CF9h Global Reset Bit = 1	No	No	Yes	
Special shutdown cycle from processor causes CF9h-like PLTRST# and CF9h Global Reset Bit = 0 and CF9h (RST_CNT Register) Bit 3 = 1	No	Yes	No (Note 4)	
Special shutdown cycle from processor causes CF9h-like PLTRST# and CF9h Global Reset Bit = 0 and CF9h (RST_CNT Register) Bit 3 = 0	Yes	No	No (Note 4)	
Intel ME Triggered Host Reset without power cycle	Yes	No	No (Note 4)	
Intel ME Triggered Host Reset with power cycle	No	Yes	No (Note 4)	
Intel ME Triggered Power Button Override	No	No	No	Yes
Intel ME Watchdog Timer Timeout	No	No	No	Yes
Intel ME Triggered Global Reset	No	No	Yes	
Intel ME Triggered Host Reset with power down (host stays there)	No	Yes (Note 5)	No (Note 4)	
PLTRST# Entry Time-out	No	No	Yes	
S3/4/5 Entry Timeout	No	No	No	Yes
PROCPWRGD Stuck Low	No	No	Yes	
Power Management Watchdog Timer	No	No	No	Yes
Intel ME Hardware Uncorrectable Error	No	No	No	Yes

Notes:

1. The PCH drops this type of reset request if received while the system is in S3/S4/S5.
2. PCH does not drop this type of reset request if received while system is in a software-entered S3/S4/S5 state. However, the PCH is allowed to perform the reset without executing the RESET_WARN protocol in these states.
3. The PCH does not send warning message to processor, reset occurs without delay.
4. Trigger will result in Global Reset with power cycle if the acknowledge message is not received by the PCH.
5. The PCH waits for enabled wake event to complete reset.

5.15 System Management (D31:F0)

The PCH provides various functions to make a system easier to manage and to lower the Total Cost of Ownership (TCO) of the system. Features and functions can be augmented using external A/D converters and GPIO, as well as an external microcontroller.

The following features and functions are supported by the PCH:

- Processor present detection
  - Detects if processor fails to fetch the first instruction after reset
- Various Error detection (such as ECC Errors) indicated by host controller
  - Can generate SMI#, SCI, SERR, NMI, or TCO interrupt
- Intruder Detect input
  - Can generate TCO interrupt or SMI# when the system cover is removed
  - INTRUDER# allowed to go active in any power state, including G3
- Detection of bad BIOS Flash (FWH or Flash on SPI) programming
  - Detects if data on first read is FFh (indicates that BIOS flash is not programmed)
- Ability to hide a PCI device
  - Allows software to hide a PCI device in terms of configuration space through the use of a device hide register. (See Section 10.1.44)

Note: Voltage ID from the processor can be read using GPI signals.

5.15.1 Theory of Operation

The System Management functions are designed to allow the system to diagnose failing subsystems. The intent of this logic is that some of the system management functionality can be provided without the aid of an external microcontroller.

5.15.1.1 Detecting a System Lockup

When the processor is reset, it is expected to fetch its first instruction. If the processor fails to fetch the first instruction after reset, the TCO timer times out twice and the PCH asserts PLTRST#.

5.15.1.2 Handling an Intruder

The PCH has an input signal, INTRUDER#, that can be attached to a switch that is activated by the system's case being open. This input has a two RTC clock debounce. If INTRUDER# goes active (after the debouncer), this will set the INTRD_DET bit in the TCO2_STS register. The INTRD_SEL bits in the TCO_CNT register can enable the PCH to cause an SMI# or interrupt. The BIOS or interrupt handler can then cause a transition to the S5 state by writing to the SLP_EN bit.

The software can also directly read the status of the INTRUDER# signal (high or low) by clearing and then reading the INTRD_DET bit. This allows the signal to be used as a GPI if the intruder function is not required.

If the INTRUDER# signal goes inactive some point after the INTRD_DET bit is written as a 1, then the INTRD_DET signal will go to a 0 when INTRUDER# input signal goes inactive. This is slightly different than a classic sticky bit, since most sticky bits would remain active indefinitely when the signal goes active and would immediately go inactive when a 1 is written to the bit.

Note: The INTRD_DET bit resides in the PCH's RTC well, and is set and cleared synchronously with the RTC clock. Thus, when software attempts to clear INTRD_DET (by writing a 1 to the bit location) there may be as much as two RTC clocks (about 65 µs) delay before the bit is actually cleared. Also, the INTRUDER# signal should be asserted for a minimum of 1 ms to ensure that the INTRD_DET bit will be set.

Note: If the INTRUDER# signal is still active when software attempts to clear the INTRD_DET bit, the bit remains set and the Intel SMI is generated again immediately. The Intel SMI handler can clear the INTRD_SEL bits to avoid further Intel SMIs. However, if the INTRUDER# signal goes inactive and then active again, there will not be further Intel SMIs, since the INTRD_SEL bits would select that no SMI# be generated.

5.15.1.3 Detecting Improper Flash Programming

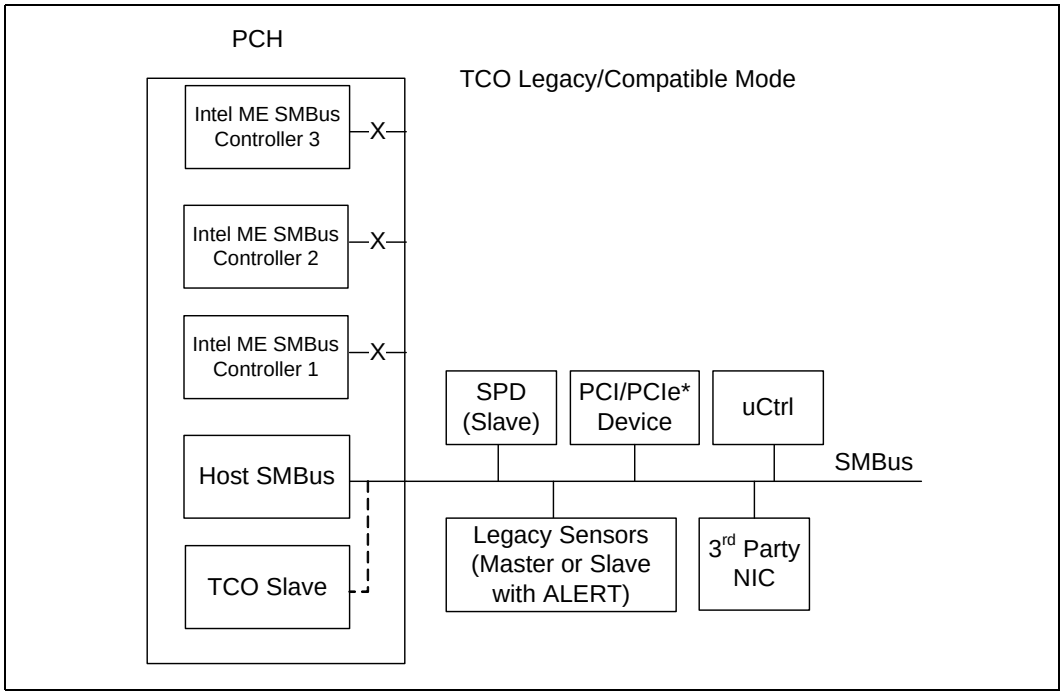
The PCH can detect the case where the BIOS flash is not programmed. This results in the first instruction fetched to have a value of FFh. If this occurs, the PCH sets the BAD_BIOS bit. The BIOS flash may reside in FWH or flash on the SPI bus.

5.15.2 TCO Modes

5.15.2.1 TCO Legacy/Compatible Mode

In TCO Legacy/Compatible mode, only the host SMBus is used. The TCO Slave is connected to the host SMBus internally by default. In this mode, the Intel ME SMBus controllers are not used and should be disabled by soft strap.

Figure 5-4. TCO Legacy/Compatible Mode SMBus Configuration



In TCO Legacy/Compatible mode the PCH can function directly with an external LAN controller or equivalent external LAN controller to report messages to a network management console without the aid of the system processor. This is crucial in cases where the processor is malfunctioning or cannot function due to being in a low-power state. Table 5-38 includes a list of events that will report messages to the network management console.

Table 5-38. Event Transitions that Cause Messages

Event	Assertion?	Deassertion?	Comments
INTRUDER# pin	yes	no	Must be in "S1 or hung S0" state
THRM# pin	yes	yes	Must be in "S1 or hung S0" state. The THRM# pin is isolated when the core power is off, thus preventing this event in S3-S5.
Watchdog Timer Expired	yes	no (NA)	"S1 or hung S0" state entered
GPIO[11]/SMBALERT# pin	yes	yes	Must be in "S1 or hung S0" state
BATLOW#	yes	yes	Must be in "S1 or hung S0" state
CPU_PWR_FLR	yes	no	"S1 or hung S0" state entered

Note: The GPIO11/SMBALERT# pin will trigger an event message (when enabled by the GPIO11_ALERT_DISABLE bit) regardless of whether it is configured as a GPI or not.

5.15.2.2 Advanced TCO Mode

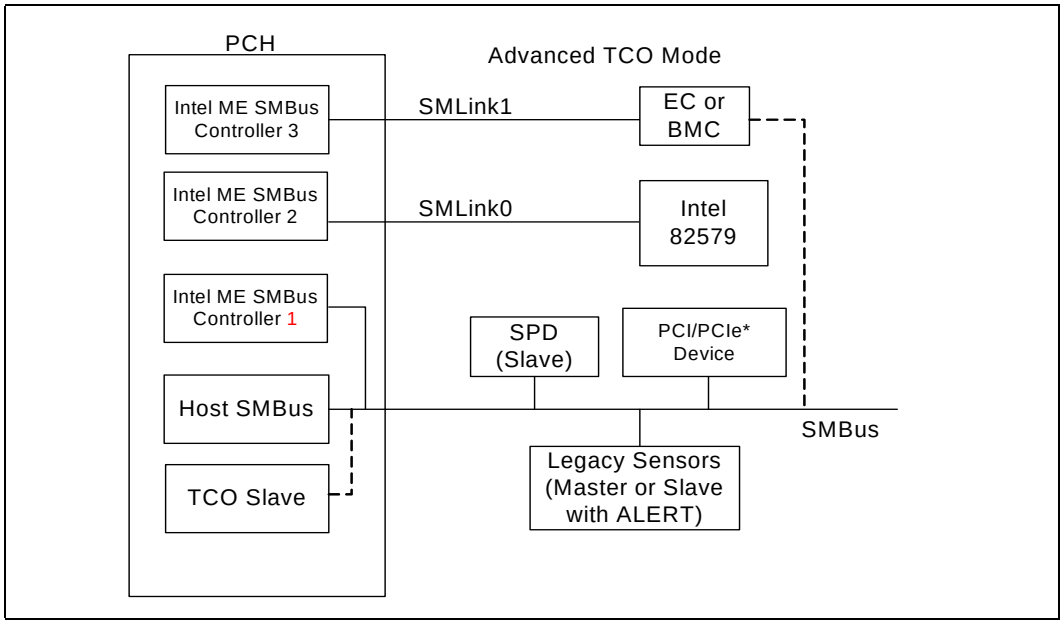
PCH supports the Advanced TCO mode in which SMLink0 and SMLink1 are used in addition to the host SMBus. See Figure 5-5 for more details. In this mode, the Intel ME SMBus controllers must be enabled by soft strap (*TCO Slave Select) in the flash descriptor.

The SMLink0 is dedicated to integrated LAN use and when an Intel PHY 82579 is connected to SMLink0, a soft strap must be set to indicate that the PHY is connected to SMLink0. The interface will be running at the frequency of 300 KHz – 400 KHz depending on different factors such as board routing or bus loading when the Fast Mode is enabled using a soft strap.

Note: With Westerlee FW, SMLink0 can also be used with BMC. However, this precludes use of the Intel PHY 82579.

SMLink1 is dedicated to Embedded Controller (EC) or Baseboard Management Controller (BMC) use. In the case where a BMC is connected to SMLink1, the BMC communicates with Intel ME through Intel ME SMBus connected to SMLink1. The host and TCO slave communicated with BMC through SMBus.

Figure 5-5. Advanced TCO Mode



5.16 General Purpose I/O (D31:F0)

The PCH contains up to 70 General Purpose Input/Output (GPIO) signals. Each GPIO can be configured as an input or output signal. The number of inputs and outputs varies depending on the configuration. Below is a brief summary of new GPIO features.

- Capability to mask Suspend well GPIOs from CF9h events configured using GP_RST_SEL registers)
- Added capability to program GPIO prior to switching to output

5.16.1 Power Wells

Some GPIOs exist in the suspend power plane. Care must be taken to make sure GPIO signals are not driven high into powered-down planes. Some PCH GPIOs may be connected to pins on devices that exist in the core well. If these GPIOs are outputs, there is a danger that a loss of core power (PCH_PWROK low) or a Power Button Override event results in PCH driving a pin to a logic 1 to another device that is powered down.

5.16.2 SMI# SCI and NMI Routing

The routing bits for GPIO[15:0] allow an input to be routed to SMI#, SCI, NMI or neither. A bit can be routed to either an SMI# or an SCI, but not both.

5.16.3 Triggering

GPIO[15:0] have “sticky” bits on the input. Refer to the GPE0_STS register and the ALT_GPI_SMI_STS register. As long as the signal goes active for at least 2 clock cycles, the PCH keeps the sticky status bit active. The active level can be selected in the GP_INV register. This does not apply to GPI_NMI_STS residing in GPIO IO space.

If the system is in an S0 or an S1 state, the GPI inputs are sampled at 33 MHz, so the signal only needs to be active for about 60 ns to be latched. In the S3–S5 states, the GPI inputs are sampled at 32.768 kHz, and thus must be active for at least 61 microseconds to be latched.

Note: GPIs that are in the core well are not capable of waking the system from sleep states where the core well is not powered.

If the input signal is still active when the latch is cleared, it will again be set. Another edge trigger is not required. This makes these signals "level" triggered inputs.

5.16.4 GPIO Registers Lockdown

The following GPIO registers are locked down when the GPIO Lockdown Enable (GLE) bit is set. The GLE bit resides in D31:F0:GPIO Control (GC) register.

- Offset 00h: GPIO_USE_SEL[31:0]
- Offset 04h: GP_IO_SEL[31:0]
- Offset 0Ch: GP_LVL[31:0]
- Offset 28h: GPI_NMI_EN[15:0]
- Offset 2Ch: GPI_INV[31:0]
- Offset 30h: GPIO_USE_SEL2[63:32]
- Offset 34h: GPI_IO_SEL2[63:32]
- Offset 38h: GP_LVL2[63:32]
- Offset 40h: GPIO_USE_SEL3[95:64]
- Offset 44h: GPI_IO_SEL3[95:64]
- Offset 48h: GP_LVL3[95:64]
- Offset 60h: GP_RST_SEL[31:0]
- Offset 64h: GP_RST_SEL2[63:32]
- Offset 68h: GP_RST_SEL3[95:64]

Once these registers are locked down, they become Read-Only registers and any software writes to these registers will have no effect. To unlock the registers, the GPIO Lockdown Enable (GLE) bit is required to be cleared to '0'. When the GLE bit changes from a '1' to a '0' a System Management Interrupt (SMI#) is generated if enabled. Once the GPIO_UNLOCK_SMI bit is set, it can not be changed until a PLTRST# occurs. This ensures that only BIOS can change the GPIO configuration. If the GLE bit is cleared by unauthorized software, BIOS will set the GLE bit again when the SMI# is triggered and these registers will continue to be locked down.

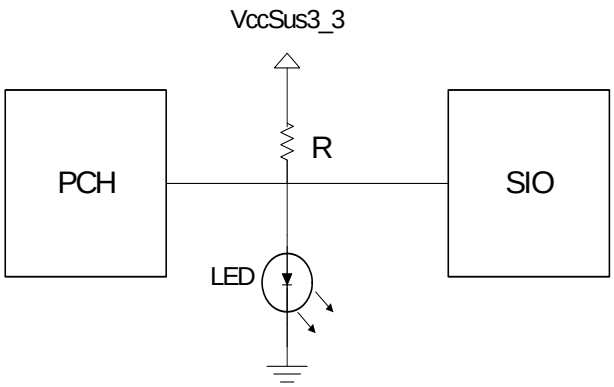
5.16.5 Serial POST Codes over GPIO

PCH adds the extended capability allowing system software to serialize POST or other messages on GPIO. This capability negates the requirement for dedicated diagnostic LEDs on the platform. Additionally, based on the newer BTX form factors, the PCI bus as a target for POST codes is increasingly difficult to support as the total number of PCI devices supported are decreasing.

5.16.5.1 Theory of Operation

For the PCH generation POST code serialization logic will be shared with GPIO. These GPIOs will likely be shared with LED control offered by the Super I/O (SIO) component. Figure 5-6 shows a likely configuration.

Figure 5-6. Serial Post over GPIO Reference Circuit



Note: The pull-up value is based on the brightness required.

The anticipated usage model is that either the PCH or the SIO can drive a pin low to turn off an LED. In the case of the power LED, the SIO would normally leave its corresponding pin in a high-Z state to allow the LED to turn on. In this state, the PCH can blink the LED by driving its corresponding pin low and subsequently tri-stating the buffer. The I/O buffer should not drive a '1' when configured for this functionality and should be capable of sinking 24 mA of current.

An external optical sensing device can detect the on/off state of the LED. By externally post-processing the information from the optical device, the serial bit stream can be recovered. The hardware will supply a 'sync' byte before the actual data transmission to allow external detection of the transmit frequency. The frequency of transmission should be limited to 1 transition every 1 µs to ensure the detector can reliably sample the on/off state of the LED. To allow flexibility in pull-up resistor values for power optimization, the frequency of the transmission is programmable using the DRS field in the GP_GB_CMDSTS register.

The serial bit stream is Manchester encoded. This choice of transmission ensures that a transition will be seen on every clock. The 1 or 0 data is based on the transmission happening during the high or low phase of the clock.

As the clock will be encoded within the data stream, hardware must ensure that the Z-0 and 0-Z transitions are glitch-free. Driving the pin directly from a flop or through glitch-free logic are possible methods to meet the glitch-free requirement.

A simplified hardware/software register interface provides control and status information to track the activity of this block. Software enabling the serial blink capability should implement an algorithm referenced below to send the serialized message on the enabled GPIO.

1. Read the Go/Busy status bit in the GP_GB_CMDSTS register and verify it is cleared. This will ensure that the GPIO is idled and a previously requested message is still not in progress.
2. Write the data to serialize into the GP_GB_DATA register.
3. Write the DLS and DRS values into the GP_GB_CMDSTS register and set the Go bit. This may be accomplished using a single write.

The reference diagram shows the LEDs being powered from the suspend supply. By providing a generic capability that can be used both in the main and the suspend power planes maximum flexibility can be achieved. A key point to make is that the PCH will not unintentionally drive the LED control pin low unless a serialization is in progress. System board connections utilizing this serialization capability are required to use the same power plane controlling the LED as the GPIO pin. Otherwise, the PCH GPIO may float low during the message and prevent the LED from being controlled from the SIO. The hardware will only be serializing messages when the core power well is powered and the processor is operational.

Care should be taken to prevent the PCH from driving an active '1' on a pin sharing the serial LED capability. Since the SIO could be driving the line to 0, having the PCH drive a 1 would create a high current path. A recommendation to avoid this condition involves choosing a GPIO defaulting to an input. The GP_SER_BLINK register should be set first before changing the direction of the pin to an output. This sequence ensures the open-drain capability of the buffer is properly configured before enabling the pin as an output.

5.16.5.2 Serial Message Format

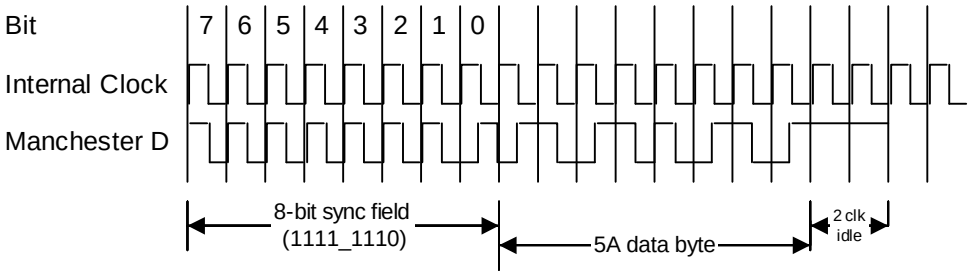
In order to serialize the data onto the GPIO, an initial state of high-Z is assumed. The SIO is required to have its LED control pin in a high-Z state as well to allow PCH to blink the LED (refer to the reference diagram).

The three components of the serial message include the sync, data, and idle fields. The sync field is 7 bits of '1' data followed by 1 bit of '0' data. Starting from the high-Z state (LED on) provides external hardware a known initial condition and a known pattern. In case one or more of the leading 1 sync bits are lost, the 1s followed by 0 provide a clear indication of 'end of sync'. This pattern will be used to 'lock' external sampling logic to the encoded clock.

The data field is shifted out with the highest byte first (MSB). Within each byte, the most significant bit is shifted first (MSb).

The idle field is enforced by the hardware and is at least 2 bit times long. The hardware will not clear the Busy and Go bits until this idle time is met. Supporting the idle time in hardware prevents time-based counting in BIOS as the hardware is immediately ready for the next serial code when the Go bit is cleared. The idle state is represented as a high-Z condition on the pin. If the last transmitted bit is a 1, returning to the idle state will result in a final 0-1 transition on the output Manchester data. Two full bit times of idle correspond to a count of 4 time intervals (the width of the time interval is controlled by the DRS field).

The following waveform shows a 1-byte serial write with a data byte of 5Ah. The internal clock and bit position are for reference purposes only. The Manchester D is the resultant data generated and serialized onto the GPIO. Since the buffer is operating in open-drain mode the transitions are from high-Z to 0 and back.



5.16.6 GPIO Serial Expander (GSX)

5.16.6.1 Overview

There are a finite number of GPIOs available to be used in the PCH frequently runs out of GPIOs. To help alleviate this issue, a new capability has been added to the PCH, the GPIO Serial Expander. This is a new interface that uses external serial-to-parallel and parallel-to-serial expander chips to provide up to 64 additional general purpose I/O signals in steps of 8 while only consuming 5 PCH's I/O pins.

5.16.6.2 Configuration

GSX uses 5 signals, Clock (GSXCLK), Dataout (GSXSDOUT), Datain (GSXSDIN), Reset (GSXSRESET#) and Load (GSXSLOAD). These signals are multiplexed onto PCI Grant and PCI Request signals. A soft strap is used to configure whether GSX is enabled or not. There is no hardstrap configuration or post-boot BIOS setting to change this.

Note: All GSX native functions are determined by GPIO Serial Expander Enable soft strap. Software MUST NOT program the GPIO53/GSXDIN pin to GPIO mode by setting GPIO_USE_SEL[53] bit when GSX is enabled through soft strap. GPIO mode will override GSX operational mode and possible cause board contention on GPIO53 if the platform had planned to use this pin as GSXDIN. It is also recommend that GPIO_IO_SEL[53] be set to 1 when operating in GSX mode as added protection against board contention.

5.16.6.3 Operation

When the soft straps for the PCH are read, the multiplexed signals become GSX only signals and can not be used as PCI signals or general purpose I/O signals. Coming out of reset, the GSXSRESET# signal automatically gets asserted to clear the outputs. This signal stays active until the first cycle to program/upload data.

Software is required to set up the appropriate registers. It defines how many output registers and input registers there are. The max number of combined registers is 8 as the maximum GPIOs are 64. The registers can be any mix and match of input and output. For example, you could have 64 outputs and no inputs, 64 inputs and no outputs, 8 inputs and 56 outputs, and so forth. Also, it's not required to add up to a maximum of 64 I/O. The GSX bus could also support only 8 inputs and 8 outputs, for example.

After resetting the GSX bus with a write to IOERST, software will load up the CxGPOLVL and CxGPOLVL_DW1 registers with data to be written out to the serial to parallel output expanders (how many bits are programmed, is dependent upon how many outputs are defined in the capabilities register). A write to the START (ST) bit will cause the serialization process to begin. First all the output bits are shifted out to the serial to parallel buffers. Then GSXSLOAD goes high to latch in and enable the output of the buffers. At the same time, GSXSLOAD latches in the data into the parallel-to-serial buffers and that data is read into the input buffers (CxGPILVL and CxGPILVL_DW1).

Once the START bit is set, the serialization process starts running continuously... writing out the contents of the CxGPOLVL registers and programming the contents of the CxGPILVL registers. Clearing this bit (writing a "0" to it) will stop the process but only on an atomic boundary. That is, hardware will finish serializing the output and finishing reading in the serial data if it began the cycle.

There are two read only bits to help software with the programming of the CxGPOLVL registers and the reading of the CxGPILVL registers. RUNNING (RUN) is set to a "1" as long as the hardware is in the process of writing out and reading in data. BUSY (BSY) is a "1" as long as the CxGPOLVL data has not been completely written out at least once. For software to make sure that data is not in the middle of being updated, it needs to

wait until RUNNING is a “0”. SW will program START to a “0” and wait for RUNNING to be a “0” before it knows it’s safe to load in new data to the output buffers, or read data from the input buffers without fear of data being updated in the middle of the cycle.

5.17 SATA Host Controller (D31:F2, F5)

The SATA function in the PCH has three modes of operation to support different operating system conditions. In the case of Native IDE enabled operating systems, the PCH uses two controllers to enable all six ports of the bus. The first controller (Device 31: Function 2) supports ports 0 -3 and the second controller (Device 31: Function 5) supports ports 4 and 5. When using a legacy operating system, only one controller (Device 31: Function 2) is available that supports ports 0 - 3. In AHCI or RAID mode, only one controller (Device 31: Function 2) is utilized enabling all six ports and the second controller (Device 31: Function 5) shall be disabled.

The MAP register, Section 15.1.28, provides the ability to share PCI functions. When sharing is enabled, all decode of I/O is done through the SATA registers. Device 31, Function 1 (IDE controller) is hidden by software writing to the Function Disable Register (D31, F0, offset F2h, bit 1), and its configuration registers are not used.

The PCH SATA controllers feature six sets of interface signals (ports) that can be independently enabled or disabled (they cannot be tri-stated or driven low). Each interface is supported by an independent DMA controller.

The PCH SATA controllers interact with an attached mass storage device through a register interface that is equivalent to that presented by a traditional IDE host adapter (when AHCI/RAID disabled). The host software follows existing standards and conventions when accessing the register interface and follows standard command protocol conventions.

Note: SATA interface transfer rates are independent of UDMA mode settings. SATA interface transfer rates will operate at the bus’s maximum speed, regardless of the UDMA mode reported by the SATA device or the system BIOS.

5.17.1 SATA 6 Gb/s Support

The PCH supports SATA 6 Gb/s transfers with all capable SATA devices. SATA 6 Gb/s supports s available on PCH Ports 0 and 1 only.

Note: PCH ports 0 and 1 also supports SATA 1.5 Gb/s and 3.0 Gb/s device transfers, while ports 2-5 only support SATA 1.5 Gb/s and 3.0 Gb/s device transfers.

5.17.2 SATA Feature Support

Feature	PCH (AHCI/RAID Disabled)	PCH (AHCI/RAID Enabled)
Native Command Queuing (NCQ)	N/A	Supported
Auto Activate for DMA	N/A	Supported
Hot-Plug Support	N/A	Supported
Asynchronous Signal Recovery	N/A	Supported
3 Gb/s Transfer Rate	Supported	Supported
ATAPI Asynchronous Notification	N/A	Supported
Host & Link Initiated Power Management	N/A	Supported
Staggered Spin-Up	Supported	Supported
Command Completion Coalescing	N/A	N/A
External SATA	N/A	Supported

Feature	Description
Native Command Queuing (NCQ)	Allows the device to reorder commands for more efficient data transfers
Auto Activate for DMA	Collapses a DMA Setup then DMA Activate sequence into a DMA Setup only
Hot Plug Support	Allows for device detection without power being applied and ability to connect and disconnect devices without prior notification to the system
Asynchronous Signal Recovery	Provides a recovery from a loss of signal or establishing communication after hot plug
6 Gb/s Transfer Rate	Capable of data transfers up to 6Gb/s
ATAPI Asynchronous Notification	A mechanism for a device to send a notification to the host that the device requires attention
Host & Link Initiated Power Management	Capability for the host controller or device to request Partial and Slumber interface power states
Staggered Spin-Up	Enables the host the ability to spin up hard drives sequentially to prevent power load problems on boot
Command Completion Coalescing	Reduces interrupt and completion overhead by allowing a specified number of commands to complete and then generating an interrupt to process the commands
External SATA	Technology that allows for an outside the box connection of up to 2 meters (when using the cable defined in SATA-IO)

5.17.3 Theory of Operation

5.17.3.1 Standard ATA Emulation

The PCH contains a set of registers that shadow the contents of the legacy IDE registers. The behavior of the Command and Control Block registers, PIO, and DMA data transfers, resets, and interrupts are all emulated.

Note: The PCH will assert INTR when the master device completes the EDD command regardless of the command completion status of the slave device. If the master completes EDD first, an INTR is generated and BSY will remain '1' until the slave completes the command. If the slave completes EDD first, BSY will be '0' when the master completes the EDD command and asserts INTR. Software must wait for busy to clear (0) before completing an EDD command, as required by the ATA5 through ATA7 (T13) industry standards.

5.17.3.2 48-Bit LBA Operation

The SATA host controller supports 48-bit LBA through the host-to-device register FIS when accesses are performed using writes to the task file. The SATA host controller will ensure that the correct data is put into the correct byte of the host-to-device FIS.

There are special considerations when reading from the task file to support 48-bit LBA operation. Software may need to read all 16-bits. Since the registers are only 8-bits wide and act as a FIFO, a bit must be set in the device/control register, which is at offset 3F6h for primary and 376h for secondary (or their native counterparts).

If software clears bit 7 of the control register before performing a read, the last item written will be returned from the FIFO. If software sets bit 7 of the control register before performing a read, the first item written will be returned from the FIFO.

5.17.4 SATA Swap Bay Support

The PCH provides for basic SATA swap bay support using the PSC register configuration bits and power management flows. A device can be powered down by software and the port can then be disabled, allowing removal and insertion of a new device.

Note: This SATA swap bay operation requires board hardware (implementation specific), BIOS, and operating system support.

5.17.5 Hot-Plug Operation

The PCH supports Hot-Plug Surprise removal and Insertion Notification. An internal SATA port with a Mechanical Presence Switch can support PARTIAL and SLUMBER with Hot Plug Enabled. Software can take advantage of power savings in the low power states while enabling hot plug operation. Refer to chapter 7 of the AHCI specification for details.

5.17.6 Intel® Rapid Storage Technology enterprise Configuration

The Intel® Rapid Storage Technology enterprise (Intel® RSTe) offers several diverse options for RAID (redundant array of independent disks) to meet the needs of the end user. AHCI support provides higher performance and alleviates disk bottlenecks by taking advantage of the independent DMA engines that each SATA port offers in PCH.

- RAID Level 0 performance scaling up to 4 drives, enabling higher throughput for data intensive applications such as video editing.
- Data security is offered through RAID Level 1, which performs mirroring.
- RAID Level 10 provides high levels of storage performance with increased data protection, combining the fault-tolerance of RAID Level 1 with the performance of RAID Level 0. By striping RAID Level 1 segments, high I/O rates can be achieved on systems that require both performance and fault-tolerance. RAID Level 10 requires 4 hard drives, and provides the capacity of two drives.
- RAID Level 5 provides highly efficient storage while maintaining fault-tolerance on 3 or more drives. By striping parity, and rotating it across all disks, fault tolerance of any single drive is achieved while only consuming 1 drive worth of capacity. That is, a 3 drive RAID 5 has the capacity of 2 drives, or a 4 drive RAID 5 has the capacity of 3 drives. RAID 5 has high read transaction rates, with a medium write rate. RAID 5 is well suited for applications that require high amounts of storage while maintaining fault tolerance.

Intel Rapid Storage Technology enterprise functionality requires the following items:

- Intel Rapid Storage Manager RAID Option ROM must be on the platform
- Intel Rapid Storage Manager drivers, most recent revision.
- At least two SATA hard disk drives (minimum depends on RAID configuration).

Intel Rapid Storage Technology enterprise is not available in the following configurations:

1. The SATA controller is in compatible mode.
2. The SATA controller is programmed in RAID mode, but the AIE bit (D31:F2:Offset 9Ch bit 7) is set to 1.

5.17.6.1 Intel® Rapid Storage Technology enterprise Manager RAID Option ROM

The Intel Rapid Storage Technology enterprise Manager RAID Option ROM is a standard PnP Option ROM that is easily integrated into any System BIOS. When in place, it provides the following three primary functions:

- Provides a text mode user interface that allows the user to manage the RAID configuration on the system in a pre-operating system environment. Its feature set is kept simple to keep size to a minimum, but allows the user to create and delete RAID volumes and select recovery options when problems occur.
- Provides boot support when using a RAID volume as a boot disk. It does this by providing Int13 services when a RAID volume needs to be accessed by MS-DOS applications (such as NTLDR) and by exporting the RAID volumes to the System BIOS for selection in the boot order.
- At each boot up, provides the user with a status of the RAID volumes and the option to enter the user interface by pressing CTRL-I.

5.17.7 Power Management Operation

Power management of the PCH SATA controller and ports will cover operations of the host controller and the SATA wire.

5.17.7.1 Power State Mappings

The D0 PCI power management state for device is supported by the PCH SATA controller.

SATA devices may also have multiple power states. From parallel ATA, three device states are supported through ACPI. They are:

- **D0** – device is working and instantly available.
- **D1** – device enters when it receives a STANDBY IMMEDIATE command. Exit latency from this state is in seconds
- **D3** – from the SATA device's perspective, no different than a D1 state, in that it is entered using the STANDBY IMMEDIATE command. However, an ACPI method is also called which will reset the device and then cut its power.

Each of these device states are subsets of the host controller's D0 state.

Finally, SATA defines three PHY layer power states, which have no equivalent mappings to parallel ATA. They are:

- **PHY READY** – PHY logic and PLL are both on and active
- **Partial** – PHY logic is powered, but in a reduced state. Exit latency is no longer than 10 ns
- **Slumber** – PHY logic is powered, but in a reduced state. Exit latency can be up to 10 ms.

Since these states have much lower exit latency than the ACPI D1 and D3 states, the SATA controller defines these states as sub-states of the device D0 state.

5.17.7.2 Power State Transitions

5.17.7.2.1 Partial and Slumber State Entry/Exit

The partial and slumber states save interface power when the interface is idle. The SATA controller defines PHY layer power management (as performed using primitives) as a driver operation from the host side, and a device proprietary mechanism on the device side. The SATA controller accepts device transition types, but does not issue any transitions as a host. All received requests from a SATA device will be ACKed.

When an operation is performed to the SATA controller such that it needs to use the SATA cable, the controller must check whether the link is in the Partial or Slumber states, and if so, must issue a COM_WAKE to bring the link back online. Similarly, the SATA device must perform the same action.

5.17.7.2.2 Device D1, D3 States

These states are entered after some period of time when software has determined that no commands will be sent to this device for some time. The mechanism for putting a device in these states does not involve any work on the host controller, other then sending commands over the interface to the device. The command most likely to be used in ATA/ATAPI is the "STANDBY IMMEDIATE" command.

5.17.7.2.3 Host Controller $D3_{HOT}$ State

After the interface and device have been put into a low power state, the SATA host controller may be put into a low power state. This is performed using the PCI power management registers in configuration space. There are two very important aspects to note when using PCI power management.

1. When the power state is D3, only accesses to configuration space are allowed. Any attempt to access the memory or I/O spaces will result in master abort.
2. When the power state is D3, no interrupts may be generated, even if they are enabled. If an interrupt status bit is pending when the controller transitions to D0, an interrupt may be generated.

When the controller is put into D3, it is assumed that software has properly shut down the device and disabled the ports. Therefore, there is no need to sustain any values on the port wires. The interface will be treated as if no device is present on the cable, and power will be minimized.

When returning from a D3 state, an internal reset will not be performed.

5.17.7.2.4 Non-AHCI Mode PME# Generation

When in non-AHCI mode (legacy mode) of operation, the SATA controller does not generate PME#. This includes attach events (since the port must be disabled), or interlock switch events (using the SATAGP pins).

5.17.7.3 Intel® Scalable Memory Interconnect (Intel® SMI) Trapping (APM)

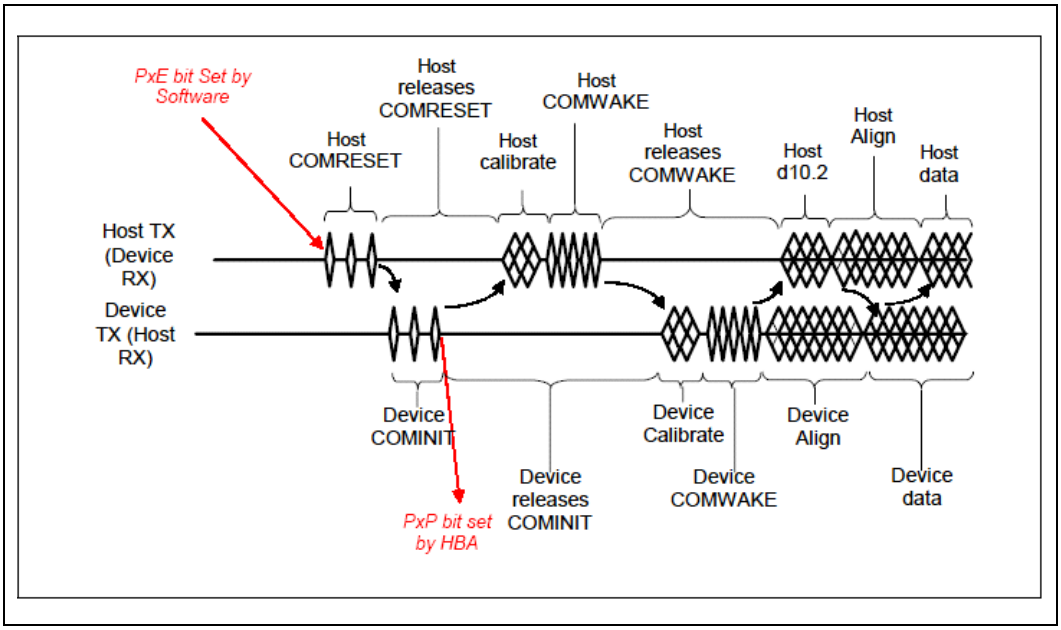
Device 31:Function2:Offset C0h (see Section 14.1.41) control for generating SMI# on accesses to the IDE I/O spaces. These bits map to the legacy ranges (1F0–1F7h, 3F6h, 170–177h, and 376h) and native IDE ranges defined by PCMDBA, PCTLBA, SCMDBA an SCTLBA. If the SATA controller is in legacy mode and is using these addresses, accesses to one of these ranges with the appropriate bit set causes the cycle to not be forwarded to the SATA controller, and for an SMI# to be generated. If an access to the Bus-Master IDE registers occurs while trapping is enabled for the device being accessed, then the register is updated, an SMI# is generated, and the device activity status bits (Section 14.1.42) are updated indicating that a trap occurred.

5.17.8 SATA Device Presence

In legacy mode, the SATA controller does not generate interrupts based on hot plug/ unplug events. However, the SATA PHY does know when a device is connected (if not in a partial or slumber state), and it s beneficial to communicate this information to host software as this will greatly reduce boot times and resume times.

The flow used to indicate SATA device presence is shown in Figure 5-7. The ‘PxE’ bit refers to PCS.P[3:0]E bits, depending on the port being checked and the ‘PxP’ bits refer to the PCS.P[3:0]P bits, depending on the port being checked. If the PCS/PxP bit is set a device is present, if the bit is cleared a device is not present. If a port is disabled, software can check to see if a new device is connected by periodically re-enabling the port and observing if a device is present, if a device is not present it can disable the port and check again later. If a port remains enabled, software can periodically poll PCS.PxP to see if a new device is connected.

Figure 5-7. Flow for Port Enable / Device Present Bits



5.17.9 SATA LED

The SATALED# output is driven whenever the BSY bit is set in any SATA port. The SATALED# is an active-low open-drain output. When SATALED# is low, the LED should be active. When SATALED# is high, the LED should be inactive.

5.17.10 AHCI Operation

The PCH provides hardware support for Advanced Host Controller Interface (AHCI), a programming interface for SATA host controllers developed through a joint industry effort. AHCI defines transactions between the SATA controller and software and enables advanced performance and usability with SATA. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices—each device is treated as a master—and hardware assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug. AHCI requires appropriate software support (e.g., an AHCI driver) and for some features, hardware support in the SATA device or additional platform hardware.

The PCH supports all of the mandatory features of the *Serial ATA Advanced Host Controller Interface Specification*, Revision 1.2 and many optional features, such as hardware assisted native command queuing, aggressive power management, LED indicator support, and Hot-Plug through the use of interlock switch support (additional platform hardware and software may be required depending upon the implementation).

For reliable device removal notification while in AHCI operation without the use of interlock switches (surprise removal), interface power management should be disabled for the associated port. See Section 7.3.1 of the *AHCI Specification* for more information.

5.17.11 SGPIO Signals

The SGPIO signals, in accordance to the SFF-8485 specification, support per-port LED signaling. These signals are not related to SATALED#, which allows for simplified indication of SATA command activity. The SGPIO group interfaces with an external controller chip that fetches and serializes the data for driving across the SGPIO bus. The output signals then control the LEDs. This feature is only valid in AHCI/RAID mode.

Note: Intel does not validate all possible usage cases of this feature. Customers should validate their specific design implementation on their own platforms.

5.17.11.1 Mechanism

The enclosure management for SATA Controller 1 (Device 31: Function 2) involves sending messages that control LEDs in the enclosure. The messages for this function are stored after the normal registers in the AHCI BAR, at Offset 580h bytes for PCH from the beginning of the AHCI BAR as specified by the EM_LOC global register (Section 14.4.1.6).

Software creates messages for transmission in the enclosure management message buffer. The data in the message buffer should not be changed if CTL.TM bit is set by software to transmit an update message. Software should only update the message buffer when CTL.TM bit is cleared by hardware otherwise the message transmitted will be indeterminate. Software then writes a register to cause hardware to transmit the message or take appropriate action based on the message content. The software should only create message types supported by the controller, which is LED messages for PCH. If the software creates other non LED message types (e.g. SAF-TE, SES-2), the SGPIO interface may hang and the result is indeterminate.

During reset all SGPIO pins will be in tri-state state. The interface will continue to be in tri-state state after reset until the first transmission occurs when software programs the message buffer and sets the transmit bit CTL.TM. The SATA Host controller will initiate the transmission by driving SCLOCK and at the same time drive the SLOAD to ‘0’ prior to the actual bit stream transmission. The Host will drive SLOAD low for at least 5 SCLOCK then only start the bit stream by driving the SLOAD to high. SLOAD will be driven high for 1 SCLOCK follow by vendor specific pattern that is default to “0000” if software has yet to program the value. A total of 21-bit stream from 7 ports (Port0, Port1, Port2, Port3, Port4 Port5 and Port6) of 3-bit per port LED message will be transmitted on SDATAOUT0 pin after the SLOAD is driven high for 1 SCLOCK. Only 3 ports (Port4, Port5 and Port6) of 9 bit total LED message follow by 12 bits of tri-state value will be transmitted out on SDATAOUT1 pin.

All the default LED message values will be high prior to software setting them, except the Activity LED message that is configured to be hardware driven that will be generated based on the activity from the respective port. All the LED message values will be driven to ‘1’ for the port that is unimplemented as indicated in the Port Implemented register regardless of the software programmed value through the message buffer.

There are 2 different ways of resetting PCH SGPIO interface, asynchronous reset and synchronous reset. Asynchronous reset is caused by platform reset to cause the SGPIO interface to be tri-state asynchronously. Synchronous reset is caused by setting the CTL.RESET bit, clearing the GHC.AE bit or HBA reset, where Host Controller will complete the existing full bit stream transmission then only tri-state all the SGPIO pins. After the reset, both synchronous and asynchronous, the SGPIO pins will stay tri-stated.

Note: PCH Host Controller does not ensure that it will cause the target SGPIO device or controller to be reset. Software is responsible to keep PCH SGPIO interface in tri-state for 2 second in order to cause a reset on the target of the SGPIO interface.

5.17.11.2 Message Format

Messages shall be constructed with a one DWord header that describes the message to be sent followed by the actual message contents. The first DWord shall be constructed as follows:

Bit	Description
31:28	Reserved
27:24	**Message Type (MTYPE):** Specifies the type of the message. The message types are: 0h = LED 1h = SAF-TE 2h = SES-2 3h = SGPIO (register based interface) All other values reserved
23:16	**Data Size (DSIZE):** Specifies the data size in bytes. If the message (enclosure services command) has a data buffer that is associated with it that is transferred, the size of that data buffer is specified in this field. If there is no separate data buffer, this field shall have a value of '0'. The data directly follows the message in the message buffer. For PCH, this value should always be '0'.
15:8	**Message Size (MSIZE):** Specifies the size of the message in bytes. The message size does not include the one DWord header. A value of '0' is invalid. For PCH, the message size is always 4 bytes.
7:0	Reserved

The SAF-TE, SES-2, and SGPIO message formats are defined in the corresponding specifications, respectively. The LED message type is defined in Section 5.17.11.3. It is the responsibility of software to ensure the content of the message format is correct. If the message type is not programmed as 'LED' for this controller, the controller shall not take any action to update its LEDs. For LED message type, the message size is always consisted of 4 bytes.

5.17.11.3 LED Message Type

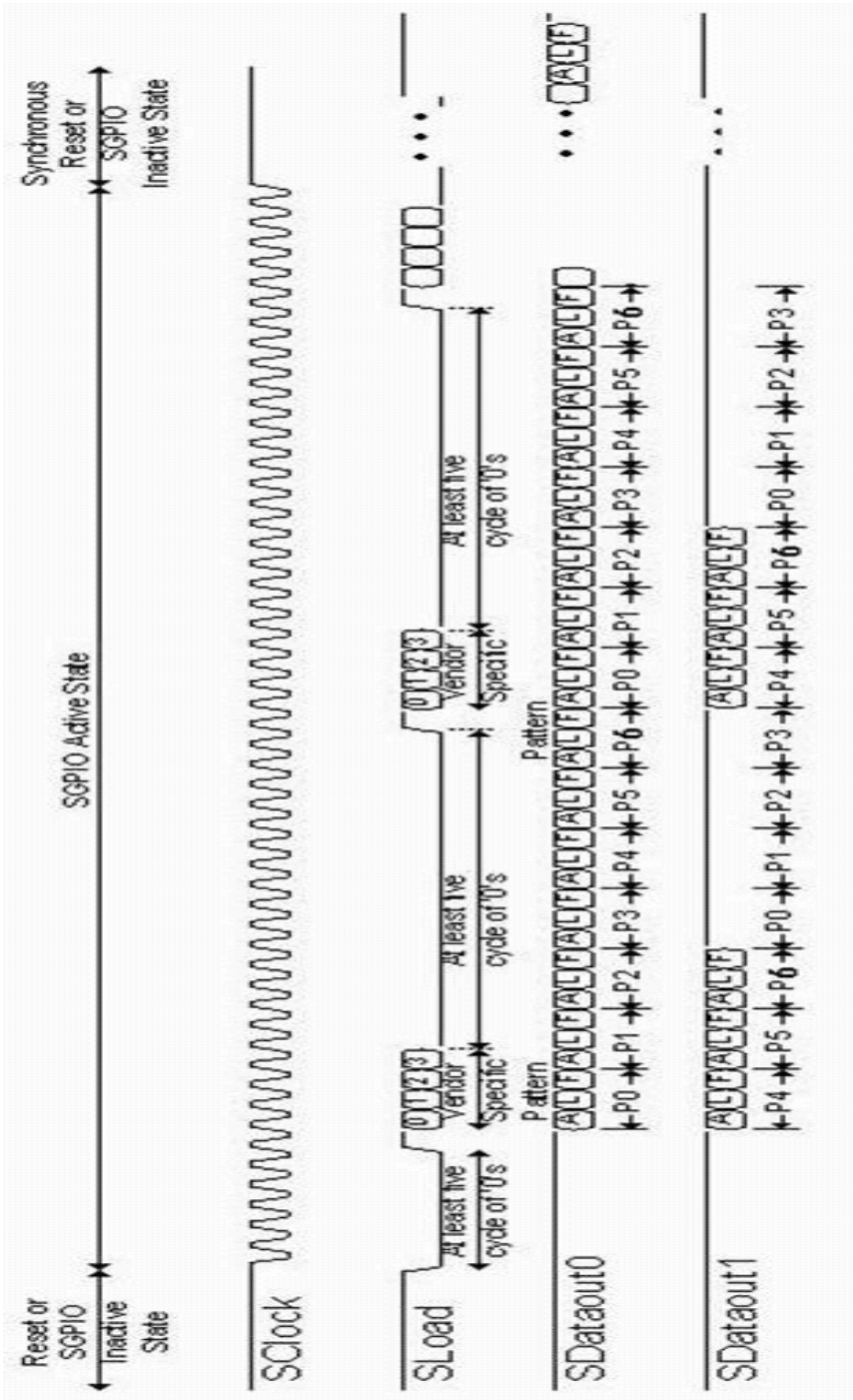
The LED message type specifies the status of up to three LEDs. Typically, the usage for these LEDs is activity, fault, and locate. Not all implementations necessarily contain all LEDs (for example, some implementations may not have a locate LED). The message identifies the HBA port number and the Port Multiplier port number that the slot status applies to. If a Port Multiplier is not in use with a particular device, the Port Multiplier port number shall be '0'. The format of the LED message type is defined in Table 5-39. The LEDs shall retain their values until there is a following update for that particular slot.

Table 5-39. Multi-Activity LED Message Type

Byte	Description
3-2	**Value (VAL):** This field describes the state of each LED for a particular location. There are three LEDs that may be supported by the HBA. Each LED has 3 bits of control. **LED values are:** 000b - LED shall be off 001b - LED shall be solid on as perceived by human eye All other values reserved **The LED bit locations are:** Bits 2:0 - Activity LED (may be driven by hardware) Bits 5:3 - Vendor Specific LED (e.g. locate) Bits 8:6 - Vendor Specific LED (e.g. fault) Bits 15:9 - Reserved **Vendor specific message is:** Bit 3:0 - Vendor Specific Pattern Bit 15:4 - Reserved ***Note:*** If Activity LED Hardware Driven (ATTR.ALHD) bit is set, host will output the hardware LED value sampled internally and will ignore software written activity value on bit [2:0]. Since PCH Enclosure Management does not support port multiplier based LED message, the LED message will be generated independently based on respective port's operation activity. Vendor specific LED values Locate (Bits 5:3) and Fault (Bits 8:6) always are driven by software.
1	**Port Multiplier Information:** Specifies slot specific information related to Port Multiplier. Bits 3:0 specify the Port Multiplier port number for the slot that requires the status update. If a Port Multiplier is not attached to the device in the affected slot, the Port Multiplier port number shall be '0'. Bits 7:4 are reserved. PCH does not support LED messages for devices behind a Port MUltiplier. This byte should be 0.
0	**HBA Information:** Specifies slot specific information related to the HBA. Bits 4:0 - HBA port number for the slot that requires the status update. Bit 5 - If set to '1', Value is a vendor specific message that applies to the entire enclosure. If cleared to '0', Value applies to the port specified in bits 4:0. Bits 7:6 - Reserved

5.17.11.4 SGPIO Waveform

Figure 5-8. Serial Data Transmitted over the SGPIO Interface



5.17.12 External SATA

PCH supports external SATA. External SATA utilizes the SATA interface outside of the system box. The usage model for this feature must comply with the Serial ATA II Cables and Connectors Volume 2 Gold specification at www.sata-io.org. Intel validates two configurations:

1. The cable-up solution involves an internal SATA cable that connects to the SATA motherboard connector and spans to a back panel PCI bracket with an eSATA connector. A separate eSATA cable is required to connect an eSATA device.
2. The back-panel solution involves running a trace to the I/O back panel and connecting a device using an external SATA connector on the board.

5.18 High Precision Event Timers

This function provides a set of timers that can be used by the operating system. The timers are defined such that in the future, the operating system may be able to assign specific timers to used directly by specific applications. Each timer can be configured to cause a separate interrupt.

PCH provides eight timers. The timers are implemented as a single counter each with its own comparator and value register. This counter increases monotonically. Each individual timer can generate an interrupt when the value in its value register matches the value in the main counter.

The registers associated with these timers are mapped to a memory space (much like the I/O APIC). However, it is not implemented as a standard PCI function. The BIOS reports to the operating system the location of the register space. The hardware can support an assignable decode space; however, the BIOS sets this space prior to handing it over to the operating system. It is not expected that the operating system will move the location of these timers once it is set by the BIOS.

5.18.1 Timer Accuracy

1. The timers are accurate over any 1 ms period to within 0.05% of the time specified in the timer resolution fields.
2. Within any 100 microsecond period, the timer reports a time that is up to two ticks too early or too late. Each tick is less than or equal to 100 ns, so this represents an error of less than 0.2%.
3. The timer is monotonic. It does not return the same value on two consecutive reads (unless the counter has rolled over and reached the same value).

The main counter is clocked by the 14.31818 MHz clock, synchronized into the 66.666 MHz domain. This results in a non-uniform duty cycle on the synchronized clock, but does have the correct average period. The accuracy of the main counter is as accurate as the 14.31818 MHz clock.

5.18.2 Interrupt Mapping

Mapping Option #1 (Legacy Replacement Option)

In this case, the Legacy Replacement Rout bit (LEG_RT_CNF) is set. This forces the mapping found in Table 5-40.

Table 5-40. Legacy Replacement Routing

Timer	8259 Mapping	APIC Mapping	Comment
0	IRQ0	IRQ2	In this case, the 8254 timer will not cause any interrupts
1	IRQ8	IRQ8	In this case, the RTC will not cause any interrupts.
2 & 3	Per IRQ Routing Field.	Per IRQ Routing Field	
4, 5, 6, 7	not available	not available	

Note: The Legacy Option does not preclude delivery of IRQ0/IRQ8 using direct FSB interrupt messages.

Mapping Option #2 (Standard Option)

In this case, the Legacy Replacement Rout bit (LEG_RT_CNF) is 0. Each timer has its own routing control. The interrupts can be routed to various interrupts in the 8259 or I/O APIC. A capabilities field indicates which interrupts are valid options for routing. If a timer is set for edge-triggered mode, the timers should not be share with any PCI interrupts.

For the PCH, the only supported interrupt values are as follows:

Timer 0 and 1: IRQ20, 21, 22 & 23 (I/O APIC only).

Timer 2: IRQ11 (8259 or I/O APIC) and IRQ20, 21, 22 & 23 (I/O APIC only).

Timer 3: IRQ12 (8259 or I/O APIC) and IRQ 20, 21, 22 & 23 (I/O APIC only).

Interrupts from Timer 4, 5, 6, 7 can only be delivered using direct FSB interrupt messages.

5.18.3 Periodic versus Non-Periodic Modes

Non-Periodic Mode

Timer 0 is configurable to 32 (default) or 64-bit mode, whereas Timers 1, 2 and 3 only support 32-bit mode (See TBD).

All of the timers support non-periodic mode.

Refer to Section 2.3.9.2.1 of the *IA-PC HPET Specification* for a description of this mode.

Periodic Mode

Timer 0 is the only timer that supports periodic mode. Refer to Section 2.3.9.2.2 of the *IA-PC HPET Specification* for a description of this mode.

The following usage model is expected:

1. Software clears the ENABLE_CNF bit to prevent any interrupts
2. Software Clears the main counter by writing a value of 00h to it.

3. Software sets the TIMER0_VAL_SET_CNF bit.
4. Software writes the new value in the TIMER0_COMPARATOR_VAL register
5. Software sets the ENABLE_CNF bit to enable interrupts.

The Timer 0 Comparator Value register cannot be programmed reliably by a single 64-bit write in a 32-bit environment except if only the periodic rate is being changed during run-time. If the actual Timer 0 Comparator Value needs to be reinitialized, then the following software solution will always work regardless of the environment:

1. Set TIMER0_VAL_SET_CNF bit
2. Set the lower 32 bits of the Timer0 Comparator Value register
3. Set TIMER0_VAL_SET_CNF bit
4. Set the upper 32 bits of the Timer0 Comparator Value register

5.18.4 Enabling the Timers

The BIOS or operating system PnP code should route the interrupts. This includes the Legacy Rout bit, Interrupt Rout bit (for each timer), interrupt type (to select the edge or level type for each timer)

The Device Driver code should do the following for an available timer:

1. Set the Overall Enable bit (Offset 10h, bit 0).
2. Set the timer type field (selects one-shot or periodic).
3. Set the interrupt enable
4. Set the comparator value

5.18.5 Interrupt Levels

Interrupts directed to the internal 8259s are active high. See Section 5.10 for information regarding the polarity programming of the I/O APIC for detecting internal interrupts.

If the interrupts are mapped to the 8259 or I/O APIC and set for level-triggered mode, they can be shared with PCI interrupts. They may be shared although it's unlikely for the operating system to attempt to do this.

If more than one timer is configured to share the same IRQ (using the TIMERn_INT_ROUT_CNF fields), then the software must configure the timers to level-triggered mode. Edge-triggered interrupts cannot be shared.

5.18.6 Handling Interrupts

If each timer has a unique interrupt and the timer has been configured for edge-triggered mode, then there are no specific steps required. No read is required to process the interrupt.

If a timer has been configured to level-triggered mode, then its interrupt must be cleared by the software. This is done by reading the interrupt status register and writing a 1 back to the bit position for the interrupt to be cleared.

Independent of the mode, software can read the value in the main counter to see how time has passed between when the interrupt was generated and when it was first serviced.

If Timer 0 is set up to generate a periodic interrupt, the software can check to see how much time remains until the next interrupt by checking the timer value register.

5.18.7 Issues Related to 64-Bit Timers with 32-Bit Processors

A 32-bit timer can be read directly using processors that are capable of 32-bit or 64-bit instructions. However, a 32-bit processor may not be able to directly read 64-bit timer. A race condition comes up if a 32-bit processor reads the 64-bit register using two separate 32-bit reads. The danger is that just after reading one half, the other half rolls over and changes the first half.

If a 32-bit processor needs to access a 64-bit timer, it must first halt the timer before reading both the upper and lower 32-bits of the timer. If a 32-bit processor does not want to halt the timer, it can use the 64-bit timer as a 32-bit timer by setting the TIMERn_32MODE_CNF bit. This causes the timer to behave as a 32-bit timer. The upper 32-bits are always 0.

Alternatively, software may do a multiple read of the counter while it is running. Software can read the high 32 bits, then the low 32 bits, the high 32 bits again. If the high 32 bits have not changed between the two reads, then a rollover has not happened and the low 32 bits are valid. If the high 32 bits have changed between reads, then the multiple reads are repeated until a valid read is performed.

Note: On a 64-bit platform, if software attempts a 64 bit read of the 64-bit counter, software must be aware that some platforms may split the 64 bit read into two 32 bit reads. The read maybe inaccurate if the low 32 bits roll over between the high and low reads.

5.19 USB EHCI Host Controllers (D29:F0 and D26:F0)

The PCH contains two Enhanced Host Controller Interface (EHCI) host controllers which support up to fourteen USB 2.0 high-speed root ports. USB 2.0 allows data transfers up to 480 Mb/s. USB 2.0 based Debug Port is also implemented in the PCH.

5.19.1 EHC Initialization

The following descriptions step through the expected PCH Enhanced Host Controller (EHC) initialization sequence in chronological order, beginning with a complete power cycle in which the suspend well and core well have been off.

5.19.1.1 BIOS Initialization

BIOS performs a number of platform customization steps after the core well has powered up. Contact your Intel Field Representative for additional PCH BIOS information.

5.19.1.2 Driver Initialization

See Chapter 4 of the *Enhanced Host Controller Interface Specification for Universal Serial Bus,* Revision 1.0.

5.19.1.3 EHC Resets

In addition to the standard PCH hardware resets, portions of the EHC are reset by the HCRESET bit and the transition from the $D3_{HOT}$ device power management state to the D0 state. The effects of each of these resets are:

Reset	Does Reset	Does not Reset	Comments
HCRESET bit set.	Memory space registers except Structural Parameters (which is written by BIOS).	Configuration registers.	The HCRESET must only affect registers that the EHCI driver controls. PCI Configuration space and BIOS-programmed parameters can not be reset.
Software writes the Device Power State from $D3_{HOT}$ (11b) to D0 (00b).	Core well registers (except BIOS-programmed registers).	Suspend well registers; BIOS-programmed core well registers.	The D3-to-D0 transition must not cause wake information (suspend well) to be lost. It also must not clear BIOS-programmed registers because BIOS may not be invoked following the D3-to-D0 transition.

If the detailed register descriptions give exceptions to these rules, those exceptions override these rules. This summary is provided to help explain the reasons for the reset policies.

5.19.2 Data Structures in Main Memory

See Section 3 and Appendix B of the *Enhanced Host Controller Interface Specification for Universal Serial Bus*, Revision 1.0 for details.

5.19.3 USB 2.0 Enhanced Host Controller DMA

The PCH USB 2.0 EHC implements three sources of USB packets. They are, in order of priority on USB during each microframe:

1. The USB 2.0 Debug Port (see Section Section 5.19.9, "USB 2.0 Based Debug Port"),
2. The Periodic DMA engine, and
3. The Asynchronous DMA engine.

The PCH always performs any currently-pending debug port transaction at the beginning of a microframe, followed by any pending periodic traffic for the current microframe. If there is time left in the microframe, then the EHC performs any pending asynchronous traffic until the end of the microframe (EOF1). The debug port traffic is only presented on Port 1 and Port 9, while the other ports are idle during this time.

5.19.4 Data Encoding and Bit Stuffing

See Chapter 8 of the *Universal Serial Bus Specification, Revision 2.0.*

5.19.5 Packet Formats

See Chapter 8 of the *Universal Serial Bus Specification, Revision 2.0*.

The PCH EHCI allows entrance to USB test modes, as defined in the USB 2.0 specification, including Test J, Test Packet, etc. However, the PCH Test Packet test mode interpacket gap timing may not meet the USB 2.0 specification.

5.19.6 USB 2.0 Interrupts and Error Conditions

Section 4 of the *Enhanced Host Controller Interface Specification for Universal Serial Bus*, Revision 1.0 goes into detail on the EHC interrupts and the error conditions that cause them. All error conditions that the EHC detects can be reported through the EHCI Interrupt status bits. Only PCH-specific interrupt and error-reporting behavior is documented in this section. The EHCI Interrupts Section must be read first, followed by this section of the datasheet to fully comprehend the EHC interrupt and error-reporting functionality.

- Based on the EHC Buffer sizes and buffer management policies, the Data Buffer Error can never occur on the PCH.
- Master Abort and Target Abort responses from hub interface on EHC-initiated read packets will be treated as Fatal Host Errors. The EHC halts when these conditions are encountered.
- The PCH may assert the interrupts which are based on the interrupt threshold as soon as the status for the last complete transaction in the interrupt interval has been posted in the internal write buffers. The requirement in the *Enhanced Host Controller Interface Specification for Universal Serial Bus*, Revision 1.0 (that the status is written to memory) is met internally, even though the write may not be seen on DMI before the interrupt is asserted.
- Since the PCH supports the 1024-element Frame List size, the Frame List Rollover interrupt occurs every 1024 milliseconds.
- The PCH delivers interrupts using PIRQH#.
- The PCH does not modify the CERR count on an Interrupt IN when the "Do Complete-Split" execution criteria are not met.
- For complete-split transactions in the Periodic list, the "Missed Microframe" bit does not get set on a control-structure-fetch that fails the late-start test. If subsequent accesses to that control structure do not fail the late-start test, then the "Missed Microframe" bit will get set and written back.

5.19.6.1 Aborts on USB 2.0-Initiated Memory Reads

If a read initiated by the EHC is aborted, the EHC treats it as a fatal host error. The following actions are taken when this occurs:

- The Host System Error status bit is set
- The DMA engines are halted after completing up to one more transaction on the USB interface
- If enabled (by the Host System Error Enable), then an interrupt is generated
- If the status is Master Abort, then the Received Master Abort bit in configuration space is set
- If the status is Target Abort, then the Received Target Abort bit in configuration space is set
- If enabled (by the SERR Enable bit in the function's configuration space), then the Signaled System Error bit in configuration bit is set.

5.19.7 USB 2.0 Power Management

5.19.7.1 Pause Feature

This feature allows platforms to dynamically enter low-power states during brief periods when the system is idle (that is, between keystrokes). This is useful for enabling power management features in the PCH. The policies for entering these states typically are based on the recent history of system bus activity to incrementally enter deeper power management states. Normally, when the EHC is enabled, it regularly accesses main memory while traversing the DMA schedules looking for work to do; this activity is viewed by the power management software as a non-idle system, thus preventing the power managed states to be entered. Suspending all of the enabled ports can prevent the memory accesses from occurring, but there is an inherent latency overhead with entering and exiting the suspended state on the USB ports that makes this unacceptable for the purpose of dynamic power management. As a result, the EHCI software drivers are allowed to pause the EHC DMA engines when it knows that the traffic patterns of the attached devices can afford the delay. The pause only prevents the EHC from generating memory accesses; the SOF packets continue to be generated on the USB ports (unlike the suspended state).

5.19.7.2 Suspend Feature

The *Enhanced Host Controller Interface (EHCI) For Universal Serial Bus Specification*, Section 4.3 describes the details of Port Suspend and Resume.

5.19.7.3 ACPI Device States

The USB 2.0 function only supports the D0 and D3 PCI Power Management states. Notes regarding the PCH implementation of the Device States:

1. The EHC hardware does not inherently consume any more power when it is in the D0 state than it does in the D3 state. However, software is required to suspend or disable all ports prior to entering the D3 state such that the maximum power consumption is reduced.
2. In the D0 state, all implemented EHC features are enabled.
3. In the D3 state, accesses to the EHC memory-mapped I/O range will master abort. Since the Debug Port uses the same memory range, the Debug Port is only operational when the EHC is in the D0 state.
4. In the D3 state, the EHC interrupt must never assert for any reason. The internal PME# signal is used to signal wake events, etc.
5. When the Device Power State field is written to D0 from D3, an internal reset is generated. See Section 5.19.1.3, "EHC Resets" for general rules on the effects of this reset.
6. Attempts to write any other value into the Device Power State field other than 00b (D0 state) and 11b (D3 state) will complete normally without changing the current value in this field.

5.19.7.4 ACPI System States

The EHC behavior as it relates to other power management states in the system is summarized in the following list:

— The System is always in the S0 state when the EHC is in the D0 state. However, when the EHC is in the D3 state, the system may be in any power management state (including S0).

— When in D0, the Pause feature (See Section 5.19.7.1) enables dynamic processor low-power states to be entered.

— The PLL in the EHC is disabled when entering the S3/S4/S5 states (core power turns off).

— All core well logic is reset in the S3/S4/S5 states.

5.19.8 USB 2.0 Legacy Keyboard Operation

The PCH must support the possibility of a keyboard downstream from either a full-speed/low-speed or a high-speed port. The description of the legacy keyboard support is unchanged from USB 1.1.

— The EHC provides the basic ability to generate SMIs on an interrupt event, along with more sophisticated control of the generation of Intel SMIs.

5.19.9 USB 2.0 Based Debug Port

The PCH supports the elimination of the legacy COM ports by providing the ability for new debugger software to interact with devices on a USB 2.0 port.

High-level restrictions and features are:

- Operational before USB 2.0 drivers are loaded.
- Functions even when the port is disabled.
- Allows normal system USB 2.0 traffic in a system that may only have one USB port.
- Debug Port device (DPD) must be high-speed capable and connect directly to Port 1 and Port 9 on PCH systems (such as, the DPD cannot be connected to Port 1/Port 9 through a hub. When a DPD is detected the PCH EHCI will bypass the integrated Rate Matching Hub and connect directly to the port and the DPD).
- Debug Port FIFO always makes forward progress (a bad status on USB is simply presented back to software).
- The Debug Port FIFO is only given one USB access per microframe.

The Debug port facilitates operating system and device driver debug. It allows the software to communicate with an external console using a USB 2.0 connection. Because the interface to this link does not go through the normal USB 2.0 stack, it allows communication with the external console during cases where the operating system is not loaded, the USB 2.0 software is broken, or where the USB 2.0 software is being debugged. Specific features of this implementation of a debug port are:

- Only works with an external USB 2.0 debug device (console)
- Implemented for a specific port on the host controller
- Operational anytime the port is not suspended AND the host controller is in D0 power state.
- Capability is interrupted when port is driving USB RESET

5.19.9.1 Theory of Operation

There are two operational modes for the USB debug port:

1. Mode 1 is when the USB port is in a disabled state from the viewpoint of a standard host controller driver. In Mode 1, the Debug Port controller is required to generate a "keepalive" packets less than 2 ms apart to keep the attached debug device from suspending. The keepalive packet should be a standalone 32-bit SYNC field.
2. Mode 2 is when the host controller is running (that is, host controller's *Run/Stop#* bit is 1). In Mode 2, the normal transmission of SOF packets will keep the debug device from suspending.

Behavioral Rules

1. In both modes 1 and 2, the Debug Port controller must check for software requested debug transactions at least every 125 microseconds.
2. If the debug port is enabled by the debug driver, and the standard host controller driver resets the USB port, USB debug transactions are held off for the duration of the reset and until after the first SOF is sent.
3. If the standard host controller driver suspends the USB port, then USB debug transactions are held off for the duration of the suspend/resume sequence and until after the first SOF is sent.
4. The ENABLED_CNT bit in the debug register space is independent of the similar port control bit in the associated Port Status and Control register.

Table 5-41 shows the debug port behavior related to the state of bits in the debug registers as well as bits in the associated Port Status and Control register.

Table 5-41. Debug Port Behavior

OWNER_CNT	ENABLED_CT	Port Enable	Run / Stop	Suspend	Debug Port Behavior
0	X	X	X	X	Debug port is not being used. Normal operation.
1	0	X	X	X	Debug port is not being used. Normal operation.
1	1	0	0	X	Debug port in Mode 1. SYNC keepalives sent plus debug traffic
1	1	0	1	X	Debug port in Mode 2. SOF (and only SOF) is sent as keepalive. Debug traffic is also sent. No other normal traffic is sent out this port, because the port is not enabled.
1	1	1	0	0	Invalid. Host controller driver should never put controller into this state (enabled, not running and not suspended).
1	1	1	0	1	Port is suspended. No debug traffic sent.
1	1	1	1	0	Debug port in Mode 2. Debug traffic is interspersed with normal traffic.
1	1	1	1	1	Port is suspended. No debug traffic sent.

5.19.9.1.1 OUT Transactions

An Out transaction sends data to the debug device. It can occur only when the following are true:

- The debug port is enabled
- The debug software sets the GO_CNT bit
- The WRITE_READ#_CNT bit is set

The sequence of the transaction is:

1. Software sets the appropriate values in the following bits:
   - USB_ADDRESS_CNF
   - USB_ENDPOINT_CNF
   - DATA_BUFFER[63:0]
   - TOKEN_PID_CNT[7:0]
   - SEND_PID_CNT[15:8]
   - DATA_LEN_CNT
   - WRITE_READ#_CNT
     Note: This will always be 1 for OUT transactions.
   - GO_CNT:
     Note: This will always be 1 to initiate the transaction
2. The debug port controller sends a token packet consisting of:
   - SYNC
   - TOKEN_PID_CNT field
   - USB_ADDRESS_CNT field
   - USB_ENDPOINT_CNT field
   - 5-bit CRC field
3. After sending the token packet, the debug port controller sends a data packet consisting of:
   - SYNC
   - SEND_PID_CNT field
   - The number of data bytes indicated in DATA_LEN_CNT from the DATA_BUFFER
   - 16-bit CRC

Note: A DATA_LEN_CNT value of 0 is valid in which case no data bytes would be included in the packet.

4. After sending the data packet, the controller waits for a handshake response from the debug device.

- If a handshake is received, the debug port controller:
  - a. Places the received PID in the RECEIVED_PID_STS field
  - b. Resets the ERROR_GOOD#_STS bit
  - c. Sets the DONE_STS bit
- If no handshake PID is received, the debug port controller:
  - a. Sets the EXCEPTION_STS field to 001b
  - b. Sets the ERROR_GOOD#_STS bit
  - c. Sets the DONE_STS bit

5.19.9.1.2 IN Transactions

An IN transaction receives data from the debug device. It can occur only when the following are true:

- The debug port is enabled
- The debug software sets the GO_CNT bit
- The WRITE_READ#_CNT bit is reset

The sequence of the transaction is:

1. Software sets the appropriate values in the following bits:
   — USB_ADDRESS_CNF
   — USB_ENDPOINT_CNF
   — TOKEN_PID_CNT[7:0]
   — DATA_LEN_CNT
   — WRITE_READ#_CNT
   Note: This will always be 0 for IN transactions.
   — GO_CNT
   Note: This will always be 1 to initiate the transaction.
2. The debug port controller sends a token packet consisting of:
   — SYNC
   — TOKEN_PID_CNT field
   — USB_ADDRESS_CNT field
   — USB_ENDPOINT_CNT field
   — 5-bit CRC field.
3. After sending the token packet, the debug port controller waits for a response from the debug device.
   If a response is received:
   — The received PID is placed into the RECEIVED_PID_STS field
   — Any subsequent bytes are placed into the DATA_BUFFER
   — The DATA_LEN_CNT field is updated to show the number of bytes that were received after the PID.
4. If a valid packet was received from the device that was one byte in length (indicating it was a handshake packet), then the debug port controller:
   — Resets the ERROR_GOOD#_STS bit
   — Sets the DONE_STS bit
5. If a valid packet was received from the device that was more than one byte in length (indicating it was a data packet), then the debug port controller:
   — Transmits an ACK handshake packet
   — Resets the ERROR_GOOD#_STS bit
   — Sets the DONE_STS bit
6. If no valid packet is received, then the debug port controller:
   — Sets the EXCEPTION_STS field to 001b
   — Sets the ERROR_GOOD#_STS bit
   — Sets the DONE_STS bit.

5.19.9.1.3 Debug Software

Enabling the Debug Port

There are two mutually exclusive conditions that debug software must address as part of its startup processing:

- The EHCI has been initialized by system software
- The EHCI has not been initialized by system software

Debug software can determine the current 'initialized' state of the EHCI by examining the Configure Flag in the EHCI USB 2.0 Command Register. If this flag is set, then system software has initialized the EHCI. Otherwise the EHCI should not be considered initialized. Debug software will initialize the debug port registers depending on the state of the EHCI. However, before this can be accomplished, debug software must determine which root USB port is designated as the debug port.

Determining the Debug Port

Debug software can easily determine which USB root port has been designated as the debug port by examining bits 20:23 of the EHCI Host Controller Structural Parameters register. This 4-bit field represents the numeric value assigned to the debug port (that is, 0001=port 1).

Debug Software Startup with Non-Initialized EHCI

Debug software can attempt to use the debug port if after setting the OWNER_CNT bit, the Current Connect Status bit in the appropriate (See *Determining the Debug Port Presence*) PORTSC register is set. If the Current Connect Status bit is not set, then debug software may choose to terminate or it may choose to wait until a device is connected.

If a device is connected to the port, then debug software must reset/enable the port. Debug software does this by setting and then clearing the Port Reset bit the PORTSC register. To ensure a successful reset, debug software should wait at least 50 ms before clearing the Port Reset bit. Due to possible delays, this bit may not change to 0 immediately; reset is complete when this bit reads as 0. Software must not continue until this bit reads 0.

If a high-speed device is attached, the EHCI will automatically set the Port Enabled/Disabled bit in the PORTSC register and the debug software can proceed. Debug software should set the ENABLED_CNT bit in the Debug Port Control/Status register, and then reset (clear) the Port Enabled/Disabled bit in the PORTSC register (so that the system host controller driver does not see an enabled port when it is first loaded).

Debug Software Startup with Initialized EHCI

Debug software can attempt to use the debug port if the Current Connect Status bit in the appropriate (See Determining the Debug Port) PORTSC register is set. If the Current Connect Status bit is not set, then debug software may choose to terminate or it may choose to wait until a device is connected.

If a device is connected, then debug software must set the OWNER_CNT bit and then the ENABLED_CNT bit in the Debug Port Control/Status register.

Determining Debug Peripheral Presence

After enabling the debug port functionality, debug software can determine if a debug peripheral is attached by attempting to send data to the debug peripheral. If all attempts result in an error (Exception bits in the Debug Port Control/Status register

indicates a Transaction Error), then the attached device is not a debug peripheral. If the debug port peripheral is not present, then debug software may choose to terminate or it may choose to wait until a debug peripheral is connected.

5.19.10 EHCI Caching

EHCI Caching is a power management feature in the USB (EHCI) host controllers which enables the controller to execute the schedules entirely in cache and eliminates the need for the DMA engine to access memory when the schedule is idle. EHCI caching allows the processor to maintain longer C-state residency times and provides substantial system power savings.

5.19.11 USB Pre-Fetch Based Pause

The Pre-Fetch Based Pause is a power management feature in USB (EHCI) host controllers to ensure maximum C3/C4 processor power state time with C2 popup. This feature applies to the period schedule, and works by allowing the DMA engine to identify periods of idleness and preventing the DMA engine from accessing memory when the periodic schedule is idle. Typically in the presence of periodic devices with multiple millisecond poll periods, the periodic schedule will be idle for several frames between polls.

The USB Pre-Fetch Based Pause feature is disabled by setting bit 4 of EHCI Configuration Register Section 16.2.1.

5.19.12 USB Overcurrent Protection

The PCH has implemented programmable USB Overcurrent signals. The PCH provides a total of 8 overcurrent pins to be shared across the 14 ports.

Four overcurrent signals have been allocated to the ports in each USB Device:

- OC[3:0]# for Device 29 (Ports 0-7)
- OC[7:4]# for Device 26 (Ports 8-13)

Each pin is mapped to one or more ports by setting bits in the USBOCM1 and USBOCM2 registers.See Section 10.1.51 and Section 10.1.52. It is system BIOS' responsibility to ensure that each port is mapped to only one over current pin. Operation with more than one overcurrent pin mapped to a port is undefined. It is expected that multiple ports are mapped to a single overcurrent pin, however they should be connected at the port and not at the PCH pin. Shorting these pins together may lead to reduced test capabilities. By default, two ports are routed to each of the OC[6:0]# pins. OC7# is not used by default.

***Notes*:**

1. All USB ports routed out of the package must have Overcurrent protection. It is system BIOS responsibility to ensure all used ports have OC protection
2. USB Ports that are unused on the system (not routed out from the package) should not have OC pins assigned to them.

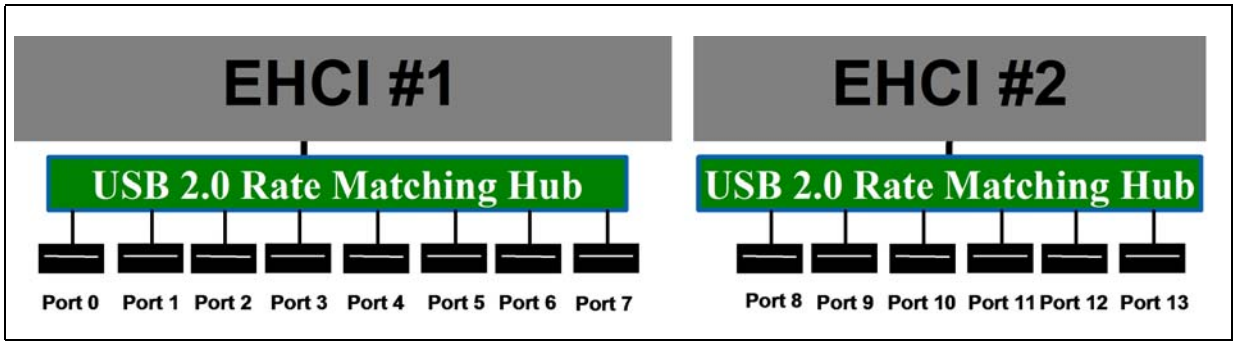
5.20 Integrated USB 2.0 Rate Matching Hub

5.20.1 Overview

The PCH has integrated two USB 2.0 Rate Matching Hubs (RMH). One hub is connected to each of the EHCI controllers as shown in the figure below. The Hubs convert low and full-speed traffic into high-speed traffic. When the RMHs are enabled, they will appear to software like an external hub is connected to Port 0 of each EHCI controller. In addition, port 1 of each of the RMHs is muxed with Port 1 of the EHCI controllers and is able to bypass the RMH for use as the Debug Port.

The hub operates like any USB 2.0 Discrete Hub and will consume one tier of hubs allowed by the USB 2.0 specification. section 4.1.1. A maximum of four additional non-root hubs can be supported on any of the PCH USB Ports. The RMH will report the following Vendor ID = 8087h and Product ID = 0024h.

Figure 5-9. EHCI with USB 2.0 with Rate Matching Hub



5.20.2 Architecture

A hub consists of three components: the Hub Repeater, the Hub Controller, and the Transaction Translator.

1. The Hub Repeater is responsible for connectivity setup and tear-down. It also supports exception handling, such as bus fault detection and recovery and connect/disconnect detect.
2. The Hub Controller provides the mechanism for host-to-hub communication. Hub-specific status and control commands permit the host to configure a hub and to monitor and control its individual downstream facing ports.
3. The Transaction Translator (TT) responds to high-speed split transactions and translates them to full-/low-speed transactions with full-/low-speed devices attached on downstream facing ports. There is 1 TT per RMH in PCH.

See chapter 11 of the USB 2.0 Specification for more details on the architecture of the hubs.

5.21 SMBus Controller

5.21.1 Host SMBus Controller (D31:F3)

The PCH provides an System Management Bus (SMBus) 2.0 host controller as well as an SMBus Slave Interface. The host controller provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves). The PCH is also capable of operating in a mode in which it can communicate with I^2C compatible devices.

The PCH can perform SMBus messages with either packet error checking (PEC) enabled or disabled. The actual PEC calculation and checking is performed in hardware by the PCH.

The Slave Interface allows an external master to read from or write to the PCH. Write cycles can be used to cause certain events or pass messages, and the read cycles can be used to determine the state of various status bits. The PCH's internal host controller cannot access the PCH's internal Slave Interface.

The PCH SMBus logic exists in Device 31:Function 3 configuration space, and consists of a transmit data path, and host controller. The transmit data path provides the data flow logic needed to implement the seven different SMBus command protocols and is controlled by the host controller. The PCH SMBus controller logic is clocked by RTC clock.

The SMBus Address Resolution Protocol (ARP) is supported by using the existing host controller commands through software, except for the new Host Notify command (which is actually a received message).

The programming model of the host controller is combined into two portions: a PCI configuration portion, and a system I/O mapped portion. All static configuration, such as the I/O base address, is done using the PCI configuration space. Real-time programming of the Host interface is done in system I/O space.

The PCH SMBus host controller checks for parity errors as a target. If an error is detected, the detected parity error bit in the PCI Status Register (Device 31:Function 3:Offset 06h:bit 15) is set. If bit 6 and bit 8 of the PCI Command Register (Device 31:Function 3:Offset 04h) are set, an SERR# is generated and the signaled SERR# bit in the PCI Status Register (bit 14) is set.

5.21.2 Host Controller

The SMBus host controller is used to send commands to other SMBus slave devices. Software sets up the host controller with an address, command, and, for writes, data and optional PEC; and then tells the controller to start. When the controller has finished transmitting data on writes, or receiving data on reads, it generates an SMI# or interrupt, if enabled.

The host controller supports 8 command protocols of the SMBus interface (see *System Management Bus (SMBus) Specification, Version 2.0*): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, Block Read/Write, Block Write–Block Read Process Call, and Host Notify.

The SMBus host controller requires that the various data and command fields be setup for the type of command to be sent. When software sets the START bit, the SMBus Host controller performs the requested transaction, and interrupts the processor (or generates an SMI#) when the transaction is completed. Once a START command has been issued, the values of the "active registers" (Host Control, Host Command, Transmit Slave Address, Data 0, Data 1) should not be changed or read until the interrupt status message (INTR) has been set (indicating the completion of the

command). Any register values needed for computation purposes should be saved prior to issuing of a new command, as the SMBus host controller updates all registers while completing the new command.

The PCH supports the *System Management Bus (SMBus) Specification, Version 2.0*. Slave functionality, including the Host Notify protocol, is available on the SMBus pins. The SMLink and SMBus signals can be tied together externally depending on TCO mode used. Refer to Section 5.14.2 for more details.

Using the SMB host controller to send commands to the PCH's SMB slave port is not supported.

5.21.2.1 Command Protocols

In all of the following commands, the Host Status Register (offset 00h) is used to determine the progress of the command. While the command is in operation, the HOST_BUSY bit is set. If the command completes successfully, the INTR bit will be set in the Host Status Register. If the device does not respond with an acknowledge, and the transaction times out, the DEV_ERR bit is set. If software sets the KILL bit in the Host Control Register while the command is running, the transaction will stop and the FAILED bit will be set.

Quick Command

When programmed for a Quick Command, the Transmit Slave Address Register is sent. The PEC byte is never appended to the Quick Protocol. Software should force the PEC_EN bit to 0 when performing the Quick Command. Software must force the I2C_EN bit to 0 when running this command. See section 5.5.1 of the *System Management Bus (SMBus) Specification*, Version 2.0 for the format of the protocol.

Send Byte / Receive Byte

For the Send Byte command, the Transmit Slave Address and Device Command Registers are sent. For the Receive Byte command, the Transmit Slave Address Register is sent. The data received is stored in the DATA0 register. Software must force the I2C_EN bit to 0 when running this command.

The Receive Byte is similar to a Send Byte, the only difference is the direction of data transfer. See sections 5.5.2 and 5.5.3 of the *System Management Bus (SMBus) Specification*, Version 2.0 for the format of the protocol.

Write Byte / Word

The first byte of a Write Byte/Word access is the command code. The next 1 or 2 bytes are the data to be written. When programmed for a Write Byte/Word command, the Transmit Slave Address, Device Command, and Data0 Registers are sent. In addition, the Data1 Register is sent on a Write Word command. Software must force the I2C_EN bit to 0 when running this command. See section 5.5.4 of the *System Management Bus (SMBus) Specification*, Version 2.0 for the format of the protocol.

Read Byte / Word

Reading data is slightly more complicated than writing data. First the PCH must write a command to the slave device. Then it must follow that command with a repeated start condition to denote a read from that device's address. The slave then returns 1 or 2 bytes of data. Software must force the I2C_EN bit to 0 when running this command.

When programmed for the read byte/word command, the Transmit Slave Address and Device Command Registers are sent. Data is received into the DATA0 on the read byte, and the DAT0 and DATA1 registers on the read word. See section 5.5.5 of the *System Management Bus (SMBus) Specification*, Version 2.0 for the format of the protocol.

Process Call

The process call is so named because a command sends data and waits for the slave to return a value dependent on that data. The protocol is simply a Write Word followed by a Read Word, but without a second command or stop condition.

When programmed for the Process Call command, the PCH transmits the Transmit Slave Address, Host Command, DATA0 and DATA1 registers. Data received from the device is stored in the DATA0 and DATA1 registers. The Process Call command with I2C_EN set and the PEC_EN bit set produces undefined results. Software must force either I2C_EN or PEC_EN to 0 when running this command. See section 5.5.6 of the *System Management Bus (SMBus) Specification*, Version 2.0 for the format of the protocol.

Note: For process call command, the value written into bit 0 of the Transmit Slave Address Register (SMB I/O register, offset 04h) needs to be 0.

Note: If the I2C_EN bit is set, the protocol sequence changes slightly: the Command Code (bits 18:11 in the bit sequence) are not sent - as a result, the slave will not acknowledge (bit 19 in the sequence).

Block Read / Write

The PCH contains a 32-byte buffer for read and write data which can be enabled by setting bit 1 of the Auxiliary Control register at offset 0Dh in I/O space, as opposed to a single byte of buffering. This 32-byte buffer is filled with write data before transmission, and filled with read data on reception. In the PCH, the interrupt is generated only after a transmission or reception of 32 bytes, or when the entire byte count has been transmitted/received.

Note: When operating in I^2C mode (I2C_EN bit is set), the PCH will never use the 32-byte buffer for any block commands.

The byte count field is transmitted but ignored by the PCH as software will end the transfer after all bytes it cares about have been sent or received.

For a Block Write, software must either force the I2C_EN bit or both the PEC_EN and AAC bits to 0 when running this command.

The block write begins with a slave address and a write condition. After the command code the PCH issues a byte count describing how many more bytes will follow in the message. If a slave had 20 bytes to send, the first byte would be the number 20 (14h), followed by 20 bytes of data. The byte count may not be 0. A Block Read or Write is allowed to transfer a maximum of 32 data bytes.

When programmed for a block write command, the Transmit Slave Address, Device Command, and Data0 (count) registers are sent. Data is then sent from the Block Data Byte register; the total data sent being the value stored in the Data0 Register. On block read commands, the first byte received is stored in the Data0 register, and the remaining bytes are stored in the Block Data Byte register. See section 5.5.7 of the *System Management Bus (SMBus) Specification*, Version 2.0 for the format of the protocol.

Note: For Block Write, if the I2C_EN bit is set, the format of the command changes slightly. The PCH will still send the number of bytes (on writes) or receive the number of bytes (on reads) indicated in the DATA0 register. However, it will not send the contents of the DATA0 register as part of the message. Also, the Block Write protocol sequence changes slightly: the Byte Count (bits 27:20 in the bit sequence) are not sent - as a result, the slave will not acknowledge (bit 28 in the sequence).

I²C Read

This command allows the PCH to perform block reads to certain I²C devices, such as serial E²PROMs. The SMBus Block Read supports the 7-bit addressing mode only.

However, this does not allow access to devices using the I²C "Combined Format" that has data bytes after the address. Typically these data bytes correspond to an offset (address) within the serial memory chips.

Note: This command is supported independent of the setting of the I2C_EN bit. The I²C Read command with the PEC_EN bit set produces undefined results. Software must force both the PEC_EN and AAC bit to 0 when running this command.

For I²C Read command, the value written into bit 0 of the Transmit Slave Address Register (SMB I/O register, offset 04h) needs to be 0.

The format that is used for the command is shown in Table 5-42.

Table 5-42. I²C Block Read

Bit	Description
1	Start
8:2	Slave Address — 7 bits
9	Write
10	Acknowledge from slave
18:11	Send DATA1 register
19	Acknowledge from slave
20	Repeated Start
27:21	Slave Address — 7 bits
28	Read
29	Acknowledge from slave
37:30	Data byte 1 from slave — 8 bits
38	Acknowledge
46:39	Data byte 2 from slave — 8 bits
47	Acknowledge
–	Data bytes from slave / Acknowledge
–	Data byte N from slave — 8 bits
–	NOT Acknowledge
–	Stop

The PCH will continue reading data from the peripheral until the NAK is received.

Block Write–Block Read Process Call

The block write-block read process call is a two-part message. The call begins with a slave address and a write condition. After the command code the host issues a write byte count (M) that describes how many more bytes will be written in the first part of the message. If a master has 6 bytes to send, the byte count field will have the value 6 (0000 0110b), followed by the 6 bytes of data. The write byte count (M) cannot be 0.

The second part of the message is a block of read data beginning with a repeated start condition followed by the slave address and a Read bit. The next byte is the read byte count (N), which may differ from the write byte count (M). The read byte count (N) cannot be 0.

The combined data payload must not exceed 32 bytes. The byte length restrictions of this process call are summarized as follows:

- M ≥ 1 byte
- N ≥ 1 byte
- M + N ≤ 32 bytes

The read byte count does not include the PEC byte. The PEC is computed on the total message beginning with the first slave address and using the normal PEC computational rules. It is highly recommended that a PEC byte be used with the Block Write-Block Read Process Call. Software must do a read to the command register (offset 2h) to reset the 32 byte buffer pointer prior to reading the block data register.

There is no STOP condition before the repeated START condition, and that a NACK signifies the end of the read transfer.

Note: E32B bit in the Auxiliary Control register must be set when using this protocol.

See section 5.5.8 of the *System Management Bus (SMBus) Specification*, Version 2.0 for the format of the protocol.

5.21.3 Bus Arbitration

Several masters may attempt to get on the bus at the same time by driving the SMBDATA line low to signal a start condition. The PCH continuously monitors the SMBDATA line. When the PCH is attempting to drive the bus to a 1 by letting go of the SMBDATA line, and it samples SMBDATA low, then some other master is driving the bus and the PCH will stop transferring data.

If the PCH sees that it has lost arbitration, the condition is called a collision. The PCH will set the BUS_ERR bit in the Host Status Register, and if enabled, generate an interrupt or SMI#. The processor is responsible for restarting the transaction.

When the PCH is a SMBus master, it drives the clock. When the PCH is sending address or command as an SMBus master, or data bytes as a master on writes, it drives data relative to the clock it is also driving. It will not start toggling the clock until the start or stop condition meets proper setup and hold time. The PCH will also guarantee minimum time between SMBus transactions as a master.

Note: The PCH supports the same arbitration protocol for both the SMBus and the System Management (SMLink) interfaces.

5.21.4 Bus Timing

5.21.4.1 Clock Stretching

Some devices may not be able to handle their clock toggling at the rate that the PCH as an SMBus master would like. They have the capability of stretching the low time of the clock. When the PCH attempts to release the clock (allowing the clock to go high), the clock will remain low for an extended period of time.

The PCH monitors the SMBus clock line after it releases the bus to determine whether to enable the counter for the high time of the clock. While the bus is still low, the high time counter must not be enabled. Similarly, the low period of the clock can be stretched by an SMBus master if it is not ready to send or receive data.

5.21.4.2 Bus Time Out (PCH as SMBus Master)

If there is an error in the transaction, such that an SMBus device does not signal an acknowledge, or holds the clock lower than the allowed time-out time, the transaction will time out. The PCH will discard the cycle and set the DEV_ERR bit. The time out minimum is 25 ms (800 RTC clocks). The time-out counter inside the PCH will start after the last bit of data is transferred by the PCH and it is waiting for a response.

The 25 ms timeout counter will not count under the following conditions:

1. BYTE_DONE_STATUS bit (SMBus I/O Offset 00h, bit 7) is set
2. The SECOND_TO_STS bit (TCO I/O Offset 06h, bit 1) is not set (this indicates that the system has not locked up).

5.21.5 Interrupts / SMI#

The PCH SMBus controller uses PIRQB# as its interrupt pin. However, the system can alternatively be set up to generate SMI# instead of an interrupt, by setting the SMBUS_SMI_EN bit (Device 31:Function 0:Offset 40h:bit 1).

Table 5-44 and Table 5-45 specify how the various enable bits in the SMBus function control the generation of the interrupt, Host and Slave SMI, and Wake internal signals. The rows in the tables are additive, which means that if more than one row is true for a particular scenario then the Results for all of the activated rows will occur.

Table 5-43. Enable for SMBALERT#

Event	INTREN (Host Control I/O Register, Offset 02h, Bit 0)	SMB_SMI_EN (Host Configuration Register, D31:F3:Offset 40h, Bit 1)	SMBALERT_DIS (Slave Command I/O Register, Offset 11h, Bit 2)	Result
SMBALERT# asserted low (always reported in Host Status Register, Bit 5)	X	X	X	Wake generated
	X	1	0	Slave SMI# generated (SMBUS_SMI_STS)
	1	0	0	Interrupt generated

Table 5-44. Enables for SMBus Slave Write and SMBus Host Events

Event	INTREN (Host Control I/O Register, Offset 02h, Bit 0)	SMB_SMI_EN (Host Configuration Register, D31:F3:Offset 40h, Bit1)	Event
Slave Write to Wake/ SMI# Command	X	X	Wake generated when asleep. Slave SMI# generated when awake (SMBUS_SMI_STS).
Slave Write to SMLINK_SLAVE_SMI Command	X	X	Slave SMI# generated when in the S0 state (SMBUS_SMI_STS)
Any combination of Host Status Register [4:1] asserted	0	X	None
	1	0	Interrupt generated
	1	1	Host SMI# generated

Table 5-45. Enables for the Host Notify Command

HOST_NOTIFY_INTREN (Slave Control I/O Register, Offset 11h, Bit 0)	SMB_SMI_EN (Host Config Register, D31:F3:Off40h, Bit 1)	HOST_NOTIFY_WKEN (Slave Control I/O Register, Offset 11h, Bit 1)	Result
0	X	0	None
X	X	1	Wake generated
1	0	X	Interrupt generated
1	1	X	Slave SMI# generated (SMBUS_SMI_STS)

5.21.6 SMBALERT#

SMBALERT# is multiplexed with GPIO[11]. When enable and the signal is asserted, The PCH can generate an interrupt, an SMI#, or a wake event from S1–S5.

5.21.7 SMBus CRC Generation and Checking

If the AAC bit is set in the Auxiliary Control register, the PCH automatically calculates and drives CRC at the end of the transmitted packet for write cycles, and will check the CRC for read cycles. It will not transmit the contents of the PEC register for CRC. The PEC bit must not be set in the Host Control register if this bit is set, or unspecified behavior will result.

If the read cycle results in a CRC error, the DEV_ERR bit and the CRCE bit in the Auxiliary Status register at offset 0Ch will be set.

5.21.8 SMBus Slave Interface

The PCH's SMBus Slave interface is accessed using the SMBus. The SMBus slave logic will not generate or handle receiving the PEC byte and will only act as a Legacy Alerting Protocol device. The slave interface allows the PCH to decode cycles, and allows an external microcontroller to perform specific actions. Key features and capabilities include:

- Supports decode of three types of messages: Byte Write, Byte Read, and Host Notify.
- Receive Slave Address register: This is the address that the PCH decodes. A default value is provided so that the slave interface can be used without the processor having to program this register.
- Receive Slave Data register in the SMBus I/O space that includes the data written by the external microcontroller.
- Registers that the external microcontroller can read to get the state of the PCH.
- Status bits to indicate that the SMBus slave logic caused an interrupt or SMI# due to the reception of a message that matched the slave address.
  - Bit 0 of the Slave Status Register for the Host Notify command
  - Bit 16 of the Intel SMI Status Register Section 13.8.3.8 for all others

Note: The external microcontroller should not attempt to access the PCH's SMBus slave logic until either:

- 800 milliseconds after both: RTCRST# is high and RSMRST# is high, OR
- The PLTRST# de-asserts

If a master leaves the clock and data bits of the SMBus interface at 1 for 50 µs or more in the middle of a cycle, the PCH slave logic's behavior is undefined. This is interpreted as an unexpected idle and should be avoided when performing management activities to the slave logic.

Note: When an external microcontroller accesses the SMBus Slave Interface over the SMBus a translation in the address is needed to accommodate the least significant bit used for read/write control. For example, if the PCH slave address (RCV_SLVA) is left at 44h (default), the external micro controller would use an address of 88h/89h (write/read).

5.21.8.1 Format of Slave Write Cycle

The external master performs Byte Write commands to the PCH SMBus Slave I/F. The "Command" field (bits 11:18) indicate which register is being accessed. The Data field (bits 20:27) indicate the value that should be written to that register.

Table 5-46 has the values associated with the registers.

Table 5-46. Slave Write Registers

Register	Function
0	Command Register. See Table 5-47 below for legal values written to this register.
1–3	Reserved
4	Data Message Byte 0
5	Data Message Byte 1
6–7	Reserved
8	Reserved
9–FFh	Reserved

Note: The external microcontroller is responsible to make sure that it does not update the contents of the data byte registers until they have been read by the system processor. The PCH overwrites the old value with any new value received. A race condition is possible where the new value is being written to the register just at the time it is being read. PCH will not attempt to cover this race condition (that is, unpredictable results in this case).

Table 5-47. Command Types (Sheet 1 of 2)

Command Type	Description
0	Reserved
1	**WAKE/SMI#.** This command wakes the system if it is not already awake. If system is already awake, an SMI# is generated. ***Note:*** The SMB_WAK_STS bit will be set by this command, even if the system is already awake. The Intel SMI handler should then clear this bit.
2	**Unconditional Powerdown.** This command sets the PWRBTNOR_STS bit, and has the same effect as the Powerbutton Override occurring.
3	**HARD RESET WITHOUT CYCLING:** This command causes a hard reset of the system (does not include cycling of the power supply). This is equivalent to a write to the CF9h register with bits 2:1 set to 1, but bit 3 set to 0.
4	**HARD RESET SYSTEM.** This command causes a hard reset of the system (including cycling of the power supply). This is equivalent to a write to the CF9h register with bits 3:1 set to 1.
5	**Disable the TCO Messages.** This command will disable the PCH from sending Heartbeat and Event messages (as described in Section 5.15). Once this command has been executed, Heartbeat and Event message reporting can only be re-enabled by assertion and deassertion of the RSMRST# signal.
6	**WD RELOAD:** Reload watchdog timer.

Table 5-47. Command Types (Sheet 2 of 2)

Command Type	Description
7	Reserved
8	**SMLINK_SLV_SMI.** When PCH detects this command type while in the S0 state, it sets the SMLINK_SLV_SMI_STS bit. This command should only be used if the system is in an S0 state. If the message is received during S1–S5 states, the PCH acknowledges it, but the SMLINK_SLV_SMI_STS bit does not get set. ***Note:*** It is possible that the system transitions out of the S0 state at the same time that the SMLINK_SLV_SMI command is received. In this case, the SMLINK_SLV_SMI_STS bit may get set but not serviced before the system goes to sleep. Once the system returns to S0, the Intel SMI associated with this bit would then be generated. Software must be able to handle this scenario.
9-FFh	Reserved.

5.21.8.2 Format of Read Command

The external master performs Byte Read commands to the PCH SMBus Slave interface. The "Command" field (bits 18:11) indicate which register is being accessed. The Data field (bits 30:37) contain the value that should be read from that register.

Table 5-48. Slave Read Cycle Format

Bit	Description	Driven by	Comment
1	Start	External Microcontroller	
2-8	Slave Address - 7 bits	External Microcontroller	Must match value in Receive Slave Address register
9	Write	External Microcontroller	Always 0
10	ACK	PCH	
11-18	Command code – 8 bits	External Microcontroller	Indicates which register is being accessed. See Table 5-49 below for list of implemented registers.
19	ACK	PCH	
20	Repeated Start	External Microcontroller	
21-27	Slave Address - 7 bits	External Microcontroller	Must match value in Receive Slave Address register
28	Read	External Microcontroller	Always 1
29	ACK	PCH	
30-37	Data Byte	PCH	Value depends on register being accessed. Table 5-49 below for list of implemented registers.
38	NOT ACK	External Microcontroller	
39	Stop	External Microcontroller	

Table 5-49. Data Values for Slave Read Registers (Sheet 1 of 2)

Register	Bits	Description
0	7:0	Reserved for capabilities indication. Should always return 00h. Future chips may return another value to indicate different capabilities.
1	2:0	System Power State 000 = S0 001 = S1 010 = Reserved 011 = S3 100 = S4 101 = S5 110 = Reserved 111 = Reserved
	7:3	Reserved
2	3:0	Reserved
	7:4	Reserved
3	5:0	**Watchdog Timer current value.** The Watchdog Timer has 10 bits, but this field is only 6 bits. If the current value is greater than 3Fh, PCH will always report 3Fh in this field.
	7:6	Reserved
4	0	1 = The **Intruder Detect** (INTRD_DET) bit is set. This indicates that the system cover has probably been opened.
	1	1 = BTI **Temperature Event** occurred. This bit will be set if the PCH's THRM# input signal is active. Else this bit will read "0."
	2	**DOA Processor Status**. This bit will be 1 to indicate that the processor is dead
	3	1 = **SECOND_TO_STS** bit set. This bit will be set after the second time-out (SECOND_TO_STS bit) of the Watchdog Timer occurs.
	6:4	Reserved. Will always be 0, but software should ignore.
	7	Reflects the value of the GPIO[11]/SMBALERT# pin (and is dependent upon the value of the GPI_INV[11] bit. If the GPI_INV[11] bit is 1, then the value in this bit equals the level of the GPI[11]/SMBALERT# pin (high = 1, low = 0). If the GPI_INV[11] bit is 0, then the value of this bit will equal the inverse of the level of the GPIO[11]/SMBALERT# pin (high = 0, low = 1).
5	0	**FWH bad bit.** This bit will be 1 to indicate that the FWH read returned FFh, which indicates that it is probably blank.
	1	Reserved
	2	**SYS_PWROK Power Failure Status:** This bit will be 1 if the SYSPWR_FLR bit in the GEN_PMCON_2 register is set.
	3	**INIT3_3V# due to receiving Shutdown message:** This event is visible from the reception of the shutdown message until a platform reset is done if the Shutdown Policy Select bit (SPS) is configured to drive INIT3_3V#. When the SPS bit is configured to generate PLTRST# based on shutdown, this register bit will always return 0. Events on signal will not create a event message
	4	Reserved
	5	**POWER_OK_BAD:** Indicates the failure core power well ramp during boot/resume. This bit will be active if the SLP_S3# pin is de-asserted and PCH_PWROK pin is not asserted.
	6	**Thermal Trip:** This bit will shadow the state of processor Thermal Trip status bit (CTS) (16.2.1.2, GEN_PMCON_2, bit 3). Events on signal will not create a event message
	7	Reserved: Default value is "X" ***Note:*** Software should not expect a consistent value when this bit is read through SMBUS/SMLink.
6	7:0	Contents of the Message 1 register. Refer to Section 13.9.8 for the description of this register.
7	7:0	Contents of the Message 2 register. Refer to Section 13.9.8 for the description of this register.
8	7:0	Contents of the TCO_WDCNT register. Refer to Section 13.9.9 for the description of this register.

Table 5-49. Data Values for Slave Read Registers (Sheet 2 of 2)

Register	Bits	Description
9	7:0	Seconds of the RTC
A	7:0	Minutes of the RTC
B	7:0	Hours of the RTC
C	7:0	"Day of Week" of the RTC
D	7:0	"Day of Month" of the RTC
E	7:0	Month of the RTC
F	7:0	Year of the RTC
10h–FFh	7:0	Reserved

Behavioral Notes

According to SMBus protocol, Read and Write messages always begin with a Start bit –Address– Write bit sequence. When the PCH detects that the address matches the value in the Receive Slave Address register, it will assume that the protocol is always followed and ignore the Write bit (bit 9) and signal an Acknowledge during bit 10. In other words, if a Start –Address–Read occurs (which is illegal for SMBus Read or Write protocol), and the address matches the PCH's Slave Address, the PCH will still grab the cycle.

Also according to SMBus protocol, a Read cycle contains a Repeated Start–Address–Read sequence beginning at bit 20. Once again, if the Address matches the PCH's Receive Slave Address, it will assume that the protocol is followed, ignore bit 28, and proceed with the Slave Read cycle.

Note: An external microcontroller must not attempt to access the PCH's SMBus Slave logic until at least 1 second after both RTCRST# and RSMRST# are deasserted (high).

5.21.8.3 Slave Read of RTC Time Bytes

The PCH SMBus slave interface allows external SMBus master to read the internal RTC's time byte registers.

The RTC time bytes are internally latched by the PCH's hardware whenever RTC time is not changing and SMBus is idle. This ensures that the time byte delivered to the slave read is always valid and it does not change when the read is still in progress on the bus. The RTC time will change whenever hardware update is in progress, or there is a software write to the RTC time bytes.

The PCH SMBus slave interface only supports Byte Read operation. The external SMBus master will read the RTC time bytes one after another. It is software's responsibility to check and manage the possible time rollover when subsequent time bytes are read.

For example, assuming the RTC time is 11 hours: 59 minutes: 59 seconds. When the external SMBus master reads the hour as 11, then proceeds to read the minute, it is possible that the rollover happens between the reads and the minute is read as 0. This results in 11 hours: 0 minute instead of the correct time of 12 hours: 0 minutes. Unless it is certain that rollover will not occur, software is required to detect the possible time rollover by reading multiple times such that the read time bytes can be adjusted accordingly if needed.

5.21.8.4 Format of Host Notify Command

The PCH tracks and responds to the standard Host Notify command as specified in the *System Management Bus (SMBus) Specification*, Version 2.0. The host address for this command is fixed to 0001000b. If the PCH already has data for a previously-received host notify command which has not been serviced yet by the host software (as indicated by the HOST_NOTIFY_STS bit), then it will NACK following the host address byte of the protocol. This allows the host to communicate non-acceptance to the master and retain the host notify address and data values for the previous cycle until host software completely services the interrupt.

Note: Host software must always clear the HOST_NOTIFY_STS bit after completing any necessary reads of the address and data registers.

Table 5-50 shows the Host Notify format.

Table 5-50. Host Notify Format

Bit	Description	Driven By	Comment
1	Start	External Master	
8:2	SMB Host Address — 7 bits	External Master	Always 0001_000
9	Write	External Master	Always 0
10	ACK (or NACK)	PCH	PCH NACKs if HOST_NOTIFY_STS is 1
17:11	Device Address – 7 bits	External Master	Indicates the address of the master; loaded into the Notify Device Address Register
18	Unused — Always 0	External Master	7-bit-only address; this bit is inserted to complete the byte
19	ACK	PCH	
27:20	Data Byte Low — 8 bits	External Master	Loaded into the Notify Data Low Byte Register
28	ACK	PCH	
36:29	Data Byte High — 8 bits	External Master	Loaded into the Notify Data High Byte Register
37	ACK	PCH	
38	Stop	External Master	

5.22 Thermal Management

5.22.1 Thermal Sensor

The PCH incorporates one on-die Digital thermal sensor (DTS) for thermal management. The thermal sensor can provide PCH temperature information to an EC or SIO device that can be used to determine how to control the fans.

This thermal sensor is located near the DMI interface. The on-die thermal sensor is placed as close as possible to the hottest on-die location to reduce thermal gradients and to reduce the error on the sensor trip thresholds. The thermal Sensor trip points may be programmed to generate various interrupts including SCI, Intel SMI, PCI and other General Purpose events.

5.22.1.1 Internal Thermal Sensor Operation

The internal thermal sensor reports four trip points: Aux2, Aux, Hot and Catastrophic trip points in the order of increasing temperature.

Aux, Aux2 Temperature Trip Points

These trip points may be set dynamically if desired and provides an interrupt to ACPI (or other software) when it is crossed in either direction. These auxiliary temperature trip points do not automatically cause any hardware throttling but may be used by software to trigger interrupts. This trip point is set below the Hot temperature trip point and responses are separately programmable from the hot temperature settings, in order to provide incrementally more aggressive actions. Aux and Aux2 trip points are fully Software programmable during system run-time. Aux2 trip point is set below the Aux temperature trip point.

Hot Temperature Trip Point

This trip point may be set dynamically if desired and provides an interrupt to ACPI (or other software) when it is crossed in either direction. Software could optionally set this as an Interrupt when the temperature exceeds this level setting. Hot trip does not provide any default hardware based thermal throttling, and is available only as a customer configurable interrupt when $T_{j,max}$ has been reached.

Catastrophic Trip Point

This trip point is set at the temperature at which the PCH must be shut down immediately without any software support. The catastrophic trip point must correspond to a temperature ensured to be functional in order for the interrupt generation and Hardware response. Hardware response using THERMTRIP# would be an unconditional transition to S5. The catastrophic transition to the S5 state does not enforce a minimum time in the S5 state. It is assumed that the S5 residence and the reboot sequence cools down the system. If the catastrophic condition remains when the catastrophic power down enable bit is set by BIOS, then the system will re-enter S5.

Thermometer Mode

The thermometer is implemented using a counter that starts at 0 and increments during each sample point until the comparator indicates the temperature is above the current value. The value of the counter is loaded into a read-only register (Thermal Sensor Thermometer Read) when the comparator first trips.

5.22.1.1.1 Recommended Programming for Available Trip Points

There may be a ±2 °C offset due to thermal gradient between the hot-spot and the location of the thermal sensor. Trip points should be programmed to account for this temperature offset between the hot-spot $T_{j,max}$ and the thermal sensor.

Aux Trip Points should be programmed for software and firmware control using interrupts.

Hot Trip Point should be set to throttle at 108°C ($T_{j,max}$) due to DTS trim accuracy adjustments. Hot trip points should also be programmed for a software response.

Catastrophic Trip Point should be set to halt operation to avoid maximum T_j of about 120 °C.

Note: Crossing a trip point in either direction may generate several types of interrupts. Each trip point has a register that can be programmed to select the type of interrupt to be generated. Crossing a trip point is implemented as edge detection on each trip point to generate the interrupts.

5.22.1.1.2 Thermal Sensor Accuracy ($T_{accuracy}$)

$T_{accuracy}$ for PCH is ±5 °C in the temperature range 90°C to 120°C. $T_{accuracy}$ is ±10 °C for temperatures from 45 °C – 90 °C. PCH may not operate above +108 °C. This value is based on product characterization and is not ensured by manufacturing test.

Software has the ability to program the Tcat, Thot, and Taux trip points, but these trip points should be selected with consideration for the thermal sensor accuracy and the quality of the platform thermal solution. Overly conservative (unnecessarily low) temperature settings may unnecessarily degrade performance due to frequent throttling, while overly aggressive (dangerously high) temperature settings may fail to protect the part against permanent thermal damage.

5.22.2 Thermal Reporting Over System Management Link 1 Interface (SMLink1)

SMLink1 interface in the PCH is the SMBus link to an optional external controller. A SMBus protocol is defined on the PCH to allow compatible devices such as Embedded Controller (EC) or SIO to obtain system thermal data from sensors integrated into components on the system using the SMLink1 interface. The sensors that can be monitored using the SMLink1 include those in the processor, PCH, and DIMMs with sensors implemented. This solution allows an external device or controller to use the system thermal data for system thermal management.

Note: To enable Thermal Reporting, the Thermal Data Reporting enable and processor/PCH/DIMM temperature read enables have to be set in the Thermal Reporting Control (TRC) Register (See Section 22.2 for details on Register)

There are 2 uses for the PCH's thermal reporting capability:

1. To provide system thermal data to an external controller. The controller can manage the fans and other cooling elements based on this data. In addition, the PCH can be programmed by setting appropriate bits in the Alert Enable (AE) Register (See Section 22.2 for details on this register) to alert the controller when a device has gone outside of its temperature limits. The alert causes the assertion of the PCH's TEMP_ALERT# (SATA5GP/GPIO49/TEMP_ALERT#) signal. See Section 5.22.2.6 for more details.
2. To provide an interface between the external controller and host software. This software interface has no direct affect on the PCH's thermal collection. It is strictly a software interface to pass information or data.

The PCH responds to thermal requests only when the system is in S0 or S1. Once the PCH has been programmed, it will start responding to a request while the system is in S0 or S1.

To implement this thermal reporting capability, the platform is required to have appropriate Intel ME firmware, BIOS support, and compatible devices that support the SMBus protocol.

5.22.2.1 Supported Addresses

The PCH supports 2 addresses: I^2C Address for writes and Block Read Address for reads. These addresses need to be distinct.

The two addresses may be fixed by the external controller, or programmable within the controller. The addresses used by the PCH are completely programmable.

5.22.2.1.1 I^2C* Address

This address is used for writes to the PCH.

- The address is set by soft straps which are values stored in SPI flash and are defined by the OEM. The address can be set to any value the platform requires.
- This address supports all the writes listed in Table 5-51 below.
- SMBus reads by the external controller to this address are not allowed and result in indeterminate behavior.

5.22.2.1.2 Block Read Address

This address is used for reads from the PCH.

- The address is set by soft straps or BIOS. It can be set to any value the platform requires.
- This address only supports SMBus Block Read command and not Byte or Word Read.
- The Block Read command is supported as defined in the SMBus 2.0 specification, with the command being 40h, and the byte count being provided by the PCH following the block read format in the SMBus specification.
- Writes are not allowed to this address, and result in indeterminate behavior.
- Packet Error Code (PEC) may be enabled or not, which is set up by BIOS.

5.22.2.2 I²C Write Commands to the Intel® ME

Table 5-51 lists the write commands supported by the Intel ME.

All bits in the write commands must be written to the PCH or the operation will be aborted. For example, for 6-bytes write commands, all 48 bits must be written or the operation will be aborted.

The command format follows the Block Write format of the SMBus specification.

Table 5-51. I²C Write Commands to the Intel® ME

Transaction	Slave Addr	Data Byte0 (Commd)	Data Byte 1 (Byte Count)	Data Byte 2	Data Byte 3	Data Byte 4	Data Byte 5	Data Byte 6	Data Byte 7
Write Processor Temp Limits	I²C	42h	4h	Lower Limit [15:8]	Lower Limit [7:0]	Upper Limit [15:8]	Upper Limit [7:0]		
Write PCH Temp Limits	I²C	44h	2h	Lower Limit [7:0]	Upper Limit [7:0]				
Write DIMM Temp Limits	I²C	45h	2h	Lower Limit [7:0]	Upper Limit [7:0]				

5.22.2.3 Block Read Command

The external controller may read thermal information from the PCH using the SMBus Block Read Command. Byte-read and Word-read SMBus commands are not supported. The reads use a different address than the writes.

The command format follows the Block Read format of the SMBus specification.

The PCH and external controller are set up by BIOS with the length of the read that is supported by the platform. The device must always do reads of the lengths set up by BIOS.

The PCH supports any one of the following lengths: 2, 4, 5, 9, 10, 14 or 20 bytes. The data always comes in the order described in Table 5-52, where 0 is the first byte received in time on the SMBus.

Table 5-52. Block Read Command – Byte Definition (Sheet 1 of 2)

Byte	Description
Byte 0	Processor Package temperature, in absolute degrees Celsius (C) It is a single byte for the highest temperature between the 2 components. This is not relative to some max or limit, but is the maximum in absolute degrees. If the processor temperature collection has errors, this field will be FFh. Read value represents bits [7:0] of PTV (Processor Temperature Value)
Byte 1	The PCH temp in degrees C. FFh indicates error condition. Read value represents bits [7:0] of ITV (Internal Temperature Values) Register described in Section 22.2. ***Note:*** Requires TRC (Thermal Reporting Control) Register bit [5] to be enabled. Please see Section 22.2.
Byte 4:2	Reserved
Byte 5	Thermal Sensor (TS) on DIMM 0 If DIMM not populated, or if there is no TS on DIMM, value will be 0h Read value represents bits[7:0] of DTV (DIMM Temperature Values) Register described in Section 22.2. ***Note:*** Requires TRC (Thermal Reporting Control) Register bit [0] to be enabled. Please see Section 22.2.

Table 5-52. Block Read Command – Byte Definition (Sheet 2 of 2)

Byte	Description
Byte 6	Thermal Sensor (TS) on DIMM 1 If DIMM not populated, or if there is no TS on DIMM, value will be 0h Read value represents bits[15:8] of DTV (DIMM Temperature Values) Register described in Section 22.2. ***Note:*** Requires TRC (Thermal Reporting Control) Register bit [1] to be enabled. Please see Section 22.2.
Byte 7	Thermal Sensor (TS) on DIMM 2 If DIMM not populated, or if there is no TS on DIMM, value will be 0h Read value represents bits[23:16] of DTV (DIMM Temperature Values) Register described in Section 22.2. ***Note:*** Requires TRC (Thermal Reporting Control) Register bit [2] to be enabled. Please see Section 22.2.
Byte 8	Thermal Sensor (TS) on DIMM 3 If DIMM not populated, or if there is no TS on DIMM, value will be 0h Read value represents bits[31:24] of DTV (DIMM Temperature Values) Register described in Section 22.2. ***Note:*** Requires TRC (Thermal Reporting Control) Register bit [3] to be enabled.
Byte 9	Sequence number. Can be used to check if PCH's FW or hardware is hung. See Section 5.22.2.9 for usage. This byte is updated every time the collected data is updated ***Note:*** Read value represents bits[23:16] of ITV (Internal Temperature Values) Register described in Section 22.2.
Byte 19:10	Reserved

A 2-byte read would provide both the PCH and processor temperature. A device that wants DIMM information would read 9 bytes.

5.22.2.4 Read Data Format

For each of the data fields an ERROR Code is listed below. This code indicates that the PCH failed in its access to the device. This would be for the case where the read returned no data, or some illegal value. In general that would mean the device is broken. The EC can treat the device that failed the read as broken or with some fail-safe mechanism.

5.22.2.4.1 PCH and DIMM Temperature

The temperature readings for the PCH, DIMM are 8-bit unsigned values from 0–255. The minimum granularity supported by the internal thermal sensor is 1°C. Thus, there are no fractional values for the PCH or DIMM temperatures.

Note the sensors used within the components do not support values below 0 degrees, so this field is treated as 8 bits (0-255) absolute and not 2's complement (-128 to 127).

Devices that are not present or that are disabled will be set to 0h. Devices that have a failed reading (that is, the read from the device did not return any legal value) will be set to FFh. A failed reading means that the attempt to read that device returned a failure. The failure could have been from a bus failure or that the device itself had an internal failure. For instance, a system may only have one DIMM and it would report only that one value, and the values for the other DIMM's would all be 00h.

5.22.2.5 Thermal Data Update Rate

The temperature values are updated every 200 ms in the PCH, so reading more often than that simply returns the same data multiple times. Also, the data may be up to 200 ms old if the external controller reads the data right before the next update window.

5.22.2.6 Temperature Comparator and Alert

The PCH has the ability to alert the external controller when temperatures are out of range. This is done using the PCH's TEMP_ALERT# signal. The alert is a simple comparator. If any device's temperature is outside the limit range for that device, then the signal is asserted (electrical low). This alert does not use the SML1ALERT#.

The PCH supports 3 ranges:

1. Processor Package range - upper and lower limit (8 bits each, in degrees C).
2. PCH range - upper and lower limit (8 bits each, in degrees C) for PCH temperature.
3. DIMM range - upper and lower limit (8 bits each, in degrees C), applies to all DIMM's (up to 4 supported) that are enabled. Disabled (unpopulated) DIMM's don't participate in the thermal compares.

The comparator checks if the device is within the specified range, including the limits. For example, a device that is at 100 degrees when the upper limit is 100 will not trigger the alert. Likewise, a device that is at 70 degrees when the lower limit is 70 will not trigger the alert.

The compares are done only on devices that have been enabled by BIOS for checking. Since BIOS knows how many DIMM's and processors are in the system, it enables the checking only for those devices that are physically present.

The compares are done in firmware, so all the compares are executed in one software loop and at the end, if there is any out of bound temperature, the PCH's TEMP_ALERT# signal is asserted.

When the external controller sees the TEMP_ALERT# signal low, it knows some device is out of range. It can read the temperatures and then change the limits for the devices. It may take up to 250 ms before the actual writes cause the signal to change state. For instance if the PCH is at 105 degrees and the limit is 100, the alert is triggered. If the controller changes the limits to 110, the TEMP_ALERT# signal may remain low until the next thermal sampling window (every 200 ms) occurs and only then go high, assuming the PCH was still within its limits.

At boot, the controller can monitor the TEMP_ALERT# signal state. When BIOS has finished all the initialization and enabled the temperature comparators, the TEMP_ALERT# signal will be asserted since the default state of the limit registers is 0h; hence, when the PCH first reads temperatures, they will be out of range. This is the positive indication that the external controller may now read thermal information and get valid data. If the TEMP_ALERT# signal is enabled and not asserted within 30 seconds after PLTRST#, the external controller should assume there is a fatal error and handle accordingly. In general the TEMP_ALERT# signal will assert within a 1-4 seconds, depending on the actual BIOS implementation and flow.

Note: The TEMP_ALERT# assertion is only valid when PLTRST# is deasserted. The controller should mask the state of this signal when PLTRST# is asserted. Since the controller may be powered even when the PCH and the rest of the platform are not, the signal may glitch as power is being asserted, thus the controller should wait until PLTRST# has deasserted before monitoring the signal.

5.22.2.6.1 Special Conditions

The external controller should have a graceful means of handling the following:

1. TEMP_ALERT# asserts, and the controller reads PCH, but all temperature values are within limits.
   In this case, the controller should assume that by the time the controller could read the data, it had changed and moved back within the limits.
2. External controller writes new values to temperature limits, but TEMP_ALERT# is still asserted after several hundred msecs. When read, the values are back within limits.
   In this case, the controller should treat this as case where the temperature changed and caused TEMP_ALERT# assertion, and then changed again to be back within limits.
3. There is the case where the external controller writes an update to the limit register, while the PCH is collecting the thermal information and updating the thermal registers. The limit change will only take affect when the write completes and the Intel ME can process this change. If the Intel ME is already in the process of collecting data and doing the compares, then it will continue to use the old limits during this round of compares, and then use the new limits in the next compare window.
4. Each SMBus write to change the limits is an atomic operation, but is distinct in itself. Therefore, the external controller could write PCH limit, and then write DIMM limit. In the middle of those 2 writes, the thermal collecting procedure could be called by the Intel ME, so that the comparisons for the limits are done with the new PCH limits but the old DIMM limits.

Note: The limit writes are done when the SMBus write is complete; therefore, the limits are updated atomically with respect to the thermal updates and compares. There is never a case where the compares and the thermal update are interrupted in the middle by the write of new limits. The thermal updates and compares are done as one non-interruptible routine, and then the limit writes would change the limit value outside of that routine.

5.22.2.7 BIOS Set Up

In order for the PCH to properly report temperature and enable alerts, the BIOS must configure the PCH at boot or from suspend/resume state by writing the following information to the PCH MMIO space. This information is NOT configurable using the external controller.

- Enables for each of the possible thermal alerts (PCH and DIMM). Each DIMM is enabled individually.
- Enables for reading DIMM and PCH temperatures. Each can be enabled individually.
- SMBus address to use for each DIMM.

Setting up the temperature calculation equations.

5.22.2.8 SMBus Rules

The PCH may NACK an incoming SMBus transaction. In certain cases the PCH will NACK the address, and in other cases it will NACK the command depending on internal conditions (for example, errors, busy conditions). Given that most of the cases are due to internal conditions, the external controller must alias a NACK of the command and a NACK of the address to the same behavior. The controller must not try to make any determination of the reason for the NACK, based on the type of NACK (command vs. address).

The PCH will NACK when it is enabled but busy. The external controller is required to retry up to 3 times when they are NACK'ed to determine if the FW is busy with a data update. When the data values are being updated by the Intel ME, it will force this NACK to occur so that the data is atomically updated to the external controller. In reality if there is a NACK because of the PCH being busy, in almost all cases the next read will succeed since the update internally takes very little time.

The only long delay where there can be a NACK is if the internal Intel ME engine is reset. This is due to some extreme error condition and is therefore rare. In this case the NACK may occur for up to 30 seconds. After that, the external controller must assume that the PCH will never return good data. Even in the best of cases, when this internal reset occurs, it will always be a second or 2 to re-enable responding.

5.22.2.8.1 During Block Read

On the Block Read, the PCH will respect the NACK and Stop indications from the external controller, but will consider this an error case. It will recover from this case and correctly handle the next SMBus request.

The PCH will honor STOP during the block read command and cease providing data. On the next Block Read, the data will start with byte 0 again. However, this is not a recommended usage except for 'emergency cases'. In general the external controller should read the entire length of data that was originally programmed.

5.22.2.8.2 Power On

On the Block Read, the PCH will respect the NACK and Stop indications from the external controller, but will consider this an error case. It will recover from this case and correctly handle the next SMBus request.

The PCH will honor STOP during the block read command and cease providing data. On the next Block Read, the data will start with byte 0 again. However, this is not a recommended usage except for 'emergency cases'. In general the external controller should read the entire length of data that was originally programmed.

5.22.2.9 Case for Considerations

Below are some corner cases and some possible actions that the external controller could take.

A1-byte sequence number is available to the data read by the external controller. Each time the PCH updates the thermal information it will increment the sequence number. The external controller can use this value as an indication that the thermal FW is actually operating. The sequence number will roll over to 00h when it reaches FFh.

1. Power on:

   The PCH will not respond to any SMBus activity (on SMLink1 interface) until it has loaded the thermal Firmware (FW), which in general would take 1-4 seconds. During this period the PCH will NACK any SMBus transaction from the external controller.

   The load should take 1-4 seconds, but the external controller should design for 30 seconds based on long delays for S4 resume which takes longer than normal power

up. This would be an extreme case, but for larger memory footprints and non-optimized recovery times, 30 seconds is a safe number to use for the timeout.

Recover/Failsafe: if PCH has not responded within 30 seconds, the external controller can assume that the system has had a major error and the external controller should ramp the fans to some reasonably high value.
The only recover from this is an internal reset on the PCH, which is not visible to the external controller. Therefore the external controller might choose to poll every 10-60 seconds (some fairly long period) hereafter to see if the PCH's thermal reporting has come alive.

2. PCH's Thermal FW hangs and requires an internal reset which is not visible to the external controller.

   The PCH will NACK any SMBus transaction from the external controller. The PCH may not be able to respond for up to 30 seconds while the FW is being reset and reconfigured.
   The external controller could choose to poll every 1-10 seconds to see if the thermal FW has been successfully reset and is now providing data.

   General recovery for this case is about 1 second, but 30 seconds should be used by the external controller at the timeout.

   Recovery/Failsafe: same as in case #1.

3. Fatal PCH error, causes a global reset of all components.

   When there is a fatal PCH error, a global reset may occur, and then case #1 applies.
   The external controller can observe, if desired, PLTRST# assertion as an indication of this event.

4. PCH thermal FW fails or is hung, but no reset occurs

   The sequence number will not be updated, so the external controller knows to go to failsafe after some number of reads (8 or so) return the same sequence number.
   The external controller could choose to poll every 1-10 seconds to see if the thermal FW has been successfully reset and working again.

   In the absence of other errors, the updates for the sequence number should never be longer than 400 ms, so the number of reads needed to indicate that there is a hang should be at around 2 seconds. But when there is an error, the sequence number may not get updated for seconds. In the case that the external controller sees a NACK from the PCH, then it should restart its sequence counter, or otherwise be aware that the NACK condition needs to be factored into the sequence number usage.

   The use of sequence numbers is not required, but is provided as a means to ensure correct PCH FW operation.

5. When PCH updates the Block Read data structure, the external controller gets a NACK during this period.

   To ensure atomicity of the SMBus data read with respect to the data itself, when the data buffer is being updated, the PCH will NACK the Block Read transaction.

   The update is only a few micro-seconds, so very short in terms of SMBus polling time; therefore, the next read should be successful. The external controller should attempt 3 reads to handle this condition before moving on.

   If the Block read has started (that is, the address is ACK'ed) then the entire read will complete successfully, and the PCH will update the data only after the SMBus read has completed.

6. System is going from S0 to S3/4/5. The thermal monitoring FW is fully operational if the system is in S0/S1, so the following only applies to S3/4/5.

   When the PCH detects the operating system request to go to S3/4/5, it will take the SMLink1 controller offline as part of the system preparation. The external controller will see a period where its transactions are getting NACK'ed, and then see SLP_S3# assert.

This period is relatively short (a couple of seconds depending on how long all the devices take to place themselves into the D3 state), and would be far less than the 30 second limit mentioned above.

7. TEMP_ALERT# - Since there can be an internal reset, the TEMP_ALERT# may get asserted after the reset. The external controller must accept this assertion and handle it.

5.22.2.9.1 Example Algorithm for Handling Transaction

One algorithm for the transaction handling could be summarized as follows. This is just an example to illustrate the above rules. There could be other algorithms that can achieve the same results.

1. Perform SMBus transaction.
2. If ACK, then continue
3. If NACK
   a. Try again for 2 more times, in case the PCH is busy updating data.
   b. If 3 successive transactions receive NACK, then
      - Ramp fans, assuming some general long reset or failure
      - Try every 1-10 seconds to see if SMBus transactions are now working
      - If they start then return to step 1
      - If they continue to fail, then stay in this step and poll, but keep the fans ramped up or implement some other failure recovery mechanism.

5.23 Intel® High Definition Audio Overview (D27:F0)

The PCH's High Definition Audio (HDA) controller communicates with the external codec(s) over the Intel High Definition Audio serial link. The controller consists of a set of DMA engines that are used to move samples of digitally encoded data between system memory and an external codec(s). The PCH implements four output DMA engines and 4 input DMA engines. The output DMA engines move digital data from system memory to a D-A converter in a codec. PCH implements a single Serial Data Output signal (HDA_SDOUT) that is connected to all external codecs. The input DMA engines move digital data from the A-D converter in the codec to system memory. The PCH implements four Serial Digital Input signals (HDA_SDI[3:0]) supporting up to four codecs.

Audio software renders outbound and processes inbound data to/from buffers in system memory. The location of individual buffers is described by a Buffer Descriptor List (BDL) that is fetched and processed by the controller. The data in the buffers is arranged in a predefined format. The output DMA engines fetch the digital data from memory and reformat it based on the programmed sample rate, bit/sample and number of channels. The data from the output DMA engines is then combined and serially sent to the external codecs over the Intel High Definition Audio link. The input DMA engines receive data from the codecs over the Intel High Definition Audio link and format the data based on the programmable attributes for that stream. The data is then written to memory in the predefined format for software to process. Each DMA engine moves one stream of data. A single codec can accept or generate multiple streams of data, one for each A-D or D-A converter in the codec. Multiple codecs can accept the same output stream processed by a single DMA engine.

Codec commands and responses are also transported to and from the codecs using DMA engines.

The PCH HD audio controller supports the Function Level Reset (FLR).

5.24 PCH Intel® ME Firmware

The PCH offers different firmware options depending on the design and platform usage models. In all cases, SPI Flash is required to connect to the PCH to load the Intel ME FW. Please also see platform specific Platform Design Guide for detailed hardware requirements.

5.24.1 High-End Desktop (HEDT) Platform Service (SPS) Firmware

SPS FW is for HEDT platforms. It comes in four flavors.

5.24.1.1 Silicon Enabling

This option provides the fundamental Intel ME FW functions required to boot a HEDT design. In addition it provides following functions:

- Dynamic fusing, which provides the ability to control availability of selected processor features for customer differentiation
- Power management controller (PMC) patching to provide a way of applying future enhancements or fixes to PMC

5.24.1.2 Intel® Intelligent Power Node Manager 2.0

Intel® Intelligent Power Node Manager 2.0 is a platform power reporting and capping technology, which provides an enhanced set of features, as compared to its previous version.

- — Intel Intelligent Power Node Manager 2.0 supports multiple power policies for multiple power domains, including thermal policies.
- — The enhanced algorithms provide shorter response times, enhanced dynamic range of power control, and reliable and uninterrupted power capping even during operating system or BMC failure.
- — By using an intelligent algorithm system, system performance is improved for a given power limit.
- — Power supply optimization technology reduces cost or improve efficiency of power supplies.
- — HEDT platform services is an accompanying function that provides access to PECI information by the BMC - critical selected information is available for efficient aggregated access by the BMC without losing the access to any other information available in a raw format.

5.24.1.3 Manageability Controller (MC) Compliant with Data Center Management Interface (DCMI) Specification

This option provides a building block infrastructure for OEMs to configure and adopt the manageability controller according to their platform design needs without spending development or engineering time for HEDT manageability. MC also provides an ability to interface with external Service Processors for advanced manageability requirements. Hardware features supported:

- Four PWM and Eight TACHS providing maximum of four Thermal zones with two TACHS per zone
- 12 GPIO dedicated for the Manageability Controller for LED and other controls
- Three SMBus Transports, two dedicated and one shared with Host
- SST, PECI and MEI transports
- Either Side-band SMBus Intel LOMs or Integrated MAC to external PHY
- LM75/TMP75 Thermal Sensors

- PMBus for Power Instrumentation and Control

Manageability Features supported:

- 128 Sensors capable to be configurable as I^2C, PECI, SST, GPIO, PMBus and Virtual Sensors.
- Up to 32 individually configurable actions based on the Sensors such as Fan Speed Control, LED Controls and any other custom build control mechanisms derived from the sensors.
- Piece-wise, Clamped algorithms for Fan Speed Control configurable through PIA.
- All commands of DCMI 1.5 including all DCMI 1.0 features.
- Additional IPMI commands for Chassis, Sensor, Storage, and Transport for Provisioning and Configuration for OEMs.
- IPMB communication to external HEDT Processors for Platform Events and Alerts.
- Well documented BIOS to MC interaction.
- Both the simple DCMI-compliant power management interface as well as the full Intel Intelligent Power Node Manager 2.0 interface for provisioning and data security.

Security Features:

- Security is provided for manufacturing data, user configuration and provisioning data through encryption using CBC-128 and xRC4.
- RMCP+ authentication and integrity algorithms support includes MD5, SHA1, and SHA-256.
- Capable of providing PSK and RSA certificate verification

5.24.1.4 Combined Intel® Intelligent Power Node Manager 2.0 and Management Controller Compliant with DCMI

A fourth SPS FW option combines both Intel Intelligent Power Node Manager 2.0 and DCMI features.

5.24.2 Intel® ME Requirements

Intel ME is a platform-level solution that utilizes multiple system components including:

- The Intel ME is the general purpose controller that resides in PCH. It operates in parallel to and is resource-isolated from the host processor.
- The flash device stores Intel ME firmware (FW) code that is executed by the Intel ME for its operations. In M0, the highest power state for Intel ME, this code is loaded from flash into DRAM and cached in secure and isolated SRAM. Code that resides in DRAM is stored in 16 MB of unified memory architecture (UMA) memory taken off the highest order rank in channel 0. PCH controls the flash device through the SPI interface and internal logic.
- In order to interface with DRAM, the Intel ME utilizes the integrated memory controller (IMC) present in the processor. DMI serves as the interface for communication between the IMC and Intel ME. This interfacing occurs in only M0 power state. In the lower Intel ME power state, M3, code is executed exclusively from secure and isolated Intel ME local RAM.
- BIOS to provide asset detection and POST diagnostics (BIOS and Intel ME FW can optionally share same flash memory device).

5.25 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is a 4-pin interface that provides a lower-cost alternative for system flash versus the Firmware Hub on the LPC bus.

The 4-pin SPI interface consists of clock (CLK), master data out (Master Out Slave In (MOSI)), master data in (Master In Slave Out (MISO)) and an active low chip select (SPI_CS[1:0]#).

The PCH supports up to two SPI flash devices using two separate Chip Select pins. Each SPI flash device can be up to 16 MB. The PCH SPI interface supports 20 MHz, 33 MHz and 50 MHz SPI devices. A SPI Flash device on with Chip Select 0 with a valid descriptor MUST be attached directly to the PCH.

Communication on the SPI bus is done with a Master – Slave protocol. The Slave is connected to the PCH and is implemented as a tri-state bus.

Note: If Boot BIOS Strap =”00” LPC is selected as the location for BIOS. BIOS may still be placed on LPC, but all platforms with PCH requires SPI flash connected directly to the PCH's SPI bus with a valid descriptor connected to Chip Select 0 in order to boot. Refer to Section 2.26 for details of Boot BIOS strap settings.

Note: When SPI is selected by the Boot BIOS Destination Strap and a SPI device is detected by the PCH, LPC based BIOS flash is disabled.

5.25.1 SPI Supported Feature Overview

SPI Flash on the PCH has two operational modes, descriptor and non-descriptor.

5.25.1.1 Non-Descriptor Mode

Non-Descriptor Mode is not supported as a valid flash descriptor is required for all PCH Platforms.

5.25.1.2 Descriptor Mode

Descriptor Mode is required for the PCH. It enables many new features of the chipset:

- Integrated Gigabit Ethernet and Host processor for Gigabit Ethernet Software
- Intel ME Firmware
- PCI Express root port configuration
- Supports up to two SPI components using two separate chip select pins
  - 1 SPI Flash and 1 user authentication device.
- Hardware enforced security restricting master accesses to different regions
- Chipset Soft Strap regions provides the ability to use Flash NVM as an alternative to hardware pull-up/pull-down resistors for PCH and Processor
- Supports the SPI Fast Read instruction and frequencies of up to 50 MHz
- Support Single Input, Dual Output Fast read
- Uses standardized Flash Instruction Set

5.25.1.2.1 SPI Flash Regions

In Descriptor Mode the Flash is divided into five separate regions:

Region	Content
0	Flash Descriptor
1	BIOS
2	Intel ME
3	Gigabit Ethernet
4	Platform Data

Only three masters can access the four regions: Host processor running BIOS code, Integrated Gigabit Ethernet and Host processor running Gigabit Ethernet Software, and Intel ME. The only required region is Region 0, the Flash Descriptor. Region 0 must be located in the first sector of device 0 (offset 0).

Flash Region Sizes

SPI flash space requirements differ by platform and configuration. The Flash Descriptor requires one 4 KB or larger block. GbE requires two 4 KB or larger blocks. The amount of flash space consumed is dependent on the erase granularity of the flash part and the platform requirements for the Intel ME and BIOS regions. The Intel ME region contains firmware to support Intel Active Management Technology, and other Intel ME capabilities.

Table 5-53. Region Size versus Erase Granularity of Flash Components

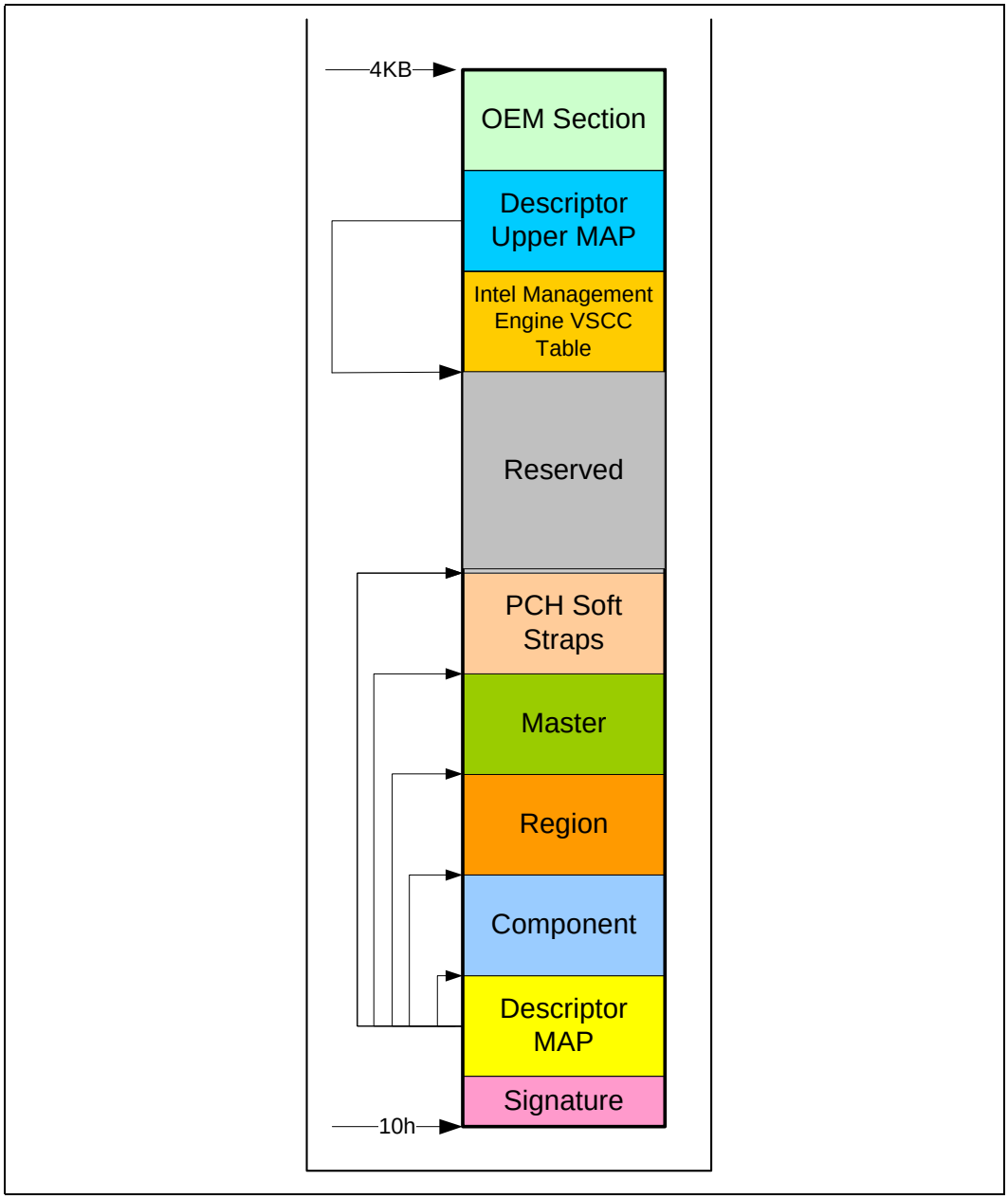
Region	Size with 4 KB Blocks	Size with 8 KB Blocks	Size with 64 KB Blocks
Descriptor	4 KB	8 KB	64 KB
GbE	8 KB	16 KB	128 KB
BIOS	Varies by Platform	Varies by Platform	Varies by Platform
ME	Varies by Platform	Varies by Platform	Varies by Platform

5.25.2 Flash Descriptor

The maximum size of the Flash Descriptor is 4 KB. If the block/sector size of the SPI flash device is greater than 4 KB, the flash descriptor will only use the first 4 KB of the first block. The flash descriptor requires its own block at the bottom of memory (00h). The information stored in the Flash Descriptor can only be written during the manufacturing process as its read/write permissions must be set to Read only when the computer leaves the manufacturing floor.

The Flash Descriptor is made up of eleven sections (see Figure 5-10).

Figure 5-10. Flash Descriptor Sections



1. The Flash signature selects Descriptor Mode as well as verifies if the flash is programmed and functioning. The data at the bottom of the flash (offset 10h) must be 0FF0A55Ah in order to be in Descriptor mode.
2. The Descriptor map has pointers to the other five descriptor sections as well as the size of each.
3. The component section has information about the SPI flash in the system including: the number of components, density of each, illegal instructions (such as chip erase), and frequencies for read, fast read and write/erase instructions.
4. The Region section points to the three other regions as well as the size of each region.

5. The master region contains the security settings for the flash, granting read/write permissions for each region and identifying each master by a requestor ID. See Section 5.25.2.1 for more information.

6 & 7. The Processor and PCH chipset soft strap sections contain Processor and PCH configurable parameters.

8. The Reserved region between the top of the Processor strap section and the bottom of the OEM Section is reserved for future chipset usages.

9. The Descriptor Upper MAP determines the length and base address of the Intel ME VSCC Table.

10. The Intel ME VSCC Table holds the JEDEC ID and the VSCC information of the entire SPI Flash supported by the NVM image.

11. OEM Section is 256 Bytes reserved at the top of the Flash Descriptor for use by OEM.

5.25.2.1 Descriptor Master Region

The master region defines read and write access setting for each region of the SPI device. The master region recognizes masters: BIOS Gigabit Ethernet, and Intel ME. Each master is only allowed to do direct reads of its primary regions.

Table 5-54. Region Access Control Table

Master Read/Write Access			
Region	**Processor and BIOS**	**Intel ME**	**GbE Controller**
Descriptor	N/A	N/A	N/A
BIOS	Processor and BIOS can always read from and write to BIOS Region	Read / Write	Read / Write
Intel ME	Read / Write	Intel ME can always read from and write to Intel ME Region	Read / Write
Gigabit Ethernet	Read / Write	Read / Write	GbE software can always read from and write to GbE region
Platform Data Region	N/A	N/A	N/A

5.25.3 Flash Access

There are two types of flash accesses:

Direct Access:

- Masters are allowed to do direct read only of their primary region.
  - Gigabit Ethernet region can only be directly accessed by the Gigabit Ethernet controller. Gigabit Ethernet software must use Program Registers to access the Gigabit Ethernet region.
- Master's Host or Intel ME virtual read address is converted into the SPI Flash Linear Address (FLA) using the Flash Descriptor Region Base/Limit registers.

Program Register Access:

- Program Register Accesses are not allowed to cross a 4 KB boundary and can not issue a command that might extend across two components.
- Software programs the FLA corresponding to the region desired.
  - Software must read the devices Primary Region Base/Limit address to create a FLA.

5.25.3.1 Direct Access Security

- Requester ID of the device must match that of the primary Requester ID in the Master Section
- Calculated Flash Linear Address must fall between primary region base/limit
- Direct Write not allowed
- Direct Read Cache contents are reset to 0's on a read from a different master
  - Supports the same cache flush mechanism in ICH7 which includes Program Register Writes

5.25.3.2 Register Access Security

- Only primary region masters can access the registers.

Note: Processor running Gigabit Ethernet software can access Gigabit Ethernet registers.

- Masters are only allowed to read or write those regions they have read/write permission.
- Using the Flash Region Access Permissions, one master can give another master read/write permissions to their area.
- Using the five Protected Range registers, each master can add separate read/write protection above that granted in the Flash Descriptor for their own accesses.
  - Example: BIOS may want to protect different regions of BIOS from being erased.
  - Ranges can extend across region boundaries.

5.25.4 Serial Flash Device Compatibility Requirements

A variety of serial flash devices exist in the market. For a serial flash device to be compatible with the PCH SPI bus, it must meet the minimum requirements detailed in the following sections.

Note: This PCH platform has require firmware.

Note: This PCH platform does not support AMT or Intel ME.

5.25.4.1 PCH SPI Based BIOS Requirements

A serial flash device must meet the following minimum requirements when used explicitly for system BIOS storage.

- Erase size capability of at least one of the following: 64 Kbytes, 8 Kbytes, 4 Kbytes, or 256 bytes.
- Device must support multiple writes to a page without requiring a preceding erase cycle (Refer to Section 5.25.5)
- Serial flash device must ignore the upper address bits such that an address of FFFFFFh aliases to the top of the flash memory.
- SPI Compatible Mode 0 support (clock phase is 0 and data is latched on the rising edge of the clock).
- If the device receives a command that is not supported or incomplete (less than 8 bits), the device must complete the cycle gracefully without any impact on the flash content.
- An erase command (page, sector, block, chip, etc.) must set all bits inside the designated area (page, sector, block, chip, and so forth) to 1 (Fh).

- Status Register bit 0 must be set to 1 when a write, erase or write to status register is in progress and cleared to 0 when a write or erase is NOT in progress.
- Devices requiring the Write Enable command must automatically clear the Write Enable Latch at the end of Data Program instructions.
- Byte write must be supported. The flexibility to perform a write between 1 byte to 64 bytes is recommended.
- Hardware Sequencing requirements are optional in BIOS only platforms.
- SPI flash parts that do not meet Hardware sequencing command set requirements may work in BIOS only platforms using software sequencing.

5.25.4.2 Integrated LAN Firmware SPI Flash Requirements

A serial flash device that will be used for system BIOS and Integrated LAN or Integrated LAN only must meet all the SPI Based BIOS Requirements plus:

- Hardware sequencing.
- 4, 8, or 64 KB erase capability must be supported.

5.25.4.2.1 SPI Flash Unlocking Requirements for Integrated LAN

BIOS must ensure there is no SPI flash based read/write/erase protection on the GbE region. GbE firmware and drivers for the integrated LAN need to be able to read, write and erase the GbE region at all times.

5.25.4.3 Intel® Management Engine (Intel® ME) Firmware SPI Flash Requirements

Intel ME Firmware must meet the SPI flash based BIOS Requirements plus:

- Hardware sequencing.
- Flash part must be uniform 4 KB erasable block throughout the entire device or have 64 KB blocks with the first block (lowest address) divided into 4 KB or 8 KB blocks.
- Write protection scheme must meet SPI flash unlocking requirements for Intel ME.

5.25.4.3.1 SPI Flash Unlocking Requirements for Intel® ME

Flash devices must be globally unlocked (read, write and erase access on the Intel ME region) from power on by writing 00h to the flash's status register to disable write protection.

If the status register must be unprotected, it must use the enable write status register command 50h or write enable 06h.

Opcode 01h (write to status register) must then be used to write a single byte of 00h into the status register. This must unlock the entire part. If the SPI flash's status register has non-volatile bits that must be written to, bits [5:2] of the flash's status register must be all 0h to indicate that the flash is unlocked.

If bits [5:2] return a non zero values, the Intel ME firmware will send a write of 00h to the status register. This must keep the flash part unlocked.

If there is no need to execute a write enable on the status register, then opcodes 06h and 50h must be ignored.

After global unlock, BIOS has the ability to lock down small sections of the flash as long as they do not involve the Intel ME or GbE region.

5.25.4.4 Hardware Sequencing Requirements

Table 5-55 contains a list of commands and the associated opcodes that a SPI-based serial flash device must support in order to be compatible with hardware sequencing.

Table 5-55. Hardware Sequencing Commands and Opcode Requirements

Commands	Opcode	Notes
Write to Status Register	01h	Writes a byte to SPI flash's status register. Enable Write to Status Register command must be run prior to this command.
Program Data	02h	Single byte or 64 byte write as determined by flash part capabilities and software.
Read Data	03h	
Write Disable	04h	
Read Status	05h	Outputs contents of SPI flash's status register
Write Enable	06h	
Fast Read	0Bh	
Enable Write to Status Register	50h or 60h	Enables a bit in the status register to allow an update to the status register
Erase	Programmable	256B, 4 Kbyte, 8 Kbyte or 64 Kbyte
Full Chip Erase	C7h	
JEDEC ID	9Fh	See Section 5.25.4.4.1.

5.25.4.4.1 Single Input, Dual Output Fast Read

The PCH now supports the functionality of a single input, dual output fast read. Opcode and address phase are shifted in serially to the serial flash SI (Serial In) pin. Data is read out after 8 clocks (dummy bits or wait states) from the both the SI and SO pin effectively doubling the through put of each fast read output. In order to enable this functionality, both Single Input Dual Output Fast Read Supported and Fast Read supported must be enabled.

5.25.4.4.2 Serial Flash Discoverable Parameters (SFDP)

As the number of features keeps growing in the serial flash, the need for correct, accurate configuration increases. A new method of determining configuration information is Serial Flash Discoverable Parameters (SFDP). Information such as VSCC values and flash attributes can be read directly from the flash parts. The discoverable parameter read opcode behaves like a fast read command. The opcode is 5Ah and the address cycle is 24 bits long. After the opcode 5Ah and address are clocked in, there will then be eight clocks (8 wait states) before valid data is clocked out. SFDP is a capability of the flash part, please confirm with target flash vendor to see if it is supported.

In order for BIOS to take advantage of the 5Ah opcode it needs to be programmed in the Software sequencing registers.

5.25.4.4.3 JEDEC ID

Since each serial flash device may have unique capabilities and commands, the JEDEC ID is the necessary mechanism for identifying the device so the uniqueness of the device can be comprehended by the controller (master). The JEDEC ID uses the opcode 9Fh and a specified implementation and usage model. This JEDEC Standard Manufacturer and Device ID read method is defined in Standard JESD21-C, PRN03-NV.

5.25.5 Multiple Page Write Usage Model

The system BIOS and Intel ME firmware usage model requires that the serial flash device support multiple writes to a page (minimum of 512 writes) without requiring a preceding erase command. BIOS commonly uses capabilities such as counters that are used for error logging and system boot progress logging. These counters are typically implemented by using byte-writes to 'increment' the bits within a page that have been designated as the counter. The Intel ME firmware usage model requires the capability for multiple data updates within any given page. These data updates occur using byte-writes without executing a preceding erase to the given page. Both the BIOS and Intel ME firmware multiple page write usage model applies to sequential and non-sequential data writes.

Note: This usage model requirement is based on any given bit only being written once from a '1' to a '0'without requiring the preceding erase. An erase would be required to change bits back to the 1 state.

5.25.5.1 Soft Flash Protection

There are two types of flash protection that are not defined in the flash descriptor supported by PCH:

1. BIOS Range Write Protection
2. SMI#-Based Global Write Protection

Both mechanisms are logically OR'd together such that if any of the mechanisms indicate that the access should be blocked, then it is blocked. Table 5-56 provides a summary of the mechanisms.

Table 5-56. Flash Protection Mechanism Summary

Mechanism	Accesses Blocked	Range Specific?	Reset-Override or SMI#-Override?	Equivalent Function on FWH
BIOS Range Write Protection	Writes	Yes	Reset Override	FWH Sector Protection
Write Protect	Writes	No	SMI# Override	Same as Write Protect in Intel ICHs for FWH

A blocked command will appear to software to finish, except that the Blocked Access status bit is set in this case.

5.25.5.2 BIOS Range Write Protection

The PCH provides a method for blocking writes to specific ranges in the SPI flash when the Protected BIOS Ranges are enabled. This is achieved by checking the Opcode type information (which can be locked down by the initial Boot BIOS) and the address of the requested command against the base and limit fields of a Write Protected BIOS range.

Note: Once BIOS has locked down the Protected BIOS Range registers, this mechanism remains in place until the next system reset.

5.25.5.3 SMI# Based Global Write Protection

The PCH provides a method for blocking writes to the SPI flash when the Write Protected bit is cleared (that is, protected). This is achieved by checking the Opcode type information (which can be locked down by the initial Boot BIOS) of the requested command.

The Write Protect and Lock Enable bits interact in the same manner for SPI BIOS as they do for the FWH BIOS.

5.25.6 Flash Device Configurations

The PCH-based platform must have a SPI flash connected directly to the PCH with a valid descriptor and Intel Firmware. BIOS may be stored in other locations such as Firmware Hub. Note this will not avoid the direct SPI flash connected to PCH requirement.

5.25.7 SPI Flash Device Recommended Pinout

Table 5-57 contains the recommended serial flash device pin-out for an 8-pin device. Use of the recommended pin-out on an 8-pin device reduces complexities involved with designing the serial flash device onto a motherboard and allows for support of a common footprint usage model (refer to Section 5.25.8.1).

Table 5-57. Recommended Pinout for 8-Pin Serial Flash Device

Pin #	Signal
1	Chips Select
2	Data Output
3	Write Protect
4	Ground
5	Data Input
6	Serial Clock
7	Hold / Reset
8	Supply Voltage

Although an 8-pin device is preferred over a 16-pin device due to footprint compatibility, the following table contains the recommended serial flash device pin-out for a 16-pin SOIC.

5.25.8 Serial Flash Device Package

Table 5-58. Recommended Pinout for 16-Pin Serial Flash Device

Pin #	Signal	Pin #	Signal
1	Hold / Reset	9	Write Protect
2	Supply Voltage	10	Ground
3	No Connect	11	No Connect
4	No Connect	12	No Connect
5	No Connect	13	No Connect
6	No Connect	14	No Connect
7	Chip Select	15	Serial Data In
8	Serial Data Out	16	Serial Clock

5.25.8.1 Common Footprint Usage Model

In order to minimize platform motherboard redesign and to enable platform Bill of Material (BOM) selectability, many PC System OEM's design their motherboard with a single common footprint. This common footprint allows population of a soldered down device or a socket that accepts a leadless device. This enables the board manufacturer to support, using selection of the appropriate BOM, either of these solutions on the same system without requiring any board redesign.

The common footprint usage model is desirable during system debug and by flash content developers since the leadless device can be easily removed and reprogrammed without damage to device leads. When the board and flash content is mature for high-volume production, both the socketed leadless solution and the soldered down leaded solution are available through BOM selection.

5.25.8.2 Serial Flash Device Package Recommendations

It is highly recommended that the common footprint usage model be supported. An example of how this can be accomplished is as follows:

- The recommended pinout for 8-pin serial flash devices is used (refer to Section 5.25.7).
- The 8-pin device is supported in either an 8-contact VDFPN (6x5 mm MLP) package or an 8-contact WSON (5x6 mm) package. These packages can fit into a socket that is land pattern compatible with the wide body SO8 package.
- The 8-pin device is supported in the SO8 (150 mil) and in the wide-body SO8 (200 mil) packages.

The 16-pin device is supported in the SO16 (300 mil) package.

5.26 Fan Control/Thermal Management

The PCH implements 4 PWM and 8 TACH signals for integrated fan speed control.

Note: Integrated fan speed control functionality requires a correctly configured system, including an appropriate processor, PCH with Intel® ME, Intel® ME Firmware, and system BIOS support.

5.26.1 PWM Outputs

This signal is driven as open-drain. An external pull-up resistor is integrated into the fan to provide the rising edge of the PWM output signal. The PWM output is driven low during reset, which represents 0% duty cycle to the fans. After reset de-assertion, the PWM output will continue to be driven low until one of the following occurs:

- The internal PWM control register is programmed to a non-zero value by the appropriate firmware.
- The watchdog timer expires (enabled and set at 4 seconds by default).
- The polarity of the signal is inverted by firmware.

If a PWM output will be programmed to inverted polarity for a particular fan, then the low voltage driven during reset represents 100% duty cycle to the fan.

5.26.2 TACH Inputs

This signal is driven as an open-collector or open-drain output from the fan. An external pull-up is expected to be implemented on the motherboard to provide the rising edge of the TACH input. This signal has analog hysteresis and digital filtering due

to the potentially slow rise and fall times. This signal has a weak internal pull-up resistor to keep the input buffer from floating if the TACH input is not connected to a fan.

5.27 Feature Capability Mechanism

A set of registers is included in the PCH LPC Interface (Device 31, Function 0, offset E0h - EBh) that allows the system software or BIOS to easily determine the features supported by PCH. These registers can be accessed through LPC PCI configuration space, thus allowing for convenient single point access mechanism for chipset feature detection.

This set of registers consists of:
Capability ID (FDCAP)
Capability Length (FDLEN)
Capability Version and Vendor-Specific Capability ID (FDVER)
Feature Vector (FVECT)

§ §

6 PCH Chipset Ballout Definition

This chapter contains the PCH ballout information.

Figure 6-1, Figure 6-2, Figure 6-3, and Figure 6-4 show the top-view ballout zoomed in from a top of package quadrant view.

Figure 6-1. PCH Ballout (Top View - Upper Left)

	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21
AW			VSS	VSS		VSS	CLKIN_SAS1P		VSS	SAS2TXN	VSS	SAS0TXN		VSS	SAS_RBIASN_0	VSS		HDA_RST#	VSS
AV		NC_3			TP15		CLKIN_SAS1N	SAS3TXN	SAS2TXP		SAS1TXN	SAS0TXP	CLKIN_SAS0P	SAS_RBIASP_0		GPIO13	LAD_1	PWM1	TACH0/GPIO17
AU	TP14		TP13		TP17	VSS	SAS3TXP		VSS	SAS1TXP	VSS	CLKIN_SAS0N		VSS	AD_8	VSS		AD_17	VSS
AT	TP16		GPIO33																
AR		TP18	LDRQ1#/GPIO23	AD_3		REQ1#/GPIO50/GSXCLK	AD_28		SAS7RXP	SAS6RXP		SAS5RXP	SAS4RXP		SAS3RXP	SAS2RXP		SAS1RXN	SAS0RXN
AP	VSS		VSS	AD_4					SAS7RXN	SAS6RXN					SAS3RXN	SAS2RXN			
AN	SAS5TXN	SAS4TXN	SAS4TXP	VSS		AD_20	GNT0#		VSS	VSS		SAS5RXN	SAS4RXN		VSS	VSS		SAS1RXP	SAS0RXP
AM		SAS5TXP		TACH7/GPIO71		VSS	VSS		C/BE0#	AD_15		VSS	VSS		AD_16	AD_24		VSS	VSS
AL	VSS	SAS6TXN	VSS	LAD_2		AD_27	C/BE2#		AD_14	AD_30		TP11	REQ0#		SAS_RBIASP_1	SAS_RBIASN_1		PIRQF#/GPIO3	AD_22
AK	SAS7TXN		SAS6TXP			REQ2#/GPIO52/GSXSLOAD	AD_21					PAR	AD_23					CLKIN_PCI	REQ3#/GPIO54/GSXSRESET#
AJ	VSS	SAS7TXP	VSS		TACH3/GPIO7	GNT2#/GPIO53/GSXDIN	VSS	DEVSEL#		PIRQB#	VSS	VccIO		VccIO	VccIO	VSS	VccRBIAS_SAS1	VccSAS1_5	
AH	HDA_SDIN_2	HDA_SDIN_3	HDA_SDIN_0									VccIO		VccIO	VccIO	VSS	VccRBIAS_SAS1	VccSAS1_5	
AG		HDA_SDIN_1		PWM3		TACH4/GPIO68	VSS	AD_19	AD_29	AD_18									
AF	VSS	USBP_7	VSS	LFRAME#		TACH6/GPIO70	VSS	PIRQE#/GPIO2	FRAME#	GNT3#/GPIO55		VccIO		VccIO	VccIO	VccIO	VccPLLSAS1	VccSAS1_5	
AE	USBP_6		USBN_7									VSS		VSS	VSS	VccIO	VSS	VSS	
AD	VSS	USBN_6	VSS		USBP_10	USBN_10	VSS	AD_26		VSS	V5REF	VccASW		VccASW	VccASW	VccSCUS	VccSCUS	VccSCUS	
AC		USBP_5			USBP_11	USBN_11	VSS	AD_10		vcc3_3	vcc3_3	VccASW		VccASW	VccASW	VccSCUS	VccSCUS	VccSCUS	
AB	USBP_4	USBN_4	USBN_5									VSS		VSS	VSS	VSS	VSS	VSS	
AA	VSS	USBP_3	VSS	USBP_12		USBN_12	VSS	PIRQG#/GPIO4	AD_31	AD_1									
Y	USBP_1		USBN_3	USBP_13		USBN_13	VSS	TACH5/GPIO69	TACH2/GPIO6	AD_6		VccIO		VccIO	VccIO	VccASW	VccASW	VccASW	

Figure 6-2. PCH Ballout (Top View - Upper Right)

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
AD_11	VSS		PWM0	VSS	AD_0		VSS	AD_9	VSS	SAS_CLOCK2		VSS	PEG0_RP_3	VSS		VSS	VSS			AW
	STOP#	PIRQC#	HDA_SYNC		LAD_0	AD_5	AD_25	REFCLK14IN		SAS_LOAD2	SAS_DATAOUT1	PEG0_RN_3		PEG0_RP_2	PEG0_RN_1			NC_4		AV
C/BE3#	VSS		LAD_3	VSS	GNT1#/GPIO51/GSXDOUT		VSS	AD_7	VSS	SAS_DATAIN2		VSS	PEG0_RN_2	VSS	PEG0_RP_1		PEG0_RN_0		TP10	AU
																	PEG0_RP_0		TP8	AT
	PIRQA#	PIRQD#		PIRQH#/GPIO5	PLOCK#		PWM2	TRDY#		SAS_DATAOUT2	SAS_LED#		PEG0_TN_3	PEG0_TP_2		PEG0_TN_1	VSS	VCCXUS		AR
	LDRQ0#	IRDY#					NC_1	AD_13					PEG0_TP_3	PEG0_TN_2			PEG0_TN_0		TP9	AP
	VSS	VSS		SERR#	AD_2		VSS	VSS		SAS_LOAD1	VCCXUS		VSS	VSS		PEG0_TP_1	PEG0_TP_0	TP7	CLKIN_SPCIE0N	AN
	PERR#	AD_12		VSS	VSS		SASSMBDATA2			VSS	VSS					VSS		CLKIN_SPCIE0P		AM
	TACH1/GPIO1	C/BE1#		GPIO64	GPIO66		SASSMBCLK2		SASSMBDATA0	VSS	SAS_DATAIN1	SAS_CLOCK1		VSS	PEG0_RBIASN	PEG0_RBIASP	VSS	PETN8	VSS	AL
				GPIO65	GPIO67												PETP8		PETN7	AK
VccPLLSAS0	VSS	vcc3_3	VSS	VCCXUS	VCCXUS		VCCRBIAS_PU	SASSMBCLK0	VSS		PERN8	PERP8	VSS	PERN4	PERP4		VSS	PETP7	VSS	AJ
VccPLLSAS0	VSS	vcc3_3	VSS	VCCXUS	VCCXUS		SASSMBCLK1	SASSMBDATA1	VSS		PERP7	PERN7	VSS	PERN3	PERP3		PETP6	PETN6	PETN5	AH
																		PETP5		AG
VccRBIAS_SAS0	VSS	VSS	VCCXUS	VCCXUS	VccPLLEXPU			VCCXUS	VCCXUS	VSS	PERP6	PERN6		VSS	PERN2	PERP2	VSS	PETN4	VSS	AF
VSS	VSS	VSS	VSS	VSS	VSS			VCCXUS	VccIO	VSS	PERP5	PERN5		VSS	PERP1	PERN1	PETP4		PETN3	AE
vccCore	vccCore	vccCore	vccCore	vccCore	VCCXUS												VSS	PETP3	VSS	AD
vccCore	vccCore	vccCore	vccCore	vccCore	VCCXUS		VccIO	VccIO	VSS		VccIO	VccIO	VSS	Reserved	Reserved			PETN2		AC
VSS	VSS	VSS	VSS	VSS	VSS		VccIO	VccIO	VSS		VccIO	VccIO	VSS	Reserved	Reserved		PETP2	PETP1	PETN1	AB
																	VSS	Reserved	VSS	AA
vccCore	vccCore	vccCore	vccCore	vccCore	VccIO			VccIO	VccIO	VSS	VccIO	VCCAPLLDMI2		VSS	CLKIN_GND0_N	CLKIN_GND0_P	Reserved		Reserved	Y

Figure 6-3. PCH Ballout (Top View - Lower Left)

W	VSS	USBN_1	VSS									vccsus3_3		vccsus3_3	vccsus3_3	VccASW	VccASW	VccASW	
V		USBP_2			USBP_9	USBN_9	VSS	USBRBIASn		HDA_SDO	HDA_BCLK	VSS		VSS	VSS	VccASW	VSS	VSS	
U	USBP_0	USBN_0	USBN_2		USBP_8	USBN_8	VSS	USBRBIASp		VSS	VccAUBG	V5REF_Sus		VccASW	VccSusHDA	VccASW	VccASW	VccASW	
T	VSS		VSS									VccASW		VccASW	vccsus3_3	VccASW	VccASW	VccASW	
R	DSWODVREN	RTCRST#	DPWROK	RTCX1		PCH_PWROK	VSS	CLKIN_DOT96N	CLKIN_DOT96P	VSS		VSS		VSS	vccsus3_3	VSS	VSS	vcc3_3	
P		SRTCRST#		RTCX2		INTRUDER#	VSS	TP23	TP24	VSS									
N	VSS	SUSWARN#/GPIO30	VSS									VccDSW3_3		DcpSus	vccSPI	VccIO	VccIO	vcc3_3	
M	SLP_SUS#	OC2#/GPIO41	OC1#/GPIO40		GPIO27	INTVRMEN	VSS	TP6		RSMRST#	VSS	DcpRTC		VSS	VccAUPLL	VccIO	VSS	VSS	
L	OC5#/GPIO9		VSS									vccRTC		DcpSusByp	DcpSST	vcc3_3	VccIO	VSS	
K	SML1DATA/GPIO75	OC7#/GPIO14	SML1CLK/GPIO58	OC3#/GPIO42		OC0#/GPIO59	GPIO31/MGPIO2		PWRBTN#	OC6#/GPIO10					SDATAOUT0/GPIO39	SPI_MOSI			
J		GPIO25		WAKE#		SST	SML1ALERT#/GPIO74		SMBALERT#/GPIO11	OC4#/GPIO43		DRAMPWROK	GPIO57		GPIO44	SATA0GP/GPIO21		SPI_MISO	SPI_CS1#
H	VSS	SMBDATA	ADR_COMPLETE			SML0ALERT#/GPIO60	SUSACK#					SLP_LAN#/GPIO29	GPIO56					SATA4GP/GPIO16	SATA5GP/GPIO49
G	RI#		SMBCLK	SML0DATA		VSS	VSS		VSS	VSS		VSS	VSS		VSS	VSS		VSS	VSS
F	LAN_PHY_PWR_CTRL/GPIO12	GPIO8	VSS	SML0CLK		GPIO24	APWROK		GPIO26	SLP_S3#		TP12	SCLOCK/GPIO22		GPIO34	SMI#/GPIO20		SATA5RXP	SATA4RXP
E		GPIO72	SLP_A#	GPIO61		PLTRST#	PCIRST#		SLP_S4#	GPIO15		JTAG_TDI	SDATAOUT1/GPIO48		GPIO45	BMBUSY#/GPIO0		SATA5RXN	SATA4RXN
D	VSS		GPIO46																
C	JTAG_TMS		PME#		SUSCLK/GPIO62	VSS	SYS_PWROK		INIT3_3V#	SYS_RESET#	VSS	SATA3GP/GPIO37		VSS	SATA2GP/GPIO36	VSS		SERIRQ	VSS
B		NC_2			SLP_S5#/GPIO63		GPIO73	GPIO47	NMI#/GPIO35		GPIO18	RCIN#	SATALED#	A20GATE		GPIO32	SPI_CLK	SATA5TXP	SATA4TXN
A			JTAG_TCK	VSS		JTAG_TDO	GPIO28		VSS	SLOAD/GPIO38	VSS	SPKR		VSS	SATA1GP/GPIO19	VSS		SATA5TXN	VSS
	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21

Figure 6-4. PCH Ballout (Top View - Lower Right)

vccCore	vccCore	vccCore	vccCore	vccCore	VccIO			VccIO	VccIO	VSS	VSS	VSS		VSS	TP2	TP1	VSS	Reserved	VSS	W
VSS	VSS	VSS	VSS	VSS	VSS													DMI_TXN_0		V
vccCore	vccCore	vccCore	vccCore	DcpSus	DcpSus		DMI_ZCOMP	DMI_RCOMP	VSS		DMIRBIAS	TP3	VSS	DMI_RXP_0	DMI_RXN_0		DMI_TXP_0	DMI_TXP_1	DMI_TXN_1	U
vccCore	vccCore	vccCore	vccCore	VccIO	vccsus3_3		VccIO	VccIO	VSS		VSS	Vcc3_3	VSS	DMI_RXN_1	DMI_RXP_1		VSS		VSS	T
VSS	VSS	VSS	VSS	VSS	VSS												DMI_TXP_2	DMI_TXN_2	DMI_TXN_3	R
								VccIO	TP4	VSS	TP5	VccAPLLEXP		VSS	DMI_RXP_2	DMI_RXN_2		DMI_TXP_3		P
VccIO	VSS	VccDFTERM	VccDFTERM	vccCore	vccCore			NC_10	NC_21	VSS	NC_6	NC_17		VSS	DMI_RXN_3	DMI_RXP_3	VSS	VSS	VSS	N
VccAPLLSATA	VccIO	VccDFTERM	VSS	VSS	VSS												VSS	CLKIN_DMI_P	CLKIN_DMI_N	M
VccVRM	VccIO	VccDFTERM	VccVRM	V_PROC_IO	VccDMI		Reserved	Reserved	VSS		NC_20	NC_9	VSS	NC_12	NC_16		VSS		VSS	L
	SPI_CS0#	SATAICOMPI					Reserved	Reserved					Reserved	Reserved			NC_24	NC_5	NC_14	K
	TP21	SATAICOMPO		SATA3COMPO	vccCore		Reserved	Reserved		Reserved	PROCPWRGD		THRMTRIPB	PM_SYNC		Reserved		NC_15		J
				TS_VSS_2	TS_VSS_4					Reserved	Reserved					PM_SYNC2	VSS	NC_19	VSS	H
	VSS	VSS		VSS	VSS		VSS	VSS		VSS	VSS		VSS	VSS		VSS	NC_18		NC_22	G
	SATA3RXP	SATA2RXP		SATA1RXP	SATA0RXP		Reserved	Reserved		Reserved	Reserved		Reserved	Reserved		Reserved	VSS	NC_8	VSS	F
	SATA3RXN	SATA2RXN		SATA1RXN	SATA0RXN		TS_VSS_1	TS_VSS_3		Reserved	Reserved		Reserved	Reserved		PECI	NC_11	NC_7		E
																	NC_13		VSS	D
SATA4TXP	VSS		SATA2TXP	VSS	SATA3COMPI		VSS	SATA1TXP	VSS	Reserved		VSS	DF_TVS	VSS	Reserved		NC_23		VSS	C
	SATA3TXP	SATA2TXN	CLKIN_SATA_N		TP22	SATA3RBIAS	SATA1TXN	SATA0TXP		TP19	VSS	Reserved		Reserved	Reserved			CHIP_DETECT#		B
SATA3TXN	VSS		CLKIN_SATA_P	VSS	TP20		VSS	SATA0TXN	VSS	VSS		VSS	Reserved	VSS		VSS	VSS			A
20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Table 6-1. PCH Ballout by Signal Name (Sheet 1 of 24)

PCH Ball Name	Ball #
A20GATE	B26
AD0	AW15
AD1	AA30
AD10	AC32
AD11	AW20
AD12	AM18
AD13	AP12
AD14	AL31
AD15	AM30
AD16	AM25
AD17	AU22
AD18	AG30
AD19	AG32
AD2	AN15
AD20	AN34
AD21	AK33
AD22	AL21
AD23	AK27
AD24	AM24
AD25	AV13
AD26	AD32
AD27	AL34
AD28	AR33
AD29	AG31
AD3	AR36
AD30	AL30
AD31	AA31
AD4	AP36
AD5	AV14
AD6	Y30
AD7	AU12
AD8	AU25
AD9	AW12
ADR_COMPLETE	H37
APWROK	F33
BMBUSY#/ GPIO0	E24
C/BE0#	AM31
C/BE1#	AL18
C/BE2#	AL33

Table 6-1. PCH Ballout by Signal Name (Sheet 2 of 24)

PCH Ball Name	Ball #
C/BE3#	AU20
CHIP_DETECT#	B2
CLKIN_DMI_N	M1
CLKIN_DMI_P	M2
CLKIN_DOT_96N	R32
CLKIN_DOT_96P	R31
CLKIN_GND0_N	Y5
CLKIN_GND0_P	Y4
CLKIN_PCI	AK22
CLKIN_SAS0_N	AU28
CLKIN_SAS0_P	AV27
CLKIN_SAS1_N	AV33
CLKIN_SAS1_P	AW33
CLKIN_SATA_N	B17
CLKIN_SATA_P	A17
CLKIN_SPCIE0_N	AN1
CLKIN_SPCIE0_P	AM2
DcpRTC	M28
DcpSST	L25
DcpSus	U15
DcpSus	U16
DcpSus	N26
DcpSusByp	L26
DEVSEL#	AJ32
DF_TVS	C7
DMI_IRCOMP	U12
DMI_RXN_0	U5
DMI_RXN_1	T6
DMI_RXN_2	P4
DMI_RXN_3	N5
DMI_RXP_0	U6
DMI_RXP_1	T5
DMI_RXP_2	P5
DMI_RXP_3	N4
DMI_TXN_0	V2
DMI_TXN_1	U1
DMI_TXN_2	R2
DMI_TXN_3	R1
DMI_TXP_0	U3

Table 6-1. PCH Ballout by Signal Name (Sheet 3 of 24)

PCH Ball Name	Ball #
DMI_TXP_1	U2
DMI_TXP_2	R3
DMI_TXP_3	P2
DMI_ZCOMP	U13
DMIRBIAS	U9
DPWROK	R37
DRAMPWROK	J28
DSWODVREN	R39
FRAME#	AF31
GNT0#	AN33
GNT1# / GPIO51 / GSXDOUT	AU15
GNT2# / GPIO53 / GSXDIN	AJ34
GNT3# / GPIO55	AF30
GPIO13	AV24
GPIO15	E30
GPIO18	B29
GPIO24	F34
GPIO25	J38
GPIO26	F31
GPIO27	M35
GPIO28	A33
GPIO31/MGPIO2	K33
GPIO32	B24
GPIO33	AT37
GPIO34	F25
GPIO44	J25
GPIO45	E25
GPIO46	D37
GPIO47	B32
GPIO56	H27
GPIO57	J27
GPIO64	AL16
GPIO65	AK16
GPIO66	AL15
GPIO67	AK15
GPIO72	E38
GPIO73	B33
GPIO8	F38

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Table 6-1. PCH Ballout by Signal Name (Sheet 4 of 24)

PCH Ball Name	Ball #
HDA_BCLK	V29
HDA_RST#	AW22
HDA_SDIN0	AH37
HDA_SDIN1	AG38
HDA_SDIN2	AH39
HDA_SDIN3	AH38
HDA_SDO	V30
HDA_SYNC	AV17
INIT3_3V#	C31
INTRUDER#	P34
INTVRMEN	M34
IRDY#	AP18
JTAG_TCK	A37
JTAG_TDI	E28
JTAG_TDO	A34
JTAG_TMS	C39
LAD0	AV15
LAD1	AV23
LAD2	AL36
LAD3	AU17
LAN_PHY_PWR_CTRL / GPIO12	F39
LDRQ0#	AP19
LDRQ1# / GPIO23	AR37
LFRAME#	AF36
NC_1	AP13
NC_2	B38
NC_3	AV38
NC_4	AV2
NMI#/GPIO35	B31
NC_5	K2
NC_6	N9
NC_7	E2
NC_8	F2
NC_9	L8
NC_10	N12
NC_11	E3
NC_12	L6
NC_13	D3

Table 6-1. PCH Ballout by Signal Name (Sheet 5 of 24)

PCH Ball Name	Ball #
NC_14	K1
NC_15	J2
NC_16	L5
NC_17	N8
NC_18	G3
NC_19	H2
NC_20	L9
NC_21	N11
NC_22	G1
NC_23	C3
NC_24	K3
OC0# / GPIO59	K34
OC1# / GPIO40	M37
OC2# / GPIO41	M38
OC3# / GPIO42	K36
OC4# / GPIO43	J30
OC5# / GPIO9	L39
OC6# / GPIO10	K30
OC7# / GPIO14	K38
PAR	AK28
PCH_PWROK	R34
PCIRST#	E33
PECI	E4
PEG0_RBIASN	AL5
PEG0_RBIASP	AL4
PEG0_RN0	AU3
PEG0_RN1	AV5
PEG0_RN2	AU7
PEG0_RN3	AV8
PEG0_RP0	AT3
PEG0_RP1	AU5
PEG0_RP2	AV6
PEG0_RP3	AW7
PEG0_TN0	AP3
PEG0_TN1	AR4
PEG0_TN2	AP6
PEG0_TN3	AR7
PEG0_TP0	AN3
PEG0_TP1	AN4

Table 6-1. PCH Ballout by Signal Name (Sheet 6 of 24)

PCH Ball Name	Ball #
PEG0_TP2	AR6
PEG0_TP3	AP7
PERn1	AE4
PERn2	AF5
PERn3	AH6
PERn4	AJ6
PERn5	AE8
PERn6	AF8
PERn7	AH8
PERn8	AJ9
PERp1	AE5
PERp2	AF4
PERp3	AH5
PERp4	AJ5
PERp5	AE9
PERp6	AF9
PERp7	AH9
PERp8	AJ8
PERR#	AM19
PETn1	AB1
PETn2	AC2
PETn3	AE1
PETn4	AF2
PETn5	AH1
PETn6	AH2
PETn7	AK1
PETn8	AL2
PETp1	AB2
PETp2	AB3
PETp3	AD2
PETp4	AE3
PETp5	AG2
PETp6	AH3
PETp7	AJ2
PETp8	AK3
PIRQA#	AR19
PIRQB#	AJ30
PIRQC#	AV18
PIRQD#	AR18

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Table 6-1. PCH Ballout by Signal Name (Sheet 7 of 24)

PCH Ball Name	Ball #
PIRQE# / GPIO2	AF32
PIRQF# / GPIO3	AL22
PIRQG# / GPIO4	AA32
PIRQH# / GPIO5	AR16
PLOCK#	AR15
PLTRST#	E34
PM_SYNC	J6
PM_SYNC2	H4
PME#	C37
PROCPWRGD	J9
PWM0	AW17
PWM1	AV22
PWM2	AR13
PWM3	AG36
PWRBTN#	K31
RCIN#	B28
REFCLK14IN	AV12
REQ0#	AL27
REQ1# / GPIO50 / GSXCLK	AR34
REQ2# / GPIO52 / GSXSLOAD	AK34
REQ3# / GPIO54 / GSXSRESET#	AK21
Reserved	A7
Reserved	AA2
Reserved	AB5
Reserved	AB6
Reserved	AC5
Reserved	AC6
Reserved	B5
Reserved	B6
Reserved	B8
Reserved	C10
Reserved	C5
Reserved	E10
Reserved	E6
Reserved	E7
Reserved	E9
Reserved	F10

Table 6-1. PCH Ballout by Signal Name (Sheet 8 of 24)

PCH Ball Name	Ball #
Reserved	F12
Reserved	F13
Reserved	F4
Reserved	F6
Reserved	F7
Reserved	F9
Reserved	H10
Reserved	H9
Reserved	J10
Reserved	J12
Reserved	J13
Reserved	J4
Reserved	K12
Reserved	K13
Reserved	K6
Reserved	K7
Reserved	L12
Reserved	L13
Reserved	W2
Reserved	Y1
Reserved	Y3
RI#	G39
RSMRST#	M30
RTCRST#	R38
RTCX1	R36
RTCX2	P36
SAS0RXN	AR21
SAS1RXN	AR22
SAS2RXN	AP24
SAS3RXN	AP25
SAS4RXN	AN27
SAS5RXN	AN28
SAS6RXN	AP30
SAS7RXN	AP31
SAS0RXP	AN21
SAS1RXP	AN22
SAS2RXP	AR24
SAS3RXP	AR25
SAS4RXP	AR27

Table 6-1. PCH Ballout by Signal Name (Sheet 9 of 24)

PCH Ball Name	Ball #
SAS5RXP	AR28
SAS6RXP	AR30
SAS7RXP	AR31
SAS0TXN	AW28
SAS1TXN	AV29
SAS2TXN	AW30
SAS3TXN	AV32
SAS4TXN	AN38
SAS5TXN	AN39
SAS6TXN	AL38
SAS7TXN	AK39
SAS0TXP	AV28
SAS1TXP	AU30
SAS2TXP	AV31
SAS3TXP	AU33
SAS4TXP	AN37
SAS5TXP	AM38
SAS6TXP	AK37
SAS7TXP	AJ38
SAS_CLOCK1	AL8
SAS_LOAD1	AN10
SAS_DATAIN1	AL9
SAS_DATAOUT1	AV9
SAS_CLOCK2	AW10
SAS_LOAD2	AV10
SAS_DATAIN2	AU10
SAS_DATAOUT2	AR10
SAS_LED#	AR9
SAS_RBIASN0	AW25
SAS_RBIASN1	AL24
SAS_RBIASP0	AV26
SAS_RBIASP1	AL25
SASSMBCLK0	AJ12
SASSMBCLK1	AH13
SASSMBCLK2	AL13
SASSMBDATA0	AL11
SASSMBDATA1	AH12
SASSMBDATA2	AM13
SATA0RXN	E15

Table 6-1. PCH Ballout by Signal Name (Sheet 10 of 24)

PCH Ball Name	Ball #
SATA1RXN	E16
SATA2RXN	E18
SATA3RXN	E19
SATA4RXN	E21
SATA5RXN	E22
SATA0RXP	F15
SATA1RXP	F16
SATA2RXP	F18
SATA3RXP	F19
SATA4RXP	F21
SATA5RXP	F22
SATA0TXN	A12
SATA1TXN	B13
SATA2TXN	B18
SATA3TXN	A20
SATA4TXN	B21
SATA5TXN	A22
SATA0TXP	B12
SATA1TXP	C12
SATA2TXP	C17
SATA3TXP	B19
SATA4TXP	C20
SATA5TXP	B22
SATA0GP / GPIO21	J24
SATA1GP / GPIO19	A25
SATA2GP / GPIO36	C25
SATA3GP / GPIO37	C28
SATA4GP / GPIO16	H22
SATA5GP / GPIO49 / TEMP_ALERT#	H21
SATAICOMPI	K18
SATAICOMPO	J18
SATALED#	B27
SCLOCK / GPIO22	F27
SDATAOUT0 / GPIO39	K25
SDATAOUT1 / GPIO48	E27
SATA3RBIAS	B14
SATA3COMPI	C15

Table 6-1. PCH Ballout by Signal Name (Sheet 11 of 24)

PCH Ball Name	Ball #
SATA3COMPO	J16
SERIRQ	C22
SERR#	AN16
SLOAD / GPIO38	A30
SLP_A#	E37
SLP_LAN# / GPIO29	H28
SLP_S3#	F30
SLP_S4#	E31
SLP_S5# / GPIO63	B35
SLP_SUS#	M39
SMBALERT# / GPIO11	J31
SMBCLK	G37
SMBDATA	H38
SMI# / GPIO20	F24
SML0ALERT# / GPIO60	H34
SML0CLK	F36
SML0DATA	G36
SML1ALERT# / GPIO74	J33
SML1CLK / GPIO58	K37
SML1DATA / GPIO75	K39
SPI_CLK	B23
SPI_CS0#	K19
SPI_CS1#	J21
SPI_MISO	J22
SPI_MOSI	K24
SPKR	A28
SRTCRST#	P38
SST	J34
STOP#	AV19
SUSACK#	H33
SUSWARN# / GPIO30	N38
GPIO61	E36
SUSCLK / GPIO62	C35
SYS_PWROK	C33
SYS_RESET#	C30

Table 6-1. PCH Ballout by Signal Name (Sheet 12 of 24)

PCH Ball Name	Ball #
TACH0 / GPIO17	AV21
TACH1 / GPIO1	AL19
TACH2 / GPIO6	Y31
TACH3 / GPIO7	AJ35
TACH4 / GPIO68	AG34
TACH5 / GPIO69	Y32
TACH6 / GPIO70	AF34
TACH7 / GPIO71	AM36
THRMTRIP#	J7
TP1	W4
TP10	AU1
TP11	AL28
TP12	F28
TP13	AU37
TP14	AU39
TP15	AV35
TP16	AT39
TP17	AU35
TP18	AR38
TP19	B10
TP2	W5
TP20	A15
TP21	J19
TP22	B15
TP23	P32
TP24	P31
TP3	U8
TP4	P11
TP5	P9
TP6	M32
TP7	AN2
TP8	AT1
TP9	AP1
TRDY#	AR12
TS_VSS1	E13
TS_VSS2	H16
TS_VSS3	E12
TS_VSS4	H15
USBP0N	U38

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Table 6-1. PCH Ballout by Signal Name (Sheet 13 of 24)

PCH Ball Name	Ball #
USBP0P	U39
USBP10N	AD34
USBP10P	AD35
USBP11N	AC34
USBP11P	AC35
USBP12N	AA34
USBP12P	AA36
USBP13N	Y34
USBP13P	Y36
USBP1N	W38
USBP1P	Y39
USBP2N	U37
USBP2P	V38
USBP3N	Y37
USBP3P	AA38
USBP4N	AB38
USBP4P	AB39
USBP5N	AB37
USBP5P	AC38
USBP6N	AD38
USBP6P	AE39
USBP7N	AE37
USBP7P	AF38
USBP8N	U34
USBP8P	U35
USBP9N	V34
USBP9P	V35
USBRBIAS	U32
USBRBIAS#	V32
V_PROC_IO	L16
V5REF	AD29
V5REF_Sus	U28
Vcc3_3	R22
Vcc3_3	N22
Vcc3_3	AJ18
Vcc3_3	AH18
Vcc3_3	AC30
Vcc3_3	AC29
Vcc3_3	T8

Table 6-1. PCH Ballout by Signal Name (Sheet 14 of 24)

PCH Ball Name	Ball #
Vcc3_3	L24
VccCore	AD20
VccCore	AD19
VccCore	AD18
VccCore	AD17
VccCore	AD16
VccCore	AC20
VccCore	AC19
VccCore	AC18
VccCore	AC17
VccCore	AC16
VccCore	Y20
VccCore	Y19
VccCore	Y18
VccCore	Y17
VccCore	Y16
VccCore	W20
VccCore	W19
VccCore	W18
VccCore	W17
VccCore	W16
VccCore	U20
VccCore	U19
VccCore	U18
VccCore	U17
VccCore	T20
VccCore	T19
VccCore	T18
VccCore	T17
VccCore	N16
VccCore	N15
VccCore	J15
VccDFTERM	N18
VccDFTERM	N17
VccDFTERM	M18
VccDFTERM	L18
VccDMI	L15
VccDSW3_3	N28
VccIO	AE11

Table 6-1. PCH Ballout by Signal Name (Sheet 15 of 24)

PCH Ball Name	Ball #
VccIO	AC13
VccIO	AC12
VccIO	AC9
VccIO	AC8
VccIO	AB13
VccIO	AB12
VccIO	AB9
VccIO	AB8
VccIO	Y15
VccIO	Y12
VccIO	Y11
VccIO	Y9
VccIO	W15
VccIO	W12
VccIO	W11
VccIO	T13
VccIO	T12
VccIO	T16
VccIO	P12
VccIO	N24
VccIO	N23
VccIO	M24
VccIO	L23
VccIO	Y28
VccIO	Y26
VccIO	Y25
VccIO	N20
VccIO	M19
VccIO	L19
VccAUPLL	M25
VccRBIAS_SAS0	AF20
VccRBIAS_SAS1	AJ23
VccRBIAS_SAS1	AH23
VccIO	AJ28
VccIO	AJ26
VccIO	AJ25
VccIO	AH28
VccIO	AH26
VccIO	AH25

Table 6-1. PCH Ballout by Signal Name (Sheet 16 of 24)

PCH Ball Name	Ball #
VccIO	AF28
VccIO	AF26
VccIO	AF25
VccIO	AF24
VccIO	AE24
VccSCUS	AC22
VccSCUS	AC23
VccSCUS	AC24
VccSCUS	AD22
VccSCUS	AD23
VccSCUS	AD24
VccXUS	AR2
VccXUS	AN9
VccRBIAS_PU	AJ13
VccXUS	AJ16
VccXUS	AJ15
VccXUS	AH16
VccXUS	AH15
VccXUS	AF17
VccXUS	AF16
VccXUS	AF12
VccXUS	AF11
VccXUS	AC15
VccXUS	AD15
VccXUS	AE12
VccASW	AD28
VccASW	AD26
VccASW	AD25
VccASW	AC28
VccASW	AC26
VccASW	AC25
VccASW	Y24
VccASW	Y23
VccASW	Y22
VccASW	W24
VccASW	W23
VccASW	W22
VccASW	V24
VccASW	U24

Table 6-1. PCH Ballout by Signal Name (Sheet 17 of 24)

PCH Ball Name	Ball #
VccASW	U23
VccASW	U22
VccASW	T24
VccASW	T23
VccASW	T22
VccASW	U26
VccASW	T28
VccASW	T26
VccAPLLDMI2	Y8
VccAPLLEXP	P8
VccAPLLSATA	M20
VccPLLSAS0	AJ20
VccPLLSAS0	AH20
VccPLLSAS1	AF23
VccPLLEXPU	AF15
VccRTC	L28
VccSAS1_5	AJ22
VccSAS1_5	AH22
VccSAS1_5	AF22
VccSPI	N25
VccSus3_3	T25
VccSus3_3	R25
VccSus3_3	W28
VccSus3_3	W26
VccSus3_3	W25
VccAUBG	U29
VccSus3_3	T15
VccSusHDA	U25
VccVRM	L17
VccVRM	L20
Vss (0)	AW37
Vss	AW36
Vss	AW34
Vss	AW31
Vss	AW29
Vss	AW26
Vss	AW24
Vss	AW21
Vss	AW19

Table 6-1. PCH Ballout by Signal Name (Sheet 18 of 24)

PCH Ball Name	Ball #
Vss	AW16
Vss (10)	AW13
Vss	AW11
Vss	AW8
Vss	AW6
Vss	AW4
Vss	AW3
Vss	AU34
Vss	AU31
Vss	AU29
Vss	AU26
Vss (20)	AU24
Vss	AU21
Vss	AU19
Vss	AU16
Vss	AU13
Vss	AU11
Vss	AU8
Vss	AU6
Vss	AR3
Vss	AP39
Vss (30)	AP37
Vss	AN36
Vss	AN31
Vss	AN30
Vss	AN25
Vss	AN24
Vss	AN19
Vss	AN18
Vss	AN13
Vss	AN12
Vss (40)	AN7
Vss	AN6
Vss	AM34
Vss	AM33
Vss	AM28
Vss	AM27
Vss	AM22
Vss	AM21

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Table 6-1. PCH Ballout by Signal Name (Sheet 19 of 24)

PCH Ball Name	Ball #
Vss	AM16
Vss	AM15
Vss (50)	AM10
Vss	AM9
Vss	AM4
Vss	AL39
Vss	AL37
Vss	AL10
Vss	AL6
Vss	AL3
Vss	AL1
Vss	AJ39
Vss (60)	AJ37
Vss	AJ33
Vss	AJ29
Vss	AJ24
Vss	AJ19
Vss	AJ17
Vss	AJ11
Vss	AJ7
Vss	AJ3
Vss	AJ1
Vss (70)	AH24
Vss	AH19
Vss	AH17
Vss	AH11
Vss	AH7
Vss	AG33
Vss	AF39
Vss	AF37
Vss	AF33
Vss	AF19
Vss (80)	AF18
Vss	AF10
Vss	AF6
Vss	AF3
Vss	AF1
Vss	AE28
Vss	AE26

Table 6-1. PCH Ballout by Signal Name (Sheet 20 of 24)

PCH Ball Name	Ball #
Vss	AE25
Vss	AE23
Vss	AE22
Vss (90)	AE20
Vss	AE19
Vss	AE18
Vss	AE17
Vss	AE16
Vss	AE15
Vss	AE10
Vss	AE6
Vss	AD39
Vss	AD37
Vss (100)	AD33
Vss	AD30
Vss	AD3
Vss	AD1
Vss	AC33
Vss	AC11
Vss	AC7
Vss	AB28
Vss	AB26
Vss	AB25
Vss (110)	AB24
Vss	AB23
Vss	AB22
Vss	AB20
Vss	AB19
Vss	AB18
Vss	AB17
Vss	AB16
Vss	AB15
Vss	AB11
Vss (120)	AB7
Vss	AA39
Vss	AA37
Vss	AA33
Vss	AA3
Vss	AA1

Table 6-1. PCH Ballout by Signal Name (Sheet 21 of 24)

PCH Ball Name	Ball #
Vss	Y33
Vss	Y10
Vss	Y6
Vss	W39
Vss (130)	W37
Vss	W10
Vss	W6
Vss	W3
Vss	W1
Vss	V33
Vss	V28
Vss	V26
Vss	V25
Vss	V23
Vss (140)	V22
Vss	V20
Vss	V19
Vss	V18
Vss	V17
Vss	V16
Vss	V15
Vss	U33
Vss	U11
Vss	U7
Vss (150)	T39
Vss	T37
Vss	T11
Vss	T7
Vss	T3
Vss	T1
Vss	R33
Vss	R30
Vss	R28
Vss	R26
Vss (160)	R24
Vss	R23
Vss	R20
Vss	R19
Vss	R18

Table 6-1. PCH Ballout by Signal Name (Sheet 22 of 24)

PCH Ball Name	Ball #
Vss	R17
Vss	R16
Vss	R15
Vss	P33
Vss	P30
Vss (170)	P10
Vss	P6
Vss	N39
Vss	N37
Vss	N19
Vss	N10
Vss	N6
Vss	N3
Vss	N1
Vss	M33
Vss (180)	M29
Vss	M26
Vss	M22
Vss	M17
Vss	M16
Vss	M15
Vss	L37
Vss	L22
Vss	L11
Vss	L7
Vss (190)	L3
Vss	L1
Vss	H39
Vss	H3
Vss	H1
Vss	G34
Vss	G33
Vss	G31
Vss	G30
Vss	G28
Vss (200)	G27
Vss	G25
Vss	G24
Vss	G22

Table 6-1. PCH Ballout by Signal Name (Sheet 23 of 24)

PCH Ball Name	Ball #
Vss	G21
Vss	G19
Vss	G18
Vss	G16
Vss	G15
Vss	G13
Vss (210)	G12
Vss	G10
Vss	G9
Vss	G7
Vss	G6
Vss	G4
Vss	F37
Vss	F3
Vss	F1
Vss	D39
Vss (220)	D1
Vss	C34
Vss	C29
Vss	C26
Vss	C24
Vss	C21
Vss	C19
Vss	C16
Vss	C13
Vss	C11
Vss (230)	C8
Vss	C1
Vss	A36
Vss	A31
Vss	A29
Vss	A26
Vss	A24
Vss	A21
Vss	A19
Vss (240)	A16
Vss	A13
Vss	A11
Vss	A8

Table 6-1. PCH Ballout by Signal Name (Sheet 24 of 24)

PCH Ball Name	Ball #
Vss	A6
Vss	A4
Vss	A3
Vss	T9
Vss	U30
Vss	M23
Vss (250)	W9
Vss	W8
Vss	N2
Vss	M3
Vss	B9
Vss	A10
WAKE#	J36

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7 Package Information

Refer to the *Intel® X79 Express Chipset Thermal and Mechanical Design Guidelines* document for PCH package information.

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8 Electrical Characteristics

This chapter contains the DC and AC characteristics for the PCH. AC timing diagrams are included.

8.1 Thermal Specifications

Refer to the *Intel® X79 Express Chipset Thermal and Mechanical Design Guidelines* document for PCH package information.

8.2 Absolute Maximum Ratings

Table 8-1. PCH Absolute Maximum Ratings

Parameter	Maximum Limits
Voltage on any 5 V Tolerant Pin with respect to Ground (V5REF = 5 V)	-0.5 to V5REF + 0.5 V
Voltage on any 3.3 V Pin with respect to Ground	-0.5 to Vcc3_3 + 0.4 V
Voltage on any 1.8 V Tolerant Pin with respect to Ground	-0.5 to VccVRM + 0.5 V
Voltage on any 1.5 V Pin with respect to Ground	-0.5 to VccVRM + 0.5 V
Voltage on any 1.1 V Tolerant Pin with respect to Ground	-0.5 to VccIO + 0.5 V
1.1 V Supply Voltage with respect to VSS	-0.5 to 1.3 V
1.8 V Supply Voltage with respect to VSS	-0.5 to 1.98 V
3.3 V Supply Voltage with respect to VSS	-0.5 to 3.7 V
5.0 V Supply Voltage with respect to VSS	-0.5 to 5.5 V
V_PROC_IO Supply Voltage with respect to VSS	-0.5 to 1.3 V
1.1 V Supply Voltage for the analog PLL with respect to VSS	-0.5 to 1.3 V
1.5 V Supply Voltage for the analog PLL with respect to VSS	-0.5 to 1.65 V
1.8 V Supply Voltage for the analog PLL with respect to VSS	-0.5 to 1.98 V

Table 8-1 specifies absolute maximum and minimum ratings. At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits (but within the absolute maximum and minimum ratings) the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time, it will either not function or its reliability will be severely degraded when returned to conditions within the functional operating condition limits.

Although the PCH contains protective circuitry to resist damage from Electrostatic Discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

8.3 PCH Power Supply Range

Table 8-2. PCH Power Supply Range

Power Supply	Minimum	Nominal	Maximum
1.0 V	0.95 V	1.00 V	1.05 V
1.05 V	0.998 V	1.05 V	1.10 V
1.1 V	1.05 V	1.10 V	1.16 V
1.5 V	1.43 V	1.50 V	1.58 V
1.8 V	1.71 V	1.80 V	1.89 V
3.3 V	3.14 V	3.30 V	3.47 V
5 V	4.75 V	5.00 V	5.25 V

8.4 General DC Characteristics

I_{CC} values in Table 8-3 specifications have been validated using post-silicon measurements. These values are provided primarily for sizing platform VR solutions.

Table 8-3. Power Supply I_{CC} Specifications by Domain

Voltage Rail	Voltage (V)	S0 Iccmax Current[3] (A)	TDC[4] (A)	TDC Typical[5] (A)	Sx Iccmax Current[3] (A)	Sx Idle Current[6] (A)
V5REF	5	1 (mA)	1 (mA)	1 (mA)	—	—
V5REF_Sus	5	1 (mA)	1 (mA)	1 (mA)	< 1 (mA)	< 1 (mA)
Vcc3_3	3.3	0.17	0.02	0.02	—	—
VccSus3_3	3.3	0.08	0.04	0.03	0.15	0.05
Vcc[1]	1.1	8.0	5.6	4.1	—	—
VccASW	1.1	1.5	1.0	0.5	0.8	0.4
VccDSW	3.3	0.002	< 1 (mA)	< 1 (mA)	< 1 (mA)	< 1 (mA)
VccSAS	1.5	0.15	0.13	0.13	—	—
VccVRM[2]	1.5	0.2	0.12	0.11	—	—
V_PROC_IO	1.0 –1.1	1(mA)	1(mA)	1(mA)	—	—
VccDMI	1.0–1.1	0.057	0.057	0.45	—	—

Notes:
1. Vcc includes VccIO, VccCORE, VccDMI, and so forth, that are in the 1.1 V core well and typically supplied by a common VR source.
2. VccVRM can optionally be used in 1.8 V mode.
3. Iccmax currents define the operational maximums which must be provided by platform power delivery VR and traces (peak activity on worst-case 3-sigma manufacturing units).
4. TDC currents represent steady-state consumption, by supply rail, for Full Feature TDP specifications. (Max) defines platform thermal solution necessary to support 3-sigma manufacturing variance,
5. TDC (Typ) is representative consumption of volume units at Full-Feature TDP configuration.
6. Sx Idle current is representative consumption of volume units at full idle (including Intel ME).

Table 8-4. DC Characteristic Input Signal Association (Sheet 1 of 2)

Symbol	Associated Signals
VIH1/VIL1 (5 V Tolerant)	**PCI Signals:** AD[31:0], C/BE[3:0]#, DEVSEL#, FRAME#, IRDY#, PAR, PERR#, PLOCK#, REQ[3:0]#, SERR#, STOP#, TRDY# **Interrupt Signals:** PIRQ[D:A]#, PIRQ[H:E]# **GPIO Signals:** GPIO[54, 52, 50, 5:2] **GSX Signals:**GSXDIN
VIMIN2-Gen3i/ VIMAX2-Gen3i	**SATA Signals:** SATA[1:0]RX[P,N] (6.0 Gb/s internal SATA)
VIH3/VIL3	**Clock Signals:** REFCLK14IN **Power Management Signals:** PWRBTN#, RI#, SYS_RESET#, WAKE#, SUSACK#. **GPIO Signals:** GPIO[71:68, 63:61, 57, 48, 39, 38, 34, 32, 31, 30, 29, 24, 22, 17, 7, 6, 1] **Thermal/Fan Control Signals**: TACH[7:0]
VIH4/VIL4	**Clock Signals:** CLKIN_PCI **Processor Signals:**A20GATE **PCI Signals:** PME# **Interrupt Signals:** SERIRQ **SATA Signals:** SATA[5:0]GP **SPI Signals:** SPI_MISO **Strap Signals:** SPKR, GNT[3:1]#, (Strap purposes only) **LPC Signals:** LAD[3:0], LDRQ0#, LDRQ1#, **GPIO Signals:** GPIO[73, 72, 67:64, 59, 56, 55, 53, 51, 49, 47:40, 37, 36, 35, 33, 28, 27, 26, 25, 23, 21, 20, 19, 18, 16, 15, 14, 12, 10, 9, 8, 0] **USB Signals:** OC[7:0]#
VIH5/VIL5	**SMBus Signals:** SMBCLK, SMBDATA, SMBALERT# **System Management Signals:** SML[1:0]CLK(1), SML[1:0]DATA(1) **GPIO Signals:** GPIO[75, 74, 60, 58, 11]
VIH6/VIL6	**JTAG Signals:** JTAG_TDI, JTAG_TMS, JTAG_TCK
VIH7/VIL7	**Processor Signals:** THRMTRIP#
VIMIN8Gen1/ VIMAX8Gen1, VIMIN8Gen2/ VIMAX8Gen2,	**PCI Express Data RX Signals:** PER[p,n][8:1] (2.5 GT/s and 5.0 GT/s)
VIH9/VIL9	**Real Time Clock Signals:** RTCX1
VIMIN10 -Gen1i/ VIMAX10-Gen1i	**SATA Signals:** SATA[5:0]RX[P,N] (1.5 Gb/s internal SATA)
VIMIN10 -Gen1m/ VIMAX10-Gen1m	**SATA Signals:** SATA[5:0]RX[P,N] (1.5 Gb/s external SATA)
VIMIN10 -Gen2i/ VIMAX10-Gen2i	**SATA Signals:** SATA[5:0]RX[P,N] (3.0 Gb/s internal SATA)
VIMIN10 -Gen2m/ VIMAX10-Gen2m	**SATA Signals:** SATA[5:0]RX[P,N] (3.0 Gb/s external SATA)
VIH11/VIL11	**Intel® High Definition Audio Signals:** HDA_SDIN[3:0] (3.3V Mode) **Strap Signals:** HDA_SDOUT, HDA_SYNC (Strap purposes only) **GPIO Signals**: GPIO13 ***Note:*** See VIL_HDA/VIH_HDA for High Definition Audio Low Voltage Mode
VIH12 (Absolute Maximum) / VIL12 (Absolute Minimum) / Vclk_in_cross(abs)	**Clock Signals:** CLKIN_DMI_[P,N], CLKIN_DOT96[P,N], CLKIN_SATA_[P,N]
VIH13/VIL13	**Miscellaneous Signals:** RTCRST#

Table 8-4. DC Characteristic Input Signal Association (Sheet 2 of 2)

Symbol	Associated Signals
VIH14/VIL14	**Power Management Signals:** PCH_PWROK, RSMRST#, DPWROK **System Management Signals:** INTRUDER# **Miscellaneous Signals:** INTVRMEN, SRTCRST#
VIH15/VIL15	**Processor Interface:** RCIN# **Power management Signals:** SYS_PWROK, APWROK
VDI / VCM / VSE (5V Tolerant)	**USB Signals:** USBP[13:0][P,N] (Low-speed and Full-speed)
V_{HSSQ} / V_{HSDSC} / V_{HSCM} (5 V Tolerant)	**USB Signals:** USBP[13:0][P,N] (in High-speed Mode)
VIH_HDA / VIL_HDA	**Intel High Definition Audio Signals:** HDA_SDIN[3:0] **Strap Signals:** HDA_SDOUT, HDA_SYNC (Strap purposes only) ***Note:*** Only applies when running in Low Voltage Mode (1.5 V)
VIH_SST/VIL_SST	**Thermal Reporting Signals:** SST
VIH_PECI/VIL_PECI	**Thermal Reporting Signals:** PECI
VIH_SASCLK/ VIL_SASCLK Vcm_sas	**SAS Clocks:**CLKIN_SAS0[P,N], CLKIN_SAS1[P,N]

Notes:
1. V_{DI} = | USBPx[P] – USBPx[N]
2. Includes VDI range
3. Applies to Low-Speed/High-Speed USB
4. PCI Express mVdiff p-p = 2*|PETp[x] – PETn[x]|
5. SATA Vdiff, RX (VIMAX10/MIN10) is measured at the SATA connector on the receiver side (generally, the motherboard connector), where SATA mVdiff p-p = 2*|SATA[x]RXP – SATA[x]RXN|
6. VccRTC is the voltage applied to the VccRTC well of the PCH. When the system is in a G3 state, this is generally supplied by the coin cell battery, but for S5 and greater, this is generally VccSus3_3.
7. This is an AC Characteristic that represents transient values for these signals.
8. Applies to Hogh-Speed USB 2.0.

Table 8-5. DC Input Characteristics (Sheet 1 of 3)

Symbol	Parameter	Min	Max	Unit	Notes
VIL1	Input Low Voltage	–0.5	0.3 x 3.3 V	V	9
VIH1	Input High Voltage	0.5 x 3.3 V	V5REF + 0.5	V	9
VIMIN2-Gen3i	Minimum Input Voltage - 6.0 Gb/s SATA	240	—	mVdiffp-p	5
VIMAX2-Gen3i	Maximum Input Voltage - 6.0 Gb/s SATA	—	1000	mVdiffp-p	5
VIL3	Input Low Voltage	–0.5	0.8	V	
VIH3	Input High Voltage	2.0	3.3 V + 0.5	V	9
VIL4	Input Low Voltage	–0.5	0.3 x 3.3 V	V	9
VIH4	Input High Voltage	0.5 x 3.3 V)	3.3 V + 0.5	V	9
VIL5	Input Low Voltage	–0.5	0.8	V	
VIH5	Input High Voltage	2.1	3.3 V + 0.5	V	9
VIL6	Input Low Voltage	-0.5	0.35	V	10
VIH6	Input High Voltage	0.75	1.1 V + 0.5	V	10
VIL7	Input Low Voltage	0	0.51 x V_PROC_IO	V	

Table 8-5. DC Input Characteristics (Sheet 2 of 3)

Symbol	Parameter	Min	Max	Unit	Notes
VIH7	Input High Voltage	0.81 x V_PROC_IO	V_PROC_IO	V	
VIMIN8Gen1	Minimum Input Voltage	175	—	mVdiffp-p	4
VIMAX8Gen1	Maximum Input Voltage	—	1200	mVdiffp-p	4
VIMIN8Gen2	Minimum Input Voltage	100	—	mVdiffp-p	4
VIMAX8Gen2	Maximum Input Voltage	—	1200	mVdiffp-p	4
VIL9	Input Low Voltage	–0.5	0.10	V	
VIH9	Input High Voltage	0.50	1.2	V	
VIMIN10-Gen1i	Minimum Input Voltage - 1.5 Gb/s internal SATA	325	—	mVdiffp-p	5
VIMAX10-Gen1i	Maximum Input Voltage - 1.5 Gb/s internal SATA	—	600	mVdiffp-p	5
VIMIN10-Gen1m	Minimum Input Voltage - 1.5 Gb/s eSATA	240	—	mVdiffp-p	5
VIMAX10-Gen1m	Maximum Input Voltage - 1.5 Gb/s eSATA	—	600	mVdiffp-p	5
VIMIN10-Gen2i	Minimum Input Voltage - 3.0 Gb/s internal SATA	275	—	mVdiffp-p	5
VIMAX10-Gen2i	Maximum Input Voltage - 3.0 Gb/s internal SATA	—	750	mVdiffp-p	5
VIMIN10-Gen2m	Minimum Input Voltage - 3.0 Gb/s eSATA	240	—	mVdiffp-p	5
VIMAX10-Gen2m	Maximum Input Voltage - 3.0 Gb/s eSATA	—	750	mVdiffp-p	5
VIL11	Input Low Voltage	−0.5	0.35 x 3.3 V	V	9
VIH11	Input High Voltage	0.65 x 3.3 V	3.3 + 0.5 V	V	9
VIL12 (Absolute Minimum)	Input Low Voltage	-0.3	—	V	
VIH12 (Absolute Maximum)	Input High Voltage	—	1.150	V	
VIL13	Input Low Voltage	−0.5	0.78	V	
VIH13	Input High Voltage	2.3	VccRTC + 0.5	V	6
VIL14	Input Low Voltage	−0.5	0.78	V	
VIH14	Input High Voltage	2.0	VccRTC + 0.5	V	6
VIL15	Input Low Voltage	−0.5	0.8	V	9
VIH15	Input High Voltage	2.1	3.3 V + 0.5	V	9
VIMIN18	Minimum Input Voltage - PCIe 8GT/s	15	—	mVdiffp-p	
VIMAX18	Maximum Input Voltage - PCIe 8GT/s	—	1200	mVdiffp-p	
Vclk_in_cross(abs)	Absolute Crossing Point	0.250	0.550	V	
Vcross-delta	Vcross variation	—	140	mV	
VDI	Differential Input Sensitivity	0.2	—	V	1,3

Table 8-5. DC Input Characteristics (Sheet 3 of 3)

Symbol	Parameter	Min	Max	Unit	Notes
VCM	Differential Common Mode Range	0.8	2.5	V	2,3
VSE	Single-Ended Receiver Threshold	0.8	2.0	V	3
VHSSQ	HS Squelch Detection Threshold	100	150	mV	8
VHSDSC	HS Disconnect Detection Threshold	525	625	mV	8
VHSCM	HS Data Signaling Common Mode Voltage Range	–50	500	mV	8
VIL_HDA	Input Low Voltage	0	0.4 x Vcc_HDA	V	
VIH_HDA	Input High Voltage	0.6 x Vcc_HDA)	1.5	V	
VIL_SST	Input Low Voltage	-0.3	0.4	V	
VIH_SST	Input High Voltage	1.1	1.5	V	
VIL_PECI	Input Low Voltage	-0.15	0.275 x V_PROC_IO	V	
VIH_PECI	Input High Voltage	0.725 x V_PROC_IO	V_PROC_IO + 0.15	V	
VIH_SASCLK	Differential Input High Voltage - SAS Clocks	150	—	mV	
VIH_SASCLK	Differential Input Low Voltage - SAS Clocks	—	-150	mV	
ERRefclk-diffRrise, ERRefclk-diff-Fall	Differential Rising and falling edge rates	1	4	V/ns	
VRB-diff	Differential ringback voltage	-100	100	mV	
ERRefclk-diffRrise, ERRefclk-diff-Fall	Differential Rising and falling edge rates	1	4	V/ns	
VRB-diff	Differential ringback voltage	-100	100	mV	

Notes:

1. V_{DI} = | USBPx[P] – USBPx[N]
2. Includes VDI range
3. Applies to Low-Speed/Full-Speed USB
4. PCI Express mVdiff p-p = 2*|PETp[x] - PETn[x]|
5. SATA Vdiff, RX (VIMAX10/MIN10) is measured at the SATA connector on the receiver side (generally, the motherboard connector), where SATA mVdiff p-p = 2*|SATA[x]RXP - SATA[x]RXN|
6. VccRTC is the voltage applied to the VccRTC well of the PCH. When the system is in a G3 state, this is generally supplied by the coin cell battery, but for S5 and greater, this is generally VccSus3_3.
7. This is an AC Characteristic that represents transient values for these signals
8. Applies to Hogh-Speed USB 2.0.
9. 3.3 V refers to VccSus3_3 for signals in the suspend well and to Vcc3_3 for signals in the core well. See Table 3-2, or Table 3-3 for signal and power well association.
10. 1.1 V refers to VccIO or VccCore for signals in the core well and to VccASW for signals in the Active Sleep well. See Table 3-2 or Table 3-3 for signal and power well association.

Table 8-6. DC Characteristic Output Signal Association

Symbol	Associated Signals
VOH1/VOL1	**Processor Signal:** PM_SYNC, PM_SYNC2, PROCPWRGD
VOH2/VOL2	**LPC Signals:** LAD[3:0], LFRAME#, INIT3_3V# **Power Management Signal:** LAN_PHY_PWR_CTRL **PCI Signals:** AD[31:0], C/BE[3:0], DEVSEL#, FRAME#, IRDY#, PAR, PCIRST#, GNT[3:0]#, PME#(1) **Interrupt Signals:** PIRQ[D:A], PIRQ[H:E]#(1) **GPIO Signals:** GPIO[73, 72, 59, 56, 55:50, 49, 47:44 43:40, 37, 36, 35, 33, 28, 27, 26, 25, 23, 21, 20, 19, 18, 16, 15, 14, 13, 12, 10, 9, 8, 5:2, 0] **SPI Signals:** SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_CLK **GSX Signals:** GSCLK, GSXSLOAD, GSXSRESET#, GSXDOUT **Miscellaneous Signals:** SPKR
VOH3/VOL3	**SMBus Signals:** SMBCLK(1), SMBDATA(1) **System Management Signals:** SML[1:0]CLK(1), SML[1:0]DATA(1), SML0ALERT#, SML1ALERT# **GPIO Signals:** GPIO[75, 74, 60, 58, 11]
VOH4/VOL4	**Power Management Signals:** SLP_S3#, SLP_S4#, SLP_S5#, SLP_A#, SLP_LAN#, SUSCLK, DRAMPWROK, SLP_SUS# **SATA Signals**: SATALED#, SCLOCK, SLOAD, SDATAOUT0, SDATAOUT1 **GPIO Signals:** GPIO[71:68, 63:61, 57, 48, 39, 38, 34, 32, 31, 30, 29, 24, 22, 17, 7, 6, 1] **Interrupt Signals:** SERIRQ **ADR Signal:** ADR_COMPLETE
VOH5/VOL5	**USB Signals**: USBP[13:0][P,N] in Low-speed and Full-speed Modes
VOMIN6 -Gen3i/ VOMAX6-Gen3i	**SATA Signals:** SATA[1:0]TX[P,N] (6.0 Gb/s Internal SATA)
VOMIN7 -Gen1i,m/ VOMAX7-Gen1i,m	**SATA Signals:** SATA[5:0]TX[P,N] (1.5 Gb/s Internal and External SATA)
VOMIN7 -Gen2i,m/ VOMAX7-Gen2i,m	**SATA Signals:** SATA[5:0]TX[P,N] (3.0 Gb/s Internal and External SATA)
VOMIN8-PCIeGen12/ VOMAX8-PCIeGen12	**PCI Express Data TX Signals:** PET[p,n][8:1] (Gen 1 and Gen 2)
VOH9/VOL9	**Power Management Signal:** PLTRST#
VHSOI VHSOH VHSOL VCHIRPJ VCHIRPK	**USB Signals:** USBP[13:0][P:N] in High-speed Mode
VOH_HDA/VOL_HDA	**Intel High Definition Audio Signals:** HDA_RST#, HDA_SDOUT, HDA_SYNC, HDA_BCLK
VOL_JTAG	**JTAG Signals:** JTAG_TDO
VOH_PCICLK/ VOL_PCICLK	**GPIO Signals:** [67:64]
VOL_SGPIO	**SGPIO Signals:** SCLOCK, SLOAD, SDATAOUT0, SDATAOUT1
VOH_PWM/ VOL_PWM	**Thermal Control Signals:** PWM[3:0]
VOH_SST/VOL_SST	**SST signal: SST**
VOH_PECI/VOL_PECI	**PECI signal: PECI**

Note:
1. These signals are open-drain.

Table 8-7. DC Output Characteristics (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Unit	I_{OL} / I_{OH}	Notes
V_{OL1}	Output Low Voltage	—	0.255	V	3 mA	
V_{OH1}	Output High Voltage	V_PROC_IO - 0.3	V_PROC_IO	V	-3 mA	
V_{OL2}	Output Low Voltage	—	0.1 x 3.3 V	V	1.5 mA	7
V_{OH2}	Output High Voltage	0.9 x 3.3 V	3.3	V	-0.5 mA	7
V_{OL3}	Output Low Voltage	0	0.4	V		
V_{OH3}	Output High Voltage	3.3 V - 0.5	—	V	4 mA	1, 7
V_{OL4}	Output Low Voltage	—	0.4	V	6 mA	
V_{OH4}	Output High Voltage	3.3 V- 0.5	3.3 V	V	-2 mA	7
V_{OL5}	Output Low Voltage	—	0.4	V	5 mA	
V_{OH5}	Output High Voltage	3.3 V – 0.5	—	V	-2 mA	7
$V_{OMIN6\text{-}Gen3i}$	Minimum Output Voltage	200	—	mVdiff p-p		3
$V_{OMAX6\text{-}Gen3i}$	Maximum Output Voltage	—	900	mVdiff p-p		3
$V_{OMIN7\text{-}Gen1i,m}$	Minimum Output Voltage	400	—	mVdiff p-p		3
$V_{OMAX7\text{-}Gen1i,m}$	Maximum Output Voltage	—	600	mVdiff p-p		3
$V_{OMIN7\text{-}Gen2i,m}$	Minimum Output Voltage	400	—	mVdiff p-p		3
$V_{OMAX7\text{-}Gen2i,m}$	Maximum Output Voltage	—	700	mVdiff p-p		3
VOMIN8-PCIeGen12	Output Low Voltage	800	—	mVdiff p-p		2
VOMAX8-PCIeGen12	Output High Voltage	—	1200	mVdiff p-p		2
V_{OL9}	Output Low Voltage	—	0.1 x 3.3 V	V	1.5 mA	7
V_{OH9}	Output High Voltage	0.9 x 3.3 V	3.3	V	-2.0 mA	7
V_{OMIN10}	Minimum Output Voltage	800	—	mVdiff p-p		
V_{OMAX10}	Maximum Output Voltage	—	1600	mVdiff p-p		
V_{OMIN11}	Minimum Output Voltage	850	—	mVdiff p-p		
V_{OMAX11}	Maximum Output Voltage	—	1200	mVdiff p-p		
VOMIN12-PCIe8GT/s/	Minimum Output Voltage	250	—	mVdiff p-p		
VOMAX12-PCIe8GT/s	Maximum Output Voltage	—	1200	mVdiff p-p		
VHSOI	HS Idle Level	–10.0	10.0	mV		
VHSOH	HS Data Signaling High	360	440	mV		
VHSOL	HS Data Signaling Low	–10.0	10.0	mV		

Table 8-7. DC Output Characteristics (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Unit	I_{OL} / I_{OH}	Notes
VCHIRPJ	Chirp J Level	700	1100	mV		
VCHIRPK	Chirp K Level	–900	–500	mV		
VOL_HDA	Output Low Voltage	—	0.1 x VccSusHDA	V	1.5 mA	
VOH_HDA	Output High Voltage	0.9 x VccSusHDA	—	V	-0.5 mA	
VOL_PWM	Output Low Voltage	—	0.4	V	8 mA	
VOH_PWM	Output High Voltage	—	—			1
VOL_SGPIO	Output Low Voltage	—	0.4	V		
VOL_PCICLK	Output Low Voltage	—	0.4	V	-1 mA	
VOH_PCICLK	Output High Voltage	2.4		V	1 mA	
VOL_SST	Output Low Voltage	0	0.3	V	0.5 mA	
VOH_SST	Output High Voltage	1.1	1.5	V	-6 mA	
VOL_PECI	Output Low Voltage	—	0.25 x V_PROC_IO	V	0.5 mA	
VOH_PECI	Output High Voltage	0.75 x V_PROC_IO	V_PROC_IO		-6 mA	
VOL_HDA	Output Low Voltage	—	0.1 x VccHDA	V	1.5 mA	
VOL_JTAG	Output Low Voltage	0	0.1 x 1.05 V	V	1.5 mA	

Notes:

1. The SERR#, PIRQ[H:A], SMBDATA, SMBCLK, SML[1:0]CLK, SML[1:0]DATA, SML[1:0]'ALERT# and PWM[3:0] signal has an open-drain driver and SATALED# has an open-collector driver, and the V_{OH} specification does not apply. This signal must have external pull up resistor.
2. PCI Express mVdiff p-p = 2*|PETp[x] – PETn[x]|
3. SATA Vdiff, tx (V_{OMIN7}/V_{OMAX7}) is measured at the SATA connector on the transmit side (generally, the motherboard connector), where SATA mVdiff p-p = 2*|SATA[x]TXP – SATA[x]TXN|
4. Maximum Iol for PROCPWRGD is 12mA for short durations (<500 mS per 1.5 s) and 9 mA for long durations.
5. For INIT3_3V only, for low current devices, the following applies: V_{OL5} Max is 0.15 V at an I_{OL5} of 2 mA.
6. 3.3 V refers to VccSus3_3 for signals in the suspend well, to Vcc3_3 for signals in the core well and to VccDSW3_3 for those signals in the Deep Sleep well. See Table 3-2 or Table 3-3 for signal and power well association.
7. 3.3 V refers to VccSus3_3 for signals in the suspend well and to Vcc3_3 for signals in the core well and to VccDSW3_3 for signals in the ME well. See Table 3-2, or Table 3-3 for signal and power well association.

Table 8-8. Other DC Characteristics

Symbol	Parameter	Min	Nom	Max	Unit	Notes
V_PROC_IO	Processor I/F	.95	1.0 - 1.1	1.16	V	1
V5REF	PCH Core Well Reference Voltage	4.75	5	5.25	V	1
Vcc3_3	I/O Buffer Voltage	3.14	3.3	3.47	V	1
VccVRM	1.5 V Internal PLL and VRMs	1.455	1.5	1.545	V	1, 3
VccVRM	1.8 V Internal PLL and VRMs	1.746	1.8	1.854	V	1, 3
V5REF_Sus	Suspend Well Reference Voltage	4.75	5	5.25	V	1
VccSus3_3	Suspend Well I/O Buffer Voltage	3.14	3.3	3.47	V	1
VccCore	Internal Logic Voltage	1.05	1.1	1.16	V	1
VccIO	Core Well I/O buffers	1.05	1.1	1.16	V	1
VccDMI	DMI Buffer Voltage	.95	1.0 - 1.1	1.16	V	1
VccSPI	3.3 V Supply for SPI Controller Logic	3.14	3.3	3.47	V	1
VccASW	1.1 V Supply for Intel ME and Interated LAN	1.05	1.1	1.16	V	1
VccRTC (G3-S0)	Battery Voltage	2	—	3.47	V	1
VccSusHDA	High Definition Audio Controller Suspend Voltage	3.14	3.3	3.47	V	1
VccSusHDA (low voltage)	High Definition Audio Controller Low Voltage Mode Suspend Voltage	1.43	1.5	1.58	V	1
VccDFTERM	1.8 V supply power supply for DF_TVS	1.71	1.8	1.89	V	1
VccDSW3_3	3.3 V supply for Deep S4/S5 wells	3.14	3.3	3.47	V	1
VccRBIAS_SAS0	SAS0 RBIAS Voltage	1.05	1.1	1.15	V	4
VccRBIAS_SAS1	SAS1 RBIAS Voltage	1.05	1.1	1.15	V	4
I_{LI1}	PCI_3V Hi-Z State Data Line Leakage	–10	—	10	µA	(0 V < VIN < Vcc3_3)
I_{LI2}	PCI_5V Hi-Z State Data Line Leakage	–70	—	70	µA	Max V_{IN} = 2.7 V Min V_{IN} = 0.5 V
I_{LI3}	Input Leakage Current – All Other	–10	—	10	µA	2
C_{IN}	Input Capacitance – All Other	—	—	TBD	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance	—	—	TBD	pF	F_C = 1 MHz
$C_{I/O}$	I/O Capacitance	—	—	10	pF	F_C = 1 MHz
		Typical Value				
CL	XTAL25_IN	3			pF	
CL	RTCX1	6			pF	
CL	RTCX2	6			pF	

Notes:

1. The I/O buffer supply voltage is measured at the PCH package pins. The tolerances shown in Table 8-8 are inclusive of all noise from DC up to 20 MHz. In testing, the voltage rails should be measured with a bandwidth limited oscilloscope that has a rolloff of 3 dB/decade above 20 MHz.
2. Includes Single Ended clocks REFCLK14IN, and CLKIN_PCI.
3. Includes only DC tolerance. AC tolerance will be 2% in addition to this range.
4. Includes both DC and AC tolerance. For optimal effect, Min/Max value should be within 3% of the nominal value.

8.5 AC Characteristics

Table 8-9. PCI Express* and DMI Interface Timings

Symbol	Parameter	Min	Max	Unit	Figures	Notes
Transmitter and Receiver Timings						
UI	Unit Interval – PCI Express* Gen 1 (2.5 GT/s)	399.88	400.12	ps		5
UI	Unit Interval – PCI Express Gen 2 (5.0 GT/s)	199.9	200.1	ps		5
UI	Unit Interval – DMI	399.88	400.12	ps		5
T_{TX-EYE}	Minimum Transmission Eye Width	0.7	—	UI	8-25	1,2
$T_{TX-RISE/Fall\ (Gen1)}$	D+/D- TX Out put Rise/Fall time	-0.125	—	UI		1,2
$T_{TX-RISE/Fall\ (Gen2)}$	D+/D- TX Out put Rise/Fall time	-0.15	—	UI		1,2
T_{RX-EYE}	Minimum Receiver Eye Width	0.40	—	UI	8-26	3,4

Notes:

1. Specified at the measurement point into a timing and voltage compliance test load and measured over any 250 consecutive TX UIs. (Also refer to the Transmitter compliance eye diagram)
2. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TXJITTER-MAX}$ = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TXEYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
3. Specified at the measurement point and measured over any 250 consecutive UIs. The test load documented in the PCI Express* specification 2.0 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
4. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to--MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total 0.6 UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
5. Nominal Unit Interval is 400 ps for 2.5 GT/s and 200 ps for 5 GT/s.

Table 8-10. Clock Timings (Sheet 1 of 3)

Sym	Parameter	Min	Max	Unit	Notes	Figure
REFCLK14IN						
t6	Period	69.820	69.862	ns		
t7	High time	29.975	38.467	ns		
t8	Low time	29.975	38.467	ns		
	Duty Cycle	40	60	%		
	Rising Edge Rate	1.0	4	V/ns		
	Falling Edge Rate	1.0	4	V/ns		
	Jitter	—	800	ps		
SMBus/SMLink Clock (SMBCLK, SML[1:0]CLK)						
f_{smb}	Operating Frequency	10	100	KHz	5	
t22	High time	4.0	50	µs	1	8-20

Table 8-10. Clock Timings (Sheet 2 of 3)

Sym	Parameter	Min	Max	Unit	Notes	Figure
t23	Low time	4.7	—	µs		8-20
t24	Rise time	—	1000	ns		8-20
t25	Fall time	—	300	ns		8-20
SMLink0 Clock (SML0CLK) (See note 7)						
fsmb	Operating Frequency	0	400	KHz		
t22_SML	High time	0.6	50	ms	2	8-20
t23_SML	Low time	1.3	—	ms		8-20
t24_SML	Rise time	—	300	ns		8-20
t25_SML	Fall time	—	300	ns		8-20
HDA_BCLK (Intel High Definition Audio)						
f_{HDA}	Operating Frequency	24.0		MHz		
	Frequency Tolerance	—	100	ppm		
t26a	Input Jitter (refer to Clock Chip Specification)	—	300	ppm		
t27a	High Time (Measured at 0.75 Vcc)	18.75	22.91	ns		8-11
t28a	Low Time (Measured at 0.35 Vcc)	18.75	22.91	ns		8-11
SATA Clock and DMI Clock (CLKIN_SATA_[P:N]) from a Clock Chip						
t36	Period	9.997	10.0533	ns		
	Slew rate	1	8	V/ns		
	Input Jitter (refer to Clock Chip Specification)	—	150	ps	3	
DMI Clock (CLKIN_DMI_[P:N]) from a Clock Chip						
tDMI	Period	9.997	10.0533	ns		
	Slew rate	1	4	V/ns		
	clock duty cycle	40	60	%		
	differential jitter		500	ps		
	VRB-Diff	-100	100	mV		
Tstable		500	—	ps		
SAS Clock (CLKIN_SPCIE0_[P:N], CLKIN_SAS[1:0]_[P:N]) from a Clock Chip						
	Reference Clock Frequency	100	—	MHz		
tSAS	Period	9.847	10.203	ns		
	slew rate	1	4	V/ns	8	
	clock duty cycle	45	55	%		
Tstable		500	—	ps		
DOT 96 MHz (CLKIN_DOT96[P,N]) from a clock chip						
t36	Period	10.066	10.768	ns		
	Slew rate	1	8	V/ns		
	Input Jitter (refer to Clock Chip Specification)	—	350	ps	3	
Suspend Clock (SUSCLK)						
f_{susclk}	Operating Frequency	32		kHz	2	
t39	High Time	10	—	µs	2	
t39a	Low Time	10	—	µs	2	

Table 8-10. Clock Timings (Sheet 3 of 3)

Sym	Parameter	Min	Max	Unit	Notes	Figure
SPI_CLK						
Slew_Rise	Output Rise Slew Rate (0.2Vcc - 0.6Vcc)	1	4	V/ns	4	8-22
Slew_Fall	Output Fall Slew Rate (0.6Vcc - 0.2Vcc)	1	4	V/ns	4	8-22

Notes:
1. The maximum high time (t18 Max) provide a simple ensured method for devices to detect bus idle conditions.
2. SUSCLK duty cycle can range from 30% minimum to 70% maximum.
3. Jitter is specified as cycle to cycle measured in pico seconds. Period min and max includes cycle to cycle jitter
4. Testing condition: 1 kohm pull up to Vcc, 1 kohm pull down and 10 pF pull down and 1/2 inch trace. See Figure 8-28 for more detail.
5. When the PCH communicates to BMC using the SMLINK signal, up to 400 kHz clock frequency can be supported.
6. When SMLink0 is configured to run in Fast Mode using a soft strap, the operating frequency is in the range of 300 KHz-400 KHz.

Table 8-11. PCI Interface Timing

Sym	Parameter	Min	Max	Units	Notes	Figure
t40	AD[31:0] Valid Delay	2	11	ns	1	8-12
t41	AD[31:0] Setup Time to PCICLK Rising	7	—	ns		8-13
t42	AD[31:0] Hold Time from PCICLK Rising	0	—	ns		8-13
t43	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, PERR#, PLOCK#, DEVSEL# Valid Delay from PCICLK Rising	2	11	ns	1	8-12
t44	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PAR, PERR#, PLOCK#, IDSEL, DEVSEL# Output Enable Delay from PCICLK Rising	2	—	ns		8-16
t45	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PERR#, PLOCK#, DEVSEL#, GNT[A:B]# Float Delay from PCICLK Rising	2	28	ns		8-14
t46	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, SERR#, PERR#, DEVSEL#, Setup Time to PCICLK Rising	7	—	ns		8-13
t47	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, SERR#, PERR#, DEVSEL#, REQ[A:B]# Hold Time from PCLKIN Rising	0	—	ns		8-13
t48	PCIRST# Low Pulse Width	1		ms		8-15
t49	GNT[3:0]# Valid Delay from PCICLK Rising	2	12	ns		
t50	REQ[3:0]# Setup Time to PCICLK Rising	12	—	ns		

Note:
1. Refer to note 3 of table 4-4 in Section 4.2.2.2 and note 2 of table 4-6 in Section 4.2.3.2 of the *PCI Local Bus Specification*, Revision 2.3, for measurement details.

Table 8-12. Universal Serial Bus Timing

Sym	Parameter	Min	Max	Units	Notes	Fig
Full-speed Source (Note 7)						
t100	USBPx+, USBPx- Driver Rise Time	4	20	ns	1, 6 C_L = 50 pF	8-17
t101	USBPx+, USBPx- Driver Fall Time	4	20	ns	1, 6 C_L = 50 pF	8-17
t102	Source Differential Driver Jitter - To Next Transition - For Paired Transitions	 −3.5 −4	 3.5 4	 ns ns	2, 3	8-18
t103	Source SE0 interval of EOP	160	175	ns	4	8-19
t104	Source Jitter for Differential Transition to SE0 Transition	−2	5	ns	5	
t105	Receiver Data Jitter Tolerance - T o Next Transition - For Paired Transitions	 −18.5 −9	 18.5 9	 ns ns	3	8-18
t106	EOP Width: Must accept as EOP	82	—	ns	4	8-19
t107	Width of SE0 interval during differential transition	—	14	ns		
Low-speed Source (Note 8)						
t108	USBPx+, USBPx – Driver Rise Time	75	300	ns	6 C_L = 200pF C_L = 600pF	8-17
t109	USBPx+, USBPx – Driver Fall Time	75	300	ns	6 C_L = 200pF C_L = 600pF	8-17
t110	Source Differential Driver Jitter To Next Transition For Paired Transitions	 −25 −14	 25 14	 ns ns	2, 3	8-18
t111	Source SE0 interval of EOP	1.25	1.50	µs	4	8-19
t112	Source Jitter for Differential Transition to SE0 Transition	−40	100	ns	5	
t113	Receiver Data Jitter Tolerance - To Next Transition- For Paired Transitions	 −152 −200	 152 200	 ns ns	3	8-18
t114	EOP Width: Must accept as EOP	670	—	ns	4	8-19
t115	Width of SE0 interval during differential transition	—	210	ns		

Notes:

1. Driver output resistance under steady state drive is specified at 28 Ω at minimum and 43 Ω at maximum.
2. Timing difference between the differential data signals.
3. Measured at crossover point of differential data signals.
4. Measured at 50% swing point of data signals.
5. Measured from last crossover point to 50% swing point of data line at leading edge of EOP.
6. Measured from 10% to 90% of the data signal.
7. Full-speed Data Rate has minimum of 11.97 Mb/s and maximum of 12.03 Mb/s.
8. Low-speed Data Rate has a minimum of 1.48 Mb/s and a maximum of 1.52 Mb/s.

Table 8-13. SATA Interface Timings

Sym	Parameter	Min	Max	Units	Notes	Figure
UI	Gen I Operating Data Period	666.43	670.23	ps		
UI-2	Gen II Operating Data Period (3Gb/s)	333.21	335.11	ps		
UI-3	Gen III Operating Data Period (6Gb/s)	166.6667	166.6083	ps		
t120gen1	Rise Time	0.15	0.41	UI	1	
t120gen2	Rise Time	0.2	0.41	UI	1	
t120gen3	Rise Time	0.2	0.41	UI	1	
t121gen1	Fall Time	0.15	0.41	UI	2	
t121gen2	Fall Time	0.2	0.41	UI	2	
t121gen3	Fall Time	0.2	0.41	UI	2	
t122	TX differential skew	—	20	ps		
t123	COMRESET	310.4	329.6	ns	3	
t124	COMWAKE transmit spacing	103.5	109.9	ns	3	
t125	OOB Operating Data period	646.67	686.67	ns	4	

Notes:
1. 20% – 80% at transmitter
2. 80% – 20% at transmitter
3. As measured from 100 mV differential crosspoints of last and first edges of burst.
4. Operating data period during Out-Of-Band burst transmissions.

Table 8-14. SMBus and SMLink Timing

Sym	Parameter	Min	Max	Units	Notes	Fig
t130	Bus Free Time Between Stop and Start Condition	4.7	—	µs		8-20
$t130_{SMLFM}$	Bus Free Time Between Stop and Start Condition	1.3	—	µs	5	8-20
t131	Hold Time after (repeated) Start Condition. After this period, the first clock is generated.	4.0	—	µs		8-20
$t131_{SMLFM}$	Hold Time after (repeated) Start Condition. After this period, the first clock is generated.	0.6	—	µs	5	8-20
t132	Repeated Start Condition Setup Time	4.7	—	µs		8-20
$t132_{SMLFM}$	Repeated Start Condition Setup Time	0.6	—	µs	5	8-20
t133	Stop Condition Setup Time	4.0	—	µs		8-20
$t133_{SMLFM}$	Stop Condition Setup Time	0.6	—	µs	5	8-20
t134	Data Hold Time	0	—	ns	4	8-20
$t134_{SMLFM}$	Data Hold Time	0	—	ns	4, 5	8-20
t135	Data Setup Time	250	—	ns		8-20
$t135_{SMLFM}$	Data Setup Time	100	—	ns	5	8-20
t136	Device Time Out	25	35	ms	1	
t137	Cumulative Clock Low Extend Time (slave device)	—	25	ms	2	8-21
t138	Cumulative Clock Low Extend Time (master device)	—	10	ms	3	8-21

Notes:
1. A device will timeout when any clock low exceeds this value.
2. t137 is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to stop. If a slave device exceeds this time, it is expected to release both its clock and data lines and reset itself.
3. t138 is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from start-to-ack, ack-to-ack or ack-to-stop.
4. t134 has a minimum timing for I^2C of 0 ns, while the minimum timing for SMBus is 300 ns.
5. Timings with the SMLFM designator apply only to SMLink0 and only when SMLink0 is operating in Fast Mode.

Table 8-15. Intel® High Definition Audio Timing

Sym	Parameter	Min	Max	Units	Notes	Fig
t143	Time duration for which HDA_SDO is valid before HDA_BCLK edge.	7	—	ns		8-23
t144	Time duration for which HDA_SDO is valid after HDA_BCLK edge.	7	—	ns		8-23
t145	Setup time for HDA_SDIN[3:0] at rising edge of HDA_BCLK	15	—	ns		8-23
t146	Hold time for HDA_SDIN[3:0] at rising edge of HDA_BCLK	0	—	ns		8-23

Table 8-16. LPC Timing

Sym	Parameter	Min	Max	Units	Notes	Fig
t150	LAD[3:0] Valid Delay from PCICLK Rising	2	11	ns		8-12
t151	LAD[3:0] Output Enable Delay from PCICLK Rising	2	—	ns		8-16
t152	LAD[3:0] Float Delay from PCICLK Rising	—	28	ns		8-14
t153	LAD[3:0] Setup Time to PCICLK Rising	7	—	ns		8-13
t154	LAD[3:0] Hold Time from PCICLK Rising	0	—	ns		8-13
t155	LDRQ[1:0]# Setup Time to PCICLK Rising	12	—	ns		8-13
t156	LDRQ[1:0]# Hold Time from PCICLK Rising	0	—	ns		8-13
t157	eE# Valid Delay from PCICLK Rising	2	12	ns		8-12

Table 8-17. Miscellaneous Timings

Sym	Parameter	Min	Max	Units	Notes	Fig
t160	SERIRQ Setup Time to PCICLK Rising	7	—	ns		8-13
t161	SERIRQ Hold Time from PCICLK Rising	0	—	ns		8-13
t162	RI#, GPIO, USB Resume Pulse Width	2	—	RTCCLK		8-15
t163	SPKR Valid Delay from OSC Rising	—	200	ns		8-12
t164	SERR# Active to NMI Active	—	200	ns		

Table 8-18. SPI Timings (20 MHz)

Sym	Parameter	Min	Max	Units	Notes	Fig
t180a	Serial Clock Frequency - 20M Hz Operation	17.06	18.73	MHz	1	
t183a	Tco of SPI_MOSI with respect to serial clock falling edge at the host	-5	13	ns		8-22
t184a	Setup of SPI_MISO with respect to serial clock falling edge at the host	16	—	ns		8-22
t185a	Hold of SPI_MISO with respect to serial clock falling edge at the host	0	—	ns		8-22
t186a	Setup of SPI_CS[1:0]# assertion with respect to serial clock rising at the host	30	—	ns		8-22
t187a	Hold of SPI_CS[1:0]# deassertion with respect to serial clock falling at the host	30	—	ns		8-22
t188a	SPI_CLK high time	26.37	—	ns		8-22
t189a	SPI_CLK low time	26.82	—	ns		8-22

Notes:
1. The typical clock frequency driven by the PCH is 17.86 MHz.
2. Measurement point for low time and high time is taken at 0.5 (VccSUS3_3).

Table 8-19. SPI Timings (33 MHz)

Sym	Parameter	Min	Max	Units	Notes	Fig
t180b	Serial Clock Frequency - 33 MHz Operation	29.83	32.81	MHz	1	
t183b	Tco of SPI_MOSI with respect to serial clock falling edge at the host	-5	5	ns		8-22
t184b	Setup of SPI_MISO with respect to serial clock falling edge at the host	8	—	ns		8-22
t185b	Hold of SPI_MISO with respect to serial clock falling edge at the host	0	—	ns		8-22
t186b	Setup of SPI_CS[1:0]# assertion with respect to serial clock rising at the host	30	—	ns		8-22
t187b	Hold of SPI_CS[1:0]# deassertion with respect to serial clock falling at the host	30	—	ns		8-22
t188b	SPI_CLK High time	14.88	—	ns		8-22
t189b	SPI_CLK Low time	15.18	—	ns		8-22

Notes:
1. The typical clock frequency driven by the PCH is 31.25 MHz.
2. Measurement point for low time and high time is taken at 0.5 (VccSUS3_3).

Table 8-20. SPI Timings (50 MHz)

Sym	Parameter	Min	Max	Units	Notes	Fig
t180c	Serial Clock Frequency - 50 MHz Operation	46.99	53.40	MHz	1	8-22
t183c	Tco of SPI_MOSI with respect to serial clock falling edge at the host	-3	3	ns		8-22
t184c	Setup of SPI_MISO with respect to serial clock falling edge at the host	8	—	ns		8-22
t185c	Hold of SPI_MISO with respect to serial clock falling edge at the host	0	—	ns		8-22
t186c	Setup of SPI_CS[1:0]# assertion with respect to serial clock rising edge at the host	30	—	ns		8-22
t187c	Hold of SPI_CS[1:0]# assertion with respect to serial clock rising edge at the host	30	—	ns		8-22
t188c	SPI_CLK High time	7.1	—	ns	2, 3	8-22
t189c	SPI_CLK Low time	11.17	—	ns	2, 3	8-22

Notes:
1. Typical clock frequency driven by the PCH is 50 MHz. This frequency is not available for ES1 samples.
2. When using 50 MHz mode ensure target flash component can meet t188c and t189c specifications.
3. Measurement point for low time and high time is taken at 0.5 (VccSUS3_3).

Table 8-21. SST Timings

Sym	Parameter	Min	Max	Units	Notes	Fig
t_{BIT}	Bit time (overall time evident on SST) Bit time driven by an originator	0.495 0.495	500 250	µs µs	1	-
$t_{BIT,}$jitter	Bit time jitter between adjacent bits in an SST message header or data bytes after timing has been negotiated	—	—	%		
$t_{BIT,}$drift	Change in bit time across a SST address or SST message bits as driven by the originator. This limit only applies across t_{BIT-A} bit drift and t_{BIT-M} drift.	—	—	%		
t_{H1}	High level time for logic '1'	0.6	0.8	x tBIT	2	
t_{H0}	High level time for logic '0'	0.2	0.4	x tBIT		
t_{SSTR}	Rise time (measured from V_{OL} = 0.3V to $V_{IH,min}$)	—	25 + 5	ns/ node		
t_{SSTF}	Fall time (measured from V_{OH} = 1.1V to $V_{IL,max}$)	—	33	ns/ node		

Notes:
1. The originator must drive a more restrictive time to allow for quantized sampling errors by a client yet still attain the minimum time less than 500 µs. t_{BIT} limits apply equally to t_{BIT}-A and t_{BIT}-M. PCH is targeted on 1 Mbps which is 1 µs bit time.
2. The minimum and maximum bit times are relative to t_{BIT} defined in the Timing Negotiation pulse.
3. t_{BIT}-A is the negotiated address bit time and t_{BIT}-M is the negotiated message bit time.

Table 8-22. PECI Timings

Sym	Parameter	Min	Max	Units	Notes	Fig
t_{BIT}	Bit time (overall time evident on PECI) Bit time driven by an originator	0.495 0.495	500 250	µs µs	1	
$t_{BIT,}$jitter	Bit time jitter between adjacent bits in an PECI message header or data bytes after timing has been negotiated	—	—	%		
$t_{BIT,}$drift	Change in bit time across a PECI address or PECI message bits as driven by the originator. This limit only applies across t_{BIT-A} bit drift and t_{BIT-M} drift.	—	—	%		
t_{H1}	High level time for logic '1'	0.6	0.8	x tBIT	2	
t_{H0}	High level time for logic '0'	0.2	0.4	x tBIT		
t_{PECIR}	Rise time (measured from VOL to VIH,min, Vtt(nom) -5%)	—	30 + 5	ns/ node	3	
t_{PECIF}	Fall time (measured from V_{OH} to V_{IL},max, Vtt(nom) +5%)	—	30	ns/ node	3	

Notes:
1. The originator must drive a more restrictive time to allow for quantized sampling errors by a client yet still attain the minimum time less than 500 µs. t_{BIT} limits apply equally to t_{BIT-A} and t_{BIT-M}. PCH is targeted on 2 MHz which is 500 ns bit time.
2. The minimum and maximum bit times are relative to t_{BIT} defined in the Timing Negotiation pulse.
3. Extended trace lengths may appear as additional nodes.
4. t_{BIT}-A is the negotiated address bit time and t_{BIT}-M is the negotiated message bit time.

8.6 Power Sequencing and Reset Signal Timings

Table 8-23. Power Sequencing and Reset Signal Timings (Sheet 1 of 2)

Sym	Parameter	Min	Max	Units	Notes	Fig
t200	VccRTC active to RTCRST# deassertion	9	—	ms		8-1, 8-2
t200a	RTCRST# deassertion to DPWROK high	0	—	ms		8-1, 8-2
t200b	VccDSW3_3 active to DPWROK high	10	—	ms		8-1, 8-2
t200c	VccDSW3_3 active to VccSus3_3 active	0	—	ms		8-1, 8-2
t201	VccSUS active to RSMRST# deassertion	10	—	ms	1	8-1, 8-2
t202	DPWROK high to SLP_SUS# deassertion	95	—	ms	2, 3	8-1, 8-2
t202a	RSMRST# and SLP_SUS# deassertion to SUSCLK toggling	5	—	ms	3, 4	8-1, 8-2
t203	SLP_S5# high to SLP_S4# high	30	—	us	5	8-3
t204	SLP_S4# high to SLP_S3# high	30	—	us	6	8-3
t205	Vcc active to PCH_PWROK active	10	—	ms	7, 14	8-3, 8-4
t206	PCH_PWROK deglitch time	1	—	ms	8	8-3, 8-4
t207	VccASW active to APWROK high	1	—	ms		8-3
t208	Clock chip clock outputs to PCH_PWROK high	1	—	ms		8-3, 8-4
t209	PCH_PWROK active to PROCPWRGD active	1	—	ms		8-3, 8-4
t210	PROCPWRGD and SYS_PWROK high to PLTRST# deassertion	1.06	—	ms		8-3, 8-4
t212	APWROK high to SPI Soft-Strap Reads	500	—	µs	22	8-5
t214	DMI message and all PCI Express ports and DMI in L2/L3 state to PLTRST# active	270	—	us		8-6
t217	PLTRST# active to PROCPWRGD inactive	30	—	us		8-6
t218	PROCPWRGD inactive to SLP_S3# assertion	11	—	us		8-6
t220	SLP_S3# low to SLP_S4# low	30	—	us		8-6
t221	SLP_S4# low to SLP_S5# low	30	—	us		8-6
t222	SLP_S3# active to PCH_PWROK deasserted	0	—			8-6
t223	PCH_PWROK rising to DRAMPWRGD rising	0	—	us		8-8
t224	DRAMPWRGD falling to SLP_S4# falling	-100	—	ns	12	8-8
t225	VccRTC active to VccDSW3_3 active	0	—	ms	1, 13	8-2
t226	RTCRST# deassertion to RSMRST# deassertion	20	—	ns		8-2
t227	VccSUS active to VccASW active	0	—	ms	1	
t229	VccASW active to Vcc active	0	—	ms		
t230	APWROK high to PCH_PWROK high	0	—	ms		

Table 8-23. Power Sequencing and Reset Signal Timings (Sheet 2 of 2)

Sym	Parameter	Min	Max	Units	Notes	Fig
t231	PCH_PWROK low to Vcc falling	40	—	ns	14, 15, 16	
t232	APWROK falling to VccASW falling	40	—	ns	16	
t233	SLP_S3# assertion to VccCore rail falling	5	—	us	14, 15	
t234	DPWROK falling to VccDSW rail falling	40	—	ns		8-7
t235	RSMRST# assertion to VccSUS falling	40	—	ns	1, 15, 16	8-7
t236	RTCRST# assertion to VccRTC falling	0	—	ms		8-7
t237	SLP_LAN# (or LANPHYPC) rising to Intel LAN Phy power high and stable	—	20	ms		
t238	DPWROK falling to any of VccDSW, VccSUS, VccASW, VccASW3_3, or Vcc falling	40	—	ns	1, 14, 15, 16	
t239	V5REF_Sus active to VccSus3_3 active	0	—	ms	17	
t240	V5REF active to Vcc3_3 active	See Note 15	—	ms	17	
t241	VccSus supplies active to Vcc supplies active	0	—	ms	1, 14	
t242	HDA_RST# active low pulse width	1	—	µs		
t244	VccSus active to SLP_S5#, SLP_S4#, SLP_S3#, PLTRST# and PCIRST# valid	—	50	ns	21	
t246	S4 Wake Event to SLP_S4# inactive (S4 Wake)	See Note Below			5	
t247	S3 Wake Event to SLP_S3# inactive (S3 Wake)	See Note Below			6	
t251	RSMRST# deassertion to APWROK assertion	0		ms		
t252	THRMTRIP# active to SLP_S3#, SLP_S4#, SLP_S5# active		175	ns		
t253	RSMRST# rising edge transition from 20% to 80%		50	µs		
t254	RSMRST# falling edge transition		50	µs	19, 20	

Notes:

1. VccSus supplies include VccSus3_3, V5REF_Sus, VccSusHDA.
2. This timing is a nominal value counted using RTC clock. If RTC clock isn't already stable at the rising edge of RSMRST#, this timing could be longer than the specified value.
3. Platforms not supporting Deep S4/S5 will typically have SLP_SUS# left as no connect. Hence DPWROK high and RSMRST# deassertion to SUSCLK toggling would be t202+t202a=100ms minimum
4. Platforms supporting Deep S4/S5 will have SLP_SUS# deassert prior to RSMRST#. Platforms not supporting Deep S4/S5 will have RSMRST# deassert prior to SLP_SUS#.
5. Dependency on SLP_S4# and SLP_A# stretching
6. Dependency on SLP_S3# and SLP_A# stretching
7. It is required that the power rails associated with PCI/PCIe (typically the 3.3 V, 5 V, and 12 V core well rails) have been valid for 99 ms prior to PCH_PWROK assertion in order to comply with the 100 ms PCI/PCIe 2.0 specification on PLTRST# deassertion. System designers must ensure the requirement is met on the platforms.
8. Ensure PCH_PWROK is a solid logic '1' before proceeding with the boot sequence.
   Note: If PCH_PWROK drops after t206 it will be considered a power failure.
9. Not Applicable for PCH.
10. Not Applicable for PCH.
11. Requires SPI messaging to be completed.
12. The negative min timing implies that DRAMPWRGD must either fall before SLP_S4# or within 100 ns after it.
13. The VccDSW3_3 supplies must never be active while the VccRTC supply is inactive.
14. Vcc includes VccIO, VccCORE, Vcc3_3, Vcc1_1, V5REF, V_PROC_IO, VccDMI and VccASW (if Intel® ME only powered in S0).
15. A Power rail is considered to be inactive when the rail is at its nominal voltage minus 5% or less.
16. Board design may meet (t231 AND t232 AND t235) OR (t238).

17. V5REF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7 V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within 0.7 V. V5REF_Sus must be powered up before VccSus3_3, or after VccSus3_3 within 0.7 V. Also, V5REF_Sus must power down after VccSus3_3, or before VccSus3_3 within 0.7 V.
18. If RTC clock is not already stable at RSMRST# rising edge, this time may be longer.
19. RSMRST# falling edge must transition to 0.8 V or less before VccSus3_3 drops to 2.9 V
20. The 50 µs should be measured from Vih to Vil (2 V to 0.78 V).
21. This is an internal timing showing when the signals (SLP_S5#, SLP_S4#, SLP_S3#, PLTRST# and PCIRST#) are valid after VccSus rail is Active.
22. APWROK high to SPI Soft-Start Read is an internal PCH timing. The timing cannot be measured externally and included here for general power sequencing reference.

8.7 Power Management Timing Diagrams

Figure 8-1. G3 w/RTC Loss to S4/S5 (With Deep S4/S5 Support) Timing Diagram

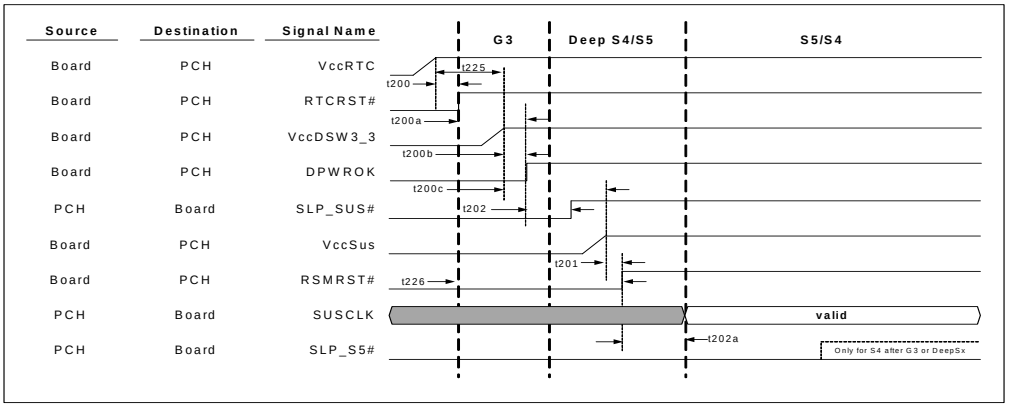


Figure 8-2. G3 w/RTC Loss to S4/S5 (Without Deep S4/S5 Support) Timing Diagram

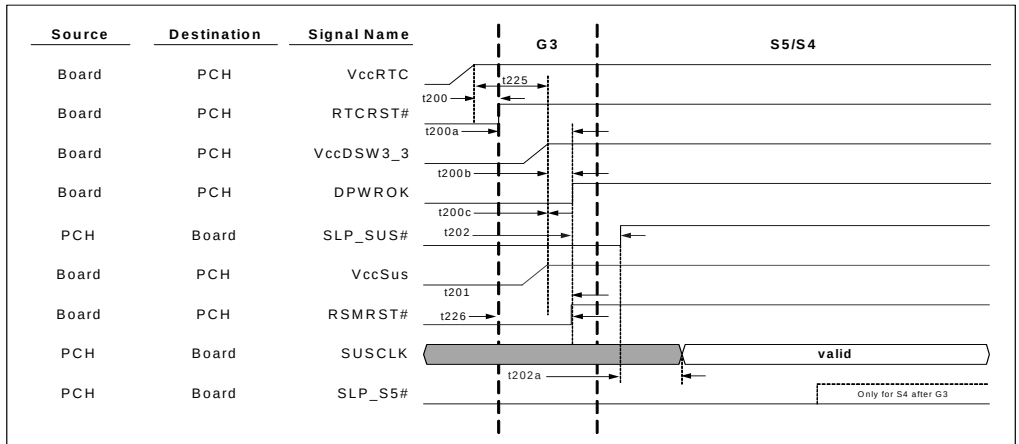


Figure 8-3. S5 to S0 Timing Diagram

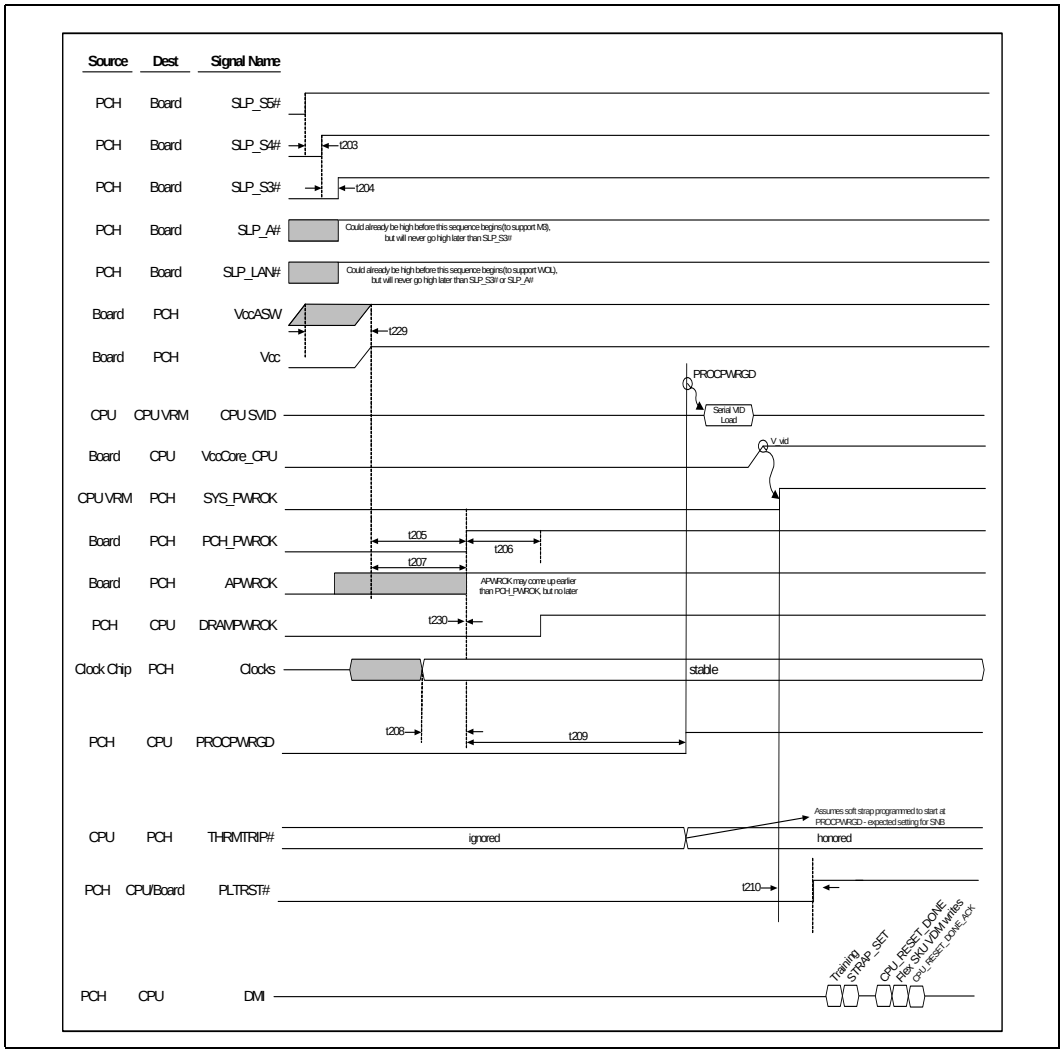


Figure 8-4. S3/M3 to S0 Timing Diagram

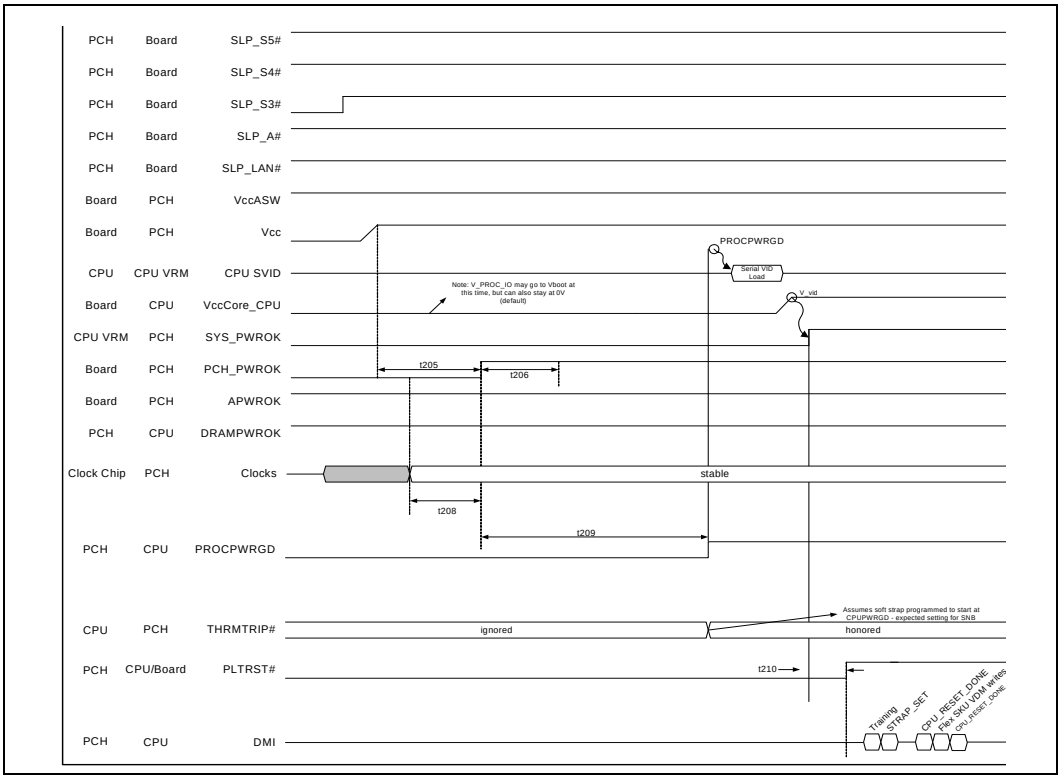


Figure 8-5. S5/Moff - S5/M3 Timing Diagram

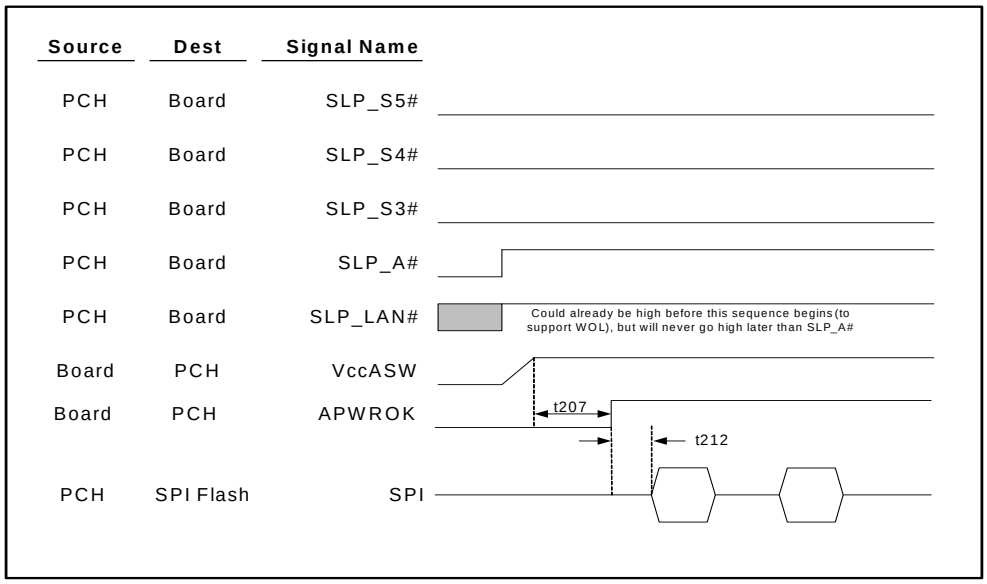


Figure 8-6. S0 to S5 Timing Diagram

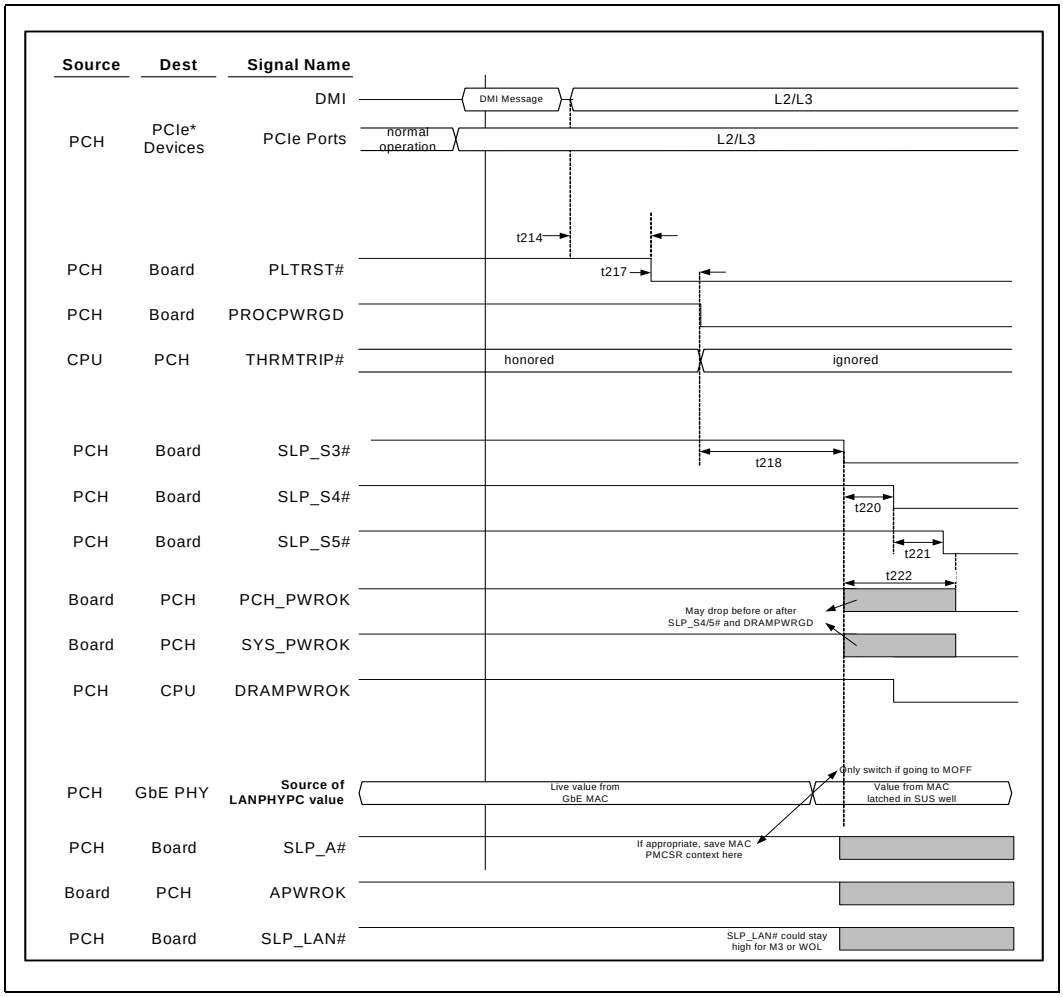


Figure 8-7. S4/S5 to Deep S4/S5 to G3 w/ RTC Loss Timing Diagram

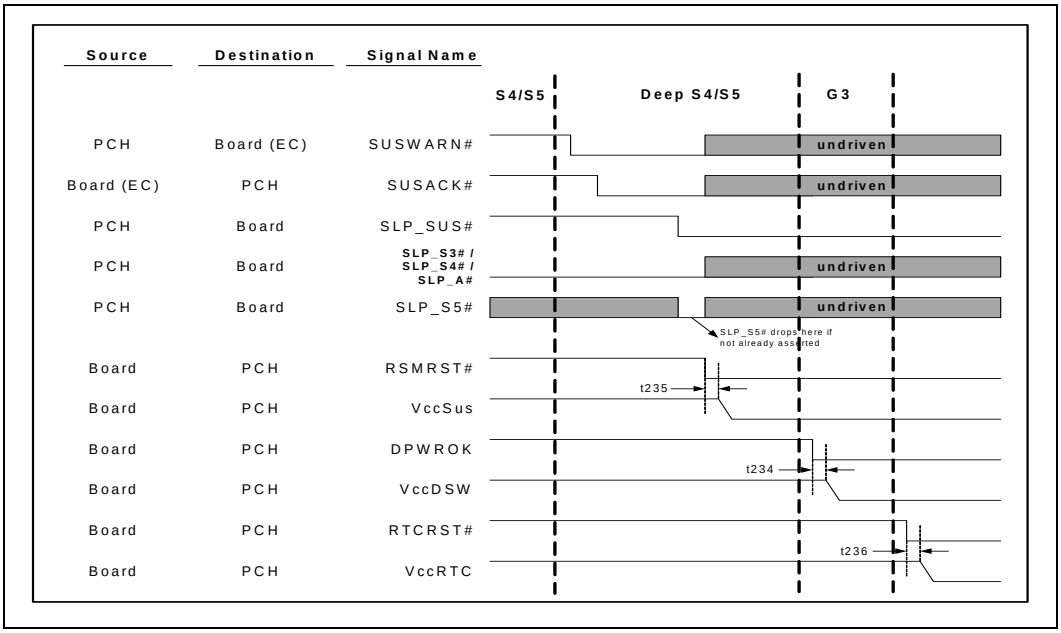
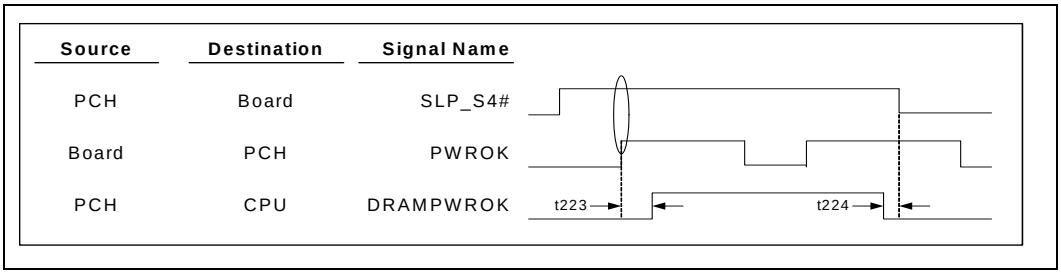


Figure 8-8. DRAMPWROK Timing Diagram



8.8 AC Timing Diagrams

Figure 8-9. Clock Cycle Time

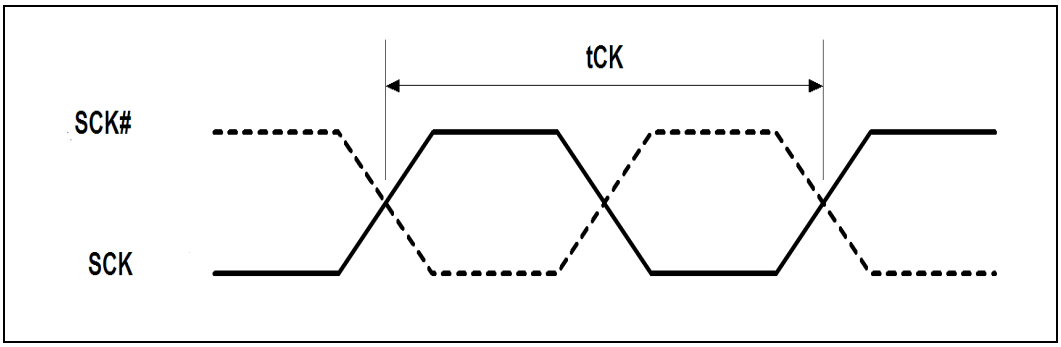


Figure 8-10. Transmitting Position (Data to Strobe)

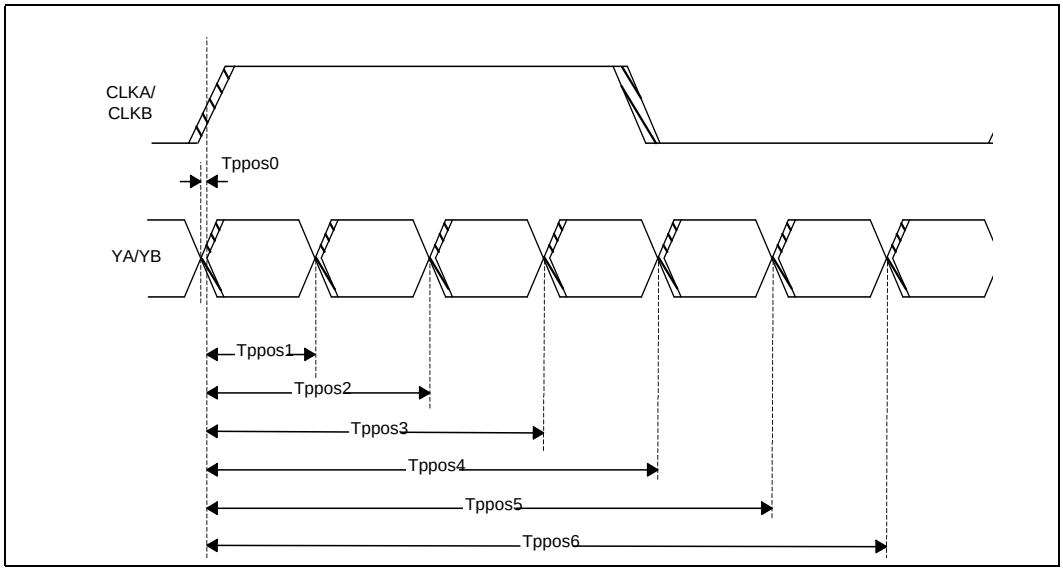


Figure 8-11. Clock Timing

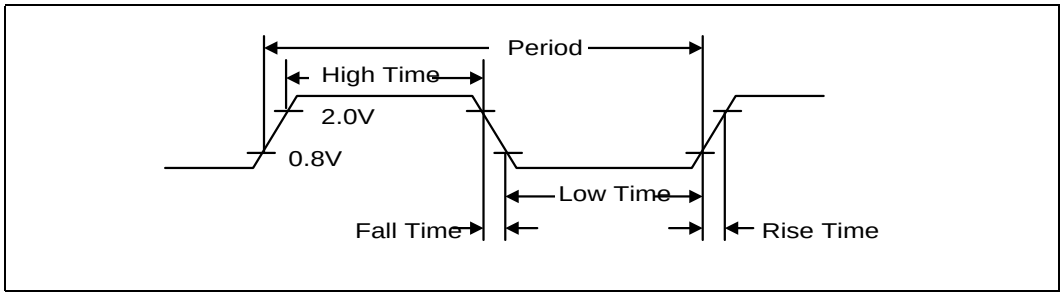


Figure 8-12. Valid Delay from Rising Clock Edge

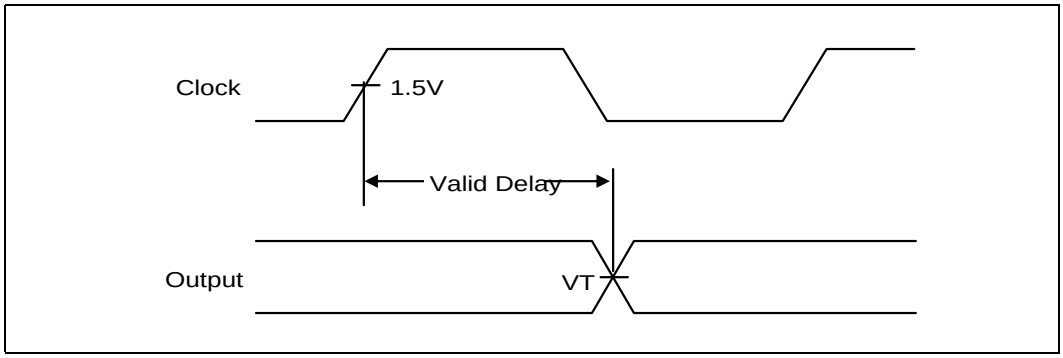


Figure 8-13. Setup and Hold Times

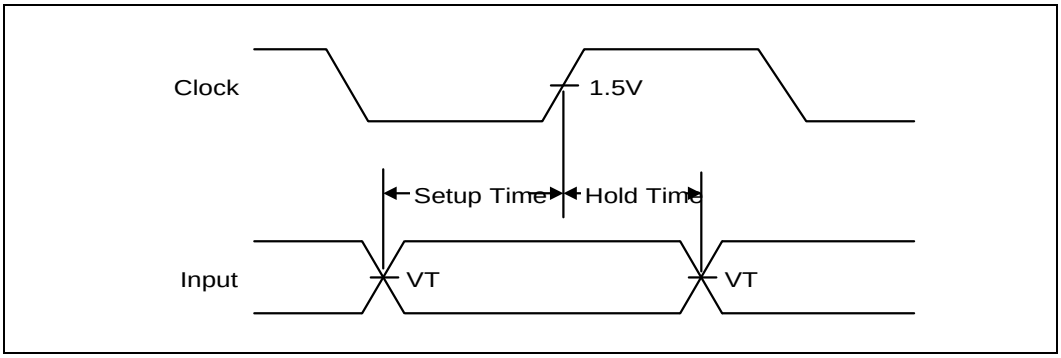


Figure 8-14. Float Delay

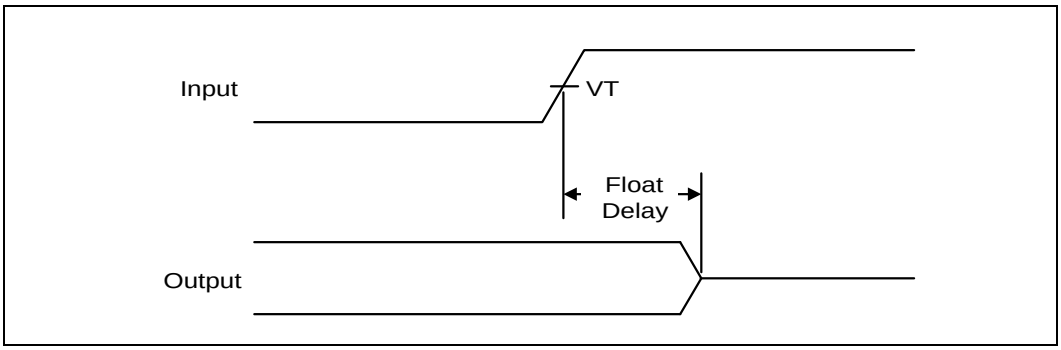


Figure 8-15. Pulse Width

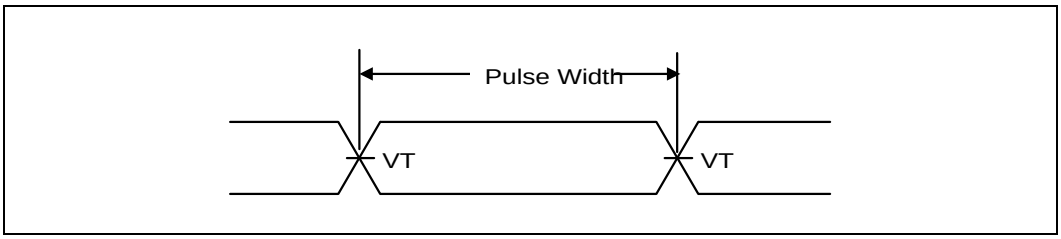


Figure 8-16. Output Enable Delay

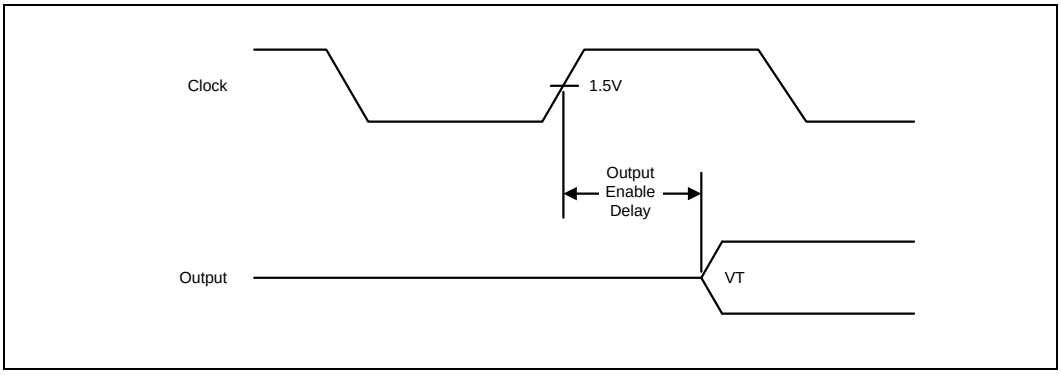


Figure 8-17. USB Rise and Fall Times

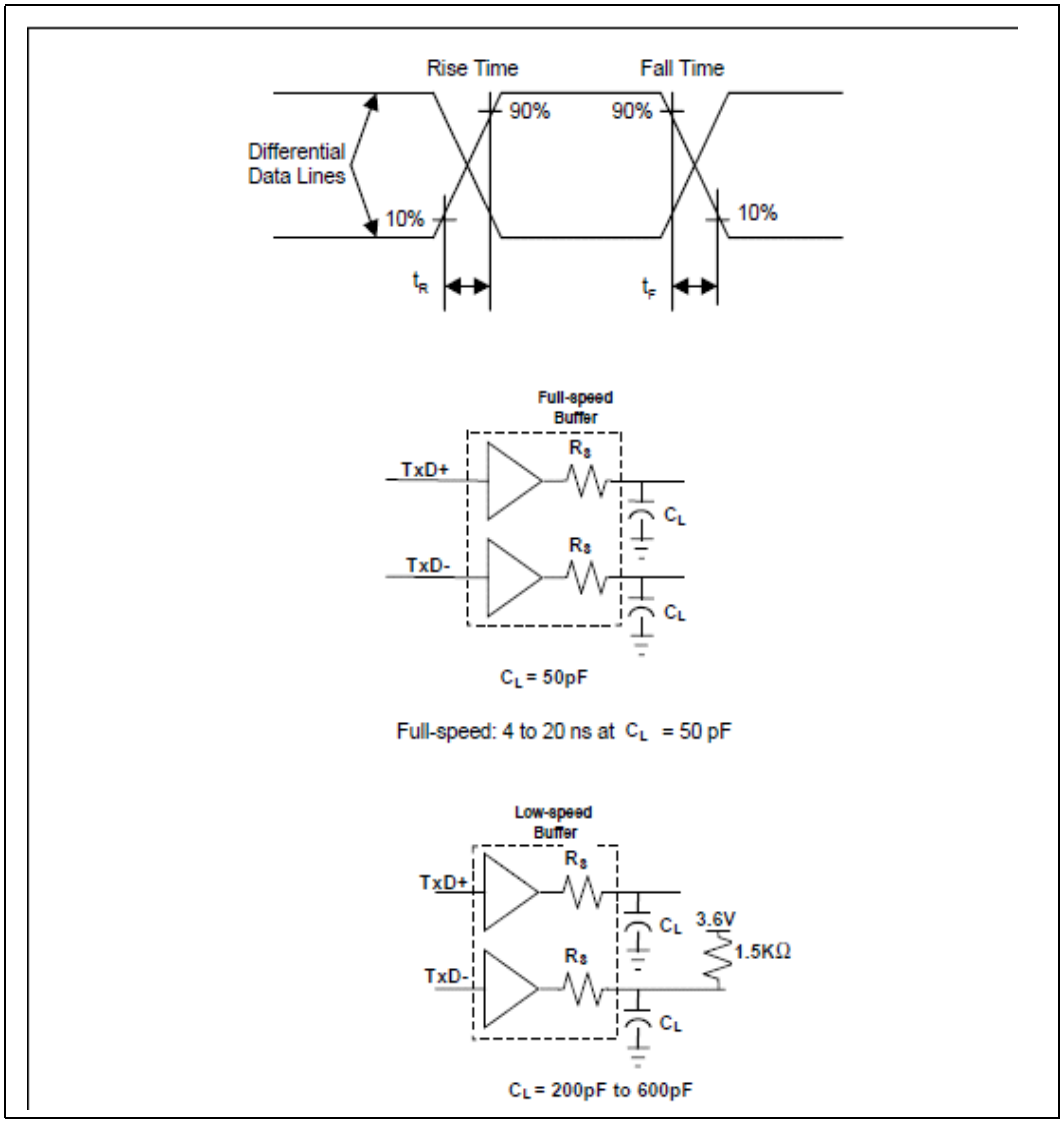


Figure 8-18. USB Jitter

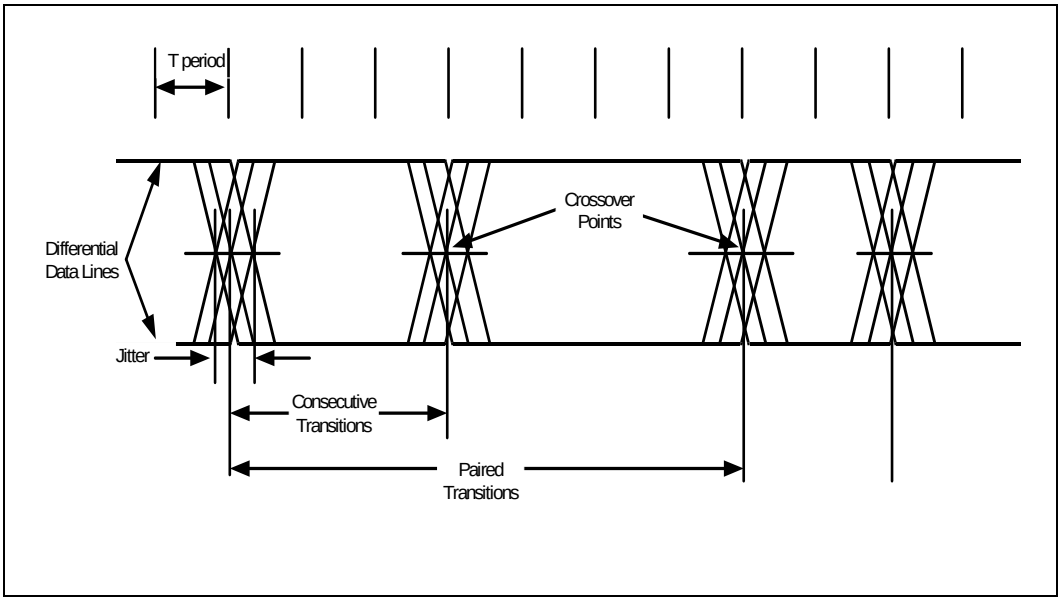


Figure 8-19. USB EOP Width

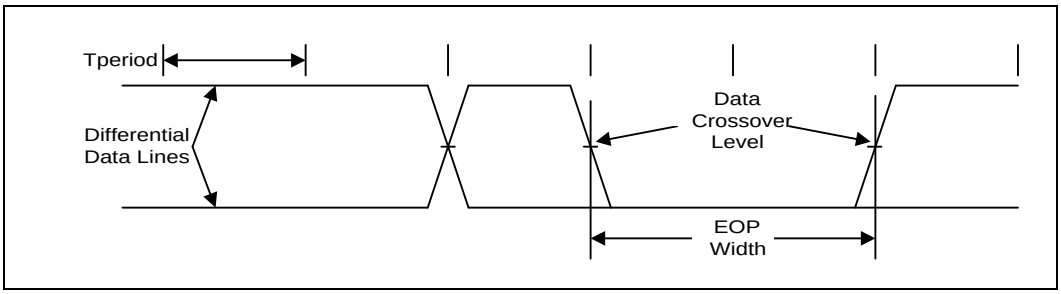
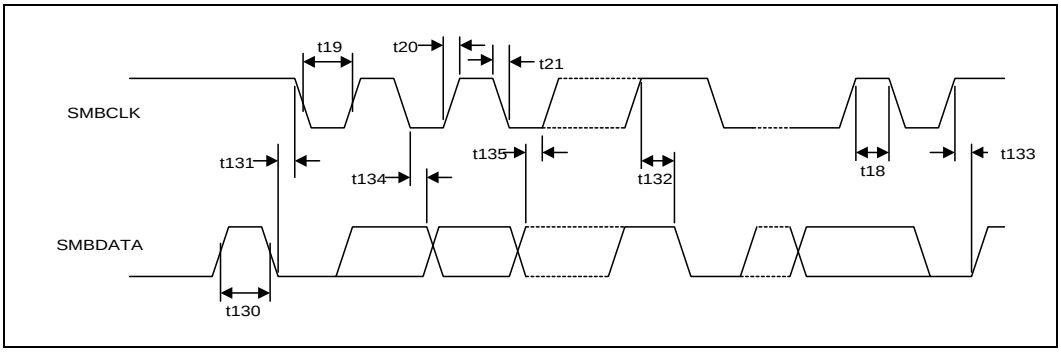
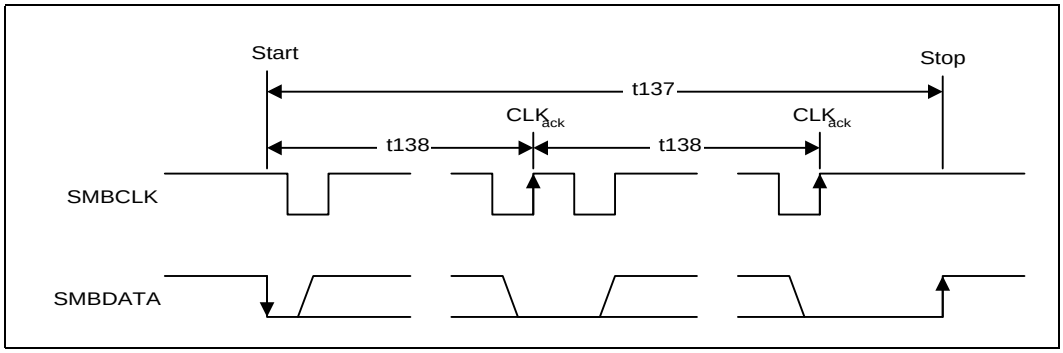


Figure 8-20. SMBus/SMLink Transaction



Note: txx also refers to txx_SM, txxx also refers to txxxSMLFM, SMBCLK also refers to SML[1:0]CLK, and SMBDATA also refers to SML[1:0]DATA in Figure 8-20.

Figure 8-21. SMBus/SMLink Timeout



Note: SMBCLK also refers to SML[1:0]CLK and SMBDATA also refers to SML[1:0]DATA in Figure 8-21.

Figure 8-22. SPI Timings

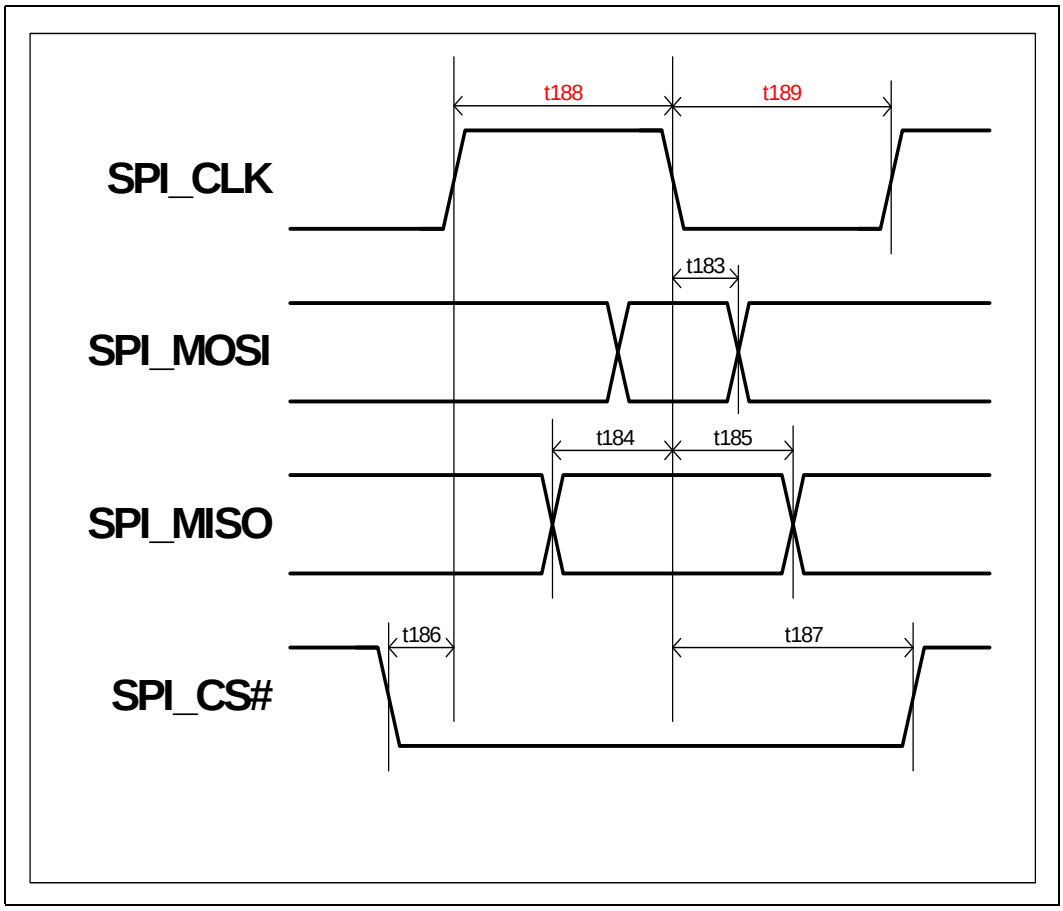


Figure 8-23. Intel® High Definition Audio Input and Output Timings

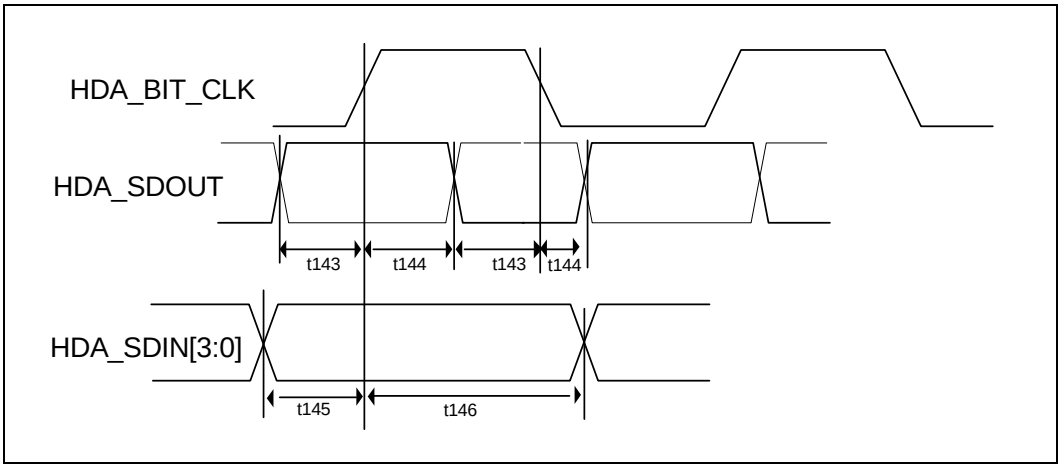


Figure 8-24. Transmitting Position (Data to Strobe)

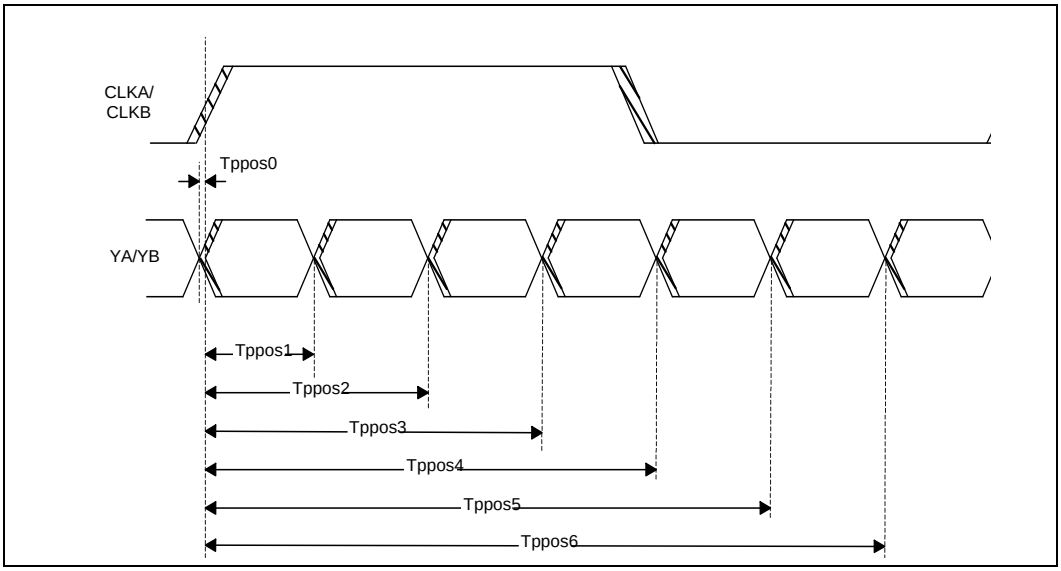


Figure 8-25. PCI Express* Transmitter Eye

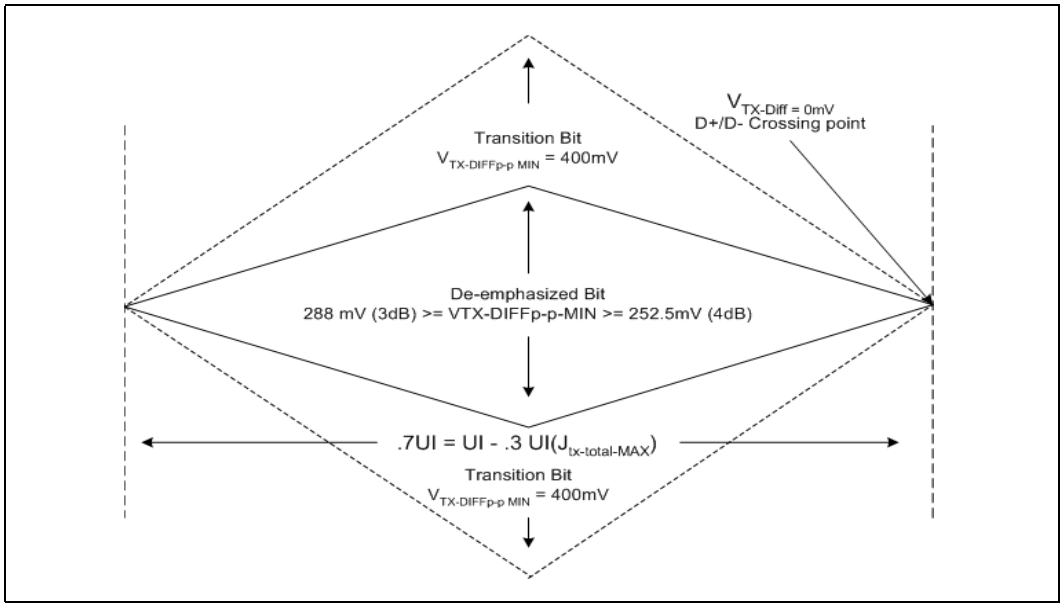


Figure 8-26. PCI Express* Receiver Eye

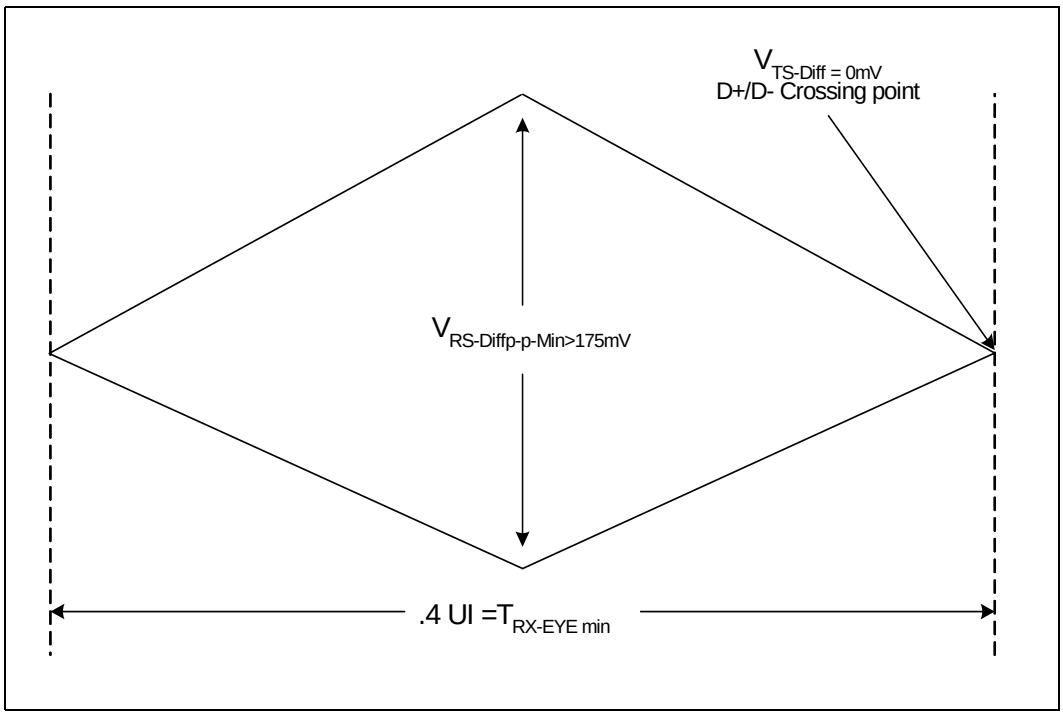


Figure 8-27. Measurement Points for Differential Waveforms.

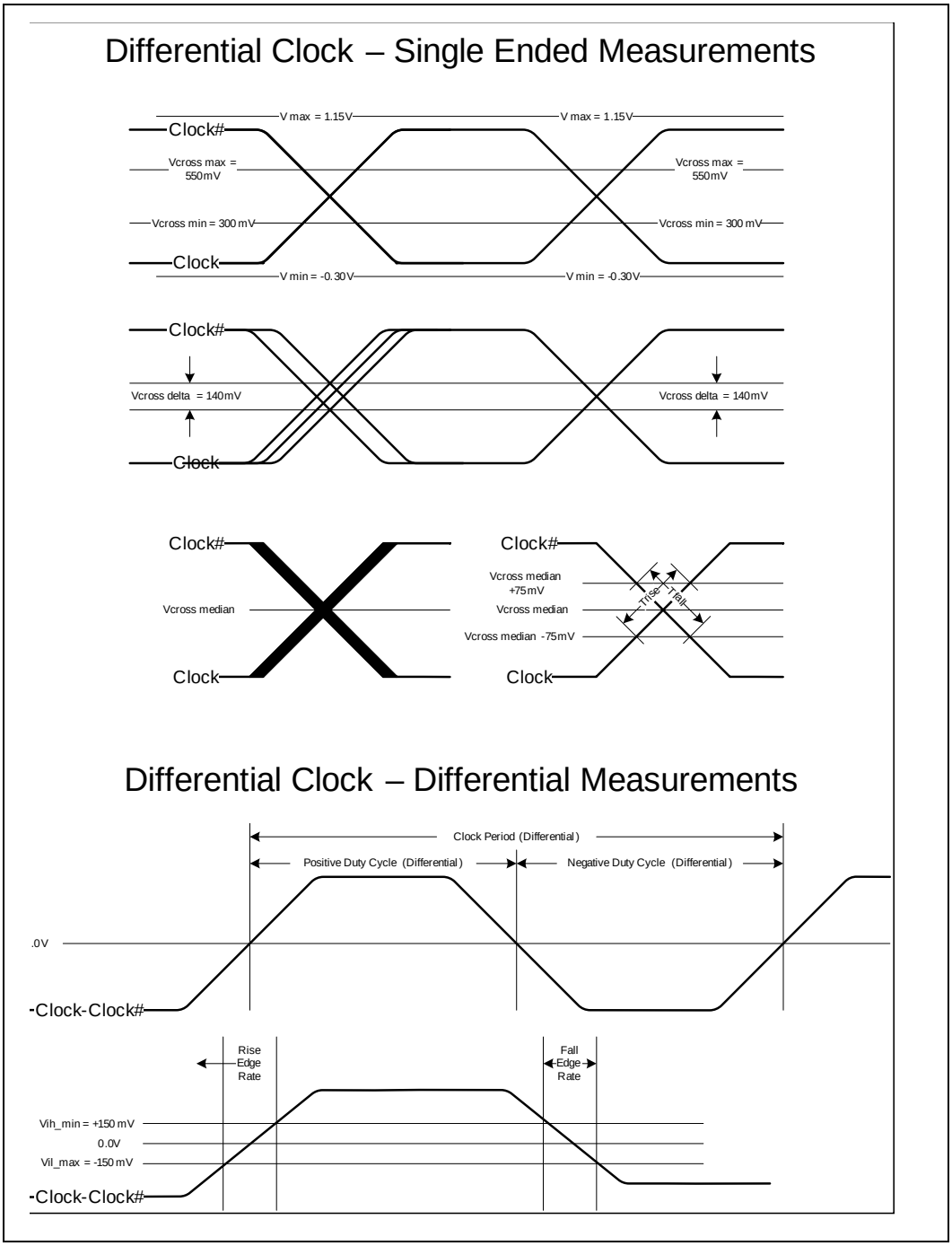
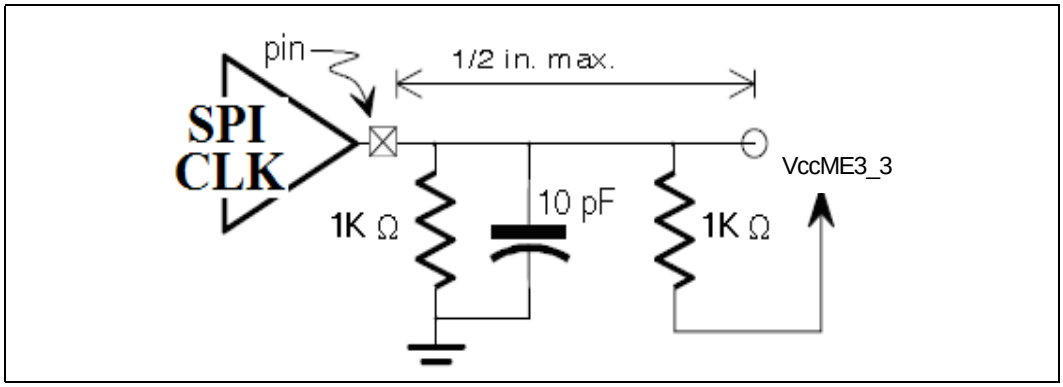


Figure 8-28. PCH Test Load



§

9 Register and Memory Mapping

The PCH contains registers that are located in the processor's I/O space and memory space and sets of PCI configuration registers that are located in PCI configuration space. This chapter describes the PCH I/O and memory maps at the register-set level. Register access is also described. Register-level address maps and Individual register bit descriptions are provided in the following chapters. The following notations and definitions are used in the register/instruction description chapters.

RO	Read Only. In some cases, if a register is read only, writes to this register location have no effect. However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. See the I/O and memory map tables for details.
WO	Write Only. In some cases, if a register is write only, reads to this register location have no effect. However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. See the I/O and memory map tables for details.
R / W	Read/Write. A register with this attribute can be read and written.
R / WC	Read/Write Clear. A register bit with this attribute can be read and written. However, a write of 1 clears (sets to 0) the corresponding bit and a write of 0 has no effect.
R / WL	Read/Write Lockable. A register bit with the attribute can be read at any time but writes may only occur if the associated lock bit is set to unlock. If the associated lock bit is set to lock, this register bit becomes RO unless otherwise indicated.
R / WO	Read/Write-Once. A register bit with this attribute can be written only once after power up. After the first write, the bit becomes read only.
R / WLO	Read/Write, Lock-Once. A register bit with this attribute can be written to the non-locked value multiple times, but to the locked value only once. After the locked value has been written, the bit becomes read only.
R / W / SN	Read/Write register initial value loaded from NVM.
Reserved	The value of reserved bits must never be changed. For details see **Section 9.2**.
Default	When the PCH is reset, it sets its registers to predetermined default states. It is the responsibility of the system initialization software to determine configuration, operating parameters, and optional system features that are applicable, and to program the PCH registers accordingly.
Bold	Register bits that are highlighted in bold text indicate that the bit is implemented in the PCH. Register bits that are not implemented or are hardwired will remain in plain text.

9.1 PCI Devices and Functions

The PCH incorporates a variety of PCI devices and functions, as shown in Table 9-1. The first is the PCI-To-PCI bridge (Device 30). The second device (Device 31) contains most of the standard PCI functions that always existed in the PCI-to-ISA bridges (South Bridges), such as the Intel® 82371AB PIIX4. The third and fourth (Device 29 and Device 26) are the USB and USB2 host controller devices. The fifth (Device 28) is PCI Express device. The sixth (Device 27) is HD Audio controller device. The seventh (Device 25) is the Gigabit Ethernet controller device. The eighth device (Device 22) is the Intel® Management Engine Interface (Intel® MEI).The ninth device (Device 17) is the Virtual Root Port.

If for some reason, the particular system platform does not want to support any one of the Device Functions, with the exception of D30:F0 can individually be disabled. The integrated Gigabit Ethernet controller will be disabled if no Platform LAN Connect component is detected (See Chapter 5.4). When a function is disabled, it does not appear at all to the software. A disabled function will not respond to any register reads or writes, insuring that these devices appear hidden to software.

Note: In the normal platform, M will equal 0. For some HEDT platforms, it may be desirable to have multiple PCH's in the system which means some PCH's may reside on a bus greater than 0.

Table 9-1. PCI Devices and Functions (Sheet 1 of 2)

Bus:Device:Function	Function Description
Bus M:Device 30:Function 0	PCI-to-PCI Bridge
Bus M:Device 31:Function 0	LPC Controller[1]
Bus M:Device 31:Function 2	SATA Controller #1
Bus M:Device 31:Function 3	SMBus Controller
Bus M:Device 31:Function 5	SATA Controller #2[2]
Bus M:Device 31:Function 6	Thermal Subsystem
Bus M:Device 29:Function 0	USB EHCI Controller #1[3]
Bus M:Device 26:Function 0	USB EHCI Controller #2[3]
Bus M:Device 28:Function 0	PCI Express Port 1[4]
Bus M:Device 28:Function 1	PCI Express Port 2[4]
Bus M:Device 28:Function 2	PCI Express Port 3[4]
Bus M:Device 28:Function 3	PCI Express Port 4[4]
Bus M:Device 28:Function 4	PCI Express Port 5[4]
Bus M:Device 28:Function 5	PCI Express Port 6[4]
Bus M:Device 28:Function 6	PCI Express Port 7[4]
Bus M:Device 28:Function 7	PCI Express Port 8[4]
Bus M:Device 27:Function 0	Intel HD Audio Controller
Bus M:Device 25:Function 0	Gigabit Ethernet Controller
Bus M:Device 22:Function 0	Host Embedded Controller Interface #1
Bus M:Device 22:Function 1	Host Embedded Controller Interface #2

Table 9-1. PCI Devices and Functions (Sheet 2 of 2)

Bus:Device:Function	Function Description
Bus M:Device 22:Function 3	KT
Bus X:Device 0:Function 0	SCU 0
Bus X:Device 0:Function 3	SMB 0 (Associate with SCU0)

Notes:
1. The PCI-to-LPC bridge contains registers that control LPC, Power Management, System Management, GPIO, Processor Interface, RTC, Interrupts, Timers, and DMA.
2. SATA controller 2 (D31:F5) is only visible when D31:F2 CC.SCC=01h.
3. Prior to BIOS initialization of the PCH USB subsystem, the EHCI controllers will appear as Function 7. After BIOS initialization, the EHCI controllers will be Function 0.
4. This section assumes the default PCI Express Function Number-to-Root Port mapping is used. Function numbers for a given root port are assignable through the "Root Port Function Number and Hide for PCI Express Root Ports" registers (RCBA+0404h).

Table 9-2. PCI Devices and Functions

Bus:Device:Function	Function Description
Bus M: Device 17: Function 0	PCIe Virtual Root Port

9.2 PCI Configuration Map

Each PCI function on the PCH has a set of PCI configuration registers. The register address map tables for these register sets are included at the beginning of the chapter for the particular function.

Configuration Space registers are accessed through configuration cycles on the PCI bus by the Host bridge using configuration mechanism #1 detailed in the *PCI Local Bus Specification*.

Some of the PCI registers contain reserved bits. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note the software does not need to perform read, merge, write operation for the configuration address register.

In addition to reserved bits within a register, the configuration space contains reserved locations. Software should not write to reserved PCI configuration locations in the device-specific region (above address offset 3Fh).

9.3 I/O Map

The I/O map is divided into Fixed and Variable address ranges. Fixed ranges cannot be moved, but in some cases can be disabled. Variable ranges can be moved and can also be disabled.

9.3.1 Fixed I/O Address Ranges

Table 9-3 shows the Fixed I/O decode ranges from the processor perspective. Note that for each I/O range, there may be separate behavior for reads and writes. DMI (Direct Media Interface) cycles that go to target ranges that are marked as "Reserved" will not be decoded by the PCH, and will be passed to PCI unless the Subtractive Decode Policy bit is set (D31:F0:Offset 42h, bit 0). If a PCI master targets one of the fixed I/O target ranges, it will be positively decoded by the PCH in medium speed.

Address ranges that are not listed or marked "Reserved" are **not** decoded by the PCH (unless assigned to one of the variable ranges).

Table 9-3. Fixed I/O Ranges Decoded by PCH (Sheet 1 of 2)

I/O Address	Read Target	Write Target	Internal Unit
00h–08h	DMA Controller	DMA Controller	DMA
09h–0Eh	RESERVED	DMA Controller	DMA
0Fh	DMA Controller	DMA Controller	DMA
10h–18h	DMA Controller	DMA Controller	DMA
19h–1Eh	RESERVED	DMA Controller	DMA
1Fh	DMA Controller	DMA Controller	DMA
20h–21h	Interrupt Controller	Interrupt Controller	Interrupt
24h–25h	Interrupt Controller	Interrupt Controller	Interrupt
28h–29h	Interrupt Controller	Interrupt Controller	Interrupt
2Ch–2Dh	Interrupt Controller	Interrupt Controller	Interrupt
2E–2F	LPC SIO	LPC SIO	Forwarded to LPC
30h–31h	Interrupt Controller	Interrupt Controller	Interrupt
34h–35h	Interrupt Controller	Interrupt Controller	Interrupt
38h–39h	Interrupt Controller	Interrupt Controller	Interrupt
3Ch–3Dh	Interrupt Controller	Interrupt Controller	Interrupt
40h–42h	Timer/Counter	Timer/Counter	PIT (8254)
43h	RESERVED	Timer/Counter	PIT
4E–4F	LPC SIO	LPC SIO	Forwarded to LPC
50h–52h	Timer/Counter	Timer/Counter	PIT
53h	RESERVED	Timer/Counter	PIT
60h	Microcontroller	Microcontroller	Forwarded to LPC
61h	NMI Controller	NMI Controller	Processor I/F
62h	Microcontroller	Microcontroller	Forwarded to LPC
64h	Microcontroller	Microcontroller	Forwarded to LPC
66h	Microcontroller	Microcontroller	Forwarded to LPC
70h	RESERVED[1]	NMI and RTC Controller	RTC
71h	RTC Controller	RTC Controller	RTC
72h	RTC Controller	NMI and RTC Controller	RTC

Table 9-3. Fixed I/O Ranges Decoded by PCH (Sheet 2 of 2)

I/O Address	Read Target	Write Target	Internal Unit
73h	RTC Controller	RTC Controller	RTC
74h	RTC Controller	NMI and RTC Controller	RTC
75h	RTC Controller	RTC Controller	RTC
76h	RTC Controller	NMI and RTC Controller	RTC
77h	RTC Controller	RTC Controller	RTC
80h	DMA Controller, LPC, PCI, or PCIe	DMA Controller and LPC, PCI, or PCIe	DMA
81h–83h	DMA Controller	DMA Controller	DMA
84h–86h	DMA Controller	DMA Controller and LPC, PCI, or PCIe	DMA
87h	DMA Controller	DMA Controller	DMA
88h	DMA Controller	DMA Controller and LPC or PCI, or PCIe	DMA
89h–8Bh	DMA Controller	DMA Controller	DMA
8Ch–8Eh	DMA Controller	DMA Controller and LPC or PCI, or PCIe	DMA
08Fh	DMA Controller	DMA Controller	DMA
90h–91h	DMA Controller	DMA Controller	DMA
92h	Reset Generator	Reset Generator	Processor I/F
93h–9Fh	DMA Controller	DMA Controller	DMA
A0h–A1h	Interrupt Controller	Interrupt Controller	Interrupt
A4h–A5h	Interrupt Controller	Interrupt Controller	Interrupt
A8h–A9h	Interrupt Controller	Interrupt Controller	Interrupt
ACh–ADh	Interrupt Controller	Interrupt Controller	Interrupt
B0h–B1h	Interrupt Controller	Interrupt Controller	Interrupt
B2h–B3h	Power Management	Power Management	Power Management
B4h–B5h	Interrupt Controller	Interrupt Controller	Interrupt
B8h–B9h	Interrupt Controller	Interrupt Controller	Interrupt
BCh–BDh	Interrupt Controller	Interrupt Controller	Interrupt
C0h–D1h	DMA Controller	DMA Controller	DMA
D2h–DDh	RESERVED	DMA Controller	DMA
DEh–DFh	DMA Controller	DMA Controller	DMA
F0h	FERR# / Interrupt Controller	FERR# / Interrupt Controller	Processor I/F
170h–177h	SATA Controller, PCI, or PCIe	SATA Controller, PCI, or PCIe	Forwarded to SATA
1F0h–1F7h	SATA Controller, PCI, or PCIe	SATA Controller, PCI, or PCIe	Forwarded to SATA
200h-207h	Gameport Low	Gameport Low	Forwarded to LPC
208h-20Fh	Gameport High	Gameport High	Forwarded to LPC
376h	SATA Controller, PCI, or PCIe	SATA Controller, PCI, or PCIe	Forwarded to SATA
3F6h	SATA Controller, PCI, or PCIe	SATA Controller, PCI, or PCIeI	Forwarded to SATA
4D0h–4D1h	Interrupt Controller	Interrupt Controller	Interrupt
CF9h	Reset Generator	Reset Generator	Processor I/F

Note:
1. See Section 13.7.2.

9.3.2 Variable I/O Decode Ranges

Table 9-4 shows the Variable I/O Decode Ranges. They are set using Base Address Registers (BARs) or other configuration bits in the various PCI configuration spaces. The PNP software (PCI or ACPI) can use their configuration mechanisms to set and adjust these values.

Warning: The Variable I/O Ranges should not be set to conflict with the Fixed I/O Ranges. Unpredictable results if the configuration software allows conflicts to occur. The PCH does not perform any checks for conflicts.

Table 9-4. Variable I/O Decode Ranges

Range Name	Mappable	Size (Bytes)	Target
ACPI	Anywhere in 64 KB I/O Space	64	Power Management
IDE Bus Master	Anywhere in 64 KB I/O Space	1. 16 or 32 2. 16	1. SATA Host Controller #1, #2
Native IDE Command	Anywhere in 64 KB I/O Space[1]	8	1. SATA Host Controller #1, #2
Native IDE Control	Anywhere in 64 KB I/O Space[1]	4	1. SATA Host Controller #1, #2
SMBus	Anywhere in 64 KB I/O Space	32	SMB Unit
TCO	96 Bytes above ACPI Base	32	TCO Unit
SATA Index/Data Pair	Anywhere in 64 KB I/O Space	16	SATA Host Controller #1, #2
GPIO	Anywhere in 64 KB I/O Space	128	GPIO Unit
Parallel Port	3 Ranges in 64 KB I/O Space	8[3]	LPC Peripheral
Serial Port 1	8 Ranges in 64 KB I/O Space	8	LPC Peripheral
Serial Port 2	8 Ranges in 64 KB I/O Space	8	LPC Peripheral
Floppy Disk Controller	2 Ranges in 64 KB I/O Space	8	LPC Peripheral
LAN	Anywhere in 64 KB I/O Space	32[2]	LAN Unit
LPC Generic 1	Anywhere in 64 KB I/O Space	4 to 256	LPC Peripheral
LPC Generic 2	Anywhere in 64 KB I/O Space	4 to 256	LPC Peripheral
LPC Generic 3	Anywhere in 64 KB I/O Space	4 to 256	LPC Peripheral
LPC Generic 4	Anywhere in 64 KB I/O Space	4 to 256	LPC Peripheral
I/O Trapping Ranges	Anywhere in 64 KB I/O Space	1 to 256	Trap on Backbone
PCI Bridge	Anywhere in 64 KB I/O Space	I/O Base/ Limit	PCI Bridge
PCI Express Root Ports	Anywhere in 64 KB I/O Space	I/O Base/ Limit	PCI Express Root Ports 1-8
KT	Anywhere in 64 KB I/O Space	8	KT

Notes:
1. All ranges are decoded directly from DMI. The I/O cycles will not be seen on PCI, except the range associated with PCI bridge.
2. The LAN range is typically not used, as the registers can also be accessed using a memory space.
3. There is also an alias 400h above the parallel port range that is used for ECP parallel ports.

9.4 Memory Map

Table 9-5 shows (from the processor perspective) the memory ranges that the PCH decodes. Cycles that arrive from DMI that are not directed to any of the internal memory targets that decode directly from DMI will be driven out on PCI unless the Subtractive Decode Policy bit is set (D31:F0:Offset 42h, bit 0).

PCI cycles generated by external PCI masters will be positively decoded unless they fall in the PCI-to-PCI bridge memory forwarding ranges (those addresses are reserved for PCI peer-to-peer traffic). If the cycle is not in the internal LAN controller's range, it will be forwarded up to DMI. Software must not attempt locks to the PCH's memory-mapped I/O ranges for EHCI and HPET. If attempted, the lock is not honored which means potential deadlock conditions may occur.

Table 9-5. Memory Decode Ranges from Processor Perspective (Sheet 1 of 2)

Memory Range	Target	Dependency/Comments
0000 0000h–000D FFFFh 0010 0000h–TOM (Top of Memory)	Main Memory	TOM registers in Host controller
000E 0000h–000E FFFFh	LPC or SPI	Bit 6 in BIOS Decode Enable register is set
000F 0000h–000F FFFFh	LPC or SPI	Bit 7 in BIOS Decode Enable register is set
FEC_ _000h–FEC_ _040h	IO(x) APIC inside PCH	_ _is controlled using APIC Range Select (ASEL) field and APIC Enable (AEN) bit
FEC1 0000h–FEC1 7FFF	PCI Express Port 1	PCI Express Root Port 1 I/OxAPIC Enable (PAE) set
FEC1 8000h–FEC1 FFFFh	PCI Express Port 2	PCI Express Root Port 2 I/OxAPIC Enable (PAE) set
FEC2 0000h–FEC2 7FFFh	PCI Express Port 3	PCI Express Root Port 3 I/OxAPIC Enable (PAE) set
FEC2 8000h–FEC2 FFFFh	PCI Express Port 4	PCI Express Root Port 4 I/OxAPIC Enable (PAE) set
FEC3 0000h–FEC3 7FFFh	PCI Express Port 5	PCI Express Root Port 5 I/OxAPIC Enable (PAE) set
FEC3 8000h–FEC3 FFFFh	PCI Express Port 6	PCI Express Root Port 6 I/OxAPIC Enable (PAE) set
FEC4 0000 - FEC4 7FFF	PCI Express Port 7	PCI Express Root Port 7I/OxAPIC Enable (PAE) set
FEC4 8000 - FEC4 FFFF	PCI Express Port 8	PCI Express Root Port 8I/OxAPIC Enable (PAE) set
FED4 0000h–FED4 BFFFh	TPM on LPC	If Intel TPM is enabled, FED4_0000h – FED4_7FFFh goes to Intel TPM. If disabled, the entire range goes to LPC.
FFC0 0000h–FFC7 FFFFh FF80 0000h–FF87 FFFFh	LPC or SPI (or PCI)[2]	Bit 8 in BIOS Decode Enable register is set
FFC8 0000h–FFCF FFFFh FF88 0000h–FF8F FFFFh	LPC or SPI (or PCI)[2]	Bit 9 in BIOS Decode Enable register is set
FFD0 0000h–FFD7 FFFFh FF90 0000h–FF97 FFFFh	LPC or SPI (or PCI)[2]	Bit 10 in BIOS Decode Enable register is set
FFD8 0000h–FFDF FFFFh FF98 0000h–FF9F FFFFh	LPC or SPI (or PCI)[2]	Bit 11 in BIOS Decode Enable register is set
FFE0 000h–FFE7 FFFFh FFA0 0000h–FFA7 FFFFh	LPC or SPI (or PCI)[2]	Bit 12 in BIOS Decode Enable register is set
FFE8 0000h–FFEF FFFFh FFA8 0000h–FFAF FFFFh	LPC or SPI (or PCI)[3]	Bit 13 in BIOS Decode Enable register is set
FFF0 0000h–FFF7 FFFFh FFB0 0000h–FFB7 FFFFh	LPC or SPI (or PCI)[2]	Bit 14 in BIOS Decode Enable register is set
FFF8 0000h–FFFF FFFFh FFB8 0000h–FFBF FFFFh	LPC or SPI (or PCI)[2]	Always enabled. The top two, 64 KB blocks of this range can be swapped, as described in Section 9.4.1.
FF70 0000h–FF7F FFFFh FF30 0000h–FF3F FFFFh	LPC or SPI (or PCI)[2]	Bit 3 in BIOS Decode Enable register is set
FF60 0000h–FF6F FFFFh FF20 0000h–FF2F FFFFh	LPC or SPI (or PCI)[2]	Bit 2 in BIOS Decode Enable register is set

Table 9-5. Memory Decode Ranges from Processor Perspective (Sheet 2 of 2)

Memory Range	Target	Dependency/Comments
FF50 0000h–FF5F FFFFh FF10 0000h–FF1F FFFFh	LPC or SPI (or PCI)[2]	Bit 1 in BIOS Decode Enable register is set
FF40 0000h–FF4F FFFFh FF00 0000h–FF0F FFFFh	LPC or SPI (or PCI)[2]	Bit 0 in BIOS Decode Enable register is set
128 KB anywhere in 4-GB range	Integrated LAN Controller	Enable using BAR in Device 25:Function 0 (Integrated LAN Controller MBARA)
4 KB anywhere in 4 GB range	Integrated LAN Controller	Enable using BAR in Device 25:Function 0 (Integrated LAN Controller MBARB)
1 KB anywhere in 4-GB range	USB EHCI Controller #1[1]	Enable using standard PCI mechanism (Device 29, Function 0)
1 KB anywhere in 4-GB range	USB EHCI Controller #2[1]	Enable using standard PCI mechanism (Device 26, Function 0)
FED4 0000h–FED4 FFFFh	TPM on LPC	None
Memory Base/Limit anywhere in 4 GB range	PCI Bridge	Enable using standard PCI mechanism (Device 30: Function 0)
Prefetchable Memory Base/Limit anywhere in 64-bit address range	PCI Bridge	Enable using standard PCI mechanism (Device 30: Function 0)
64 KB anywhere in 4 GB range	LPC	LPC Generic Memory Range. Enable using setting bit[0] of the LPC Generic Memory Range register (D31:F0:offset 98h).
32 Bytes anywhere in 64-bit address range	SMBus	Enable using standard PCI mechanism (Device 31: Function 3)
2 KB anywhere above 64 KB to 4 GB range	SATA Host Controller #1	AHCI memory-mapped registers. Enable using standard PCI mechanism (Device 31: Function 2)
Memory Base/Limit anywhere in 4 GB range	PCI Express Root Ports 1-8	Enable using standard PCI mechanism (Device 28: Function 0-7)
Prefetchable Memory Base/Limit anywhere in 64-bit address range	PCI Express Root Ports 1-8	Enable using standard PCI mechanism (Device 28: Function 0-7)
4 KB anywhere in 64-bit address range	Thermal Reporting	Enable using standard PCI mechanism (Device 31: Function 6 TBAR/TBARH)
4 KB anywhere in 64-bit address range	Thermal Reporting	Enable using standard PCI mechanism (Device 31: Function 6 TBARB/TBARBH)
16 Bytes anywhere in 64-bit address range	Intel® Management Engine Interface (Intel® MEI) #1, #2	Enable using standard PCI mechanism (Device 22: Function 1:0)
4 KB anywhere in 4 GB range	KT	Enable using standard PCI mechanism (Device 22: Function 3)
16 KB anywhere in 4 GB range	Root Complex Register Block (RCRB)	Enable using setting bit[0] of the Root Complex Base Address register (D31:F0:offset F0h).
512 B anywhere in 64-bit addressing space	Intel HD Audio Host Controller	Enable using standard PCI mechanism (Device 27, Function 0)
FED0 X000h–FED0 X3FFh	High Precision Event Timers [1]	BIOS determines the "fixed" location which is one of four, 1-KB ranges where X (in the first column) is 0h, 1h, 2h, or 3h.
All other	PCI	None

Notes:

1. Software must not attempt locks to memory mapped I/O ranges for USB EHCI or High Precision Event Timers. If attempted, the lock is not honored, which means potential deadlock conditions may occur.
2. PCI is the target when the Boot BIOS Destination selection bits are set to 10b (Chipset Config Registers:Offset 3401 bits 11:10). When PCI selected, the Firmware Hub Decode Enable bits have no effect.

9.4.1 Boot-Block Update Scheme

The PCH supports a "top-block swap" mode that has the PCH swap the top block in the FWH or SPI flash (the boot block) with another location. This allows for safe update of the Boot Block (even if a power failure occurs). When the "TOP_SWAP" Enable bit is set, the PCH will invert A16 for cycles going to the upper two 64 KB blocks in the FWH or appropriate address lines as selected in Boot Block Size (BIOS Boot-Block size) soft strap for SPI.

Specifically for FHW, in this mode accesses to FFFF_0000h-FFFF_FFFFh are directed to FFFE_0000h-FFFE_FFFFh and vice versa. When the Top Swap Enable bit is 0, the PCH will not invert A16.

Specifically for SPI, in this mode the "Top-Block Swap" behavior is as described below. When the Top Swap Enable bit is 0, the PCH will not invert any address bit.

Table 9-6. SPI Mode Address Swapping

BIOS Boot-Block size Value	Accesses to	Being Directed to
000 (64 KB)	FFFF_0000h–FFFF_FFFFh	FFFE_0000h–FFFE_FFFFh and vice versa
001 (128 KB)	FFFE_0000h–FFFF_FFFFh	FFFC_0000h–FFFD_FFFFh and vice versa
010 (256 KB)	FFFC_0000h–FFFF_FFFFh	FFF8_0000h–FFFB_FFFFh and vice versa
011 (512 KB)	FFF8_0000h–FFFF_FFFFh	FFF0_0000h–FFF7_FFFFh and vice versa
100 (1 MB)	FFF0_0000h–FFFF_FFFFh	FFE0_0000h–FFEF_FFFFh and vice versa
101 - 111	Reserved	Reserved

This bit is automatically set to 0 by RTCRST#, but not by PLTRST#.

The scheme is based on the concept that the top block is reserved as the "boot" block, and the block immediately below the top block is reserved for doing boot-block updates.

The algorithm is:

1. Software copies the top block to the block immediately below the top.
2. Software checks that the copied block is correct. This could be done by performing a checksum calculation.
3. Software sets the TOP_SWAP bit. This will invert the appropriate address bits for the cycles going to the FWH or SPI.
4. Software erases the top block.
5. Software writes the new top block.
6. Software checks the new top block.
7. Software clears the TOP_SWAP bit.
8. Software sets the Top_Swap Lock-Down bit.

If a power failure occurs at any point after step 3, the system will be able to boot from the copy of the boot block that is stored in the block below the top. This is because the TOP_SWAP bit is backed in the RTC well.

Note: The top-block swap mode may be forced by an external strapping option (See Section §). When top-block swap mode is forced in this manner, the TOP_SWAP bit cannot be cleared by software. A re-boot with the strap removed will be required to exit a forced top-block swap mode.

Note: Top-block swap mode only affects accesses to the Firmware Hub space, not feature space for FWH.

Note: The top-block swap mode has no effect on accesses below FFFE_0000h for FWH.

§

10 Chipset Configuration Registers

This section describes all registers and base functionality that is related to chipset configuration and not a specific interface (such as LPC, PCI, or PCI Express*). It contains the root complex register block, which describes the behavior of the upstream internal link.

This block is mapped into memory space, using the Root Complex Base Address (RCBA) register of the PCI-to-LPC bridge. Accesses in this space must be limited to 32-(DW) bit quantities. Burst accesses are not allowed.

All chipset configuration registers are located in the core well unless otherwise indicated.

10.1 Chipset Configuration Registers (Memory Space)

Note: Address locations that are not shown should be treated as Reserved (see Section 9.2 for details).

Table 10-1. Chipset Configuration Register Memory Map (Memory Space) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Type
0050–0053h	CIR0	Chipset Initialization Register 0	00000000h	R/WL
0400–0403h	RPC	Root Port Configuration	0000000yh	R/W, RO
0404–0407h	RPFN	Root Port Function Number for PCI Express Root Ports	76543210h	R/WO, RO
0408–040Bh	FLRSTAT	Function Level Reset Pending Status Summary	00000000h	RO
1E00–1E03h	TRSR	Trap Status Register	00000000h	R/WC, RO
1E10–1E17h	TRCR	Trapped Cycle Register	0000000000000000h	RO
1E18–1E1Fh	TWDR	Trapped Write Data Register	0000000000000000h	RO
1E80–1E87h	IOTR0	I/O Trap Register 0	0000000000000000h	R/W
1E88–1E8Fh	IOTR1	I/O Trap Register 1	0000000000000000h	R/W
1E90–1E97h	IOTR2	I/O Trap Register 2	0000000000000000h	R/W
1E98–1E9Fh	IOTR3	I/O Trap Register 3	0000000000000000h	R/W
2014–2017h	V0CTL	VC 0 Resource Control	800000FFh	R/WL, RO
201A–201Bh	V0STS	VC 0 Resource Status	0000h	RO
2020–2023h	V1CTL	VC 1 Resource Control	00000000h	R/W, RO, R/WL
2026–2027h	V1STS	VC 1 Resource Status	0000h	RO
20AC–20AFh	REC	Root Error Command	0000h	R/W
21A4–21A7h	LCAP	Link Capabilities	00012C42h	RO, R/WO
21A8–21A9h	LCTL	Link Control	0000h	R/W
21AA–21ABh	LSTS	Link Status	0042h	RO
21B0–21B1h	DLCTL2	DMI Link Control 2	0000h	R/W, RO
2234–2237h	DMIC	DMI Control	00000000h	R/W, RO
2238–223Bh	CIR30	Chipset Initialization Register 30	00000900h	R/W
3000–3000h	TCTL	TCO Control	00h	R/W

Table 10-1. Chipset Configuration Register Memory Map (Memory Space) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Type
3100–3103h	D31IP	Device 31 Interrupt Pin	03243200h	R/W, RO
3104–3107h	D30IP	Device 30 Interrupt Pin	00000000h	RO
3108–310Bh	D29IP	Device 29 Interrupt Pin	10004321h	R/W
310C–310Fh	D28IP	Device 28 Interrupt Pin	00214321h	R/W
3110–3113h	D27IP	Device 27 Interrupt Pin	00000001h	R/W
3114–3117h	D26IP	Device 26 Interrupt Pin	30000321h	R/W
3118–311Bh	D25IP	Device 25 Interrupt Pin	00000001h	R/W
311C–311Fh	D24IP	Device 24 Interrupt Pin	00000001h	R/W
3124–3127h	D22IP	Device 22 Interrupt Pin	00000001h	R/W
3140–3141h	D31IR	Device 31 Interrupt Route	3210h	R/W
3144–3145h	D29IR	Device 29 Interrupt Route	3210h	R/W
3146–3147h	D28IR	Device 28 Interrupt Route	3210h	R/W
3148–3149h	D27IR	Device 27 Interrupt Route	3210h	R/W
314C–314Fh	D26IR	Device 26 Interrupt Route	3210h	R/W
3150–3153h	D25IR	Device 25 Interrupt Route	3210h	R/W
3154–3157h	D24IR	Device 24 Interrupt Route	3210h	R/W
315C–316Fh	D22IR	Device 22 Interrupt Route	3210h	R/W
31FE–31FFh	OIC	Other Interrupt Control	0000h	R/W
3310–3313h	PRSTS	Power and Reset Status	03000000h	RO, R/WC
3318–331Bh	PM_CFG	Power Management Configuration	00000000h	R/W
332C–332Fh	DEEP_S4_POL	Deep S4 Power Policies	00000000h	R/W
3330–3333h	DEEP_S5_POL	Deep S5 Power Policies	00000000h	R/W
3400–3403h	RC	RTC Configuration	00000000h	R/W, R/WLO
3404–3407h	HPTC	High Precision Timer Configuration	00000000h	R/W
3410–3413h	GCS	General Control and Status	000000yy0h	R/W, R/WLO
3414–3414h	BUC	Backed Up Control	00h	R/W
3418–341Bh	FD	Function Disable	00000000h	R/W
341C–341Fh	CG	Clock Gating	00000000h	R/W
3420–3420h	FDSW	Function Disable SUS Well	00h	R/W
3428–342Bh	FD2	Function Disable 2	00000000h	R/W
3450–3453h	GSXBAR	GPIO Serial Expander Base Address	00000000h	R/W, RO
3454–3457h	GSXCTRL	GPIO Serial Expander Control Register	0000000h	R/W, RO
3500–3537h	USBIR[13:0]	USB Initialization Registers[13:0]	20000B4Ah	R/W
3590–3593h	MISCCTL	Miscellaneous Control Register	00000000h	R/W
35A0–35A3h	USBOCM1	USB Overcurrent MAP Register 1	00000000h	R/WO
35A4–35A7h	USBOCM2	USB Overcurrent MAP Register 2	00000000h	R/WO
35B0–35B3h	RMHWKCTL	USB Remap Control	00000000h	R/WO

10.1.1 CIR0—Chipset Initialization Register 0

Offset Address: 0050–0053h Attribute: R/WL
Default Value: 00000000h Size: 32-bit

Bit	Description
31	**TC Lock-Down (TCLOCKDN)**—R/WL. When set to 1, certain DMI configuration registers are locked down by this and cannot be written. Once set to 1, this bit can only be cleared by a PLTRST#.
30:0	**CIR0 Field 0**—R/WL. BIOS must set this field. Bits locked by TCLOCKDN.

10.1.2 RPC—Root Port Configuration Register

Offset Address: 0400–0403h Attribute: R/W, RO
Default Value: 0000000yh (y = 00xxb) Size: 32-bit

Bit	Description
31:12	Reserved
11	**GbE Over PCIe Root Port Enable (GBEPCIERPEN)—**R/W. '0': GbE MAC/PHY communication is not enabled over PCI Express. '1': The PCI Express port selected by the GBEPCIEPORTSEL register will be used for GbE MAC/PHY over PCI Express communication The default value for this register is set by the GBE_PCIE_EN soft strap. ***Note:*** GbE and PCIe will use the output of this register and not the soft strap.
10:8	**GbE Over PCIe Root Port Select (GBEPCIERPSEL)—**R/W. If the GBEPCIERPEN is a '1', then this register determines which port is used for GbE MAC/PHY communication over PCI Express. This register is set by soft strap and is writable to support separate PHY on motherboard and docking station. 111 = Port 8 (Lane 7) 110 = Port 7 (Lane 6) 101 = Port 6 (Lane 5) 100 = Port 5 (Lane 4) 011 = Port 4 (Lane 3) 010 = Port 3 (Lane 2) 001 = Port 2 (Lane 1) 000 = Port 1 (Lane 0) The default value for this register is set by the GBE_PCIEPORTSEL[2:0] soft strap. ***Note:*** GbE and PCIe will use the output of this register and not the soft strap.
7:4	**Reserved**
3:2	**Port Configuration2 (PC2)**—RO. This controls how the PCI bridges are organized in various modes of operation for Ports 5–8. For the following mappings, if a port is not shown, it is considered a x1 port with no connection. This bit is set by the PCIEPCS2[1:0] soft strap. 11 = 1 x4, Port 5(x4) 10 = 2x2, Port 5 (x2) Port 7 (x7) 01 = 1x2 and 2x1s, Port 5 (x2), Port 7(x1) and Port 8(x1) 00 = 4 x1s, Port 5(x1), Port 6(x1), Port 7(x1) and Port 8(x1)
1:0	**Port Configuration (PC)**—RO. This controls how the PCI bridges are organized in various modes of operation for Ports 1–4. For the following mappings, if a port is not shown, it is considered a x1 port with no connection. These bits are set by the PCIEPCS1[1:0] soft strap. 11 = 1 x4, Port 1 (x4) 10 = 2x2, Port 1 (x2, Port 3 (x2) 01 = 1x2 and 2x1s, Port 1 (x2), Port 3 (x1) and Port 4 (x1) 00 = 4 x1s, Port 1 (x1), Port 2 (x1), Port 3 (x1) and Port 4 (x1)

10.1.3 RPFN—Root Port Function Number and Hide for PCI Express* Root Ports

Offset Address:	0404–0407h	Attribute:	R/WO, RO
Default Value:	76543210h	Size:	32-bit

For the PCI Express root ports, the assignment of a function number to a root port is not fixed. BIOS may re-assign the function numbers on a port by port basis. This capability will allow BIOS to disable/hide any root port and still have functions 0 through N-1 where N is the total number of enabled root ports.

Port numbers will remain fixed to a physical root port.

The existing root port Function Disable registers operate on physical ports (not functions).

Port Configuration (1x4, 4x1, and so forth) is not affected by the logical function number assignment and is associated with physical ports.

Bit	Description
31	**Root Port 8 Config Hide (RP8CH)—**R/W. This bit is used to hide the root port and any devices behind it from being discovered by the operating system. When set to '1' the root port will not claim any downstream configuration transactions.
30:28	**Root Port 8 Function Number (RP8FN)**—R/WO. These bits set the function number for PCI Express Root Port 8. This root port function number must be a unique value from the other root port function numbers
27	**Root Port 7 Config Hide (RP7CH)**—R/W. This bit is used to hide the root port and any devices behind it from being discovered by the operating system. When set to '1' the root port will not claim any downstream configuration transactions.
26:24	**Root Port 7 Function Number (RP7FN)**—R/WO. These bits set the function number for PCI Express Root Port 7. This root port function number must be a unique value from the other root port function numbers
23	**Root Port 6 Config Hide (RP6CH)—**R/W. This bit is used to hide the root port and any devices behind it from being discovered by the operating system. When set to '1' the root port will not claim any downstream configuration transactions.
22:20	**Root Port 6 Function Number (RP6FN)**—R/WO. These bits set the function number for PCI Express Root Port 6. This root port function number must be a unique value from the other root port function numbers
19	**Root Port 5 Config Hide (RP5CH)**—R/W. This bit is used to hide the root port and any devices behind it from being discovered by the operating system. When set to '1' the root port will not claim any downstream configuration transactions.
18:16	**Root Port 5 Function Number (RP5FN)**—R/WO. These bits set the function number for PCI Express Root Port 5. This root port function number must be a unique value from the other root port function numbers
15	**Root Port 4 Config Hide (RP4CH)**—R/W. This bit is used to hide the root port and any devices behind it from being discovered by the operating system. When set to '1' the root port will not claim any downstream configuration transactions.
14:12	**Root Port 4 Function Number (RP4FN)**—R/WO. These bits set the function number for PCI Express Root Port 4. This root port function number must be a unique value from the other root port function numbers
11	**Root Port 3 Config Hide (RP3CH)**—R/W. This bit is used to hide the root port and any devices behind it from being discovered by the operating system. When set to '1' the root port will not claim any downstream configuration transactions.
10:8	**Root Port 3 Function Number (RP3FN)**—R/WO. These bits set the function number for PCI Express Root Port 3. This root port function number must be a unique value from the other root port function numbers
7	**Root Port 2 Config Hide (RP2CH)**—R/W. This bit is used to hide the root port and any devices behind it from being discovered by the operating system. When set to '1' the root port will not claim any downstream configuration transactions.

Bit	Description
6:4	**Root Port 2 Function Number (RP2FN)**—R/WO. These bits set the function number for PCI Express Root Port 2. This root port function number must be a unique value from the other root port function numbers
3	**Root Port 1 Config Hide (RP1CH)**—R/W. This bit is used to hide the root port and any devices behind it from being discovered by the operating system. When set to '1' the root port will not claim any downstream configuration transactions.
2:0	**Root Port 1 Function Number (RP1FN)**—R/WO. These bits set the function number for PCI Express Root Port 1. This root port function number must be a unique value from the other root port function numbers

10.1.4 FLRSTAT—FLR Pending Status Register

Offset Address: 0408–040Bh Attribute: RO
Default Value: 00000000h Size: 32-bit

Bit	Description
31:17	Reserved.
16	**FLR Pending Status for D29:F0, EHCI #1**—R0. 0 = Function Level Reset is not pending. 1 = Function Level Reset is pending.
15	**FLR Pending Status for D26:F0, EHCI #2**—R0. 0 = Function Level Reset is not pending. 1 = Function Level Reset is pending.
10:9	Reserved
8	**FLR Pending Status for D26:F0, EHCI#2**—R0. 0 = Function Level Reset is not pending. 1 = Function Level Reset is pending.
7:0	Reserved.

10.1.5 TRSR—Trap Status Register

Offset Address: 1E00–1E03h Attribute: R/WC, RO
Default Value: 00000000h Size: 32-bit

Bit	Description
31:4	Reserved
3:0	**Cycle Trap SMI# Status (CTSS)**—R/WC. These bits are set by hardware when the corresponding Cycle Trap register is enabled and a matching cycle is received (and trapped). These bits are OR'ed together to create a single status bit in the Power Management register space. Note that the SMI# and trapping must be enabled in order to set these bits. These bits are set before the completion is generated for the trapped cycle, thereby ensuring that the processor can enter the SMI# handler when the instruction completes. Each status bit is cleared by writing a 1 to the corresponding bit location in this register.

10.1.6 TRCR—Trapped Cycle Register

Offset Address: 1E10–1E17h Attribute: RO
Default Value: 0000000000000000h Size: 64-bit

This register saves information about the I/O Cycle that was trapped and generated the SMI# for software to read.

Bit	Description
63:25	Reserved
24	**Read/Write# (RWI)**—RO. Trapped cycle was a write cycle. Trapped cycle was a read cycle.
23:20	Reserved
19:16	**Active-high Byte Enables (AHBE)**—RO. This is the DWord-aligned byte enables associated with the trapped cycle. A 1 in any bit location indicates that the corresponding byte is enabled in the cycle.
15:2	**Trapped I/O Address (TIOA)**—RO. This is the DWord-aligned address of the trapped cycle.
1:0	Reserved

10.1.7 TWDR—Trapped Write Data Register

Offset Address: 1E18–1E1Fh Attribute: RO
Default Value: 0000000000000000h Size: 64-bit

This register saves the data from I/O write cycles that are trapped for software to read.

Bit	Description
63:32	Reserved
31:0	**Trapped I/O Data (TIOD)**—RO. DWord of I/O write data. This field is undefined after trapping a read cycle.

10.1.8 IOTRn—I/O Trap Register (0–3)

Offset Address:	1E80–1E87h Register 0 1E88–1E8Fh Register 1 1E90–1E97h Register 2 1E98–1E9Fh Register 3	Attribute:	R/W
Default Value:	0000000000000000h	Size:	64-bit

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Bit	Description
63:50	Reserved
49	**Read/Write Mask (RWM)**—R/W. The cycle must match the type specified in bit 48. Trapping logic will operate on both read and write cycles.
48	**Read/Write# (RWIO)**—R/W. 0 = Write 1 = Read ***Note:*** The value in this field does not matter if bit 49 is set.
47:40	Reserved
39:36	**Byte Enable Mask (BEM)**—R/W. A 1 in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
35:32	**Byte Enables (TBE)**—R/W. Active-high DWord-aligned byte enables.
31:24	Reserved
23:18	**Address[7:2] Mask (ADMA)**—R/W. A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	Reserved
15:2	**I/O Address[15:2] (IOAD)**—R/W. DWord-aligned address
1	Reserved
0	**Trap and SMI# Enable (TRSE)**—R/W. 0 = Trapping and SMI# logic disabled. 1 = The trapping logic specified in this register is enabled.

10.1.9 V0CTL—Virtual Channel 0 Resource Control Register

Offset Address: 2014–2017h Attribute: R/WL, RO
Default Value: 80000011h Size: 32-bit

Bit	Description
31	**Virtual Channel Enable (EN)—**RO. Always set to 1. VC0 is always enabled and cannot be disabled.
30:27	Reserved
26:24	**Virtual Channel Identifier (ID)**—RO. Indicates the ID to use for this virtual channel.
23:16	Reserved
15:10	**Extended TC/VC Map (ETVM):** R/WL. Defines the upper 8-bits of the VC0 16-bit TC/VC mapping registers. These registers use the PCI Express reserved TC[3] traffic class bit. These bits are locked if the TCLOCKDN bit (RCBA+0050h:bit 31) is set.
9:7	**Reserved**
6:1	**Transaction Class / Virtual Channel Map (TVM)**—R/WL. Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel.hese bits are locked if the TCLOCKDN bit (RCBA+0050h:bit 31) is set.
0	Reserved

10.1.10 V0STS—Virtual Channel 0 Resource Status Register

Offset Address: 201A–201Bh Attribute: RO
Default Value: 0000h Size: 16-bit

Bit	Description
15:2	Reserved
1	**VC Negotiation Pending (NP)**—RO. When set, indicates the virtual channel is still being negotiated with ingress ports.
0	Reserved

10.1.11 V1CTL—Virtual Channel 1 Resource Control Register

Offset Address: 2020–2023h Attribute: R/W, RO, R/WL
Default Value: 00000000h Size: 32-bit

Bit	Description
31	**Virtual Channel Enable (EN)**—R/W. Enables the VC when set. Disables the VC when cleared.
30:28	Reserved
27:24	**Virtual Channel Identifier (ID)**—R/W. Indicates the ID to use for this virtual channel.
23:16	Reserved
15:10	**Extended TC/VC Map (ETVM):** R/WL. Defines the upper 8-bits of the VC0 16-bit TC/VC mapping registers. These registers use the PCI Express reserved TC[3] traffic class bit. These bits are locked if the TCLOCKDN bit (RCBA+0050h:bit 31) is set.
9:8	**Reserved**
7:1	**Transaction Class / Virtual Channel Map (TVM)**—R/WL. Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. These bits are locked if the TCLOCKDN bit (RCBA+0050h:bit 31) is set.
0	Reserved

10.1.12 V1STS—Virtual Channel 1 Resource Status Register

Offset Address: 2026–2027h Attribute: RO
Default Value: 0000h Size: 16-bit

Bit	Description
15:2	Reserved
1	**VC Negotiation Pending (NP)**—RO. When set, indicates the virtual channel is still being negotiated with ingress ports.
0	Reserved

10.1.13 REC—Root Error Command Register

Offset Address: 20AC–20AFh Attribute: R/W
Default Value: 0000h Size: 32-bit

Bit	Description
31	**Drop Poisoned Downstream Packets (DPDP)**—R/W. Determines how downstream packets on DMI are handled that are received with the EP field set, indicating poisoned data: 0 = Packets are forwarded downstream without forcing the UT field set. 1 = This packet and all subsequent packets with data received on DMI for any VC will have their Unsupported Transaction (UT) field set causing them to master Abort downstream. Packets without data such as memory, IO and config read requests are allowed to proceed.
30:0	Reserved

10.1.14 LCAP—Link Capabilities Register

Offset Address: 21A4–21A7h Attribute: R/WO, RO
Default Value: 00012C42h Size: 32-bit

Bit	Description
31:18	Reserved
17:15	**L1 Exit Latency (EL1)**—R/WO. 000b = Less than 1 µs 001b = 1 µs to less than 2 µs 010b = 2 µs to less than 4 µs 011b = 4 µs to less than 8 µs 100b = 8 µs to less than 16 µs 101b = 16 µs to less than 32 µs 110b = 32 µs to 64 µs 111b = More than 64 µs
14:12	**L0s Exit Latency (EL0)**—R/W. This field indicates that exit latency is 128 ns to less than 256 ns.
11:10	**Active State Link PM Support (APMS)**—R/W. Indicates the level of ASPM support on DMI. 00 = Disabled 01 = L0s entry supported 10 = Reserved 11 = L0s and L1 entry supported
9:4	**Maximum Link Width (MLW)**—RO. Indicates the maximum link width is 4 ports.
3:0	**Supported Link Speed (MLS)**—RO. Indicates the supported links speeds is 5.0 GT/s.

10.1.15 LCTL—Link Control Register

Offset Address: 21A8–21A9h Attribute: R/W
Default Value: 0000h Size: 16-bit

Bit	Description
15:8	Reserved
7	**Extended Synch (ES)**—R/W. When set, forces extended transmission of FTS ordered sets when exiting L0s prior to entering L0 and extra TS1 sequences at exit from L1 prior to entering L0.
6:2	Reserved
1:0	**Active State Link PM Control (ASPM)**—R/W. Indicates whether DMI should enter L0s, L1, or both. 00 = Disabled 01 = L0s entry enabled 10 = L1 entry enabled 11 = L0s and L1 entry enabled

10.1.16 LSTS—Link Status Register

Offset Address: 21AA–21ABh Attribute: RO
Default Value: 0042h Size: 16-bit

Bit	Description
15:10	Reserved
9:4	**Negotiated Link Width (NLW)—**RO. Negotiated link width is x4 (000100b).
3:0	**Current Link Speed (LS)**—RO. 0001b = 2.5 Gb/s 0010b = 5.0 Gb/s

10.1.17 DLCTL2—DMI Link Control 2 Register

Offset Address: 21B0–21B1h Attribute: R/W, RO
Default Value: 0001h Size: 16-bit

Bit	Description
31:4	Reserved
3:0	**DLCTL2 Field 1—**R/W. BIOS must set these bits.

10.1.18 DMIC—DMI Control Register

Offset Address: 2234–2237h Attribute: R/W
Default Value: 00000000h Size: 32-bit

Bit	Description
31:2	Reserved
1:0	**DMI Clock Gate Enable (DMICGEN)**—R/W. BIOS must program this field to 11b.

10.1.19 TCTL—TCO Configuration Register

Offset Address:	3000–3000h	Attribute:	R/W
Default Value:	00h	Size:	8-bit

Bit	Description
7	**TCO IRQ Enable (IE)**—R/W. 0 = TCO IRQ is disabled. 1 = TCO IRQ is enabled, as selected by the TCO_IRQ_SEL field.
6:3	Reserved
2:0	**TCO IRQ Select (IS)**—R/W. Specifies on which IRQ the TCO will internally appear. If not using the APIC, the TCO interrupt must be routed to IRQ9–11, and that interrupt is not sharable with the SERIRQ stream, but is shareable with other PCI interrupts. If using the APIC, the TCO interrupt can also be mapped to IRQ20–23, and can be shared with other interrupt. 000 = IRQ 9 001 = IRQ 10 010 = IRQ 11 011 = Reserved 100 = IRQ 20 (only if APIC enabled) 101 = IRQ 21 (only if APIC enabled) 110 = IRQ 22 (only if APIC enabled) 111 = IRQ 23 (only if APIC enabled) When setting these bits, the IE bit should be cleared to prevent glitching. When the interrupt is mapped to APIC interrupts 9, 10 or 11, the APIC should be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, the APIC should be programmed for active-low reception.

10.1.20 D31IP—Device 31 Interrupt Pin Register

Offset Address: 3100–3103h Attribute: R/W, RO
Default Value: 03243200h Size: 32-bit

Bit	Description
31:28	Reserved
27:24	**Thermal Sensor Pin (TSIP)—**R/W. Indicates which pin the Thermal Throttle controller drives as its interrupt 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h–Fh = Reserved
23:20	**SATA Pin 2 (SIP2)—**R/W. Indicates which pin the SATA controller 2 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h–Fh = Reserved
19:16	Reserved
15:12	**SMBus Pin (SMIP)**—R/W. Indicates which pin the SMBus controller drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h–Fh = Reserved
11:8	**SATA Pin (SIP)**—R/W. Indicates which pin the SATA controller drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h–Fh = Reserved
7:4	Reserved
3:0	LPC Bridge Pin (LIP)—RO. Currently, the LPC bridge does not generate an interrupt, so this field is read-only and 0.

10.1.21 D30IP—Device 30 Interrupt Pin Register

Offset Address: 3104–3107h Attribute: RO
Default Value: 00000000h Size: 32-bit

Bit	Description
31:4	Reserved
3:0	PCI Bridge Pin (PIP)—RO. Currently, the PCI bridge does not generate an interrupt, so this field is read-only and 0.

10.1.22 D29IP—Device 29 Interrupt Pin Register

Offset Address:	3108–310Bh	Attribute:	R/W
Default Value:	10004321h	Size:	32-bit

Bit	Description
31:4	Reserved
3:0	**EHCI #1 Pin (E1P)**—R/W. Indicates which pin the EHCI controller #1 drives as its interrupt, if controller exists. 0h = No interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h–7h = Reserved ***Note:*** EHCI Controller #1 is mapped to Device 29 Function 0.

10.1.23 D28IP—Device 28 Interrupt Pin Register

Offset Address:	310C–310Fh	Attribute:	R/W
Default Value:	00214321h	Size:	32-bit

Bit	Description
31:28	**PCI Express #8 Pin (P8IP)**—R/W. Indicates which pin the PCI Express* port #8 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h–7h = Reserved
27:24	**PCI Express #7 Pin (P7IP)**—R/W. Indicates which pin the PCI Express port #7 drives as its interrupt. 0h = No interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h–7h = Reserved
23:20	**PCI Express #6 Pin (P6IP)**—R/W. Indicates which pin the PCI Express* port #6 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h–7h = Reserved
19:16	**PCI Express #5 Pin (P5IP)**—R/W. Indicates which pin the PCI Express port #5 drives as its interrupt. 0h = No interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h–7h = Reserved
15:12	**PCI Express #4 Pin (P4IP)**—R/W. Indicates which pin the PCI Express* port #4 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# (Default) 5h–7h = Reserved

Bit	Description
11:8	**PCI Express #3 Pin (P3IP)**—R/W. Indicates which pin the PCI Express port #3 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# (Default) 4h = INTD# 5h–7h = Reserved
7:4	**PCI Express #2 Pin (P2IP)**—R/W. Indicates which pin the PCI Express port #2 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h–7h = Reserved
3:0	**PCI Express #1 Pin (P1IP)**—R/W. Indicates which pin the PCI Express port #1 drives as its interrupt. 0h = No interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h–7h = Reserved

10.1.24 D27IP—Device 27 Interrupt Pin Register

Offset Address: 3110–3113h Attribute: R/W
Default Value: 00000001h Size: 32-bit

Bit	Description
31:4	Reserved
3:0	**Intel HD Audio Pin (ZIP)—**R/W. Indicates which pin the Intel HD Audio controller drives as its interrupt. 0h = No interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h–Fh = Reserved

10.1.25 D26IP—Device 26 Interrupt Pin Register

Offset Address: 3114–3117h Attribute: R/W
Default Value: 30000321h Size: 32-bit

Bit	Description
31:4	Reserved
3:0	**EHCI #2 Pin (E2P)—**R/W. Indicates which pin EHCI controller #2 drives as its interrupt, if controller exists. 0h = No Interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h–Fh = Reserved ***Note:*** EHCI Controller #2 is mapped to Device 26 Function 0.

10.1.26 D25IP—Device 25 Interrupt Pin Register

Offset Address:	3118–311Bh	Attribute:	R/W
Default Value:	00000001h	Size:	32-bit

Bit	Description
31:4	Reserved
3:0	**GbE LAN Pin (LIP)**—R/W. Indicates which pin the internal GbE LAN controller drives as its interrupt 0h = No Interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h–Fh = Reserved

10.1.27 D22IP—Device 22 Interrupt Pin Register

Offset Address:	3124–3127h	Attribute:	R/W
Default Value:	00000001h	Size:	32-bit

Bit	Description
31:16	Reserved
15:12	**KT Pin (KTIP)**—R/W. Indicates which pin the Keyboard text PCI functionality drives as its interrupt 0h = No Interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h–Fh = Reserved
11:8	Reserved
7:4	**Intel MEI #2 Pin (MEI2IP)**—R/W. Indicates which pin the Intel MEI #2 drives as its interrupt 0h = No Interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h–Fh = Reserved
3:0	**Intel MEI #1 Pin (MEI1IP)**—R/W. Indicates which pin the Intel MEI #1 drives as its interrupt 0h = No Interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h–Fh = Reserved

10.1.28 D31IR—Device 31 Interrupt Route Register

Offset Address:	3140–3141h	Attribute:	R/W
Default Value:	3210h	Size:	16-bit

Bit	Description
15	Reserved
14:12	**Interrupt D Pin Route (IDR)**—R/W. Indicates which physical pin on the PCH is connected to the INTD# pin reported for device 31 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	**Interrupt C Pin Route (ICR)**—R/W. Indicates which physical pin on the PCH is connected to the INTC# pin reported for device 31 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	**Interrupt B Pin Route (IBR)**—R/W. Indicates which physical pin on the PCH is connected to the INTB# pin reported for device 31 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	**Interrupt A Pin Route (IAR)**—R/W. Indicates which physical pin on the PCH is connected to the INTA# pin reported for device 31 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

10.1.29 D29IR—Device 29 Interrupt Route Register

Offset Address:	3144–3145h	Attribute:	R/W
Default Value:	3210h	Size:	16-bit

Bit	Description
15	Reserved
14:12	**Interrupt D Pin Route (IDR)**—R/W. Indicates which physical pin on the PCH is connected to the INTD# pin reported for device 29 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	**Interrupt C Pin Route (ICR)**—R/W. Indicates which physical pin on the PCH is connected to the INTC# pin reported for device 29 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	**Interrupt B Pin Route (IBR)**—R/W. Indicates which physical pin on the PCH is connected to the INTB# pin reported for device 29 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	**Interrupt A Pin Route (IAR)**—R/W. Indicates which physical pin on the PCH is connected to the INTA# pin reported for device 29 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

10.1.30 D28IR—Device 28 Interrupt Route Register

Offset Address:	3146–3147h	Attribute:	R/W
Default Value:	3210h	Size:	16-bit

Bit	Description
15	Reserved
14:12	**Interrupt D Pin Route (IDR)**—R/W. Indicates which physical pin on the PCH is connected to the INTD# pin reported for device 28 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	**Interrupt C Pin Route (ICR)**—R/W. Indicates which physical pin on the PCH is connected to the INTC# pin reported for device 28 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	**Interrupt B Pin Route (IBR)**—R/W. Indicates which physical pin on the PCH is connected to the INTB# pin reported for device 28 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	**Interrupt A Pin Route (IAR)**—R/W. Indicates which physical pin on the PCH is connected to the INTA# pin reported for device 28 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

10.1.31 D27IR—Device 27 Interrupt Route Register

Offset Address:	3148–3149h	Attribute:	R/W
Default Value:	3210h	Size:	16-bit

Bit	Description
15	Reserved
14:12	**Interrupt D Pin Route (IDR)**—R/W. Indicates which physical pin on the PCH is connected to the INTD# pin reported for device 27 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	**Interrupt C Pin Route (ICR)**—R/W. Indicates which physical pin on the PCH is connected to the INTC# pin reported for device 27 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	**Interrupt B Pin Route (IBR)**—R/W. Indicates which physical pin on the PCH is connected to the INTB# pin reported for device 27 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	**Interrupt A Pin Route (IAR)**—R/W. Indicates which physical pin on the PCH is connected to the INTA# pin reported for device 27 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

10.1.32 D26IR—Device 26 Interrupt Route Register

Offset Address: 314C–314Dh Attribute: R/W
Default Value: 3210h Size: 16-bit

Bit	Description
15	Reserved
14:12	**Interrupt D Pin Route (IDR)—**R/W. Indicates which physical pin on the PCH is connected to the INTD# pin reported for device 26 functions: 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	**Interrupt C Pin Route (ICR)**—R/W. Indicates which physical pin on the PCH is connected to the INTC# pin reported for device 26 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	**Interrupt B Pin Route (IBR)**—R/W. Indicates which physical pin on the PCH is connected to the INTB# pin reported for device 26 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	**Interrupt A Pin Route (IAR)**—R/W. Indicates which physical pin on the PCH is connected to the INTA# pin reported for device 26 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

10.1.33 D25IR—Device 25 Interrupt Route Register

Offset Address:	3150–3151h	Attribute:	R/W
Default Value:	3210h	Size:	16-bit

Bit	Description
15	Reserved
14:12	**Interrupt D Pin Route (IDR):**—R/W. Indicates which physical pin on the PCH is connected to the INTD# pin reported for device 25 functions: 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	**Interrupt C Pin Route (ICR)**—R/W. Indicates which physical pin on the PCH is connected to the INTC# pin reported for device 25 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	**Interrupt B Pin Route (IBR)**—R/W. Indicates which physical pin on the PCH is connected to the INTB# pin reported for device 25 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	**Interrupt A Pin Route (IAR)**—R/W. Indicates which physical pin on the PCH is connected to the INTA# pin reported for device 25 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

10.1.34 D22IR—Device 22 Interrupt Route Register

Offset Address: 315C–315Dh Attribute: R/W
Default Value: 3210h Size: 16-bit

Bit	Description
15	Reserved
14:12	**Interrupt D Pin Route (IDR):**—R/W. Indicates which physical pin on the PCH is connected to the INTD# pin reported for device 22 functions: 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	**Interrupt C Pin Route (ICR)**—R/W. Indicates which physical pin on the PCH is connected to the INTC# pin reported for device 22 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	**Interrupt B Pin Route (IBR)**—R/W. Indicates which physical pin on the PCH is connected to the INTB# pin reported for device 22 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	**Interrupt A Pin Route (IAR)**—R/W. Indicates which physical pin on the PCH is connected to the INTA# pin reported for device 22 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

10.1.35 OIC—Other Interrupt Control Register

Offset Address: 31FE–31FFh Attribute: R/W
Default Value: 0000h Size: 16-bit

Bit	Description
15:10	Reserved
9	**Coprocessor Error Enable (CEN)**—R/W. 0 = FERR# will not generate IRQ13 nor IGNNE#. 1 = If FERR# is low, the PCH generates IRQ13 internally and holds it until an I/O port F0h write. It will also drive IGNNE# active.
8	**APIC Enable (AEN)**—R/W. 0 = The internal IOxAPIC is disabled. 1 = Enables the internal IOxAPIC and its address decode. ***Note:*** Software should read this register after modifying APIC enable bit prior to access to the IOxAPIC address range.
7:0	**APIC Range Select (ASEL)—**R/W.These bits define address bits 19:12 for the IOxAPIC range. The default value of 00h enables compatibility with prior PCH products as an initial value. This value must not be changed unless the IOxAPIC Enable bit is cleared.

Note: FEC1_0000h–FEC4_FFFFh is allocated to PCIe when I/OxApic Enable (PAE) bit is set.

10.1.36 PRSTS—Power and Reset Status Register

Offset Address: 3310–3313h Attribute: RO, R/WC
Default Value: 03000000h Size: 32-bit

Bit	Description
31:16	Reserved
15	**Power Management Watchdog Timer**—R/WC. This bit is set when the Power Management watchdog timer causes a global reset.
14:5	Reserved
6	**Intel ME Watchdog Timer Status**—R/WC. This bit is set when the Intel ME watchdog timer causes a global reset.
5	**Wake On LAN Override Wake Status (WOL_OVR_WK_STS)**—R/WC. This bit gets set when all of the following conditions are met: • Integrated LAN Signals a Power Management Event • The system is not in S0 • The "WOL Enable Override" bit is set in configuration space. BIOS can read this status bit to determine this wake source. Software clears this bit by writing a 1 to it.
4	**PRSTS Field 1 —** R/W. BIOS may write to this bit field.
3	**Intel ME Host Power Down (ME_HOST_PWRDN)—**R/WC. This bit is set when the Intel ME generates a host reset with power down.
2	**Intel ME Host Reset Warm Status (ME_HRST_WARM_STS)**—R/WC. This bit is set when the Intel ME generates a Host reset without power cycling. Software clears this bit by writing a 1 to this bit position.
1	**Intel ME Host Reset Cold Status (ME_HRST_COLD_STS)**—R/WC. This bit is set when the Intel ME generates a Host reset with power cycling. Software clears this bit by writing a 1 to this bit position.
0	**Intel ME WAKE STATUS (ME_WAKE_STS)**—R/WC. This bit is set when the Intel ME generates a Non-Maskable wake event, and is not affected by any other enable bit. When this bit is set, the Host Power Management logic wakes to S0.

10.1.37 PM_CFG—Power Management Configuration

Offset Address:	3318–331Bh	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit

Bit	Description
31:27	Reserved.
26:24	**PM_CFG Field 1**—R/W. BIOS must program this field to '101'.
23:22	Reserved.
21	**RTC Wake from Deep S4/S5 Disable (RTC_DS_WAKE_DIS)**—R/W. When set, this bit disables RTC wakes from waking the system from Deep S4/S5. This bit is reset by RTCRST#.
20	Reserved.
19:18	**SLP_SUS# Minimum Assertion Width (SLP_SUS_MIN_ASST_WDTH)**—R/W. This field indicates the minimum assertion width of the SLP_SUS# signal to guarantee that the SUS power supplies have been fully power cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power circuits, etc. Valid values are: 11 = 4 seconds 10 = 1 second 01 = 500 ms 00 = 0 ms (that is, stretching disabled – default) These bits are cleared by RTCRST# assertion. This field is RO when the SLP Stretching Policy Lock-Down bit is set. This field is ignored when exiting G3 or Deep S4/S5 states if the "Disable SLP Stretching After SUS Well Power Up" bit is set. Note that unlike with all other SLP_* pin stretching, this disable bit only impacts SLP_SUS# stretching during G3 exit rather than both G3 and Deep S4/S5 exit. SLP_SUS# stretching always applies to Deep S4/S5 regardless of the disable bit. For platforms that enable Deep S4/S5, BIOS must program SLP_SUS# stretching to be greater than or equal to the largest stretching value on any other SLP_* pin (SLP_S3#, SLP_S4#, or SLP_A#).
17:16	**SLP_A# Minimum Assertion Width (SLP_A_MIN_ASST_WDTH)—**R/W. This field indicates the minimum assertion width of the SLP_A# signal to guarantee that the ASW power supplies have been fully power cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power circuits, etc. Valid values are: 11 = 2 seconds 10 = 98 ms 01 = 4 seconds 00 = 0 ms (that is, stretching disabled – default) These bits are cleared by RTCRST# assertion. ***Notes:*** 1. This field is RO when the SLP Stretching Policy Lock-Down bit is set. 2. This field is ignored when exiting G3 or Deep S4/S5 states if the "Disable SLP Stretching After SUS Well Power Up" bit is set.
15:0	Reserved.

10.1.38 DEEP_S4_POL—Deep S4/S5 From S4 Power Policies

Offset Address: 332C–332Fh Attribute: R/W
Default Value: 00000000h Size: 32-bit
This register is in the RTC power well and is reset by RTCRST# assertion.

Bit	Description
31:2	Reserved.
1	**Deep S4/S5 From S4 Enable in DC Mode (DPS4_EN_DC)**—R/W. A '1' in this bit enables the platform to enter Deep S4/S5 while operating in S4 on DC power (based on the AC_PRESENT pin value).
0	**Deep S4/S5 From S4 Enable in AC Mode (DPS4_EN_AC)**—R/W. A '1' in this bit enables the platform to enter Deep S4 while operating in S4 on AC power (based on the AC_PRESENT pin value).

10.1.39 DEEP_S5_POL—Deep S4/S5 From S5 Power Policies

Offset Address: 3330–3333h Attribute: R/W
Default Value: 00000000h Size: 32-bit
This register is in the RTC power well and is reset by RTCRST# assertion.

Bit	Description
31:16	Reserved.
15	**Deep S4/S5 From S5 Enable in DC Mode (DPS5_EN_DC)**—R/W. A '1' in this bit enables the platform to enter Deep S4/S5 while operating in S5 on DC power.
14	**Deep S4/S5 From S5 Enable in AC Mode (DPS5_EN_AC)**—R/W. A '1' in this bit enables the platform to enter Deep S4/S5 while operating in S5 on AC power.
13:0	Reserved.

10.1.40 RC—RTC Configuration Register

Offset Address: 3400–3403h Attribute: R/W, R/WLO
Default Value: 00000000h Size: 32-bit

Bit	Description
31:5	Reserved
4	**Upper 128 Byte Lock (UL)**—R/WLO. 0 = Bytes not locked. 1 = Bytes 38h–3Fh in the upper 128-byte bank of RTC RAM are locked and cannot be accessed. Writes will be dropped and reads will not return any ensured data. Bit reset on system reset.
3	**Lower 128 Byte Lock (LL)**—R/WLO. 0 = Bytes not locked. 1 = Bytes 38h–3Fh in the lower 128-byte bank of RTC RAM are locked and cannot be accessed. Writes will be dropped and reads will not return any ensured data. Bit reset on system reset.
2	**Upper 128 Byte Enable (UE)**—R/W. 0 = Bytes locked. 1 = The upper 128-byte bank of RTC RAM can be accessed.
1:0	Reserved

10.1.41 HPTC—High Precision Timer Configuration Register

Offset Address: 3404–3407h Attribute: R/W
Default Value: 00000000h Size: 32-bit

Bit	Description
31:8	Reserved
7	**Address Enable (AE)**—R/W. 0 = Address disabled. 1 = The PCH will decode the High Precision Timer memory address range selected by bits 1:0 below.
6:2	Reserved
1:0	**Address Select (AS)**—R/W. This 2-bit field selects 1 of 4 possible memory address ranges for the High Precision Timer functionality. The encodings are: 00 = FED0_0000h – FED0_03FFh 01 = FED0_1000h – FED0_13FFh 10 = FED0_2000h – FED0_23FFh 11 = FED0_3000h – FED0_33FFh

10.1.42 GCS—General Control and Status Register

Offset Address: 3410–3413h Attribute: R/W, R/WLO
Default Value: 00000yy0h (yy = xx0000x0b)Size: 32-bit

Bit	Description
31:13	Reserved.
12	**Function Level Reset Capability Structure Select (FLRCSSEL)**—R/W. 0 = Function Level Reset (FLR) will utilize the standard capability structure with unique capability ID assigned by PCISIG. 1 = Vendor Specific Capability Structure is selected for FLR.
11:10	**Boot BIOS Straps (BBS)—**R/W. This field determines the destination of accesses to the BIOS memory range. The default values for these bits represent the strap values of GNT1# /GPIO51 (bit 11) at the rising edge of PCH_PWROK and SATA1GP/GPIO19 (bit 10) at the rising edge of PCH_PWROK. 00 = LPC 01 = Reserved 10 = PCI 11 = SPI When PCI is selected, the top 16 MB of memory below 4 GB (FF00_0000h to FFFF_FFFFh) is accepted by the primary side of the PCI P2P bridge and forwarded to the PCI bus. This allows systems with corrupted or unprogrammed flash to boot from a PCI device. The PCI-to-PCI bridge Memory Space Enable bit does not need to be set (nor any other bits) in order for these cycles to go to PCI. Note that BIOS decode range bits and the other BIOS protection bits have no effect when PCI is selected. This functionality is intended for debug/testing only. When SPI or LPC is selected, the range that is decoded is further qualified by other configuration bits described in the respective sections. The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down (bit 0) is not set. ***Note:*** Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN.
9	**Server Error Reporting Mode (SERM)**—R/W. 0 = The PCH is the final target of all errors. The Processor sends a messages to the PCH for the purpose of generating NMI. 1 = The Processor is the final target of all errors from PCI Express* and DMI. In this mode, if the PCH detects a fatal, non-fatal, or correctable error on DMI or its downstream ports, it sends a message to the Processor. If the PCH receives an ERR_* message from the downstream port, it sends that message to the Processor.
8:6	Reserved

Bit	Description
5	**No Reboot (NR)**—R/W. This bit is set when the "No Reboot" strap (SPKR pin on the PCH) is sampled high on PCH_PWROK. This bit may be set or cleared by software if the strap is sampled low but may not override the strap when it indicates "No Reboot". 0 = System will reboot upon the second timeout of the TCO timer. 1 = The TCO timer will count down and generate the SMI# on the first timeout, but will not reboot on the second timeout.
4	**Alternate Access Mode Enable (AME)**—R/W. 0 = Disabled. 1 = Alternate access read only registers can be written, and write only registers can be read. Before entering a low power state, several registers from powered down parts may need to be saved. In the majority of cases, this is not an issue, as registers have read and write paths. However, several of the ISA compatible registers are either read only or write only. To get data out of write-only registers, and to restore data into read-only registers, the PCH implements an alternate access mode. For a list of these registers see Section 5.14.9.
3	**Shutdown Policy Select (SPS)**—R/W. 0 = PCH will drive INIT# in response to the shutdown Vendor Defined Message (VDM). (Default) 1 = PCH will treat the shutdown VDM similar to receiving a CF9h I/O write with data value 06h, and will drive PLTRST# active.
2	**Reserved Page Route (RPR)**—R/W. Determines where to send the reserved page registers. These addresses are sent to PCI or LPC for the purpose of generating POST codes. The I/O addresses modified by this field are: 80h, 84h, 85h, 86h, 88h, 8Ch, 8Dh, and 8Eh. 0 = Writes will be forwarded to LPC, shadowed within the PCH, and reads will be returned from the internal shadow 1 = Writes will be forwarded to PCI, shadowed within the PCH, and reads will be returned from the internal shadow. ***Note:*** If some writes are done to LPC/PCI to these I/O ranges, and then this bit is flipped, such that writes will now go to the other interface, the reads will not return what was last written. Shadowing is performed on each interface. The aliases for these registers, at 90h, 94h, 95h, 96h, 98h, 9Ch, 9Dh, and 9Eh, are always decoded to LPC.
1	Reserved
0	**BIOS Interface Lock-Down (BILD)**—R/WLO. 0 = Disabled. 1 = Prevents BUC.TS (offset 3414, bit 0) and GCS.BBS (offset 3410h, bits 11:10) from being changed. This bit can only be written from 0 to 1 once.

10.1.43 BUC—Backed Up Control Register

Offset Address:	3414–3414h	Attribute:	R/W
Default Value:	0000000xb	Size:	8-bit

All bits in this register are in the RTC well and only cleared by RTCRST#

Bit	Description
7:6	Reserved
5	**LAN Disable—**R/W. 0 = LAN is Enabled 1 = LAN is Disabled. Changing the internal GbE controller from disabled to enabled requires a system reset (write of 0Eh to CF9h (RST_CNT Register)) immediately after clearing the LAN disable bit. A reset is not required if changing the bit from enabled to disabled. This bit is locked by the Function Disable SUS Well Lockdown register. Once locked this bit can not be changed by software.
4	**Daylight Savings Override (SDO)—**R/W. 0 = Daylight Savings is Enabled. 1 = The DSE bit in RTC Register B is set to Read-only with a value of 0 to disable daylight savings.
3:1	**Reserved**
0	**Top Swap (TS)**—R/W. 0 = PCH will not invert A16. 1 = PCH will invert A16, A17, or A18 for cycles going to the BIOS space. If booting from LPC (FWH), then the boot-block size is 64 KB and A16 is inverted if Top Swap is enabled. If booting from SPI, then the BIOS Boot-Block size soft strap determines if A16, A17, or A18 should be inverted if Top Swap is enabled. If PCH is strapped for Top Swap (GNT3#/GPIO55 is low at rising edge of PCH_PWROK), then this bit cannot be cleared by software. The strap jumper should be removed and the system rebooted.

10.1.44 FD—Function Disable Register

Offset Address:	3418–341Bh	Attribute:	R/W
Default Value:	See bit description	Size:	32-bit

When disabling a function, only the configuration space is disabled. Software must ensure that all functionality within a controller that is not desired (such as memory spaces, I/O spaces, and DMA engines) is disabled prior to disabling the function.

When a function is disabled, software must not attempt to re-enable it. A disabled function can only be re-enabled by a platform reset.

Bit	Description
31:26	Reserved
25	**Serial ATA Disable 2 (SAD2)—**R/W. Default is 0. 0 = The SATA controller #2 (D31:F5) is enabled. 1 = The SATA controller #2 (D31:F5) is disabled.
24	**Thermal Sensor Registers Disable (TTD)—**R/W. Default is 0. 0 = Thermal Sensor Registers (D31:F6) are enabled. 1 = Thermal Sensor Registers (D31:F6) are disabled.
23	**PCI Express 8 Disable (PE8D)**—R/W. Default is 0. When disabled, the link for this port is put into the "link down" state. 0 = PCI Express port #8 is enabled. 1 = PCI Express port #8 is disabled.
22	**PCI Express 7 Disable (PE7D)**—R/W. Default is 0. When disabled, the link for this port is put into the link down state. 0 = PCI Express port #7 is enabled. 1 = PCI Express port #7 is disabled.

Bit	Description
21	**PCI Express 6 Disable (PE6D)**—R/W. Default is 0. When disabled, the link for this port is put into the "link down" state. 0 = PCI Express port #6 is enabled. 1 = PCI Express port #6 is disabled.
20	**PCI Express 5 Disable (PE5D)**—R/W. Default is 0. When disabled, the link for this port is put into the link down state. 0 = PCI Express port #5 is enabled. 1 = PCI Express port #5 is disabled.
19	**PCI Express 4 Disable (PE4D)**—R/W. Default is 0. When disabled, the link for this port is put into the "link down" state. 0 = PCI Express port #4 is enabled. 1 = PCI Express port #4 is disabled. ***Note:*** This bit must be set when Port 1 is configured as a x4.
18	**PCI Express 3 Disable (PE3D)**—R/W. Default is 0. When disabled, the link for this port is put into the link down state. 0 = PCI Express port #3 is enabled. 1 = PCI Express port #3 is disabled. ***Note:*** This bit must be set when Port 1 is configured as a x4.
17	**PCI Express 2 Disable (PE2D)**—R/W. Default is 0. When disabled, the link for this port is put into the link down state. 0 = PCI Express port #2 is enabled. 1 = PCI Express port #2 is disabled. ***Note:*** This bit must be set when Port 1 is configured as a x4 or a x2.
16	**PCI Express 1 Disable (PE1D)**—R/W. Default is 0. When disabled, the link for this port is put into the link down state. 0 = PCI Express port #1 is enabled. 1 = PCI Express port #1 is disabled.
15	**EHCI #1 Disable (EHCI1D)**—R/W. Default is 0. 0 = The EHCI #1 is enabled. 1 = The EHCI #1 is disabled.
14	**LPC Bridge Disable (LBD)**—R/W. Default is 0. 0 = The LPC bridge is enabled. 1 = The LPC bridge is disabled. Unlike the other disables in this register, the following additional spaces will no longer be decoded by the LPC bridge: • Memory cycles below 16 MB (1000000h) • I/O cycles below 64 KB (10000h) • The Internal I/OxAPIC at FEC0_0000 to FECF_FFFF Memory cycles in the LPC BIOS range below 4 GB will still be decoded when this bit is set, but the aliases at the top of 1 MB (the E and F segment) no longer will be decoded.
13	**EHCI #2 Disable (EHCI2D)**—R/W. Default is 0. 0 = The EHCI #2 is enabled. 1 = The EHCI #2 is disabled.
12:5	Reserved
4	**Intel HD Audio Disable (HDAD)**—R/W. Default is 0. 0 = The Intel HD Audio controller is enabled. 1 = The Intel HD Audio controller is disabled and its PCI configuration space is not accessible.
3	**SMBus Disable (SD)**—R/W. Default is 0. 0 = The SMBus controller is enabled. 1 = The SMBus controller is disabled. In ICH5 and previous, this also disabled the I/O space. In the PCH, it only disables the configuration space.
2	**Serial ATA Disable 1 (SAD1)**—R/W. Default is 0. 0 = The SATA controller #1 (D31:F2) is enabled. 1 = The SATA controller #1 (D31:F2) is disabled.
1	**PCI Bridge Disable—**R/W. Default is 0. 0 = The PCI-to-PCI bridge (D30:F0) is enabled. The PCI-to-PCI bridge (D30:F0) is disabled.
0	BIOS must set this bit to 1b.

10.1.45 CG—Clock Gating

Offset Address: 341C–341Fh Attribute: R/W
Default Value: 00000000h Size: 32-bit

Bit	Description
31	**Legacy (LPC) Dynamic Clock Gate Enable—**R/W. 0 = Legacy Dynamic Clock Gating is Disabled 1 = Legacy Dynamic Clock Gating is Enabled
30	Reserved
29:28	**CG Field 1**—R/W. BIOS must program this field to 11b.
27	**SATA Port 3 Dynamic Clock Gate Enable—**R/W. 0 = SATA Port 3 Dynamic Clock Gating is Disabled 1 = SATA Port 3 Dynamic Clock Gating is Enabled
26	**SATA Port 2 Dynamic Clock Gate Enable—**R/W. 0 = SATA Port 2 Dynamic Clock Gating is Disabled 1 = SATA Port 2 Dynamic Clock Gating is Enabled
25	**SATA Port 1 Dynamic Clock Gate Enable—**R/W. 0 = SATA Port 1 Dynamic Clock Gating is Disabled 1 = SATA Port 1 Dynamic Clock Gating is Enabled
24	**SATA Port 0 Dynamic Clock Gate Enable—**R/W. 0 = SATA Port 0 Dynamic Clock Gating is Disabled 1 = SATA Port 0 Dynamic Clock Gating is Enabled
23	**LAN Static Clock Gating Enable (LANSCGE)—**R/W. 0 = LAN Static Clock Gating is Disabled 1 = LAN Static Clock Gating is Enabled when the LAN Disable bit is set in the Backed Up Control RTC register.
22	**Intel HD Audio Dynamic Clock Gate Enable—**R/W. 0 = Intel HD Audio Dynamic Clock Gating is Disabled 1 = Intel HD Audio Dynamic Clock Gating is Enabled
21	**Intel HD Audio Static Clock Gate Enable—**R/W. 0 = Intel HD Audio Static Clock Gating is Disabled 1 = Intel HD Audio Static Clock Gating is Enabled
20	**USB EHCI Static Clock Gate Enable—**R/W. 0 = USB EHCI Static Clock Gating is Disabled 1 = USB EHCI Static Clock Gating is Enabled
19	**USB EHCI Dynamic Clock Gate Enable—**R/W. 0 = USB EHCI Dynamic Clock Gating is Disabled 1 = USB EHCI Dynamic Clock Gating is Enabled
18	**SATA Port 5 Dynamic Clock Gate Enable—**R/W. 0 = SATA Port 5 Dynamic Clock Gating is Disabled 1 = SATA Port 5 Dynamic Clock Gating is Enabled
17	**SATA Port 4 Dynamic Clock Gate Enable—**R/W. 0 = SATA Port 4 Dynamic Clock Gating is Disabled 1 = SATA Port 4 Dynamic Clock Gating is Enabled
16	**PCI Dynamic Gate Enable—**R/W. 0 = PCI Dynamic Gating is Disabled 1 = PCI Dynamic Gating is Enabled
15:6	Reserved
5	**SMBus Clock Gating Enable (SMBCGEN)—**R/W. 0 = SMBus Clock Gating is Disabled. 1 = SMBus Clock Gating is Enabled.
4:1	Reserved
0	**PCI Express Root Port Static Clock Gate Enable—**R/W. 0 = PCI Express root port Static Clock Gating is Disabled 1 = PCI Express root port Static Clock Gating is Enabled

10.1.46 FDSW—Function Disable SUS Well

Offset Address: 3420h Attribute: R/W
Default Value: 00h Size: 8-bit

Bit	Description
7	**Function Disable SUS Well Lockdown (FDSWL)**—R/W03 0 = FDSW registers are not locked down 1 = FDSW registers are locked down ***Note:***
6:0	Reserved

10.1.47 FD2—Function Disable 2

Offset Address: 3428–342Bh Attribute: R/W
Default Value: 00000000h Size: 32-bit

Bit	Description
31:5	Reserved
4	**KT Disable (KTD)—**R/W. Default is 0. 0 = Keyboard Text controller (D22:F3) is enabled. 1 = Keyboard Text controller (D22:F3) is Disabled.
3	Reserved
2	**Intel MEI #2 Disable (MEI2D)—**R/W. Default is 0. 0 = Intel MEI controller #2 (D22:F1) is enabled. 1 = Intel MEI controller #2 (D22:F1) is disabled.
1	**Intel MEI #1 Disable (MEI1D)—**R/W. Default is 0. 0 = Intel MEI controller #1 (D22:F0) is enabled. 1 = Intel MEI controller #1 (D22:F0) is disabled.
0	Reserved

10.1.48 GSXBAR—GPIO Serial Expander Base Address

Offset Address: 3450–3453h Attribute: R/W, RO
Default Value: FED04000h Size: 32-bit

Bit	Description
31:10	**Base Address (BA)**—R/W. Base Address of GPIO Serial Expander logic.
9:4	Reserved
3	**Prefetchable Memory (PF)—**RO. Default is 0. Indicate the memory space is not prefetchable.
2:1	**Memory Type (TP)—**RO. Set to 00b indicating a 32-bit BAR.
0	**Resource Type (RTE)—**RO. Set to 0 indicating a Memory Space BAR.

10.1.49 GSXCTRL—GPIO Serial Expander Control Register

Offset Address: 3454–3457h Attribute: R/W, RO
Default Value: 00000000h Size: 32-bit

Bit	Description
31:5	Reserved
4	**GSX BAR Enable (GSXBAREN)—**R/W. Default is 0. 0 = GSXBAR is disabled. 1 = GSXBAR is enabled. ***Note:*** If GSX is disabled using soft strap, this bit will always read 0.
3:0	Reserved

10.1.50 MISCCTL—Miscellaneous Control Register

Offset Address: 3590–3593h Attribute: R/W
Default Value: 00000000h Size: 32-bit

This register is in the suspend well. This register is not reset on D3-to-D0, HCRESET nor core well reset.

Bit	Description
31:2	Reserved.
1	**EHCI 2 USBR Enable—**R/W. When set, this bit enables support for the USB-r redirect device on the EHCI controller in Device 26. Software must complete programming the following registers before this bit is set: 1. Enable RMH 2. HCSPARAMS (N_CC, N_Ports)
0	**EHCI 1 USBR Enable—**R/W. When set, this bit enables support for the USB-r redirect device on the EHCI controller in Device 29. Software must complete programming the following registers before this bit is set: 1. Enable RMH 2. HCSPARAMS (N_CC, N_Ports)

10.1.51 USBOCM1—Overcurrent MAP Register 1

Offset Address:	35A0–35A3h	Attribute:	R/W0
Default Value:	C0300C03h	Size:	32-bit

All bits in this register are in the Resume Well and is only cleared by RSMRST#.

Bit	Description
31:24	**OC3 Mapping** Each bit position maps OC3# to a set of ports as follows: The OC3# pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is software's responsibility to ensure that a given port's bit map is set only for one OC pin. **Bit** 31 30 29 28 27 26 25 24 **Port** 7 6 5 4 3 2 1 0
23:16	**OC2 Mapping** Each bit position maps OC2# to a set of ports as follows: The OC2# pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is software's responsibility to ensure that a given port's bit map is set only for one OC pin. **Bit** 23 22 21 20 19 18 17 16 **Port** 7 6 5 4 3 2 1 0
15:8	**OC1 Mapping** Each bit position maps OC1# to a set of ports as follows: The OC1# pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is software's responsibility to ensure that a given port's bit map is set only for one OC pin. **Bit** 15 14 13 12 11 10 9 8 **Port** 7 6 5 4 3 2 1 0
7:0	**OC0 Mapping** Each bit position maps OC0# to a set of ports as follows: The OC0# pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is software's responsibility to ensure that a given port's bit map is set only for one OC pin. **Bit** 7 6 5 4 3 2 1 0 **Port** 7 6 5 4 3 2 1 0

10.1.52 USBOCM2—Overcurrent MAP Register 2

Offset Address:	35A4–35A7h	Attribute:	R/W0
Default Value:	00h	Size:	32-bit

All bits in this register are in the Resume Well and is only cleared by RSMRST#.

Bit	Description
31:30	**Reserved**
29:24	**OC7 Mapping** Each bit position maps OC7# to a set of ports as follows: The OC7# pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is software's responsibility to ensure that a given port's bit map is set only for one OC pin. **Bit** 29 28 27 26 25 24 **Port** 13 12 11 10 9 8
23:22	**Reserved**
21:16	**OC6 Mapping** Each bit position maps OC6# to a set of ports as follows: The OC6# pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is software's responsibility to ensure that a given port's bit map is set only for one OC pin. **Bit** 21 20 19 18 17 16 **Port** 13 12 11 10 9 8
15:14	**Reserved**
13:8	**OC5 Mapping** Each bit position maps OC5# to a set of ports as follows: The OC5# pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is software's responsibility to ensure that a given port's bit map is set only for one OC pin. **Bit** 13 12 11 10 9 8 **Port** 13 12 11 10 9 8
7:6	**Reserved**
5:0	**OC4 Mapping** Each bit position maps OC4# to a set of ports as follows: The OC4# pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is software's responsibility to ensure that a given port's bit map is set only for one OC pin. **Bit** 5 4 3 2 1 0 **Port** 13 12 11 10 9 8

10.1.53 RMHWKCTL—Rate Matching Hub Wake Control Register

Offset Address:	35B0–35B3h	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit

All bits in this register are in the Resume Well and is only cleared by RSMRST#

Bit	Description
31:10	**Reserved**
9	**RMH 2 Inherit EHCI2 Wake Control Settings:** When this bit is set, the RMH behaves as if bits 6:4 of this register reflect the appropriate bits of EHCI PORTSC0 bits 22:20.
8	**RMH 1 Inherit EHCI1 Wake Control Settings:** When this bit is set, the RMH behaves as if bits 2:0 of this register reflect the appropriate bits of EHCI PORTSC0 bits 22:20.
7	**RMH 2 Upstream Wake on Device Resume** This bit governs the hub behavior when globally suspended and the system is in Sx. 0 = Enables the port to be sensitive to device initiated resume events as system wake-up events. that is, the hub will initiate a resume on its upstream port and cause a wake from Sx when a device resume occurs on an enabled DS port 1 = Device resume event is seen on a downstream port, the hub does not initiate a wake upstream and does not cause a wake from Sx

Bit	Description
6	**RMH 2 Upstream Wake on OC Disable** This bit governs the hub behavior when globally suspended and the system is in Sx. 0 = Enables the port to be sensitive to over-current conditions as system wake-up events. That is, the hub will initiate a resume on its upstream port and cause a wake from Sx when an OC condition occurs on an enabled DS port 1 = Over-current event does not initiate a wake upstream and does not cause a wake from Sx
5	**RMH 2 Upstream Wake on Disconnect Disable** This bit governs the hub behavior when globally suspended and the system is in Sx 0 = Enables disconnect events on downstream port to be treated as resume events to be propagated upstream. In this case, it is allowed to initiate a wake on its upstream port and cause a system wake from Sx in response to a disconnect event on a downstream port 1 = Downstream disconnect events do not initiate a resume on its upstream port or cause a resume from Sx.
4	**RMH 2 Upstream Wake on Connect Enable** This bit governs the hub behavior when globally suspended and the system is in Sx. 0 = Enables connect events on a downstream port to be treated as resume events to be propagated upstream. As well as waking up the system from Sx. 1 = Downstream connect events do not wake the system from Sx nor does it initiate a resume on its upstream port.
3	**RMH 1 Upstream Wake on Device Resume** This bit governs the hub behavior when globally suspended and the system is in Sx. 0 = Enables the port to be sensitive to device initiated resume events as system wake-up events. That is, the hub will initiate a resume on its upstream port and cause a wake from Sx when a device resume occurs on an enabled DS port 1 = Device resume event is seen on a downstream port, the hub does not initiate a wake upstream and does not cause a wake from Sx
2	**RMH 1 Upstream Wake on OC Disable** This bit governs the hub behavior when globally suspended and the system is in Sx. 0 = Enables the port to be sensitive to over-current conditions as system wake-up events. That is, the hub will initiate a resume on its upstream port and cause a wake from Sx when an OC condition occurs on an enabled DS port 1 = Over-current event does not initiate a wake upstream and does not cause a wake from Sx
1	**RMH 1 Upstream Wake on Disconnect Disable** This bit governs the hub behavior when globally suspended and the system is in Sx 0 = Enables disconnect events on downstream port to be treated as resume events to be propagated upstream. In this case, it is allowed to initiate a wake on its upstream port and cause a system wake from Sx in response to a disconnect event on a downstream port 1 = Downstream disconnect events do not initiate a resume on its upstream port or cause a resume from Sx.
0	**RMH 1 Upstream Wake on Connect Enable** This bit governs the hub behavior when globally suspended and the system is in Sx. 0 = Enables connect events on a downstream port to be treated as resume events to be propagated upstream. As well as waking up the system from Sx. 1 = Downstream connect events do not wake the system from Sx nor does it initiate a resume on its upstream port.

§

11 PCI-to-PCI Bridge Registers (D30:F0)

The PCH PCI bridge resides in PCI Device 30, Function 0 on bus #0. This implements the buffering and control logic between PCI and the backbone. The arbitration for the PCI bus is handled by this PCI device.

11.1 PCI Configuration Registers (D30:F0)

Note: Address locations that are not shown should be treated as Reserved (see Section 9.2 for details).

Table 11-1. PCI Bridge Register Address Map (PCI-PCI—D30:F0)

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PSTS	PCI Status	0010h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h–0Bh	CC	Class Code	060401h	RO
0Dh	PMLT	Primary Master Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	01h	RO
18h–1Ah	BNUM	Bus Number	000000h	RO
1Bh	SMLT	Secondary Master Latency Timer	00h	R/W
1Ch–1Dh	IOBASE_LIMIT	I/O Base and Limit	0000h	R/W, RO
1Eh–1Fh	SECSTS	Secondary Status	0280h	R/WC, RO
20h–23h	MEMBASE_LIMIT	Memory Base and Limit	00000000h	R/W
24h–27h	PREF_MEM_BASE_LIMIT	Prefetchable Memory Base and Limit	00010001h	R/W, RO
28h–2Bh	PMBU32	Prefetchable Memory Upper 32 Bits	00000000h	R/W
2Ch–2Fh	PMLU32	Prefetchable Memory Limit Upper 32 Bits	00000000h	R/W
34h	CAPP	Capability List Pointer	50h	RO
3Ch–3Dh	INTR	Interrupt Information	0000h	R/W, RO
3Eh–3Fh	BCTRL	Bridge Control	0000h	R/WC, RO, R/W
40h–41h	SPDH	Secondary PCI Device Hiding	0000h	R/W, RO
44h–47h	DTC	Delayed Transaction Control	00000000h	R/W
48h–4Bh	BPS	Bridge Proprietary Status	00000000h	R/WC, RO
4Ch–4Fh	BPC	Bridge Policy Configuration	00001200h	R/W RO
50–51h	SVCAP	Subsystem Vendor Capability Pointer	000Dh	RO
54h–57h	SVID	Subsystem Vendor IDs	00000000	R/WO

11.1.1 VID—Vendor Identification Register (PCI-PCI—D30:F0)

Offset Address:	00h–01h	Attribute:	RO
Default Value:	8086h	Size:	16 bits

Bit	Description
15:0	**Vendor ID**—RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h.

11.1.2 DID—Device Identification Register (PCI-PCI—D30:F0)

Offset Address:	02h–03h	Attribute:	RO
Default Value:	See bit description	Size:	16 bits

Bit	Description
15:0	**Device ID—**RO. This is a 16-bit value assigned to the PCI bridge. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Device ID Register.

11.1.3 PCICMD—PCI Command (PCI-PCI—D30:F0)

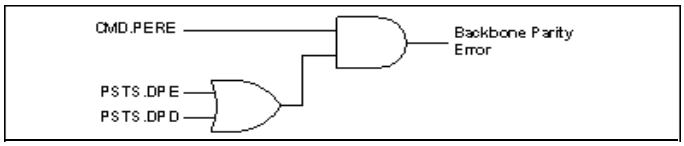
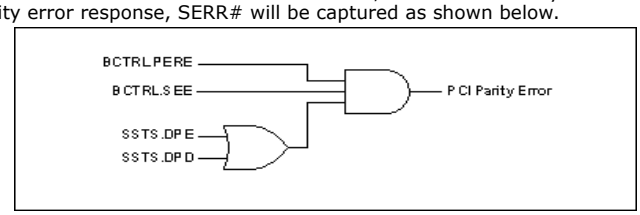
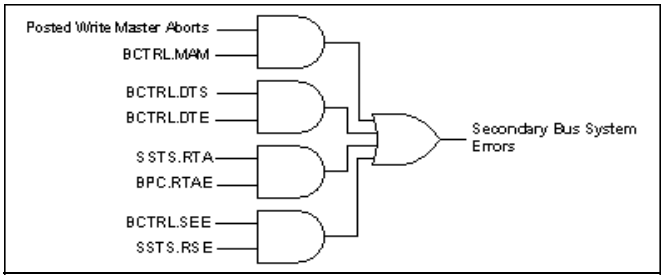
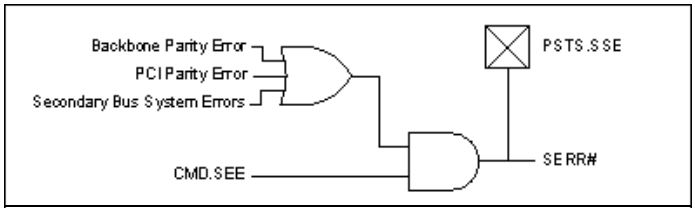
Offset Address:	04h–05h	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:11	Reserved
10	Interrupt Disable (ID)—RO. Hardwired to 0. The PCI bridge has no interrupts to disable
9	Fast Back to Back Enable (FBE)—RO. Hardwired to 0, per the *PCI Express* Base Specification, Revision 1.0a*.
8	**SERR# Enable (SERR_EN)**—R/W. 0 = Disable. 1 = Enable the PCH to generate an NMI (or SMI# if NMI routed to SMI#) when the D30:F0 SSE bit (offset 06h, bit 14) is set.
7	Wait Cycle Control (WCC)—RO. Hardwired to 0, per the *PCI Express* Base Specification, Revision 1.0a*.
6	**Parity Error Response (PER)—**R/W. 0 = The PCH ignores parity errors on the PCI bridge. 1 = The PCH will set the SSE bit (D30:F0, offset 06h, bit 14) when parity errors are detected on the PCI bridge.
5	VGA Palette Snoop (VPS)—RO. Hardwired to 0, per the *PCI Express* Base Specification, Revision 1.0a*.
4	Memory Write and Invalidate Enable (MWE)—RO. Hardwired to 0, per the *PCI Express* Base Specification, Revision 1.0a*
3	Special Cycle Enable (SCE)—RO. Hardwired to 0, per the *PCI Express* Base Specification, Revision 1.0a* and the *PCI- to-PCI Bridge Specification.*
2	**Bus Master Enable (BME)—**R/W. 0 = Disable 1 = Enable. Allows the PCI-to-PCI bridge to accept cycles from PCI.
1	**Memory Space Enable (MSE)**—R/W. Controls the response as a target for memory cycles targeting PCI. 0 = Disable 1 = Enable
0	**I/O Space Enable (IOSE)—**R/W. Controls the response as a target for I/O cycles targeting PCI. 0 = Disable 1 = Enable

11.1.4 PSTS—PCI Status Register (PCI-PCI—D30:F0)

Offset Address:	06h–07h	Attribute:	R/WC, RO
Default Value:	0010h	Size:	16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)—**R/WC. 0 = Parity error Not detected. 1 = Indicates that the PCH detected a parity error on the internal backbone. This bit gets set even if the Parity Error Response bit (D30:F0:04 bit 6) is not set.
14	**Signaled System Error (SSE)**—R/WC. Several internal and external sources of the bridge can cause SERR#. The first class of errors is parity errors related to the backbone. The PCI bridge captures generic data parity errors (errors it finds on the backbone) as well as errors returned on backbone cycles where the bridge was the master. If either of these two conditions is met, and the primary side of the bridge is enabled for parity error response, SERR# will be captured as shown below.  As with the backbone, the PCI bus captures the same sets of errors. The PCI bridge captures generic data parity errors (errors it finds on PCI) as well as errors returned on PCI cycles where the bridge was the master. If either of these two conditions is met, and the secondary side of the bridge is enabled for parity error response, SERR# will be captured as shown below.  The final class of errors is system bus errors. There are three status bits associated with system bus errors, each with a corresponding enable. The diagram capturing this is shown below.  After checking for the three above classes of errors, an SERR# is generated, and PSTS.SSE logs the generation of SERR#, if CMD.SEE (D30:F0:04, bit 8) is set, as shown below. 
13	**Received Master Abort (RMA)—**R/WC. 0 = No master abort received. 1 = Set when the bridge receives a master abort status from the backbone.

Bit	Description
12	**Received Target Abort (RTA)**—R/WC. 0 = No target abort received. 1 = Set when the bridge receives a target abort status from the backbone.
11	**Signaled Target Abort (STA)**—R/WC. 0 = No signaled target abort 1 = Set when the bridge generates a completion packet with target abort status on the backbone.
10:9	Reserved.
8	**Data Parity Error Detected (DPD)—**R/WC. 0 = Data parity error Not detected. 1 = Set when the bridge receives a completion packet from the backbone from a previous request, and detects a parity error, and CMD.PERE is set (D30:F0:04 bit 6).
7:5	Reserved.
4	**Capabilities List (CLIST)**—RO. Hardwired to 1. Capability list exist on the PCI bridge.
3	**Interrupt Status (IS)**—RO. Hardwired to 0. The PCI bridge does not generate interrupts.
2:0	Reserved

11.1.5 RID—Revision Identification Register (PCI-PCI—D30:F0)

Offset Address: 08h Attribute: RO
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	**Revision ID**—RO. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Revision ID Register.

11.1.6 CC—Class Code Register (PCI-PCI—D30:F0)

Offset Address: 09h–0Bh Attribute: RO
Default Value: 060401h Size: 24 bits

Bit	Description
23:16	**Base Class Code (BCC)**—RO. Hardwired to 06h. Indicates this is a bridge device.
15:8	**Sub Class Code (SCC)**—RO. Hardwired to 04h. Indicates this device is a PCI-to-PCI bridge.
7:0	**Programming Interface (PI)**—RO. Hardwired to 01h. Indicates the bridge is subtractive decode

11.1.7 PMLT—Primary Master Latency Timer Register (PCI-PCI—D30:F0)

Offset Address: 0Dh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:3	Master Latency Timer Count (MLTC)—RO. Reserved per the *PCI Express* Base Specification, Revision 1.0a*.
2:0	Reserved

11.1.8 HEADTYP—Header Type Register (PCI-PCI—D30:F0)

Offset Address: 0Eh Attribute: RO
Default Value: 01h Size: 8 bits

Bit	Description
7	**Multi-Function Device (MFD)**—RO. '0' indicates a single function device
6:0	**Header Type (HTYPE)—**RO. This 7-bit field identifies the header layout of the configuration space, which is a PCI-to-PCI bridge in this case.

11.1.9 BNUM—Bus Number Register (PCI-PCI—D30:F0)

Offset Address: 18h–1Ah Attribute: R/W
Default Value: 000000h Size: 24 bits

Bit	Description
23:16	**Subordinate Bus Number (SBBN)**—R/W. Indicates the highest PCI bus number below the bridge.
15:8	**Secondary Bus Number (SCBN)**—R/W. Indicates the bus number of PCI.
7:0	**Primary Bus Number (PBN)**—R/W. This field is default to 00h. In a multiple-PCH system, programmable PBN allows an PCH to be located on any bus. System configuration software is responsible for initializing these registers to appropriate values. PBN is not used by hardware in determining its bus number.

11.1.10 SMLT—Secondary Master Latency Timer Register (PCI-PCI—D30:F0)

Offset Address: 1Bh Attribute: R/W
Default Value: 00h Size: 8 bits

This timer controls the amount of time the PCH PCI-to-PCI bridge will burst data on its secondary interface. The counter starts counting down from the assertion of FRAME#. If the grant is removed, then the expiration of this counter will result in the deassertion of FRAME#. If the grant has not been removed, then the PCH PCI-to-PCI bridge may continue ownership of the bus.

Bit	Description
7:3	**Master Latency Timer Count (MLTC)—**R/W. This 5-bit field indicates the number of PCI clocks, in 8-clock increments, that the PCH remains as master of the bus.
2:0	Reserved

11.1.11 IOBASE_LIMIT—I/O Base and Limit Register (PCI-PCI—D30:F0)

Offset Address:	1Ch–1Dh	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:12	**I/O Limit Address Limit bits**[15:12]—R/W. I/O Base bits corresponding to address lines 15:12 for 4-KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	**I/O Limit Address Capability (IOLC)—**RO. Indicates that the bridge does not support 32-bit I/O addressing.
7:4	**I/O Base Address (IOBA)**—R/W. I/O Base bits corresponding to address lines 15:12 for 4-KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	**I/O Base Address Capability (IOBC)**—RO. Indicates that the bridge does not support 32-bit I/O addressing.

11.1.12 SECSTS—Secondary Status Register (PCI-PCI—D30:F0)

Offset Address:	1Eh–1Fh	Attribute:	R/WC, RO
Default Value:	0280h	Size:	16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)**—R/WC. 0 = Parity error **not** detected. 1 = PCH PCI bridge detected an address or data parity error on the PCI bus
14	**Received System Error (RSE)—**R/WC. 0 = SERR# assertion **not** received 1 = SERR# assertion is received on PCI.
13	**Received Master Abort (RMA)—**R/WC. 0 = No master abort. 1 = This bit is set whenever the bridge is acting as an initiator on the PCI bus and the cycle is master-aborted. For Processor/PCH interface packets that have completion required, this must also cause a target abort to be returned and sets PSTS.STA. (D30:F0:06 bit 11)
12	**Received Target Abort (RTA)**—R/WC. 0 = No target abort. 1 = This bit is set whenever the bridge is acting as an initiator on PCI and a cycle is target-aborted on PCI. For Processor/PCH interface packets that have completion required, this event must also cause a target abort to be returned, and sets PSTS.STA. (D30:F0:06 bit 11).
11	**Signaled Target Abort (STA)—**R/WC. 0 = No target abort. 1 = This bit is set when the bridge is acting as a target on the PCI Bus and signals a target abort.
10:9	DEVSEL# Timing (DEVT)—RO. 01h = Medium decode timing.
8	**Data Parity Error Detected (DPD)**—R/WC. 0 = Conditions described below **not** met. 1 = The PCH sets this bit when all of the following three conditions are met: • The bridge is the initiator on PCI. • PERR# is detected asserted or a parity error is detected internally • BCTRL.PERE (D30:F0:3E bit 0) is set.
7	Fast Back to Back Capable (FBC)—RO. Hardwired to 1 to indicate that the PCI to PCI target logic is capable of receiving fast back-to-back cycles.
6	Reserved
5	66 MHz Capable (66MHZ_CAP)—RO. Hardwired to 0. This bridge is 33 MHz capable only.
4:0	Reserved

11.1.13 MEMBASE_LIMIT—Memory Base and Limit Register (PCI-PCI—D30:F0)

Offset Address:	20h–23h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

This register defines the base and limit, aligned to a 1-MB boundary, of the non-prefetchable memory area of the bridge. Accesses that are within the ranges specified in this register will be sent to PCI if CMD.MSE is set. Accesses from PCI that are outside the ranges specified will be accepted by the bridge if CMD.BME is set.

Bit	Description
31:20	**Memory Limit** (ML)—R/W. These bits are compared with bits 31:20 of the incoming address to determine the upper 1-MB aligned value (exclusive) of the range. The incoming address must be less than this value.
19:16	Reserved
15:4	**Memory Base** (MB)—R/W. These bits are compared with bits 31:20 of the incoming address to determine the lower 1-MB aligned value (inclusive) of the range. The incoming address must be greater than or equal to this value.
3:0	Reserved

11.1.14 PREF_MEM_BASE_LIMIT—Prefetchable Memory Base and Limit Register (PCI-PCI—D30:F0)

Offset Address:	24h–27h	Attribute:	R/W, RO
Default Value:	00010001h	Size:	32-bit

Defines the base and limit, aligned to a 1-MB boundary, of the prefetchable memory area of the bridge. Accesses that are within the ranges specified in this register will be sent to PCI if CMD.MSE is set. Accesses from PCI that are outside the ranges specified will be accepted by the bridge if CMD.BME is set.

Bit	Description
31:20	**Prefetchable Memory Limit (PML)—**R/W. These bits are compared with bits 31:20 of the incoming address to determine the upper 1-MB aligned value (exclusive) of the range. The incoming address must be less than this value.
19:16	64-bit Indicator (I64L)—RO. Indicates support for 64-bit addressing.
15:4	**Prefetchable Memory Base (PMB)—**R/W. These bits are compared with bits 31:20 of the incoming address to determine the lower 1-MB aligned value (inclusive) of the range. The incoming address must be greater than or equal to this value.
3:0	64-bit Indicator (I64B)—RO. Indicates support for 64-bit addressing.

11.1.15 PMBU32—Prefetchable Memory Base Upper 32 Bits Register (PCI-PCI—D30:F0)

Offset Address:	28h–2Bh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	**Prefetchable Memory Base Upper Portion (PMBU)**—R/W. Upper 32-bits of the prefetchable address base.

11.1.16 PMLU32—Prefetchable Memory Limit Upper 32 Bits Register (PCI-PCI—D30:F0)

Offset Address:	2C–2Fh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	**Prefetchable Memory Limit Upper Portion (PMLU)**—R/W. Upper 32-bits of the prefetchable address limit.

11.1.17 CAPP—Capability List Pointer Register (PCI-PCI—D30:F0)

Offset Address:	34h	Attribute:	RO
Default Value:	50h	Size:	8 bits

Bit	Description
7:0	**Capabilities Pointer (PTR)**—RO. Indicates that the pointer for the first entry in the capabilities list is at 50h in configuration space.

11.1.18 INTR—Interrupt Information Register (PCI-PCI—D30:F0)

Offset Address:	3Ch–3Dh	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:8	**Interrupt Pin (IPIN)**—RO. The PCI bridge does not assert an interrupt.
7:0	**Interrupt Line (ILINE)**—R/W. Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register. Since the bridge does not generate an interrupt, BIOS should program this value to FFh as per the PCI bridge specification.

11.1.19 BCTRL—Bridge Control Register (PCI-PCI—D30:F0)

Offset Address:	3Eh–3Fh	Attribute:	R/WC, RO, R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15:12	Reserved
11	**Discard Timer SERR# Enable (DTE)**—R/W. Controls the generation of SERR# on the primary interface in response to the DTS bit being set: 0 = Do not generate SERR# on a secondary timer discard 1 = Generate SERR# in response to a secondary timer discard
10	**Discard Timer Status (DTS)—**R/WC. This bit is set to 1 when the secondary discard timer (see the SDT bit below) expires for a delayed transaction in the hard state.
9	**Secondary Discard Timer (SDT)**—R/W. This bit sets the maximum number of PCI clock cycles that the PCH waits for an initiator on PCI to repeat a delayed transaction request. The counter starts once the delayed transaction data is has been returned by the system and is in a buffer in the PCH PCI bridge. If the master has not repeated the transaction at least once before the counter expires, the PCH PCI bridge discards the transaction from its queue. 0 = The PCI master timeout value is between 2^{15} and 2^{16} PCI clocks 1 = The PCI master timeout value is between 2^{10} and 2^{11} PCI clocks
8	**Primary Discard Timer (PDT**)—R/W. This bit is R/W for software compatibility only.
7	**Fast Back to Back Enable (FBE)—**RO. Hardwired to 0. The PCI logic will not generate fast back-to-back cycles on the PCI bus.
6	**Secondary Bus Reset (SBR)—**R/W. Controls PCIRST# assertion on PCI. 0 = Bridge deasserts PCIRST# 1 = Bridge asserts PCIRST#. When PCIRST# is asserted, the delayed transaction buffers, posting buffers, and the PCI bus are initialized back to reset conditions. The rest of the part and the configuration registers are not affected.
5	**Master Abort Mode (MAM**)—R/W. Controls the PCH PCI bridge's behavior when a master abort occurs: Master Abort on Processor /PCH Interconnect (DMI): 0 = Bridge asserts TRDY# on PCI. It drives all 1s for reads, and discards data on writes. 1 = Bridge returns a target abort on PCI. Master Abort PCI (non-locked cycles): 0 = Normal completion status will be returned on the Processor/PCH interconnect. 1 = Target abort completion status will be returned on the Processor/PCH interconnect. ***Note:*** All locked reads will return a completer abort completion status on the Processor/PCH interconnect.
4	**VGA 16-Bit Decode (V16D)—**R/W. Enables the PCH PCI bridge to provide 16-bits decoding of VGA I/O address precluding the decode of VGA alias addresses every 1 KB. This bit requires the VGAE bit in this register be set.
3	**VGA Enable (VGAE)**—R/W. When set to a 1, the PCH PCI bridge forwards the following transactions to PCI regardless of the value of the I/O base and limit registers. The transactions are qualified by CMD.MSE (D30:F0:04 bit 1) and CMD.IOSE (D30:F0:04 bit 0) being set. • Memory addresses: 000A0000h–000BFFFFh • I/O addresses: 3B0h–3BBh and 3C0h–3DFh. For the I/O addresses, bits [63:16] of the address must be 0, and bits [15:10] of the address are ignored (that is, aliased). The same holds true from secondary accesses to the primary interface in reverse. That is, when the bit is 0, memory and I/O addresses on the secondary interface between the above ranges will be claimed.
2	**ISA Enable (IE)**—R/W. This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64 KB of PCI I/O space. If this bit is set, the PCH PCI bridge will block any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1-KB block (offsets 100h to 3FFh).
1	**SERR# Enable (SEE)—**R/W. Controls the forwarding of secondary interface SERR# assertions on the primary interface. When set, the PCI bridge will forward SERR# pin. • SERR# is asserted on the secondary interface. • This bit is set. • CMD.SEE (D30:F0:04 bit 8) is set.
0	Parity Error Response Enable (PERE)—R/W. 0 = Disable 1 = The PCH PCI bridge is enabled for parity error reporting based on parity errors on the PCI bus.

11.1.20 SPDH—Secondary PCI Device Hiding Register (PCI-PCI—D30:F0)

Offset Address:	40h–41h	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits

This register allows software to hide the PCI devices, either plugged into slots or on the motherboard.

Bit	Description
15:4	Reserved
3	**Hide Device 3 (HD3)**—R/W, RO. Same as bit 0 of this register, except for device 3 (AD[19])
2	**Hide Device 2 (HD2)—**R/W, RO. Same as bit 0 of this register, except for device 2 (AD[18])
1	**Hide Device 1 (HD1)**—R/W, RO. Same as bit 0 of this register, except for device 1 (AD[17])
0	**Hide Device 0 (HD0)—**R/W, RO. 0 = The PCI configuration cycles for this slot are not affected. 1 = The PCH hides device 0 on the PCI bus. This is done by masking the IDSEL (keeping it low) for configuration cycles to that device. Since the device will not see its IDSEL go active, it will not respond to PCI configuration cycles and the processor will think the device is not present. AD[16] is used as IDSEL for device 0.

11.1.21 DTC—Delayed Transaction Control Register (PCI-PCI—D30:F0)

Offset Address:	44h–47h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31	**Discard Delayed Transactions (DDT)—**R/W. 0 = Logged delayed transactions are kept. 1 = The PCH PCI bridge will discard any delayed transactions it has logged. This includes transactions in the pending queue, and any transactions in the active queue, whether in the hard or soft DT state. The prefetchers will be disabled and return to an idle state. ***Note:*** If a transaction is running on PCI at the time this bit is set, that transaction will continue until either the PCI master disconnects (by deasserting FRAME#) or the PCI bridge disconnects (by asserting STOP#). This bit is cleared by the PCI bridge when the delayed transaction queues are empty and have returned to an idle state. Software sets this bit and polls for its completion
30	**Block Delayed Transactions (BDT)**—R/W. 0 = Delayed transactions accepted 1 = The PCH PCI bridge will not accept incoming transactions which will result in delayed transactions. It will blindly retry these cycles by asserting STOP#. All postable cycles (memory writes) will still be accepted.
29:8	Reserved
7:6	**Maximum Delayed Transactions (MDT)**—R/W. Controls the maximum number of delayed transactions that the PCH PCI bridge will run. Encodings are: 00 =) 2 Active, 5 pending 01 =) 2 active, no pending 10 =) 1 active, no pending 11 =) Reserved
5	Reserved
4	**Auto Flush After Disconnect Enable (AFADE)**—R/W. 0 = The PCI bridge will retain any fetched data until required to discard by producer/consumer rules. 1 = The PCI bridge will flush any prefetched data after either the PCI master (by deasserting FRAME#) or the PCI bridge (by asserting STOP#) disconnects the PCI transfer.

Bit	Description
3	**Never Prefetch (NP)**—R/W. 0 = Prefetch enabled 1 = The PCH will only fetch a single DW and will not enable prefetching, regardless of the command being an Memory read (MR), Memory read line (MRL), or Memory read multiple (MRM).
2	**Memory Read Multiple Prefetch Disable (MRMPD)—**R/W. 0 = MRM commands will fetch multiple cache lines as defined by the prefetch algorithm. 1 = Memory read multiple (MRM) commands will fetch only up to a single, 64-byte aligned cache line.
1	**Memory Read Line Prefetch Disable (MRLPD)—**R/W. 0 = MRL commands will fetch multiple cache lines as defined by the prefetch algorithm. 1 = Memory read line (MRL) commands will fetch only up to a single, 64-byte aligned cache line.
0	**Memory Read Prefetch Disable (MRPD)—**R/W. 0 = MR commands will fetch up to a 64-byte aligned cache line. 1 = Memory read (MR) commands will fetch only a single DW.

11.1.22 BPS—Bridge Proprietary Status Register (PCI-PCI—D30:F0)

Offset Address:	48h–4Bh	Attribute:	R/WC, RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:17	Reserved
16	**PERR# Assertion Detected (PAD)**—R/WC. This bit is set by hardware whenever the PERR# pin is asserted on the rising edge of PCI clock. This includes cases in which the chipset is the agent driving PERR#. It remains asserted until cleared by software writing a 1 to this location. When enabled by the PERR#-to-SERR# Enable bit (in the Bridge Policy Configuration register), a 1 in this bit can generate an internal SERR# and be a source for the NMI logic. This bit can be used by software to determine the source of a system problem.
15:7	Reserved
6:4	**Number of Pending Transactions (NPT)—**RO. This read-only indicator tells debug software how many transactions are in the pending queue. Possible values are: 000 = No pending transaction 001 = 1 pending transaction 010 = 2 pending transactions 011 = 3 pending transactions 100 = 4 pending transactions 101 = 5 pending transactions 110–111 = Reserved ***Note:*** This field is not valid if DTC.MDT (offset 44h:bits 7:6) is any value other than '00'.
3:2	Reserved
1:0	**Number of Active Transactions (NAT)—**RO. This read-only indicator tells debug software how many transactions are in the active queue. Possible values are: 00 = No active transactions 01 = 1 active transaction 10 = 2 active transactions 11 = Reserved

11.1.23 BPC—Bridge Policy Configuration Register (PCI-PCI—D30:F0)

Offset Address:	4Ch–4Fh	Attribute:	R/W
Default Value:	00001200h	Size:	32 bits

Bit	Description
31:30	Reserved
29	**Subtractive Decode Compatibility Device ID (SDCDID)**—R/W. When '0', this function shall report a Device ID of 244Eh. When set to '1', this function shall report the device Device ID value assigned to the PCI-to-PCI Bridge in Section §. If subtractive decode (SDE) is enabled, having this bit as '0' allows the function to present a Device ID that is recognized by the operating system.
28	**Subtractive Decode Enable (SDE)**—R/W. 0 = Subtractive decode is disabled this function and will only claim transactions positively. 1 = The subtractive decode policy as listed in SDP below applies. Software must ensure that only one PCH device is enabled for Subtractive decode at a time.
27:14	Reserved
13:8	**Upstream Read Latency Threshold (URLT)**—R/W. This field specifies the number of PCI clocks after internally enqueuing an upstream memory read request at which point the PCI target logic should insert wait states in order to optimize lead-off latency. When the master returns after this threshold has been reached and data has not arrived in the Delayed Transaction completion queue, then the PCI target logic will insert wait states instead of immediately retrying the cycle. The PCI target logic will insert up to 16 clocks of target initial latency (from FRAME# assertion to TRDY# or STOP# assertion) before retrying the PCI read cycle (if the read data has not arrived yet). Note that the starting event for this Read Latency Timer is not explicitly visible externally. A value of 0h disables this policy completely such that wait states will never be inserted on the read lead-off data phase. The default value (12h) specifies 18 PCI clocks (540 ns) and is approximately 4 clocks less than the typical idle lead-off latency expected for desktop PCH systems. This value may need to be changed by BIOS, depending on the platform.
7	**Subtractive Decode Policy (SDP)**—R/W. 0 = The PCI bridge always forwards memory and I/O cycles that are not claimed by any other device on the backbone (primary interface) to the PCI bus (secondary interface). 1 = The PCI bridge will not claim and forward memory or I/O cycles at all unless the corresponding Space Enable bit is set in the Command register. ***Note:*** The Boot BIOS Destination Selection strap can force the BIOS accesses to PCI. **CMD.MSE** / **BPC.SDP** / **Range** / **Forwarding Policy** 0 / 0 / Don't Care / Forward unclaimed cycles 0 / 1 / Don't Care / Forwarding Prohibited 1 / X / Within range / Positive decode and forward 1 / X / Outside / Subtractive decode & forward
6	**PERR#-to-SERR# Enable (PSE)**—R/W. When this bit is set, a 1 in the PERR# Assertion status bit (in the Bridge Proprietary Status register) will result in an internal SERR# assertion on the primary side of the bridge (if also enabled by the SERR# Enable bit in the primary Command register). SERR# is a source of NMI.
5	**Secondary Discard Timer Testmode (SDTT)—**R/W. 0 = The secondary discard timer expiration will be defined in BCTRL.SDT (D30:F0:3E, bit 9) 1 = The secondary discard timer will expire after 128 PCI clocks.
4:3	Reserved
2	**Peer Decode Enable (PDE)—**R/W. 0 = The PCI bridge assumes that all memory cycles target main memory, and all I/O cycles are not claimed. 1 = The PCI bridge will perform peer decode on any memory or I/O cycle from PCI that falls outside of the memory and I/O window registers
1	Reserved
0	**Received Target Abort SERR# Enable (RTAE)**—R/W. When set, the PCI bridge will report SERR# when PSTS.RTA (D30:F0:06 bit 12) or SSTS.RTA (D30:F0:1E bit 12) are set, and CMD.SEE (D30:F0:04 bit 8) is set.

11.1.24 SVCAP—Subsystem Vendor Capability Register (PCI-PCI—D30:F0)

Offset Address:	50h–51h	Attribute:	RO
Default Value:	000Dh	Size:	16 bits

Bit	Description
15:8	**Next Capability (NEXT)—**RO. Value of 00h indicates this is the last item in the list.
7:0	**Capability Identifier (CID)—**RO. Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

11.1.25 SVID—Subsystem Vendor IDs Register (PCI-PCI—D30:F0)

Offset Address:	54h–57h	Attribute:	R/WO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:16	**Subsystem Identifier (SID)—**R/WO. Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	**Subsystem Vendor Identifier (SVID)—**R/WO. Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

§

12 Gigabit LAN Configuration Registers

12.1 Gigabit LAN Configuration Registers (Gigabit LAN—D25:F0)

Note: Refer to the Intel 82579 datasheet for additional LAN Configuration Status Register information.

Note: Register address locations that are not shown in Table 12-1 should be treated as Reserved.

Table 12-1. Gigabit LAN Configuration Registers Address Map (Gigabit LAN—D25:F0) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0010h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h–0Bh	CC	Class Code	020000h	RO
0Ch	CLS	Cache Line Size	00h	R/W
0Dh	PLT	Primary Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	00h	RO
10h–13h	MBARA	Memory Base Address A	00000000h	R/W, RO
14h–17h	MBARB	Memory Base Address B	00000000h	R/W, RO
18h–1Bh	MBARC	Memory Base Address C	00000001h	R/W, RO
2Ch–2Dh	SVID	Subsystem Vendor ID	See register description	RO
2Eh–2Fh	SID	Subsystem ID	See register description	RO
30h–33h	ERBA	Expansion ROM Base Address	See register description	RO
34h	CAPP	Capabilities List Pointer	C8h	RO
3Ch–3Dh	INTR	Interrupt Information	See register description	R/W, RO
3Eh	MLMG	Maximum Latency/Minimum Grant	00h	RO
C8h–C9h	CLIST1	Capabilities List 1	D001h	RO
CAh–CBh	PMC	PCI Power Management Capability	See register description	RO
CCh–CDh	PMCS	PCI Power Management Control and Status	See register description	R/WC, R/W, RO
CFh	DR	Data Register	See register description	RO
D0h–D1h	CLIST2	Capabilities List 2	E005h	R/WO, RO

Table 12-1. Gigabit LAN Configuration Registers Address Map (Gigabit LAN—D25:F0) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Type
D2h–D3h	MCTL	Message Control	0080h	R/W, RO
D4h–D7h	MADDL	Message Address Low	See register description	R/W
D8h–DBh	MADDH	Message Address High	See register description	R/W
DCh–DDh	MDAT	Message Data	See register description	R/W
E0h–E1h	FLRCAP	Function Level Reset Capability	0009h	RO
E2h–E3h	FLRCLV	Function Level Reset Capability Length and Value	See register description	R/WO, RO
E4h–E5h	DEVCTRL	Device Control	0000h	R/W, RO

12.1.1 VID—Vendor Identification Register (Gigabit LAN—D25:F0)

Address Offset: 00h–01h Attribute: RO
Default Value: 8086h Size: 16 bits

Bit	Description
15:0	**Vendor ID—**RO. This is a 16-bit value assigned to Intel. The field may be auto-loaded from the NVM at address 0Dh during init time depending on the "Load Vendor/Device ID" bit field in NVM word 0Ah with a default value of 8086h.

12.1.2 DID—Device Identification Register (Gigabit LAN—D25:F0)

Address Offset: 02h–03h Attribute: RO
Default Value: See bit description Size: 16 bits

Bit	Description
15:0	**Device ID**—RO. This is a 16-bit value assigned to the PCH Gigabit LAN controller. The field may be auto-loaded from the NVM word 0Dh during initialization time depending on the "Load Vendor/ Device ID" bit field in NVM word 0Ah.

12.1.3 PCICMD—PCI Command Register (Gigabit LAN—D25:F0)

Address Offset:	04h–05h	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable**—R/W. This disables pin-based INTx# interrupts on enabled Hot-Plug and power management events. This bit has no effect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt for Hot-Plug or power management and MSI is not enabled. 1 = Internal INTx# messages will not be generated. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set.
9	Fast Back to Back Enable (FBE)—RO. Hardwired to 0.
8	**SERR# Enable (SEE)**—R/W. 0 = Disable 1 = Enables the Gb LAN controller to generate an SERR# message when PSTS.SSE is set.
7	Wait Cycle Control (WCC)—RO. Hardwired to 0.
6	**Parity Error Response (PER)**—R/W. 0 = Disable. 1 = Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	Palette Snoop Enable (PSE)—RO. Hardwired to 0.
4	Postable Memory Write Enable (PMWE)—RO. Hardwired to 0.
3	Special Cycle Enable (SCE)—RO. Hardwired to 0.
2	**Bus Master Enable (BME)**—R/W. 0 = Disable. All cycles from the device are master aborted 1 = Enable. Allows the root port to forward cycles onto the backbone from a Gigabit LAN* device.
1	**Memory Space Enable (MSE)**—R/W. 0 = Disable. Memory cycles within the range specified by the memory base and limit registers are master aborted on the backbone. 1 = Enable. Allows memory cycles within the range specified by the memory base and limit registers can be forwarded to the Gigabit LAN device.
0	**I/O Space Enable (IOSE)**—R/W. This bit controls access to the I/O space registers. 0 = Disable. I/O cycles within the range specified by the I/O base and limit registers are master aborted on the backbone. 1 = Enable. Allows I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the Gigabit LAN device.

12.1.4 PCISTS—PCI Status Register (Gigabit LAN—D25:F0)

Address Offset:	06h–07h	Attribute:	R/WC, RO
Default Value:	0010h	Size:	16 bits

Bit	Description
15	**Detected Parity Error (DPE)—**R/WC. 0 = No parity error detected. 1 = Set when the Gb LAN controller receives a command or data from the backbone with a parity error. This is set even if PCIMD.PER (D25:F0, bit 6) is not set.
14	**Signaled System Error (SSE)—**R/WC. 0 = No system error signaled. 1 = Set when the Gb LAN controller signals a system error to the internal SERR# logic.
13	**Received Master Abort (RMA)—**R/WC. 0 = Root port has not received a completion with unsupported request status from the backbone. 1 = Set when the GbE LAN controller receives a completion with unsupported request status from the backbone.
12	**Received Target Abort (RTA)—**R/WC. 0 = Root port has not received a completion with completer abort from the backbone. 1 = Set when the Gb LAN controller receives a completion with completer abort from the backbone.
11	**Signaled Target Abort (STA)—**R/WC. 0 = No target abort received. 1 = Set whenever the Gb LAN controller forwards a target abort received from the downstream device onto the backbone.
10:9	DEVSEL# Timing Status (DEV_STS)—RO. Hardwired to '0'.
8	**Master Data Parity Error Detected (DPED)**—R/WC. 0 = No data parity error received. 1 = Set when the Gb LAN Controller receives a completion with a data parity error on the backbone and PCIMD.PER (D25:F0, bit 6) is set.
7	Fast Back to Back Capable (FB2BC)—RO. Hardwired to '0'.
6	Reserved
5	66 MHz Capable—RO. Hardwired to 0.
4	Capabilities List—RO. Hardwired to 1. Indicates the presence of a capabilities list.
3	**Interrupt Status**—RO. Indicates status of Hot-Plug and power management interrupts on the root port that result in INTx# message generation. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of PCICMD.Interrupt Disable bit (D25:F0:04h:bit 10).
2:0	Reserved

12.1.5 RID—Revision Identification Register (Gigabit LAN—D25:F0)

Offset Address:	08h	Attribute:	RO
Default Value:	See bit description	Size:	8 bits

Bit	Description
7:0	**Revision ID**—RO. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Revision ID Register.

12.1.6 CC—Class Code Register (Gigabit LAN—D25:F0)

Address Offset: 09h–0Bh
Default Value: 020000h
Attribute: RO
Size: 24 bits

Bit	Description
23:0	**Class Code**—RO. Identifies the device as an Ethernet Adapter. 020000h = Ethernet Adapter.

12.1.7 CLS—Cache Line Size Register (Gigabit LAN—D25:F0)

Address Offset: 0Ch
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Cache Line Size**—R/W. This field is implemented by PCI devices as a read write field for legacy compatibility purposes but has no impact on any device functionality.

12.1.8 PLT—Primary Latency Timer Register (Gigabit LAN—D25:F0)

Address Offset: 0Dh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Latency Timer (LT)—RO. Hardwired to 0.

12.1.9 HEADTYP—Header Type Register (Gigabit LAN—D25:F0)

Address Offset: 0Eh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Header Type (HT)**—RO. 00h = Indicates this is a single function device.

12.1.10 MBARA—Memory Base Address Register A (Gigabit LAN—D25:F0)

Address Offset:	10h–13h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

The internal CSR registers and memories are accessed as direct memory mapped offsets from the base address register. Software may only access whole DWord at a time.

Bit	Description
31:17	**Base Address (BA)—R/W**. Software programs this field with the base address of this region.
16:4	**Memory Size (MSIZE)—R/W**. Memory size is 128 KB.
3	**Prefetchable Memory (PM)—**RO. The GbE LAN controller does not implement prefetchable memory.
2:1	**Memory Type (MT)**—RO. Set to 00b indicating a 32 bit BAR.
0	**Memory / IO Space (MIOS)**—RO. Set to 0 indicating a Memory Space BAR.

12.1.11 MBARB—Memory Base Address Register B (Gigabit LAN—D25:F0)

Address Offset:	14h–17h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

The internal registers that are used to access the LAN Space in the External FLASH device. Access to these registers are direct memory mapped offsets from the base address register. Software may only access a DWord at a time.

Bit	Description
31:12	**Base Address (BA)—R/W**. Software programs this field with the base address of this region.
11:4	**Memory Size (MSIZE)—R/W**. Memory size is 4 KB.
3	**Prefetchable Memory (PM)**—RO. The Gb LAN controller does not implement prefetchable memory.
2:1	**Memory Type (MT)**—RO. Set to 00b indicating a 32 bit BAR.
0	**Memory / IO Space (MIOS)**—RO. Set to 0 indicating a Memory Space BAR.

12.1.12 MBARC—Memory Base Address Register C (Gigabit LAN—D25:F0)

Address Offset:	18h–1Bh	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

Internal registers, and memories, can be accessed using I/O operations. There are two 4B registers in the I/O mapping window: Addr Reg and Data Reg. Software may only access a DWord at a time.

Bit	Description
31:5	**Base Address (BA)—R/W**. Software programs this field with the base address of this region.
4:1	**I/O Size (IOSIZE)—**RO. I/O space size is 32 Bytes.
0	**Memory / I/O Space (MIOS)—**RO. Set to 1 indicating an I/O Space BAR.

12.1.13 SVID—Subsystem Vendor ID Register (Gigabit LAN—D25:F0)

Address Offset:	2Ch–2Dh	Attribute:	RO
Default Value:	See bit description	Size:	16 bits

Bit	Description
15:0	**Subsystem Vendor ID (SVID)—**RO. This value may be loaded automatically from the NVM Word 0Ch upon power up depending on the "Load Subsystem ID" bit field in NVM word 0Ah. A value of 8086h is default for this field upon power up if the NVM does not respond or is not programmed. All functions are initialized to the same value.

12.1.14 SID—Subsystem ID Register (Gigabit LAN—D25:F0)

Address Offset:	2Eh–2Fh	Attribute:	RO
Default Value:	See bit description	Size:	16 bits

Bit	Description
15:0	**Subsystem ID (SID)**—RO. This value may be loaded automatically from the NVM Word 0Bh upon power up or reset depending on the "Load Subsystem ID" bit field in NVM word 0Ah with a default value of 0000h. This value is loadable from NVM word location 0Ah.

12.1.15 ERBA—Expansion ROM Base Address Register (Gigabit LAN—D25:F0)

Address Offset:	30h–33h	Attribute:	RO
Default Value:	See bit description	Size:	32 bits

Bit	Description
31:0	**Expansion ROM Base Address (ERBA)—**RO. This register is used to define the address and size information for boot-time access to the optional FLASH memory. If no Flash memory exists, this register reports 00000000h.

12.1.16 CAPP—Capabilities List Pointer Register (Gigabit LAN—D25:F0)

Address Offset:	34h	Attribute:	R0
Default Value:	C8h	Size:	8 bits

Bit	Description
7:0	**Capabilities Pointer (PTR)—**RO. Indicates that the pointer for the first entry in the capabilities list is at C8h in configuration space.

12.1.17 INTR—Interrupt Information Register (Gigabit LAN—D25:F0)

Address Offset: 3Ch–3Dh
Attribute: R/W, RO
Default Value: 0100h
Size: 16 bits
Function Level Reset: No

Bit	Description
15:8	**Interrupt Pin (IPIN)—**RO. Indicates the interrupt pin driven by the GbE LAN controller. 01h = The GbE LAN controller implements legacy interrupts on INTA.
7:0	**Interrupt Line (ILINE)—**R/W. Default = 00h. Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

12.1.18 MLMG—Maximum Latency/Minimum Grant Register (Gigabit LAN—D25:F0)

Address Offset: 3Eh
Attribute: RO
Default Value: 00h
Size: 8 bits

Bit	Description
7:0	Maximum Latency/Minimum Grant (MLMG)—RO. Not used. Hardwired to 00h.

12.1.19 CLIST1—Capabilities List Register 1 (Gigabit LAN—D25:F0)

Address Offset: C8h–C9h
Attribute: RO
Default Value: D001h
Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT)—**RO. Value of D0h indicates the location of the next pointer.
7:0	**Capability ID (CID)—**RO. Indicates the linked list item is a PCI Power Management Register.

12.1.20 PMC—PCI Power Management Capabilities Register (Gigabit LAN—D25:F0)

Address Offset: CAh–CBh
Attribute: RO
Default Value: See bit descriptions
Size: 16 bits
Function Level Reset: No (Bits 15:11 only)

Bit	Description
15:11	**PME_Support (PMES)**—RO. This five-bit field indicates the power states in which the function may assert PME#. It depend on PM Ena and AUX-PWR bits in word 0Ah in the NVM: **Condition** / **Function** / **Value** PM Ena=0 / No PME at all states / 0000b PM Ena & AUX-PWR=0 / PME at D0 and D3hot / 01001b PM Ena & AUX-PWR=1 / PME at D0, D3hot and D3cold / 11001b These bits are not reset by Function Level Reset.
10	**D2_Support (D2S)**—RO. The D2 state is not supported.
9	**D1_Support (D1S)—**RO. The D1 state is not supported.

Bit	Description
8:6	**Aux_Current (AC)**—RO. Required current defined in the Data Register.
5	**Device Specific Initialization (DSI)**—RO. Set to 1. The GbE LAN Controller requires its device driver to be executed following transition to the D0 un-initialized state.
4	Reserved
3	PME Clock (PMEC)—RO. Hardwired to 0.
2:0	**Version (VS)**—RO. Hardwired to 010b to indicate support for *Revision 1.1 of the PCI Power Management Specification*.

12.1.21 PMCS—PCI Power Management Control and Status Register (Gigabit LAN—D25:F0)

Address Offset: CCh–CDh
Attribute: R/WC, R/W, RO
Default Value: See bit description
Size: 16 bits
Function Level Reset: No (Bit 8 only)

Bit	Description
15	**PME Status (PMES)—**R/WC. This bit is set to 1 when the function detects a wake-up event independent of the state of the PMEE bit. Writing a 1 will clear this bit.
14:13	**Data Scale (DSC)—**R/W. This field indicates the scaling factor to be used when interpreting the value of the Data register. For the GbE LAN and common functions this field equals 01b (indicating 0.1 watt units) if the PM is enabled in the NVM, and the Data_Select field is set to 0, 3, 4, 7, (or 8 for Function 0). Else it equals 00b. For the manageability functions this field equals 10b (indicating 0.01 watt units) if the PM is enabled in the NVM, and the Data_Select field is set to 0, 3, 4, 7. Else it equals 00b.
12:9	**Data Select (DSL)—**R/W. This four-bit field is used to select which data is to be reported through the Data register (offset CFh) and Data_Scale field. These bits are writeable only when the Power Management is enabled using NVM. 0h = D0 Power Consumption 3h = D3 Power Consumption 4h = D0 Power Dissipation 7h = D3 Power Dissipation 8h = Common Power All other values are reserved.
8	**PME Enable (PMEE)—**R/W. If Power Management is enabled in the NVM, writing a 1 to this register will enable Wakeup. If Power Management is disabled in the NVM, writing a 1 to this bit has no affect, and will not set the bit to 1. This bit is not reset by Function Level Reset.
7:4	Reserved – Returns a value of 0000.
3	**No Soft Reset (NSR)—**RO. Defines if the device executed internal reset on the transition to D0. the LAN controller always reports 0 in this field.
2	Reserved – Returns a value of 0b.
1:0	**Power State (PS)—**R/W. This field is used both to determine the current power state of the GbE LAN Controller and to set a new power state. The values are: 00 = D0 state (default) 01 = Ignored 10 = Ignored 11 = D3 state (Power Management must be enables in the NVM or this cycle will be ignored).

12.1.22 DR—Data Register (Gigabit LAN—D25:F0)

Address Offset: CFh
Attribute: RO
Default Value: See bit description
Size: 8 bits

Bit	Description
7:0	**Reported Data (RD)**—RO. This register is used to report power consumption and heat dissipation. This register is controlled by the Data_Select field in the PMCS (Offset CCh, bits 12:9), and the power scale is reported in the Data_Scale field in the PMCS (Offset CCh, bits 14:13). The data of this field is loaded from the NVM if PM is enabled in the NVM or with a default value of 00h otherwise.

12.1.23 CLIST2—Capabilities List Register 2 (Gigabit LAN—D25:F0)

Address Offset: D0h–D1h
Attribute: R/WO, RO
Default Value: E005h
Size: 16 bits
Function Level Reset: No (Bits 15:8 only)

Bit	Description
15:8	**Next Capability (NEXT)—**R/WO. Value of E0h points to the Function Level Reset capability structure. These bits are not reset by Function Level Reset.
7:0	**Capability ID (CID)—**RO. Indicates the linked list item is a Message Signaled Interrupt Register.

12.1.24 MCTL—Message Control Register (Gigabit LAN—D25:F0)

Address Offset: D2h–D3h
Attribute: R/W, RO
Default Value: 0080h
Size: 16 bits

Bit	Description
15:8	Reserved
7	**64-bit Capable (CID)—**RO. Set to 1 to indicate that the GbE LAN Controller is capable of generating 64-bit message addresses.
6:4	**Multiple Message Enable (MME)—**RO. Returns 000b to indicate that the GbE LAN controller only supports a single message.
3:1	**Multiple Message Capable (MMC)—**RO. The GbE LAN controller does not support multiple messages.
0	**MSI Enable (MSIE)—**R/W. 0 = MSI generation is disabled. 1 = The Gb LAN controller will generate MSI for interrupt assertion instead of INTx signaling.

12.1.25 MADDL—Message Address Low Register (Gigabit LAN—D25:F0)

Address Offset:	D4h–D7h	Attribute:	R/W
Default Value:	See bit description	Size:	32 bits

Bit	Description
31:0	**Message Address Low (MADDL)—**R/W. Written by the system to indicate the lower 32 bits of the address to use for the MSI memory write transaction. The lower two bits will always return 0 regardless of the write operation.

12.1.26 MADDH—Message Address High Register (Gigabit LAN—D25:F0)

Address Offset:	D8h–DBh	Attribute:	R/W
Default Value:	See bit description	Size:	32 bits

Bit	Description
31:0	**Message Address High (MADDH)—**R/W. Written by the system to indicate the upper 32 bits of the address to use for the MSI memory write transaction.

12.1.27 MDAT—Message Data Register (Gigabit LAN—D25:F0)

Address Offset:	DCh–DDh	Attribute:	R/W
Default Value:	See bit description	Size:	16 bits

Bit	Description
31:0	**Message Data (MDAT)—**R/W. Written by the system to indicate the lower 16 bits of the data written in the MSI memory write DWORD transaction. The upper 16 bits of the transaction are written as 0000h.

12.1.28 FLRCAP—Function Level Reset Capability (Gigabit LAN—D25:F0)

Address Offset:	E0h–E1h	Attribute:	RO
Default Value:	0009h	Size:	16 bits

Bit	Description
15:8	**Next Pointer—**RO. This field provides an offset to the next capability item in the capability list. The value of 00h indicates the last item in the list.
7:0	**Capability ID—**RO. The value of this field depends on the FLRCSSEL bit. 13h = If FLRCSSEL = 0 09h = If FLRCSSEL = 1, indicating vendor specific capability.

12.1.29 FLRCLV—Function Level Reset Capability Length and Version (Gigabit LAN—D25:F0)

Address Offset: E2h–E3h Attribute: R/WO, RO
Default Value: See Description. Size: 16 bits
Function Level Reset: No (Bits 9:8 Only When FLRCSSEL = 0)

When FLRCSSEL = 0, this register is defined as follows:

Bit	Description
15:10	Reserved.
9	**Function Level Reset Capability**—R/WO. 1 = Support for Function Level Reset. This bit is not reset by Function Level Reset.
8	**TXP Capability**—R/WO. 1 = Indicates support for the Transactions Pending (TXP) bit. TXP must be supported if FLR is supported.
7:0	**Capability Length**—RO. The value of this field indicates the number of bytes of the vendor specific capability as require by the PCI specification. It has the value of 06h for the Function Level Reset capability.

When FLRCSSEL = 1, this register is defined as follows:

Bit	Description
15:12	**Vendor Specific Capability ID**—RO. A value of 2h in this field identifies this capability as Function Level Reset.
11:8	**Capability Version**—RO. The value of this field indicates the version of the Function Level Reset Capability. Default is 0h.
7:0	**Capability Length**—RO. The value of this field indicates the number of bytes of the vendor specific capability as require by the PCI specification. It has the value of 06h for the Function Level Reset capability.

12.1.30 DEVCTRL—Device Control (Gigabit LAN—D25:F0)

Address Offset: E4–E5h Attribute: R/W, RO
Default Value: 0000h Size: 16 bits

Bit	Description
15:9	Reserved.
8	**Transactions Pending (TXP)**—R/W. 1 = Indicates the controller has issued Non-Posted requests which have not been completed. 0 = Indicates that completions for all Non-Posted requests have been received.
7:1	Reserved
0	**Initiate Function Level Reset**—RO. This bit is used to initiate an FLT transition. A write of 1 initiates the transition. Since hardware must not respond to any cycles until Function Level Reset completion, the value read by software from this bit is 0.

12.2 Gigabit LAN Capabilities and Status Registers (CSR)

The internal CSR registers and memories are accessed as direct memory mapped offsets from the base address register in Section 12.1.10, "MBARA—Memory Base Address Register A (Gigabit LAN—D25:F0)" on page 330. Software may only access whole DWord at a time.

Note: Register address locations that are not shown in Table 12-2 should be treated as Reserved.

Table 12-2. Gigabit LAN Capabilities and Status Registers Address Map (Gigabit LAN —MBARA)

MBARA + Offset	Mnemonic	Register Name	Default	Attribute
00h-03h	GBECSR1	Gigabit Ethernet Capabilities and Status Register 1	00100241h	R/W
18h-1Bh	GBECSR2	Gigabit Ethernet Capabilities and Status Register 2	01501000h	R/W/SN
20h-23h	GBECSR3	Gigabit Ethernet Capabilities and Status Register 3	1000XXXXh	R/W/V
2Ch-2Fh	GBECSR4	Gigabit Ethernet Capabilities and Status Register 4	00000000h	R/W
F00h-F03h	GBECSR5	Gigabit Ethernet Capabilities and Status Register 5	00010008h	R/W/V
F10h-F13h	GBECSR6	Gigabit Ethernet Capabilities and Status Register 6	0004000Ch	R/W/SN
5400h-5403h	GBECSR7	Gigabit Ethernet Capabilities and Status Register 7	XXXXXXXXh	R/W
5404h-5407h	GBECSR8	Gigabit Ethernet Capabilities and Status Register 8	XXXXXXXXh	R/W
5800h-5803h	GBECSR9	Gigabit Ethernet Capabilities and Status Register 9	00000008h	R/W/SN

12.2.1 GBECSR1—Gigabit Ethernet Capabilities and Status Register 1

Address Offset: MBARA + 00h Attribute: R/W
Default Value: 00100241h Size: 32 bit

Bit	Description
31:25	Reserved
24	**PHY Power Down (PHYPDN)** — R/W. When cleared (0b), the PHY power down setting is controlled by the internal logic of PCH.
23:0	Reserved

12.2.2 GBECSR2—Gigabit Ethernet Capabilities and Status Register 2

Address Offset: MBARA + 18h
Default Value: 01501000h
Attribute: R/W/SN
Size: 32 bit

Bit	Description
31:21	Reserved
20	**PHY Power Down Enable (PHYPDEN)** — R/W/SN. When set, this bit enables the PHY to enter a low-power state when the LAN controller is at the DMoff/D3 or with no WOL.
19:0	Reserved

12.2.3 GBECSR3—Gigabit Ethernet Capabilities and Status Register 3

Address Offset: MBARA + 20h
Default Value: 1000XXXXh
Attribute: R/W/V
Size: 32 bit

Bit	Description
31:29	Reserved
28	**Ready Bit (RB)** — R/W/V. Set to 1 by the Gigabit Ethernet Controller at the end of the MDI transaction. This bit should be reset to 0 by software at the same time the command is written.
27:26	**MDI Type — R/W/V.** 01 = MDI Write 10 = MDI Read All other values are reserved.
25:21	**LAN Connected Device Address (PHYADD)** — R/W/V.
20:16	**LAN Connected Device Register Address (PHYREGADD)** — R/W/V.
15:0	**DATA** — R/W/V.

12.2.4 GBECSR4—Gigabit Ethernet Capabilities and Status Register 4

Address Offset: MBARA + 2Ch
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31	**WOL Indication Valid (WIV)** — R/W. Set to 1 by BIOS to indicate that the WOL indication setting in bit 30 of this register is valid.
30	**WOL Enable Setting by BIOS (WESB)** — R/W. 1 = WOL Enabled in BIOS. 0 = WOL Disabled in BIOS.
29:0	Reserved

12.2.5 GBECSR5—Gigabit Ethernet Capabilities and Status Register 5

Address Offset:	MBARA + F00h	Attribute:	R/W/V
Default Value:	00010008h	Size:	32 bits

Bit	Description
31:6	Reserved
5	**SW Semaphore FLAG (SWFLAG)** — R/W/V. This bit is set by the device driver to gain access permission to shared CSR registers with the firmware and hardware.
4:0	Reserved

12.2.6 GBECSR6—Gigabit Ethernet Capabilities and Status Register 6

Address Offset:	MBARA + F10h	Attribute:	R/W/SN
Default Value:	0004000Ch	Size:	32 bits

Bit	Description
31:7	Reserved
6	**Global GbE Disable (GGD)**— R/W/SN. Prevents the PHY from autonegotiating 1000Mb/s link in all power states.
5:4	Reserved
3	**GbE Disable at non D0a** — R/W/SN. Prevents the PHY from autonegotiating 1000Mb/s link in all power states except D0a. This bit must be set since GbE is not supported in Sx states.
2	**LPLU in non D0a (LPLUND)** — R/W/SN. Enables the PHY to negotiate for the slowest possible link in all power states except D0a.
1	**LPLU in D0a (LPLUD)** — R/W/SN. Enables the PHY to negotiate for the slowest possible link in all power states. This bit overrides bit 2.
0	Reserved

12.2.7 GBECSR7—Gigabit Ethernet Capabilities and Status Register 7

Address Offset:	MBARA + 5400h	Attribute:	R/W
Default Value:	XXXXXXXXh	Size:	32 bits

Bit	Description
31:0	**Receive Address Low (RAL)**— R/W. The lower 32 bits of the 48 bit Ethernet Address.

12.2.8 GBECSR8—Gigabit Ethernet Capabilities and Status Register 8

Address Offset:	MBARA + 5404h	Attribute:	R/W
Default Value:	XXXXXXXXh	Size:	32 bits

Bit	Description
31	**Address Valid**— R/W.
30:16	Reserved
15:0	**Receive Address High (RAH)**— R/W. The lower 16 bits of the 48 bit Ethernet Address.

12.2.9 GBECSR9—Gigabit Ethernet Capabilities and Status Register 9

Address Offset:	MBARA + 5800h	Attribute:	R/W/SN
Default Value:	00000008h	Size:	32 bits

Bit	Description
31:1	Reserved
0	**Advanced Power Management Enable (APME)** — R/W/SN. 1 = APM Wakeup is enabled 0 = APM Wakeup is disabled

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13 LPC Interface Bridge Registers (D31:F0)

The LPC bridge function of the PCH resides in PCI Device 31:Function 0. This function contains many other functional units, such as DMA and Interrupt controllers, Timers, Power Management, System Management, GPIO, RTC, and LPC Configuration Registers.

Registers and functions associated with other functional units are described in their respective sections.

13.1 PCI Configuration Registers (LPC I/F—D31:F0)

Note: Address locations that are not shown should be treated as Reserved.

Table 13-1. LPC Interface PCI Register Address Map (LPC I/F—D31:F0) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0007h	R/W, RO
06h–07h	PCISTS	PCI Status	0210h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	01h	RO
0Bh	BCC	Base Class Code	06h	RO
0Dh	PLT	Primary Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	80h	RO
2Ch–2Fh	SS	Sub System Identifiers	00000000h	R/WO
34h	CAPP	Capability List Pointer	E0h	RO
40h–43h	PMBASE	ACPI Base Address	00000001h	R/W, RO
44h	ACPI_CNTL	ACPI Control	00h	R/W
48h–4Bh	GPIOBASE	GPIO Base Address	00000001h	R/W, RO
4C	GC	GPIO Control	00h	R/W
60h–63h	PIRQ[*n*]_ROUT	PIRQ[A–D] Routing Control	80808080h	R/W
64h	SIRQ_CNTL	Serial IRQ Control	10h	R/W, RO
68h–6Bh	PIRQ[*n*]_ROUT	PIRQ[E–H] Routing Control	80808080h	R/W
6Ch–6Dh	LPC_IBDF	IOxAPIC Bus:Device:Function	00F8h	R/W
70h–7Fh	**LPC_HnBDF**	HPET Configuration	00F8h	R/W
80h	LPC_I/O_DEC	I/O Decode Ranges	0000h	R/W
82h–83h	LPC_EN	LPC I/F Enables	0000h	R/W
84h–87h	GEN1_DEC	LPC I/F Generic Decode Range 1	00000000h	R/W
88h–8Bh	GEN2_DEC	LPC I/F Generic Decode Range 2	00000000h	R/W
8Ch–8Eh	GEN3_DEC	LPC I/F Generic Decode Range 3	00000000h	R/W

Table 13-1. LPC Interface PCI Register Address Map (LPC I/F—D31:F0) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Type
90h–93h	GEN4_DEC	LPC I/F Generic Decode Range 4	00000000h	R/W
94h–97h	ULKMC	USB Legacy Keyboard / Mouse Control		
98h–9Bh	LGMR	LPC Generic Memory Range	00000000h	R/W
A0h–CFh		Power Management (See Section 13.8.1)		
D0h–D3h	BIOS_SEL1	BIOS Select 1	00112233h	R/W, RO
D4h–D5h	BIOS_SEL2	BIOS Select 2	4567h	R/W
D8h–D9h	BIOS_DEC_EN1	BIOS Decode Enable 1	FFCFh	R/W, RO
DCh	BIOS_CNTL	BIOS Control	00h	R/WLO, R/W, RO
E0h–E1h	FDCAP	Feature Detection Capability ID	0009h	RO
E2h	FDLEN	Feature Detection Capability Length	0Ch	RO
E3h	FDVER	Feature Detection Version	10h	RO
E4h–EBh	FDVCT	Feature Vector	See Description	RO
F0h–F3h	RCBA	Root Complex Base Address	00000000h	R/W

13.1.1 VID—Vendor Identification Register (LPC I/F—D31:F0)

Offset Address: 00h–01h
Default Value: 8086h
Lockable: No
Attribute: RO
Size: 16-bit
Power Well: Core

Bit	Description
15:0	**Vendor ID**—RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

13.1.2 DID—Device Identification Register (LPC I/F—D31:F0)

Offset Address: 02h–03h
Default Value: See bit description
Lockable: No
Attribute: RO
Size: 16-bit
Power Well: Core

Bit	Description
15:0	**Device ID—**RO. This is a 16-bit value assigned to the PCH LPC bridge. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Device ID Register.

13.1.3 PCICMD—PCI COMMAND Register (LPC I/F—D31:F0)

Offset Address:	04h–05h	Attribute:	R/W, RO
Default Value:	0007h	Size:	16-bit
Lockable:	No	Power Well:	Core

Bit	Description
15:10	Reserved
9	Fast Back to Back Enable (FBE)—RO. Hardwired to 0.
8	**SERR# Enable (SERR_EN)—**R/W. The LPC bridge generates SERR# if this bit is set.
7	Wait Cycle Control (WCC)—RO. Hardwired to 0.
6	**Parity Error Response Enable (PERE)—**R/W. 0 = No action is taken when detecting a parity error. 1 = Enables the PCH LPC bridge to respond to parity errors detected on backbone interface.
5	VGA Palette Snoop (VPS)—RO. Hardwired to 0.
4	Memory Write and Invalidate Enable (MWIE)—RO. Hardwired to 0.
3	Special Cycle Enable (SCE)—RO. Hardwired to 0.
2	Bus Master Enable (BME)—RO. Bus Masters cannot be disabled.
1	Memory Space Enable (MSE)—RO. Memory space cannot be disabled on LPC.
0	I/O Space Enable (IOSE)—RO. I/O space cannot be disabled on LPC.

13.1.4 PCISTS—PCI Status Register (LPC I/F—D31:F0)

Offset Address:	06h–07h	Attribute:	RO, R/WC
Default Value:	0210h	Size:	16-bit
Lockable:	No	Power Well:	Core

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)—**R/WC. Set when the LPC bridge detects a parity error on the internal backbone. Set even if the PCICMD.PERE bit (D31:F0:04, bit 6) is 0. 0 = Parity Error Not detected. 1 = Parity Error detected.
14	**Signaled System Error (SSE)**—R/WC. Set when the LPC bridge signals a system error to the internal SERR# logic.
13	**Master Abort Status (RMA)—**R/WC. 0 = Unsupported request status not received. 1 = The bridge received a completion with unsupported request status from the backbone.
12	**Received Target Abort (RTA)—**R/WC. 0 = Completion abort not received. 1 = Completion with completion abort received from the backbone.
11	**Signaled Target Abort (STA)—**R/WC. 0 = Target abort Not generated on the backbone. 1 = LPC bridge generated a completion packet with target abort status on the backbone.
10:9	**DEVSEL# Timing Status (DEV_STS)—**RO. 01 = Medium Timing.
8	**Data Parity Error Detected (DPED)—**R/WC. 0 = All conditions listed below Not met. 1 = Set when all three of the following conditions are met: • LPC bridge receives a completion packet from the backbone from a previous request, • Parity error has been detected (D31:F0:06, bit 15) • PCICMD.PERE bit (D31:F0:04, bit 6) is set.

Bit	Description
7	Fast Back to Back Capable (FBC): Reserved – bit has no meaning on the internal backbone.
6	Reserved.
5	66 MHz Capable (66MHZ_CAP)—Reserved – bit has no meaning on the internal backbone.
4	**Capabilities List (CLIST)—**RO. Capability list exists on the LPC bridge.
3	**Interrupt Status (IS)**—RO. The LPC bridge does not generate interrupts.
2:0	Reserved.

13.1.5 RID—Revision Identification Register (LPC I/F—D31:F0)

Offset Address: 08h Attribute: R/WO
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	**Revision ID (RID)—**R/WO. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Revision ID Register.

13.1.6 PI—Programming Interface Register (LPC I/F—D31:F0)

Offset Address: 09h Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Programming Interface**—RO.

13.1.7 SCC—Sub Class Code Register (LPC I/F—D31:F0)

Offset Address: 0Ah Attribute: RO
Default Value: 01h Size: 8 bits

Bit	Description
7:0	**Sub Class Code**—RO. 8-bit value that indicates the category of bridge for the LPC bridge. 01h = PCI-to-ISA bridge.

13.1.8 BCC—Base Class Code Register (LPC I/F—D31:F0)

Offset Address: 0Bh Attribute: RO
Default Value: 06h Size: 8 bits

Bit	Description
7:0	**Base Class Code**—RO. 8-bit value that indicates the type of device for the LPC bridge. 06h = Bridge device.

13.1.9 PLT—Primary Latency Timer Register (LPC I/F—D31:F0)

Offset Address: 0Dh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:3	Master Latency Count (MLC)—Reserved.
2:0	Reserved.

13.1.10 HEADTYP—Header Type Register (LPC I/F—D31:F0)

Offset Address: 0Eh Attribute: RO
Default Value: 80h Size: 8 bits

Bit	Description
7	**Multi-Function Device—**RO. This bit is 1 to indicate a multi-function device.
6:0	**Header Type—**RO. This 7-bit field identifies the header layout of the configuration space.

13.1.11 SS—Sub System Identifiers Register (LPC I/F—D31:F0)

Offset Address: 2Ch–2Fh Attribute: R/WO
Default Value: 00000000h Size: 32 bits

This register is initialized to logic 0 by the assertion of PLTRST#. This register can be written only once after PLTRST# deassertion.

Bit	Description
31:16	**Subsystem ID (SSID)—**R/WO. This is written by BIOS. No hardware action taken on this value.
15:0	**Subsystem Vendor ID (SSVID)—**R/WO. This is written by BIOS. No hardware action taken on this value.

13.1.12 CAPP—Capability List Pointer Register (LPC I/F—D31:F0)

Offset Address: 34h Attribute: RO
Default Value: E0h Size: 8 bits

Bit	Description
7:0	**Capability Pointer (CP)**—RO. This field indicates the offset of the first Capability Item.

13.1.13 PMBASE—ACPI Base Address Register (LPC I/F—D31:F0)

Offset Address:	40h–43h	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bit
Lockable:	No	Usage:	ACPI, Legacy
		Power Well:	Core

Sets base address for ACPI I/O registers, GPIO registers and TCO I/O registers. These registers can be mapped anywhere in the 64-K I/O space on 128-byte boundaries.

Bit	Description
31:16	Reserved
15:7	**Base Address**—R/W. This field provides 128 bytes of I/O space for ACPI, GPIO, and TCO logic. This is placed on a 128-byte boundary.
6:1	Reserved
0	Resource Type Indicator (RTE)—RO. Hardwired to 1 to indicate I/O space.

13.1.14 ACPI_CNTL—ACPI Control Register (LPC I/F—D31:F0)

Offset Address:	44h	Attribute:	R/W
Default Value:	00h	Size:	8 bit
Lockable:	No	Usage:	ACPI, Legacy
		Power Well:	Core

Bit	Description
7	**ACPI Enable (ACPI_EN)—**R/W. 0 = Disable. 1 = Decode of the I/O range pointed to by the ACPI base register is enabled, and the ACPI power management function is enabled. Note that the APM power management ranges (B2/B3h) are always enabled and are not affected by this bit.
6:3	Reserved
2:0	**SCI IRQ Select (SCI_IRQ_SEL)—**R/W. Specifies on which IRQ the SCI will internally appear. If not using the APIC, the SCI must be routed to IRQ9–11, and that interrupt is not sharable with the SERIRQ stream, but is shareable with other PCI interrupts. If using the APIC, the SCI can also be mapped to IRQ20–23, and can be shared with other interrupts. **Bits** — **SCI Map** 000b — IRQ9 001b — IRQ10 010b — IRQ11 011b — Reserved 100b — IRQ20 (Only available if APIC enabled) 101b — IRQ21 (Only available if APIC enabled) 110b — IRQ22 (Only available if APIC enabled) When the interrupt is mapped to APIC interrupts 9, 10 or 11, the APIC should be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, the APIC should be programmed for active-low reception.

13.1.15 GPIOBASE—GPIO Base Address Register (LPC I/F—D31:F0)

Offset Address:	48h–4Bh	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bit

Bit	Description
31:16	Reserved. Always 0.
15:7	**Base Address (BA)—**R/W. Provides the 128 bytes of I/O space for GPIO.
6:1	Reserved. Always 0.
0	RO. Hardwired to 1 to indicate I/O space.

13.1.16 GC—GPIO Control Register (LPC I/F—D31:F0)

Offset Address:	4Ch	Attribute:	R/W
Default Value:	00h	Size:	8 bit

Bit	Description
7:5	Reserved.
4	**GPIO Enable (EN)—**R/W. This bit enables/disables decode of the I/O range pointed to by the GPIO Base Address register (D31:F0:48h) and enables the GPIO function. 0 = Disable. 1 = Enable.
3:1	Reserved.
0	**GPIO Lockdown Enable (GLE)**—R/W. This bit enables lockdown of the following GPIO registers: • Offset 00h: GPIO_USE_SEL • Offset 04h: GP_IO_SEL • Offset 0Ch: GP_LVL • Offset 30h: GPIO_USE_SEL2 • Offset 34h: GP_IO_SEL2 • Offset 38h: GP_LVL2 • Offset 40h: GPIO_USE_SEL3 • Offset 44h: GP_IO_SEL3 • Offset 48h: GP_LVL3 • Offset 60h: GP_RST_SEL 0 = Disable. 1 = Enable. When this bit is written from a 1-to-0, an SMI# is generated, if enabled. This ensures that only SMM code can change the above GPIO registers after they are locked down.

13.1.17 PIRQ[n]_ROUT—PIRQ[A,B,C,D] Routing Control Register (LPC I/F—D31:F0)

Offset Address:	PIRQA – 60h, PIRQB – 61h, PIRQC – 62h, PIRQD – 63h	Attribute:	R/W
Default Value:	80h	Size:	8 bit
Lockable:	No	Power Well:	Core

Bit	Description
7	**Interrupt Routing Enable (IRQEN)—**R/W. 0 = The corresponding PIRQ is routed to one of the ISA-compatible interrupts specified in bits[3:0]. 1 = The PIRQ is not routed to the 8259. ***Note:*** BIOS must program this bit to 0 during POST for any of the PIRQs that are being used. The value of this bit may subsequently be changed by the operating system when setting up for I/O APIC interrupt delivery mode.
6:4	Reserved
3:0	**IRQ Routing**—R/W. (ISA compatible.) Value / IRQ / Value / IRQ 0000b Reserved 1000b Reserved 0001b Reserved 1001b IRQ9 0010b Reserved 1010b IRQ10 0011b IRQ3 1011b IRQ11 0100b IRQ4 1100b IRQ12 0101b IRQ5 1101b Reserved 0110b IRQ6 1110b IRQ14 0111b IRQ7 1111b IRQ15

13.1.18 SIRQ_CNTL—Serial IRQ Control Register (LPC I/F—D31:F0)

Offset Address:	64h	Attribute:	R/W, RO
Default Value:	10h	Size:	8 bit
Lockable:	No	Power Well:	Core

Bit	Description
7	**Serial IRQ Enable (SIRQEN)—**R/W. 0 = The buffer is input only and internally SERIRQ will be a 1. 1 = Serial IRQs will be recognized. The SERIRQ pin will be configured as SERIRQ.
6	**Serial IRQ Mode Select (SIRQMD)—**R/W. 0 = The serial IRQ machine will be in quiet mode. 1 = The serial IRQ machine will be in continuous mode. ***Note:*** For systems using Quiet Mode, this bit should be set to 1 (Continuous Mode) for at least one frame after coming out of reset before switching back to Quiet Mode. Failure to do so will result in the PCH not recognizing SERIRQ interrupts.
5:2	**Serial IRQ Frame Size (SIRQSZ)—**RO. Fixed field that indicates the size of the SERIRQ frame as 21 frames.
1:0	**Start Frame Pulse Width (SFPW)—**R/W. This is the number of PCI clocks that the SERIRQ pin will be driven low by the serial IRQ machine to signal a start frame. In continuous mode, the PCH will drive the start frame for the number of clocks specified. In quiet mode, the PCH will drive the start frame for the number of clocks specified minus one, as the first clock was driven by the peripheral. 00 = 4 clocks 01 = 6 clocks 10 = 8 clocks 11 = Reserved

13.1.19 PIRQ[n]_ROUT—PIRQ[E,F,G,H] Routing Control Register (LPC I/F—D31:F0)

Offset Address:	PIRQE – 68h, PIRQF – 69h, PIRQG – 6Ah, PIRQH – 6Bh	Attribute:	R/W
Default Value:	80h	Size:	8 bit
Lockable:	No	Power Well:	Core

Bit	Description
7	**Interrupt Routing Enable (IRQEN)—**R/W. 0 = The corresponding PIRQ is routed to one of the ISA-compatible interrupts specified in bits[3:0]. 1 = The PIRQ is not routed to the 8259. ***Note:*** BIOS must program this bit to 0 during POST for any of the PIRQs that are being used. The value of this bit may subsequently be changed by the operating system when setting up for I/O APIC interrupt delivery mode.
6:4	Reserved
3:0	**IRQ Routing**—R/W. (ISA compatible.) Value / IRQ / Value / IRQ 0000b Reserved 1000b Reserved 0001b Reserved 1001b IRQ9 0010b Reserved 1010b IRQ10 0011b IRQ3 1011b IRQ11 0100b IRQ4 1100b IRQ12 0101b IRQ5 1101b Reserved 0110b IRQ6 1110b IRQ14 0111b IRQ7 1111b IRQ15

13.1.20 LPC_IBDF—IOxAPIC Bus:Device:Function Register (LPC I/F—D31:F0)

Offset Address:	6Ch–6Dh	Attribute:	R/W
Default Value:	00F8h	Size:	16 bit

Bit	Description
15:0	**IOxAPIC Bus:Device:Function (IBDF)**—R/W. this field specifies the bus:device:function that PCH's IOxAPIC will be using for the following: • As the Requester ID when initiating Interrupt Messages to the processor. • As the Completer ID when responding to the reads targeting the IOxAPIC's Memory-Mapped I/O registers. The 16-bit field comprises the following: Bits / Description 15:8 Bus Number 7:3 Device Number 2:0 Function Number This field defaults to Bus 0: Device 31: Function 0 after reset. BIOS can program this field to provide a unique bus:device:function number for the internal IOxAPIC.

13.1.21 LPC_HnBDF—HPET n Bus:Device:Function Register (LPC I/F—D31:F0)

Address Offset	H0BDF 70h–71h H1BDF 72h–73h H2BDF 74h–75h H3BDF 76h–77h H4BDF 78h–79h H5BDF 7Ah–7Bh H6BDF 7Ch–7Dh H7BDF 7Eh–7Fh	Attribute:	R/W
Default Value:	00F8h	Size:	16 bit

Bit	Description
15:0	**HPET n Bus:Device:Function (HnBDF)**—R/W. This field specifies the bus:device:function that the PCH's HPET n will be using in the following: • As the Requester ID when initiating Interrupt Messages to the processor • As the Completer ID when responding to the reads targeting the corresponding HPET's Memory-Mapped I/O registers The 16-bit field comprises the following: **Bits** / **Description** 15:8 — Bus Number 7:3 — Device Number 2:0 — Function Number This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required for the corresponding HPET.

13.1.22 LPC_I/O_DEC—I/O Decode Ranges Register (LPC I/F—D31:F0)

Offset Address: 80h Attribute: R/W
Default Value: 0000h Size: 16 bit

Bit	Description
15:13	Reserved
12	**FDD Decode Range**—R/W. Determines which range to decode for the FDD Port 0 = 3F0h–3F5h, 3F7h (Primary) 1 = 370h–375h, 377h (Secondary)
11:10	Reserved
9:8	**LPT Decode Range**—R/W. This field determines which range to decode for the LPT Port. 00 = 378h–37Fh and 778h–77Fh 01 = 278h–27Fh (port 279h is read only) and 678h–67Fh 10 = 3BCh –3BEh and 7BCh–7BEh 11 = Reserved
7	Reserved
6:4	**COMB Decode Range**—R/W. This field determines which range to decode for the COMB Port. 000 = 3F8h–3FFh (COM1) 001 = 2F8h–2FFh (COM2) 010 = 220h–227h 011 = 228h–22Fh 100 = 238h–23Fh 101 = 2E8h–2EFh (COM4) 110 = 338h–33Fh 111 = 3E8h–3EFh (COM3)
3	Reserved
2:0	**COMA Decode Range**—R/W. This field determines which range to decode for the COMA Port. 000 = 3F8h–3FFh (COM1) 001 = 2F8h–2FFh (COM2) 010 = 220h–227h 011 = 228h–22Fh 100 = 238h–23Fh 101 = 2E8h–2EFh (COM4) 110 = 338h–33Fh 111 = 3E8h–3EFh (COM3)

13.1.23 LPC_EN—LPC I/F Enables Register (LPC I/F—D31:F0)

Offset Address:	82h – 83h	Attribute:	R/W
Default Value:	0000h	Size:	16 bit
		Power Well:	Core

Bit	Description
15:14	Reserved
13	**CNF2_LPC_EN**—R/W. Microcontroller Enable # 2. 0 = Disable. 1 = Enables the decoding of the I/O locations 4Eh and 4Fh to the LPC interface. This range is used for a microcontroller.
12	**CNF1_LPC_EN**—R/W. Super I/O Enable. 0 = Disable. 1 = Enables the decoding of the I/O locations 2Eh and 2Fh to the LPC interface. This range is used for Super I/O devices.
11	**MC_LPC_EN**—R/W. Microcontroller Enable # 1. 0 = Disable. 1 = Enables the decoding of the I/O locations 62h and 66h to the LPC interface. This range is used for a microcontroller.
10	**KBC_LPC_EN**—R/W. Keyboard Enable. 0 = Disable. 1 = Enables the decoding of the I/O locations 60h and 64h to the LPC interface. This range is used for a microcontroller.
9	**GAMEH_LPC_EN**—R/W. High Gameport Enable 0 = Disable. 1 = Enables the decoding of the I/O locations 208h to 20Fh to the LPC interface. This range is used for a gameport.
8	**GAMEL_LPC_EN**—R/W. Low Gameport Enable 0 = Disable. 1 = Enables the decoding of the I/O locations 200h to 207h to the LPC interface. This range is used for a gameport.
7:4	Reserved
3	**FDD_LPC_EN**—R/W. Floppy Drive Enable 0 = Disable. 1 = Enables the decoding of the FDD range to the LPC interface. This range is selected in the LPC_FDD/LPT Decode Range Register (D31:F0:80h, bit 12).
2	**LPT_LPC_EN**—R/W. Parallel Port Enable 0 = Disable. 1 = Enables the decoding of the LPTrange to the LPC interface. This range is selected in the LPC_FDD/LPT Decode Range Register (D31:F0:80h, bit 9:8).
1	**COMB_LPC_EN**—R/W. Com Port B Enable 0 = Disable. 1 = Enables the decoding of the COMB range to the LPC interface. This range is selected in the LPC_COM Decode Range Register (D31:F0:80h, bits 6:4).
0	**COMA_LPC_EN**—R/W. Com Port A Enable 0 = Disable. 1 = Enables the decoding of the COMA range to the LPC interface. This range is selected in the LPC_COM Decode Range Register (D31:F0:80h, bits 3:2).

13.1.24 GEN1_DEC—LPC I/F Generic Decode Range 1 Register (LPC I/F—D31:F0)

Offset Address:	84h – 87h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bit
		Power Well:	Core

Bit	Description
31:24	Reserved
23:18	**Generic I/O Decode Range Address[7:2] Mask—**R/W. A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	Reserved
15:2	**Generic I/O Decode Range 1 Base Address (GEN1_BASE)—**R/W. ***Note:*** The PCH Does not provide decode down to the word or byte level
1	Reserved
0	**Generic Decode Range 1 Enable (GEN1_EN)—**R/W. 0 = Disable. 1 = Enable the GEN1 I/O range to be forwarded to the LPC I/F

13.1.25 GEN2_DEC—LPC I/F Generic Decode Range 2 Register (LPC I/F—D31:F0)

Offset Address:	88h – 8Bh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bit
		Power Well:	Core

Bit	Description
31:24	Reserved
23:18	**Generic I/O Decode Range Address[7:2] Mask—**R/W. A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	Reserved
15:2	**Generic I/O Decode Range 2 Base Address (GEN1_BASE)—**R/W. ***Note:*** The PCH does not provide decode down to the word or byte level
1	Reserved
0	**Generic Decode Range 2 Enable (GEN2_EN)—**R/W. 0 = Disable. 1 = Enable the GEN2 I/O range to be forwarded to the LPC I/F

13.1.26 GEN3_DEC—LPC I/F Generic Decode Range 3 Register (LPC I/F—D31:F0)

Offset Address:	8Ch – 8Eh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bit
		Power Well:	Core

Bit	Description
31:24	Reserved
23:18	**Generic I/O Decode Range Address[7:2] Mask—**R/W. A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	Reserved
15:2	**Generic I/O Decode Range 3 Base Address (GEN3_BASE)—**R/W. ***Note:*** The PCH Does not provide decode down to the word or byte level
1	Reserved
0	**Generic Decode Range 3 Enable (GEN3_EN)—**R/W. 0 = Disable. 1 = Enable the GEN3 I/O range to be forwarded to the LPC I/F

13.1.27 GEN4_DEC—LPC I/F Generic Decode Range 4 Register (LPC I/F—D31:F0)

Offset Address:	90h – 93h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bit
		Power Well:	Core

Bit	Description
31:24	Reserved
23:18	**Generic I/O Decode Range Address[7:2] Mask—**R/W. A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	Reserved
15:2	**Generic I/O Decode Range 4 Base Address (GEN4_BASE)—**R/W. ***Note:*** The PCH Does not provide decode down to the word or byte level
1	Reserved
0	**Generic Decode Range 4 Enable (GEN4_EN)—**R/W. 0 = Disable. 1 = Enable the GEN4 I/O range to be forwarded to the LPC I/F

13.1.28 ULKMC—USB Legacy Keyboard / Mouse Control (LPC I/F—D31:F0)

Offset Address:	94h – 97h	Attribute:	RO, R/WC, R/W
Default Value:	00002000h	Size:	32 bit
		Power Well:	Core

Bit	Description
31:16	Reserved
15	**Intel SMI Caused by End of Pass-Through (SMIBYENDPS)—**R/WC. This bit indicates if the event occurred. Note that even if the corresponding enable bit is not set in bit 7, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred
14:12	Reserved
11	**Intel SMI Caused by Port 64 Write (TRAPBY64W)—**R/WC. This bit indicates if the event occurred. Note that even if the corresponding enable bit is not set in bit 3, this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Note that the A20Gate Pass-Through Logic allows specific port 64h writes to complete without setting this bit. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred.
10	**Intel SMI Caused by Port 64 Read (TRAPBY64R)—**R/WC. This bit indicates if the event occurred. Note that even if the corresponding enable bit is not set in bit 2, this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred.
9	**Intel SMI Caused by Port 60 Write (TRAPBY60W)—**R/WC. This bit indicates if the event occurred. Note that even if the corresponding enable bit is not set in bit 1, this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Note that the A20Gate Pass-Through Logic allows specific port 64h writes to complete without setting this bit. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred.
8	**Intel SMI Caused by Port 60 Read (TRAPBY60R)—**R/WC. This bit indicates if the event occurred. Note that even if the corresponding enable bit is not set in the bit 0, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event Occurred.
7	**Intel SMI at End of Pass-Through Enable (SMIATENDPS)—**R/W. This bit enables Intel SMI at the end of a pass-through. This can occur if an Intel SMI is generated in the middle of a pass-through, and needs to be serviced later. 0 = Disable 1 = Enable
6	**Pass Through State (PSTATE)**—RO. 0 = If software needs to reset this bit, it should set bit 5 in all of the host controllers to 0. 1 = Indicates that the state machine is in the middle of an A20GATE pass-through sequence.
5	**A20Gate Pass-Through Enable (A20PASSEN)—R/W.** 0 = Disable. 1 = Enable. Allows A20GATE sequence Pass-Through function. A specific cycle sequence involving writes to port 60h and 64h does not result in the setting of the Intel SMI status bits.
4	**Intel SMI on USB IRQ Enable (USBSMIEN)—R/W.** 0 = Disable 1 = Enable. USB interrupt will cause an Intel SMI event.
3	**Intel SMI on Port 64 Writes Enable (64WEN)—R/W.** 0 = Disable 1 = Enable. A 1 in bit 11 will cause an Intel SMI event.
2	**Intel SMI on Port 64 Reads Enable (64REN)—**R/W. 0 = Disable 1 = Enable. A 1 in bit 10 will cause an Intel SMI event.
1	**Intel SMI on Port 60 Writes Enable (60WEN)—**R/W. 0 = Disable 1 = Enable. A 1 in bit 9 will cause an Intel SMI event.
0	**Intel SMI on Port 60 Reads Enable (60REN)—**R/W. 0 = Disable 1 = Enable. A 1 in bit 8 will cause an Intel SMI event.

13.1.29 LGMR—LPC I/F Generic Memory Range (LPC I/F—D31:F0)

Offset Address:	98h – 9Bh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bit
		Power Well:	Core

Bit	Description
31:16	**Memory Address[31:16]—**R/W. This field specifies a 64 KB memory block anywhere in the 4 GB memory space that will be decoded to LPC as standard LPC memory cycle if enabled.
15:1	Reserved
0	**LPC Memory Range Decode Enable**—R/W. When this bit is set to '1', then the range specified in bits 31:16 of this register is enabled for decoding to LPC

13.1.30 BIOS_SEL1—BIOS Select 1 Register (LPC I/F—D31:F0)

Offset Address:	D0h–D3h	Attribute:	R/W, RO
Default Value:	00112233h	Size:	32 bits

Bit	Description
31:28	**BIOS_F8_IDSEL**—RO. IDSEL for two 512-KB BIOS memory ranges and one 128-KB memory range. This field is fixed at 0000. The IDSEL programmed in this field addresses the following memory ranges: FFF8 0000h–FFFF FFFFh FFB8 0000h–FFBF FFFFh 000E 0000h–000F FFFFh
27:24	**BIOS_F0_IDSEL**—R/W. IDSEL for two 512-KB BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFF0 0000h–FFF7 FFFFh FFB0 0000h–FFB7 FFFFh
23:20	**BIOS_E8_IDSEL**—R/W. IDSEL for two 512-KB BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFE8 0000h–FFEF FFFFh FFA8 0000h–FFAF FFFFh
19:16	**BIOS_E0_IDSEL**—R/W. IDSEL for two 512-KB BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFE0 0000h–FFE7 FFFFh FFA0 0000h–FFA7 FFFFh
15:12	**BIOS_D8_IDSEL**—R/W. IDSEL for two 512-KB BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFD8 0000h–FFDF FFFFh FF98 0000h–FF9F FFFFh
11:8	**BIOS_D0_IDSEL**—R/W. IDSEL for two 512-KB BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFD0 0000h–FFD7 FFFFh FF90 0000h–FF97 FFFFh
7:4	**BIOS_C8_IDSEL**—R/W. IDSEL for two 512-KB BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFC8 0000h–FFCF FFFFh FF88 0000h–FF8F FFFFh
3:0	**BIOS_C0_IDSEL**—R/W. IDSEL for two 512-KB BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFC0 0000h–FFC7 FFFFh FF80 0000h–FF87 FFFFh

13.1.31 BIOS_SEL2—BIOS Select 2 Register (LPC I/F—D31:F0)

Offset Address: D4h–D5h
Default Value: 4567h
Attribute: R/W
Size: 16 bits

Bit	Description
15:12	**BIOS_70_IDSEL**—R/W. IDSEL for two, 1-M BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF70 0000h–FF7F FFFFh FF30 0000h–FF3F FFFFh
11:8	**BIOS_60_IDSEL**—R/W. IDSEL for two, 1-M BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF60 0000h–FF6F FFFFh FF20 0000h–FF2F FFFFh
7:4	**BIOS_50_IDSEL**—R/W. IDSEL for two, 1-M BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF50 0000h–FF5F FFFFh FF10 0000h–FF1F FFFFh
3:0	**BIOS_40_IDSEL**—R/W. IDSEL for two, 1-M BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF40 0000h–FF4F FFFFh FF00 0000h–FF0F FFFFh

13.1.32 BIOS_DEC_EN1—BIOS Decode Enable Register (LPC I/F—D31:F0)

Offset Address:	D8h–D9h	Attribute:	R/W, RO
Default Value:	FFCFh	Size:	16 bits

Bit	Description
15	**BIOS_F8_EN**—RO. This bit enables decoding two 512-KB BIOS memory ranges, and one 128-KB memory range. 0 = Disable 1 = Enable the following ranges for the BIOS FFF80000h–FFFFFFFFh FFB80000h–FFBFFFFFh
14	**BIOS_F0_EN**—R/W. This bit enables decoding two 512-KB BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS: FFF00000h–FFF7FFFFh FFB00000h–FFB7FFFFh
13	**BIOS_E8_EN**—R/W. This bit enables decoding two 512-KB BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS: FFE80000h–FFEFFFFFh FFA80000h–FFAFFFFFh
12	**BIOS_E0_EN**—R/W. This bit enables decoding two 512-KB BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS: FFE00000h–FFE7FFFFh FFA00000h–FFA7FFFFh
11	**BIOS_D8_EN**—R/W. This bit enables decoding two 512-KB BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS FFD80000h–FFDFFFFFh FF980000h–FF9FFFFFh
10	**BIOS_D0_EN**—R/W. This bit enables decoding two 512-KB BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS FFD00000h–FFD7FFFFh FF900000h–FF97FFFFh
9	**BIOS_C8_EN**—R/W. This bit enables decoding two 512-KB BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS FFC80000h–FFCFFFFFh FF880000h–FF8FFFFFh
8	**BIOS_C0_EN**—R/W. This bit enables decoding two 512-KB BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS FFC00000h–FFC7FFFFh FF800000h–FF87FFFFh
7	**BIOS_Legacy_F_EN**—R/W. This enables the decoding of the legacy 64 KB range at F0000h–FFFFFh. 0 = Disable. 1 = Enable the following legacy ranges for the BIOS F0000h–FFFFFh ***Note:*** The decode for the BIOS legacy F segment is enabled only by this bit and is not affected by the GEN_PMCON_1.iA64_EN bit.
6	**BIOS_Legacy_E_EN**—R/W. This enables the decoding of the legacy 64 KB range at E0000h–EFFFFh. 0 = Disable. 1 = Enable the following legacy ranges for the BIOS E0000h–EFFFFh ***Note:*** The decode for the BIOS legacy E segment is enabled only by this bit and is not affected by the GEN_PMCON_1.iA64_EN bit.
5:4	Reserved

Bit	Description
3	**BIOS_70_EN**—R/W. Enables decoding two 1-M BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS FF700000h–FF7FFFFFh FF300000h–FF3FFFFFh
2	**BIOS_60_EN**—R/W. Enables decoding two 1-M BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS FF600000h–FF6FFFFFh FF200000h–FF2FFFFFh
1	**BIOS_50_EN—**R/W. Enables decoding two 1-M BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS FF500000h–FF5FFFFFh FF100000h–FF1FFFFFh
0	**BIOS_40_EN**—R/W. Enables decoding two 1-M BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS FF400000h–FF4FFFFFh FF000000h–FF0FFFFFh

Note: This register effects the BIOS decode regardless of whether the BIOS is resident on LPC or SPI. The concept of Feature Space does not apply to SPI-based flash. The PCH simply decodes these ranges as memory accesses when enabled for the SPI flash interface.

13.1.33 BIOS_CNTL—BIOS Control Register (LPC I/F—D31:F0)

Offset Address:	DCh	Attribute:	R/WLO, R/W, RO
Default Value:	20h	Size:	8 bit
Lockable:	No	Power Well:	Core

Bit	Description
7:6	Reserved
5	**SMM BIOS Write Protect Disable (SMM_BWP)**—R/WLO. This bit set defines when the BIOS region can be written by the host. 0 = BIOS region SMM protection is disabled. The BIOS Region is writable regardless if Processors are in SMM or not. (Set this field to 0 for legacy behavior) 1 = BIOS region SMM protection is enabled. The BIOS Region is not writable unless all Processors are in SMM.
4	**Top Swap Status (TSS)—**RO. This bit provides a read-only path to view the state of the Top Swap bit that is at offset 3414h, bit 0.
3:2	**SPI Read Configuration (SRC)—**R/W. This 2-bit field controls two policies related to BIOS reads on the SPI interface: Bit 3- Prefetch Enable Bit 2- Cache Disable Settings are summarized below: **Bits 3:2** — **Description** 00b — **No prefetching, but caching enabled.** 64B demand reads load the read buffer cache with "valid" data, allowing repeated code fetches to the same line to complete quickly 01b — **No prefetching and no caching.** One-to-one correspondence of host BIOS reads to SPI cycles. This value can be used to invalidate the cache. 10b — **Prefetching and Caching enabled.** This mode is used for long sequences of short reads to consecutive addresses (that is, shadowing). 11b — **Reserved. This is an invalid configuration**, caching must be enabled when prefetching is enabled.
1	**BIOS Lock Enable (BLE)—**R/WLO. 0 = Setting the BIOSWE will not cause SMIs. 1 = Enables setting the BIOSWE bit to cause SMIs. Once set, this bit can only be cleared by a PLTRST#
0	**BIOS Write Enable (BIOSWE)—**R/W. 0 = Only read cycles result in BIOS I/F cycles. 1 = Access to the BIOS space is enabled for both read and write cycles. When this bit is written from a 0 to a 1 and BIOS Lock Enable (BLE) is also set, an SMI# is generated. This ensures that only Intel SMI code can update BIOS.

13.1.34 FDCAP—Feature Detection Capability ID (LPC I/F—D31:F0)

Offset Address:	E0h–E1h	Attribute:	RO
Default Value:	0009h	Size:	16 bit
		Power Well:	Core

Bit	Description
15:8	**Next Item Pointer (NEXT)—**RO. Configuration offset of the next Capability Item. 00h indicates the last item in the Capability List.
7:0	**Capability ID—**RO. Indicates a Vendor Specific Capability

13.1.35 FDLEN—Feature Detection Capability Length (LPC I/F—D31:F0)

Offset Address:	E2h	Attribute:	RO
Default Value:	0Ch	Size:	8 bit
		Power Well:	Core

Bit	Description
7:0	**Capability Length—**RO. Indicates the length of this Vendor Specific capability, as required by PCI Specification.

13.1.36 FDVER—Feature Detection Version (LPC I/F—D31:F0)

Offset Address:	E3h	Attribute:	RO
Default Value:	10h	Size:	8 bit
		Power Well:	Core

Bit	Description
7:4	**Vendor-Specific Capability ID—**RO. A value of 1h in this 4-bit field identifies this Capability as Feature Detection Type. This field allows software to differentiate the Feature Detection Capability from other Vendor-Specific capabilities
3:0	**Capability Version—**RO. This field indicates the version of the Feature Detection capability

13.1.37 FVECIDX—Feature Vector Index (LPC I/F—D31:F0)

Offset Address:	E4h–E7h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bit
		Power Well:	Core

Bit	Description
31:6	Reserved
5:2	**Index (IDX)—**R/W. 4-bit index pointer into the 64-byte Feature Vector space. Data is read from the FVECD register. This points to a DWord register.
1:0	Reserved

13.1.38 FVECD—Feature Vector Data (LPC I/F—D31:F0)

Offset Address:	E8h–EBh	Attribute:	RO
Default Value:	See Description	Size:	32 bit
		Power Well:	Core

Bit	Description
31:0	Data (DATA)—RO. 32-bit data value that is read from the Feature Vector offset pointed to by FVECIDX.

13.1.39 Feature Vector Space

13.1.39.1 FVEC0—Feature Vector Register 0

FVECIDX.IDX:	0000b	Attribute:	RO
Default Value:	See Description	Size:	32 bit
		Power Well:	Core

Bit	Description
31:12	Reserved
11:10	USB Port Count Capability—RO 00 = 14 ports 01 = 12 ports 10 = 10 ports 11 = Reserved
9:8	Reserved
7	RAID Capability—RO Disabled Capable
6	SATA Ports 2 and 3—RO Capable Disabled
5:4	Reserved
3	SATA Port 1 6 Gb/s Capability—RO Capable Disabled
2	SATA Port 0 6 Gb/s Capability—RO Capable Disabled
1	PCI Interface Capability—RO Capable Disabled
0	Reserved

13.1.39.2 FVEC1—Feature Vector Register 1

FVECIDX.IDX:	0001b	Attribute:	RO
Default Value:	See Description	Size:	32 bit
		Power Well:	Core

Bit	Description
31:23	Reserved
22	USB Redirect (USBr) Capability—RO 0 = Capable 1 = Disabled
21:0	Reserved

13.1.39.3 FVEC2—Feature Vector Register 2

FVECIDX.IDX:	0010b	Attribute:	RO
Default Value:	See Description	Size:	32 bit
		Power Well:	Core

Bit	Description
31:23	Reserved
22	Intel® Anti-Theft Technology Capability—RO 0 = Disabled 1 = Capable
21	PCI Express* Ports 7 and 8—RO 0 = Capable 1 = Disabled
20:0	Reserved

13.1.39.4 FVEC3—Feature Vector Register 3

FVECIDX.IDX:	0011b	Attribute:	RO
Default Value:	See Description	Size:	32 bit
		Power Well:	Core

Bit	Description
31:14	Reserved
13	Data Center Manageability Interface (DCMI) Capability—RO 0 = Capable 1 = Disabled
12	Node Manager Capability—RO 0 = Capable 1 = Disabled
11:0	Reserved

13.1.40 RCBA—Root Complex Base Address Register (LPC I/F—D31:F0)

Offset Address:	F0–F3h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bit

Bit	Description
31:14	**Base Address (BA)—**R/W. Base Address for the root complex register block decode range. This address is aligned on a 16-KB boundary.
13:1	Reserved
0	**Enable (EN)—**R/W. When set, this bit enables the range specified in BA to be claimed as the Root Complex Register Block.

13.2 DMA I/O Registers

Table 13-2. DMA Registers (Sheet 1 of 2)

Port	Alias	Register Name	Default	Type
00h	10h	Channel 0 DMA Base & Current Address	Undefined	R/W
01h	11h	Channel 0 DMA Base & Current Count	Undefined	R/W
02h	12h	Channel 1 DMA Base & Current Address	Undefined	R/W
03h	13h	Channel 1 DMA Base & Current Count	Undefined	R/W
04h	14h	Channel 2 DMA Base & Current Address	Undefined	R/W
05h	15h	Channel 2 DMA Base & Current Count	Undefined	R/W
06h	16h	Channel 3 DMA Base & Current Address	Undefined	R/W
07h	17h	Channel 3 DMA Base & Current Count	Undefined	R/W
08h	18h	Channel 0–3 DMA Command	Undefined	WO
		Channel 0–3 DMA Status	Undefined	RO
0Ah	1Ah	Channel 0–3 DMA Write Single Mask	000001XXb	WO
0Bh	1Bh	Channel 0–3 DMA Channel Mode	000000XXb	WO
0Ch	1Ch	Channel 0–3 DMA Clear Byte Pointer	Undefined	WO
0Dh	1Dh	Channel 0–3 DMA Master Clear	Undefined	WO
0Eh	1Eh	Channel 0–3 DMA Clear Mask	Undefined	WO
0Fh	1Fh	Channel 0–3 DMA Write All Mask	0Fh	R/W
80h	90h	Reserved Page	Undefined	R/W
81h	91h	Channel 2 DMA Memory Low Page	Undefined	R/W
82h	—	Channel 3 DMA Memory Low Page	Undefined	R/W
83h	93h	Channel 1 DMA Memory Low Page	Undefined	R/W
84h–86h	94h–96h	Reserved Pages	Undefined	R/W
87h	97h	Channel 0 DMA Memory Low Page	Undefined	R/W
88h	98h	Reserved Page	Undefined	R/W
89h	99h	Channel 6 DMA Memory Low Page	Undefined	R/W
8Ah	9Ah	Channel 7 DMA Memory Low Page	Undefined	R/W
8Bh	9Bh	Channel 5 DMA Memory Low Page	Undefined	R/W
8Ch–8Eh	9Ch–9Eh	Reserved Page	Undefined	R/W
8Fh	9Fh	Refresh Low Page	Undefined	R/W
C0h	C1h	Channel 4 DMA Base & Current Address	Undefined	R/W
C2h	C3h	Channel 4 DMA Base & Current Count	Undefined	R/W
C4h	C5h	Channel 5 DMA Base & Current Address	Undefined	R/W
C6h	C7h	Channel 5 DMA Base & Current Count	Undefined	R/W
C8h	C9h	Channel 6 DMA Base & Current Address	Undefined	R/W
CAh	CBh	Channel 6 DMA Base & Current Count	Undefined	R/W
CCh	CDh	Channel 7 DMA Base & Current Address	Undefined	R/W
CEh	CFh	Channel 7 DMA Base & Current Count	Undefined	R/W
D0h	D1h	Channel 4–7 DMA Command	Undefined	WO
		Channel 4–7 DMA Status	Undefined	RO
D4h	D5h	Channel 4–7 DMA Write Single Mask	000001XXb	WO

Table 13-2. DMA Registers (Sheet 2 of 2)

Port	Alias	Register Name	Default	Type
D6h	D7h	Channel 4–7 DMA Channel Mode	000000XXb	WO
D8h	D9h	Channel 4–7 DMA Clear Byte Pointer	Undefined	WO
DAh	DBh	Channel 4–7 DMA Master Clear	Undefined	WO
DCh	DDh	Channel 4–7 DMA Clear Mask	Undefined	WO
DEh	DFh	Channel 4–7 DMA Write All Mask	0Fh	R/W

13.2.1 DMABASE_CA—DMA Base and Current Address Registers

I/O Address: Ch. #0 = 00h; Ch. #1 = 02h Ch. #2 = 04h; Ch. #3 = 06h Ch. #5 = C4h Ch. #6 = C8h Ch. #7 = CCh;

Attribute: R/W

Size: 16 bit (per channel), but accessed in two 8-bit quantities

Default Value: Undefined

Lockable: No

Power Well: Core

Bit	Description
15:0	**Base and Current Address**—R/W. This register determines the address for the transfers to be performed. The address specified points to two separate registers. On writes, the value is stored in the *Base Address* register and copied to the *Current Address* register. On reads, the value is returned from the *Current Address* register. The address increments/decrements in the Current Address register after each transfer, depending on the mode of the transfer. If the channel is in auto-initialize mode, the Current Address register will be reloaded from the Base Address register after a terminal count is generated. For transfers to/from a 16-bit slave (channels 5–7), the address is shifted left one bit location. Bit 15 will be shifted into Bit 16. The register is accessed in 8 bit quantities. The byte is pointed to by the current byte pointer flip/flop. Before accessing an address register, the byte pointer flip/flop should be cleared to ensure that the low byte is accessed first

13.2.2 DMABASE_CC—DMA Base and Current Count Registers

I/O Address:	Ch. #0 = 01h; Ch. #1 = 03h Ch. #2 = 05h; Ch. #3 = 07h Ch. #5 = C6h; Ch. #6 = CAh Ch. #7 = CEh;	Attribute:	R/W
		Size:	16-bit (per channel), but accessed in two 8-bit quantities
Default Value:	Undefined		
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Base and Current Count**—R/W. This register determines the number of transfers to be performed. The address specified points to two separate registers. On writes, the value is stored in the *Base Count* register and copied to the *Current Count* register. On reads, the value is returned from the *Current Count* register. The actual number of transfers is one more than the number programmed in the Base Count Register (that is, programming a count of 4h results in 5 transfers). The count is decrements in the Current Count register after each transfer. When the value in the register rolls from 0 to FFFFh, a terminal count is generated. If the channel is in auto-initialize mode, the Current Count register will be reloaded from the Base Count register after a terminal count is generated. For transfers to/from an 8-bit slave (channels 0–3), the count register indicates the number of bytes to be transferred. For transfers to/from a 16-bit slave (channels 5–7), the count register indicates the number of words to be transferred. The register is accessed in 8 bit quantities. The byte is pointed to by the current byte pointer flip/flop. Before accessing a count register, the byte pointer flip/flop should be cleared to ensure that the low byte is accessed first.

13.2.3 DMAMEM_LP—DMA Memory Low Page Registers

I/O Address:	Ch. #0 = 87h; Ch. #1 = 83h Ch. #2 = 81h; Ch. #3 = 82h Ch. #5 = 8Bh; Ch. #6 = 89h Ch. #7 = 8Ah;	Attribute:	R/W
Default Value:	Undefined	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**DMA Low Page** (ISA Address bits [23:16])—R/W. This register works in conjunction with the DMA controller's Current Address Register to define the complete 24-bit address for the DMA channel. This register remains static throughout the DMA transfer. Bit 16 of this register is ignored when in 16 bit I/O count by words mode as it is replaced by the bit 15 shifted out from the current address register.

13.2.4 DMACMD—DMA Command Register

I/O Address:	Ch. #0–3 = 08h; Ch. #4–7 = D0h	Attribute:	WO
Default Value:	Undefined	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:5	Reserved. Must be 0.
4	**DMA Group Arbitration Priority**—WO. Each channel group is individually assigned either fixed or rotating arbitration priority. At part reset, each group is initialized in fixed priority. 0 = Fixed priority to the channel group 1 = Rotating priority to the group.
3	Reserved. Must be 0.
2	**DMA Channel Group Enable**—WO. Both channel groups are enabled following part reset. 0 = Enable the DMA channel group. 1 = Disable. Disabling channel group 4–7 also disables channel group 0–3, which is cascaded through channel 4.
1:0	Reserved. Must be 0.

13.2.5 DMASTA—DMA Status Register

I/O Address:	Ch. #0–3 = 08h; Ch. #4–7 = D0h	Attribute:	RO
Default Value:	Undefined	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:4	**Channel Request Status**—RO. When a valid DMA request is pending for a channel, the corresponding bit is set to 1. When a DMA request is not pending for a particular channel, the corresponding bit is set to 0. The source of the DREQ may be hardware or a software request. Note that channel 4 is the cascade channel, so the request status of channel 4 is a logical OR of the request status for channels 0 through 3. 4 = Channel 0 5 = Channel 1 (5) 6 = Channel 2 (6) 7 = Channel 3 (7)
3:0	**Channel Terminal Count Status**—RO. When a channel reaches terminal count (TC), its status bit is set to 1. If TC has not been reached, the status bit is set to 0. Channel 4 is programmed for cascade, so the TC bit response for channel 4 is irrelevant: 0 = Channel 0 1 = Channel 1 (5) 2 = Channel 2 (6) 3 = Channel 3 (7)

13.2.6 DMA_WRSMSK—DMA Write Single Mask Register

I/O Address:	Ch. #0–3 = 0Ah; Ch. #4–7 = D4h	Attribute:	WO
Default Value:	0000 01xx	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:3	Reserved. Must be 0.
2	**Channel Mask Select**—WO. 0 = Enable DREQ for the selected channel. The channel is selected through bits [1:0]. Therefore, only one channel can be masked / unmasked at a time. 1 = Disable DREQ for the selected channel.
1:0	**DMA Channel Select**—WO. These bits select the DMA Channel Mode Register to program. 00 = Channel 0 (4) 01 = Channel 1 (5) 10 = Channel 2 (6) 11 = Channel 3 (7)

13.2.7 DMACH_MODE—DMA Channel Mode Register

I/O Address:	Ch. #0–3 = 0Bh; Ch. #4–7 = D6h	Attribute:	WO
Default Value:	0000 00xx	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:6	**DMA Transfer Mode**—WO. Each DMA channel can be programmed in one of four different modes: 00 = Demand mode 01 = Single mode 10 = Reserved 11 = Cascade mode
5	**Address Increment/Decrement Select**—WO. This bit controls address increment/decrement during DMA transfers. 0 = Address increment. (default after part reset or Master Clear) 1 = Address decrement.
4	**Autoinitialize Enable**—WO. 0 = Autoinitialize feature is disabled and DMA transfers terminate on a terminal count. A part reset or Master Clear disables autoinitialization. 1 = DMA restores the Base Address and Count registers to the current registers following a terminal count (TC).
3:2	**DMA Transfer Type**—WO. These bits represent the direction of the DMA transfer. When the channel is programmed for cascade mode, (bits[7:6] = 11) the transfer type is irrelevant. 00 = Verify – No I/O or memory strobes generated 01 = Write – Data transferred from the I/O devices to memory 10 = Read – Data transferred from memory to the I/O device 11 = Invalid
1:0	**DMA Channel Select**—WO. These bits select the DMA Channel Mode Register that will be written by bits [7:2]. 00 = Channel 0 (4) 01 = Channel 1 (5) 10 = Channel 2 (6) 11 = Channel 3 (7)

13.2.8 DMA Clear Byte Pointer Register

I/O Address:	Ch. #0–3 = 0Ch; Ch. #4–7 = D8h	Attribute:	WO
Default Value:	xxxx xxxx	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**Clear Byte Pointer**—WO. No specific pattern. Command enabled with a write to the I/O port address. Writing to this register initializes the byte pointer flip/flop to a known state. It clears the internal latch used to address the upper or lower byte of the 16-bit Address and Word Count Registers. The latch is also cleared by part reset and by the Master Clear command. This command precedes the first access to a 16-bit DMA controller register. The first access to a 16-bit register will then access the significant byte, and the second access automatically accesses the most significant byte.

13.2.9 DMA Master Clear Register

I/O Address:	Ch. #0–3 = 0Dh; Ch. #4–7 = DAh	Attribute:	WO
Default Value:	xxxx xxxx	Size:	8-bit

Bit	Description
7:0	**Master Clear**—WO. No specific pattern. Enabled with a write to the port. This has the same effect as the hardware Reset. The Command, Status, Request, and Byte Pointer flip/flop registers are cleared and the Mask Register is set.

13.2.10 DMA_CLMSK—DMA Clear Mask Register

I/O Address:	Ch. #0–3 = 0Eh; Ch. #4–7 = DCh	Attribute:	WO
Default Value:	xxxx xxxx	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**Clear Mask Register**—WO. No specific pattern. Command enabled with a write to the port.

13.2.11 DMA_WRMSK—DMA Write All Mask Register

I/O Address:	Ch. #0–3 = 0Fh; Ch. #4–7 = DEh	Attribute:	R/W
Default Value:	0000 1111	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:4	Reserved. Must be 0.
3:0	**Channel Mask Bits**—R/W. This register permits all four channels to be simultaneously enabled/disabled instead of enabling/disabling each channel individually, as is the case with the Mask Register – Write Single Mask Bit. In addition, this register has a read path to allow the status of the channel mask bits to be read. A channel's mask bit is automatically set to 1 when the Current Byte/Word Count Register reaches terminal count (unless the channel is in auto-initialization mode). Setting the bit(s) to a 1 disables the corresponding DREQ(s). Setting the bit(s) to a 0 enables the corresponding DREQ(s). Bits [3:0] are set to 1 upon part reset or Master Clear. When read, bits [3:0] indicate the DMA channel [3:0] ([7:4]) mask status. Bit 0 = Channel 0 (4)1 = Masked, 0 = Not Masked Bit 1 = Channel 1 (5)1 = Masked, 0 = Not Masked Bit 2 = Channel 2 (6)1 = Masked, 0 = Not Masked Bit 3 = Channel 3 (7)1 = Masked, 0 = Not Masked ***Note:*** Disabling channel 4 also disables channels 0–3 due to the cascade of channels 0 – 3 through channel 4.

13.3 Timer I/O Registers

Port	Aliases	Register Name	Default Value	Type
40h	50h	Counter 0 Interval Time Status Byte Format	0XXXXXXXb	RO
		Counter 0 Counter Access Port	Undefined	R/W
41h	51h	Counter 1 Interval Time Status Byte Format	0XXXXXXXb	RO
		Counter 1 Counter Access Port	Undefined	R/W
42h	52h	Counter 2 Interval Time Status Byte Format	0XXXXXXXb	RO
		Counter 2 Counter Access Port	Undefined	R/W
43h	53h	Timer Control Word	Undefined	WO
		Timer Control Word Register	XXXXXXX0b	WO
		Counter Latch Command	X0h	WO

13.3.1 TCW—Timer Control Word Register

I/O Address: 43h Attribute: WO
Default Value: All bits undefined Size: 8 bits

This register is programmed prior to any counter being accessed to specify counter modes. Following part reset, the control words for each register are undefined and each counter output is 0. Each timer must be programmed to bring it into a known state.

Bit	Description
7:6	**Counter Select**—WO. The Counter Selection bits select the counter the control word acts upon as shown below. The Read Back Command is selected when bits[7:6] are both 1. 00 = Counter 0 select 01 = Counter 1 select 10 = Counter 2 select 11 = Read Back Command
5:4	**Read/Write Select**—WO. These bits are the read/write control bits. The actual counter programming is done through the counter port (40h for counter 0, 41h for counter 1, and 42h for counter 2). 00 = Counter Latch Command 01 = Read/Write Least Significant Byte (LSB) 10 = Read/Write Most Significant Byte (MSB) 11 = Read/Write LSB then MSB
3:1	**Counter Mode Selection**—WO. These bits select one of six possible modes of operation for the selected counter. **Bit Value** — **Mode** 000b — Mode 0 Out signal on end of count (=0) 001b — Mode 1 Hardware retriggerable one-shot x10b — Mode 2 Rate generator (divide by n counter) x11b — Mode 3 Square wave output 100b — Mode 4 Software triggered strobe 101b — Mode 5 Hardware triggered strobe
0	Binary/BCD Countdown Select—WO. 0 = Binary countdown is used. The largest possible binary count is 2^{16} 1 = Binary coded decimal (BCD) count is used. The largest possible BCD count is 10^4

There are two special commands that can be issued to the counters through this register, the Read Back Command and the Counter Latch Command. When these commands are chosen, several bits within this register are redefined. These register formats are described below:

RDBK_CMD—Read Back Command

The Read Back Command is used to determine the count value, programmed mode, and current states of the OUT pin and Null count flag of the selected counter or counters. Status and/or count may be latched in any or all of the counters by selecting the counter during the register write. The count and status remain latched until read, and further latch commands are ignored until the count is read. Both count and status of the selected counters may be latched simultaneously by setting both bit 5 and bit 4 to 0. If both are latched, the first read operation from that counter returns the latched status. The next one or two reads, depending on whether the counter is programmed for one or two byte counts, returns the latched count. Subsequent reads return an unlatched count.

Bit	Description
7:6	**Read Back Command.** Must be 11 to select the Read Back Command
5	**Latch Count of Selected Counters**. 0 = Current count value of the selected counters will be latched 1 = Current count will not be latched
4	**Latch Status of Selected Counters**. 0 = Status of the selected counters will be latched 1 = Status will not be latched
3	**Counter 2 Select**. 1 = Counter 2 count and/or status will be latched
2	**Counter 1 Select**. 1 = Counter 1 count and/or status will be latched
1	**Counter 0 Select**. 1 = Counter 0 count and/or status will be latched.
0	Reserved. Must be 0.

LTCH_CMD—Counter Latch Command

The Counter Latch Command latches the current count value. This command is used to insure that the count read from the counter is accurate. The count value is then read from each counter's count register through the Counter Ports Access Ports Register (40h for counter 0, 41h for counter 1, and 42h for counter 2). The count must be read according to the programmed format, that is, if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other (read, write, or programming operations for other counters may be inserted between the reads). If a counter is latched once and then latched again before the count is read, the second Counter Latch Command is ignored.

Bit	Description
7:6	**Counter Selection.** These bits select the counter for latching. If "11" is written, then the write is interpreted as a read back command. 00 = Counter 0 01 = Counter 1 10 = Counter 2
5:4	**Counter Latch Command**. 00 = Selects the Counter Latch Command.
3:0	Reserved. Must be 0.

13.3.2 SBYTE_FMT—Interval Timer Status Byte Format Register

I/O Address:	Counter 0 = 40h, Counter 1 = 41h, Counter 2 = 42h	Attribute: Size:	RO 8 bits per counter
Default Value:	Bits[6:0] undefined, Bit 7=0		

Each counter's status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for a given counter, the next read from the counter's Counter Access Ports Register (40h for counter 0, 41h for counter 1, and 42h for counter 2) returns the status byte. The status byte returns the following:

Bit	Description
7	**Counter OUT Pin State**—RO. 0 = OUT pin of the counter is also a 0 1 = OUT pin of the counter is also a 1
6	**Count Register Status**—RO. This bit indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the counter mode, but until the count is loaded into the counting element (CE), the count value will be incorrect. 0 = Count has been transferred from CR to CE and is available for reading. 1 = Null Count. Count has not been transferred from CR to CE and is not yet available for reading.
5:4	**Read/Write Selection Status**—RO. These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 = Counter Latch Command 01 = Read/Write Least Significant Byte (LSB) 10 = Read/Write Most Significant Byte (MSB) 11 = Read/Write LSB then MSB
3:1	**Mode Selection Status**—RO. These bits return the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. 000 = Mode 0 – Out signal on end of count (=0) 001 = Mode 1 – Hardware retriggerable one-shot x10 = Mode 2 – Rate generator (divide by n counter) x11 = Mode 3 – Square wave output 100 = Mode 4 – Software triggered strobe 101 = Mode 5 – Hardware triggered strobe
0	**Countdown Type Status**—RO. This bit reflects the current countdown type. 0 = Binary countdown 1 = Binary Coded Decimal (BCD) countdown.

13.3.3 Counter Access Ports Register

I/O Address:	Counter 0 – 40h, Counter 1 – 41h, Counter 2 – 42h	Attribute:	R/W
Default Value:	All bits undefined	Size:	8 bit

Bit	Description
7:0	**Counter Port**—R/W. Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

13.4 8259 Interrupt Controller (PIC) Registers

13.4.1 Interrupt Controller I/O MAP

The interrupt controller registers are located at 20h and 21h for the master controller (IRQ 0–7), and at A0h and A1h for the slave controller (IRQ 8–13). These registers have multiple functions, depending upon the data written to them. Table 13-3 shows the different register possibilities for each address.

Table 13-3. PIC Registers

Port	Aliases	Register Name	Default Value	Type
20h	24h, 28h, 2Ch, 30h, 34h, 38h, 3Ch	Master PIC ICW1 Init. Cmd Word 1	Undefined	WO
		Master PIC OCW2 Op Ctrl Word 2	001XXXXXb	WO
		Master PIC OCW3 Op Ctrl Word 3	X01XXX10b	WO
21h	25h, 29h, 2Dh, 31h, 35h, 39h, 3Dh	Master PIC ICW2 Init. Cmd Word 2	Undefined	WO
		Master PIC ICW3 Init. Cmd Word 3	Undefined	WO
		Master PIC ICW4 Init. Cmd Word 4	01h	WO
		Master PIC OCW1 Op Ctrl Word 1	00h	R/W
A0h	A4h, A8h, ACh, B0h, B4h, B8h, BCh	Slave PIC ICW1 Init. Cmd Word 1	Undefined	WO
		Slave PIC OCW2 Op Ctrl Word 2	001XXXXXb	WO
		Slave PIC OCW3 Op Ctrl Word 3	X01XXX10b	WO
A1h	A5h, A9h, ADh, B1h, B5h, B9h, BDh	Slave PIC ICW2 Init. Cmd Word 2	Undefined	WO
		Slave PIC ICW3 Init. Cmd Word 3	Undefined	WO
		Slave PIC ICW4 Init. Cmd Word 4	01h	WO
		Slave PIC OCW1 Op Ctrl Word 1	00h	R/W
4D0h	–	Master PIC Edge/Level Triggered	00h	R/W
4D1h	–	Slave PIC Edge/Level Triggered	00h	R/W

Note: Refer to note addressing active-low interrupt sources in 8259 Interrupt Controllers section (Section 5.9).

13.4.2 ICW1—Initialization Command Word 1 Register

Offset Address:	Master Controller – 20h Slave Controller – A0h	Attribute:	WO
		Size:	8 bit /controller
Default Value:	All bits undefined		

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs:

1. The Interrupt Mask register is cleared.
2. IRQ7 input is assigned priority 7.
3. The slave mode address is set to 7.
4. Special mask mode is cleared and Status Read is set to IRR.

Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Bit	Description
7:5	**ICW/OCW Select**—WO. These bits are MCS-85 specific, and not needed. 000 = Should be programmed to "000"
4	**ICW/OCW Select**—WO. 1 = This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	**Edge/Level Bank Select (LTIM)**—WO. Disabled. Replaced by the edge/level triggered control registers (ELCR, D31:F0:4D0h, D31:F0:4D1h).
2	ADI—WO. 0 = Ignored for the PCH. Should be programmed to 0.
1	**Single or Cascade (SNGL)**—WO. 0 = Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	**ICW4 Write Required (IC4)**—WO. 1 = This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

13.4.3 ICW2—Initialization Command Word 2 Register

Offset Address:	Master Controller – 21h Slave Controller – A1h	Attribute:	WO
		Size:	8 bit /controller
Default Value:	All bits undefined		

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the processor to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Bit	Description
7:3	**Interrupt Vector Base Address**—WO. Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.
2:0	**Interrupt Request Level**—WO. When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: **Code** / **Master Interrupt** / **Slave Interrupt** 000b / IRQ0 / IRQ8 001b / IRQ1 / IRQ9 010b / IRQ2 / IRQ10 011b / IRQ3 / IRQ11 100b / IRQ4 / IRQ12 101b / IRQ5 / IRQ13 110b / IRQ6 / IRQ14 111b / IRQ7 / IRQ15

13.4.4 ICW3—Master Controller Initialization Command Word 3 Register

Offset Address:	21h	Attribute:	WO
Default Value:	All bits undefined	Size:	8 bits

Bit	Description
7:3	0 = These bits must be programmed to 0.
2	**Cascaded Interrupt Controller IRQ Connection**—WO. This bit indicates that the slave controller is cascaded on IRQ2. When IRQ8#–IRQ15 is asserted, it goes through the slave controller's priority resolver. The slave controller's INTR output onto IRQ2. IRQ2 then goes through the master controller's priority solver. If it wins, the INTR signal is asserted to the processor, and the returning interrupt acknowledge returns the interrupt vector for the slave controller. 1 = This bit must always be programmed to a 1.
1:0	0 = These bits must be programmed to 0.

13.4.5 ICW3—Slave Controller Initialization Command Word 3 Register

Offset Address:	A1h	Attribute:	WO
Default Value:	All bits undefined	Size:	8 bits

Bit	Description
7:3	0 = These bits must be programmed to 0.
2:0	**Slave Identification Code**—WO. These bits are compared against the slave identification code broadcast by the master controller from the trailing edge of the first internal INTA# pulse to the trailing edge of the second internal INTA# pulse. These bits must be programmed to 02h to match the code broadcast by the master controller. When 02h is broadcast by the master controller during the INTA# sequence, the slave controller assumes responsibility for broadcasting the interrupt vector.

13.4.6 ICW4—Initialization Command Word 4 Register

Offset Address:	Master Controller – 021h Slave Controller – 0A1h	Attribute:	WO
		Size:	8 bits
Default Value:	01h		

Bit	Description
7:5	0 = These bits must be programmed to 0.
4	**Special Fully Nested Mode (SFNM)**—WO. 0 = Should normally be disabled by writing a 0 to this bit. 1 = Special fully nested mode is programmed.
3	**Buffered Mode (BUF)**—WO. 0 = Must be programmed to 0 for the PCH. This is non-buffered mode.
2	**Master/Slave in Buffered Mode**—WO. Not used. 0 = Should always be programmed to 0.
1	**Automatic End of Interrupt (AEOI)**—WO. 0 = This bit should normally be programmed to 0. This is the normal end of interrupt. 1 = Automatic End of Interrupt (AEOI) mode is programmed.
0	**Microprocessor Mode**—WO. 1 = Must be programmed to 1 to indicate that the controller is operating in an Intel Architecture-based system.

13.4.7 OCW1—Operational Control Word 1 (Interrupt Mask) Register

Offset Address:	Master Controller – 021h Slave Controller – 0A1h	Attribute: Size:	R/W 8 bits
Default Value:	00h		

Bit	Description
7:0	**Interrupt Request Mask**—R/W. When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

13.4.8 OCW2—Operational Control Word 2 Register

Offset Address:	Master Controller – 020h Slave Controller – 0A0h	Attribute: Size:	WO 8 bits
Default Value:	Bit[4:0]=undefined, Bit[7:5]=001		

Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Bit	Description
7:5	**Rotate and EOI Codes** (R, SL, EOI)—WO. These three bits control the Rotate and End of Interrupt modes and combinations of the two. 000 = Rotate in Auto EOI Mode (Clear) 001 = Non-specific EOI command 010 = No Operation 011 = *Specific EOI Command 100 = Rotate in Auto EOI Mode (Set) 101 = Rotate on Non-Specific EOI Command 110 = *Set Priority Command 111 = *Rotate on Specific EOI Command *L0 – L2 Are Used
4:3	**OCW2 Select**—WO. When selecting OCW2, bits 4:3 = 00
2:0	**Interrupt Level Select** (L2, L1, L0)—WO. L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined below, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function; programming L2, L1 and L0 to 0 is sufficient in this case. Code / Interrupt Level: 000b IRQ0/8; 001b IRQ1/9; 010b IRQ2/10; 011b IRQ3/11 Code / Interrupt Level: 000b IRQ4/12; 001b IRQ5/13; 010b IRQ6/14; 011b IRQ7/15

13.4.9 OCW3—Operational Control Word 3 Register

Offset Address:	Master Controller – 020h Slave Controller – 0A0h	Attribute: Size:	WO 8 bits
Default Value:	Bit[6,0]=0, Bit[7,4:2]=undefined, Bit[5,1]=1		

Bit	Description
7	Reserved. Must be 0.
6	**Special Mask Mode (SMM)**—WO. 1 = The Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/disabling of the other channel's mask bits. Bit 5, the ESMM bit, must be set for this bit to have any meaning.
5	**Enable Special Mask Mode (ESMM)**—WO. 0 = Disable. The SMM bit becomes a "don't care". 1 = Enable the SMM bit to set or reset the Special Mask Mode.
4:3	**OCW3 Select**—WO. When selecting OCW3, bits 4:3 = 01
2	**Poll Mode Command**—WO. 0 = Disable. Poll Command is not issued. 1 = Enable. The next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	**Register Read Command**—WO. These bits provide control for reading the In-Service Register (ISR) and the Interrupt Request Register (IRR). When bit 1=0, bit 0 will not affect the register read selection. When bit 1=1, bit 0 selects the register status returned following an OCW3 read. If bit 0=0, the IRR will be read. If bit 0=1, the ISR will be read. Following ICW initialization, the default OCW3 port address read will be "read IRR". To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. 00 = No Action 01 = No Action 10 = Read IRQ Register 11 = Read IS Register

13.4.10 ELCR1—Master Controller Edge/Level Triggered Register

Offset Address:	4D0h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

In edge mode, (bit[x] = 0), the interrupt is recognized by a low to high transition. In level mode (bit[x] = 1), the interrupt is recognized by a high level. The cascade channel, IRQ2, the heart beat timer (IRQ0), and the keyboard controller (IRQ1), cannot be put into level mode.

Bit	Description
7	**IRQ7 ECL**—R/W. 0 = Edge 1 = Level
6	**IRQ6 ECL**—R/W. 0 = Edge 1 = Level
5	**IRQ5 ECL**—R/W. 0 = Edge 1 = Level

Bit	Description
4	**IRQ4 ECL**—R/W. 0 = Edge 1 = Level
3	**IRQ3 ECL**—R/W. 0 = Edge 1 = Level
2:0	Reserved. Must be 0.

13.4.11 ELCR2—Slave Controller Edge/Level Triggered Register

Offset Address: 4D1h Attribute: R/W
Default Value: 00h Size: 8 bits

In edge mode, (bit[x] = 0), the interrupt is recognized by a low to high transition. In level mode (bit[x] = 1), the interrupt is recognized by a high level. The real time clock, IRQ8#, and the floating point error interrupt, IRQ13, cannot be programmed for level mode.

Bit	Description
7	**IRQ15 ECL**—R/W. 0 = Edge 1 = Level
6	**IRQ14 ECL**—R/W. 0 = Edge 1 = Level
5	Reserved. Must be 0.
4	**IRQ12 ECL**—R/W. 0 = Edge 1 = Level
3	**IRQ11 ECL**—R/W. 0 = Edge 1 = Level
2	**IRQ10 ECL**—R/W. 0 = Edge 1 = Level
1	**IRQ9 ECL**—R/W. 0 = Edge 1 = Level
0	Reserved. Must be 0.

13.5 Advanced Programmable Interrupt Controller (APIC)

13.5.1 APIC Register Map

The APIC is accessed using an indirect addressing scheme. Two registers are visible by software for manipulation of most of the APIC registers. These registers are mapped into memory space. The address bits 19:12 of the address range are programmable through bits 7:0 of OIC register (Chipset Config Registers:Offset 31FEh) The registers are shown in Table 13-4.

Table 13-4. APIC Direct Registers

Address	Mnemonic	Register Name	Size	Type
FEC_ _0000h	IND	Index	8 bits	R/W
FEC_ _0010h	DAT	Data	32 bits	R/W
FEC_ _0040h	EOIR	EOI	32 bits	WO

Table 13-5 lists the registers which can be accessed within the APIC using the Index Register. When accessing these registers, accesses must be done one DWord at a time. For example, software should never access byte 2 from the Data register before accessing bytes 0 and 1. The hardware will not attempt to recover from a bad programming model in this case.

Table 13-5. APIC Indirect Registers

Index	Mnemonic	Register Name	Size	Type
00	ID	Identification	32 bits	R/W
01	VER	Version	32 bits	RO
02–0F	—	Reserved	—	RO
10–11	REDIR_TBL0	Redirection Table 0	64 bits	R/W, RO
12–13	REDIR_TBL1	Redirection Table 1	64 bits	R/W, RO
...	...	...	...	...
3E–3F	REDIR_TBL23	Redirection Table 23	64 bits	R/W, RO
40–FF	—	Reserved	—	RO

13.5.2 IND—Index Register

Memory Address FEC_ _0000h Attribute: R/W
Default Value: 00h Size: 8 bits

The Index Register will select which APIC indirect register to be manipulated by software. The selector values for the indirect registers are listed in Table 13-5. Software will program this register to select the desired APIC internal register.

Bit	Description
7:0	**APIC Index**—R/W. This is an 8-bit pointer into the I/O APIC register table.

13.5.3 DAT—Data Register

Memory Address FEC_ _0000h Attribute: R/W
Default Value: 00000000h Size: 32 bits

This is a 32-bit register specifying the data to be read or written to the register pointed to by the Index register. This register can only be accessed in dword quantities.

Bit	Description
7:0	**APIC Data**—R/W. This is a 32-bit register for the data to be read or written to the APIC indirect register (Figure 13-5) pointed to by the Index register (Memory Address FEC0_0000h).

13.5.4 EOIR—EOI Register

Memory Address FEC_ _0000h Attribute: R/W
Default Value: N/A Size: 32 bits

The EOI register is present to provide a mechanism to maintain the level triggered semantics for level-triggered interrupts issued on the parallel bus.

When a write is issued to this register, the I/O APIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the Remote_IRR bit (Index Offset 10h, bit 14) for that I/O Redirection Entry will be cleared.

Note: If multiple I/O Redirection entries, for any reason, assign the same vector for more than one interrupt input, each of those entries will have the Remote_IRR bit reset to 0. The interrupt which was prematurely reset will not be lost because if its input remained active when the Remote_IRR bit is cleared, the interrupt will be reissued and serviced at a later time. Note that only bits 7:0 are actually used. Bits 31:8 are ignored by the PCH.

Note: To provide for future expansion, the processor should always write a value of 0 to Bits 31:8.

Bit	Description
31:8	Reserved. To provide for future expansion, the processor should always write a value of 0 to Bits 31:8.
7:0	**Redirection Entry Clear**—WO. When a write is issued to this register, the I/O APIC will check this field, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the Remote_IRR bit for that I/O Redirection Entry will be cleared.

13.5.5 ID—Identification Register

Index Offset:	00h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

The APIC ID serves as a physical name of the APIC. The APIC bus arbitration ID for the APIC is derived from its I/O APIC ID. This register is reset to 0 on power-up reset.

Bit	Description
31:28	Reserved
27:24	**APIC ID**—R/W. Software must program this value before using the APIC.
23:16	Reserved
15	Scratchpad Bit.
14:0	Reserved

13.5.6 VER—Version Register

Index Offset:	01h	Attribute:	RO, R/WO
Default Value:	00170020h	Size:	32 bits

Each I/O APIC contains a hardwired Version Register that identifies different implementation of APIC and their versions. The maximum redirection entry information also is in this register, to let software know how many interrupt are supported by this APIC.

Bit	Description
31:24	Reserved
23:16	**Maximum Redirection Entries (MRE)—**R/WO. This is the entry number (0 being the lowest entry) of the highest entry in the redirection table. It is equal to the number of interrupt input pins minus one and is in the range 0 through 239. In the PCH this field is hardwired to 17h to indicate 24 interrupts. BIOS must write to this field after PLTRST# to lockdown the value. this allows BIOS to utilize some of the entries for its own purpose and thus advertising fewer IOxAPIC Redirection Entries to the operating system.
15	**Pin Assertion Register Supported (PRQ)**—RO. Indicate that the IOxAPIC does not implement the Pin Assertion Register.
14:8	Reserved
7:0	**Version (VS)**—RO. This is a version number that identifies the implementation version.

13.5.7 REDIR_TBL—Redirection Table

Index Offset:	10h–11h (vector 0) through 3E–3Fh (vector 23)	Attribute:	R/W, RO
Default Value:	Bit 16 = 1. All other bits undefined	Size:	64 bits each, (accessed as two 32 bit quantities)

The Redirection Table has a dedicated entry for each interrupt input pin. The information in the Redirection Table is used to translate the interrupt manifestation on the corresponding interrupt pin into an APIC message.

The APIC will respond to an edge triggered interrupt as long as the interrupt is held until after the acknowledge cycle has begun. Once the interrupt is detected, a delivery status bit internally to the I/O APIC is set. The state machine will step ahead and wait for an acknowledgment from the APIC unit that the interrupt message was sent. Only

then will the I/O APIC be able to recognize a new edge on that interrupt pin. That new edge will only result in a new invocation of the handler if its acceptance by the destination APIC causes the Interrupt Request Register bit to go from 0 to 1. (In other words, if the interrupt was not already pending at the destination.)

Bit	Description
63:56	**Destination**—R/W. If bit 11 of this entry is 0 (Physical), then bits 59:56 specifies an APIC ID. In this case, bits 63:59 should be programmed by software to 0. If bit 11 of this entry is 1 (Logical), then bits 63:56 specify the logical destination address of a set of processors.
55:48	**Extended Destination ID (EDID)**—RO. These bits are sent to a local APIC only when in Processor System Bus mode. They become bits 11:4 of the address.
47:17	Reserved
16	**Mask**—R/W. 0 = Not masked: An edge or level on this interrupt pin results in the delivery of the interrupt to the destination. 1 = Masked: Interrupts are not delivered nor held pending. Setting this bit after the interrupt is accepted by a local APIC has no effect on that interrupt. This behavior is identical to the device withdrawing the interrupt before it is posted to the processor. It is software's responsibility to deal with the case where the mask bit is set after the interrupt message has been accepted by a local APIC unit but before the interrupt is dispensed to the processor.
15	**Trigger Mode**—R/W. This field indicates the type of signal on the interrupt pin that triggers an interrupt. 0 = Edge triggered. 1 = Level triggered.
14	**Remote IRR**—R/W. This bit is used for level triggered interrupts; its meaning is undefined for edge triggered interrupts. 0 = Reset when an EOI message is received from a local APIC. 1 = Set when Local APIC/s accept the level interrupt sent by the I/O APIC.
13	**Interrupt Input Pin Polarity**—R/W. This bit specifies the polarity of each interrupt signal connected to the interrupt pins. 0 = Active high. 1 = Active low.
12	**Delivery Status**—RO. This field contains the current status of the delivery of this interrupt. Writes to this bit have no effect. 0 = Idle. No activity for this interrupt. 1 = Pending. Interrupt has been injected, but delivery is not complete.
11	**Destination Mode**—R/W. This field determines the interpretation of the Destination field. 0 = Physical. Destination APIC ID is identified by bits 59:56. 1 = Logical. Destinations are identified by matching bit 63:56 with the Logical Destination in the Destination Format Register and Logical Destination Register in each Local APIC.
10:8	**Delivery Mode**—R/W. This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are listed in the note below:
7:0	**Vector**—R/W. This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

Note: Delivery Mode encoding:

000 = Fixed. Deliver the signal on the INTR signal of all processor cores listed in the destination. Trigger Mode can be edge or level.

001 = Lowest Priority. Deliver the signal on the INTR signal of the processor core that is executing at the lowest priority among all the processors listed in the specified destination. Trigger Mode can be edge or level.

010 = SMI (System Management Interrupt). Requires the interrupt to be programmed as edge triggered. The vector information is ignored but must be programmed to all 0s for future compatibility: **not supported**

011 = Reserved

100 = NMI. Deliver the signal on the NMI signal of all processor cores listed in the destination. Vector information is ignored. NMI is treated as an edge triggered interrupt even if it is programmed as level triggered. For proper operation this redirection table entry must be programmed to edge triggered. The NMI delivery mode does not set the RIRR bit. If the redirection table is incorrectly set to level, the loop count will continue counting through the redirection table addresses. Once the count for the NMI pin is reached again, the interrupt will be sent again: **not supported**

101 = INIT. Deliver the signal to all processor cores listed in the destination by asserting the INIT signal. All addressed local APICs will assume their INIT state. INIT is always treated as an edge triggered interrupt even if programmed as level triggered. For proper operation this redirection table entry must be programmed to edge triggered. The INIT delivery mode does not set the RIRR bit. If the redirection table is incorrectly set to level, the loop count will continue counting through the redirection table addresses. Once the count for the INIT pin is reached again, the interrupt will be sent again: **not supported**

110 = Reserved

111 = ExtINT. Deliver the signal to the INTR signal of all processor cores listed in the destination as an interrupt that originated in an externally connected 8259A compatible interrupt controller. The INTA cycle that corresponds to this ExtINT delivery will be routed to the external controller that is expected to supply the vector. Requires the interrupt to be programmed as edge triggered.

13.6 Real Time Clock Registers

13.6.1 I/O Register Address Map

The RTC internal registers and RAM are organized as two banks of 128 bytes each, called the standard and extended banks. The first 14 bytes of the standard bank contain the RTC time and date information along with four registers, A–D, that are used for configuration of the RTC. The extended bank contains a full 128 bytes of battery backed SRAM, and will be accessible even when the RTC module is disabled (using the RTC configuration register). Registers A–D do not physically exist in the RAM.

All data movement between the host processor and the real-time clock is done through registers mapped to the standard I/O space. The register map appears in Table 13-6.

Table 13-6. RTC I/O Registers

I/O Locations	If U128E bit = 0	Function
70h and 74h	Also alias to 72h and 76h	Real-Time Clock (Standard RAM) Index Register
71h and 75h	Also alias to 73h and 77h	Real-Time Clock (Standard RAM) Target Register
72h and 76h		Extended RAM Index Register (if enabled)
73h and 77h		Extended RAM Target Register (if enabled)

Notes:

1. I/O locations 70h and 71h are the standard legacy location for the real-time clock. The map for this bank is shown in Table 13-7. Locations 72h and 73h are for accessing the extended RAM. The extended RAM bank is also accessed using an indexed scheme. I/O address 72h is used as the address pointer and I/O address 73h is used as the data register. Index addresses above 127h are not valid. If the extended RAM is not needed, it may be disabled.
2. Software must preserve the value of bit 7 at I/O addresses 70h and 74h. When writing to this address, software must first read the value, and then write the same value for bit 7 during the sequential address write. Note that port 70h is not directly readable. The only way to read this register is through Alt Access mode. Although RTC Index bits 6:0 are readable from port 74h, bit 7 will always return 0. If the NMI# enable is not changed during normal operation, software can alternatively read this bit once and then retain the value for all subsequent writes to port 70h.

13.6.2 Indexed Registers

The RTC contains two sets of indexed registers that are accessed using the two separate Index and Target registers (70/71h or 72/73h), as shown in Table 13-7.

Table 13-7. RTC (Standard) RAM Bank

Index	Name
00h	Seconds
01h	Seconds Alarm
02h	Minutes
03h	Minutes Alarm
04h	Hours
05h	Hours Alarm
06h	Day of Week
07h	Day of Month
08h	Month
09h	Year
0Ah	Register A
0Bh	Register B
0Ch	Register C
0Dh	Register D
0Eh–7Fh	114 Bytes of User RAM

13.6.2.1 RTC_REGA—Register A

RTC Index:	0A	Attribute:	R/W
Default Value:	Undefined	Size:	8-bit
Lockable:	No	Power Well:	RTC

This register is used for general configuration of the RTC functions. None of the bits are affected by RSMRST# or any other PCH reset signal.

Bit	Description
7	**Update In Progress (UIP)—**R/W. This bit may be monitored as a status flag. 0 = The update cycle will not start for at least 488 µs. The time, calendar, and alarm information in RAM is always available when the UIP bit is 0. 1 = The update is soon to occur or is in progress.
6:4	**Division Chain Select (DV[2:0])—**R/W. These three bits control the divider chain for the oscillator, and are not affected by RSMRST# or any other reset signal. 010 = Normal Operation 11X = Divider Reset 101 = Bypass 15 stages (test mode only) 100 = Bypass 10 stages (test mode only) 011 = Bypass 5 stages (test mode only) 001 = Invalid 000 = Invalid
3:0	**Rate Select (RS[3:0])—**R/W. Selects one of 13 taps of the 15 stage divider chain. The selected tap can generate a periodic interrupt if the PIE bit is set in Register B. Otherwise this tap will set the PF flag of Register C. If the periodic interrupt is not to be used, these bits should all be set to 0. RS3 corresponds to bit 3. 0000 = Interrupt never toggles 0001 = 3.90625 ms 0010 = 7.8125 ms 0011 = 122.070 µs 0100 = 244.141 µs 0101 = 488.281 µs 0110 = 976.5625 µs 0111 = 1.953125 ms 1000 = 3.90625 ms 1001 = 7.8125 ms 1010 = 15.625 ms 1011 = 31.25 ms 1100 = 62.5 ms 1101 = 125 ms 1110 = 250 ms 1111= 500 ms

13.6.2.2 RTC_REGB—Register B (General Configuration)

RTC Index:	0Bh	Attribute:	R/W
Default Value:	U0U00UUU (U: Undefined)	Size:	8-bit
Lockable:	No	Power Well:	RTC

Bit	Description
7	**Update Cycle Inhibit (SET)—**R/W. Enables/Inhibits the update cycles. This bit is not affected by RSMRST# nor any other reset signal. 0 = Update cycle occurs normally once each second. 1 = A current update cycle will abort and subsequent update cycles will not occur until SET is returned to 0. When set is one, the BIOS may initialize time and calendar bytes safely. ***Note:*** This bit should be set then cleared early in BIOS POST after each powerup directly after coin-cell battery insertion.
6	**Periodic Interrupt Enable (PIE)**—R/W. This bit is cleared by RSMRST#, but not on any other reset. 0 = Disable. 1 = Enable. Allows an interrupt to occur with a time base set with the RS bits of register A.
5	**Alarm Interrupt Enable (AIE)**—R/W. This bit is cleared by RTCRST#, but not on any other reset. 0 = Disable. 1 = Enable. Allows an interrupt to occur when the AF is set by an alarm match from the update cycle. An alarm can occur once a second, one an hour, once a day, or one a month.
4	**Update-Ended Interrupt Enable (UIE)**—R/W. This bit is cleared by RSMRST#, but not on any other reset. 0 = Disable. 1 = Enable. Allows an interrupt to occur when the update cycle ends.
3	**Square Wave Enable (SQWE)—**R/W. This bit serves no function in the PCH. It is left in this register bank to provide compatibility with the Motorola 146818B. The PCH has no SQW pin. This bit is cleared by RSMRST#, but not on any other reset.
2	**Data Mode (DM)—**R/W. This bit specifies either binary or BCD data representation. This bit is not affected by RSMRST# nor any other reset signal. 0 = BCD 1 = Binary
1	**Hour Format (HOURFORM)—**R/W. This bit indicates the hour byte format. This bit is not affected by RSMRST# nor any other reset signal. 0 = Twelve-hour mode. In twelve-hour mode, the seventh bit represents AM as 0 and PM as one. 1 = Twenty-four hour mode.
0	**Daylight Savings Legacy Software Support (DSLSWS)—**R/W. Daylight savings functionality is no longer supported. This bit is used to maintain legacy software support and has no associated functionality. If BUC.DSO bit is set, the DSLSWS bit continues to be R/W.

13.6.2.3 RTC_REGC—Register C (Flag Register)

RTC Index:	0Ch	Attribute:	RO
Default Value:	00U00000 (U: Undefined)	Size:	8-bit
Lockable:	No	Power Well:	RTC

Writes to Register C have no effect.

Bit	Description
7	**Interrupt Request Flag (IRQF)—**RO. IRQF = (PF * PIE) + (AF * AIE) + (UF *UFE). This bit also causes the RTC Interrupt to be asserted. This bit is cleared upon RSMRST# or a read of Register C.
6	**Periodic Interrupt Flag (PF)—**RO. This bit is cleared upon RSMRST# or a read of Register C. 0 = If no taps are specified using the RS bits in Register A, this flag will not be set. 1 = Periodic interrupt Flag will be 1 when the tap specified by the RS bits of register A is 1.
5	**Alarm Flag (AF)—**RO. 0 = This bit is cleared upon RTCRST# or a read of Register C. 1 = Alarm Flag will be set after all Alarm values match the current time.
4	**Update-Ended Flag (UF)—**RO. 0 = The bit is cleared upon RSMRST# or a read of Register C. 1 = Set immediately following an update cycle for each second.
3:0	Reserved. Will always report 0.

13.6.2.4 RTC_REGD—Register D (Flag Register)

RTC Index:	0Dh	Attribute:	R/W
Default Value:	10UUUUUU (U: Undefined)	Size:	8-bit
Lockable:	No	Power Well:	RTC

Bit	Description
7	**Valid RAM and Time Bit (VRT)**—R/W. 0 = This bit should always be written as a 0 for write cycle, however it will return a 1 for read cycles. 1 = This bit is hardwired to 1 in the RTC power well.
6	Reserved. This bit always returns a 0 and should be set to 0 for write cycles.
5:0	**Date Alarm**—R/W. These bits store the date of month alarm value. If set to 000000b, then a don't care state is assumed. The host must configure the date alarm for these bits to do anything, yet they can be written at any time. If the date alarm is not enabled, these bits will return 0s to mimic the functionality of the Motorola 146818B. These bits are not affected by any reset assertion.

13.7 Processor Interface Registers

Table 13-8 is the register address map for the processor interface registers.

Table 13-8. Processor Interface PCI Register Address Map

Offset	Mnemonic	Register Name	Default	Type
61h	NMI_SC	NMI Status and Control	00h	R/W, RO
70h	NMI_EN	NMI Enable	80h	R/W (special)
92h	PORT92	Fast A20 and Init	00h	R/W
F0h	COPROC_ERR	Coprocessor Error	00h	WO
CF9h	RST_CNT	Reset Control	00h	R/W

13.7.1 NMI_SC—NMI Status and Control Register

I/O Address:	61h	Attribute:	R/W, RO
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7	**SERR# NMI Source Status (SERR#_NMI_STS)—**RO. 1 = Bit is set if a PCI agent detected a system error and pulses the PCI SERR# line and if bit 2 (PCI_SERR_EN) is cleared. This interrupt source is enabled by setting bit 2 to 0. To reset the interrupt, set bit 2 to 1 and then set it to 0. When writing to port 61h, this bit must be 0. ***Note:*** This bit is set by any of the PCH internal sources of SERR; this includes SERR assertions forwarded from the secondary PCI bus, errors on a PCI Express port, or other internal functions that generate SERR#.
6	**IOCHK# NMI Source Status (IOCHK_NMI_STS)—**RO. 1 = Bit is set if an LPC agent (using SERIRQ) asserted IOCHK# and if bit 3 (IOCHK_NMI_EN) is cleared. This interrupt source is enabled by setting bit 3 to 0. To reset the interrupt, set bit 3 to 1 and then set it to 0. When writing to port 61h, this bit must be a 0.
5	**Timer Counter 2 OUT Status (TMR2_OUT_STS)—**RO. This bit reflects the current state of the 8254 counter 2 output. Counter 2 must be programmed following any PCI reset for this bit to have a determinate value. When writing to port 61h, this bit must be a 0.
4	**Refresh Cycle Toggle (REF_TOGGLE)—**RO. This signal toggles from either 0 to 1 or 1 to 0 at a rate that is equivalent to when refresh cycles would occur. When writing to port 61h, this bit must be a 0.
3	**IOCHK# NMI Enable (IOCHK_NMI_EN)—**R/W. 0 = Enabled. 1 = Disabled and cleared.
2	**PCI SERR# Enable (PCI_SERR_EN)—**R/W. 0 = SERR# NMIs are enabled. 1 = SERR# NMIs are disabled and cleared.
1	**Speaker Data Enable (SPKR_DAT_EN)—**R/W. 0 = SPKR output is a 0. 1 = SPKR output is equivalent to the Counter 2 OUT signal value.
0	**Timer Counter 2 Enable (TIM_CNT2_EN)—**R/W. 0 = Disable 1 = Enable

13.7.2 NMI_EN—NMI Enable (and Real Time Clock Index) Register

I/O Address:	70h	Attribute:	R/W (special)
Default Value:	80h	Size:	8-bit
Lockable:	No	Power Well:	Core

Note: The RTC Index field is write-only for normal operation. This field can only be read in Alt-Access Mode. Note, however, that this register is aliased to Port 74h (documented in), and all bits are readable at that address.

Bits	Description
7	**NMI Enable (NMI_EN)—**R/W (special). 0 = Enable NMI sources. 1 = Disable All NMI sources.
6:0	**Real Time Clock Index Address (RTC_INDX)—**R/W (special). This data goes to the RTC to select which register or CMOS RAM address is being accessed.

13.7.3 PORT92—Fast A20 and Init Register

I/O Address:	92h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:2	Reserved
1	**Alternate A20 Gate (ALT_A20_GATE)—**R/W. This bit is Or'd with the A20GATE input signal to generate A20M# to the processor. 0 = A20M# signal can potentially go active. 1 = This bit is set when INIT# goes active.
0	**INIT_NOW**—R/W. When this bit transitions from a 0 to a 1, the PCH will force INIT# active for 16 PCI clocks.

13.7.4 COPROC_ERR—Coprocessor Error Register

I/O Address:	F0h	Attribute:	WO
Default Value:	00h	Size:	8-bits
Lockable:	No	Power Well:	Core

Bits	Description
7:0	**Coprocessor Error (COPROC_ERR)**—WO. Any value written to this register will cause IGNNE# to go active, if FERR# had generated an internal IRQ13. For FERR# to generate an internal IRQ13, the CEN bit must be 1.

13.7.5 RST_CNT—Reset Control Register

I/O Address:	CF9h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:4	Reserved
3	**Full Reset (FULL_RST)—**R/W. This bit is used to determine the states of SLP_S3#, SLP_S4#, and SLP_S5# after a CF9 hard reset (SYS_RST =1 and RST_CPU is set to 1), after PCH_PWROK going low (with RSMRST# high), or after two TCO timeouts. 0 = PCH will keep SLP_S3#, SLP_S4# and SLP_S5# high. 1 = PCH will drive SLP_S3#, SLP_S4# and SLP_S5# low for 3 – 5 seconds. ***Note:*** When this bit is set, it also causes the full power cycle (SLP_S3/4/5# assertion) in response to SYS_RESET#, PCH_PWROK#, and Watchdog timer reset sources.
2	**Reset Processor(RST_CPU)—**R/W. When this bit transitions from a 0 to a 1, it initiates a hard or soft reset, as determined by the SYS_RST bit (bit 1 of this register).
1	**System Reset (SYS_RST)—**R/W. This bit is used to determine a hard or soft reset to the processor. 0 = When RST_CPU bit goes from 0 to 1, the PCH performs a soft reset by activating INIT# for 16 PCI clocks. 1 = When RST_CPU bit goes from 0 to 1, the PCH performs a hard reset by activating PLTRST# 0active for a minimum of about 1 milliseconds. In this case, SLP_S3#, SLP_S4# and SLP_S5# state (assertion or deassertion) depends on FULL_RST bit setting. The PCH main power well is reset when this bit is 1. It also resets the resume well bits (except for those noted throughout the EDS).
0	Reserved

13.8 Power Management Registers

The power management registers are distributed within the PCI Device 31: Function 0 space, as well as a separate I/O range. Each register is described below. Unless otherwise indicated, bits are in the main (core) power well.

Bits not explicitly defined in each register are assumed to be reserved. When writing to a reserved bit, the value should always be 0. Software should not attempt to use the value read from a reserved bit, as it may not be consistently 1 or 0.

13.8.1 Power Management PCI Configuration Registers (PM—D31:F0)

Table 13-9 shows a small part of the configuration space for PCI Device 31: Function 0. It includes only those registers dedicated for power management. Some of the registers are only used for Legacy Power management schemes.

Table 13-9. Power Management PCI Register Address Map (PM—D31:F0)

Offset	Mnemonic	Register Name	Default	Type
A0h–A1h	GEN_PMCON_1	General Power Management Configuration 1	0000h	R/W, R/WO, RO
A2h	GEN_PMCON_2	General Power Management Configuration 2	00h	RO, R/WC, R/W
A4h–A5h	GEN_PMCON_3	General Power Management Configuration 3	4206h	R/W, R/WL
A6h	GEN_PMCON_LOCK	General Power Management Configuration Lock	00h	RO, R/WL, R/WS
A9h	CIR4	Chipset Initialization Register 4	03h	R/W
AAh	BM_BREAK_EN_2	BM_BREAK_EN Register #2	00h	R/W, RO
ABh	BM_BREAK_EN	BM_BREAK_EN	00h	R/W, RO
ACh	ETR3	Extended Test Mode Register 3	00000000h	R/W, R/WL
B8–BBh	GPI_ROUT	GPI Route Control	00000000h	R/W

13.8.1.1 GEN_PMCON_1—General PM Configuration 1 Register (PM—D31:F0)

Offset Address:	A0h	Attribute:	R/W, RO, R/WO
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI, Legacy
		Power Well:	Core

Bit	Description
15:12	Reserved
11	**GEN_PMCON_1 Field 1**—R/W. BIOS must program this field to 1b.
10	**BIOS_PCI_EXP_EN**—R/W. This bit acts as a global enable for the SCI associated with the PCI Express* ports. 0 = The various PCI Express ports and processor cannot cause the PCI_EXP_STS bit to go active. 1 = The various PCI Express ports and processor can cause the PCI_EXP_STS bit to go active.
9	**PWRBTN_LVL**—RO. This bit indicates the current state of the PWRBTN# signal. 0 = Low. 1 = High.
8:5	Reserved
4	**SMI_LOCK—**R/WS. When this bit is set, writes to the GLB_SMI_EN bit (PMBASE + 30h, bit 0) will have no effect. Once the SMI_LOCK bit is set, writes of 0 to SMI_LOCK bit will have no effect (that is., once set, this bit can only be cleared by PLTRST#).
3:2	Reserved
1:0	**Periodic SMI# Rate Select (PER_SMI_SEL)**—R/W. Set by software to control the rate at which periodic SMI# is generated. 00 = 64 seconds 01 = 32 seconds 10 = 16 seconds 11 = 8 seconds

13.8.1.2 GEN_PMCON_2—General PM Configuration 2 Register (PM—D31:F0)

Offset Address:	A2h	Attribute:	RO, R/WC, R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI, Legacy
		Power Well:	Resume

Bit	Description
7	**DRAM Initialization Bit**—R/W. This bit does not affect hardware functionality in any way. BIOS is expected to set this bit prior to starting the DRAM initialization sequence and to clear this bit after completing the DRAM initialization sequence. BIOS can detect that a DRAM initialization sequence was interrupted by a reset by reading this bit during the boot sequence. • If the bit is 1, then the DRAM initialization was interrupted. • This bit is reset by the assertion of the RSMRST# pin.
6	Reserved
5	**Memory Placed in Self-Refresh (MEM_SR)**—RO. • If the bit is 1, DRAM should have remained powered and held in Self-Refresh through the last power state transition (that is, the last time the system left S0). • This bit is reset by the assertion of the RSMRST# pin.
4	**System Reset Status (SRS)—**R/WC. Software clears this bit by writing a 1 to it. 0 = SYS_RESET# button Not pressed. 1 = PCH sets this bit when the SYS_RESET# button is pressed. BIOS is expected to read this bit and clear it, if it is set. ***Notes:*** 1. This bit is also reset by RSMRST# and CF9h resets. 2. The SYS_RESET# is implemented in the Main power well. This pin must be properly isolated and masked to prevent incorrectly setting this Suspend well status bit.
3	**Processor Thermal Trip Status (CTS)—**R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set when PLTRST# is inactive and THRMTRIP# goes active while the system is in an S0 or S1 state. ***Notes:*** 1. This bit is also reset by RSMRST#, and CF9h resets. It is not reset by the shutdown and reboot associated with the Processor THRMTRIP# event. 2. The CF9h reset in the description refers to CF9h type core well reset which includes SYS_RESET#, PCH_PWROK/SYS_PWROK low, SMBus hard reset, TCO Timeout. This type of reset will clear CTS bit.
2	**Minimum SLP_S4# Assertion Width Violation Status**—R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Hardware sets this bit when the SLP_S4# assertion width is less than the time programmed in the SLP_S4# Minimum Assertion Width field (D31:F0:Offset A4h:bits 5:4). The PCH begins the timer when SLP_S4# is asserted during S4/S5 entry or when the RSMRST# input is deasserted during SUS well power-up. Note that this bit is functional regardless of the values in the SLP_S4# Assertion Stretch Enable (D31:F0:Offset A4h:bit 3) and in the Disable SLP Stretching after SUS Well Power Up (D31:F0:Offset A4h:bit 12). ***Note:*** This bit is reset by the assertion of the RSMRST# pin, but can be set in some cases before the default value is readable.
1	**SYS_PWROK Failure (SYSPWR_FLR)—**R/WC. 0 = This bit will be cleared only be software writing a 1 back to the bit or by SUS well power loss. ***Note:*** This bit will be set any time SYS_PWROK drops unexpectedly when the system was in S0 or S1 state.
0	**PCH_PWROK Failure (PWROK_FLR)—**R/WC. 0 = This bit will be cleared only be software writing a 1 back to the bit or by SUS well power loss. 1 = This bit will be set any time PCH_PWROK goes low when the system was in S0 or S1 state. ***Note:*** See Chapter 5.14.9.3 for more details about the PCH_PWROK pin functionality.

13.8.1.3 GEN_PMCON_3—General PM Configuration 3 Register (PM—D31:F0)

Offset Address:	A4h	Attribute:	R/W, R/WC
Default Value:	4206h	Size:	16-bit
Lockable:	No	Usage:	ACPI, Legacy
		Power Well:	RTC, SUS

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>15</td><td>
PME B0 S5 Disable (PME_B0_S5_DIS)—R/W. When set to '1', this bit blocks wake events from PME_B0_STS in S5, regardless of the state of PME_B0_EN. When cleared (default), wake events from PME_B0_STS are allowed in S5 if PME_B0_EN = '1'.
Wakes from power states other than S5 are not affected by this policy bit.
The net effect of setting PME_B0_S5_DIS = '1' is described by the truth table below:
Y = Wake; N = Don't wake; B0 = PME_B0_EN; OV = WOL Enable Override
<table>
<tr><th>B0/OV</th><th>S1/S3/S4</th><th>S5</th></tr>
<tr><td>00</td><td>N</td><td>N</td></tr>
<tr><td>01</td><td>N</td><td>Y (LAN only)</td></tr>
<tr><td>11</td><td>Y (all PME B0 sources)</td><td>Y (LAN only)</td></tr>
<tr><td>01</td><td>Y (all PME B0 sources)</td><td>N</td></tr>
</table>
This bit is cleared by the RTCRST# pin.
</td></tr>
<tr><td>14</td><td>
SUS Well Power Failure (SUS_PWR_FLR)—R/WC.
0 = Software writes a 1 to this bit to clear it.
1 = This bit is set to '1' whenever SUS well power is lost, as indicated by RSMRST# assertion.
Note: This bit is in the SUS well, and defaults to '1' based on RSMRST# assertion (not cleared by any type of reset).
</td></tr>
<tr><td>13</td><td>
WOL Enable Override(WOL_EN_OVRD)—R/W.
0 = WOL policies are determined by PMEB0 enable bit and appropriate LAN status bits
1 = Enable appropriately configured integrated LAN to wake the system in S5 only regardless of the value in the PME_B0_EN bit in the GPE0_EN register.
Note: This bit is cleared by the RTCRST# pin.
</td></tr>
<tr><td>12</td><td>
Disable SLP Stretching After SUS Well Power Up (DIS_SLP_STRCH_SUS_UP): R/W
0 = Enables stretching on SLP signals after SUS power failure as enabled and configured in other fields.
1 = Disables stretching on SLP signals when powering up after a SUS well power loss. regardless of the state of the SLP_S4# Assertion Stretch Enable (bit 3).
This bit is cleared by the RTCRST# pin.
Notes:
1. This field is RO when the SLP Stretching Policy Lock-Down bit is set.
2. If this bit is cleared, SLP stretch timers start on SUS well power up (the PCH has no ability to count stretch time while the SUS well is powered down).
3. This policy bit has a different effect on SLP_SUS# stretching than on the other SLP_* pins since SLP_SUS# is the control signal for one of the scenarios where SUS well power is lost (Deep S4/S5). The effect of setting this bit to '1' on:
— SLP_S3# and SLP_S4# stretching: disabled after any SUS power loss.
— SLP_SUS# stretching: disabled after G3, but no impact on Deep S4/S5.
</td></tr>
<tr><td>11:10</td><td>
SLP_S3# Minimum Assertion Width: R/W This 2-bit value indicates the minimum assertion width of the SLP_S3# signal to ensure that the Main power supplies have been fully power-cycled.
Valid Settings are:
00 = 60 us
01 = 1 ms
10 = 50 ms
11 = 2 s
This bit is cleared by the RSMRST# pin.
Note: This field is RO when the SLP Stretching Policy Lock-Down bit is set.
</td></tr>
<tr><td>9</td><td>
General Reset Status (GEN_RST_STS)—R/WC. This bit is set by hardware whenever PLTRST# asserts for any reason other than going into a software-entered sleep state (using PM1CNT.SLP_EN write) or a suspend well power failure (RSMRST# pin assertion).
BIOS is expected to consult and then write a 1 to clear this bit during the boot flow before determining what action to take based on PM1_STS.WAK_STS = 1. If GEN_RST_STS = '1', the cold reset boot path should be followed rather than the resume path, regardless of the setting of WAK_STS.
This bit is cleared by the RSMRST# pin.
</td></tr>
</table>

Bit	Description
8	**SLP_LAN# Default Value (SLP_LAN_DEFAULT)—**R/W. This bit specifies the value to drive on the SLP_LAN# pin when in Sx/Moff and Intel ME FW nor host BIOS has configured SLP_LAN# as an output. When this bit is set to 1 SLP_LAN# will default to be driven high, when set to 0 SLP_LAN# will default to be driven low. This bit will always determine SLP_LAN# behavior when in S4/S5/Moff after SUS power loss, in S5/Moff after a host partition reset with power down and when in S5/Moff due to an unconditional power down. This bit is cleared by RTCRST#.
7:6	**SWSMI_RATE_SEL**—R/W. This field indicates when the SWSMI timer will time out. Valid values are: 00 = 1.5 ms ± 0.6 ms 01 = 16 ms ± 4 ms 10 = 32 ms ± 4 ms 11 = 64 ms ± 4 ms These bits are not cleared by any type of reset except RTCRST#.
5:4	**SLP_S4# Minimum Assertion Width**—R/W. This field indicates the minimum assertion width of the SLP_S4# signal to ensure that the DRAM modules have been safely power-cycled. Valid values are: 11 = 1 second 10 = 2 seconds 01 = 3 seconds 00 = 4 seconds This value is used in two ways: 1. If the SLP_S4# assertion width is ever shorter than this time, a status bit is set for BIOS to read when S0 is entered. 2. If enabled by bit 3 in this register, the hardware will prevent the SLP_S4# signal from deasserting within this minimum time period after asserting. RTCRST# forces this field to the conservative default state (00b). ***Notes:*** 1. This field is RO when the SLP Stretching Policy Lock-Down bit is set. 2. Note that the logic that measures this time is in the suspend power well. Therefore, when leaving a G3 or Deep S4/S5 state, the minimum time is measured from the deassertion of the internal suspend well reset (unless the "Disable SLP Stretching After SUS Well Power Up" bit is set).
3	**SLP_S4# Assertion Stretch Enable**—R/W. 0 = The SLP_S4# minimum assertion time is defined in Power Sequencing and Reset Signal Timings table. 0 = The SLP_S4# signal minimally assert for the time specified in bits 5:4 of this register. This bit is cleared by RTCRST#. ***Note:*** This bit is RO when the SLP Stretching Policy Lock-Down bit is set.
2	**RTC Power Status (RTC_PWR_STS)**—R/W. This bit is set when RTCRST# indicates a weak or missing battery. The bit is not cleared by any type of reset. The bit will remain set until the software clears it by writing a 0 back to this bit position.
1	**Power Failure (PWR_FLR)—**R/WC. This bit is in the DeepS4/S5 well and defaults to 1 based on DPWROK deassertion (not cleared by any type of reset). 0 = Indicates that the trickle current has not failed since the last time the bit was cleared. Software clears this bit by writing a 1 to it. 1 = Indicates that the trickle current (from the main battery or trickle supply) was removed or failed. ***Note:*** Clearing CMOS in a PCH-based platform can be done by using a jumper on RTCRST# or GPI. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low.
0	**AFTERG3_EN**—R/W. This bit determines what state to go to when power is re-applied after a power failure (G3 state). This bit is in the RTC well and is only cleared by RTCRST# assertion. 0 = System will return to S0 state (boot) after power is re-applied. 1 = System will return to the S5 state (except if it was in S4, in which case it will return to S4). In the S5 state, the only enabled wake event is the Power Button or any enabled wake event that was preserved through the power failure.

Note: RSMRST# is sampled using the RTC clock. Therefore, low times that are less than one RTC clock period may not be detected by the PCH.

13.8.1.4 GEN_PMCON_LOCK—General Power Management Configuration Lock Register

Offset Address:	A6h	Attribute:	RO, R/WLO
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI
Power Well:	Core		

Bit	Description
7:3	Reserved
2	**SLP Stretching Policy Lock-Down (SLP_STR_POL_LOCK)—**R/WLO. R/WLO. When set to 1, this bit locks down the Disable SLP Stretching After SUS Well Power Up, SLP_S3# Minimum Assertion Width, SLP_S4# Minimum Assertion Width, SLP_S4# Assertion Stretch Enable bits in the GEN_PMCON_3 register, making them read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. This bit is cleared by platform reset.
1	**ACPI_BASE_LOCK—**R/WLO. When set to 1, this bit locks down the ACPI Base Address Register (ABASE) at offset 40h. The Base Address Field becomes read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset.
0	Reserved

13.8.1.5 Chipset Initialization Register 4 (PM—D31:F0)

Offset Address:	A9h	Attribute:	R/W
Default Value:	03h	Size:	8-bit
Lockable:	No	Usage:	ACPI, Legacy
Power Well:	Core		

Bit	Description
7:0	**CIR4 Field 1**—R/W. BIOS must program this field to 47h.

13.8.1.6 BM_BREAK_EN Register #2 (PM—D31:F0)

Offset Address:	AAh	Attribute:	R/W, RO
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI, Legacy
Power Well:	Core		

Bit	Description
7:1	Reserved
0	**SATA3 Break Enable (SATA3_BREAK_EN)—**R/W 0 = SATA3 traffic will not cause BM_STS to be set. 1 = SATA3 traffic will cause BM_STS to be set.

13.8.1.7 BM_BREAK_EN Register (PM—D31:F0)

Offset Address:	ABh	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI, Legacy
Power Well:	Core		

Bit	Description
7	**Storage Breka Enable (STORAGE_BREAK_EN)—**R/W. 0 = Serial ATA traffic will not cause BM_STS to be set.. 1 = Serial ATA traffic will cause BM_STS to be set.
6	**PCIE_BREAK_EN—**R/W. 0 = PCI Express* traffic will not cause BM_STS to be set.. 1 = PCI Express traffic will cause BM_STS to be set.
5	**PCI_BREAK_EN—**R/W. 0 = PCI traffic will not cause BM_STS to be set.. 1 = PCI traffic will cause BM_STS to be set.
4:3	Reserved
2	**EHCI_BREAK_EN—**R/W. 0 = EHCI traffic will not cause BM_STS to be set.. 1 = EHCI traffic will cause BM_STS to be set.
1	Reserved
0	**HDA_BREAK_EN—**R/W. 0 = Intel® High Definition Audio traffic will not cause BM_STS to be set. 1 = Intel® High Definition Audio traffic will cause BM_STS to be set.

13.8.1.8 PMIR—Power Management Initialization Register (PM—D31:F0)

Offset Address:	ACh	Attribute:	R/W, R/WLO
Default Value:	00000000h	Size:	32-bit
Lockable:	Yes	Power Well:	Resume

Bit	Description
31	**CF9h Lockdown (CF9LOCK)—**R/WLO. 0 = CF9h Global Reset bit R/W. 1 = CF9h Global Reset bit RO. When set, this bit becomes RO and is reset only by a CF9h reset or RSMRST# assertion (other reset types are not applicable). In manufacturing/debug environments this bit should be left as default 0b. In all other environments, BIOS must program this bit to 1b.
30:21	Reserved.
20	**CF9h Global Reset (CF9GR)**—R/WL. 0 = A CF9h write of 6h or Eh will reset only the host partition. 1 = A CF9h write of 6h or Eh will cause a Global reset of both the host and Intel® ME partitions. This bit is locked by the CF9h Lockdown (CF9LOCK) bit. This bit field is not reset by a CF9h reset.
19:0	Reserved

13.8.1.9 GPIO_ROUT—GPIO Routing Control Register (PM—D31:F0)

Offset Address:	B8h–BBh	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Power Well:	Resume

Bit	Description
31:30	**GPIO15 Route**—R/W. See bits 1:0 for description.
Same pattern for GPIO14 through GPIO3	
5:4	**GPIO2 Route**—R/W. See bits 1:0 for description.
3:2	**GPIO1 Route**—R/W. See bits 1:0 for description.
1:0	**GPIO0 Route**—R/W. GPIO can be routed to cause an NMI, SMI# or SCI when the GPIO[n]_STS bit is set. If the GPIO0 is not set to an input, this field has no effect. If the system is in an S1–S5 state and if the GPE0_EN bit is also set, then the GPIO can cause a Wake event, even if the GPIO is NOT routed to cause an NMI, SMI# or SCI. 00 = No effect. 01 = SMI# (if corresponding ALT_GPI_SMI_EN bit is also set) 10 = SCI (if corresponding GPE0_EN bit is also set) 11 = NMI (If corresponding GPI_NMI_EN is also set)

Note: GPIOs that are not implemented will not have the corresponding bits implemented in this register.

13.8.2 APM I/O Decode

Table 13-10 shows the I/O registers associated with APM support. This register space is enabled in the PCI Device 31: Function 0 space (APMDEC_EN), and cannot be moved (fixed I/O location).

Table 13-10. APM Register Map

Address	Mnemonic	Register Name	Default	Type
B2h	APM_CNT	Advanced Power Management Control Port	00h	R/W
B3h	APM_STS	Advanced Power Management Status Port	00h	R/W

13.8.2.1 APM_CNT—Advanced Power Management Control Port Register

I/O Address:	B2h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	Legacy Only
Power Well:	Core		

Bit	Description
7:0	Used to pass an APM command between the operating system and the SMI handler. Writes to this port not only store data in the APMC register, but also generates an SMI# when the APMC_EN bit is set.

13.8.2.2 APM_STS—Advanced Power Management Status Port Register

I/O Address:	B3h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	Legacy Only
Power Well:	Core		

Bit	Description
7:0	Used to pass data between the operating system and the SMI handler. Basically, this is a scratchpad register and is not affected by any other register or function (other than a PCI reset).

13.8.3 Power Management I/O Registers

Table 13-11 shows the registers associated with ACPI and Legacy power management support. These registers locations are all offsets from the ACPI base address defined in the PCI Device 31: Function 0 space (PMBASE), and can be moved to any 128-byte aligned I/O location. In order to access these registers, the ACPI Enable bit(ACPI_EN) must be set. The registers are defined to be compliant with the ACPI 3.0b specification, and generally use the same bit names.

Note: All reserved bits and registers will always return 0 when read, and will have no effect when written.

Table 13-11. ACPI and Legacy I/O Register Map

PMBASE + Offset	Mnemonic	Register Name		Default	Type
00h–01h	PM1_STS	PM1 Status		0000h	R/WC
02h–03h	PM1_EN	PM1 Enable		0000h	R/W
04h–07h	PM1_CNT	PM1 Control		00000000h	R/W, WO
08h–0Bh	PM1_TMR	PM1 Timer		xx000000h	RO
20–27h	GPE0_STS	General Purpose Event 0 Status		00000000 00000000h	R/WC
28–2Fh	GPE0_EN	General Purpose Event 0a Enables		00000000 00000000h	R/W
30h–33h	SMI_EN	SMI# Control and Enable		00000002h	R/W, WO, R/WO
34h–37h	SMI_STS	SMI Status		00000000h	R/WC, RO
38h–39h	ALT_GP_SMI_EN	Alternate GPI SMI Enable		0000h	R/W
3Ah–3Bh	ALT_GP_SMI_STS	Alternate GPI SMI Status		0000h	R/WC
42h	GPE_CNTL	General Purpose Event Control		00h	R/W
44h–45h	DEVTRAP_STS	Device Trap Status Status		0000h	R/WC
50h	PM2_CNT	Power Management 2 Control		00h	R/W
60h–7Fh	—	Reserved for TCO	—	—	—

13.8.3.1 PM1_STS—Power Management 1 Status Register

I/O Address:	PMBASE + 00h	Attribute:	R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Bits 0–7: Core, Bits 12–15: Resume Bit 11: RTC, Bits 8 and 10: DSW		

If bit 10 or 8 in this register is set, and the corresponding _EN bit is set in the PM1_EN register, then the PCH will generate a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the PCH will also generate an SCI if the SCI_EN bit is set, or an SMI# if the SCI_EN bit is not set.

Note: Bit 5 does not cause an SMI# or a wake event. Bit 0 does not cause a wake event but can cause an SMI# or SCI.

Bit	Description
15	**Wake Status (WAK_STS)—**R/WC. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST#. 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware when the system is in one of the sleep states (using the SLP_EN bit) and an enabled wake event occurs. Upon setting this bit, the PCH will transition the system to the ON state. If the AFTERG3_EN bit is not set and a power failure (such as removed batteries) occurs without the SLP_EN bit set, the system will return to an S0 state when power returns, and the WAK_STS bit will not be set. If the AFTERG3_EN bit is set and a power failure occurs without the SLP_EN bit having been set, the system will go into an S5 state when power returns, and a subsequent wake event will cause the WAK_STS bit to be set. Note that any subsequent wake event would have to be caused by either a Power Button press, or an enabled wake event that was preserved through the power failure (enable bit in the RTC well).
14	**PCI Express Wake Status (PCIEXPWAK_STS)—**R/WC. 0 = Software clears this bit by writing a 1 to it. If the WAKE# pin is still active during the write or the PME message received indication has not been cleared in the root port, then the bit will remain active (that is, all inputs to this bit are level-sensitive). 1 = This bit is set by hardware to indicate that the system woke due to a PCI Express wakeup event. This wakeup event can be caused by the PCI Express WAKE# pin being active or receipt of a PCI Express PME message at a root port. This bit is set only when one of these events causes the system to transition from a non-S0 system power state to the S0 system power state. This bit is set independent of the state of the PCIEXP_WAKE_DIS bit. ***Note:*** This bit does not itself cause a wake event or prevent entry to a sleeping state. Thus, if the bit is 1 and the system is put into a sleeping state, the system will not automatically wake.
13:12	Reserved
11	**Power Button Override Status (PWRBTNOR_STS)—**R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set any time a Power Button Override occurs (that is., the power button is pressed for at least 4 consecutive seconds), due to the corresponding bit in the SMBus slave message, Intel ME Initiated Power Button Override, Intel ME Initiated Host Reset with Power down or due to an internal thermal sensor catastrophic condition. The power button override causes an unconditional transition to the S5 state. The BIOS or SCI handler clears this bit by writing a 1 to it. This bit is not affected by hard resets using CF9h writes, and is not reset by RSMRST#. Thus, this bit is preserved through power failures. Note that if this bit is still asserted when the global SCI_EN is set then an SCI will be generated.
10	**RTC Status (RTC_STS)—**R/WC. This bit is not affected by hard resets caused by a CF9 write, but is reset by DPWROK. 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware when the RTC generates an alarm (assertion of the IRQ8# signal). Additionally if the RTC_EN bit (PMBASE + 02h, bit 10) is set, the setting of the RTC_STS bit will generate a wake event.
9	Reserved

Bit	Description
8	**Power Button Status (PWRBTN__STS)—**R/WC. This bit is not affected by hard resets caused by a CF9 write but is reset by DPWROK 0 = If the PWRBTN# signal is held low for more than 4 seconds, the hardware clears the PWRBTN_STS bit, sets the PWRBTNOR_STS bit, and the system transitions to the S5 state with only PWRBTN# enabled as a wake event. This bit can be cleared by software by writing a one to the bit position. 1 = This bit is set by hardware when the PWRBTN# signal is asserted Low, independent of any other enable bit. In the S0 state, while PWRBTN_EN and PWRBTN_STS are both set, an SCI (or SMI# if SCI_EN is not set) will be generated. In any sleeping state S1–S5, while PWRBTN_EN (PMBASE + 02h, bit 8) and PWRBTN_STS are both set, a wake event is generated. ***Note:*** If the PWRBTN_STS bit is cleared by software while the PWRBTN# signal is sell asserted, this will not cause the PWRBN_STS bit to be set. The PWRBTN# signal must go inactive and active again to set the PWRBTN_STS bit.
7:6	Reserved
5	**Global Status (GBL _STS)—**R/WC. 0 = The SCI handler should then clear this bit by writing a 1 to the bit location. 1 = Set when an SCI is generated due to BIOS wanting the attention of the SCI handler. BIOS has a corresponding bit, BIOS_RLS, which will cause an SCI and set this bit.
4	**Bus Master Status (BM_STS)**—R/WC. This bit will not cause a wake event, SCI or SMI#. 0 = Software clears this bit by writing a 1 to it. 1 = Set by the PCH when a PCH-visible bus master requests access to memory or the BM_BUSY# signal is active.
3:1	Reserved
0	**Timer Overflow Status (TMROF_STS)—**R/WC. 0 = The SCI or SMI# handler clears this bit by writing a 1 to the bit location. 1 = This bit gets set any time bit 22 of the 24-bit timer goes high (bits are numbered from 0 to 23). This will occur every 2.3435 seconds. When the TMROF_EN bit (PMBASE + 02h, bit 0) is set, then the setting of the TMROF_STS bit will additionally generate an SCI or SMI# (depending on the SCI_EN).

13.8.3.2 PM1_EN—Power Management 1 Enable Register

I/O Address:	PMBASE + 02h	Attribute:	RO; R/W
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Bits 0–7: Core, Bits 8–9, 11–15: Resume, Bit 10: RTC		

Bit	Description
15	Reserved
14	**PCI Express Wake Disable (PCIEXPWAK_DIS)—R**/W. Modification of this bit has no impact on the value of the PCIEXP_WAKE_STS bit. 0 = Inputs to the PCIEXP_WAKE_STS bit in the PM1 Status register enabled to wake the system. 1 = Inputs to the PCIEXP_WAKE_STS bit in the PM1 Status register disabled from waking the system.
13:11	Reserved
10	**RTC Alarm Enable (RTC_EN)—**R/W. This bit is in the RTC well to allow an RTC event to wake after a power failure. In addition to being cleared by RTCRST# assertion, the PCH also clears this bit due to a Power Button Override event, Intel ME Initiated Power Button Override, Intel ME Initiated Host Reset with Power down, SMBus unconditional power down, Processor thermal trip event, or due to an internal thermal sensor catastrophic condition. 0 = No SCI (or SMI#) or wake event is generated then RTC_STS (PMBASE + 00h, bit 10) goes active. 1 = An SCI (or SMI#) or wake event will occur when this bit is set and the RTC_STS bit goes active.
9	Reserved.
8	**Power Button Enable (PWRBTN_EN)—**R/W. This bit is used to enable the setting of the PWRBTN_STS bit to generate a power management event (SMI#, SCI). PWRBTN_EN has no effect on the PWRBTN_STS bit (PMBASE + 00h, bit 8) being set by the assertion of the power button. The Power Button is always enabled as a Wake event. 0 = Disable. 1 = Enable.
7:6	Reserved.
5	**Global Enable (GBL_EN)—**R/W. When both the GBL_EN and the GBL_STS bit (PMBASE + 00h, bit 5) are set, an SCI is raised. 0 = Disable. 1 = Enable SCI on GBL_STS going active.
4:1	Reserved.
0	**Timer Overflow Interrupt Enable (TMROF_EN)—**R/W. Works in conjunction with the SCI_EN bit (PMBASE + 04h, bit 0) as described below: TMROF_EN / SCI_EN / Effect when TMROF_STS is set 0 / X / No SMI# or SCI 1 / 0 / SMI# 1 / 1 / SCI

13.8.3.3 PM1_CNT—Power Management 1 Control

I/O Address:	PMBASE + 04h	Attribute:	R/W, WO
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Bits 0–7: Core, Bits 8–12: RTC, Bits 13–15: Resume		

Bit	Description
31:14	Reserved.
13	**Sleep Enable (SLP_EN)—**WO. Setting this bit causes the system to sequence into the Sleep state defined by the SLP_TYP field.
12:10	**Sleep Type (SLP_TYP)—**R/W. This 3-bit field defines the type of Sleep the system should enter when the SLP_EN bit is set to 1. These bits are only reset by RTCRST#. **Code** — **Master Interrupt** 000b — ON: Typically maps to S0 state. 001b — Puts CPU in S1 state. 010b — Reserved 011b — Reserved 100b — Reserved 101b — Suspend-To-RAM. Assert SLP_S3#: Typically maps to S3 state. 110b — Suspend-To-Disk. Assert SLP_S3#, and SLP_S4#: Typically maps to S4 state. 111b — Soft Off. Assert SLP_S3#, SLP_S4#, and SLP_S5#: Typically maps to S5 state.
9:3	Reserved.
2	**Global Release (GBL_RLS)—**WO. 0 = This bit always reads as 0. 1 = ACPI software writes a 1 to this bit to raise an event to the BIOS. BIOS software has a corresponding enable and status bits to control its ability to receive ACPI events.
1	**Bus Master Reload (BM_RLD)—**R/W. This bit is treated as a scratchpad bit. his bit is reset to 0 by PLTRST# 0 = Bus master requests will not cause a break from the C3 state. 1 = Enables Bus Master requests (internal or external) to cause a break from the C3 state. If software fails to set this bit before going to C3 state, the PCH will still return to a snoopable state from C3 or C4 states due to bus master activity.
0	**SCI Enable (SCI_EN)—**R/W. Selects the SCI interrupt or the SMI# interrupt for various events including the bits in the PM1_STS register (bit 10, 8, 0), and bits in GPE0_STS. 0 = These events will generate an SMI#. 1 = These events will generate an SCI.

13.8.3.4 PM1_TMR—Power Management 1 Timer Register

I/O Address:	PMBASE + 08h	Attribute:	RO
Default Value:	xx000000h	Size:	32-bit
Lockable:	No	Usage:	ACPI
Power Well:	Core		

Bit	Description
31:24	Reserved
23:0	**Timer Value (TMR_VAL)—**RO. Returns the running count of the PM timer. This counter runs off a 3.579545 MHz clock (14.31818 MHz divided by 4). It is reset to 0 during a PCI reset, and then continues counting as long as the system is in the S0 state. After an S1 state, the counter will not be reset (it will continue counting from the last value in S0 state. Anytime bit 22 of the timer goes HIGH to LOW (bits referenced from 0 to 23), the TMROF_STS bit (PMBASE + 00h, bit 0) is set. The High-to-Low transition will occur every 2.3435 seconds. If the TMROF_EN bit (PMBASE + 02h, bit 0) is set, an SCI interrupt is also generated.

13.8.3.5 GPE0_STS—General Purpose Event 0a Status Register

I/O Address:	PMBASE + 20h	Attribute:	R/WC; RO
Default Value:	0000000000000000h	Size:	64-bit
Lockable:	No	Usage:	ACPI
Power Well:	Bits 0-34, 56-63: Resume, Bit 35: DSW		

This register is symmetrical to the General Purpose Event 0a Enable Register. Unless indicated otherwise below, if the corresponding _EN bit is set, then when the _STS bit get set, the PCH will generate a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the PCH will also generate an SCI if the SCI_EN bit is set, or an SMI# if the SCI_EN bit (PMBASE + 04h, bit 0) is not set.

Bits 15:0 should not be reset by CF9 write. Bits 31:16 are reset by CF9h full resets.

Bit	Description
63:36	Reserved.
35	**GPIO27_STS**—R/WC. 0 = Disable. 1 = Set by hardware and can be reset by writing a one to this bit position or a resume well reset. This bit is set at the level specified in GP27IO_POL. Note that GPIO27 is always monitored as an input for the purpose of setting this bit, regardless of the actual GPIO configuration.
34:32	Reserved
31:16	**GPIOn_STS—**R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = These bits are set any time the corresponding GPIO is set up as an input and the corresponding GPIO signal is high (or low if the corresponding GP_INV bit is set). If the corresponding enable bit is set in the GPE0_EN register, then when the GPIO[n]_STS bit is set: • If the system is in an S1–S5 state, the event will also wake the system. • If the system is in an S0 state (or upon waking back to an S0 state), a SCI will be caused depending on the GPIO_ROUT bits (D31:F0:B8h, bits 31:30) for the corresponding GPI. ***Note:*** Mapping is as follows: bit 31 corresponds to GPIO[15]... and bit 16 corresponds to GPIO[0].
15:14	Reserved

Bit	Description
13	**Power Management Event Bus 0 Status (PME_B0_STS)—**R/WC This bit will be set to 1 by the Intel PCH when any internal device with PCI Power Management capabilities on bus 0 asserts the equivalent of the PME# signal. Additionally, if the PME_B0_EN and SCI_EN bits are set, and the system is in an S0 state, then the setting of the PME_B0_STS bit will generate an SCI (or SMI# if SCI_EN is not set). If the PME_B0_EN bit is set, and the system is in an S1–S4 state (or S5 state due to SLP_TYP and SLP_EN), then the setting of the PME_B0_STS bit will generate a wake event, If the system is in an S5 state due to power button override, then the PME_B0_STS bit will not cause a wake event or SCI. The default for this bit is 0. This bit is cleared by a software write of '1'. The following are internal devices which can set this bit: • Intel HD Audio • Intel ME "maskable" wake events • Integrated LAN • SATA • EHCI
12	Reserved
11	**PME_STS**—R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware when the PME# signal goes active. Additionally, if the PME_EN and SCI_EN bits are set, and the system is in an S0 state, then the setting of the PME_STS bit will generate an SCI (or SMI# if SCI_EN is not set). If the PME_EN bit is set, and the system is in an S1–S4 state (or S5 state due to setting SLP_TYP and SLP_EN), then the setting of the PME_STS bit will generate a wake event. If the system is in an S5 state due to power button override or a power failure, then PME_STS will not cause a wake event or SCI.
10	Reserved
9	**PCI_EXP_STS—**R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware to indicate that: • The PME event message was received on one or more of the PCI Express ports • An Assert PMEGPE message received from the Processor using DMI ***Notes:*** 1. The PCI WAKE# pin has no impact on this bit. 2. If the PCI_EXP_STS bit went active due to an Assert PMEGPE message, then a Deassert PMEGPE message must be received prior to the software write in order for the bit to be cleared. 3. If the bit is not cleared and the corresponding PCI_EXP_EN bit is set, the level-triggered SCI will remain active. 4. A race condition exists where the PCI Express device sends another PME message because the PCI Express device was not serviced within the time when it must resend the message. This may result in a spurious interrupt, and this is comprehended and approved by the PCI Express specification. The window for this race condition is approximately 95–105 milliseconds.
8	**RI_STS**—R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware when the RI# input signal goes active.
7	**SMBus Wake Status (SMB_WAK_STS)—**R/WC. The SMBus controller can independently cause an SMI#, so this bit does not need to do so (unlike the other bits in this register). Software clears this bit by writing a 1 to it. 0 = Wake event Not caused by the PCH's SMBus logic. 1 = Set by hardware to indicate that the wake event was caused by the PCH's SMBus logic.This bit will be set by the WAKE/SMI# command type, even if the system is already awake. The SMI handler should then clear this bit. ***Notes:*** 1. The SMBus controller will independently cause an SMI# so this bit does not need to do so (unlike the other bits in this register). 2. This bit is set by the SMBus slave command 01h (Wake/SMI#) even when the system is in the S0 state. Therefore, to avoid an instant wake on subsequent transitions to sleep states, software must clear this bit after each reception of the Wake/SMI# command or just prior to entering the sleep state. 3. The SMBALERT_STS bit (D31:F3:I/O Offset 00h:Bit 5) should be cleared by software before the SMB_WAK_STS bit is cleared.
6	**TCOSCI_STS**—R/WC. Software clears this bit by writing a 1 to it. 0 = TOC logic or thermal sensor logic did Not cause SCI. 1 = Set by hardware when the TCO logic or thermal sensor logic causes an SCI.

Bit	Description
5:3	Reserved
2	**SWGPE_STS**—R/WC. The SWGPE_CTRL bit (bit 1 of GPE_CTRL reg) acts as a level input to this bit.
1	**HOT_PLUG_STS—**R/WC. 0 = This bit is cleared by writing a 1 to this bit position. 1 = When a PCI Express Hot-Plug event occurs. This will cause an SCI if the HOT_PLUG_EN and SCI_EN bits are set.
0	Reserved

13.8.3.6 GPE0_EN—General Purpose Event 0 Enables Register

I/O Address:	PMBASE + 28h	Attribute:	R/W
Default Value:	0000000000000000h	Size:	64-bit
Lockable:	No	Usage:	ACPI
Power Well:	Bits 0–7, 9, 12, 14–34, 36–63: Resume, Bits 8, 10–11, 13, 35: RTC		

This register is symmetrical to the General Purpose Event 0Status Register.

Bit	Description
63:36	Reserved
35	**GPIO27_EN**—R/W. 0 = Disable. 1 = Enable the setting of the GPIO27_STS bit to generate a wake event/SCI/SMI#. GPIO27 is a valid host wake event from Deep S4/S5. The wake enable configuration persists after a G3 state.
34:32	Reserved.
31:16	**GPIn_EN**—R/W. These bits enable the corresponding GPI[n]_STS bits being set to cause a SCI, and/or wake event. These bits are cleared by RSMRST#. ***Note:*** Mapping is as follows: bit 31 corresponds to GPIO15... and bit 16 corresponds to GPIO0.
15:14	Reserved
13	**PME_B0_EN—**R/W. 0 = Disable 1 = Enables the setting of the PME_B0_STS bit to generate a wake event and/or an SCI or SMI#. PME_B0_STS can be a wake event from the S1–S4 states, or from S5 (if entered using SLP_TYP and SLP_EN) or power failure, but not Power Button Override. This bit defaults to 0. It is only cleared by Software or RTCRST#. It is not cleared by CF9h writes.
12	Reserved
11	**Power Management Event Enable (PME_EN)**—R/W. 0 = Disable. 1 = Enables the setting of the PME_STS to generate a wake event and/or an SCI. PME# can be a wake event from the S1 – S4 state or from S5 (if entered using SLP_EN, but not power button override). In addition to being cleared by RTCRST# assertion, the PCH also clears this bit due to a Power Button Override event, Intel ME Initiated Power Button Override, Intel ME Initiated Host Reset with Power down, SMBus unconditional power down, Processor thermal trip event, or due to an internal thermal sensor catastrophic condition.
10	Reserved
9	**PCI Express Enable (PCI_EXP_EN)**—R/W. 0 = Disable SCI generation upon PCI_EXP_STS bit being set. 1 = Enables PCH to cause an SCI when PCI_EXP_STS bit is set. This is used to allow the PCI Express* ports, including the link to the Processor, to cause an SCI due to wake/PME events.

Bit	Description
8	**RI_EN**—R/W. The value of this bit will be maintained through a G3 state and is not affected by a hard reset caused by a CF9h write. 0 = Disable. 1 = Enables the setting of the RI_STS to generate a wake event. In addition to being cleared by RTCRST# assertion, the PCH also clears this bit due to a Power Button Override event, Intel ME Initiated Power Button Override, Intel ME Initiated Host Reset with Power down, SMBus unconditional power down, Processor thermal trip event, or due to an internal thermal sensor catastrophic condition.
7	Reserved
6	**TCOSCI_EN**—R/W. 0 = Disable. 1 = Enables the setting of the TCOSCI_STS to generate an SCI. In addition to being cleared by RTCRST# assertion, the PCH also clears this bit due to a Power Button Override event, Intel ME Initiated Power Button Override, Intel ME Initiated Host Reset with Power down, SMBus unconditional power down, Processor thermal trip event, or due to an internal thermal sensor catastrophic condition.
5:3	Reserved
2	**Software GPE Enable (SWGPE_EN)—**R/W. This bit allows software to control the assertion of SWGPE_STS bit. This bit This bit, when set to 1, enables the software GPE function. If SWGPE_CTRL is written to a 1, hardware will set SWGPE_STS (acts as a level input) If SWGPE_STS, SWGPE_EN, and SCI_EN are all 1's, an SCI will be generated If SWGPE_STS = 1, SWGPE_EN = 1, SCI_EN = 0, and GBL_SMI_EN = 1 then an SMI# will be generated
1	**HOT_PLUG_EN—**R/W. 0 = Disables SCI generation upon the HOT_PLUG_STS bit being set. 1 = Enables the PCH to cause an SCI when the HOT_PLUG_STS bit is set. This is used to allow the PCI Express ports to cause an SCI due to hot-plug events.
0	Reserved.

13.8.3.7 SMI_EN—SMI Control and Enable Register

I/O Address:	PMBASE + 30h	Attribute:	R/W, R/WO, WO
Default Value:	00000002h	Size:	32 bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Core		

Note: This register is symmetrical to the SMI status register.

Bit	Description
31:28	**Reserved**
27	**GPIO_UNLOCK_SMI_EN**—R/WO. Setting this bit will cause the Intel PCH to generate an SMI# when the GPIO_UNLOCK_SMI_STS bit is set in the SMI_STS register. Once written to '1', this bit can only be cleared by PLTRST#.
26:19	Reserved
18	**INTEL_USB2_EN**—R/W. 0 = Disable 1 = Enables Intel-Specific USB2 SMI logic to cause SMI#.
17	**LEGACY_USB2_EN**—R/W. 0 = Disable 1 = Enables legacy USB2 logic to cause SMI#.
16:15	Reserved
14	**PERIODIC_EN**—R/W. 0 = Disable. 1 = Enables the PCH to generate an SMI# when the PERIODIC_STS bit is set in the SMI_STS register.
13	**TCO_EN**—R/W. 0 = Disables TCO logic generating an SMI#. Note that if the NMI2SMI_EN bit is set, SMIs that are caused by re-routed NMIs will not be gated by the TCO_EN bit. Even if the TCO_EN bit is 0, NMIs will still be routed to cause SMIs. 1 = Enables the TCO logic to generate SMI#. ***Note:*** This bit cannot be written once the TCO_LOCK bit is set.
12	Reserved
11	**MCSMI_ENMicrocontroller SMI Enable (MCSMI_EN)—**R/W. 0 = Disable. 1 = Enables PCH to trap accesses to the microcontroller range (62h or 66h) and generate an SMI#. Note that "trapped' cycles will be claimed by the PCH on PCI, but not forwarded to LPC.
10:8	Reserved
7	**BIOS Release (BIOS_RLS)—**WO. 0 = This bit will always return 0 on reads. Writes of 0 to this bit have no effect. 1 = Enables the generation of an SCI interrupt for ACPI software when a one is written to this bit position by BIOS software. ***Note:*** GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place.
6	**Software SMI# Timer Enable (SWSMI_TMR_EN)**—R/W. 0 = Disable. Clearing the SWSMI_TMR_EN bit before the timer expires will reset the timer and the SMI# will not be generated. 1 = Starts Software SMI# Timer. When the SWSMI timer expires (the timeout period depends upon the SWSMI_RATE_SEL bit setting), SWSMI_TMR_STS is set and an SMI# is generated. SWSMI_TMR_EN stays set until cleared by software.
5	**APMC_EN**—R/W. 0 = Disable. Writes to the APM_CNT register will not cause an SMI#. 1 = Enables writes to the APM_CNT register to cause an SMI#.
4	**SLP_SMI_EN)**—R/W. 0 = Disables the generation of SMI# on SLP_EN. Note that this bit must be 0 before the software attempts to transition the system into a sleep state by writing a 1 to the SLP_EN bit. 1 = A write of 1 to the SLP_EN bit (bit 13 in PM1_CNT register) will generate an SMI#, and the system will not transition to the sleep state based on that write to the SLP_EN bit.

Bit	Description
3	**LEGACY_USB_EN**—R/W. 0 = Disable. 1 = Enables legacy USB circuit to cause SMI#.
2	**BIOS_EN**—R/W. 0 = Disable. 1 = Enables the generation of SMI# when ACPI software writes a 1 to the GBL_RLS bit. Note that if the BIOS_STS bit, which gets set when software writes 1 to GBL_RLS bit, is already a 1 at the time that BIOS_EN becomes 1, an SMI# will be generated when BIOS_EN gets set.
1	**End of SMI (EOS)—**R/W (special). This bit controls the arbitration of the SMI signal to the processor. This bit must be set for the PCH to assert SMI# low to the processor after SMI# has been asserted previously. 0 = Once the PCH asserts SMI# low, the EOS bit is automatically cleared. 1 = When this bit is set to 1, SMI# signal will be deasserted for 4 PCI clocks before its assertion. In the SMI handler, the processor should clear all pending SMIs (by servicing them and then clearing their respective status bits), set the EOS bit, and exit SMM. This will allow the SMI arbiter to re-assert SMI upon detection of an SMI event and the setting of a SMI status bit. ***Note:*** PCH is able to generate 1st SMI after reset even though EOS bit is not set. Subsequent SMI require EOS bit is set.
0	**GBL_SMI_EN—**R/W. 0 = No SMI# will be generated by PCH. This bit is reset by a PCI reset event. 1 = Enables the generation of SMI# in the system upon any enabled SMI event. ***Note:*** When the SMI_LOCK bit is set, this bit cannot be changed.

13.8.3.8 SMI_STS—SMI Status Register

I/O Address:	PMBASE + 34h	Attribute:	RO, R/WC
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Core		

Note: If the corresponding _EN bit is set when the _STS bit is set, the Intel PCH will cause an SMI# (except bits 8–10 and 12, which do not need enable bits since they are logic ORs of other registers that have enable bits). The PCH uses the same GPE0_EN register (I/O address: PMBase+2Ch) to enable/disable both SMI and ACPI SCI general purpose input events. ACPI operating system assumes that it owns the entire GPE0_EN register per the ACPI specification. Problems arise when some of the general-purpose inputs are enabled as SMI by BIOS, and some of the general purpose inputs are enabled for SCI. In this case ACPI operating system turns off the enabled bit for any GPIx input signals that are not indicated as SCI general-purpose events at boot, and exit from sleeping states. BIOS should define a dummy control method which prevents the ACPI operating system from clearing the SMI GPE0_EN bits.

Bit	Description
31:28	Reserved
27	**GPIO_UNLOCK_SMI_STS—**R/WC. This bit will be set if the GPIO registers lockdown logic is requesting an SMI#. Writing a '1' to this bit position clears this bit to '0'.
26	**SPI_STS—**RO. This bit will be set if the SPI logic is generating an SMI#. This bit is read only because the sticky status and enable bits associated with this function are located in the SPI registers.
25:22	Reserved
21	**MONITOR_STS—**RO. This bit will be set if the Trap/SMI logic has caused the SMI. This will occur when the processor or a bus master accesses an assigned register (or a sequence of accesses). See Section 10.1.20 through Section 10.1.34 for details on the specific cause of the SMI.
20	**PCI_EXP_SMI_STS—**RO. PCI Express* SMI event occurred. This could be due to a PCI Express PME event or Hot-Plug event.
19	Reserved

Bit	Description
18	**INTEL_USB2_STS—**RO. This non-sticky read-only bit is a logical OR of each of the SMI status bits in the Intel-Specific USB2 SMI Status Register ANDed with the corresponding enable bits. This bit will not be active if the enable bits are not set. Writes to this bit will have no effect. All integrated EHCIs are represented with this bit.
17	**LEGACY_USB2_STS—**RO. This non-sticky read-only bit is a logical OR of each of the SMI status bits in the USB2 Legacy Support Register ANDed with the corresponding enable bits. This bit will not be active if the enable bits are not set. Writes to this bit will have no effect. All integrated EHCIs are represented with this bit.
16	**SMBus SMI Status (SMBUS_SMI_STS)—**R/WC. Software clears this bit by writing a 1 to it. 0 = This bit is set from the 64 kHz clock domain used by the SMBus. Software must wait at least 15.63 µs after the initial assertion of this bit before clearing it. 1 = Indicates that the SMI# was caused by: 1. The SMBus Slave receiving a message that an SMI# should be caused, or 2. The SMBALERT# signal goes active and the SMB_SMI_EN bit is set and the SMBALERT_DIS bit is cleared, or 3. The SMBus Slave receiving a Host Notify message and the HOST_NOTIFY_INTREN and the SMB_SMI_EN bits are set, or 4. The PCH detecting the SMLINK_SLAVE_SMI command while in the S0 state.
15	**SERIRQ_SMI_STS**—RO. 0 = SMI# was not caused by the SERIRQ decoder. 1 = Indicates that the SMI# was caused by the SERIRQ decoder. ***Note:*** This is not a sticky bit
14	**PERIODIC_STS**—R/WC. Software clears this bit by writing a 1 to it. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set at the rate determined by the PER_SMI_SEL bits. If the PERIODIC_EN bit (PMBASE + 30h, bit 14) is also set, the PCH generates an SMI#.
13	**TCO_STS**—R/WC. Software clears this bit by writing a 1 to it. 0 = SMI# not caused by TCO logic. 1 = Indicates the SMI# was caused by the TCO logic. Note that this is not a wake event.
12	**Device Monitor Status (DEVMON_STS)—**RO. 0 = SMI# not caused by Device Monitor. 1 = Set if bit 0 of the DEVACT_STS register (PMBASE + 44h) is set. The bit is not sticky, so writes to this bit will have no effect.
11	**Microcontroller SMI# Status** (**MCSMI_STS)—**R/WC. Software clears this bit by writing a 1 to it. 0 = Indicates that there has been no access to the power management microcontroller range (62h or 66h). 1 = Set if there has been an access to the power management microcontroller range (62h or 66h) and the Microcontroller Decode Enable #1 bit in the LPC Bridge I/O Enables configuration register is 1 (D31:F0:Offset 82h:bit 11). Note that this implementation assumes that the Microcontroller is on LPC. If this bit is set, and the MCSMI_EN bit is also set, the PCH will generate an SMI#.
10	**GPE0_STS**—RO. This bit is a logical OR of the bits in the ALT_GP_SMI_STS register that are also set up to cause an SMI# (as indicated by the GPI_ROUT registers) and have the corresponding bit set in the ALT_GP_SMI_EN register. Bits that are not routed to cause an SMI# will have no effect on this bit. 0 = SMI# was not generated by a GPI assertion. 1 = SMI# was generated by a GPI assertion.
9	**GPE0_STS**—RO. This bit is a logical OR of the bits 47:32, 14:10, 8, 6:2, and 0 in the GPE0_STS register (PMBASE + 28h) that also have the corresponding bit set in the GPE0_EN register (PMBASE + 2Ch). 0 = SMI# was not generated by a GPE0 event. 1 = SMI# was generated by a GPE0 event.
8	**PM1_STS_REG**—RO. This is an ORs of the bits in the ACPI PM1 Status Register (offset PMBASE+00h) that can cause an SMI#. 0 = SMI# was not generated by a PM1_STS event. 1 = SMI# was generated by a PM1_STS event.
7	Reserved
6	**SWSMI_TMR_STS**—R/WC. Software clears this bit by writing a 1 to it. 0 = Software SMI# Timer has Not expired. 1 = Set by the hardware when the Software SMI# Timer expires.
5	**APM_STS**—R/WC. Software clears this bit by writing a 1 to it. 0 = No SMI# generated by write access to APM Control register with APMCH_EN bit set. 1 = SMI# was generated by a write access to the APM Control register with the APMC_EN bit set.

Bit	Description
4	**SLP SMI Status (SLP_SMI_STS)—**R/WC This bit will be set by the Intel PCH when a write access attempts to set the SLP_EN bit. This bit is cleared by writing a 1 to this bit position
3	**LEGACY_USB_STS**—RO. This bit is a logical OR of each of the SMI status bits in the USB Legacy Keyboard/Mouse Control Registers ANDed with the corresponding enable bits. This bit will not be active if the enable bits are not set. 0 = SMI# was not generated by USB Legacy event. 1 = SMI# was generated by USB Legacy event.
2	**BIOS_STS**—R/WC. 0 = No SMI# generated due to ACPI software requesting attention. 1 = This bit gets set by hardware when a 1 is written by software to the GBL_RLS bit (D31:F0:PMBase + 04h:bit 2). When both the BIOS_EN bit (D31:F0:PMBase + 30h:bit 2) and the BIOS_STS bit are set, an SMI# will be generated. The BIOS_STS bit is cleared when software writes a 1 to its bit position.
1:0	Reserved

13.8.3.9 ALT_GP_SMI_EN—Alternate GPI SMI Enable Register

I/O Address:	PMBASE +38h	Attribute:	R/W
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Resume		

Bit	Description
15:0	**Alternate GPI Intel SMI Enable—**R/W. These bits are used to enable the corresponding GPIO to cause an SMI#. For these bits to have any effect, the following must be true. • The corresponding bit in the ALT_GP_SMI_EN register is set. • The corresponding GPI must be routed in the GPI_ROUT register to cause an Intel SMI. • The corresponding GPIO must be implemented. ***Note:*** Mapping is as follows: bit 15 corresponds to GPIO15... bit 0 corresponds to GPIO0.

13.8.3.10 ALT_GP_SMI_STS—Alternate GPI SMI Status Register

I/O Address:	PMBASE +3Ah	Attribute:	R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Resume		

Bit	Description
15:0	**Alternate GPI SMI Status**—R/WC. These bits report the status of the corresponding GPIOs. 0 = Inactive. Software clears this bit by writing a 1 to it. 1 = Active These bits are sticky. If the following conditions are true, then an SMI# will be generated and the GPE0_STS bit set: • The corresponding bit in the ALT_GPI_SMI_EN register (PMBASE + 38h) is set • The corresponding GPIO must be routed in the GPI_ROUT register to cause an SMI. • The corresponding GPIO must be implemented. All bits are in the resume well. Default for these bits is dependent on the state of the GPIO pins.

13.8.3.11 GPE_CNTL—General Purpose Control Register

I/O Address:	PMBASE +42h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Bits 0-1, 3–7: Resume Bit 2: RTC		

Bit	Description
7:3	Reserved
2	**GPIO27_POL**—R/W. This bit controls the polarity of the GPIO27 pin needed to set the GPIO27_STS bit. 0 = GPIO27 = 0 will set the GPIO27_STS bit. 1 = GPIO27 = 1 will set the GPIO27_STS bit. ***Note:*** This bit is cleared by RTCRST# assertion.
1	**SWGPE_CTRL**—R/W. This bit allows software to control the assertion of SWGPE_STS bit. This bit is used by hardware as the level input signal for the SWGPE_STS bit in the GPE0_STS register. When SWGPE_CTRL is 1, SWGPE_STS will be set to 1, and writes to SWGPE_STS with a value of 1 to clear SWGPE_STS will result in SWGPE_STS being set back to 1 by hardware. When SWGPE_CTRL is 0, writes to SWGPE_STS with a value of 1 will clear SWGPE_STS to 0. In addition to being cleared by RSMRST# assertion, the PCH also clears this bit due to a Power Button Override event, Intel ME Initiated Power Button Override, Intel ME Initiated Host Reset with Power down, SMBus unconditional power down, Processor thermal trip event, or due to an internal thermal sensor catastrophic condition.
0	Reserved.

13.8.3.12 DEVACT_STS—Device Activity Status Register

I/O Address:	PMBASE +44h	Attribute:	R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	Legacy Only
Power Well:	Core		

Each bit indicates if an access has occurred to the corresponding device's trap range, or for bits 6:9 if the corresponding PCI interrupt is active. This register is used in conjunction with the Periodic SMI# timer to detect any system activity for legacy power management. The periodic SMI# timer indicates if it is the right time to read the DEVACT_STS register (PMBASE + 44h).

Note: Software clears bits that are set in this register by writing a 1 to the bit position.

Bit	Description
15:13	Reserved
12	**KBC_ACT_STS**—R/WC. KBC (60/64h). 0 = Indicates that there has been no access to this device's I/O range. 1 = This device's I/O range has been accessed. Clear this bit by writing a 1 to the bit location.
11:10	Reserved
9	**PRIQDH_ACT_STS—**R/WC. PIRQ[D or H]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.
8	**PIRQCG_ACT_STS**—R/WC. PIRQ[C or G]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.
7	**PIRQBF_ACT_STS—**R/WC. PIRQ[B or F]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.
6	**PIRQAE_ACT_STS—**R/WC. PIRQ[A or E]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.
5:0	Reserved

13.8.3.13 PM2_CNT—Power Management 2 Control

I/O Address:	PMBASE + 50h		
		Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Usage:	ACPI
Power Well:	Core		

Bit	Description
7:1	Reserved
0	**Arbiter Disable (ARB_DIS)—**R/W This bit is a scratchpad bit for legacy software compatibility.

13.9 System Management TCO Registers

The TCO logic is accessed using registers mapped to the PCI configuration space (Device 31:Function 0) and the system I/O space. For TCO PCI Configuration registers, see LPC Device 31:Function 0 PCI Configuration registers.

TCO Register I/O Map

The TCO I/O registers reside in a 32-byte range pointed to by a TCOBASE value, which is, PMBASE + 60h in the PCI config space. The following table shows the mapping of the registers within that 32-byte range. Each register is described in the following sections.

Table 13-12. TCO I/O Register Address Map

TCOBASE + Offset	Mnemonic	Register Name	Default	Type
00h–01h	TCO_RLD	TCO Timer Reload and Current Value	0000h	R/W
02h	TCO_DAT_IN	TCO Data In	00h	R/W
03h	TCO_DAT_OUT	TCO Data Out	00h	R/W
04h–05h	TCO1_STS	TCO1 Status	0000h	R/WC, RO
06h–07h	TCO2_STS	TCO2 Status	0000h	R/WC
08h–09h	TCO1_CNT	TCO1 Control	0000h	R/W, R/WLO, R/WC
0Ah–0Bh	TCO2_CNT	TCO2 Control	0008h	R/W
0Ch–0Dh	TCO_MESSAGE1, TCO_MESSAGE2	TCO Message 1 and 2	00h	R/W
0Eh	TCO_WDCNT	Watchdog Control	00h	R/W
0Fh	—	Reserved	—	—
10h	SW_IRQ_GEN	Software IRQ Generation	03h	R/W
11h	—	Reserved	—	—
12h–13h	TCO_TMR	TCO Timer Initial Value	0004h	R/W
14h–1Fh	—	Reserved	—	—

13.9.1 TCO_RLD—TCO Timer Reload and Current Value Register

I/O Address:	TCOBASE +00h	Attribute:	R/W
Default Value:	0000h	Size:	16-bit
Lockable:	No	Power Well:	Core

Bit	Description
15:10	Reserved
9:0	**TCO Timer Value**—R/W. Reading this register will return the current count of the TCO timer. Writing any value to this register will reload the timer to prevent the timeout.

13.9.2 TCO_DAT_IN—TCO Data In Register

I/O Address:	TCOBASE +02h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**TCO Data In Value**—R/W. This data register field is used for passing commands from the operating system to the SMI handler. Writes to this register will cause an SMI and set the SW_TCO_SMI bit in the TCO1_STS register (D31:F0:04h).

13.9.3 TCO_DAT_OUT—TCO Data Out Register

I/O Address:	TCOBASE +03h	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Core

Bit	Description
7:0	**TCO Data Out Value**—R/W. This data register field is used for passing commands from the Intel SMI handler to the operating system. Writes to this register will set the TCO_INT_STS bit in the TCO1_STS register. It will also cause an interrupt, as selected by the TCO_INT_SEL bits.

13.9.4 TCO1_STS—TCO1 Status Register

I/O Address:	TCOBASE +04h	Attribute:	R/WC, RO
Default Value:	2000h ‘Size:	16-bit	
Lockable:	No	Power Well:	Core (Except bit 7, in RTC)

Bit	Description
15:14	Reserved
13	**TCO_SLVSEL (TCO Slave Select)—**RO. This register bit is Read Only by Host and indicates the value of TCO Slave Select Soft Strap. Refer to the PCH Soft Straps section of the SPI Chapter for details.
12	**DMISERR_STS**—R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = PCH received a DMI special cycle message using DMI indicating that it wants to cause an SERR#. The software must read the Processor to determine the reason for the SERR#.
11	Reserved
10	**DMISMI_STS**—R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = PCH received a DMI special cycle message using DMI indicating that it wants to cause an SMI. The software must read the Processor to determine the reason for the SMI.
9	**DMISCI_STS**—R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = PCH received a DMI special cycle message using DMI indicating that it wants to cause an SCI. The software must read the Processor to determine the reason for the SCI.
8	**BIOSWR_STS**—R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = PCH sets this bit and generates and SMI# to indicate an invalid attempt to write to the BIOS. This occurs when either: a) The BIOSWP bit is changed from 0 to 1 and the BLD bit is also set, or b) any write is attempted to the BIOS and the BIOSWP bit is also set. ***Note:*** On write cycles attempted to the 4 MB lower alias to the BIOS space, the BIOSWR_STS will not be set.

Bit	Description
7	**NEWCENTURY_STS**—R/WC. This bit is in the RTC well. 0 = Cleared by writing a 1 to the bit position or by RTCRST# going active. 1 = This bit is set when the Year byte (RTC I/O space, index offset 09h) rolls over from 99 to 00. Setting this bit will cause an SMI# (but not a wake event). ***Note:*** The NEWCENTURY_STS bit is not valid when the RTC battery is first installed (or when RTC power has not been maintained). Software can determine if RTC power has not been maintained by checking the RTC_PWR_STS bit (D31:F0:A4h, bit 2), or by other means (such as a checksum on RTC RAM). If RTC power is determined to have not been maintained, BIOS should set the time to a valid value and then clear the NEWCENTURY_STS bit. The NEWCENTURY_STS bit may take up to 3 RTC clocks for the bit to be cleared after a 1 is written to the bit to clear it. After writing a 1 to this bit, software should not exit the SMI handler until verifying that the bit has actually been cleared. This will ensure that the SMI is not re-entered.
6:4	Reserved
3	**TIMEOUT**—R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Set by PCH to indicate that the SMI was caused by the TCO timer reaching 0.
2	**TCO_INT_STS**—R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = SMI handler caused the interrupt by writing to the TCO_DAT_OUT register (TCOBASE + 03h).
1	**SW_TCO_SMI**—R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Software caused an SMI# by writing to the TCO_DAT_IN register (TCOBASE + 02h).
0	**NMI2SMI_STS**—RO. 0 = Cleared by clearing the associated NMI status bit. 1 = Set by the PCH when an SMI# occurs because an event occurred that would otherwise have caused an NMI (because NMI2SMI_EN is set).

13.9.5 TCO2_STS—TCO2 Status Register

I/O Address:	TCOBASE +06h	Attribute:	R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Power Well:	Resume (Except Bit 0, in RTC)

Bit	Description
15:5	Reserved
4	**SMLink Slave Intel SMI Status (SMLINK_SLV_SMI_STS)**—R/WC. Allow the software to go directly into a pre-determined sleep state. This avoids race conditions. Software clears this bit by writing a 1 to it. 0 = The bit is reset by RSMRST#, but not due to the PCI Reset associated with exit from S3–S5 states. 1 = PCH sets this bit to 1 when it receives the Intel SMI message on the SMLink Slave Interface.
3	Reserved
2	**BOOT_STS**—R/WC. 0 = Cleared by PCH based on RSMRST# or by software writing a 1 to this bit. Note that software should first clear the SECOND_TO_STS bit before writing a 1 to clear the BOOT_STS bit. 1 = Set to 1 when the SECOND_TO_STS bit goes from 0 to 1 and the processor has not fetched the first instruction. If rebooting due to a second TCO timer timeout, and if the BOOT_STS bit is set, the PCH will reboot using the 'safe' multiplier (1111). This allows the system to recover from a processor frequency multiplier that is too high, and allows the BIOS to check the BOOT_STS bit at boot. If the bit is set and the frequency multiplier is 1111, then the BIOS knows that the processor has been programmed to an invalid multiplier.
1	**SECOND_TO_STS**—R/WC. 0 = Software clears this bit by writing a 1 to it, or by a RSMRST#. 1 = PCH sets this bit to 1 to indicate that the TIMEOUT bit had been (or is currently) set and a second timeout occurred before the TCO_RLD register was written. If this bit is set and the NO_REBOOT config bit is 0, then the PCH will reboot the system after the second timeout. The reboot is done by asserting PLTRST#.
0	**Intruder Detect (INTRD_DET)—**R/WC. 0 = Software clears this bit by writing a 1 to it, or by RTCRST# assertion. 1 = Set by PCH to indicate that an intrusion was detected. This bit is set even if the system is in G3 state. ***Notes:*** 1. This bit has a recovery time. After writing a 1 to this bit position (to clear it), the bit may be read back as a 1 for up 65 microseconds before it is read as a 0. Software must be aware of this recovery time when reading this bit after clearing it. 2. If the INTRUDER# signal is active when the software attempts to clear the INTRD_DET bit, the bit will remain as a 1, and the SMI# will be generated again immediately. The SMI handler can clear the INTRD_SEL bits (TCOBASE + 0Ah, bits 2:1), to avoid further SMIs. However, if the INTRUDER# signals goes inactive and then active again, there will not be further SMI's (because the INTRD_SEL bits would select that no SMI# be generated). 3. If the INTRUDER# signal goes inactive some point after the INTRD_DET bit is written as a 1, then the INTRD_DET signal will go to a 0 when INTRUDER# input signal goes inactive. Note that this is slightly different than a classic sticky bit, since most sticky bits would remain active indefinitely when the signal goes active and would immediately go inactive when a 1 is written to the bit.

13.9.6 TCO1_CNT—TCO1 Control Register

I/O Address:	TCOBASE +08h	Attribute:	R/W, R/WLO, R/WC
Default Value:	0000h	Size:	16-bit
Lockable:	No	Power Well:	Core

Bit	Description
15:13	Reserved
12	**TCO_LOCK**—R/WLO. When set to 1, this bit prevents writes from changing the TCO_EN bit (in offset 30h of Power Management I/O space). Once this bit is set to 1, it can not be cleared by software writing a 0 to this bit location. A core-well reset is required to change this bit from 1 to 0. This bit defaults to 0.
11	**TCO Timer Halt (TCO_TMR_HLT)**—R/W. 0 = The TCO Timer is enabled to count. 1 = The TCO Timer will halt. It will not count, and thus cannot reach a value that will cause an SMI# or set the SECOND_TO_STS bit. When set, this bit will prevent rebooting and prevent Alert On LAN event messages from being transmitted on the SMLink (but not Alert On LAN* heartbeat messages).
10	Reserved
9	**NMI2SMI_EN**—R/W. 0 = Normal NMI functionality. 1 = Forces all NMIs to instead cause SMIs. The functionality of this bit is dependent upon the settings of the NMI_EN bit and the GBL_SMI_EN bit as detailed in the following table: NMI_EN / GBL_SMI_EN / Description 0b / 0b / No SMI# at all because GBL_SMI_EN = 0 0b / 1b / SMI# will be caused due to NMI events 1b / 0b / No SMI# at all because GBL_SMI_EN = 0 1b / 1b / No SMI# due to NMI because NMI_EN = 1
8	**NMI_NOW**—R/WC. 0 = Software clears this bit by writing a 1 to it. The NMI handler is expected to clear this bit. Another NMI will not be generated until the bit is cleared. 1 = Writing a 1 to this bit causes an NMI. This allows the BIOS or SMI handler to force an entry to the NMI handler.
7:0	Reserved

13.9.7 TCO2_CNT—TCO2 Control Register

I/O Address:	TCOBASE +0Ah	Attribute:	R/W
Default Value:	0008h	Size:	16-bit
Lockable:	No	Power Well:	Resume

Bit	Description
15:6	Reserved
5:4	**OS_POLICY**—R/W. Operating system-based software writes to these bits to select the policy that the BIOS will use after the platform resets due the WDT. The following convention is recommended for the BIOS and operating system: 00 = Boot normally 01 = Shut down 10 = Do not load operating system. Hold in pre-boot state and use LAN to determine next step 11 = Reserved ***Note:*** These are just scratchpad bits. They should not be reset when the TCO logic resets the platform due to Watchdog Timer.
3	**GPIO11_ALERT_DISABLE**—R/W. At reset (using RSMRST# asserted) this bit is set and GPIO[11] alerts are disabled. 0 = Enable. 1 = Disable GPIO11/SMBALERT# as an alert source for the heartbeats and the SMBus slave.
2:1	**INTRD_SEL**—R/W. This field selects the action to take if the INTRUDER# signal goes active. 00 = No interrupt or SMI# 01 = Interrupt (as selected by TCO_INT_SEL). 10 = Intel SMI 11 = Reserved
0	Reserved

13.9.8 TCO_MESSAGE1 and TCO_MESSAGE2 Registers

I/O Address:	TCOBASE +0Ch (Message 1) TCOBASE +0Dh (Message 2)	Attribute:	R/W
Default Value:	00h	Size:	8-bit
Lockable:	No	Power Well:	Resume

Bit	Description
7:0	**TCO_MESSAGE[*n*]**—R/W. BIOS can write into these registers to indicate its boot progress. The external microcontroller can read these registers to monitor the boot progress.

13.9.9 TCO_WDCNT—TCO Watchdog Control Register

Offset Address:	TCOBASE + 0Eh	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Power Well:	Resume		

Bit	Description
7:0	The BIOS or system management software can write into this register to indicate more details on the boot progress. The register will reset to 00h based on a RSMRST# (but not PLTRST#). The external microcontroller can read this register to monitor boot progress.

13.9.10 SW_IRQ_GEN—Software IRQ Generation Register

Offset Address:	TCOBASE + 10h	Attribute:	R/W
Default Value:	03h	Size:	8 bits
Power Well:	Core		

Bit	Description
7:2	Reserved
1	**IRQ12_CAUSE**—R/W. When software sets this bit to 1, IRQ12 will be asserted. When software sets this bit to 0, IRQ12 will be deasserted.
0	**IRQ1_CAUSE**—R/W. When software sets this bit to 1, IRQ1 will be asserted. When software sets this bit to 0, IRQ1 will be deasserted.

13.9.11 TCO_TMR—TCO Timer Initial Value Register

I/O Address:	TCOBASE +12h	Attribute:	R/W
Default Value:	0004h	Size:	16-bit
Lockable:	No	Power Well:	Core

Bit	Description
15:10	Reserved
9:0	**TCO Timer Initial Value**—R/W. Value that is loaded into the timer each time the TCO_RLD register is written. Values of 0000h or 0001h will be ignored and should not be attempted. The timer is clocked at approximately 0.6 seconds, and thus allows timeouts ranging from 1.2 second to 613.8 seconds. ***Note:*** The timer has an error of ±1 tick (0.6s). The TCO Timer will only count down in the S0 state.

13.10 General Purpose I/O Registers (D31:F0)

The control for the general purpose I/O signals is handled through a 128-byte I/O space. The base offset for this space is selected by the GPIOBASE register.

Table 13-13. Registers to Control GPIO Address Map

GPIOBASE + Offset	Mnemonic	Register Name	Default	Access
00h–03h	GPIO_USE_SEL	GPIO Use Select	BF7FA1FFh	R/W
04h–07h	GP_IO_SEL	GPIO Input/Output Select	E8EB6EFFh	R/W
08h–0Bh	—	Reserved	0h	—
0Ch–0Fh	GP_LVL	GPIO Level for Input or Output	02FE0100h	R/W
10h–13h	—	Reserved	0h	—
14h–17h	—	Reserved	0h	—
18h–1Bh	GPO_BLINK	GPIO Blink Enable	00040000h	R/W
1Ch–1Fh	GP_SER_BLINK	GP Serial Blink	00000000h	R/W
20–23h	GP_SB_CMDSTS	GP Serial Blink Command Status	00080000h	R/W
24–27h	GP_SB_DATA	GP Serial Blink Data	00000000h	R/W
28–29h	GPI_NMI_EN	GPI NMI Enable	0000	R/W
2A–2Bh	GPI_NMI_STS	GPI NMI Status	0000	R/WC
2C–2Fh	GPI_INV	GPIO Signal Invert	00000000h	R/W
30h–33h	GPIO_USE_SEL2	GPIO Use Select 2	020300FFh	R/W
34h–37h	GP_IO_SEL2	GPIO Input/Output Select 2	1F57FFF4h	R/W
38h–3Bh	GP_LVL2	GPIO Level for Input or Output 2	A4AA0007h	R/W
3Ch–3Fh	—	Reserved	0h	—
40h–43h	GPIO_USE_SEL3	GPIO Use Select 3	0000033Fh	R/W
44h–47h	GPIO_SEL3	GPIO Input/Output Select 3	00000FF0h	R/W
48h–4Bh	GP_LVL3	GPIO Level for Input or Output 3	000000C0h	R/W
4Ch–5Fh	—	Reserved	0h	—
60h–63h	GP_RST_SEL1	GPIO Reset Select 1	01000000h	R/W
64h–67h	GP_RST_SEL2	GPIO Reset Select 2	0h	R/W
68h–6Bh	GP_RST_SEL3	GPIO Reset Select 3	0h	R/W
6Ch–7Fh	—	Reserved	0h	—

13.10.1 GPIO_USE_SEL—GPIO Use Select Register

Offset Address:	GPIOBASE + 00h	Attribute:	R/W
Default Value:	BF7FA1FFh	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	**GPIO_USE_SEL[31:0]—**R/W. Each bit in this register enables the corresponding GPIO (if it exists) to be used as a GPIO, rather than for the native function. 0 = Signal used as native function. 1 = Signal used as a GPIO. ***Notes:*** 1. The following bits are always 1 because they are always unMultiplexed: 8, 15, 24, 27, and 28. 2. After a full reset (RSMRST#) all multiplexed signals in the resume and core wells are configured as their default function. After only a PLTRST#, the GPIOs in the core well are configured as their default function. 3. When configured to GPIO mode, the muxing logic will present the inactive state to native logic that uses the pin as an input. 4. By default, all GPIOs are reset to the default state by CF9h reset except GPIO24. Other resume well GPIOs' reset behavior can be programmed using GP_RST_SEL registers. 5. Bit 26 may be overridden by bit 8 in the GEN_PMCON_3 Register. 6. Bit 29 can be configured to GPIO when SLP_LAN#/GPIO29 Select Soft-strap is set to 1 (GPIO usage).

13.10.2 GP_IO_SEL—GPIO Input/Output Select Register

Offset Address:	GPIOBASE +04h	Attribute:	R/W
Default Value:	E8EB6EFFh	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	**GP_IO_SEL[31:0]**—R/W. When configured in native mode (GPIO_USE_SEL[n] is 0), writes to these bits have no effect. The value reported in this register is undefined when programmed as native mode. 0 = Output. The corresponding GPIO signal is an output. 1 = Input. The corresponding GPIO signal is an input.

13.10.3 GP_LVL—GPIO Level for Input or Output Register

Offset Address:	GPIOBASE +0Ch	Attribute:	R/W
Default Value:	02FE0100h	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	**GP_LVL[31:0]**—R/W. These registers are implemented as dual read/write with dedicated storage each. Write value will be stored in the write register, while read is coming from the read register which will always reflect the value of the pin. If GPIO[n] is programmed to be an output (using the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL[n] write register value will drive a high or low value on the output pin. 1 = high, 0 = low. When configured in native mode (GPIO_USE_SEL[n] is 0), writes to these bits are stored but have no effect to the pin value. The value reported in this register is undefined when programmed as native mode. ***Note:*** Bit 29 setting will be ignored if Intel ME FW is configuring SLP_LAN# behavior. When GPIO29/SLP_LAN# Select Soft-strap is set to 1 (GPIO usage), bit 29 can be used as regular GP_LVL bit.

13.10.4 GPO_BLINK—GPO Blink Enable Register

Offset Address:	GPIOBASE +18h	Attribute:	R/W
Default Value:	00040000h	Size:	32-bit
Lockable:	No	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	**GP_BLINK[31:0]**—R/W. The setting of this bit has no effect if the corresponding GPIO signal is programmed as an input. 0 = The corresponding GPIO will function normally. 1 = If the corresponding GPIO is programmed as an output, the output signal will blink at a rate of approximately once per second. The high and low times have approximately 0.5 seconds each. The GP_LVL bit is not altered when this bit is set. The value of the corresponding GP_LVL bit remains unchanged during the blink process, and does not effect the blink in any way. The GP_LVL bit is not altered when programmed to blink. It will remain at its previous value. These bits correspond to GPIO in the Resume well. These bits revert to the default value based on RSMRST# or a write to the CF9h register (but not just on PLTRST#).

Note: GPIO18 will blink by default immediately after reset. This signal could be connected to an LED to indicate a failed boot (by programming BIOS to clear GP_BLINK18 after successful POST).

13.10.5 GP_SER_BLINK—GP Serial Blink

Offset Address:	GPIOBASE +1Ch	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	**GP_SER_BLINK[31:0]—**R/W. The setting of this bit has no effect if the corresponding GPIO is programmed as an input or if the corresponding GPIO has the GPO_BLINK bit set. When set to a '0', the corresponding GPIO will function normally. When using serial blink, this bit should be set to a 1 while the corresponding GP_IO_SEL bit is set to 1. Setting the GP_IO_SEL bit to 0 after the GP_SER_BLINK bit ensures PCH will not drive a 1 on the pin as an output. When this corresponding bit is set to a 1 and the pin is configured to output mode, the serial blink capability is enabled. The PCH will serialize messages through an open-drain buffer configuration. The value of the corresponding GP_LVL bit remains unchanged and does not impact the serial blink capability in any way. Writes to this register have no effect when the corresponding pin is configured in native mode and the read value returned is undefined.

13.10.6 GP_SB_CMDSTS—GP Serial Blink Command Status

Offset Address:	GPIOBASE +20h	Attribute:	R/W, RO
Default Value:	00080000h	Size:	32-bit
Lockable:	No	Power Well:	Core

Bit	Description
31:24	Reserved
23:22	**Data Length Select (DLS)—**R/W. This field determines the number of bytes to serialize on GPIO 00 = Serialize bits 7:0 of GP_SB_DATA (1 byte) 01 = Serialize bits 15:0 of GP_SB_DATA (2 bytes) 10 = Undefined – Software must not write this value 11 = Serialize bits 31:0 of GP_SB_DATA (4 bytes) Software should not modify the value in this register unless the Busy bit is clear. Writes to this register have no effect when the corresponding pin is configured in native mode and the read value returned is undefined.
21:16	**Data Rate Select (DRS)—**R/W. This field selects the number of 120 ns time intervals to count between Manchester data transitions. The default of 8h results in a 960 ns minimum time between transitions. A value of 0h in this register produces undefined behavior. Software should not modify the value in this register unless the Busy bit is clear.
15:9	Reserved
8	**Busy—**RO. This read-only status bit is the hardware indication that a serialization is in progress. Hardware sets this bit to 1 based on the Go bit being set. Hardware clears this bit when the Go bit is cleared by the hardware.
7:1	Reserved
0	**Go—**R/W. This bit is set to 1 by software to start the serialization process. Hardware clears the bit after the serialized data is sent. Writes of 0 to this register have no effect. Software should not write this bit to 1 unless the Busy status bit is cleared.

13.10.7 GP_SB_DATA—GP Serial Blink Data

Offset Address:	GPIOBASE +24h	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Power Well:	Core

Bit	Description
31:0	**GP_SB_DATA[31:0]—**R/W. This register contains the data serialized out. The number of bits shifted out are selected through the DLS field in the GP_SB_CMDSTS register. This register should not be modified by software when the Busy bit is set.

13.10.8 GPI_NMI_EN—GPI NMI Enable

Offset Address:	GPIOBASE +28h	Attribute:	R/W
Default Value:	00000h	Size:	16-bit
Lockable:	No	Power Well:	Core for 0:7 Resume for 8:15

Bit	Description
15:0	**GPI_NMI_EN[15:0]. GPI NMI Enable:** This bit only has effect if the corresponding GPIO is used as an input and its GPI_ROUT register is being programmed to NMI functionality. When set to 1, it used to allow active-low and active-high inputs (depends on inversion bit) to cause NMI.

13.10.9 GPI_NMI_STS—GPI NMI Status

Offset Address:	GPIOBASE +2Ah	Attribute:	R/WC
Default Value:	00000h	Size:	16-bit
Lockable:	Yes	Power Well:	Core for 0:7 Resume for 8:15

Bit	Description
15:0	**GPI_NMI_STS[15:0]. GPI NMI Status:** GPI_NMI_STS[15:0]. GPI NMI Status: This bit is set if the corresponding GPIO is used as an input, and its GPI_ROUT register is being programmed to NMI functionality and also GPI_NMI_EN bit is set when it detects either: 1) active-high edge when its corresponding GPI_INV is configured with value 0. 2) active-low edge when its corresponding GPI_INV is configured with value 1. ***Note:*** Writing a value of 1 will clear the bit, while writing value of 0 have no effect.

13.10.10 GPI_INV—GPIO Signal Invert Register

Offset Address:	GPIOBASE +2Ch	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit
Lockable:	No	Power Well:	Core for 17, 16, 7:0

Bit	Description
31:16	Reserved
31:0	**Input Inversion (GP_INV[n])—**R/W. This bit only has effect if the corresponding GPIO is used as an input and used by the GPE logic, where the polarity matters. When set to '1', then the GPI is inverted as it is sent to the GPE logic that is using it. This bit has no effect on the value that is reported in the GP_LVL register. These bits are used to allow both active-low and active-high inputs to cause SMI# or SCI. Note that in the S0 or S1 state, the input signal must be active for at least two PCI clocks to ensure detection by the PCH. In the S3, S4 or S5 states the input signal must be active for at least 2 RTC clocks to ensure detection. The setting of these bits has no effect if the corresponding GPIO is programmed as an output. These bits correspond to GPI that are in the resume well, and will be reset to their default values by RSMRST# or by a write to the CF9h register. 0 = The corresponding GPI_STS bit is set when the PCH detects the state of the input pin to be high. 1 = The corresponding GPI_STS bit is set when the PCH detects the state of the input pin to be low.

13.10.11 GPIO_USE_SEL2—GPIO Use Select 2 Register

Offset Address:	GPIOBASE +30h	Attribute:	R/W
Default Value:	020300FFh	Size:	32-bit
Dockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	**GPIO_USE_SEL2[63:32]**—R/W. Each bit in this register enables the corresponding GPIO (if it exists) to be used as a GPIO, rather than for the native function. 0 = Signal used as native function. 1 = Signal used as a GPIO. ***Notes:*** 1. The following bit are always 1 because it is always unMultiplexed:0, 3, 25. 2. If GPIO[n] does not exist, then, the (n-32) bit in this register will always read as 0 and writes will have no effect. The following bits are always 0: 29, 30 and 31. 3. After a full reset RSMRST# all multiplexed signals in the resume and core wells are configured as their default function. After only a PLTRST#, the GPIOs in the core well are configured as their default function. 4. When configured to GPIO mode, the muxing logic will present the inactive state to native logic that uses the pin as an input. 5. Bit 26 is ignored, functionality is configured by bits 9:8 of FLMAP0 register. This register corresponds to GPIO[63:32]. Bit 0 corresponds to GPIO32 and bit 28 corresponds to GPIO60.

13.10.12 GP_IO_SEL2—GPIO Input/Output Select 2 Register

Offset Address:	GPIOBASE +34h	Attribute:	R/W
Default Value:	1F57FFF4h		
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	**GP_IO_SEL2[63:32]**—R/W. 0 = GPIO signal is programmed as an output. 1 = Corresponding GPIO signal (if enabled in the GPIO_USE_SEL2 register) is programmed as an input. This register corresponds to GPIO[63:32]. Bit 0 corresponds to GPIO32.

13.10.13 GP_LVL2—GPIO Level for Input or Output 2 Register

Offset Address:	GPIOBASE +38h	Attribute:	R/W
Default Value:	A4AA0007h	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	**GP_LVL[63:32]**—R/W. These registers are implemented as dual read/write with dedicated storage each. Write value will be stored in the write register, while read is coming from the read register which will always reflect the value of the pin. If GPIO[n] is programmed to be an output (using the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL[n] write register value will drive a high or low value on the output pin. 1 = high, 0 = low. When configured in native mode (GPIO_USE_SEL[n] is 0), writes to these bits are stored but have no effect to the pin value. The value reported in this register is undefined when programmed as native mode. ***Note:*** This register corresponds to GPIO[63:32]. Bit 0 corresponds to GPIO32.

13.10.14 GPIO_USE_SEL3—GPIO Use Select 3 Register

Offset Address:	GPIOBASE +40h	Attribute:	R/W
Default Value:	0000033Fh	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:12	Always 0. No corresponding GPIO.
11:0	**GPIO_USE_SEL3[75:64]**—R/W. Each bit in this register enables the corresponding GPIO (if it exists) to be used as a GPIO, rather than for the native function. 0 = Signal used as native function. 1 = Signal used as a GPIO. ***Notes:*** 1. The following bit is always 1 because it is always unMultiplexed: 8 2. If GPIO[n] does not exist, then, the (n-32) bit in this register will always read as 0 and writes will have no effect. 3. After a full reset RSMRST# all multiplexed signals in the resume and core wells are configured as their default function. After only a PLTRST#, the GPIOs in the core well are configured as their default function. 4. When configured to GPIO mode, the muxing logic will present the inactive state to native logic that uses the pin as an input. This register corresponds to GPIO[95:64]. Bit 0 corresponds to GPIO64 and bit 11 corresponds to GPIO75.

13.10.15 GP_IO_SEL3—GPIO Input/Output Select 3 Register

Offset Address:	GPIOBASE +44h	Attribute:	R/W
Default Value:	00000^{FF0}	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:12	Always 0. No corresponding GPIO.
11:0	**GPIO_IO_SEL3[75:64]**—R/W. 0 = GPIO signal is programmed as an output. 1 = Corresponding GPIO signal (if enabled in the GPIO_USE_SEL3 register) is programmed as an input. This register corresponds to GPIO[95:64]. Bit 0 corresponds to GPIO64.

13.10.16 GP_LVL3—GPIO Level for Input or Output 3 Register

Offset Address:	GPIOBASE +48h	Attribute:	R/W
Default Value:	000000C0h	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
11:0	**GP_LVL[75:64]**—R/W. These registers are implemented as dual read/write with dedicated storage each. Write value will be stored in the write register, while read is coming from the read register which will always reflect the value of the pin. If GPIO[n] is programmed to be an output (using the corresponding bit in the GP_IO_SEL register), then the corresponding GP_LVL[n] write register value will drive a high or low value on the output pin. 1 = high 0 = low. When configured in native mode (GPIO_USE_SEL[n] is 0), writes to these bits are stored but have no effect to the pin value. The value reported in this register is undefined when programmed as native mode. This register corresponds to GPIO[95:64]. Bit 0 corresponds to GPIO64.

13.10.17 GP_RST_SEL1—GPIO Reset Select

Offset Address:	GPIOBASE +60h	Attribute:	R/W
Default Value:	01000000h	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:24	**GP_RST_SEL[31:24]—**R/W. 0 = Corresponding GPIO registers will be reset by PCH_PWROK deassertion, CF9h reset (06h or 0Eh), or SYS_RST# assertion. 1 = Corresponding GPIO registers will be reset by RSMRST# assertion only. ***Note:*** GPIO[24] register bits are not cleared by CF9h reset by default.
23:16	Reserved
15:8	**GP_RST_SEL[15:8]**—R/W. 0 = Corresponding GPIO registers will be reset by PCH_PWROK deassertion, CF9h reset (06h or 0Eh), or SYS_RST# assertion. 1 = Corresponding GPIO registers will be reset by RSMRST# assertion only.
7:0	Reserved

13.10.18 GP_RST_SEL2—GPIO Reset Select

Offset Address:	GPIOBASE +64h	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:24	**GP_RST_SEL[63:56]**—R/W. 0 = Corresponding GPIO registers will be reset by PCH_PWROK deassertion, CF9h reset (06h or 0Eh), or SYS_RST# assertion. 1 = Corresponding GPIO registers will be reset by RSMRST# assertion only.
23:16	Reserved
15:8	**GP_RST_SEL[47:40]**—R/W. 0 = Corresponding GPIO registers will be reset by PCH_PWROK deassertion, CF9h reset (06h or 0Eh), or SYS_RST# assertion. 1 = Corresponding GPIO registers will be reset by RSMRST# assertion only.
7:0	Reserved

13.10.19 GP_RST_SEL3—GPIO Reset Select

Offset Address:	GPIOBASE +68h	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:12	Reserved
11:8	**GP_RST_SEL[75:72]—**R/W. 0 = Corresponding GPIO registers will be reset by PCH_PWROK deassertion, CF9h reset (06h or 0Eh), or SYS_RST# assertion. 1 = Corresponding GPIO registers will be reset by RSMRST# assertion only.
7:0	Reserved

13.11 GPIO Serial Expander MMIO Registers

The control for the GSX signals is handled through MMIO space. The base offset for this space is selected by the GSXBAR register in Section 10.1.48.

Table 13-14. Registers to Control GSX Address Map

GSXBAR + offset	Mnemonic	Register Name	Default	Access
000h–00Fh	—	Reserved	0h	—
010h–013h	GSX_CxCAP	GSX Capabilities 1	00000000h	R/W, RO
014h–017h	GSX_CxCAP2	GSX Capabilities 2	00031250h	—
018h–01Fh	—	Reserved	0h	—
020h–023h	GSX_CxGPILVL	GSX Input Level DWord 0	00000000h	RO
024h–027h	GSX_CxGPILVL_DW1	GSX Input Level DWord 1	00000000h	RO
028h–02Fh	—	Reserved	0h	—
030h–033h	GSX_CxGPOLVL	GSX Output Level DWord 0	00000000h	R/W
034h–037h	GSX_CxGPOLVL_DW1	GSX Output Level DWord 1	00000000h	R/W
038h–03Fh	—	Reserved	0h	—
0040h–0043h	GSX_CxCMD	GSX Command Register	00000000h	R/W, RO
044h–3FFh	—	Reserved	0h	—

13.11.1 GSX_CxCAP—GSX Capabilities Register 1

Offset Address: GSXBAR +10h Attribute: R/W, RO
Default Value: 00000000h Size: 32-bit

Bit	Description
31:10	Reserved
9:5	**Number of Output Expanders (NOUT)** - R/W. BIOS programs this field to indicate number of output expander components which corresponds to multiple of CxGPO in byte granularity. 00000b = No output expanders 00001b = 1 output expander 00010b = 2 output expanders ... ***Note:*** Total number of NOUT + NIN ≤ 8
4:0	**Number of Input Expanders (NIN)** - R/W. BIOS programs this field to indicate number of output expander components which corresponds to multiple of CxGPI in byte granularity. 00000b = No input expanders 00001b = 1 input expander 00010b = 2 input expanders ... ***Note:*** Total number of NOUT + NIN ≤ 8

13.11.2 GSX_CxCAP2—GSX Capabilities Register 2

Offset Address: GSXBAR +14h Attribute: R/W, RO
Default Value: 000015625h Size: 32-bit

Bit	Description
31:26	Reserved
25:12	**SCLK Rate (SCLKR)—**RO. SCLKR and SCLKRD are BCD (binary-coded decimal) encoded. The SCLKR represent MHz rate as a whole number, and SCLKR_D represent the decimal number. ***Note:*** The GSXSCLK is running at 15.625 MHZ.
11:0	**SCLK Rate Decimal (SCLKR_D)—**RO. Refer to SCLKR. ***Note:*** The GSXSCLK is running at 15.625 MHZ.

13.11.3 GSX_CxGPILVL—GSX Input Level Register DW0

Offset Address: GSXBAR +20h Attribute: RO
Default Value: 00000000h Size: 32-bit

Bit	Description
31:0	**GPI Level (GPILVL)—**RO. BIOS or software read returns the value of the CxGPI received over the GSX channel. GPILVL[y] corresponds to CxGPI[y] where y falls within [31:0] range. CGPILVL[0] contains the first bit being serially shifted in during an atomic input serialization process. Hardware serialization process shifts in each bit of CxGPI value in ascending order from [bit 0] to [((NIN*8)-1)'s MSB bit].

13.11.4 GSX_CxGPILVL_DW1—GSX Input Level Register DW1

Offset Address: GSXBAR +24h Attribute: RO
Default Value: 00000000h Size: 32-bit

Bit	Description
31:0	**GPI Level (GPILVL_DW1)—**RO. BIOS or software read returns the value of the CxGPI received over the GSX channel. GPILVL[y] corresponds to CxGPI[y] where y falls within [63:32] range.

13.11.5 GSX_CxGPOLVL—GSX Output Level Register DW0

Offset Address: GSXBAR +30h Attribute: R/W
Default Value: 00000000h Size: 32-bit

Bit	Description
31:0	**GPO Level (GPOLVL)—**R/W. BIOS or software writes to this field to program the value of each output bit that will be sent in the serialization process. GPOLVL[y] corresponds to CxGPO[y] where y within CxGPO[31:0] range. GPOLVL[0] is the last bit in this register to be shifted out serially. Hardware serialization process shifts out each bit of CxGPOLVL_DW1 & CxGPOLVL in descending order from [((NOUT*8)-1)'s MSB bit] to [bit 0].

13.11.6 GSX_CxGPOLVL_DW1—GSX Output Level Register DW1

Offset Address:	GSXBAR +34h	Attribute:	R/W
Default Value:	00000000h	Size:	32-bit

Bit	Description
31:0	**GPO Level (GPOLVL_DW1)—**R/W. BIOS or software writes to this field to program the value of each output bit that will be sent in the serialization process. GPOLVL[y] corresponds to CxGPO[y] where y within CxGPO[63:32] range.

13.11.7 GSX_CxCMD—GSX Command Register

Offset Address:	GSXBAR +40h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32-bit

Bit	Description
31:4	Reserved
3	**Input and Output Expander Reset Sequence (IOERST)—**R/W. Software writes '1' to this bit to cause a reset sequence that brings both input and output expander into a default state. Serialization process will be able to begin at default bit position again. ***Note:*** This bit is cleared once the above reset sequence is completed.
2	**Serialization Running (RUN)—**RO. 0 = Serialization is complete. 1 = Serialization is in progress. ***Note:*** When software clears the ST bit, software shall poll on RUN bit to be '0' before software can write '1' to ST bit again.
1	**Busy (BSY)—**RO. Software reads this field to determine if the serialization of most recently updated GPOLVL_DW1 and/or GPOLVL content has been completely serialized out on the GSX. Hardware will automatically clear the bit to'0' after all of the newly written value of GPOLVL_DW1 and/or GPOLVL bits have been serialized out at least once.
0	**Start (ST)—**R/W. 0 = Stop serialization process. 1 = Start serialization process. ***Notes:*** 1. Software can only write this bit to '1' when Busy (BSY) status bit is cleared and CxCAP register is programmed. 2. If software write this bit to '0', serialization process will stop at an atomic boundary. 3. Clearing Start (ST) bit does not cause GSXSRESET# to be asserted.

§

14 SATA Controller Registers (D31:F2)

14.1 PCI Configuration Registers (SATA–D31:F2)

Note: Address locations that are not shown should be treated as Reserved.

All of the SATA registers are in the core well. None of the registers can be locked.

Table 14-1. SATA Controller PCI Register Address Map (SATA–D31:F2) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	02B0h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	See register description	See register description
0Ah	SCC	Sub Class Code	See register description	See register description
0Bh	BCC	Base Class Code	01h	RO
0Dh	PMLT	Primary Master Latency Timer	00h	RO
0Eh	HTYPE	Header Type	00h	RO
10h–13h	PCMD_BAR	Primary Command Block Base Address	00000001h	R/W, RO
14h–17h	PCNL_BAR	Primary Control Block Base Address	00000001h	R/W, RO
18h–1Bh	SCMD_BAR	Secondary Command Block Base Address	00000001h	R/W, RO
1Ch–1Fh	SCNL_BAR	Secondary Control Block Base Address	00000001h	R/W, RO
20h–23h	BAR	Legacy Bus Master Base Address	00000001h	R/W, RO
24h–27h	ABAR / SIDPBA	AHCI Base Address / SATA Index Data Pair Base Address	See register description	See register description
2Ch–2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2Eh–2Fh	SID	Subsystem Identification	0000h	R/WO
34h	CAP	Capabilities Pointer	80h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	See register description	RO
40h–41h	IDE_TIM	Primary IDE Timing Register	0000h	R/W
44h	SIDETIM	Slave IDE Timing	00h	R/W
48h	SDMA_CNT	Synchronous DMA Control	00h	R/W
4Ah–4Bh	SDMA_TIM	Synchronous DMA Timing	0000h	R/W
54h–47h	IDE_CONFIG	IDE I/O Configuration	00000000h	R/W
70h–71h	PID	PCI Power Management Capability ID	See register description	RO

Table 14-1. SATA Controller PCI Register Address Map (SATA–D31:F2) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Type
72h–73h	PC	PCI Power Management Capabilities	See register description	RO
74h–75h	PMCS	PCI Power Management Control and Status	See register description	R/W, RO, R/WC
80h–81h	MSICI	Message Signaled Interrupt Capability ID	7005h	RO
82h–83h	MSIMC	Message Signaled Interrupt Message Control	0000h	RO, R/W
84h–87h	MSIMA	Message Signaled Interrupt Message Address	00000000h	RO, R/W
88h–89h	MSIMD	Message Signaled Interrupt Message Data	0000h	R/W
90h	MAP	Address Map	0000h	R/W
92h–93h	PCS	Port Control and Status	0000h	R/W, RO
94h–97h	SCLKCG	SATA Clock Gating Control	00000000h	R/W
9Ch–9Fh	SCC	SATA General Configuration	00000000h	R/W, R/WO
A8h–ABh	SCAP0	SATA Capability Register 0	0010B012h	RO, R/WO
ACh–AFh	SCAP1	SATA Capability Register 1	00000048h	RO
B0h–B1h	FLRCID	FLR Capability ID	0009h	RO
B2h–B3h	FLRCLV	FLR Capability Length and Version	See register description	R/WO, RO
B4h–B5h	FLRC	FLR Control	0000h	RO, R/W
C0h	ATC	APM Trapping Control	00h	R/W
C4h	ATS	ATM Trapping Status	00h	R/WC
D0h–D3h	SP	Scratch Pad	00000000h	R/W
E0h–E3h	BFCS	BIST FIS Control/Status	00000000h	R/W, R/WC
E4h–E7h	BFTD1	BIST FIS Transmit Data, DW1	00000000h	R/W
E8h–EBh	BFTD2	BIST FIS Transmit Data, DW2	00000000h	R/W

Note: The PCH SATA controller is not arbitrated as a PCI device, therefore it does not need a master latency timer.

14.1.1 VID—Vendor Identification Register (SATA—D31:F2)

Offset Address: 00h–01h
Default Value: 8086h
Lockable: No
Attribute: RO
Size: 16 bit
Power Well: Core

Bit	Description
15:0	**Vendor ID**—RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

14.1.2 DID—Device Identification Register (SATA—D31:F2)

Offset Address:	02h–03h	Attribute:	RO
Default Value:	See bit description	Size:	16 bit
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Device ID**—RO. This is a 16-bit value assigned to the PCH SATA controller. ***Note:*** The value of this field will change dependent upon the value of the MAP Register. See Section 14.1.34

14.1.3 PCICMD—PCI Command Register (SATA–D31:F2)

Address Offset:	04h–05h	Attribute:	RO, R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable**—R/W. This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt and MSI is not enabled. 1 = Internal INTx# messages will not be generated.
9	Fast Back to Back Enable (FBE)—RO. Reserved as 0.
8	SERR# Enable (SERR_EN)—RO. Reserved as 0.
7	Wait Cycle Control (WCC)—RO. Reserved as 0.
6	**Parity Error Response (PER)—**R/W. 0 = Disabled. SATA controller will not generate PERR# when a data parity error is detected. 1 = Enabled. SATA controller will generate PERR# when a data parity error is detected.
5	VGA Palette Snoop (VPS)—RO. Reserved as 0.
4	Postable Memory Write Enable (PMWE)—RO. Reserved as 0.
3	Special Cycle Enable (SCE)—RO. Reserved as 0.
2	**Bus Master Enable (BME)—**R/W. This bit controls the SATA controller's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands.
1	**Memory Space Enable (MSE)—**R/W / RO. Controls access to the SATA controller's target memory space (for AHCI). This bit is RO '0' when not in AHCI/RAID modes.
0	**I/O Space Enable (IOSE)—**R/W. This bit controls access to the I/O space registers. 0 = Disables access to the Legacy or Native IDE ports (both Primary and Secondary) as well as the Bus Master I/O registers. 1 = Enable. Note that the Base Address register for the Bus Master registers should be programmed before this bit is set.

14.1.4 PCISTS—PCI Status Register (SATA–D31:F2)

Address Offset:	06h–07h	Attribute:	R/WC, RO
Default Value:	02B0h	Size:	16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)**—R/WC. 0 = No parity error detected by SATA controller. 1 = SATA controller detects a parity error on its interface.
14	Signaled System Error (SSE)—RO. Reserved as 0.
13	**Received Master Abort (RMA)—**R/WC. 0 = Master abort Not generated. 1 = SATA controller, as a master, generated a master abort.
12	Reserved—R/WC.
11	Signaled Target Abort (STA)—RO. Reserved as 0.
10:9	**DEVSEL# Timing Status (DEV_STS)**—RO. 01 = Hardwired; Controls the device select time for the SATA controller's PCI interface.
8	**Data Parity Error Detected (DPED)—**R/WC. For PCH, this bit can only be set on read completions received from the bus when there is a parity error. 0 = No data parity error received. 1 = SATA controller, as a master, either detects a parity error or sees the parity error line asserted, and the parity error response bit (bit 6 of the command register) is set.
7	Fast Back to Back Capable (FB2BC)—RO. Reserved as 1.
6	Reserved.
5	66 MHz Capable (66MHZ_CAP)—RO. Reserved as 1.
4	**Capabilities List (CAP_LIST)—**RO. This bit indicates the presence of a capabilities list. The minimum requirement for the capabilities list must be PCI power management for the SATA controller.
3	**Interrupt Status (INTS)**—RO. Reflects the state of INTx# messages, IRQ14 or IRQ15. 0 = Interrupt is cleared (independent of the state of Interrupt Disable bit in the command register [offset 04h]). 1 = Interrupt is to be asserted
2:0	Reserved

14.1.5 RID—Revision Identification Register (SATA—D31:F2)

Offset Address:	08h	Attribute:	RO
Default Value:	See bit description	Size:	8 bits

Bit	Description
7:0	**Revision ID**—RO. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Revision ID Register.

14.1.6 PI—Programming Interface Register (SATA–D31:F2)

14.1.6.1 When Sub Class Code Register (D31:F2:Offset 0Ah) = 01h

Address Offset: 09h
Attribute: R/W, RO
Default Value: 8Ah
Size: 8 bits

Bit	Description
7	This read-only bit is a 1 to indicate that the PCH supports bus master operation
6:4	Reserved. Will always return 0.
3	Secondary Mode Native Capable (SNC)—RO. Hardwired to '1' to indicate secondary controller supports both legacy and native modes.
2	**Secondary Mode Native Enable (SNE)**—R/W. Determines the mode that the secondary channel is operating in. 0 = Secondary controller operating in legacy (compatibility) mode 1 = Secondary controller operating in native PCI mode. When MAP.MV (D31:F2:Offset 90:bits 1:0) is any value other than 00b, this bit is read-only (RO). When MAP.MV is 00b, this bit is read/write (R/W). If this bit is set by software, then the PNE bit (bit 0 of this register) must also be set by software. While in theory these bits can be programmed separately, such a configuration is not supported by hardware.
1	Primary Mode Native Capable (PNC)—RO. Hardwired to '1' to indicate primary controller supports both legacy and native modes.
0	**Primary Mode Native Enable (PNE)**—R/W. Determines the mode that the primary channel is operating in. 0 = Primary controller operating in legacy (compatibility) mode. 1 = Primary controller operating in native PCI mode. If this bit is set by software, then the SNE bit (bit 2 of this register) must also be set by software simultaneously.

14.1.6.2 When Sub Class Code Register (D31:F2:Offset 0Ah) = 04h

Address Offset: 09h
Attribute: RO
Default Value: 00h
Size: 8 bits

Bit	Description
7:0	**Interface (IF)**—RO. When configured as RAID, this register becomes read only 0.

14.1.6.3 When Sub Class Code Register (D31:F2:Offset 0Ah) = 06h

Address Offset: 09h
Attribute: RO
Default Value: 01h
Size: 8 bits

Bit	Description
7:0	**Interface (IF)**—RO. Indicates that the SATA Controller is an AHCI HBA that has a major revision of 1.

14.1.7 SCC—Sub Class Code Register (SATA–D31:F2)

Address Offset:	0Ah	Attribute:	RO
Default Value:	See bit description	Size:	8 bits

Bit	Description
7:0	**Sub Class Code (SCC)** This field specifies the sub-class code of the controller, per the table below: MAP.SMS (D31:F2:Offset 90h:bit 7:6) — SCC Default Register Value 00b — 01h (IDE Controller) 01b — 06h (AHCI Controller) 10b — 04h (RAID Controller)

14.1.8 BCC—Base Class Code Register (SATA–D31:F2)

Address Offset:	0Bh	Attribute:	RO
Default Value:	01h	Size:	8 bits

Bit	Description
7:0	**Base Class Code (BCC)**—RO. 01h = Mass storage device

14.1.9 PMLT—Primary Master Latency Timer Register (SATA–D31:F2)

Address Offset:	0Dh	Attribute:	RO
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	**Master Latency Timer Count (MLTC)**—RO. 00h = Hardwired. The SATA controller is implemented internally, and is not arbitrated as a PCI device, so it does not need a Master Latency Timer.

14.1.10 HTYPE—Header Type (SATA–D31:F2)

Address Offset:	0Eh	Attribute:	RO
Default Value:	00h	Size:	8 bits

Bit	Description
7	**Multi-function Device (MFD)**—RO. Indicates this SATA controller is not part of a multifunction device.
6:0	**Header Layout (HL)**—RO. Indicates that the SATA controller uses a target device layout.

14.1.11 PCMD_BAR—Primary Command Block Base Address Register (SATA–D31:F2)

Address Offset:	10h–13h	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

Bit	Description
31:16	Reserved
15:3	**Base Address—**R/W. This field provides the base address of the I/O space (8 consecutive I/O locations).
2:1	Reserved
0	**Resource Type Indicator (RTE)—**RO. Hardwired to 1 to indicate a request for I/O space.

Note: This 8-byte I/O space is used in native mode for the Primary Controller's Command Block.

14.1.12 PCNL_BAR—Primary Control Block Base Address Register (SATA–D31:F2)

Address Offset:	14h–17h	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

Bit	Description
31:16	Reserved
15:2	**Base Address—**R/W. This field provides the base address of the I/O space (4 consecutive I/O locations).
1	Reserved
0	**Resource Type Indicator (RTE)**—RO. Hardwired to 1 to indicate a request for I/O space.

Note: This 4-byte I/O space is used in native mode for the Primary Controller's Control Block.

14.1.13 SCMD_BAR—Secondary Command Block Base Address Register (IDE D31:F2)

Address Offset:	18h–1Bh	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

Bit	Description
31:16	Reserved
15:3	**Base Address—**R/W. This field provides the base address of the I/O space (8 consecutive I/O locations).
2:1	Reserved
0	**Resource Type Indicator (RTE)**—RO. Hardwired to 1 to indicate a request for I/O space.

Note: This 8-byte I/O space is used in native mode for the Secondary Controller's Command Block.

14.1.14 SCNL_BAR—Secondary Control Block Base Address Register (IDE D31:F2)

Address Offset:	1Ch–1Fh	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

Bit	Description
31:16	Reserved
15:2	**Base Address—**R/W. This field provides the base address of the I/O space (4 consecutive I/O locations).
1	Reserved
0	**Resource Type Indicator (RTE)—**RO. Hardwired to 1 to indicate a request for I/O space.

Note: This 4-byte I/O space is used in native mode for the Secondary Controller's Control Block.

14.1.15 BAR—Legacy Bus Master Base Address Register (SATA–D31:F2)

Address Offset:	20h–23h	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

The Bus Master IDE interface function uses Base Address register 5 to request a 16-byte I/O space to provide a software interface to the Bus Master functions. Only 12 bytes are actually used (6 bytes for primary, 6 bytes for secondary). Only bits [15:4] are used to decode the address.

Bit	Description
31:16	Reserved
15:5	**Base Address—**R/W. This field provides the base address of the I/O space (16 consecutive I/O locations).
4	**Base**—R/W / RO. When SCC is 01h, this bit will be R/W resulting in requesting 16B of I/O space. When SCC is not 01h, this bit will be Read Only 0, resulting in requesting 32B of I/O space.
3:1	Reserved
0	**Resource Type Indicator (RTE)—**RO. Hardwired to 1 to indicate a request for I/O space.

14.1.16 ABAR/SIDPBA1—AHCI Base Address Register/Serial ATA Index Data Pair Base Address (SATA–D31:F2)

When the programming interface is not IDE (that is, SCC is not 01h), this register is named ABAR. When the programming interface is IDE, this register becomes SIDPBA.

Note that hardware does not clear those BA bits when switching from IDE component to non-IDE component or vice versa. BIOS is responsible for clearing those bits to 0 since the number of writable bits changes after component switching (as indicated by a change in SCC). In the case, this register will then have to be re-programmed to a proper value.

14.1.16.1 When SCC is not 01h

When the programming interface is not IDE, the register represents a memory BAR allocating space for the AHCI memory registers defined in Section 14.4.

Address Offset:	24–27h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:11	**Base Address (BA)—**R/W. Base address of register memory space (aligned to 2 KB)
10:4	Reserved
3	**Prefetchable (PF)**—RO. Indicates that this range is not pre-fetchable
2:1	**Type (TP)—**RO. Indicates that this range can be mapped anywhere in 32-bit address space.
0	**Resource Type Indicator (RTE)—**RO. Hardwired to 0 to indicate a request for register memory space.

Note:
1. The ABAR register must be set to a value of 0001_0000h or greater.

14.1.16.2 When SCC is 01h

When the programming interface is IDE, the register becomes an I/O BAR allocating 16 bytes of I/O space for the I/O-mapped registers defined in Section 14.2. Note that although 16 bytes of locations are allocated, only 8 bytes are used to as SINDX and SDATA registers; with the remaining 8 bytes preserved for future enhancement.

Address Offset:	24h–27h	Attribute:	R/WO
Default Value:	00000001h	Size:	32 bits

Bit	Description
31:16	Reserved
15:4	**Base Address (BA)—**R/W. Base address of the I/O space.
3:1	Reserved
0	**Resource Type Indicator (RTE)—**RO. Indicates a request for I/O space.

14.1.17 SVID—Subsystem Vendor Identification Register (SATA–D31:F2)

Address Offset:	2Ch–2Dh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core
Function Level Reset: No			

Bit	Description
15:0	**Subsystem Vendor ID (SVID)—**R/WO. Value is written by BIOS. No hardware action taken on this value.

14.1.18 SID—Subsystem Identification Register (SATA–D31:F2)

Address Offset:	2Eh–2Fh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core
Function Level Reset: No			

Bit	Description
15:0	**Subsystem ID (SID)**—R/WO. Value is written by BIOS. No hardware action taken on this value.

14.1.19 CAP—Capabilities Pointer Register (SATA–D31:F2)

Address Offset:	34h	Attribute:	RO
Default Value:	80h	Size:	8 bits

Bit	Description
7:0	**Capabilities Pointer (CAP_PTR)**—RO. Indicates that the first capability pointer offset is 80h. This value changes to 70h if the Sub Class Code (SCC) (Dev 31:F2:0Ah) is configure as IDE mode (value of 01).

14.1.20 INT_LN—Interrupt Line Register (SATA–D31:F2)

Address Offset:	3Ch	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Function Level Reset:No			

Bit	Description
7:0	**Interrupt Line—**R/W. This field is used to communicate to software the interrupt line that the interrupt pin is connected to. Interrupt Line register is not reset by FLR

14.1.21 INT_PN—Interrupt Pin Register (SATA–D31:F2)

Address Offset:	3Dh	Attribute:	RO
Default Value:	See Register Description	Size:	8 bits

Bit	Description
7:0	**Interrupt Pin—**RO. This reflects the value of D31IP.SIP (Chipset Config Registers:Offset 3100h:bits 11:8).

14.1.22 IDE_TIM—IDE Timing Register (SATA–D31:F2)

Address Offset:	Primary: 40h–41h Secondary: 42h–43h	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

Bits 14:12 and 9:0 of this register are R/W to maintain software compatibility. These bits have no effect on hardware.

Bit	Description
15	**IDE Decode Enable (IDE)—**R/W. Individually enable/disable the Primary or Secondary decode. 0 = Disable. 1 = Enables the PCH to decode the associated Command Blocks (1F0–1F7h for primary, 170–177h for secondary, or their native mode BAR equivalents) and Control Block (3F6h for primary, 376h for secondary, or their native mode BAR equivalents). This bit effects the IDE decode ranges for both legacy and native-Mode decoding.
14:12	**IDE_TIM Field 2**—R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
11:10	Reserved
9:0	**IDE_TIM Field 1**—R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.

14.1.23 SIDETIM—Slave IDE Timing Register (SATA–D31:F2)

Address Offset:	44h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Note: This register is R/W to maintain software compatibility. These bits have no effect on hardware.

Bit	Description
7:0	**SIDETIM Field 1** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.

14.1.24 SDMA_CNT—Synchronous DMA Control Register (SATA–D31:F2)

Address Offset:	48h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Note: This register is R/W to maintain software compatibility. These bits have no effect on hardware.

Bit	Description
7:4	Reserved
3:0	**SDMA_CNT Field 1** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.

14.1.25 SDMA_TIM—Synchronous DMA Timing Register (SATA–D31:F2)

Address Offset:	4Ah–4Bh	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

Note: This register is R/W to maintain software compatibility. These bits have no effect on hardware.

Bit	Description
15:14	Reserved
13:12	**SDMA_TIM Field 4**— R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
11:10	Reserved
9:8	**SDMA_TIM Field 3**— R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
7:6	Reserved
5:4	**SDMA_TIM Field 2**— R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
3:2	Reserved
1:0	**SDMA_TIM Field 1** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.

14.1.26 IDE_CONFIG—IDE I/O Configuration Register (SATA–D31:F2)

Address Offset:	54h–57h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Note: This register is R/W to maintain software compatibility. These bits have no effect on hardware.

Bit	Description
31:24	Reserved
23:12	**IDE_CONFIG Field 2** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
11:8	Reserved
7:0	**IDE_CONFIG Field 1** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.

14.1.27 PID—PCI Power Management Capability Identification Register (SATA–D31:F2)

Address Offset:	70h–71h	Attribute:	RO
Default Value:	See Register Description	Size:	16 bits

Bits	Description
15:8	Next Capability (NEXT)—RO. B0h—if SCC = 01h (IDE mode) indicating next item is FLR capability pointer. A8h—for all other values of SCC to point to the next capability structure.
7:0	Capability ID (CID)—RO. Hardwired to 01h. Indicates that this pointer is a PCI power management.

14.1.28 PC—PCI Power Management Capabilities Register (SATA–D31:F2)

Address Offset: 72h–73h Attribute: RO
Default Value: See Register Description Size: 16 bits

Bits	Description
15:11	**PME Support (PME_SUP)**—RO. 00000 = If SCC = 01h, indicates no PME support in IDE mode. 01000 = If SCC is not 01h, in a non-IDE mode, indicates PME# can be generated from the $D3_{HOT}$ state in the SATA host controller.
10	D2 Support (D2_SUP)—RO. Hardwired to 0. The D2 state is not supported
9	D1 Support (D1_SUP)—RO. Hardwired to 0. The D1 state is not supported
8:6	**Auxiliary Current (AUX_CUR)**—RO. PME# from $D3_{COLD}$ state is not supported, therefore this field is 000b.
5	**Device Specific Initialization (DSI)**—RO. Hardwired to 0 to indicate that no device-specific initialization is required.
4	Reserved
3	PME Clock (PME_CLK)—RO. Hardwired to 0 to indicate that PCI clock is not required to generate PME#.
2:0	**Version (VER)**—RO. Hardwired to 011 to indicates support for Revision 1.2 of the PCI Power Management Specification.

14.1.29 PMCS—PCI Power Management Control and Status Register (SATA–D31:F2)

Address Offset: 74h–75h Attribute: R/W, R/WC
Default Value: 0008h Size: 16 bits
Function Level Reset: No (Bits 8 and 15)

Bits	Description
15	**PME Status (PMES)**—R/WC. Bit is set when a PME event is to be requested, and if this bit and PMEE is set, a PME# will be generated from the SATA controller. ***Note:*** Whenever SCC = 01h, hardware will automatically change the attribute of this bit to RO '0'. Software is advised to clear PMEE and PMES together prior to changing SCC thru MAP.SMS. This bit is not reset by Function Level Reset.
14:9	Reserved
8	**PME Enable (PMEE)**—R/W. When set, the SATA controller generates PME# form $D3_{HOT}$ on a wake event. ***Note:*** Whenever SCCSCC = 01h, hardware will automatically change the attribute of this bit to RO '0'. Software is advised to clear PMEE and PMES together prior to changing SCC thru MAP.SMS. This bit is not reset by Function Level Reset.
7:4	Reserved
3	**No Soft Reset (NSFRST)**—RO. These bits are used to indicate whether devices transitioning from $D3_{HOT}$ state to D0 state will perform an internal reset. 0 = Device transitioning from $D3_{HOT}$ state to D0 state perform an internal reset. 1 = Device transitioning from $D3_{HOT}$ state to D0 state do not perform an internal reset. Configuration content is preserved. Upon transition from the $D3_{HOT}$ state to D0 state initialized state, no additional operating system intervention is required to preserve configuration context beyond writing to the PowerState bits. Regardless of this bit, the controller transition from $D3_{HOT}$ state to D0 state by a system or bus segment reset will return to the state D0 uninitialized with only PME context preserved if PME is supported and enabled.
2	Reserved

Bits	Description
1:0	**Power State (PS)**—R/W. These bits are used both to determine the current power state of the SATA controller and to set a new power state. 00 = D0 state 11 = $D3_{HOT}$ state When in the $D3_{HOT}$ state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked.

14.1.30 MSICI—Message Signaled Interrupt Capability Identification (SATA–D31:F2)

Address Offset:	80h–81h	Attribute:	RO
Default Value:	7005h	Size:	16 bits

Note: There is no support for MSI when the software is operating in legacy (IDE) mode when AHCI is not enabled. Prior to switching from AHCI to IDE mode, software **must** make sure that MSI is disabled.

Bits	Description
15:8	**Next Pointer (NEXT)—**RO. Indicates the next item in the list is the PCI power management pointer.
7:0	**Capability ID (CID)—**RO. Capabilities ID indicates MSI.

14.1.31 MSIMC—Message Signaled Interrupt Message Control (SATA–D31:F2)

Address Offset:	82h–83h	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits

Note: There is no support for MSI when the software is operating in legacy (IDE) mode when AHCI is not enabled. Prior to switching from AHCI to IDE mode, software **must** make sure that MSI is disabled.

Bits	Description
15:8	Reserved
7	**64 Bit Address Capable (C64)—**RO. Capable of generating a 32-bit message only.

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>6:4</td><td>

Multiple Message Enable (MME)—RO.

= 000 (and MSIE is set), a single MSI message will be generated for all SATA ports, and bits [15:0] of the message vector will be driven from MD[15:0].

For 6 port components:

<table>
<tr><th rowspan="2">MME</th><th colspan="4">Value Driven on MSI Memory Write</th></tr>
<tr><th>Bits[15:3]</th><th>Bit[2]</th><th>Bit[1]</th><th>Bit[0]</th></tr>
<tr><td>000, 001, 010</td><td>MD[15:3]</td><td>MD[2]</td><td>MD[1]</td><td>MD[0]</td></tr>
<tr><td>011</td><td>MD[15:3]</td><td>Port 0: 0
Port 1: 0
Port 2: 0
Port 3: 0
Port 4: 1
Port 5: 1</td><td>Port 0: 0
Port 1: 0
Port 2: 1
Port 3: 1
Port 4: 0
Port 5: 0</td><td>Port 0: 0
Port 1: 1
Port 2: 0
Port 3: 1
Port 4: 0
Port 5: 1</td></tr>
</table>

<table>
<tr><th rowspan="2">MME</th><th colspan="4">Value Driven on MSI Memory Write</th></tr>
<tr><th>Bits[15:3]</th><th>Bit[2]</th><th>Bit[1]</th><th>Bit[0]</th></tr>
<tr><td>000, 001, 010</td><td>MD[15:3]</td><td>MD[2]</td><td>MD[1]</td><td>MD[0]</td></tr>
<tr><td>011</td><td>MD[15:3]</td><td>Port 0: 0
Port 1: 0
Port 4: 1
Port 5: 1</td><td>Port 0: 0
Port 1: 0
Port 2: 0
Port 3: 0</td><td>Port 0: 0
Port 1: 1
Port 2: 0
Port 3: 1</td></tr>
</table>

All other MME values are reserved. If this field is set to one of these reserved values, the results are undefined.

Note: The CCC interrupt is generated on unimplemented port (AHCI PI register bit equal to 0). If CCC interrupt is disabled, no MSI shall be generated for the port dedicated to the CCC interrupt. When CCC interrupt occurs, MD[2:0] is dependant on CCC_CTL.INT (in addition to MME).

</td></tr>
<tr><td>3:1</td><td>**Multiple Message Capable (MMC)—**RO. MMC is not supported.</td></tr>
<tr><td>0</td><td>

MSI Enable (MSIE)—R/W /RO. If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. This bit is R/W when SC.SCC is not 01h and is read-only ‘0’ when SCC is 01h. Note that CMD.ID bit has no effect on MSI.

Note: Software must clear this bit to ‘0’ to disable MSI first before changing the number of messages allocated in the MMC field. Software must also make sure this bit is cleared to ‘0’ when operating in legacy mode (when GHC.AE = 0).

</td></tr>
</table>

14.1.32 MSIMA—Message Signaled Interrupt Message Address (SATA–D31:F2)

Address Offset:	84h–87h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Note: There is no support for MSI when the software is operating in legacy (IDE) mode when AHCI is not enabled. Prior to switching from AHCI to IDE mode, software **must** make sure that MSI is disabled.

Bits	Description
31:2	**Address (ADDR)—**R/W. Lower 32 bits of the system specified message address, always DWORD aligned.
1:0	Reserved

14.1.33 MSIMD—Message Signaled Interrupt Message Data (SATA–D31:F2)

Address Offset:	88h–89h	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

Note: There is no support for MSI when the software is operating in legacy (IDE) mode when AHCI is not enabled. Prior to switching from AHCI to IDE mode, software **must** make sure that MSI is disabled.

Bits	Description
15:0	**Data (DATA)—**R/W. This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word of the data bus of the MSI memory write transaction. Note that when the MME field is set to ‘001’ or ‘010’, bit [0] and bits [1:0] respectively of the MSI memory write transaction will be driven based on the source of the interrupt rather than from MD[2:0]. See the description of the MME field.

14.1.34 MAP—Address Map Register (SATA–D31:F2)

Address Offset: 90h Attribute: R/W, R/WO
Default Value: 0000hSize: 16 bits
Function Level Reset: No (Bits 7:5 and 13:8 only)

Bits	Description
15:14	Reserved
13:8	Reserved
7:6	**SATA Mode Select (SMS)—**R/W. Software programs these bits to control the mode in which the SATA Controller should operate: 00b = IDE mode 01b = AHCI mode 10b = RAID mode 11b = Reserved **NOTES:** 1. The SATA Function Device ID will change based on the value of this register. 2. When switching from AHCI or RAID mode to IDE mode, a 2 port SATA controller (Device 31, Function 5) will be enabled. 3. AHCI mode may only be selected when MV = 00 4. RAID mode may only be selected when MV = 00 5. Programming these bits with values that are invalid (e.g. selecting RAID when in combined mode) will result in indeterministic behavior by the HW 6. Software shall not manipulate SMS during runtime operation; that is, the operating system will not do this. The BIOS may choose to switch from one mode to another during POST. These bits are not reset by Function Level Reset.
5	**SATA Port-to-Controller Configuration (SC)—**R/W. This bit changes the number of SATA ports available within each SATA Controller. 0 = Up to 4 SATA ports are available for Controller 1 (Device 31 Function 2) with ports [3:0] and up to 2 SATA ports are available for Controller 2 (Device 31 Function 5) with ports [5:4]. 1 = Up to 6 SATA ports are available for Controller 1 (Device 31 Function 2) with ports [5:0] and no SATA ports are available for Controller 2 (Device 31 Function 5). This bit should be set to 1 in AHCI/RAID mode. This bit is not reset by Function Level Reset.
4:0	Reserved

14.1.35 PCS—Port Control and Status Register (SATA–D31:F2)

Address Offset: 92h–93h Attribute: R/W, RO
Default Value: 0000h Size: 16 bits
Function Level Reset: No

By default, the SATA ports are set to the disabled state (bits [5:0] = '0'). When enabled by software, the ports can transition between the on, partial, and slumber states and can detect devices. When disabled, the port is in the "off" state and cannot detect any devices.

If an AHCI-aware or RAID enabled operating system is being booted, then system BIOS shall insure that all supported SATA ports are enabled prior to passing control to the operating system. Once the AHCI aware operating system is booted it becomes the enabling/disabling policy owner for the individual SATA ports. This is accomplished by manipulating a port's PxSCTL and PxCMD fields. Because an AHCI or RAID aware operating system will typically not have knowledge of the PxE bits and because the PxE bits act as master on/off switches for the ports, pre-boot software must insure that these bits are set to '1' prior to booting the operating system, regardless as to whether or not a device is currently on the port.

Bits	Description
15	**OOB Retry Mode (ORM)—**R/W. 0 = The SATA controller will not retry after an OOB failure 1 = The SATA controller will continue to retry after an OOB failure until successful (infinite retry)
14	Reserved.
13	**Port 5 Present (P5P)—**RO. The status of this bit may change at any time. This bit is cleared when the port is disabled using P5E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 5 has been detected.
12	**Port 4 Present (P4P)—**RO. The status of this bit may change at any time. This bit is cleared when the port is disabled using P4E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 4 has been detected.
11	**Port 3 Present (P3P)—**RO. The status of this bit may change at any time. This bit is cleared when the port is disabled using P3E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 3 has been detected.
10	**Port 2 Present (P2P)—**RO. The status of this bit may change at any time. This bit is cleared when the port is disabled using P2E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 2 has been detected.
9	**Port 1 Present (P1P)—**RO. The status of this bit may change at any time. This bit is cleared when the port is disabled using P1E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 1 has been detected.
8	**Port 0 Present (P0P)—**RO. The status of this bit may change at any time. This bit is cleared when the port is disabled using P0E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 0 has been detected.
7:6	Reserved
5	**Port 5 Enabled (P5E)**—R/W, RO. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. ***Note:*** This bit takes precedence over P5CMD.SUD (offset ABAR+398h:bit 1) If MAP.SC is '0', if SCC is '01h' this bit will be read only '0' or if MAP.SPD[5] is '1'.

Bits	Description
4	**Port 4 Enabled (P4E)**—R/W, RO. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. ***Note:*** This bit takes precedence over P4CMD.SUD (offset ABAR+318h:bit 1) If MAP.SC is '0', if SCC is '01h' this bit will be read only '0' or if MAP.SPD[4] is '1'.
3	**Port 3 Enabled (P3E)**—R/W, RO. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. ***Note:*** This bit takes precedence over P3CMD.SUD (offset ABAR+298h:bit 1). When MAP.SPD[3] is '1' this is reserved and is read-only 0.
2	**Port 2 Enabled (P2E)**—R/W, RO. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. ***Note:*** This bit takes precedence over P2CMD.SUD (offset ABAR+218h:bit 1). When MAP.SPD[2] is '1' this is reserved and is read-only 0.
1	**Port 1 Enabled (P1E)**—R/W, RO. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. ***Note:*** This bit takes precedence over P1CMD.SUD (offset ABAR+198h:bit 1). When MAP.SPD[1] is '1' this is reserved and is read-only 0.
0	**Port 0 Enabled (P0E)**—R/W, RO. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. ***Note:*** This bit takes precedence over P0CMD.SUD (offset ABAR+118h:bit 1). When MAP.SPD[0] is '1' this is reserved and is read-only 0.

14.1.36 SCLKCG—SATA Clock Gating Control Register

Address Offset:	94h–97h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:30	Reserved.
29:24	**Port Clock Disable (PCD)—**R/W 0 = All clocks to the associated port logic will operate normally. 1 = The backbone clock driven to the associated port logic is gated and will not toggle. Bit 29: Port 5 Bit 28: Port 4 Bit 27: Port 3 BIt 26: Port 2 Bit 25: Port 1 Bit 24: Port 0 If a port is not available, software shall set the corresponding bit to 1. Software can also set the corresponding bits to 1 on ports that are disabled. Software cannot set the PCD [port x]='1' if the corresponding PCS.PxE='1' in either Dev31Func2 or Dev31Func5 (dual controller IDE mode).
23:9	Reserved.
8:0	**SCLKCG Field 1**—R/W. BIOS must program these bits to 183h.

14.1.37 SGC—SATA General Configuration Register

Address Offset:	9Ch–9Fh	Attribute:	R/W, R/WO
Default Value:	00000000h	Size:	32 bits
Function Level Reset:	No		

Bit	Description
31:10	Reserved
9	BIOS must program this bit to 1b.
8	Reserved
7 (PCH Raid Capable SKUs Only)	**Alternate ID Enable (AIE)—**R/WO. 0 = When in RAID mode the SATA Controller located at Device 31: Function 2 will report the following Device ID 2826h the PCH and the Microsoft Windows Vista* and Windows* 7 in-box version of the Intel® Rapid Storage Technology enterprise will load on the platform. 1 = When in RAID mode the SATA Controller located at Device 31: Function 2 will report the Device ID 1D04h for RAID 0/1/5/10, to prevent the Microsoft Windows Vista or Windows 7 in-box version of the Intel® Rapid Storage Technology enterprise from loading on the platform and will require the user to perform an 'F6' installation of the appropriate Intel® Rapid Storage Technology enterprise. ***Note:*** This field is applicable when the AHCI is configured for RAID mode of operation. It has no impact for AHCI and IDE modes of operation. BIOS is recommended to program this bit prior to programming the MAP.SMS field to reflect RAID. This field is reset by PLTRST#. BIOS is required to reprogram the value of this bit after resuming from S3, S4 and S5.
6:2	**SATA Traffic Monitor**—R/W. 00000b = Disable. 00011b = Enable. SATA Traffic Monitor allows for aggressive C2 Pop down by monitoring SATA bus mastering activity. When enabled, BIOS must ensure bit 3 and bit 4 of Cx_STATE_CNF (Cx State Configuration Register) are ones. ***Note:*** This field is reset by PLTRST# and BIOS is required to reprogram the value after resuming from S3–S5. All other bit combinations are Reserved.
1	Reserved
0	**SATA4-port All Master Configuration Indicator (SATA4PMIND)—**RO. 0 = Normal configuration. 1 = Two IDE Controllers are implemented, each supporting two ports for a Primary Master and a Secondary Master. ***Note:*** When set, BIOS must ensure that bit 2 and bit 3 of the AHCI PI registers are zeros. BIOS must also make sure that Port 2 and Port 3 are disabled (using PCS configuration register) and the port clocks are gated (using SCLKCG configuration register).

14.1.37.1 SATACR0—SATA Capability Register 0 (SATA–D31:F2)

Address Offset:	A8h–ABh	Attribute:	RO, R/WO
Default Value:	0010B012h	Size:	32 bits
Function Level Reset:	No (Bits 15:8 only)		

Note: This register shall be read-only 0 when SCC is 01h.

Bit	Description
31:24	Reserved
23:20	**Major Revision (MAJREV)**—RO. Major revision number of the SATA Capability Pointer implemented.
19:16	**Minor Revision (MINREV)**—RO. Minor revision number of the SATA Capability Pointer implemented.
15:8	**Next Capability Pointer (NEXT)**—R/WO. Points to the next capability structure. These bits are not reset by Function Level Reset.
7:0	**Capability ID (CAP)**—RO: This value of 12h has been assigned by the PCI SIG to designate the SATA Capability Structure.

14.1.37.2 SATACR1—SATA Capability Register 1 (SATA–D31:F2)

Address Offset:	ACh–AFh	Attribute:	RO
Default Value:	00000048h	Size:	32 bits

Note: This register shall be read-only 0 when SCC is 01h.

Bit	Description
31:16	Reserved
15:4	**BAR Offset (BAROFST)—**RO**:** Indicates the offset into the BAR where the Index/Data pair are located (in DWord granularity). The Index and Data I/O registers are located at offset 10h within the I/O space defined by LBAR. A value of 004h indicates offset 10h. 000h = 0h offset 001h = 4h offset 002h = 8h offset 003h = Bh offset 004h = 10h offset ... FFFh = 3FFFh offset (max 16KB)
3:0	**BAR Location (BARLOC)—**RO**:** Indicates the absolute PCI Configuration Register address of the BAR containing the Index/Data pair (in DWord granularity). The Index and Data I/O registers reside within the space defined by LBAR in the SATA controller. A value of 8h indicates offset 20h, which is LBAR. 0000 – 0011b = reserved 0100b = 10h => BAR0 0101b = 14h => BAR1 0110b = 18h => BAR2 0111b = 1Ch => BAR3 1000b = 20h => LBAR 1001b = 24h => BAR5 1010 – 1110b = reserved 1111b = Index/Data pair in PCI Configuration space. This is not supported in the PCH.

14.1.38 FLRCID—FLR Capability ID (SATA–D31:F2)

Address Offset:	B0–B1h	Attribute:	RO
Default Value:	0009h	Size:	16 bits

Bit	Description
15:8	**Next Capability Pointer—**RO. 00h indicates the final item in the capability list.
7:0	**Capability ID—**RO. The value of this field depends on the FLRCSSEL (RCBA+3410h:bit 12) bit. 13h = If PFLRCSSEL = 0 09h (Vendor Specific) = If PFLRCSSEL = 1

14.1.39 FLRCLV—FLR Capability Length and Version (SATA–D31:F2)

Address Offset: B2–B3h Attribute: RO, R/WO
Default Value: xx06h Size: 16 bits
Function Level Reset: No (Bit 9:8 Only when FLRCSSEL = '0')

When FLRCSSEL (RCBA+3410h:bit 12) = '0', this register is defined as follows:

Bit	Description
15:10	Reserved.
9	**FLR Capability—**R/WO. 1 = Support for Function Level reset. This bit is not reset by the Function Level Reset.
8	**TXP Capability—**R/WO. 1 = Support for Transactions Pending (TXP) bit. TXP must be supported if FLR is supported.
7:0	**Vendor-Specific Capability ID**—RO. This field indicates the # of bytes of this Vendor Specific capability as required by the PCI specification. It has the value of 06h for the FLR capability.

When FLRCSSEL = '1', this register is defined as follows:

Bit	Description
15:12	**Vendor-Specific Capability ID**—RO. A value of 2h identifies this capability as the Function Level Reset (FLR).
11:8	**Capability Version—**RO. This field indicates the version of the FLR capability.
7:0	**Vendor-Specific Capability ID**—RO. This field indicates the # of bytes of this Vendor Specific capability as required by the PCI specification. It has the value of 06h for the FLR capability.

14.1.40 FLRC—FLR Control (SATA–D31:F2)

Address Offset: B4–B5h Attribute: RO, R/W
Default Value: 0000h Size: 16 bits

Bit	Description
15:9	Reserved.
8	**Transactions Pending (TXP)—**RO. 0 = Controller has received all non-posted requests. 1 = Controller has issued non-posted requests which has not been completed.
7:1	Reserved.
0	**Initiate FLR—**R/W. Used to initiate FLR transition. A write of '1' indicates FLR transition. Since hardware must no t respond to any cycles till FLR completion the value read by software from this bit is '0'.

14.1.41 ATC—APM Trapping Control Register (SATA–D31:F2)

Address Offset: C0h
Attribute: R/W
Default Value: 00h
Size: 8 bits
Function Level Reset: No

Bit	Description
7:4	Reserved
3	**Secondary Slave Trap (SST)—**R/W. Enables trapping and SMI# assertion on legacy I/O accesses to 170h-177h and 376h. The active device on the secondary interface must be device 1 for the trap and/or SMI# to occur.
2	**Secondary Master Trap (SPT)—**R/W. Enables trapping and SMI# assertion on legacy I/O accesses to 170h-177h and 376h. The active device on the secondary interface must be device 0 for the trap and/or SMI# to occur.
1	**Primary Slave Trap (PST)—**R/W. Enables trapping and SMI# assertion on legacy I/O accesses to 1F0h-1F7h and 3F6h. The active device on the primary interface must be device 1 for the trap and/or SMI# to occur.
0	**Primary Master Trap (PMT)—**R/W. Enables trapping and SMI# assertion on legacy I/O accesses to 1F0h-1F7h and 3F6h. The active device on the primary interface must be device 0 for the trap and/or SMI# to occur.

14.1.42 ATS—APM Trapping Status Register (SATA–D31:F2)

Address Offset: C4h
Attribute: R/WC
Default Value: 00h
Size: 8 bits
Function Level Reset: No

Bit	Description
7:4	Reserved
3	**Secondary Slave Trap (SST)—**R/WC. Indicates that a trap occurred to the secondary slave device.
2	**Secondary Master Trap (SPT)—**R/WC. Indicates that a trap occurred to the secondary master device.
1	**Primary Slave Trap (PST)—**R/WC. Indicates that a trap occurred to the primary slave device.
0	**Primary Master Trap (PMT)—**R/WC. Indicates that a trap occurred to the primary master device.

14.1.43 SP Scratch Pad Register (SATA–D31:F2)

Address Offset: D0h
Attribute: R/W
Default Value: 00000000h
Size: 32 bits

Bit	Description
31:0	**Data (DT)—**R/W. This is a read/write register that is available for software to use. No hardware action is taken on this register.

14.1.44 BFCS—BIST FIS Control/Status Register (SATA–D31:F2)

Address Offset:	E0h–E3h	Attribute:	R/W, R/WC
Default Value:	00000000h	Size:	32 bits

Bits	Description
31:16	Reserved
15	**Port 5 BIST FIS Initiate (P5BFI)**—R/W. When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 5, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 5 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISs or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P5BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully.
14	**Port 4 BIST FIS Initiate (P4BFI)**—R/W. When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 4, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 4 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISs or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P4BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully.
13	**Port 3 BIST FIS Initiate (P3BFI)**—R/W. When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 3, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 3 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISs or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P3BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully.
12	**Port 2 BIST FIS Initiate (P2BFI)**—R/W. When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 2, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 2 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISes or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P2BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully.
11	**BIST FIS Successful (BFS)**—R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set any time a BIST FIS transmitted by PCH receives an R_OK completion status from the device. ***Note:*** This bit must be cleared by software prior to initiating a BIST FIS.
10	**BIST FIS Failed (BFF)**—R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set any time a BIST FIS transmitted by PCH receives an R_ERR completion status from the device. ***Note:*** This bit must be cleared by software prior to initiating a BIST FIS.
9	**Port 1 BIST FIS Initiate (P1BFI)**—R/W. When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 1, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 1 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISes or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P1BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully.

Bits	Description
8	**Port 0 BIST FIS Initiate (P0BFI)—**R/W. When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 0, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 0 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISes or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P0BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully.
7:2	**BIST FIS Parameters (BFP)—**R/W. These 6 bits form the contents of the upper 6 bits of the BIST FIS Pattern Definition in any BIST FIS transmitted by the PCH. This field is not port specific—its contents will be used for any BIST FIS initiated on port 0, port 1, port 2 or port 3. The specific bit definitions are: Bit 7: T – Far End Transmit mode Bit 6: A – Align Bypass mode Bit 5: S – Bypass Scrambling Bit 4: L – Far End Retimed Loopback Bit 3: F – Far End Analog Loopback Bit 2: P – Primitive bit for use with Transmit mode
1:0	Reserved

14.1.45 BFTD1—BIST FIS Transmit Data1 Register (SATA–D31:F2)

Address Offset:	E4h–E7h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bits	Description
31:0	**BIST FIS Transmit Data 1**—R/W. The data programmed into this register will form the contents of the second DWord of any BIST FIS initiated by the PCH. This register is not port specific—its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the "T" bit of the BIST FIS is set to indicate "Far-End Transmit mode", this register's contents will be transmitted as the BIST FIS 2nd DW regardless of whether or not the "T" bit is indicated in the BFCS register (D31:F2:E0h).

14.1.46 BFTD2—BIST FIS Transmit Data2 Register (SATA–D31:F2)

Address Offset:	E8h–EBh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bits	Description
31:0	**BIST FIS Transmit Data 2—**R/W. The data programmed into this register will form the contents of the third DWord of any BIST FIS initiated by the PCH. This register is not port specific—its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the "T" bit of the BIST FIS is set to indicate "Far-End Transmit mode", this register's contents will be transmitted as the BIST FIS 3rd DW regardless of whether or not the "T" bit is indicated in the BFCS register (D31:F2:E0h).

14.2 Bus Master IDE I/O Registers (D31:F2)

The bus master IDE function uses 16 bytes of I/O space, allocated using the BAR register, located in Device 31:Function 2 Configuration space, offset 20h. All bus master IDE I/O space registers can be accessed as byte, word, or DWord quantities. Reading reserved bits returns an indeterminate, inconsistent value, and writes to reserved bits have no affect (but should not be attempted). These registers are only used for legacy operation. Software must not use these registers when running AHCI. All I/O registers are reset by Function Level Reset. The description of the I/O registers address map is shown in Table 14-2.

Table 14-2. Bus Master IDE I/O Register Address Map

BAR+ Offset	Mnemonic	Register	Default	Type
00h	BMICP	Command Register Primary	00h	R/W
01h	—	Reserved	—	RO
02h	BMISP	Bus Master IDE Status Register Primary	00h	R/W, R/WC, RO
03h	—	Reserved	—	RO
04h–07h	BMIDP	Bus Master IDE Descriptor Table Pointer Primary	xxxxxxxxh	R/W
08h	BMICS	Command Register Secondary	00h	R/W
09h	—	Reserved	—	RO
0Ah	BMISS	Bus Master IDE Status Register Secondary	00h	R/W, R/WC, RO
0Bh	—	Reserved	—	RO
0Ch–0Fh	BMIDS	Bus Master IDE Descriptor Table Pointer Secondary	xxxxxxxxh	R/W
10h	AIR	AHCI Index Register	00000000h	R/W, RO
14h	AIDR	AHCI Index Data Register	xxxxxxxxh	R/W

14.2.1 BMIC[P,S]—Bus Master IDE Command Register (D31:F2)

Address Offset:	Primary: BAR + 00h Secondary: BAR + 08h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:4	Reserved. Returns 0.
3	**Read / Write Control (R/WC)—**R/W. This bit sets the direction of the bus master transfer. This bit must NOT be changed when the bus master function is active. 0 = Memory reads 1 = Memory writes
2:1	Reserved. Returns 0.

Bit	Description
0	**Start/Stop Bus Master (START)—**R/W. 0 = All state information is lost when this bit is cleared. Master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active (that is, the Bus Master IDE Active bit (D31:F2:BAR + 02h, bit 0) of the Bus Master IDE Status register for that IDE channel is set) and the drive has not yet finished its data transfer (the Interrupt bit in the Bus Master IDE Status register for that IDE channel is not set), the bus master command is said to be aborted and data transferred from the drive may be discarded instead of being written to system memory. 1 = Enables bus master operation of the controller. Bus master operation does not actually start unless the Bus Master Enable bit (D31:F2:04h, bit 2) in PCI configuration space is also set. Bus master operation begins when this bit is detected changing from 0 to 1. The controller will transfer data between the IDE device and memory only when this bit is set. Master operation can be halted by writing a 0 to this bit. ***Note:*** This bit is intended to be cleared by software after the data transfer is completed, as indicated by either the Bus Master IDE Active bit being cleared or the Interrupt bit of the Bus Master IDE Status register for that IDE channel being set, or both. Hardware does not clear this bit automatically. If this bit is cleared to 0 prior to the DMA data transfer being initiated by the drive in a Device to memory data transfer, then the PCH will not send DMAT to terminate the data transfer. Software intervention (such as sending SRST) is required to reset. the interface in this condition.

14.2.2 BMIS[P,S]—Bus Master IDE Status Register (D31:F2)

Address Offset:	Primary: BAR + 02h Secondary: BAR + 0Ah	Attribute:	R/W, R/WC, RO
Default Value:	00h	Size:	8 bits

Bit	Description
7	**Simplex Only**—RO. 0 = Both bus master channels (primary and secondary) can be operated independently and can be used at the same time. 1 = Only one channel may be used at the same time.
6	**Drive 1 DMA Capable—**R/W. 0 = Not Capable. 1 = Capable. Set by device dependent code (BIOS or device driver) to indicate that drive 1 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance. The PCH does not use this bit. It is intended for systems that do not attach BMIDE to the PCI bus.
5	**Drive 0 DMA Capable—**R/W. 0 = Not Capable 1 = Capable. Set by device dependent code (BIOS or device driver) to indicate that drive 0 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance. The PCH does not use this bit. It is intended for systems that do not attach BMIDE to the PCI bus.
4:3	Reserved. Returns 0.
2	**Interrupt—**R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = Set when a device FIS is received with the 'I' bit set, provided that software has not disabled interrupts using the IEN bit of the Device Control Register (see chapter 5 of the *Serial ATA Specification*, Revision 1.0a).
1	**Error—**R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set when the controller encounters a target abort or master abort when transferring data on PCI.
0	**Bus Master IDE Active (ACT)**—RO. 0 = This bit is cleared by the PCH when the last transfer for a region is performed, where EOT for that region is set in the region descriptor. It is also cleared by the PCH when the Start Bus Master bit (D31:F2:BAR+ 00h, bit 0) is cleared in the Command register. When this bit is read as a 0, all data transferred from the drive during the previous bus master command is visible in system memory, unless the bus master command was aborted. 1 = Set by the PCH when the Start bit is written to the Command register.

14.2.3 BMID[P,S]—Bus Master IDE Descriptor Table Pointer Register (D31:F2)

Address Offset:	Primary: BAR + 04h–07h Secondary: BAR + 0Ch–0Fh	Attribute:	R/W
Default Value:	All bits undefined	Size:	32 bits

Bit	Description
31:2	**Address of Descriptor Table (ADDR)**—R/W. The bits in this field correspond to bits [31:2] of the memory location of the Physical Region Descriptor (PRD). The Descriptor Table must be Dword-aligned. The Descriptor Table must not cross a 64-K boundary in memory.
1:0	Reserved

14.2.4 AIR—AHCI Index Register (D31:F2)

Address Offset:	Primary: BAR + 10h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

This register is available only when SCC is not 01h.

Bit	Description
31:11	Reserved
10:2	**Index (INDEX)**—R/W: This Index register is used to select the Dword offset of the Memory Mapped AHCI register to be accessed. A Dword, Word or Byte access is specified by the active byte enables of the I/O access to the Data register.
1:0	Reserved

14.2.5 AIDR—AHCI Index Data Register (D31:F2)

Address Offset:	Primary: BAR + 14h	Attribute:	R/W
Default Value:	All bits undefined	Size:	32 bits

This register is available only when SCC is not 01h.

Bit	Description
31:0	**Data (DATA)**—R/W: This Data register is a "window" through which data is read or written to the AHCI memory mapped registers. A read or write to this Data register triggers a corresponding read or write to the memory mapped register pointed to by the Index register. The Index register must be setup prior to the read or write to this Data register. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the "default" value is the same as the default value of the register pointed to by Index.

14.3 Serial ATA Index/Data Pair Superset Registers

All of these I/O registers are in the core well. They are exposed only when SCC is 01h (that is, IDE programming interface).

These are Index/Data Pair registers that are used to access the SerialATA superset registers (SerialATA Status (PxSSTS), SerialATA Control (PxSCTL) and SerialATA Error (PxSERR)). The I/O space for these registers is allocated through SIDPBA. Locations with offset from 08h to 0Fh are reserved for future expansion. Software-write operations to the reserved locations will have no effect while software-read operations to the reserved locations will return 0.

Offset	Mnemonic	Register
00h–03h	SINDEX	Serial ATA Index
04h–07h	SDATA	Serial ATA Data
08h–0Ch	—	Reserved
0Ch–0Fh	—	Reserved

14.3.1 SINDX—Serial ATA Index (D31:F2)

Address Offset: SIDPBA + 00h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:16	Reserved
15.8	**Port Index (PIDX)**—R/W. This Index field is used to specify the port of the SATA controller at which the port-specific SSTS, SCTL, and SERR registers are located. 00h = Primary Master (Port 0) 01h = Primary Slave (Port 2) 02h = Secondary Master (Port 1) 03h = Secondary Slave (Port 3) All other values are Reserved.
7:0	**Register Index (RIDX)**—R/W. This index field is used to specify one out of three registers currently being indexed into. These three registers are the Serial ATA superset SStatus, SControl and SError memory registers and are port specific, hence for this SATA controller, there are four sets of these registers. Refer to Section 14.4.2.10, Section 14.4.2.11, and Section 14.4.2.12 for definitions of the SStatus, SControl and SError registers. 00h = SSTS 01h = SCTL 02h = SERR All other values are Reserved.

14.3.2 SDATA—Serial ATA Data (D31:F2)

Address Offset: SIDPBA + 04h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	**Data (DATA)**—R/W. This Data register is a "window" through which data is read or written to from the register pointed to by the Serial ATA Index (SINDX) register above. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the "default" value is the same as the default value of the register pointed to by SINDX.RIDX field.

14.3.2.1 PxSSTS—Serial ATA Status Register (D31:F2)

Address Offset:		Attribute:	RO
Default Value:	00000000h	Size:	32 bits

SDATA when SINDX.RIDX is 00h. This is a 32-bit register that conveys the current state of the interface and host. The PCH updates it continuously and asynchronously. When the PCH transmits a COMRESET to the device, this register is updated to its reset values.

Bit	Description
31:12	Reserved
11:8	**Interface Power Management (IPM)—**RO**.** Indicates the current interface state: **Value** — **Description** 0h — Device not present or communication not established 1h — Interface in active state 2h — Interface in PARTIAL power management state 6h — Interface in SLUMBER power management state All other values reserved.
7:4	**Current Interface Speed (SPD)**—RO. Indicates the negotiated interface communication speed. **Value** — **Description** 0h — Device not present or communication not established 1h — Generation 1 communication rate negotiated 2h — Generation 2 communication rate negotiated 3h — Generation 3communication rate negotiated All other values reserved. The PCH Supports Generation 1 communication rates (1.5 Gb/s) and Gen 2 rates (3.0 Gb/s) and Gen 3 rates (6.0Gb/s).
3:0	**Device Detection (DET)—**RO**.** Indicates the interface device detection and Phy state: **Value** — **Description** 0h — No device detected and Phy communication not established 1h — Device presence detected but Phy communication not established 3h — Device presence detected and Phy communication established 4h — Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode All other values reserved.

14.3.2.2 PxSCTL—Serial ATA Control Register (D31:F2)

Address Offset:		Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

SDATA when SINDX.RIDX is 01h. This is a 32-bit read-write register by which software controls SATA capabilities. Writes to the SControl register result in an action being taken by the PCH or the interface. Reads from the register return the last value written to it.

Bit	Description
31:20	Reserved
19:16	Port Multiplier Port (PMP)—R/W. This field is not used by AHCI.
15:12	Select Power Management (SPM)—R/W. This field is not used by AHCI.
11:8	**Interface Power Management Transitions Allowed (IPM)—**R/W**.** Indicates which power states the PCH is allowed to transition to: **Value** — **Description** 0h — No interface restriction 1h — Transitions to the PARTIAL state disabled 2h — Transitions to the SLUMBER state disabled 3h — Transitions to both PARTIAL and SLUMBER state disabled All other values reserved
7:4	**Speed Allowed (SPD)**—R/W. Indicates the highest allowable speed of the interface. This speed is limited by the CAP.ISS (ABAR+00h:bit 23:20) field. **Value** — **Description** 0h — No speed negotiation restriction 1h — Limit speed negotiation to Generation 1 communication rate 2h — Limit speed negotiation to Generation 2 communication rate 3h — Limit speed negotiation to Generation 3 communication rate All other values reserved. The PCH Supports Generation 1 communication rates (1.5 Gb/s), Gen 2 rates (3.0 Gb/s) and Gen 3 rates (6Gb/s).
3:0	**Device Detection Initialization (DET)—**R/W**.** Controls the PCH's device detection and interface initialization. **Value** — **Description** 0h — No device detection or initialization action requested 1h — Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications re-initialized 4h — Disable the Serial ATA interface and put Phy in offline mode All other values reserved. When this field is written to a 1h, the PCH initiates COMRESET and starts the initialization process. When the initialization is complete, this field shall remain 1h until set to another value by software. This field may only be changed to 1h or 4h when PxCMD.ST is 0. Changing this field while the PCH is running results in undefined behavior.

14.3.2.3 PxSERR—Serial ATA Error Register (D31:F2)

Address Offset:		Attribute:	R/WC
Default Value:	00000000h	Size:	32 bits

SDATA when SINDx.RIDX is 02h.

Bits 26:16 of this register contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes. Bits 11:0 contain error information used by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer.

Bit	Description
31:27	Reserved
26	**Exchanged (X)**: When set to '1' this bit indicates that a change in device presence has been detected since the last time this bit was cleared. This bit shall always be set to 1 anytime a COMINIT signal is received. This bit is reflected in the P0IS.PCS bit.
25	**Unrecognized FIS Type (F)**: Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized.
24	**Transport state transition error (T)**: Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared.
23	**Link Sequence Error (S)**: Indicates that one or more Link state machine error conditions was encountered. The Link Layer state machine defines the conditions under which the link layer detects an erroneous transition.
22	**Handshake (H)**: Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.
21	**CRC Error (C)**: Indicates that one or more CRC errors occurred with the Link Layer.
20	**Disparity Error (D)**: This field is not used by AHCI.
19	**10b to 8b Decode Error (B)**: Indicates that one or more 10b to 8b decoding errors occurred.
18	**Comm Wake (W)**: Indicates that a Comm Wake signal was detected by the Phy.
17	**Phy Internal Error (I)**: Indicates that the Phy detected some internal error.
16	**PhyRdy Change (N)**: When set to 1 this bit indicates that the internal PhyRdy signal changed state since the last time this bit was cleared. In the PCH, this bit will be set when PhyRdy changes from a 0 -> 1 or a 1 -> 0. The state of this bit is then reflected in the PxIS.PRCS interrupt status bit and an interrupt will be generated if enabled. Software clears this bit by writing a 1 to it.
15:12	Reserved
11	**Internal Error (E)**: The SATA controller failed due to a master or target abort when attempting to access system memory.
10	**Protocol Error (P)**: A violation of the Serial ATA protocol was detected. ***Notes:*** The PCH does not set this bit for all protocol violations that may occur on the SATA link.
9	**Persistent Communication or Data Integrity Error (C)**: A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes.
8	**Transient Data Integrity Error (T)**: A data integrity error occurred that was not recovered by the interface.
7:2	Reserved.
1	**Recovered Communications Error (M)**: Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers.
0	**Recovered Data Integrity Error (I)**: A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.

14.4 AHCI Registers (D31:F2)

Note: These registers are AHCI-specific and available when the PCH is properly configured. The Serial ATA Status, Control, and Error registers are special exceptions and may be accessed on all PCH components if properly configured; see Section 14.3 for details.

The memory mapped registers within the SATA controller exist in non-cacheable memory space. Additionally, locked accesses are not supported. If software attempts to perform locked transactions to the registers, indeterminate results may occur. Register accesses shall have a maximum size of 64-bits; 64-bit access must not cross an 8-byte alignment boundary. All memory registers are reset by Function Level Reset unless specified otherwise.

The registers are broken into two sections – generic host control and port control. The port control registers are the same for all ports, and there are as many registers banks as there are ports.

Table 14-3. AHCI Register Address Map

ABAR + Offset	Mnemonic	Register
00–1Fh	GHC	Generic Host Control
20h–FFh	—	Reserved
100h–17Fh	P0PCR	Port 0 port control registers
180h–1FFh	P1PCR	Port 1 port control registers
200h–27Fh	P2PCR	Port 2 port control registers
280h–2FFh	P3PCR	Port 3 port control registers
300h–37Fh	P4PCR	Port 4 port control registers
380h–3FFh	P5PCR	Port 5 port control registers
400h–47Fh	P6PCR	Port 6 port control registers

14.4.1 AHCI Generic Host Control Registers (D31:F2)

Table 14-4. Generic Host Controller Register Address Map

ABAR + Offset	Mnemonic	Register	Default	Type
00–03	CAP	Host Capabilities	FF22FFC2h	R/WO, RO
04–07	GHC	Global PCH Control	00000000h	R/W, RO
08–0Bh	IS	Interrupt Status	00000000h	R/WC
0Ch–0Fh	PI	Ports Implemented	00000000h	R/WO, RO
10h–13h	VS	AHCI Version	00010300h	RO
14h–17h	CCC_CTL	Command Completion Coalescing Control	00010121h	R/W, RO
18h–1Bh	CCC_PORTS	Command Completion Coalescing Ports	00000000h	R/W
1Ch–1Fh	EM_LOC	Enclosure Management Location	01600002h	RO
20h–23h	EM_CTRL	Enclosure Management Control	07010000h	R/W, R/WO, RO
70h–73h	VS	AHCI Version	00010000h	RO
A0h–A3h	VSP	Vendor Specific	00000000h	RO, R/WO
C8h–C9h	RSTF	Intel RST Feature Capabilities	003Fh	R/WO

14.4.1.1 CAP—Host Capabilities Register (D31:F2)

Address Offset: ABAR + 00h–03hAttribute: R/WO, RO
Default Value: FF22FFC2h Size: 32 bits
Function Level Reset:No

All bits in this register that are R/WO are reset only by PLTRST#.

Bit	Description
31	**Supports 64-bit Addressing (S64A)**—RO. Indicates that the SATA controller can access 64-bit data structures. The 32-bit upper bits of the port DMA Descriptor, the PRD Base, and each PRD entry are read/write.
30	**Supports Command Queue Acceleration (SCQA)—**R/WO. When set to 1, indicates that the SATA controller supports SATA command queuing using the DMA Setup FIS. The PCH handles DMA Setup FISes natively, and can handle auto-activate optimization through that FIS.
29	Supports SNotification Register (SSNTF)—RO. The PCH SATA Controller does not support the SNotification register.
28	**Supports Mechanical Presence Switch (SMPS)—**R/WO. When set to 1, indicates whether the SATA controller supports mechanical presence switches on its ports for use in Hot Plug operations. This value is loaded by platform BIOS prior to operating system initialization. If this bit is set, BIOS must also map the SATAGP pins to the SATA controller through GPIO space.
27	**Supports Staggered Spin-up (SSS)—**R/WO. Indicates whether the SATA controller supports staggered spin-up on its ports, for use in balancing power spikes. This value is loaded by platform BIOS prior to operating system initialization. 0 = Staggered spin-up not supported. 1 = Staggered spin-up supported.
26	**Supports Aggressive Link Power Management (SALP)—**R/WO. 0 = Software shall treat the PxCMD.ALPE and PxCMD.ASP bits as reserved. 1 = The SATA controller supports auto-generating link requests to the partial or slumber states when there are no commands to process.
25	**Supports Activity LED (SAL)**—RO. Indicates that the SATA controller supports a single output pin (SATALED#) which indicates activity.
24	**Supports Command List Override (SCLO)**—R/WO. When set to '1', indicates that the Controller supports the PxCMD.CLO bit and its associated function. When cleared to '0', the Controller is not capable of clearing the BSY and DRQ bits in the Status register in order to issue a software reset if these bits are still set from a previous operation.
23:20	**Interface Speed Support (ISS)**—R/WO. Indicates the maximum speed the SATA controller can support on its ports. 1h = 1.5 Gb/s; 2h =3.0 Gb/s; 3h = 6.0 Gb/s.
19	Supports Non-Zero DMA Offsets (SNZO)—RO. Reserved, as per the AHCI Revision 1.3 specification
18	**Supports AHCI Mode Only (SAM)**—RO. The SATA controller may optionally support AHCI access mechanism only. 0 = SATA controller supports both IDE and AHCI Modes 1 = SATA controller supports AHCI Mode Only
17	**Supports Port Multiplier (PMS)**—R/WO. The PCH SATA controller does not support Port Multipliers. BIOS must clear this bit by writing a 0 to this field.
16	Reserved
15	**PIO Multiple DRQ Block (PMD)—**RO. Hardwired to 1. The SATA controller supports PIO Multiple DRQ Command Block
14	**Slumber State Capable (SSC)**—R/WO. When set to 1, the SATA controller supports the slumber state.
13	**Partial State Capable (PSC)**—R/WO. When set to 1, the SATA controller supports the partial state.
12:8	**Number of Command Slots (NCS)**—RO. Hardwired to 1Fh to indicate support for 32 slots.
7	**Command Completion Coalescing Supported (CCCS)—**R/WO. 0 = Command Completion Coalescing Not Supported 1 = Command Completion Coalescing Supported

Bit	Description
6	**Enclosure Management Supported (EMS)—**R/WO. 0 = Enclosure Management Not Supported 1 = Enclosure Management Supported
5	**Supports External SATA (SXS)—**R/WO. 0 = External SATA is not supported on any ports 1 = External SATA is supported on one or more ports When set, Software can examine each SATA port's Command Register (PxCMD) to determine which port is routed externally.
4:0	**Number of Ports (NPS)**—RO. Indicates number of supported ports. Note that the number of ports indicated in this field may be more than the number of ports indicated in the PI (ABAR + 0Ch) register.

14.4.1.2 GHC—Global PCH Control Register (D31:F2)

Address Offset:	ABAR + 04h–07h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31	**AHCI Enable (AE)**—R/W. When set, this bit indicates that an AHCI driver is loaded and the controller will be talked to using AHCI mechanisms. This can be used by an PCH that supports both legacy mechanisms (such as SFF-8038i) and AHCI to know when the controller will not be talked to as legacy. 0 = Software will communicate with the PCH using legacy mechanisms. 1 = Software will communicate with the PCH using AHCI. The PCH will not have to allow command processing using both AHCI and legacy mechanisms. Software shall set this bit to 1 before accessing other AHCI registers.
30:3	Reserved
2	**MSI Revert to Single Message (MRSM)**—RO: When set to '1' by hardware, this bit indicates that the host controller requested more than one MSI vector but has reverted to using the first vector only. When this bit is cleared to '0', the Controller has not reverted to single MSI mode (that is hardware is already in single MSI mode, software has allocated the number of messages requested, or hardware is sharing interrupt vectors if MC.MME < MC.MMC). "MC.MSIE = '1' (MSI is enabled) "MC.MMC > 0 (multiple messages requested) "MC.MME > 0 (more than one message allocated) "MC.MME!= MC.MMC (messages allocated not equal to number requested) When this bit is set to '1', single MSI mode operation is in use and software is responsible for clearing bits in the IS register to clear interrupts. This bit shall be cleared to '0' by hardware when any of the four conditions stated is false. This bit is also cleared to '0' when MC.MSIE = '1' and MC.MME = 0h. In this case, the hardware has been programmed to use single MSI mode, and is not "reverting" to that mode. For PCH, the Controller shall always revert to single MSI mode when the number of vectors allocated by the host is less than the number requested. This bit is ignored when GHC.HR = 1.
1	**Interrupt Enable (IE)—**R/W. This global bit enables interrupts from the PCH. 0 = All interrupt sources from all ports are disabled. 1 = Interrupts are allowed from the AHCI controller.
0	**Controller Reset (HR)**—R/W. Resets PCH AHCI controller. 0 = No effect 1 = When set by software, this bit causes an internal reset of the PCH AHCI controller. All state machines that relate to data transfers and queuing return to an idle condition, and all ports are re-initialized using COMRESET. ***Note:*** For further details, consult Section 10.4.3 of the *Serial ATA Advanced Host Controller Interface* specification revision 1.3.

14.4.1.3 IS—Interrupt Status Register (D31:F2)

Address Offset:	ABAR + 08h–0Bh	Attribute:	R/WC
Default Value:	00000000h	Size:	32 bits

This register indicates which of the ports within the controller have an interrupt pending and require service.

Bit	Description
31:6	Reserved. Returns 0.
5	**Interrupt Pending Status Port[5] (IPS[5])—**R/WC**.** 0 = No interrupt pending. 1 = Port 5 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
4	**Interrupt Pending Status Port[4] (IPS[4])—**R/WC**.** 0 = No interrupt pending. 1 = Port 4 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
3	**Interrupt Pending Status Port[3] (IPS[3])—**R/WC**.** 0 = No interrupt pending. 1 = Port 3 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
2	**Interrupt Pending Status Port[2] (IPS[2])—**R/WC. 0 = No interrupt pending. 1 = Port 2 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
1	**Interrupt Pending Status Port[1] (IPS[1])—**R/WC**.** 0 = No interrupt pending. 1 = Port 1has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
0	**Interrupt Pending Status Port[0] (IPS[0])—**R/WC**.** 0 = No interrupt pending. 1 = Port 0 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.

14.4.1.4 PI—Ports Implemented Register (D31:F2)

Address Offset: ABAR + 0Ch–0Fh
Attribute: R/WO, RO
Default Value: 00000000h
Size: 32 bits
Function Level Reset: No

This register indicates which ports are exposed to the PCH. It is loaded by platform BIOS. It indicates which ports that the device supports are available for software to use. For ports that are not available, software must not read or write to registers within that port.

Bit	Description
31:6	Reserved. Returns 0.
5	**Ports Implemented Port 5 (PI5)**—R/WO. 0 = The port is not implemented. 1 = The port is implemented. This bit is read-only '0' if MAP.SC = '0' or SCC = '01h'.
4	**Ports Implemented Port 4 (PI4)**—R/WO. 0 = The port is not implemented. 1 = The port is implemented. This bit is read-only '0' if MAP.SC = '0' or SCC = '01h'.
3	**Ports Implemented Port 3 (PI3)**—R/WO. 0 = The port is not implemented. 1 = The port is implemented.
2	**Ports Implemented Port 2 (PI2)**—R/WO. 0 = The port is not implemented. 1 = The port is implemented.
1	**Ports Implemented Port 1 (PI1)**—R/WO. 0 = The port is not implemented. 1 = The port is implemented.
0	**Ports Implemented Port 0 (PI0)—**R/WO**.** 0 = The port is not implemented. 1 = The port is implemented.

14.4.1.5 VS—AHCI Version (D31:F2)

Address Offset:	ABAR + 10h–13h	Attribute:	RO
Default Value:	00010300h	Size:	32 bits

This register indicates the major and minor version of the AHCI specification. It is BCD encoded. The upper two bytes represent the major version number, and the lower two bytes represent the minor version number. Example: Version 3.12 would be represented as 00030102h. The current version of the specification is 1.30 (00010300h).

Bit	Description
31:16	**Major Version Number (MJR)**—RO. Indicates the major version is 1
15:0	**Minor Version Number (MNR)**—RO. Indicates the minor version is 30.

14.4.1.6 EM_LOC—Enclosure Management Location Register (D31:F2)

Address Offset:	ABAR + 1Ch–1Fh	Attribute:	RO
Default Value:	01600002h	Size:	32 bits

This register identifies the location and size of the enclosure management message buffer. This register is reserved if enclosure management is not supported (that is, CAP.EMS = 0).

Bit	Description
31:16	**Offset (OFST)**—RO. The offset of the message buffer in Dwords from the beginning of the ABAR.
15:0	**Buffer Size (SZ)**—RO. Specifies the size of the transmit message buffer area in Dwords. The PCH SATA controller only supports transmit buffer. A value of 0 is invalid.

14.4.1.7 EM_CTRL—Enclosure Management Control Register (D31:F2)

Address Offset:	ABAR + 20h–23h	Attribute:	R/W, R/WO, RO
Default Value:	07010000h	Size:	32 bits

This register is used to control and obtain status for the enclosure management interface. This register includes information on the attributes of the implementation, enclosure management messages supported, the status of the interface, whether any message are pending, and is used to initiate sending messages. This register is reserved if enclosure management is not supported (CAP_EMS = 0).

Bit	Description
31:27	Reserved
26	**Activity LED Hardware Driven (ATTR.ALHD)**—R/WO. 1 = The SATA controller drives the activity LED for the LED message type in hardware and does not utilize software for this LED. The host controller does not begin transmitting the hardware based activity signal until after software has written CTL.TM=1 after a reset condition.
25	**Transmit Only (ATTR.XMT)**—RO. 0 = The SATA controller supports transmitting and receiving messages. 1 = The SATA controller only supports transmitting messages and does not support receiving messages.
24	**Single Message Buffer (ATTR.SMB)**—RO. 0 = There are separate receive and transmit buffers such that unsolicited messages could be supported. 1 = The SATA controller has one message buffer that is shared for messages to transmit and messages received. Unsolicited receive messages are not supported and it is software's responsibility to manage access to this buffer.
23:20	Reserved
19	**SGPIO Enclosure Management Messages (SUPP.SGPIO)—**RO. 1 = The SATA controller supports the SGPIO register interface message type.
18	**SES-2 Enclosure Management Messages (SUPP.SES2)—**RO. 1 = The SATA controller supports the SES-2 message type.
17	**SAF-TE Enclosure Management Messages (SUPP.SAFTE)—**RO. 1 = The SATA controller supports the SAF-TE message type.
16	**LED Message Types (SUPP.LED)—**RO. 1 = The SATA controller supports the LED message type.
15:10	Reserved
9	**Reset (RST):—**R/W. 0 = A write of 0 to this bit by software will have no effect. 1 = When set by software, The SATA controller resets all enclosure management message logic and takes all appropriate reset actions to ensure messages can be transmitted / received after the reset. After the SATA controller completes the reset operation, the SATA controller sets the value to 0.
8	**Transmit Message (CTL.TM)—**R/W. 0 = A write of 0 to this bit by software will have no effect. 1 = When set by software, The SATA controller transmits the message contained in the message buffer. When the message is completely sent, the SATA controller sets the value to 0. Software must not change the contents of the message buffer while CTL.TM is set to 1.
7:1	Reserved
0	**Message Received (STS.MR):—**RO. Message Received is not supported in the PCH.

14.4.1.8 CAP2—HBA Capabilities Extended

Address Offset: ABAR + 24h–27h Attribute: RO
Default Value: 00000004h Size: 32 bits
Function Level Reset: No

Bit	Description
31:3	Reserved
2	**Automatic Partial to Slumber Transitions (APST)** 0= Not supported 1= Supported
1	Reserved
0	Reserved

14.4.1.9 VSP—Vendor Specific (D31:F2)

Address Offset: ABAR + A0h–A3h Attribute: RO, R/WO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:1	Reserved
0	**SATA Initialization Field—**R/WO BIOS must clear this bit by writing a 0 to this field.

14.4.1.10 Intel® Rapid Storage Technology enterprise (Intel® RSTe) Feature Capabilities

Address Offset: ABAR + C8h–C9h Attribute: R/WO
Default Value: 003Fh Size: 16 bits
Function Level Reset: No

No hardware action is taken on this register. This register is needed for the Intel® Rapid Storage Technology enterprise software. These bits are set by BIOS to request the feature from the appropriate Intel Rapid Storage Technology enterprise software.

Bit	Description
15:12	Reserved
11:10	**OROM UI Normal Delay (OUD)**—R/WO. The values of these bits specify the delay of the OROM UI Splash Screen in a normal status. 00 = 2 Seconds (Default) 01 = 4 Seconds 10 = 6 Seconds 11 = 8 Seconds If bit 5 = 0b these values will be disregarded.
9	Reserved
8	**Intel® RRT Only on eSATA (ROES)**—R/WO Indicates the request that only Intel® Rapid Recovery Technology (RRT) volumes can can span internal and external SATA (eSATA). If not set, any RAID volume can span internal and external SATA. 0 = Disabled 1 = Enabled
7	**LED Locate (LEDL)**—R/WO Indicates the request that the LED/SGPIO hardware is attached and ping to locate feature is enabled in the operating system. 0 = Disabled 1 = Enabled

Bit	Description
6	**HDD Unlock (HDDLK)**—R/WO Indicates the requested status of HDD password unlock in the operating system. 0 = Disabled 1 = Enabled
5	**Intel RSTe OROM UI (RSTOROMUI)**—R/WO. Indicates the requested status of the Intel® RSTe OROM UI display. 0 = The Intel RSTe OROM UI and banner are not displayed if all disks and RAID volumes have a normal status. 1 = The Intel RSTe OROM UI is displayed during each boot.
4	**Intel RSTe**—R/WO Indicates the requested status of the Intel® Rapid Recovery Technology Support 0 = The Intel RSTe is disabled 1 = The Intel RSTe is enabled
3	**RAID 5 Enable (R5E)**—R/WO Indicates the requested status of RAID 5 Support 0 = Disabled 1 = Enabled
2	**RAID 10 Enable (R10E)**—R/WO Indicates the requested status of RAID 10 Support 0 = Disabled 1 = Enabled
1	**RAID 1 Enable (R1E)**—R/WO Indicates the requested status of RAID 1 Support 0 = Disabled 1 = Enabled
0	**RAID 0 Enable (R0E)**—R/WO Indicates the requested status of RAID 0 Support 0 = Disabled 1 = Enabled

14.4.2 Port Registers (D31:F2)

Ports not available will result in the corresponding Port DMA register space being reserved. The controller shall ignore writes to the reserved space on write cycles and shall return '0' on read cycle accesses to the reserved location.

SSD Functionality of Integrated NAND Module appears as Port 6(7th SATA port)

When the NVMHCI is exposed as a port under AHCI, Port 7 registers will start at ABAR + 480h.

Table 14-5. Port [5:0] DMA Register Address Map (Sheet 1 of 3)

ABAR + Offset	Mnemonic	Register
100h–103h	P0CLB	Port 0 Command List Base Address
104h–107h	P0CLBU	Port 0 Command List Base Address Upper 32-Bits
108h–10Bh	P0FB	Port 0 FIS Base Address
10Ch–10Fh	P0FBU	Port 0 FIS Base Address Upper 32-Bits
110h–113h	P0IS	Port 0 Interrupt Status
114h–117h	P0IE	Port 0 Interrupt Enable
118h–11Bh	P0CMD	Port 0 Command
11Ch–11Fh	—	Reserved
120h–123h	P0TFD	Port 0 Task File Data
124h–127h	P0SIG	Port 0 Signature
128h–12Bh	P0SSTS	Port 0 Serial ATA Status
12Ch–12Fh	P0SCTL	Port 0 Serial ATA Control
130h–133h	P0SERR	Port 0 Serial ATA Error
134h–137h	P0SACT	Port 0 Serial ATA Active
138h–13Bh	P0CI	Port 0 Command Issue
13Ch–17Fh	—	Reserved
180h–183h	P1CLB	Port 1 Command List Base Address
184h–187h	P1CLBU	Port 1 Command List Base Address Upper 32-Bits
188h–18Bh	P1FB	Port 1 FIS Base Address
18Ch–18Fh	P1FBU	Port 1 FIS Base Address Upper 32-Bits
190h–193h	P1IS	Port 1 Interrupt Status
194h–197h	P1IE	Port 1 Interrupt Enable
198h–19Bh	P1CMD	Port 1 Command
19Ch–19Fh	—	Reserved
1A0h–1A3h	P1TFD	Port 1 Task File Data
1A4h–1A7h	P1SIG	Port 1 Signature
1A8h–1ABh	P1SSTS	Port 1 Serial ATA Status
1ACh–1AFh	P1SCTL	Port 1 Serial ATA Control
1B0h–1B3h	P1SERR	Port 1 Serial ATA Error
1B4h–1B7h	P1SACT	Port 1 Serial ATA Active
1B8h–1BBh	P1CI	Port 1 Command Issue
1BCh–1FFh	—	Reserved
200h–203h	P2CLB	Port 2 Command List Base Address
204h–207h	P2CLBU	Port 2 Command List Base Address Upper 32-Bits

Table 14-5. Port [5:0] DMA Register Address Map (Sheet 2 of 3)

ABAR + Offset	Mnemonic	Register
208h–20Bh	P2FB	Port 2 FIS Base Address
20Ch–20Fh	P2FBU	Port 2 FIS Base Address Upper 32-Bits
210h–213h	P2IS	Port 2 Interrupt Status
214h–217h	P2IE	Port 2 Interrupt Enable
218h–21Bh	P2CMD	Port 2 Command
21Ch–21Fh	—	Reserved
220h–223h	P2TFD	Port 2 Task File Data
224h–227h	P2SIG	Port 2 Signature
228h–22Bh	P2SSTS	Port 2 Serial ATA Status
22Ch–22Fh	P2SCTL	Port 2 Serial ATA Control
230h–233h	P2SERR	Port 2 Serial ATA Error
234h–237h	P2SACT	Port 2 Serial ATA Active
238h–23Bh	P2CI	Port 2 Command Issue
23Ch–27Fh	—	Reserved
280h–283h	P3CLB	Port 3 Command List Base Address
284h–287h	P3CLBU	Port 3 Command List Base Address Upper 32-Bits
288h–28Bh	P3FB	Port 3 FIS Base Address
28Ch–28Fh	P3FBU	Port 3 FIS Base Address Upper 32-Bits
290h–293h	P3IS	Port 3 Interrupt Status
294h–297h	P3IE	Port 3 Interrupt Enable
298h–29Bh	P3CMD	Port 3 Command
29Ch–29Fh	—	Reserved
2A0h–2A3h	P3TFD	Port 3 Task File Data
2A4h–2A7h	P3SIG	Port 3 Signature
2A8h–2ABh	P3SSTS	Port 3 Serial ATA Status
2ACh–2AFh	P3SCTL	Port 3 Serial ATA Control
2B0h–2B3h	P3SERR	Port 3 Serial ATA Error
2B4h–2B7h	P3SACT	Port 3 Serial ATA Active
2B8h–2BBh	P3CI	Port 3 Command Issue
2BCh–2FFh	—	Reserved
300h–303h	P4CLB	Port 4 Command List Base Address
304h–307h	P4CLBU	Port 4 Command List Base Address Upper 32-Bits
308h–30Bh	P4FB	Port 4 FIS Base Address
30Ch–30Fh	P4FBU	Port 4 FIS Base Address Upper 32-Bits
310h–313h	P4IS	Port 4 Interrupt Status
314h–317h	P4IE	Port 4 Interrupt Enable
318h–31Bh	P4CMD	Port 4 Command
31Ch–31Fh	—	Reserved
320h–323h	P4TFD	Port 4 Task File Data
324h–327h	P4SIG	Port 4 Signature
328h–32Bh	P4SSTS	Port 4 Serial ATA Status
32Ch–32Fh	P4SCTL	Port 4 Serial ATA Control

Table 14-5. Port [5:0] DMA Register Address Map (Sheet 3 of 3)

ABAR + Offset	Mnemonic	Register
330h–333h	P4SERR	Port 4 Serial ATA Error
334h–337h	P4SACT	Port 4 Serial ATA Active
338h–33Bh	P4CI	Port 4 Command Issue
33Ch–37Fh	—	Reserved
380h–383h	P5CLB	Port 5 Command List Base Address
384h–387h	P5CLBU	Port 5 Command List Base Address Upper 32-Bits
388h–38Bh	P5FB	Port 5 FIS Base Address
38Ch–38Fh	P5FBU	Port 5 FIS Base Address Upper 32-Bits
390h–393h	P5IS	Port 5 Interrupt Status
394h–397h	P5IE	Port 5 Interrupt Enable
398h–39Bh	P5CMD	Port 5 Command
39Ch–39Fh	—	Reserved
3A0h–3A3h	P5TFD	Port 5 Task File Data
3A4h–3A7h	P5SIG	Port 5 Signature
3A8h–3ABh	P5SSTS	Port 5 Serial ATA Status
3ACh–3AFh	P5SCTL	Port 5 Serial ATA Control
3B0h–3B3h	P5SERR	Port 5 Serial ATA Error
3B4h–3B7h	P5SACT	Port 5 Serial ATA Active
3B8h–3BBh	P5CI	Port 5 Command Issue
3BCh–FFFh	—	Reserved

14.4.2.1 PxCLB—Port [5:0] Command List Base Address Register (D31:F2)

Address Offset: Port 0: ABAR + 100h
Port 1: ABAR + 180h
Port 2: ABAR + 200h
Port 3: ABAR + 280h
Port 4: ABAR + 300h
Port 5: ABAR + 380h

Attribute: R/W

Default Value: Undefined

Size: 32 bits

Bit	Description
31:10	**Command List Base Address (CLB)—**R/W**.** Indicates the 32-bit base for the command list for this port. This base is used when fetching commands to execute. The structure pointed to by this address range is 1 KB in length. This address must be 1-KB aligned as indicated by bits 31:10 being read/write. Note that these bits are not reset on a Controller reset.
9:0	Reserved

14.4.2.2 PxCLBU—Port [5:0] Command List Base Address Upper 32-Bits Register (D31:F2)

Address Offset: Port 0: ABAR + 104h
Port 1: ABAR + 184h
Port 2: ABAR + 204h
Port 3: ABAR + 284h
Port 4: ABAR + 304h
Port 5: ABAR + 384h

Attribute: R/W

Default Value: Undefined

Size: 32 bits

Bit	Description
31:0	**Command List Base Address Upper (CLBU)—**R/W**.** Indicates the upper 32-bits for the command list base address for this port. This base is used when fetching commands to execute. Note that these bits are not reset on a Controller reset.

14.4.2.3 PxFB—Port [5:0] FIS Base Address Register (D31:F2)

Address Offset: Port 0: ABAR + 108h
Port 1: ABAR + 188h
Port 2: ABAR + 208h
Port 3: ABAR + 288h
Port 4: ABAR + 308h
Port 5: ABAR + 388h

Attribute: R/W

Default Value: Undefined

Size: 32 bits

Bit	Description
31:8	**FIS Base Address (FB)—**R/W**.** Indicates the 32-bit base for received FISes. The structure pointed to by this address range is 256 bytes in length. This address must be 256-byte aligned, as indicated by bits 31:3 being read/write. Note that these bits are not reset on a Controller reset.
7:0	Reserved

14.4.2.4 PxFBU—Port [5:0] FIS Base Address Upper 32-Bits Register (D31:F2)

Address Offset: Port 0: ABAR + 10Ch
Port 1: ABAR + 18Ch
Port 2: ABAR + 20Ch
Port 3: ABAR + 28Ch
Port 4: ABAR + 30Ch
Port 5: ABAR + 38Ch

Attribute: R/W

Default Value: Undefined

Size: 32 bits

Bit	Description
31:0	**FIS Base Address Upper (FBU)—**R/W**.** Indicates the upper 32-bits for the received FIS base for this port. Note that these bits are not reset on a Controller reset.

14.4.2.5 PxIS—Port [5:0] Interrupt Status Register (D31:F2)

Address Offset:	Port 0: ABAR + 110h Port 1: ABAR + 190h Port 2: ABAR + 210h Port 3: ABAR + 290h Port 4: ABAR + 310h Port 5: ABAR + 390h	Attribute:	R/WC, RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31	**Cold Port Detect Status (CPDS)—**RO**.** Cold presence detect is not supported.
30	**Task File Error Status (TFES)**—R/WC. This bit is set whenever the status register is updated by the device and the error bit (PxTFD.bit 0) is set.
29	**Host Bus Fatal Error Status (HBFS)—**R/WC**.** Indicates that the PCH encountered an error that it cannot recover from due to a bad software pointer. In PCI, such an indication would be a target or master abort.
28	**Host Bus Data Error Status (HBDS)—**R/WC**.** Indicates that the PCH encountered a data error (uncorrectable ECC / parity) when reading from or writing to system memory.
27	**Interface Fatal Error Status (IFS)—**R/WC**.** Indicates that the PCH encountered an error on the SATA interface which caused the transfer to stop.
26	**Interface Non-fatal Error Status (INFS)**—R/WC. Indicates that the PCH encountered an error on the SATA interface but was able to continue operation.
25	Reserved
24	**Overflow Status (OFS)—**R/WC**.** Indicates that the PCH received more bytes from a device than was specified in the PRD table for the command.
23	**Incorrect Port Multiplier Status (IPMS)**—R/WC. The PCH SATA controller does not support Port Multipliers.
22	**PhyRdy Change Status (PRCS)**—RO. When set to '1', this bit indicates the internal PhyRdy signal changed state. This bit reflects the state of PxSERR.DIAG.N. Unlike most of the other bits in the register, this bit is RO and is only cleared when PxSERR.DIAG.N is cleared. Note that the internal PhyRdy signal also transitions when the port interface enters partial or slumber power management states. Partial and slumber must be disabled when Surprise Removal Notification is desired, otherwise the power management state transitions will appear as false insertion and removal events.
21:8	Reserved
7	**Device Interlock Status (DIS)—**R/WC. When set, this bit indicates that a platform interlock switch has been opened or closed, which may lead to a change in the connection state of the device. This bit is only valid in systems that support an interlock switch (CAP.SIS [ABAR+00:bit 28] set). For systems that do not support an interlock switch, this bit will always be 0.
6	**Port Connect Change Status (PCS)—**RO**.** This bit reflects the state of PxSERR.DIAG.X. (ABAR+130h/1D0h/230h/2D0h, bit 26) Unlike other bits in this register, this bit is only cleared when PxSERR.DIAG.X is cleared. 0 = No change in Current Connect Status. 1 = Change in Current Connect Status.
5	**Descriptor Processed (DPS)—**R/WC**.** A PRD with the I bit set has transferred all its data.
4	**Unknown FIS Interrupt (UFS)—**RO. When set to '1', this bit indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to '0' by software clearing the PxSERR.DIAG.F bit to '0'. Note that this bit does not directly reflect the PxSERR.DIAG.F bit. PxSERR.DIAG.F is set immediately when an unknown FIS is detected, whereas this bit is set when the FIS is posted to memory. Software should wait to act on an unknown FIS until this bit is set to '1' or the two bits may become out of sync.
3	**Set Device Bits Interrupt (SDBS)—**R/WC**.** A Set Device Bits FIS has been received with the I bit set and has been copied into system memory.
2	**DMA Setup FIS Interrupt (DSS)—**R/WC**.** A DMA Setup FIS has been received with the I bit set and has been copied into system memory.
1	**PIO Setup FIS Interrupt (PSS)—**R/WC**.** A PIO Setup FIS has been received with the I bit set, it has been copied into system memory, and the data related to that FIS has been transferred.
0	**Device to Host Register FIS Interrupt (DHRS)—**R/WC**.** A D2H Register FIS has been received with the I bit set, and has been copied into system memory.

14.4.2.6 PxIE—Port [5:0] Interrupt Enable Register (D31:F2)

Address Offset:	Port 0: ABAR + 114h Port 1: ABAR + 194h Port 2: ABAR + 214h Port 3: ABAR + 294h Port 4: ABAR + 314h Port 5: ABAR + 394h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

This register enables and disables the reporting of the corresponding interrupt to system software. When a bit is set ('1') and the corresponding interrupt condition is active, then an interrupt is generated. Interrupt sources that are disabled ('0') are still reflected in the status registers.

Bit	Description
31	**Cold Presence Detect Enable (CPDE)—**RO. Cold Presence Detect is not supported.
30	**Task File Error Enable (TFEE)—**R/W. When set, and GHC.IE and PxTFD.STS.ERR (due to a reception of the error register from a received FIS) are set, the PCH will generate an interrupt.
29	**Host Bus Fatal Error Enable (HBFE)—**R/W. When set, and GHC.IE and PxS.HBFS are set, the PCH will generate an interrupt.
28	**Host Bus Data Error Enable (HBDE)—**R/W. When set, and GHC.IE and PxS.HBDS are set, the PCH will generate an interrupt.
27	**Host Bus Data Error Enable (HBDE)**—R/W. When set, GHC.IE is set, and PxIS.HBDS is set, the PCH will generate an interrupt.
26	**Interface Non-fatal Error Enable (INFE)**—R/W. When set, GHC.IE is set, and PxIS.INFS is set, the PCH will generate an interrupt.
25	Reserved
24	**Overflow Error Enable (OFE)—**R/W. When set, and GHC.IE and PxS.OFS are set, the PCH will generate an interrupt.
23	**Incorrect Port Multiplier Enable (IPME)**—R/W. The PCH SATA controller does not support Port Multipliers. BIOS and storage software should keep this bit cleared to 0.
22	**PhyRdy Change Interrupt Enable (PRCE)**—R/W. When set, and GHC.IE is set, and PxIS.PRCS is set, the PCH shall generate an interrupt.
21:8	Reserved
7	**Device Interlock Enable (DIE)—**R/W. When set, and PxIS.DIS is set, the PCH will generate an interrupt. For systems that do not support an interlock switch, this bit shall be a read-only 0.
6	**Port Change Interrupt Enable (PCE)—**R/W. When set, and GHC.IE and PxS.PCS are set, the PCH will generate an interrupt.
5	**Descriptor Processed Interrupt Enable (DPE)—**R/W. When set, and GHC.IE and PxS.DPS are set, the PCH will generate an interrupt
4	**Unknown FIS Interrupt Enable (UFIE)—**R/W. When set, and GHC.IE is set and an unknown FIS is received, the PCH will generate this interrupt.
3	**Set Device Bits FIS Interrupt Enable (SDBE)—**R/W. When set, and GHC.IE and PxS.SDBS are set, the PCH will generate an interrupt.
2	**DMA Setup FIS Interrupt Enable (DSE)—**R/W. When set, and GHC.IE and PxS.DSS are set, the PCH will generate an interrupt.
1	**PIO Setup FIS Interrupt Enable (PSE)—**R/W. When set, and GHC.IE and PxS.PSS are set, the PCH will generate an interrupt.
0	**Device to Host Register FIS Interrupt Enable (DHRE)—**R/W. When set, and GHC.IE and PxS.DHRS are set, the PCH will generate an interrupt.

14.4.2.7 PxCMD—Port [5:0] Command Register (D31:F2)

Address Offset: Port 0: ABAR + 118h
Port 1: ABAR + 198h
Port 2: ABAR + 218h
Port 3: ABAR + 298h
Port 4: ABAR + 318h
Port 5: ABAR + 398h

Attribute: R/W, RO, R/WO

Default Value: 0000w00wh
where w = 00?0b (for?, see bit description)

Size: 32 bits

Function Level Reset:No (Bit 21, 19 and 18 only)

Bit	Description
31:28	**Interface Communication Control (ICC)—**R/W**.** This is a four bit field that can be used to control reset and power states of the interface. Writes to this field will cause actions on the interface, either as primitives or an OOB sequence, and the resulting status of the interface will be reported in the PxSSTS register (Address offset Port 0:ABAR+124h, Port 1: ABAR+1A4h, Port 2: ABAR+224h, Port 3: ABAR+2A4h, Port 4: ABAR+224h, Port 5: ABAR+2A4h). **Value** — **Definition** Fh–7h — Reserved 6h — Slumber: This will cause the PCH to request a transition of the interface to the slumber state. The SATA device may reject the request and the interface will remain in its current state 5h–3h — Reserved 2h — Partial: This will cause the PCH to request a transition of the interface to the partial state. The SATA device may reject the request and the interface will remain in its current state. 1h — Active: This will cause the PCH to request a transition of the interface into the active 0h — No-Op / Idle: When software reads this value, it indicates the PCH is not in the process of changing the interface state or sending a device reset, and a new link command may be issued. When system software writes a non-reserved value other than No-Op (0h), the PCH will perform the action and update this field back to Idle (0h). If software writes to this field to change the state to a state the link is already in (such as interface is in the active state and a request is made to go to the active state), the PCH will take no action and return this field to Idle. ***Note:*** When the ALPE bit (bit 26) is set, then this register should not be set to 02h or 06h.
27	**Aggressive Slumber / Partial (ASP)—**R/W**.** When set, and the ALPE bit (bit 26) is set, the PCH shall aggressively enter the slumber state when it clears the PxCI register and the PxSACT register is cleared. When cleared, and the ALPE bit is set, the PCH will aggressively enter the partial state when it clears the PxCI register and the PxSACT register is cleared. If CAP.SALP is cleared to '0', software shall treat this bit as reserved.
26	**Aggressive Link Power Management Enable (ALPE)—**R/W**.** When set, the PCH will aggressively enter a lower link power state (partial or slumber) based upon the setting of the ASP bit (bit 27).
25	**Drive LED on ATAPI Enable (DLAE)—**R/W**.** When set to 1, the PCH will drive the LED pin active for ATAPI commands (PxCLB[CHz.A] set) in addition to ATA commands. When cleared, the PCH will only drive the LED pin active for ATA commands. See Section 5.17.9 for details on the activity LED.
24	**Device is ATAPI (ATAPI)—**R/W. When set to 1, the connected device is an ATAPI device. This bit is used by the PCH to control whether or not to generate the LED when commands are active. See Section 5.17.9 for details on the activity LED.
23	**Automatic Partial Slumber Transitions Enabled (APSTE)**—R/W. 0 = This port will not perform Automatic Partial to Slumber Transitions. 1 = The HBA may perform Automatic Partial to Slumber Transitions. ***Note:*** Software should only set this bit to '1' if CAP2.APST is set to '1'.

Bit	Description
22	**SATA Initialization Field—**R/WO BIOS must write a 0 to this field. This field is not reset by FLR.
21	**External SATA Port (ESP)—**R/WO. 0 = This port supports internal SATA devices only. 1 = This port will be used with an external SATA device and hot plug is supported. When set, CAP.SXS must also be set. This bit is not reset by Function Level Reset.
20	Reserved
19	**Mechanical Switch Attached to Port (MPSP)**—R/WO. If set to 1, the PCH supports a mechanical presence switch attached to this port. The PCH takes no action on the state of this bit – it is for system software only. For example, if this bit is cleared, and an interlock switch toggles, the PCH still treats it as a proper interlock switch event. ***Note:*** This bit is not reset on a Controller reset or by a Function Level Reset.
18	**Hot-Plug Capable Port (HPCP)**—R/WO. 0 = Port is not capable of Hot-Plug. 1 = Port is Hot-Plug capable. This indicates whether the platform exposes this port to a device which can be Hot-Plugged. SATA by definition is hot-pluggable, but not all platforms are constructed to allow the device to be removed (it may be screwed into the chassis, for example). This bit can be used by system software to indicate a feature such as "eject device" to the end-user. The PCH takes no action on the state of this bit – it is for system software only. For example, if this bit is cleared, and a Hot-Plug event occurs, the PCH still treats it as a proper Hot-Plug event. ***Note:*** This bit is not reset on a Controller reset or by a Function Level Reset.
17:16	Reserved.
15	**Controller Running (CR)—**RO. When this bit is set, the DMA engines for a port are running. See section 5.2.2 of the *Serial ATA AHCI Specification* for details on when this bit is set and cleared by the PCH.
14	**FIS Receive Running (FR)**—RO. When set, the FIS Receive DMA engine for the port is running. See section 12.2.2 of the *Serial ATA AHCI Specification* for details on when this bit is set and cleared by the PCH.
13	**Mechanical Presence Switch State (MPSS)**—RO. The MPSS bit reports the state of a mechanical presence switch attached to this port. If CAP.SMPS is set to 1 and the mechanical presence switch is closed then this bit is cleared to 0. If CAP.SMPS is set to 1 and the mechanical presence switch is open then this bit is set to 1. If CAP.SMPS is set to '0' then this bit is cleared to 0. Software should only use this bit if both CAP.SMPS and PxCMD.MPSP are set to 1.
12:8	**Current Command Slot (CCS)—**RO**.** Indicates the current command slot the PCH is processing. This field is valid when the ST bit is set in this register, and is constantly updated by the PCH. This field can be updated as soon as the PCH recognizes an active command slot, or at some point soon after when it begins processing the command. This field is used by software to determine the current command issue location of the PCH. In queued mode, software shall not use this field, as its value does not represent the current command being executed. Software shall only use PxCI and PxSACT when running queued commands.
7:5	Reserved
4	**FIS Receive Enable (FRE)**—R/W. When set, the PCH may post received FISes into the FIS receive area pointed to by PxFB (ABAR+108h/188h/208h/288h) and PxFBU (ABAR+10Ch/18Ch/20Ch/28Ch). When cleared, received FISes are not accepted by the PCH, except for the first D2H (device-to-host) register FIS after the initialization sequence. System software must not set this bit until PxFB (PxFBU) have been programmed with a valid pointer to the FIS receive area, and if software wishes to move the base, this bit must first be cleared, and software must wait for the FR bit (bit 14) in this register to be cleared.

Bit	Description
3	**Command List Override (CLO)**—R/W. Setting this bit to '1' causes PxTFD.STS.BSY and PxTFD.STS.DRQ to be cleared to '0'. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the PxTFD.STS register. The Controller sets this bit to '0' when PxTFD.STS.BSY and PxTFD.STS.DRQ have been cleared to '0'. A write to this register with a value of '0' shall have no effect. This bit shall only be set to '1' immediately prior to setting the PxCMD.ST bit to '1' from a previous value of '0'. Setting this bit to '1' at any other time is not supported and will result in indeterminate behavior. Software must wait for CLO to be cleared to '0' before setting PxCMD.ST to '1'.
2	**Power On Device (POD)—**RO**.** Cold presence detect not supported. Defaults to 1.
1	**Spin-Up Device (SUD)**—R/W / RO This bit is R/W and defaults to 0 for systems that support staggered spin-up (R/W when CAP.SSS (ABAR+00h:bit 27) is 1). Bit is RO 1 for systems that do not support staggered spin-up (when CAP.SSS is 0). 0 = No action. 1 = On an edge detect from 0 to 1, the PCH starts a COMRESET initialization sequence to the device. Clearing this bit to '0' does not cause any OOB signal to be sent on the interface. When this bit is cleared to '0' and PxSCTL.DET=0h, the Controller will enter listen mode.
0	**Start (ST)—**R/W**.** When set, the PCH may process the command list. When cleared, the PCH may not process the command list. Whenever this bit is changed from a 0 to a 1, the PCH starts processing the command list at entry 0. Whenever this bit is changed from a 1 to a 0, the PxCI register is cleared by the PCH upon the PCH putting the controller into an idle state. Refer to section 10.3 of the Serial ATA AHCI Specification for important restrictions on when ST can be set to 1 and cleared to 0.

14.4.2.8 PxTFD—Port [5:0] Task File Data Register (D31:F2)

Address Offset: Port 0: ABAR + 120h
Port 1: ABAR + 1A0h
Port 2: ABAR + 220h
Port 3: ABAR + 2A0h
Port 4: ABAR + 320h
Port 5: ABAR + 3A0h

Attribute: RO

Default Value: 0000007Fh

Size: 32 bits

This is a 32-bit register that copies specific fields of the task file when FISes are received. The FISes that contain this information are: D2H Register FIS,PIO Setup FIS and Set Device Bits FIS

Bit	Description
31:16	Reserved
15:8	**Error (ERR)—**RO**.** Contains the latest copy of the task file error register.
7:0	**Status (STS)—**RO**.** Contains the latest copy of the task file status register. Fields of note in this register that affect AHCI. **Bit** / **Field** / **Definition** 7 / BSY / Indicates the interface is busy 6:4 / N/A / Not applicable 3 / DRQ / Indicates a data transfer is requested 2:1 / N/A / Not applicable 0 / ERR / Indicates an error during the transfer

14.4.2.9 PxSIG—Port [5:0] Signature Register (D31:F2)

Address Offset:	Port 0: ABAR + 124h Port 1: ABAR + 1A4h Port 2: ABAR + 224h Port 3: ABAR + 2A4h Port 4: ABAR + 324h Port 5: ABAR + 3A4h	Attribute:	RO
Default Value:	FFFFFFFFh	Size:	32 bits

This is a 32-bit register which contains the initial signature of an attached device when the first D2H Register FIS is received from that device. It is updated once after a reset sequence.

Bit	Description
31:0	**Signature (SIG)—**RO**.** Contains the signature received from a device on the first D2H register FIS. The bit order is as follows: **Bit** — **Field** 31:24 — LBA High Register 23:16 — LBA Mid Register 15:8 — LBA Low Register 7:0 — Sector Count Register

14.4.2.10 PxSSTS—Port [5:0] Serial ATA Status Register (D31:F2)

Address Offset: Port 0: ABAR + 128h
Port 1: ABAR + 1A8h
Port 2: ABAR + 228h
Port 3: ABAR + 2A8h
Port 4: ABAR + 328h
Port 5: ABAR + 3A8h

Attribute: RO

Default Value: 00000000h

Size: 32 bits

This is a 32-bit register that conveys the current state of the interface and host. The PCH updates it continuously and asynchronously. When the PCH transmits a COMRESET to the device, this register is updated to its reset values.

Bit	Description
31:12	Reserved
11:8	**Interface Power Management (IPM)—**RO**.** Indicates the current interface state: **Value** — **Description** 0h — Device not present or communication not established 1h — Interface in active state 2h — Interface in PARTIAL power management state 6h — Interface in SLUMBER power management state All other values reserved.
7:4	**Current Interface Speed (SPD)**—RO. Indicates the negotiated interface communication speed. **Value** — **Description** 0h — Device not present or communication not establisl 1h — Generation 1 communication rate negotiated 2h — Generation 2 communication rate negotiated All other values reserved. The PCH Supports Gen 1 communication rates (1.5 Gb/s) and Gen 2 rates (3.0 Gb/s).
3:0	**Device Detection (DET)—**RO**.** Indicates the interface device detection and Phy state: **Value** — **Description** 0h — No device detected and Phy communication not established 1h — Device presence detected but Phy communication not established 3h — Device presence detected and Phy communication established 4h — Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode All other values reserved.

14.4.2.11 PxSCTL—Port [5:0] Serial ATA Control Register (D31:F2)

Address Offset:	Port 0: ABAR + 12Ch Port 1: ABAR + 1ACh Port 2: ABAR + 22Ch Port 3: ABAR + 2ACh Port 4: ABAR + 32Ch Port 5: ABAR + 3ACh	Attribute:	R/W, RO
Default Value:	00000004h	Size:	32 bits

This is a 32-bit read-write register by which software controls SATA capabilities. Writes to the SControl register result in an action being taken by the PCH or the interface. Reads from the register return the last value written to it.

Bit	Description
31:20	Reserved
19:16	**Port Multiplier Port (PMP)**—R/W. This field is not used by AHCI
15:12	Select Power Management (SPM)—R/W. This field is not used by AHCI
11:8	**Interface Power Management Transitions Allowed (IPM)—**R/W**.** Indicates which power states the PCH is allowed to transition to: **Value** — **Description** 0h — No interface restrictions 1h — Transitions to the PARTIAL state disabled 2h — Transitions to the SLUMBER state disabled 3h — Transitions to both PARTIAL and SLUMBER states disabled All other values reserved
7:4	**Speed Allowed (SPD)**—R/W. Indicates the highest allowable speed of the interface. This speed is limited by the CAP.ISS (ABAR+00h:bit 23:20) field. **Value** — **Description** 0h — No speed negotiation restrictions 1h — Limit speed negotiation to Generation 1 communication rate 2h — Limit speed negotiation to Generation 2 communication rate 3h — Limit speed negotiation to Generation 3 communication rate (Port 0 and Port 1 only) The PCH Supports Gen 1 communication rates (1.5 Gb/s) and Gen 2 rates (3.0 Gb/s) and Gen 3 rates (6 Gb/s).
3:0	**Device Detection Initialization (DET)—**R/W. Controls the PCH's device detection and interface initialization. **Value** — **Description** 0h — No device detection or initialization action requested 1h — Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications re-initialized 4h — Disable the Serial ATA interface and put Phy in offline mode All other values reserved. When this field is written to a 1h, the PCH initiates COMRESET and starts the initialization process. When the initialization is complete, this field shall remain 1h until set to another value by software. This field may only be changed to 1h or 4h when PxCMD.ST is 0. Changing this field while the PCH is running results in undefined behavior. ***Note:*** It is permissible to implement any of the Serial ATA defined behaviors for transmission of COMRESET when DET=1h.

14.4.2.12 PxSERR—Port [5:0] Serial ATA Error Register (D31:F2)

Address Offset:	Port 0: ABAR + 130h Port 1: ABAR + 1B0h Port 2: ABAR + 230h Port 3: ABAR + 2B0h Port 4: ABAR + 330h Port 5: ABAR + 3B0h	Attribute:	R/WC
Default Value:	00000000h	Size:	32 bits

Bits 26:16 of this register contain diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes. Bits 11:0 contain error information used by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer.

Bit	Description
31:27	Reserved
26	**Exchanged (X)—**R/WC. When set to '1' this bit indicates that a change in device presence has been detected since the last time this bit was cleared. This bit shall always be set to 1 anytime a COMINIT signal is received. This bit is reflected in the P0IS.PCS bit.
25	**Unrecognized FIS Type (F)—**R/WC. Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized.
24	**Transport state transition error (T)—**R/WC. Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared.
23	**Link Sequence Error (S)**: Indicates that one or more Link state machine error conditions was encountered. The Link Layer state machine defines the conditions under which the link layer detects an erroneous transition.
22	**Handshake (H)—**R/WC. Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.
21	**CRC Error (C)—**R/WC. Indicates that one or more CRC errors occurred with the Link Layer.
20	**Disparity Error (D)—**R/WC. This field is not used by AHCI.
19	**10b to 8b Decode Error (B)—**R/WC. Indicates that one or more 10b to 8b decoding errors occurred.
18	**Comm Wake (W)—**R/WC. Indicates that a Comm Wake signal was detected by the Phy.
17	**Phy Internal Error (I)—**R/WC. Indicates that the Phy detected some internal error.
16	**PhyRdy Change (N)—**R/WC. When set to 1 this bit indicates that the internal PhyRdy signal changed state since the last time this bit was cleared. In the PCH, this bit will be set when PhyRdy changes from a 0 -> 1 or a 1 -> 0. The state of this bit is then reflected in the PxIS.PRCS interrupt status bit and an interrupt will be generated if enabled. Software clears this bit by writing a 1 to it.
15:12	Reserved
11	**Internal Error (E)—**R/WC. The SATA controller failed due to a master or target abort when attempting to access system memory.
10	**Protocol Error (P)—**R/WC. A violation of the Serial ATA protocol was detected. ***Note:*** The PCH does not set this bit for all protocol violations that may occur on the SATA link.
9	**Persistent Communication or Data Integrity Error (C)—**R/WC. A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes.
8	**Transient Data Integrity Error (T)—**R/WC. A data integrity error occurred that was not recovered by the interface.

Bit	Description
7:2	Reserved.
1	**Recovered Communications Error (M)—**R/WC. Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers.
0	**Recovered Data Integrity Error (I)—**R/WC. A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.

14.4.2.13 PxSACT—Port [5:0] Serial ATA Active (D31:F2)

Address Offset: Port 0: ABAR + 134h
Port 1: ABAR + 1B4h
Port 2: ABAR + 234h
Port 3: ABAR + 2B4h
Port 4: ABAR + 334h
Port 5: ABAR + 3B4h

Attribute: R/W

Default Value: 00000000h

Size: 32 bits

Bit	Description
31:0	**Device Status (DS)—**R/W. System software sets this bit for SATA queuing operations prior to setting the PxCI.CI bit in the same command slot entry. This field is cleared using the Set Device Bits FIS. This field is also cleared when PxCMD.ST (ABAR+118h/198h/218h/298h:bit 0) is cleared by software, and as a result of a COMRESET or SRST.

14.4.2.14 PxCI—Port [5:0] Command Issue Register (D31:F2)

Address Offset: Port 0: ABAR + 138h
Port 1: ABAR + 1B8h
Port 2: ABAR + 238h
Port 3: ABAR + 2B8h
Port 4: ABAR + 338h
Port 5: ABAR + 3B8h

Attribute: R/W

Default Value: 00000000h

Size: 32 bits

Bit	Description
31:0	**Commands Issued (CI)—**R/W. This field is set by software to indicate to the PCH that a command has been built-in system memory for a command slot and may be sent to the device. When the PCH receives a FIS which clears the BSY and DRQ bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field shall only be set to '1' by software when PxCMD.ST is set to '1'. This field is also cleared when PxCMD.ST (ABAR+118h/198h/218h/298h:bit 0) is cleared by software.

Bit	Description
31:0	**Command List Base Address Upper (CLBU)—**R/W**.** Indicates the upper 32-bits for the command list base address for this port. This base is used when fetching commands to execute. Note that these bits are not reset on a Controller reset.

§

15 SATA Controller Registers (D31:F5)

15.1 PCI Configuration Registers (SATA–D31:F5)

Note: Address locations that are not shown should be treated as Reserved.

Note: All of the SATA registers are in the core well. None of the registers can be locked.

Table 15-1. SATA Controller PCI Register Address Map (SATA–D31:F5) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	02B0h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	See register description	See register description
0Ah	SCC	Sub Class Code	See register description	See register description
0Bh	BCC	Base Class Code	01h	RO
0Dh	PMLT	Primary Master Latency Timer	00h	RO
10h–13h	PCMD_BAR	Primary Command Block Base Address	00000001h	R/W, RO
14h–17h	PCNL_BAR	Primary Control Block Base Address	00000001h	R/W, RO
18h–1Bh	SCMD_BAR	Secondary Command Block Base Address	00000001h	R/W, RO
1Ch–1Fh	SCNL_BAR	Secondary Control Block Base Address	00000001h	R/W, RO
20h–23h	BAR	Legacy Bus Master Base Address	00000001h	R/W, RO
24h–27h	SIDPBA	Serial ATA Index / Data Pair Base Address	00000000h	See register description
2Ch–2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2Eh–2Fh	SID	Subsystem Identification	0000h	R/WO
34h	CAP	Capabilities Pointer	80h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	See register description	RO
40h–41h	IDE_TIM	Primary IDE Timing Register	0000h	R/W
48h	SDMA_CNT	Synchronous DMA Control	00h	R/W
4Ah–4Bh	SDMA_TIM	Synchronous DMA Timing	0000h	R/W
54h–57h	IDE_CONFIG	IDE I/O Configuration	00000000h	R/W
70h–71h	PID	PCI Power Management Capability ID	See register description	RO
72h–73h	PC	PCI Power Management Capabilities	4003h	RO
74h–75h	PMCS	PCI Power Management Control and Status	0008h	R/W, RO, R/WC

Table 15-1. SATA Controller PCI Register Address Map (SATA–D31:F5) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Type
90h	MAP	Address Map	00h	R/W
92h–93h	PCS	Port Control and Status	0000h	R/W, RO, R/WC
A8h–ABh	SATACAP0	SATA Capability Register 0	0010B012h	RO
ACh–AFh	SATACAP1	SATA Capability Register 1	00000048h	RO
B0h–B1h	FLRCID	FLR Capability ID	0009h	RO
B2h–B3h	FLRCLV	FLR Capability Length and Value	2006h	RO
B4h–B5h	FLRCTRL	FLR Control	0000h	R/W, RO
C0h	ATC	APM Trapping Control	00h	R/W
C4h	ATS	ATM Trapping Status	00h	R/WC

Note: The PCH SATA controller is not arbitrated as a PCI device; therefore, it does not need a master latency timer.

15.1.1 VID—Vendor Identification Register (SATA—D31:F5)

Offset Address:	00h–01h	Attribute:	RO
Default Value:	8086h	Size:	16 bit
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Vendor ID**—RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

15.1.2 DID—Device Identification Register (SATA—D31:F5)

Offset Address:	02h–03h	Attribute:	RO
Default Value:	See bit description	Size:	16 bit
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Device ID**—RO. This is a 16-bit value assigned to the PCH SATA controller. ***Note:*** The value of this field will change dependent upon the value of the MAP Register. See Section 15.1.28.

15.1.3 PCICMD—PCI Command Register (SATA–D31:F5)

Address Offset:	04h–05h	Attribute:	RO, R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable**—R/W. This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt and MSI is not enabled. 1 = Internal INTx# messages will not be generated.
9	Fast Back to Back Enable (FBE)—RO. Reserved as '0'.
8	SERR# Enable (SERR_EN)—RO. Reserved as '0'.
7	Wait Cycle Control (WCC)—RO. Reserved as '0'.
6	**Parity Error Response (PER)—**R/W. 0 = Disabled. SATA controller will not generate PERR# when a data parity error is detected. 1 = Enabled. SATA controller will generate PERR# when a data parity error is detected.
5	VGA Palette Snoop (VPS)—RO. Reserved as '0'.
4	Postable Memory Write Enable (PMWE)—RO. Reserved as '0'.
3	Special Cycle Enable (SCE)—RO. Reserved as '0'.
2	**Bus Master Enable (BME)—**R/W. This bit controls the PCH ability to act as a PCI master for IDE Bus Master transfers. This bit does not impact the generation of completions for split transaction commands.
1	**Memory Space Enable (MSE)—**RO. This controller does not support AHCI; therefore, no memory space is required.
0	**I/O Space Enable (IOSE)—**R/W. This bit controls access to the I/O space registers. 0 = Disables access to the Legacy or Native IDE ports (both Primary and Secondary) as well as the Bus Master I/O registers. 1 = Enable. Note that the Base Address register for the Bus Master registers should be programmed before this bit is set.

15.1.4 PCISTS—PCI Status Register (SATA–D31:F5)

Address Offset:	06h–07h	Attribute:	R/WC, RO
Default Value:	02B0h	Size:	16 bits

Note: For the writable bits, software must write a '1' to clear bits that are set. Writing a '0' to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)**—R/WC. 0 = No parity error detected by SATA controller. 1 = SATA controller detects a parity error on its interface.
14	**Signaled System Error (SSE)**—RO. Reserved as '0'.
13	**Received Master Abort (RMA)—**R/WC. 0 = Master abort Not generated. 1 = SATA controller, as a master, generated a master abort.
12	Reserved
11	**Signaled Target Abort (STA)**—RO. Reserved as '0'.
10:9	**DEVSEL# Timing Status (DEV_STS)**—RO. 01 = Hardwired; Controls the device select time for the SATA controller's PCI interface.
8	**Data Parity Error Detected (DPED)—**R/WC. For PCH, this bit can only be set on read completions received from SiBUS where there is a parity error. 1 = SATA controller, as a master, either detects a parity error or sees the parity error line asserted, and the parity error response bit (bit 6 of the command register) is set.
7	**Fast Back to Back Capable (FB2BC)**—RO. Reserved as '1'.
6	**User Definable Features (UDF)—**RO. Reserved as '0'.
5	**66 MHz Capable (66 MHZ_CAP)—**RO. Reserved as '1'.
4	**Capabilities List (CAP_LIST)—**RO. This bit indicates the presence of a capabilities list. The minimum requirement for the capabilities list must be PCI power management for the SATA controller.
3	**Interrupt Status (INTS)**—RO. Reflects the state of INTx# messages, IRQ14 or IRQ15. 0 = Interrupt is cleared (independent of the state of Interrupt Disable bit in the command register [offset 04h]). 1 = Interrupt is to be asserted
2:0	Reserved

15.1.5 RID—Revision Identification Register (SATA—D31:F5)

Offset Address:	08h	Attribute:	RO
Default Value:	See bit description	Size:	8 bits

Bit	Description
7:0	**Revision ID**—RO. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Revision ID Register.

15.1.6 PI—Programming Interface Register (SATA–D31:F5)

Address Offset:	09h	Attribute:	RO
Default Value:	85h	Size:	8 bits

When SCC = 01h

Bit	Description
7	This read-only bit is a '1' to indicate that the PCH supports bus master operation
6:4	Reserved.
3	**Secondary Mode Native Capable (SNC)**—RO. Indicates whether or not the secondary channel has a fixed mode of operation. 0 = Indicates the mode is fixed and is determined by the (read-only) value of bit 2. This bit will always return '0'.
2	**Secondary Mode Native Enable (SNE)**—RO. Determines the mode that the secondary channel is operating in. 1 = Secondary controller operating in native PCI mode. This bit will always return '1'.
1	**Primary Mode Native Capable (PNC)—**RO. Indicates whether or not the primary channel has a fixed mode of operation. 0 = Indicates the mode is fixed and is determined by the (read-only) value of bit '0'. This bit will always return '0'.
0	**Primary Mode Native Enable (PNE)**—RO. Determines the mode that the primary channel is operating in. 1 = Primary controller operating in native PCI mode. This bit will always return '1'.

15.1.7 SCC—Sub Class Code Register (SATA–D31:F5)

Address Offset:	0Ah	Attribute:	RO
Default Value:	01h	Size:	8 bits

Bit	Description
7:0	**Sub Class Code (SCC)—**RO. The value of this field determines whether the controller supports legacy IDE mode.

15.1.8 BCC—Base Class Code Register (SATA–D31:F5SATA–D31:F5)

Address Offset: 0Bh Attribute: RO
Default Value: 01h Size: 8 bits

Bit	Description
7:0	**Base Class Code (BCC)**—RO. 01h = Mass storage device

15.1.9 PMLT—Primary Master Latency Timer Register (SATA–D31:F5)

Address Offset: 0Dh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Master Latency Timer Count (MLTC)**—RO. 00h = Hardwired. The SATA controller is implemented internally, and is not arbitrated as a PCI device, so it does not need a Master Latency Timer.

15.1.10 PCMD_BAR—Primary Command Block Base Address Register (SATA–D31:F5)

Address Offset: 10h–13h Attribute: R/W, RO
Default Value: 00000001h Size: 32 bits

Bit	Description
31:16	Reserved
15:3	**Base Address—**R/W. This field provides the base address of the I/O space (8 consecutive I/O locations).
2:1	Reserved
0	**Resource Type Indicator (RTE)—**RO. Hardwired to '1' to indicate a request for I/O space.

Note: This 8-byte I/O space is used in native mode for the Primary Controller's Command Block.

15.1.11 PCNL_BAR—Primary Control Block Base Address Register (SATA–D31:F5)

Address Offset: 14h–17h Attribute: R/W, RO
Default Value: 00000001h Size: 32 bits

Bit	Description
31:16	Reserved
15:2	**Base Address—**R/W. This field provides the base address of the I/O space (4 consecutive I/O locations).
1	Reserved
0	**Resource Type Indicator (RTE)—**RO. Hardwired to '1' to indicate a request for I/O space.

Note: This 4-byte I/O space is used in native mode for the Primary Controller's Command Block.

15.1.12 SCMD_BAR—Secondary Command Block Base Address Register (IDE D31:F1)

Address Offset:	18h–1Bh	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

Bit	Description
31:16	Reserved
15:3	**Base Address—**R/W. This field provides the base address of the I/O space (8 consecutive I/O locations).
2:1	Reserved
0	**Resource Type Indicator (RTE)**—RO. Hardwired to '1' to indicate a request for I/O space.

Note: This 8-byte I/O space is used in native mode for the Secondary Controller's Command Block.

15.1.13 SCNL_BAR—Secondary Control Block Base Address Register (IDE D31:F1)

Address Offset:	1Ch–1Fh	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

Bit	Description
31:16	Reserved
15:2	**Base Address—**R/W. This field provides the base address of the I/O space (4 consecutive I/O locations).
1	Reserved
0	**Resource Type Indicator (RTE)**—RO. Hardwired to '1' to indicate a request for I/O space.

Note: This 4-byte I/O space is used in native mode for the Secondary Controller's Command Block.

15.1.14 BAR—Legacy Bus Master Base Address Register (SATA–D31:F5)

Address Offset:	20h–23h	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits

The Bus Master IDE interface function uses Base Address register 5 to request a 16-byte I/O space to provide a software interface to the Bus Master functions. Only 12 bytes are actually used (6 bytes for primary, 6 bytes for secondary). Only bits [15:4] are used to decode the address.

Bit	Description
31:16	Reserved
15:5	**Base Address—**R/W. This field provides the base address of the I/O space (16 consecutive I/O locations).
4	**Base Address 4 (BA4)**—R/W. When SCC is 01h, this bit will be R/W resulting in requesting 16B of I/O space.
3:1	Reserved
0	**Resource Type Indicator (RTE)—**RO. Hardwired to 1 to indicate a request for I/O space.

15.1.15 SIDPBA—SATA Index/Data Pair Base Address Register (SATA–D31:F5)

Address Offset:	24h–27h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

When SCC is 01h

When the programming interface is IDE, the register represents an I/O BAR allocating 16B of I/O space for the I/O mapped registers defined in Section 15.3. Note that although 16B of locations are allocated, some maybe reserved.

Bit	Description
31:16	Reserved
15:4	**Base Address (BA)—**R/W. Base address of register I/O space
3:1	Reserved
0	**Resource Type Indicator (RTE)—**RO. Hardwired to 1 to indicate a request for I/O space.

15.1.16 SVID—Subsystem Vendor Identification Register (SATA–D31:F5)

Address Offset:	2Ch–2Dh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core
Function Level Reset: No			

Bit	Description
15:0	**Subsystem Vendor ID (SVID)—**R/WO. Value is written by BIOS. No hardware action taken on this value.

15.1.17 SID—Subsystem Identification Register (SATA–D31:F5)

Address Offset:	2Eh–2Fh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Subsystem ID (SID)**—R/WO. Value is written by BIOS. No hardware action taken on this value.

15.1.18 CAP—Capabilities Pointer Register (SATA–D31:F5)

Address Offset:	34h	Attribute:	RO
Default Value:	70h	Size:	8 bits

Bit	Description
7:0	**Capabilities Pointer (CAP_PTR)**—RO. Indicates that the first capability pointer offset is 70h if the Sub Class Code (SCC) (Dev 31:F2:0Ah) is configure as IDE mode (value of 01).

15.1.19 INT_LN—Interrupt Line Register (SATA–D31:F5)

Address Offset: 3Ch
Attribute: R/W
Default Value: 00h
Size: 8 bits
Function Level Reset: No

Bit	Description
7:0	**Interrupt Line—**R/W. This field is used to communicate to software the interrupt line that the interrupt pin is connected to. These bits are not reset by FLR.

15.1.20 INT_PN—Interrupt Pin Register (SATA–D31:F5)

Address Offset: 3Dh
Attribute: RO
Default Value: See Register Description
Size: 8 bits

Bit	Description
7:0	**Interrupt Pin—**RO. This reflects the value of D31IP.SIP1 (Chipset Config Registers:Offset 3100h:bits 11:8).

15.1.21 IDE_TIM—IDE Timing Register (SATA–D31:F5)

Address Offset: Primary: 40h–41h
Secondary: 42h–43h
Attribute: R/W
Default Value: 0000h
Size: 16 bits

Bits 14:12 and 9:0 of this register are R/W to maintain software compatibility. These bits have no effect on hardware.

Bit	Description
15	**IDE Decode Enable (IDE)—**R/W. Individually enable/disable the Primary or Secondary decode. 0 = Disable. 1 = Enables the PCH to decode the associated Command Blocks (1F0–1F7h for primary, 170–177h for secondary) and Control Block (3F6h for primary and 376h for secondary). This bit effects the IDE decode ranges for both legacy and native-Mode decoding. ***Note:*** This bit affects SATA operation in both combined and non-combined ATA modes. See Section 5.17 for more on ATA modes of operation.
14:12	**IDE_TIM Field 2** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
11:10	Reserved
9:0	**IDE_TIM Field 1** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.

15.1.22 SDMA_CNT—Synchronous DMA Control Register (SATA–D31:F5)

Address Offset: 48h
Attribute: R/W
Default Value: 00h
Size: 8 bits

Bits	Description
7:4	Reserved
3:0	**SDMA_CNT Field 1** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.

15.1.23 SDMA_TIM—Synchronous DMA Timing Register (SATA–D31:F5)

Address Offset: 4Ah–4Bh Attribute: R/W
Default Value: 0000h Size: 16 bits

Bits	Description
15:10	Reserved
9:8	**SDMA_TIM Field 2**— R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
7:2	Reserved
1:0	**SDMA_TIM Field 1** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.

15.1.24 IDE_CONFIG—IDE I/O Configuration Register (SATA–D31:F5)

Address Offset: 54h–57h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bits	Description
31:24	Reserved
23:16	**IDE_CONFIG Field 6** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
15	Reserved
14	**IDE_CONFIG Field 5** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
13	Reserved
12	**IDE_CONFIG Field 4** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
11:8	Reserved
7:4	**IDE_CONFIG Field 3** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
3	Reserved
2	**IDE_CONFIG Field 2** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.
1	Reserved
0	**IDE_CONFIG Field 1** — R/W. This field is R/W to maintain software compatibility. This field has no effect on hardware.

15.1.25 PID—PCI Power Management Capability Identification Register (SATA–D31:F5)

Address Offset: 70h–71h Attribute: RO
Default Value: B001h Size: 16 bits

Bits	Description
15:8	**Next Capability (NEXT)**—RO. When SCC is 01h, this field will be B0h indicating the next item is FLR Capability Pointer in the list.
7:0	**Capability ID (CID)**—RO. Indicates that this pointer is a PCI power management.

15.1.26 PC—PCI Power Management Capabilities Register (SATA–D31:F5)

Address Offset: 72h–73h Attribute: RO
Default Value: 4003h Size: 16 bits

Bits	Description
15:11	**PME Support (PME_SUP)**—RO. By default with SCC = 01h, the default value of '00000' indicates no PME support in IDE mode.
10	D2 Support (D2_SUP)—RO. Hardwired to '0'. The D2 state is not supported
9	D1 Support (D1_SUP)—RO. Hardwired to '0'. The D1 state is not supported
8:6	Auxiliary Current (AUX_CUR)—RO. PME# from $D3_{COLD}$ state is not supported, therefore this field is 000b.
5	Device Specific Initialization (DSI)—RO. Hardwired to '0' to indicate that no device-specific initialization is required.
4	Reserved
3	PME Clock (PME_CLK)—RO. Hardwired to '0' to indicate that PCI clock is not required to generate PME#.
2:0	**Version (VER)—**RO. Hardwired to '011' to indicates support for Revision 1.2 of the PCI Power Management Specification.

15.1.27 PMCS—PCI Power Management Control and Status Register (SATA–D31:F5)

Address Offset: 74h–75h Attribute: RO, R/W, R/WC
Default Value: 0008h Size: 16 bits
Function Level Reset:No (Bits 8 and 15 only)

Bits	Description
15	**PME Status (PMES)**—R/WC. Bit is set when a PME event is to be requested, and if this bit and PMEE is set, a PME# will be generated from the SATA controller. ***Note:*** When SCC=01h this bit will be RO '0'. Software is advised to clear PMEE together with PMES prior to changing SCC through MAP.SMS. This bit is not reset by Function Level Reset.
14:9	Reserved
8	**PME Enable (PMEE)**—R/W. When SCC is not 01h, this bit R/W. When set, the SATA controller generates PME# form $D3_{HOT}$ on a wake event. ***Note:*** When SCC=01h this bit will be RO '0'. Software is advised to clear PMEE together with PMES prior to changing SCC through MAP.SMS. This bit is not reset by Function Level Reset.
7:4	Reserved
3	**No Soft Reset (NSFRST)**—RO. These bits are used to indicate whether devices transitioning from $D3_{HOT}$ state to D0 state will perform an internal reset. 0 = Device transitioning from $D3_{HOT}$ state to D0 state perform an internal reset. 1 = Device transitioning from $D3_{HOT}$ state to D0 state do not perform an internal reset. Configuration content is preserved. Upon transition from the $D3_{HOT}$ state to D0 state initialized state, no additional operating system intervention is required to preserve configuration context beyond writing to the PowerState bits. Regardless of this bit, the controller transition from $D3_{HOT}$ state to D0 state by a system or bus segment reset will return to the state D0 uninitialized with only PME context preserved if PME is supported and enabled.
2	Reserved
1:0	**Power State (PS)**—R/W. These bits are used both to determine the current power state of the SATA controller and to set a new power state. 00 = D0 state 11 = $D3_{HOT}$ state When in the $D3_{HOT}$ state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked.

15.1.28 MAP—Address Map Register (SATA–D31:F5)16

Address Offset: 90h
Default Value: 00h
Function Level Reset: No (Bits 9:8 only)
Attribute: R/W, R/WO, RO
Size: bits

Bits	Description
15:10	Reserved.
9:8	Reserved
7:6	**SATA Mode Select (SMS)—**R/W. Software programs these bits to control the mode in which the SATA Controller should operate. 00b = IDE Mode All other combinations are reserved.
5:2	Reserved.
1:0	**Map Value (MV)**—Reserved.

15.1.29 PCS—Port Control and Status Register (SATA–D31:F5)

Address Offset: 92h–93h
Default Value: 0000h
Function Level Reset: No
Attribute: R/W, RO
Size: 16 bits

By default, the SATA ports are set to the disabled state (bits [5:0] = '0'). When enabled by software, the ports can transition between the on, partial, and slumber states and can detect devices. When disabled, the port is in the "off" state and cannot detect any devices.

If an AHCI-aware or RAID enabled operating system is being booted then system BIOS shall insure that all supported SATA ports are enabled prior to passing control to the operating system. Once the AHCI aware operating system is booted it becomes the enabling/disabling policy owner for the individual SATA ports. This is accomplished by manipulating a port's PxSCTL and PxCMD fields. Because an AHCI or RAID aware operating system will typically not have knowledge of the PxE bits and because the PxE bits act as master on/off switches for the ports, pre-boot software must insure that these bits are set to '1' prior to booting the operating system, regardless as to whether or not a device is currently on the port.

Bits	Description
15:10	Reserved
9	**Port 5 Present (P5P)—**RO. The status of this bit may change at any time. This bit is cleared when the port is disabled using P1E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 1 has been detected.
8	**Port 4 Present (P4P)—**RO. The status of this bit may change at any time. This bit is cleared when the port is disabled using P0E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 0 has been detected.
7:2	Reserved
1	**Port 5 Enabled (P5E)**—R/W. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. This bit is read-only '0' when MAP.SPD[1]= 1.
0	**Port 4 Enabled (P4E)**—R/W. 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. This bit is read-only '0' when MAP.SPD[0]= 1.

15.1.30 SATACR0—SATA Capability Register 0 (SATA–D31:F5)

Address Offset: A8h–ABh Attribute: RO, R/WO
Default Value: 0010B012h Size: 32 bits
Function Level Reset: No (Bits 15:8 only)

Note: When SCC is 01h this register is read-only 0.

Bit	Description
31:24	Reserved.
23:20	**Major Revision (MAJREV)—**RO. Major revision number of the SATA Capability Pointer implemented.
19:16	**Minor Revision (MINREV)—**RO. Minor revision number of the SATA Capability Pointer implemented.
15:8	**Next Capability Pointer (NEXT)—**R/WO. Points to the next capability structure.
7:0	**Capability ID (CAP)—**RO. The value of 12h has been assigned by the PCI SIG to designate the SATA capability pointer.

15.1.31 SATACR1—SATA Capability Register 1 (SATA–D31:F5)

Address Offset: ACh–AFh Attribute: RO
Default Value: 00000048h Size: 32 bits

When SCC is 01h this register is read-only 0.

Bit	Description
31:16	Reserved.
15:4	**BAR Offset (BAROFST)—**RO. Indicates the offset into the BAR where the index/Data pair are located (in DWord granularity). The index and Data I/O registers are located at offset 10h within the I/O space defined by LBAR (BAR4). A value of 004h indicates offset 10h.
3:0	**BAR Location (BARLOC)—**RO. Indicates the absolute PCI Configuration Register address of the BAR containing the Index/Data pair (in DWord granularity). The Index and Data I/O registers reside within the space defined by LBAR (BAR4) in the SATA controller. a value of 8h indicates and offset of 20h, which is LBAR (BAR4).

15.1.32 FLRCID—FLR Capability ID (SATA–D31:F5)

Address Offset: B0h–B1h Attribute: RO
Default Value: 0009h Size: 16 bits

Bit	Description
15:8	**Next Capability Pointer—**RO. A value of 00h indicates the final item in the Capability List.
7:0	**Capability ID—**RO. The value of this field depends on the FLRCSSECL bit. If FLRCSSEL = 0, this field is 13h If FLRCSSEL = 1, this field is 09h, indicating vendor specific capability.

15.1.33 FLRCLV—FLR Capability Length and Value (SATA–D31:F5)

Address Offset:	B2h–B3h	Attribute:	RO, R/WO
Default Value:	2006h	Size:	16 bits
Function Level Reset:	No (Bits 9:8 only)		

When FLRCSSEL = '0' , this register is defined as follows.

Bit	Description
15:10	Reserved.
9	**FLR Capability**—R/WO. This field indicates support for Function Level Reset.
8	**TXP Capability**—R/WO. This field indicates support for the Transactions Pending (TXP) bit. TXP must be supported if FLR is supported.
7:0	**Capability Length**—RO. This field indicates the number of bytes of the Vendor Specific capability as required by the PCI specification. It has the value of 06h for FLR Capability.

When FLRCSSEL = '1' , this register is defined as follows.

Bit	Description
15:12	**Vendor Specific Capability ID**—RO. A value of 02h identifies this capability as a Function Level Reset.
11:8	**Capability Version**—RO. This field indicates the version of the FLR capability.
7:0	**Capability Length**—RO. This field indicates the number of bytes of the Vendor Specific capability as required by the PCI specification. It has the value of 06h for FLR Capability.

15.1.34 FLRCTRL—FLR Control (SATA–D31:F5)

Address Offset:	B4h–B5h	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:9	Reserved.
8	**Transactions Pending (TXP)**—RO. 0 = Completions for all Non-Posted requests have been received by the controller. 1 = Controller has issued Non-Posted request which has not been completed.
7:1	Reserved.
0	**Initiate FLR**—R/W. Used to initiate FLR transition. A write of '1' indicates FLR transition.

15.1.35 ATC—APM Trapping Control Register (SATA–D31:F5)

Address Offset:	C0h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Note: This SATA controller does not support legacy I/O access. Therefore, this register is reserved. Software shall not change the default values of the register; otherwise, the result will be undefined.

Bit	Description
7:0	Reserved

15.1.36 ATC—APM Trapping Control (SATA–D31:F5)

Address Offset:	C4h	Attribute:	R/WC
Default Value:	00h	Size:	8 bits

Note: This SATA controller does not support legacy I/O access. Therefore, this register is reserved. Software shall not change the default values of the register; otherwise, the result will be undefined.

Bit	Description
7:0	Reserved

15.2 Bus Master IDE I/O Registers (D31:F5)

The bus master IDE function uses 16 bytes of I/O space, allocated using the BAR register, located in Device 31:Function 2 Configuration space, offset 20h. All bus master IDE I/O space registers can be accessed as byte, word, or DWord quantities. Reading reserved bits returns an indeterminate, inconsistent value, and writes to reserved bits have no affect (but should not be attempted). These registers are only used for legacy operation. Software must not use these registers when running AHCI. The description of the I/O registers is shown in Table 15-2.

Table 15-2. Bus Master IDE I/O Register Address Map

BAR+ Offset	Mnemonic	Register	Default	Type
00	BMICP	Command Register Primary	00h	R/W
01	—	Reserved	—	RO
02	BMISP	Bus Master IDE Status Register Primary	00h	R/W, R/WC, RO
03	—	Reserved	—	RO
04–07	BMIDP	Bus Master IDE Descriptor Table Pointer Primary	xxxxxxxxh	R/W
08	BMICS	Command Register Secondary	00h	R/W
09	—	Reserved	—	RO
0Ah	BMISS	Bus Master IDE Status Register Secondary	00h	R/W, R/WC, RO
0Bh	—	Reserved	—	RO
0Ch–0Fh	BMIDS	Bus Master IDE Descriptor Table Pointer Secondary	xxxxxxxxh	R/W

15.2.1 BMIC[P,S]—Bus Master IDE Command Register (D31:F5)

Address Offset:	Primary: BAR + 00h Secondary: BAR + 08h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:4	Reserved.
3	**Read / Write Control (R/WC)—**R/W. This bit sets the direction of the bus master transfer: This bit must NOT be changed when the bus master function is active. 0 = Memory reads 1 = Memory writes
2:1	Reserved.
0	**Start/Stop Bus Master (START)—**R/W. 0 = All state information is lost when this bit is cleared. Master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active (that is, the Bus Master IDE Active bit (D31:F5:BAR + 02h, bit 0) of the Bus Master IDE Status register for that IDE channel is set) and the drive has not yet finished its data transfer (the Interrupt bit in the Bus Master IDE Status register for that IDE channel is not set), the bus master command is said to be aborted and data transferred from the drive may be discarded instead of being written to system memory. 1 = Enables bus master operation of the controller. Bus master operation does not actually start unless the Bus Master Enable bit (D31:F1:04h, bit 2) in PCI configuration space is also set. Bus master operation begins when this bit is detected changing from '0' to '1'. The controller will transfer data between the IDE device and memory only when this bit is set. Master operation can be halted by writing a '0' to this bit. ***Note:*** This bit is intended to be cleared by software after the data transfer is completed, as indicated by either the Bus Master IDE Active bit being cleared or the Interrupt bit of the Bus Master IDE Status register for that IDE channel being set, or both. Hardware does not clear this bit automatically. If this bit is cleared to '0' prior to the DMA data transfer being initiated by the drive in a device to memory data transfer, then the PCH will not send DMAT to terminate the data transfer. Software intervention (for example, sending SRST) is required to reset the interface in this condition.

15.2.2 BMIS[P,S]—Bus Master IDE Status Register (D31:F5)

Address Offset:	Primary: BAR + 02h Secondary: BAR + 0Ah	Attribute:	R/W, R/WC, RO
Default Value:	00h	Size:	8 bits

Bit	Description
7	**PRD Interrupt Status (PRDIS)**—R/WC. 0 = Software clears this bit by writing a '1' to it. 1 = This bit is set when the host controller execution of a PRD that has its PRD_INT bit set.
6	Reserved.
5	**Drive 0 DMA Capable—**R/W. 0 = Not Capable 1 = Capable. Set by device dependent code (BIOS or device driver) to indicate that drive 0 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance. The PCH does not use this bit. It is intended for systems that do not attach BMIDE to the PCI bus.
4:3	Reserved.
2	**Interrupt—**R/WC. 0 = Software clears this bit by writing a '1' to it. 1 = Set when a device FIS is received with the 'I' bit set, provided that software has not disabled interrupts using the IEN bit of the Device Control Register (see Chapter 5 of the *Serial ATA Specification*, Revision 1.0a).
1	**Error—**R/WC. 0 = Software clears this bit by writing a '1' to it. 1 = This bit is set when the controller encounters a target abort or master abort when transferring data on PCI.
0	**Bus Master IDE Active (ACT)**—RO. 0 = This bit is cleared by the PCH when the last transfer for a region is performed, where EOT for that region is set in the region descriptor. It is also cleared by the PCH when the Start Bus Master bit (D31:F5:BAR+ 00h, bit 0) is cleared in the Command register. When this bit is read as a 0, all data transferred from the drive during the previous bus master command is visible in system memory, unless the bus master command was aborted. 1 = Set by the PCH when the Start bit is written to the Command register.

15.2.3 BMID[P,S]—Bus Master IDE Descriptor Table Pointer Register (D31:F5)

Address Offset:	Primary: BAR + 04h–07h Secondary: BAR + 0Ch–0Fh	Attribute:	R/W
Default Value:	All bits undefined	Size:	32 bits

Bit	Description
31:2	**Address of Descriptor Table (ADDR)**—R/W. The bits in this field correspond to bits [31:2] of the memory location of the Physical Region Descriptor (PRD). The Descriptor Table must be DWord-aligned. The Descriptor Table must not cross a 64-K boundary in memory.
1:0	Reserved

15.3 Serial ATA Index/Data Pair Superset Registers

All of these I/O registers are in the core well. They are exposed only when SCC is 01h (that is, IDE programming interface) and the controller is not in combined mode. These are Index/Data Pair registers that are used to access the SerialATA superset registers (SerialATA Status, SerialATA Control and SerialATA Error). The I/O space for these registers is allocated through SIDPBA. Locations with offset from 08h to 0Fh are reserved for future expansion. Software-write operations to the reserved locations shall have no effect while software-read operations to the reserved locations shall return '0'.

15.3.1 SINDX—SATA Index Register (D31:F5)

Address Offset:	SIDPBA + 00h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Note: These are Index/Data Pair Registers that are used to access the SSTS, SCTL, and SERR. The I/O space for these registers is allocated through SIDPBA.

Bit	Description
31:16	Reserved
15:8	**Port Index (PIDX)**—R/W: This Index field is used to specify the port of the SATA controller at which the port-specific SSTS, SCTL, and SERR registers are located. 00h = Primary Master (Port 4) 02h = Secondary Master (Port 5) All other values are Reserved.
7:0	**Register Index (RIDX)**—R/W: This Index field is used to specify one out of three registers currently being indexed into. 00h = SSTS 01h = SCTL 02h = SERR All other values are Reserved

15.3.2 SDATA—SATA Index Data Register (D31:F5)

Address Offset:	SIDPBA + 04h	Attribute:	R/W
Default Value:	All bits undefined	Size:	32 bits

Note: These are Index/Data Pair Registers that are used to access the SSTS, SCTL, and SERR. The I/O space for these registers is allocated through SIDPBA.

Bit	Description
31:0	**Data (DATA)**—R/W: This Data register is a "window" through which data is read or written to the memory mapped registers. A read or write to this Data register triggers a corresponding read or write to the memory mapped register pointed to by the Index register. The Index register must be setup prior to the read or write to this Data register. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the "default" value is the same as the default value of the register pointed to by Index.

15.3.2.1 PxSSTS—Serial ATA Status Register (D31:F5)

Address Offset:		Attribute:	RO
Default Value:	00000000h	Size:	32 bits

SDATA when SINDX.RIDX is 00h. This is a 32-bit register that conveys the current state of the interface and host. The PCH updates it continuously and asynchronously. When the PCH transmits a COMRESET to the device, this register is updated to its reset values.

Bit	Description
31:12	Reserved
11:8	**Interface Power Management (IPM)—**RO**.** Indicates the current interface state: **Value** — **Description** 0h — Device not present or communication not established 1h — Interface in active state 2h — Interface in PARTIAL power management state 6h — Interface in SLUMBER power management state All other values reserved.
7:4	**Current Interface Speed (SPD)**—RO. Indicates the negotiated interface communication speed. **Value** — **Description** 0h — Device not present or communication not established 1h — Generation 1 communication rate negotiated 2h — Generation 2 communication rate negotiated All other values reserved. The PCH Supports Gen 1 communication rates (1.5 Gb/s) and Gen 2 rates (3.0 Gb/s).
3:0	**Device Detection (DET)—**RO**.** Indicates the interface device detection and Phy state: **Value** — **Description** 0h — No device detected and Phy communication not established 1h — Device presence detected but Phy communication not established 3h — Device presence detected and Phy communication established 4h — Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode All other values reserved.

15.3.2.2 PxSCTL—Serial ATA Control Register (D31:F5)

Address Offset:		Attribute:	R/W, RO
Default Value:	00000004h	Size:	32 bits

SDATA when SINDX.RIDX is 01h. This is a 32-bit read-write register by which software controls SATA capabilities. Writes to the SControl register result in an action being taken by the PCH or the interface. Reads from the register return the last value written to it.

Bit	Description
31:20	Reserved
19:16	Port Multiplier Port (PMP)—RO. This field is not used by AHCI.
15:12	Select Power Management (SPM)—RO. This field is not used by AHCI.
11:8	**Interface Power Management Transitions Allowed (IPM)—**R/W**.** Indicates which power states the PCH is allowed to transition to: **Value** — **Description** 0h — No interface restrictions 1h — Transitions to the PARTIAL state disabled 2h — Transitions to the SLUMBER state disabled 3h — Transitions to both PARTIAL and SLUMBER states disabled All other values reserved
7:4	**Speed Allowed (SPD)**—R/W. Indicates the highest allowable speed of the interface. This speed is limited by the CAP.ISS (ABAR+00h:bit 23:20) field. **Value** — **Description** 0h — No speed negotiation restrictions 1h — Limit speed negotiation to Generation 1 communication rate 2h — Limit speed negotiation to Generation 2 communication rate All other values reserved. The PCH Supports Gen 1 communication rates (1.5 Gb/s) and Gen 2 rates (3.0 Gb/s).
3:0	**Device Detection Initialization (DET)—**R/W**.** Controls the PCH's device detection and interface initialization. **Value** — **Description** 0h — No device detection or initialization action requested 1h — Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications re-initialized 4h — Disable the Serial ATA interface and put Phy in offline mode All other values reserved.

15.3.2.3 PxSERR—Serial ATA Error Register (D31:F5)

Address Offset:		Attribute:	R/WC
Default Value:	00000000h	Size:	32 bits

SDATA when SINDx.RIDX is 02h.

Bits 26:16 of this register contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes. Bits 11:0 contain error information used by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer.

Bit	Description
31:27	Reserved
26	**Exchanged (X)—**R/WC. When set to '1' this bit indicates that a change in device presence has been detected since the last time this bit was cleared. This bit shall always be set to 1' anytime a COMINIT signal is received. This bit is reflected in the P0IS.PCS bit.
25	**Unrecognized FIS Type (F)—**R/WC. Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized.
24	**Transport state transition error (T)—**R/WC. Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared.
23	**Link Sequence Error (S)**: Indicates that one or more Link state machine error conditions was encountered. The Link Layer state machine defines the conditions under which the link layer detects an erroneous transition.
22	**Handshake (H)—**R/WC. Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.
21	**CRC Error (C)—**R/WC. Indicates that one or more CRC errors occurred with the Link Layer.
20	**Disparity Error (D)—**R/WC. This field is not used by AHCI.
19	**10b to 8b Decode Error (B)—**R/WC. Indicates that one or more 10b to 8b decoding errors occurred.
18	**Comm Wake (W)—**R/WC. Indicates that a Comm Wake signal was detected by the Phy.
17	**Phy Internal Error (I)—**R/WC. Indicates that the Phy detected some internal error.
16	**PhyRdy Change (N)—**R/WC. When set to '1' this bit indicates that the internal PhyRdy signal changed state since the last time this bit was cleared. In the PCH, this bit will be set when PhyRdy changes from a 0 —> 1 or a 1 —> 0. The state of this bit is then reflected in the PxIS.PRCS interrupt status bit and an interrupt will be generated if enabled. Software clears this bit by writing a '1' to it.
15:12	Reserved
11	**Internal Error (E)—**R/WC. The SATA controller failed due to a master or target abort when attempting to access system memory.
10	**Protocol Error (P)—**R/WC. A violation of the Serial ATA protocol was detected. ***Note:*** The PCH does not set this bit for all protocol violations that may occur on the SATA link.
9	**Persistent Communication or Data Integrity Error (C)—**R/WC. A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes.
8	**Transient Data Integrity Error (T)—**R/WC. A data integrity error occurred that was not recovered by the interface.
7:2	Reserved.
1	**Recovered Communications Error (M)—**R/WC. Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers.
0	**Recovered Data Integrity Error (I)—**R/WC. A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.

§

16 EHCI Controller Registers (D29:F0, D26:F0)

16.1 USB EHCI Configuration Registers (USB EHCI—D29:F0, D26:F0)

Note: Register address locations that are not shown in Table 16-1 should be treated as Reserved (see Table 9-3 for details).

Note: Prior to BIOS initialization of the PCH USB subsystem, the EHCI controllers will appear as Function 7. After BIOS initialization, the EHCI controllers will be Function 0.

Table 16-1. USB EHCI PCI Register Address Map (USB EHCI—D29:F0, D26:F0) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default Value	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0290h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	20h	RO
0Ah	SCC	Sub Class Code	03h	RO
0Bh	BCC	Base Class Code	0Ch	RO
0Dh	PMLT	Primary Master Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	80h	RO
10h–13h	MEM_BASE	Memory Base Address	00000000h	R/W, RO
2Ch–2Dh	SVID	USB EHCI Subsystem Vendor Identification	XXXXh	R/W
2Eh–2Fh	SID	USB EHCI Subsystem Identification	XXXXh	R/W
34h	CAP_PTR	Capabilities Pointer	50h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	See register description	RO
50h	PWR_CAPID	PCI Power Management Capability ID	01h	RO
51h	NXT_PTR1	Next Item Pointer	58h	R/W
52h–53h	PWR_CAP	Power Management Capabilities	C9C2h	R/W
54h–55h	PWR_CNTL_STS	Power Management Control/Status	0000h	R/W, R/WC, RO
58h	DEBUG_CAPID	Debug Port Capability ID	0Ah	RO
59h	NXT_PTR2	Next Item Pointer #2	98h	RO
5Ah–5Bh	DEBUG_BASE	Debug Port Base Offset	20A0h	RO
60h	USB_RELNUM	USB Release Number	20h	RO
61h	FL_ADJ	Frame Length Adjustment	20h	R/W
62h–63h	PWAKE_CAP	Port Wake Capabilities	01FFh	R/W

Table 16-1. USB EHCI PCI Register Address Map (USB EHCI—D29:F0, D26:F0) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default Value	Type
64h–67h	—	Reserved	—	—
68h–6Bh	LEG_EXT_CAP	USB EHCI Legacy Support Extended Capability	00000001h	R/W, RO
6Ch–6Fh	LEG_EXT_CS	USB EHCI Legacy Extended Support Control/Status	00000000h	R/W, R/WC, RO
70h–73h	SPECIAL_SMI	Intel Specific USB 2.0 Intel SMI	00000000h	R/W, R/WC
74h–7Fh	—	Reserved	—	—
80h	ACCESS_CNTL	Access Control	00h	R/W
84–87h	EHCIIR1	EHCI Initialization Register 1	83088E01h	R/W
88–8Bh	EHCIIR2	EHCI Initialization Register 2	04000010h	R/W
98h	FLR_CID	FLR Capability ID	09h	RO
99h	FLR_NEXT	FLR Next Capability Pointer	00h	RO
9Ah–9Bh	FLR_CLV	FLR Capability Length and Version	2006h	RO, R/WO
9Ch	FLR_CTRL	FLR Control	00h	R/W
9Dh	FLR_STS	FLR Status	00h	RO
F4h–F7h	EHCIIR3	EHCI Initialization Register 3	00408588h	R/W
FCh–FFh	EHCIIR4	EHCI Initialization Register 4	20591708h	R/W

Note: All configuration registers in this section are in the core well and reset by a core well reset and the D3-to-D0 warm reset, except as noted.

16.1.1 VID—Vendor Identification Register (USB EHCI—D29:F0, D26:F0)

Offset Address: 00h–01h Attribute: RO
Default Value: 8086h Size: 16 bits

Bit	Description
15:0	**Vendor ID**—RO. This is a 16-bit value assigned to Intel.

16.1.2 DID—Device Identification Register (USB EHCI—D29:F0, D26:F0)

Offset Address: 02h–03h Attribute: RO
Default Value: See bit description Size: 16 bits

Bit	Description
15:0	**Device ID**—RO. This is a 16-bit value assigned to the PCH USB EHCI controller. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Device ID Register.

16.1.3 PCICMD—PCI Command Register (USB EHCI—D29:F0, D26:F0)

Address Offset:	04h–05h	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable—**R/W. 0 = The function is capable of generating interrupts. 1 = The function can not generate its interrupt to the interrupt controller. Note that the corresponding Interrupt Status bit (D29:F0, D26:F0:06h, bit 3) is not affected by the interrupt enable.
9	Fast Back to Back Enable (FBE)—RO. Hardwired to 0.
8	**SERR# Enable (SERR_EN)**—R/W. 0 = Disables EHC's capability to generate an SERR#. 1 = The Enhanced Host controller (EHC) is capable of generating (internally) SERR# in the following cases: • When it receive a completion status other than "successful" for one of its DMA initiated memory reads on DMI (and subsequently on its internal interface). • When it detects an address or command parity error and the Parity Error Response bit is set. • When it detects a data parity error (when the data is going into the EHC) and the Parity Error Response bit is set.
7	Wait Cycle Control (WCC)—RO. Hardwired to 0.
6	**Parity Error Response (PER)—**R/W. 0 = The EHC is not checking for correct parity (on its internal interface). 1 = The EHC is checking for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase. ***Note:*** If the EHC detects bad parity on the address or command phases when the bit is set to 1, the host controller does not take the cycle. It halts the host controller (if currently not halted) and sets the Host System Error bit in the USBSTS register. This applies to both requests and completions from the system interface. This bit must be set in order for the parity errors to generate SERR#.
5	VGA Palette Snoop (VPS)—RO. Hardwired to 0.
4	Postable Memory Write Enable (PMWE)—RO. Hardwired to 0.
3	Special Cycle Enable (SCE)—RO. Hardwired to 0.
2	**Bus Master Enable (BME)**—R/W. 0 = Disables this functionality. 1 = Enables the PCH to act as a master on the PCI bus for USB transfers.
1	**Memory Space Enable (MSE)—**R/W. This bit controls access to the USB 2.0 Memory Space registers. 0 = Disables this functionality. 1 = Enables accesses to the USB 2.0 registers. The Base Address register (D29:F0, D26:F0:10h) for USB 2.0 should be programmed before this bit is set.
0	I/O Space Enable (IOSE)—RO. Hardwired to 0.

16.1.4 PCISTS—PCI Status Register (USB EHCI—D29:F0, D26:F0)

Address Offset:	06h–07h	Attribute:	R/WC, RO
Default Value:	0290h	Size:	16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)**—R/WC. 0 = No parity error detected. 1 = This bit is set by the PCH when a parity error is seen by the EHCI controller, regardless of the setting of bit 6 or bit 8 in the Command register or any other conditions.
14	**Signaled System Error (SSE)—**R/WC. 0 = No SERR# signaled by the PCH. 1 = This bit is set by the PCH when it signals SERR# (internally). The SER_EN bit (bit 8 of the Command Register) must be 1 for this bit to be set.
13	**Received Master Abort (RMA)—**R/WC. 0 = No master abort received by EHC on a memory access. 1 = This bit is set when EHC, as a master, receives a master abort status on a memory access. This is treated as a Host Error and halts the DMA engines. This event can optionally generate an SERR# by setting the SERR# Enable bit**.**
12	**Received Target Abort (RTA)—**R/WC. 0 = No target abort received by EHC on memory access. 1 = This bit is set when EHC, as a master, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. This event can optionally generate an SERR# by setting the SERR# Enable bit (D29:F0, D26:F0:04h, bit 8).
11	Signaled Target Abort (STA)—RO. This bit is used to indicate when the EHCI function responds to a cycle with a target abort. There is no reason for this to happen, so this bit is hardwired to 0.
10:9	DEVSEL# Timing Status (DEVT_STS)—RO. This 2-bit field defines the timing for DEVSEL# assertion.
8	**Master Data Parity Error Detected (DPED)—**R/WC. 0 = No data parity error detected on USB2.0 read completion packet. 1 = This bit is set by the PCH when a data parity error is detected on a USB 2.0 read completion packet on the internal interface to the EHCI host controller and bit 6 of the Command register is set to 1.
7	Fast Back to Back Capable (FB2BC)—RO. Hardwired to 1.
6	User Definable Features (UDF)—RO. Hardwired to 0.
5	66 MHz Capable (66 MHz _CAP)—RO. Hardwired to 0.
4	Capabilities List (CAP_LIST)—RO. Hardwired to 1 indicating that offset 34h contains a valid capabilities pointer.
3	**Interrupt Status—**RO. This bit reflects the state of this function's interrupt at the input of the enable/disable logic. 0 = This bit will be 0 when the interrupt is deasserted. 1 = This bit is a 1 when the interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
2:0	Reserved

16.1.5 RID—Revision Identification Register (USB EHCI—D29:F0, D26:F0)

Offset Address:	08h	Attribute:	RO
Default Value:	See bit description	Size:	8 bits

Bit	Description
7:0	**Revision ID**—RO. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Revision ID Register.

16.1.6 PI—Programming Interface Register (USB EHCI—D29:F0, D26:F0)

Address Offset:	09h	Attribute:	RO
Default Value:	20h	Size:	8 bits

Bit	Description
7:0	**Programming Interface**—RO. A value of 20h indicates that this USB 2.0 host controller conforms to the EHCI Specification.

16.1.7 SCC—Sub Class Code Register (USB EHCI—D29:F0, D26:F0)

Address Offset:	0Ah	Attribute:	RO
Default Value:	03h	Size:	8 bits

Bit	Description
7:0	**Sub Class Code (SCC)**—RO. 03h = Universal serial bus host controller.

16.1.8 BCC—Base Class Code Register (USB EHCI—D29:F0, D26:F0)

Address Offset:	0Bh	Attribute:	RO
Default Value:	0Ch	Size:	8 bits

Bit	Description
7:0	**Base Class Code (BCC)**—RO. 0Ch = Serial bus controller.

16.1.9 PMLT—Primary Master Latency Timer Register (USB EHCI—D29:F0, D26:F0)

Address Offset:	0Dh	Attribute:	RO
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	**Master Latency Timer Count (MLTC)—**RO. Hardwired to 00h. Because the EHCI controller is internally implemented with arbitration on an interface (and not PCI), it does not need a master latency timer.

16.1.10 HEADTYP—Header Type Register (USB EHCI—D29:F0, D26:F0)

Address Offset:	0Eh	Attribute:	RO
Default Value:	80h	Size:	8 bits

Bit	Description
7	**Multi-Function Device**—RO. When set to '1' indicates this is a multifunction device: 0 = Single-function device 1 = Multi-function device.
6:0	Configuration Layout. Hardwired to 00h, which indicates the standard PCI configuration layout.

16.1.11 MEM_BASE—Memory Base Address Register (USB EHCI—D29:F0, D26:F0)

Address Offset:	10h–13h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:10	**Base Address**—R/W. Bits [31:10] correspond to memory address signals [31:10], respectively. This gives 1-KB of locatable memory space aligned to 1-KB boundaries.
9:4	Reserved
3	**Prefetchable**—RO. Hardwired to 0 indicating that this range should not be prefetched.
2:1	**Type**—RO. Hardwired to 00b indicating that this range can be mapped anywhere within 32-bit address space.
0	**Resource Type Indicator (RTE)**—RO. Hardwired to 0 indicating that the base address field in this register maps to memory space.

16.1.12 SVID—USB EHCI Subsystem Vendor ID Register (USB EHCI—D29:F0, D26:F0)

Address Offset:	2Ch–2Dh	Attribute:	R/W
Default Value:	XXXXh	Size:	16 bits
Reset:	None		

Bit	Description
15:0	**Subsystem Vendor ID (SVID)**—R/W. This register, in combination with the USB 2.0 Subsystem ID register, enables the operating system to distinguish each subsystem from the others. ***Note:*** Writes to this register are enabled when the WRT_RDONLY bit (D29:F0, D26:F0:80h, bit 0) is set to 1.

16.1.13 SID—USB EHCI Subsystem ID Register (USB EHCI—D29:F0, D26:F0)

Address Offset:	2Eh–2Fh	Attribute:	R/W
Default Value:	XXXXh	Size:	16 bits
Reset:	None		

Bit	Description
15:0	**Subsystem ID (SID)**—R/W. BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s). ***Note:*** Writes to this register are enabled when the WRT_RDONLY bit (D29:F0, D26:F0:80h, bit 0) is set to 1.

16.1.14 CAP_PTR—Capabilities Pointer Register (USB EHCI—D29:F0, D26:F0)

Address Offset:	34h	Attribute:	RO
Default Value:	50h	Size:	8 bits

Bit	Description
7:0	**Capabilities Pointer (CAP_PTR)**—RO. This register points to the starting offset of the USB 2.0 capabilities ranges.

16.1.15 INT_LN—Interrupt Line Register (USB EHCI—D29:F0, D26:F0)

Address Offset:	3Ch	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Function Level Reset:	No		

Bit	Description
7:0	**Interrupt Line (INT_LN)—**R/W. This data is not used by the PCH. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to.

16.1.16 INT_PN—Interrupt Pin Register (USB EHCI—D29:F0, D26:F0)

Address Offset:	3Dh	Attribute:	RO
Default Value:	See Description	Size:	8 bits

Bit	Description
7:0	**Interrupt Pin—**RO. This reflects the value of D29IP.E1IP (Chipset Config Registers:Offset 3108:bits 3:0) or D26IP.E2IP (Chipset Config Registers:Offset 3114:bits 3:0). ***Note:*** Bits 7:4 are always 0h

16.1.17 PWR_CAPID—PCI Power Management Capability ID Register (USB EHCI—D29:F0, D26:F0)

Address Offset:	50h	Attribute:	RO
Default Value:	01h	Size:	8 bits

Bit	Description
7:0	**Power Management Capability ID**—RO. A value of 01h indicates that this is a PCI Power Management capabilities field.

16.1.18 NXT_PTR1—Next Item Pointer #1 Register (USB EHCI—D29:F0, D26:F0)

Address Offset:	51h	Attribute:	R/W
Default Value:	58h	Size:	8 bits

Bit	Description
7:0	**Next Item Pointer 1 Value**—R/W (special). This register defaults to 58h, which indicates that the next capability registers begin at configuration offset 58h. This register is writable when the WRT_RDONLY bit (D29:F0, D26:F0:80h, bit 0) is set. This allows BIOS to effectively hide the Debug Port capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any master-initiated traffic. Only values of 58h (Debug Port and FLR capabilities visible) and 98h (Debug Port invisible, next capability is FLR) are expected to be programmed in this register. ***Note:*** Register not reset by D3-to-D0 warm reset.

16.1.19 PWR_CAP—Power Management Capabilities Register (USB EHCI—D29:F0, D26:F0)

Address Offset:	52h–53h	Attribute:	R/W, RO
Default Value:	C9C2h	Size:	16 bits

Bit	Description
15:11	**PME Support (PME_SUP)**—R/W. This 5-bit field indicates the power states in which the function may assert PME#. The PCH EHC does not support the D1 or D2 states. For all other states, the PCH EHC is capable of generating PME#. Software should never need to modify this field.
10	D2 Support (D2_SUP)—RO. 0 = D2 State is not supported
9	D1 Support (D1_SUP)—RO. 0 = D1 State is not supported
8:6	**Auxiliary Current (AUX_CUR)**—R/W. The PCH EHC reports 375 mA maximum suspend well current required when in the $D3_{COLD}$ state.
5	**Device Specific Initialization (DSI)**—RO. The PCH reports 0, indicating that no device-specific initialization is required.
4	Reserved
3	**PME Clock (PME_CLK)**—RO. The PCH reports 0, indicating that no PCI clock is required to generate PME#.
2:0	**Version (VER)**—RO. The PCH reports 010b, indicating that it complies with Revision 1.1 of the PCI Power Management Specification.

Notes:
1. Normally, this register is read-only to report capabilities to the power management software. To report different power management capabilities, depending on the system in which the PCH is used, bits 15:11 and 8:6 in this register are writable when the WRT_RDONLY bit (D29:F0, D26:F0:80h, bit 0) is set. The value written to this register does not affect the hardware other than changing the value returned during a read.
2. Reset: core well, but not D3-to-D0 warm reset.

16.1.20 PWR_CNTL_STS—Power Management Control/ Status Register (USB EHCI—D29:F0, D26:F0)

Address Offset: 54h–55h Attribute: R/W, R/WC, RO
Default Value: 0000h Size: 16 bits
Function Level Reset: No (Bits 8 and 15 only)

Bit	Description
15	**PME Status—**R/WC. 0 = Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). 1 = This bit is set when the PCH EHC would normally assert the PME# signal independent of the state of the PME_En bit. ***Note:*** This bit must be explicitly cleared by the operating system each time the operating system is loaded. This bit is not reset by Function Level Reset.
14:13	Data Scale—RO. Hardwired to 00b indicating it does not support the associated Data register.
12:9	Data Select—RO. Hardwired to 0000b indicating it does not support the associated Data register.
8	**PME Enable—**R/W. 0 = Disable. 1 = Enables the PCH EHC to generate an internal PME signal when PME_Status is 1. ***Note:*** This bit must be explicitly cleared by the operating system each time it is initially loaded. This bit is not reset by Function Level Reset.
7:2	Reserved
1:0	**Power State—**R/W. This 2-bit field is used both to determine the current power state of EHC function and to set a new power state. The definition of the field values are: 00 = D0 state 11 = $D3_{HOT}$ state If software attempts to write a value of 10b or 01b in to this field, the write operation completes normally; however, the data is discarded and no state change occurs. When in the D3HOT state, the PCH does not accept accesses to the EHC memory range; but the configuration space is still accessible. When not in the D0 state, the generation of the interrupt output is blocked. Specifically, the EHC interrupt is not asserted by the PCH when not in the D0 state. When software changes this value from the D3HOT state to the D0 state, an internal warm (soft) controller reset is generated, and software must re-initialize the function.

Note: Reset (bits 15, 8): suspend well, and not D3-to-D0 warm reset nor core well reset.

16.1.21 DEBUG_CAPID—Debug Port Capability ID Register (USB EHCI—D29:F0, D26:F0)

Address Offset: 58h Attribute: RO
Default Value: 0Ah Size: 8 bits

Bit	Description
7:0	**Debug Port Capability ID**—RO. Hardwired to 0Ah indicating that this is the start of a Debug Port Capability structure.

16.1.22 NXT_PTR2—Next Item Pointer #2 Register (USB EHCI—D29:F0, D26:F0)

Address Offset: 59h
Default Value: 98h
Function Level Reset: No
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Next Item Pointer 2 Capability—**RO. This register points to the next capability in the Function Level Reset capability structure.

16.1.23 DEBUG_BASE—Debug Port Base Offset Register (USB EHCI—D29:F0, D26:F0)

Address Offset: 5Ah–5Bh
Default Value: 20A0h
Attribute: RO
Size: 16 bits

Bit	Description
15:13	**BAR Number—**RO. Hardwired to 001b to indicate the memory BAR begins at offset 10h in the EHCI configuration space.
12:0	**Debug Port Offset—**RO. Hardwired to 0A0h to indicate that the Debug Port registers begin at offset A0h in the EHCI memory range.

16.1.24 USB_RELNUM—USB Release Number Register (USB EHCI—D29:F0, D26:F0)

Address Offset: 60h
Default Value: 20h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**USB Release Number**—RO. A value of 20h indicates that this controller follows *Universal Serial Bus (USB) Specification, Revision 2.0*.

16.1.25 FL_ADJ—Frame Length Adjustment Register (USB EHCI—D29:F0, D26:F0)

Address Offset: 61h
Default Value: 20h
Function Level Reset: No
Attribute: R/W
Size: 8 bits

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register should only be modified when the HChalted bit (D29:F0, D26:F0:CAPLENGTH + 24h, bit 12) in the USB2.0_STS register is a 1. Changing value of this register while the host controller is operating yields undefined results. It should not be reprogrammed by USB system software unless the default or BIOS programmed values are incorrect, or the system is restoring the register while returning from a suspended state.

These bits in suspend well and not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description
7:6	Reserved—RO. These bits are reserved for future use and should read as 00b.
5:0	**Frame Length Timing Value—**R/W. Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. **Frame Length (# 480 MHz Clocks) (decimal)** / **Frame Length Timing Value (this register) (decimal)** 59488 / 0 59504 / 1 59520 / 2 — / — 59984 / 31 60000 / 32 — / — 60480 / 62

16.1.26 PWAKE_CAP—Port Wake Capability Register (USB EHCI—D29:F0, D26:F0)

Address Offset: 62–63h
Default Value: 01FFh
Default Value: 07FFh
Function Level Reset: No

Attribute: R/W
Size: 16 bits

This register is in the suspend power well. The intended use of this register is to establish a policy about which ports are to be used for wake events. Bit positions 1–8(D29) or 1–6(D26) in the mask correspond to a physical port implemented on the current EHCI controller. A 1 in a bit position indicates that a device connected below the port can be enabled as a wake-up device and the port may be enabled for disconnect/connect or overcurrent events as wake-up events. This is an information-only mask register. The bits in this register **do not** affect the actual operation of the EHCI host controller. The system-specific policy can be established by BIOS initializing this register to a system-specific value. System software uses the information in this register when enabling devices and ports for remote wake-up.

These bits are not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description
15:9 (D29) 15:7 (D26)	Reserved.
8:1 (D29) 6:1 (D26)	**Port Wake Up Capability Mask—**R/W. Bit positions 1 through 8 (Device 29) or 1 through 6(Device 26) correspond to a physical port implemented on this host controller. For example, bit position 1 corresponds to port 1, bit position 2 corresponds to port 2, etc.
0	**Port Wake Implemented—**R/W. A 1 in this bit indicates that this register is implemented to software.

16.1.27 LEG_EXT_CAP—USB EHCI Legacy Support Extended Capability Register (USB EHCI—D29:F0, D26:F0)

Address Offset: 68–6Bh
Attribute: R/W, RO
Default Value: 00000001h
Size: 32 bits
Power Well: Suspend
Function Level Reset: No

Note: These bits are not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description
31:25	Reserved—RO. Hardwired to 00h
24	**HC OS Owned Semaphore**—R/W. System software sets this bit to request ownership of the EHCI controller. Ownership is obtained when this bit reads as 1 and the HC BIOS Owned Semaphore bit reads as clear.
23:17	Reserved—RO. Hardwired to 00h
16	**HC BIOS Owned Semaphore—**R/W. The BIOS sets this bit to establish ownership of the EHCI controller. System BIOS will clear this bit in response to a request for ownership of the EHCI controller by system software.
15:8	**Next EHCI Capability Pointer**—RO. Hardwired to 00h to indicate that there are no EHCI Extended Capability structures in this device.
7:0	**Capability ID**—RO. Hardwired to 01h to indicate that this EHCI Extended Capability is the Legacy Support Capability.

16.1.28 LEG_EXT_CS—USB EHCI Legacy Support Extended Control / Status Register (USB EHCI—D29:F0, D26:F0)

Address Offset: 6C–6Fh
Attribute: R/W, R/WC, RO
Default Value: 00000000h
Size: 32 bits
Power Well: Suspend
Function Level Reset: No

Note: These bits are not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description
31	**Intel SMI on BAR—**R/WC. Software clears this bit by writing a 1 to it. 0 = Base Address Register (BAR) not written. 1 = This bit is set to 1 when the Base Address Register (BAR) is written.
30	**Intel SMI on PCI Command**—R/WC. Software clears this bit by writing a 1 to it. 0 = PCI Command (PCICMD) Register Not written. 1 = This bit is set to 1 when the PCI Command (PCICMD) Register is written.
29	**Intel SMI on OS Ownership Change**—R/WC. Software clears this bit by writing a 1 to it. 0 = No HC operating system Owned Semaphore bit change. 1 = This bit is set to 1 when the HC operating system Owned Semaphore bit in the LEG_EXT_CAP register (D29:F0, D26:F0:68h, bit 24) transitions from 1 to 0 or 0 to 1.
28:22	Reserved.
21	**Intel SMI on Async Advance**—RO. This bit is a shadow bit of the Interrupt on Async Advance bit (D29:F0, D26:F0:CAPLENGTH + 24h, bit 5) in the USB2.0_STS register. ***Note:*** To clear this bit system software must write a 1 to the Interrupt on Async Advance bit in the USB2.0_STS register.
20	**Intel SMI on Host System Error**—RO. This bit is a shadow bit of Host System Error bit in the USB2.0_STS register (D29:F0, D26:F0:CAPLENGTH + 24h, bit 4). ***Note:*** To clear this bit system software must write a 1 to the Host System Error bit in the USB2.0_STS register.

Bit	Description
19	**Intel SMI on Frame List Rollover**—RO. This bit is a shadow bit of Frame List Rollover bit (D29:F0, D26:F0:CAPLENGTH + 24h, bit 3) in the USB2.0_STS register. ***Note:*** To clear this bit system software must write a 1 to the Frame List Rollover bit in the USB2.0_STS register.
18	**Intel SMI on Port Change Detect**—RO. This bit is a shadow bit of Port Change Detect bit (D29:F0, D26:F0:CAPLENGTH + 24h, bit 2) in the USB2.0_STS register. ***Note:*** To clear this bit system software must write a 1 to the Port Change Detect bit in the USB2.0_STS register.
17	**Intel SMI on USB Error**—RO. This bit is a shadow bit of USB Error Interrupt (USBERRINT) bit (D29:F0, D26:F0:CAPLENGTH + 24h, bit 1) in the USB2.0_STS register. ***Note:*** To clear this bit system software must write a 1 to the USB Error Interrupt bit in the USB2.0_STS register.
16	**Intel SMI on USB Complete—**RO. This bit is a shadow bit of USB Interrupt (USBINT) bit (D29:F0, D26:F0:CAPLENGTH + 24h, bit 0) in the USB2.0_STS register. ***Note:*** To clear this bit system software must write a 1 to the USB Interrupt bit in the USB2.0_STS register.
15	**Intel SMI on BAR Enable—**R/W. 0 = Disable. 1 = Enable. When this bit is 1 and Intel SMI on BAR (D29:F0, D26:F0:6Ch, bit 31) is 1, then the host controller will issue an Intel SMI.
14	**Intel SMI on PCI Command Enable**—R/W. 0 = Disable. 1 = Enable. When this bit is 1 and Intel SMI on PCI Command (D29:F0, D26:F0:6Ch, bit 30) is 1, then the host controller will issue an Intel SMI.
13	**Intel SMI on OS Ownership Enable**—R/W. 0 = Disable. 1 = Enable. When this bit is a 1 AND the operating system Ownership Change bit (D29:F0, D26:F0:6Ch, bit 29) is 1, the host controller will issue an Intel SMI.
12:6	Reserved
5	**Intel SMI on Async Advance Enable**—R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the Intel SMI on Async Advance bit (D29:F0, D26:F0:6Ch, bit 21) is a 1, the host controller will issue an Intel SMI immediately.
4	**Intel SMI on Host System Error Enable**—R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the Intel SMI on Host System Error (D29:F0, D26:F0:6Ch, bit 20) is a 1, the host controller will issue an Intel SMI.
3	**Intel SMI on Frame List Rollover Enable**—R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the Intel SMI on Frame List Rollover bit (D29:F0, D26:F0:6Ch, bit 19) is a 1, the host controller will issue an Intel SMI.
2	**Intel SMI on Port Change Enable**—R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the Intel SMI on Port Change Detect bit (D29:F0, D26:F0:6Ch, bit 18) is a 1, the host controller will issue an Intel SMI.
1	**Intel SMI on USB Error Enable**—R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the Intel SMI on USB Error bit (D29:F0, D26:F0:6Ch, bit 17) is a 1, the host controller will issue an Intel SMI immediately.
0	**Intel SMI on USB Complete Enable**—R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the Intel SMI on USB Complete bit (D29:F0, D26:F0:6Ch, bit 16) is a 1, the host controller will issue an Intel SMI immediately.

16.1.29 SPECIAL_SMI—Intel® Specific USB 2.0 Intel® SMI Register (USB EHCI—D29:F0, D26:F0)

Address Offset: 70h–73h
Attribute: R/W, R/WC
Default Value: 00000000h
Size: 32 bits
Power Well: Suspend
Function Level Reset: No

Note: These bits are not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description
31:25	Reserved
24:22	**Intel SMI on PortOwner—**R/WC. Software clears these bits by writing a 1 to it. 0 = No Port Owner bit change. 1 = Bits 24:22 correspond to the Port Owner bits for ports 0 (22) through 3(24). These bits are set to 1 when the associated Port Owner bits transition from 0 to 1 or 1 to 0.
21	**Intel SMI on PMCSR**—R/WC. Software clears these bits by writing a 1 to it. 0 = Power State bits Not modified. 1 = Software modified the Power State bits in the Power Management Control/Status (PMCSR) register (D29:F0, D26:F0:54h).
20	**Intel SMI on Async**—R/WC. Software clears these bits by writing a 1 to it. 0 = No Async Schedule Enable bit change 1 = Async Schedule Enable bit transitioned from 1 to 0 or 0 to 1.
19	**Intel SMI on Periodic**—R/WC. Software clears this bit by writing a 1 it. 0 = No Periodic Schedule Enable bit change. 1 = Periodic Schedule Enable bit transitions from 1 to 0 or 0 to 1.
18	**Intel SMI on CF**—R/WC. Software clears this bit by writing a 1 it. 0 = No Configure Flag (CF) change. 1 = Configure Flag (CF) transitions from 1 to 0 or 0 to 1.
17	**Intel SMI on HCHalted—**R/WC. Software clears this bit by writing a 1 it. 0 = HCHalted did Not transition to 1 (as a result of the Run/Stop bit being cleared). 1 = HCHalted transitions to 1 (as a result of the Run/Stop bit being cleared).
16	**Intel SMI on HCReset—**R/WC. Software clears this bit by writing a 1 it. 0 = HCRESET did Not transitioned to 1. 1 = HCRESET transitioned to 1.
15:14	Reserved
13:6	**Intel SMI on PortOwner Enable**—R/W. 0 = Disable. 1 = Enable. When any of these bits are 1 and the corresponding Intel SMI on PortOwner bits are 1, then the host controller will issue an SMI. Unused ports should have their corresponding bits cleared.
5	**Intel SMI on PMSCR Enable**—R/W. 0 = Disable. 1 = Enable. When this bit is 1 and Intel SMI on PMSCR is 1, then the host controller will issue an Intel SMI.
4	**Intel SMI on Async Enable**—R/W. 0 = Disable. 1 = Enable. When this bit is 1 and Intel SMI on Async is 1, then the host controller will issue an Intel SMI
3	**Intel SMI on Periodic Enable**—R/W. 0 = Disable. 1 = Enable. When this bit is 1 and Intel SMI on Periodic is 1, then the host controller will issue an Intel SMI.
2	**Intel SMI on CF Enable**—R/W. 0 = Disable. 1 = Enable. When this bit is 1 and Intel SMI on CF is 1, then the host controller will issue an Intel SMI.

Bit	Description
1	**Intel SMI on HCHalted Enable**—R/W. 0 = Disable. 1 = Enable. When this bit is a 1 and Intel SMI on HCHalted is 1, then the host controller will issue an Intel SMI.
0	**Intel SMI on HCReset Enable**—R/W. 0 = Disable. 1 = Enable. When this bit is a 1 and Intel SMI on HCReset is 1, then host controller will issue an Intel SMI.

16.1.30 ACCESS_CNTL—Access Control Register (USB EHCI—D29:F0, D26:F0)

Address Offset: 80h
Attribute: R/W
Default Value: 00h
Size: 8 bits
Function Level Reset: No

Bit	Description
7:1	Reserved
0	**WRT_RDONLY—**R/W. When set to 1, this bit enables a select group of normally read-only registers in the EHC function to be written by software. Registers that may only be written when this mode is entered are noted in the summary tables and detailed description as "Read/Write-Special". The registers fall into two categories: 1. System-configured parameters 2. Status bits

16.1.31 EHCIIR1—EHCI Initialization Register 1 (USB EHCI—D29:F0, D26:F0)

Address Offset: 84h–87h
Attribute: R/W
Default Value: 83088E01h
Size: 32 bits

Bit	Description
31:29	Reserved
28	**EHCI Prefetch Entry Clear—**R/W. 0 = EHC will clear prefetched entries in DMA. 1 = EHC will not clear prefetched entries in DMA
27:19	Reserved
18	**EHCI Initialization Register 1 Field 2**—R/W. BIOS may write to this bit field.
17:11	Reserved
10:9	**EHCI Initialization Register 1 Field 1**—R/W. BIOS may write to this bit field.
8	**Asynchronous Schedule Caching Disable**—R/W. 0 = Caching of Asynchronous Schedule is enabled. (default) 1 = Caching of Asynchronous Schedule is disabled.
7:5	Reserved
4	**Intel® Pre-fetch Based Pause Enable—**R/W. 0 = Intel Pre-fetch Based Pause is disabled. 1 = Intel Pre-fetch Based Pause is enabled.
3:0	Reserved

16.1.32 EHCIIR2—EHCI Initialization Register 2 (USB EHCI—D29:F0, D26:F0)

Offset Address: 88h–8Bh Attribute: R/W
Default Value: 04000010h Size: 32-bit

Bit	Description
31:30	Reserved
29	**EHCI Initialization Register 2 Field 6**—R/W. BIOS may write to this bit field.
28:20	Reserved
19	**EHCI Initialization Register 2 Field 5**—R/W. BIOS may write to this bit field.
18:12	Reserved
11	**EHCI Initialization Register 2 Field 4**—R/W. BIOS may write to this bit field.
10	**EHCI Initialization Register 2 Field 3**—R/W. BIOS may write to this bit field.
9	Reserved
8	**EHCI Initialization Register 2 Field 2**—R/W. BIOS may write to this bit field.
7:6	Reserved
5	**EHCI Initialization Register 2 Field 1—**R/W. BIOS may write to this bit field.
4:0	Reserved

16.1.33 FLR_CID—Function Level Reset Capability ID (USB EHCI—D29:F0, D26:F0)

Address Offset: 98h Attribute: RO
Default Value: 09h Size: 8 bits
Function Level Reset: No

Bit	Description
7:0	**Capability ID**—R0. 13h = If FLRCSSEL = 0 09h (Vendor Specific Capability) = If FLRCSSEL = 1

16.1.34 FLR_NEXT—Function Level Reset Next Capability Pointer (USB EHCI—D29:F0, D26:F0)

Address Offset: 99h Attribute: RO
Default Value: 00h Size: 8 bits
Function Level Reset: No

Bit	Description
7:0	A value of 00h in this register indicates this is the last capability field.

16.1.35 FLR_CLV—Function Level Reset Capability Length and Version (USB EHCI—D29:F0, D26:F0)

Address Offset: 9Ah-9Bh
Attribute: R/WO, RO
Default Value: 2006h
Size: 16 bits
Function Level Reset: No

When FLRCSSEL = '0' this register is defined as follows:

Bit	Description
15:10	Reserved.
9	**FLR Capability**—R/WO. 1 = Support for Function Level Reset (FLR).
8	**TXP Capability**—R/WO. 1 = Support for Transactions Pending (TXP) bit. TXP must be supported if FLR is supported.
7:0	**Capability Length—**RO. This field indicates the # of bytes of this vendor specific capability as required by the PCI specification. It has the value of 06h for the FLR capability.

When FLRCSSEL = '1' this register is defined as follows:

Bit	Description
15:12	**Vendor Specific Capability ID—**RO. A value of 2h in this field identifies this capability as Function Level Reset.
11:8	**Capability Version—**RO. This field indicates the version of the FLR capability.
7:0	**Capability Length—**RO. This field indicates the # of bytes of this vendor specific capability as required by the PCI specification. It has the value of 06h for the FLR capability.

16.1.36 FLR_CTRL—Function Level Reset Control Register (USB EHCI—D29:F0, D26:F0)

Address Offset: 9Ch
Attribute: R/W
Default Value: 00h
Size: 8 bits
Function Level Reset: No

Bit	Description
7:1	Reserved
0	**Initiate FLR**—R/W. This bit is used to initiate FLR transition. A write of '1' initiates FLR transition. Since hardware must not respond to any cycles until FLR completion, the value read by software from this bit is always '0'.

16.1.37 FLR_STS—Function Level Reset Status Register (USB EHCI—D29:F0, D26:F0)

Address Offset: 9Dh
Default Value: 00h
Function Level Reset: No
Attribute: RO
Size: 8 bits

Bit	Description
7:1	Reserved
0	**Transactions Pending (TXP)**—RO. 0 = Completions for all non-posted requests have been received. 1 = Controller has issued non-posted requests which have no bee completed.

16.1.38 EHCIIR3—EHCI Initialization Register 3 (USB EHCI—D29:F0, D26:F0)

Offset Address: F4h–F7h
Default Value: 00408588h
Attribute: R/W
Size: 32-bit

Bit	Description
31	**EHCIIR3 Write Enable**—R/W. 0 = Writes to the EHCIIR3 register are disabled 1 = If set, the values of the EHCIIR3 register may be modified
30:24	Reserved
23:22	**EHCI Initialization Register 3 Field 1**—R/W. BIOS may write to this bit field.
21:0	Reserved

16.1.39 EHCIIR4—EHCI Initialization Register 4 (USB EHCI—D29:F0, D26:F0)

Offset Address: FCh–FFh
Default Value: 20591708h
Attribute: R/W
Size: 32-bit

Bit	Description
31:18	Reserved
17	**EHCI Initialization Register 4 Field 2**—R/W. BIOS may write to this bit field.
16	Reserved
15	**EHCI Initialization Register 4 Field 1**—R/W. BIOS may write to this bit field.
14:0	Reserved

16.2 Memory-Mapped I/O Registers

The EHCI memory-mapped I/O space is composed of two sets of registers: Capability Registers and Operational Registers.

Note: The PCH EHCI controller will not accept memory transactions (neither reads nor writes) as a target that are locked transactions. The locked transactions should not be forwarded to PCI as the address space is known to be allocated to USB.

Note: When the EHCI function is in the D3 PCI power state, accesses to the USB 2.0 memory range are ignored and result a master abort. Similarly, if the Memory Space Enable (MSE) bit (D29:F0, D26:F0:04h, bit 1) is not set in the Command register in configuration space, the memory range will not be decoded by the PCH enhanced host controller (EHC). If the MSE bit is not set, the PCH must default to allowing any memory accesses for the range specified in the BAR to go to PCI. This is because the range may not be valid and, therefore, the cycle must be made available to any other targets that may be currently using that range.

16.2.1 Host Controller Capability Registers

These registers specify the limits, restrictions and capabilities of the host controller implementation. Within the host controller capability registers, only the structural parameters register is writable. These registers are implemented in the suspend well and is only reset by the standard suspend-well hardware reset, not by HCRESET or the D3-to-D0 reset.

Note: Note that the EHCI controller does not support as a target memory transactions that are locked transactions. Attempting to access the EHCI controller Memory-Mapped I/O space using locked memory transactions will result in undefined behavior.

Note: Note that when the USB2 function is in the D3 PCI power state, accesses to the USB2 memory range are ignored and will result in a master abort Similarly, if the Memory Space Enable (MSE) bit is not set in the Command register in configuration space, the memory range will not be decoded by the Enhanced Host Controller (EHC). If the MSE bit is not set, the EHC will not claim any memory accesses for the range specified in the BAR.

Table 16-2. Enhanced Host Controller Capability Registers

MEM_BASE + Offset	Mnemonic	Register	Default	Type
00h	CAPLENGTH	Capabilities Registers Length	20h	RO
02h–03h	HCIVERSION	Host Controller Interface Version Number	0100h	RO
04h–07h	HCSPARAMS	Host Controller Structural Parameters	00204208h (D29:F0) 00203206 (D26:F0)	R/W (special), RO
08h–0Bh	HCCPARAMS	Host Controller Capability Parameters	00006881h	RO

Note: "Read/Write Special" means that the register is normally read-only, but may be written when the WRT_RDONLY bit is set. Because these registers are expected to be programmed by BIOS during initialization, their contents must not get modified by HCRESET or D3-to-D0 internal reset.

16.2.1.1 CAPLENGTH—Capability Registers Length Register

Offset:	MEM_BASE + 00h	Attribute:	RO
Default Value:	20h	Size:	8 bits

Bit	Description
7:0	**Capability Register Length Value**—RO. This register is used as an offset to add to the Memory Base Register (D29:F0, D26:F0:10h) to find the beginning of the Operational Register Space. This field is hardwired to 20h indicating that the Operation Registers begin at offset 20h.

16.2.1.2 HCIVERSION—Host Controller Interface Version Number Register

Offset:	MEM_BASE + 02h–03h	Attribute:	RO
Default Value:	0100h	Size:	16 bits

Bit	Description
15:0	**Host Controller Interface Version Number—**RO. This is a two-byte register containing a BCD encoding of the version number of interface that this host controller interface conforms.

16.2.1.3 HCSPARAMS—Host Controller Structural Parameters

Offset:	MEM_BASE + 04h–07h	Attribute:	R/W, RO
Default Value:	00204208h (D29:F0) 00203206h (D26:F0)	Size:	32 bits

Function Level Reset: No

Note: This register is reset by a suspend well reset and not a D3-to-D0 reset or HCRESET.

Bit	Description
31:24	Reserved
23:20	**Debug Port Number (DP_N)—**RO. Hardwired to 2h indicating that the Debug Port is on the second lowest numbered port on the EHCI. EHCI#1: Port 1 EHCI#2: Port 9
19:16	Reserved
15:12	**Number of Companion Controllers (N_CC)—**R/W. This field indicates the number of companion controllers associated with this USB EHCI host controller. BIOS must program this field to 0b to indicate companion host controllers are not supported. Port-ownership hand-off is not supported. Only high-speed devices are supported on the host controller root ports.
11:8	**Number of Ports per Companion Controller (N_PCC)**—RO. This field indicates the number of ports supported per companion host controller. This field is 0h indication no other companion controller support.
7:4	Reserved. These bits are reserved and default to 0.
3:0	**N_PORTS—**R/W. This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 1h to Fh. A 0 in this field is undefined. For Integrated USB 2.0 Rate Matching Hub Enabled: Each EHCI reports 2 ports by default. Port 0 assigned to the RMH and port 1 assigned as the debug port. When the KVM/USB-R feature is enabled it will show up as Port2 on the EHCI, and BIOS would need to update this field to 3h.

Note: This register is writable when the WRT_RDONLY bit is set.

16.2.1.4 HCCPARAMS—Host Controller Capability Parameters Register

Offset:	MEM_BASE + 08h–0Bh	Attribute:	RO
Default Value:	00006881h	Size:	32 bits

Bit	Description
31:18	Reserved
17	**Asynchronous Schedule Update Capability (ASUC)**—R/W. There is no functionality associated with this bit.
16	**Periodic Schedule Update Capability (PSUC)—**RO. This field is hardwired to 0b to indicate that the EHC hardware supports the Periodic Schedule Update Event Flag in the USB2.0_CMD register.
15:8	**EHCI Extended Capabilities Pointer (EECP)—**RO. This field is hardwired to 68h, indicating that the EHCI capabilities list exists and begins at offset 68h in the PCI configuration space.
7:4	**Isochronous Scheduling Threshold**—RO. This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit 7 is 0, the value of the least significant 3 bits indicates the number of micro-frames a host controller hold a set of isochronous data structures (one or more) before flushing the state. When bit 7 is a 1, then host software assumes the host controller may cache an isochronous data structure for an entire frame. Refer to the EHCI specification for details on how software uses this information for scheduling isochronous transfers. This field is hardwired to 8h.
3	Reserved.
2	**Asynchronous Schedule Park Capability**—RO. This bit is hardwired to 0 indicating that the host controller does not support this optional feature
1	**Programmable Frame List Flag**—RO. 0 = System software must use a frame list length of 1024 elements with this host controller. The USB2.0_CMD register (D29:F0, D26:F0:CAPLENGTH + 20h, bits 3:2) *Frame List Size* field is a read-only register and must be set to 0. 1 = System software can specify and use a smaller frame list and configure the host controller using the USB2.0_CMD register *Frame List Size* field. The frame list must always be aligned on a 4K page boundary. This requirement ensures that the frame list is always physically contiguous.
0	**64-bit Addressing Capability**—RO. This field documents the addressing range capability of this implementation. The value of this field determines whether software should use the 32-bit or 64-bit data structures. This bit is hardwired to 1. ***Note:*** The PCH supports 64 bit addressing only.

16.2.2 Host Controller Operational Registers

This section defines the enhanced host controller operational registers. These registers are located after the capabilities registers. The operational register base must be DWord-aligned and is calculated by adding the value in the first capabilities register (CAPLENGTH) to the base address of the enhanced host controller register address space (MEM_BASE). Since CAPLENGTH is always 20h, Table 16-3 already accounts for this offset. All registers are 32 bits in length.

Table 16-3. Enhanced Host Controller Operational Register Address Map

MEM_BASE + Offset	Mnemonic	Register Name	Default	Special Notes	Type
20h–23h	USB2.0_CMD	USB 2.0 Command	00080000h		R/W, RO
24h–27h	USB2.0_STS	USB 2.0 Status	00001000h		R/WC, RO
28h–2Bh	USB2.0_INTR	USB 2.0 Interrupt Enable	00000000h		R/W
2Ch–2Fh	FRINDEX	USB 2.0 Frame Index	00000000h		R/W,
30h–33h	CTRLDSSEGMENT	Control Data Structure Segment	00000000h		R/W, RO
34h–37h	PERODICLISTBASE	Period Frame List Base Address	00000000h		R/W
38h–3Bh	ASYNCLISTADDR	Current Asynchronous List Address	00000000h		R/W
3Ch–5Fh	—	Reserved	0h		RO
60h–63h	CONFIGFLAG	Configure Flag	00000000h	Suspend	R/W
64h–67h	PORT0SC	Port 0 Status and Control	00003000h	Suspend	R/W, R/WC, RO
68h–6Bh	PORT1SC	Port 1 Status and Control	00003000h	Suspend	R/W, R/WC, RO
6Ch–6Fh	PORT2SC	Port 2 Status and Control	00003000h	Suspend	R/W, R/WC, RO
70h–73h	PORT3SC	Port 3 Status and Control	00003000h	Suspend	R/W, R/WC, RO
74h–77h	PORT4SC	Port 4 Status and Control	00003000h	Suspend	R/W, R/WC, RO
78h–7Bh	PORT5SC	Port 5 Status and Control	00003000h	Suspend	R/W, R/WC, RO
74h–77h (D29 Only)	PORT6SC	Port 6 Status and Control	00003000h	Suspend	R/W, R/WC, RO
78h–7Bh (D29 Only)	PORT7SC	Port 7 Status and Control	00003000h	Suspend	R/W, R/WC, RO
7Ch–9Fh	—	Reserved	Undefined		RO
A0h–B3h	—	Debug Port Registers	Undefined		See register description
B4h–3FFh	—	Reserved	Undefined		RO

Note: Software must read and write these registers using only DWord accesses.These registers are divided into two sets. The first set at offsets MEM_BASE + 00:3Bh are implemented in the core power well. Unless otherwise noted, the core well registers are reset by the assertion of any of the following:

- Core well hardware reset
- HCRESET
- D3-to-D0 reset

The second set at offsets MEM_BASE + 60h to the end of the implemented register space are implemented in the Suspend power well. Unless otherwise noted, the suspend well registers are reset by the assertion of either of the following:

- Suspend well hardware reset
- HCRESET

16.2.2.1 USB2.0_CMD—USB 2.0 Command Register

Offset:	MEM_BASE + 20–23h	Attribute:	R/W, RO
Default Value:	00080000h	Size:	32 bits

Bit	Description
31:24	Reserved.
23:16	**Interrupt Threshold Control**—R/W. System software uses this field to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below. If software writes an invalid value to this register, the results are undefined. **Value** — **Maximum Interrupt Interval** 00h — Reserved 01h — 1 micro-frame 02h — 2 micro-frames 04h — 4 micro-frames 08h — 8 micro-frames (default, equates to 1 ms) 10h — 16 micro-frames (2 ms) 20h — 32 micro-frames (4 ms) 40h — 64 micro-frames (8 ms)
15:14	Reserved.
13	**Asynch Schedule Update (ASC)—**R/W. There is no functionality associated with this bit.
12	**Periodic Schedule Prefetch Enable**—R/W. This bit is used by software to enable the host controller to prefetch the periodic schedule even in C0. 0 = Prefetch based pause enabled only when not in C0. 1 = Prefetch based pause enable in C0. Once software has written a 1b to this bit to enable periodic schedule prefetching, it must disable prefecthing by writing a 0b to this bit whenever periodic schedule updates are about to begin. Software should continue to dynamically disable and re-enable the prefetcher surrounding any updates to the periodic scheduler (that is until the host controller has been reset using a HCRESET).
11:8	Unimplemented Asynchronous Park Mode Bits—RO. Hardwired to 000b indicating the host controller does not support this optional feature.
7	Light Host Controller Reset—RO. Hardwired to 0. The PCH does not implement this optional reset.
6	**Interrupt on Async Advance Doorbell**—R/W. This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. 0 = The host controller sets this bit to a 0 after it has set the Interrupt on Async Advance status bit (D29:F0, D26:F0:CAPLENGTH + 24h, bit 5) in the USB2.0_STS register to a 1. 1 = Software must write a 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USB2.0_STS register. If the *Interrupt on Async Advance Enable* bit in the USB2.0_INTR register (D29:F0, D26:F0:CAPLENGTH + 28h, bit 5) is a 1 then the host controller will assert an interrupt at the next interrupt threshold. See the EHCI specification for operational details. ***Note:*** Software should not write a 1 to this bit when the asynchronous schedule is inactive. Doing so will yield undefined results.
5	**Asynchronous Schedule Enable**—R/W. This bit controls whether the host controller skips processing the Asynchronous Schedule. 0 = Do not process the Asynchronous Schedule 1 = Use the ASYNCLISTADDR register to access the Asynchronous Schedule.
4	**Periodic Schedule Enable**—R/W. This bit controls whether the host controller skips processing the Periodic Schedule. 0 = Do not process the Periodic Schedule 1 = Use the PERIODICLISTBASE register to access the Periodic Schedule.

Bit	Description
3:2	**Frame List Size**—RO. The PCH hardwires this field to 00b because it only supports the 1024-element frame list size.
1	**Host Controller Reset (HCRESET)**—R/W. This control bit used by software to reset the host controller. The effects of this on root hub registers are similar to a Chip Hardware Reset (that is, RSMRST# assertion and PCH_PWROK deassertion on the PCH). When software writes a 1 to this bit, the host controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. ***Note:*** PCI configuration registers and Host controller capability registers are not effected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s), with the side effects described in the EHCI specification. Software must re-initialize the host controller in order to return the host controller to an operational state. This bit is set to 0 by the host controller when the reset process is complete. Software cannot terminate the reset process early by writing a 0 to this register. Software should not set this bit to a 1 when the HCHalted bit (D29:F0, D26:F0:CAPLENGTH + 24h, bit 12) in the USB2.0_STS register is a 0. Attempting to reset an actively running host controller will result in undefined behavior. This reset me be used to leave EHCI port test modes.
0	**Run/Stop (RS)**—R/W. 0 = Stop (default) 1 = Run. When set to a 1, the Host controller proceeds with execution of the schedule. The Host controller continues execution as long as this bit is set. When this bit is set to 0, the Host controller completes the current transaction on the USB and then halts. The HCHalted bit in the USB2.0_STS register indicates when the Host controller has finished the transaction and has entered the stopped state. Software should not write a 1 to this field unless the host controller is in the Halted state (that is, HCHalted in the USBSTS register is a 1). The Halted bit is cleared immediately when the Run bit is set. The following table explains how the different combinations of Run and Halted should be interpreted: **Run/Stop** / **Halted** / **Interpretation** 0b / 0b / In the process of halting 0b / 1b / Halted 1b / 0b / Running 1b / 1b / Invalid – the HCHalted bit clears immediately Memory read cycles initiated by the EHC that receive any status other than Successful will result in this bit being cleared.

Note: The Command Register indicates the command to be executed by the serial bus host controller. Writing to the register causes a command to be executed.

16.2.2.2 USB2.0_STS—USB 2.0 Status Register

Offset:	MEM_BASE + 24h–27h	Attribute:	R/WC, RO
Default Value:	00001000h	Size:	32 bits

This register indicates pending interrupts and various states of the Host controller. The status resulting from a transaction on the serial bus is not indicated in this register. See the Interrupts description in section 4 of the EHCI specification for additional information concerning USB 2.0 interrupt conditions.

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 has no effect.

Bit	Description
31:16	Reserved.
15	**Asynchronous Schedule Status** — RO. This bit reports the current real status of the Asynchronous Schedule. 0 = Disabled. (Default) 1 = Enabled. ***Note:*** The Host controller is not required to *immediately* disable or enable the Asynchronous Schedule when software transitions the *Asynchronous Schedule Enable* bit (D29:F0, D26:F0:CAPLENGTH + 20h, bit 5) in the USB2.0_CMD register. When this bit and the *Asynchronous Schedule Enable* bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
14	**Periodic Schedule Status** — RO. This bit reports the current real status of the Periodic Schedule. 0 = Disabled. (Default) 1 = Enabled. ***Note:*** The Host controller is not required to *immediately* disable or enable the Periodic Schedule when software transitions the *Periodic Schedule Enable* bit (D29:F0, D26:F0:CAPLENGTH + 20h, bit 4) in the USB2.0_CMD register. When this bit and the *Periodic Schedule Enable* bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	**Reclamation** — RO. This read-only status bit is used to detect an empty asynchronous schedule. The operational model and valid transitions for this bit are described in Section 4 of the EHCI Specification.
12	**HCHalted** — RO. 0 = This bit is a 0 when the Run/Stop bit is a 1. 1 = The Host controller sets this bit to 1 after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host controller hardware (such as, internal error). (Default)
11:6	Reserved
5	**Interrupt on Async Advance—**R/WC. System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a 1 to the *Interrupt on Async Advance Doorbell* bit (D29:F0, D26:F0:CAPLENGTH + 20h, bit 6) in the USB2.0_CMD register. This bit indicates the assertion of that interrupt source.
4	**Host System Error—**R/WC. 0 = No serious error occurred during a host system access involving the Host controller module 1 = The Host controller sets this bit to 1 when a serious error occurs during a host system access involving the Host controller module. A hardware interrupt is generated to the system. Memory read cycles initiated by the EHC that receive any status other than Successful will result in this bit being set. When this error occurs, the Host controller clears the Run/Stop bit in the USB2.0_CMDregister (D29:F0, D26:F0:CAPLENGTH + 20h, bit 0) to prevent further execution of the scheduled TDs. A hardware interrupt is generated to the system (if enabled in the Interrupt Enable Register).
3	**Frame List Rollover—**R/WC. 0 = No *Frame List Index* rollover from its maximum value to 0. 1 = The Host controller sets this bit to a 1 when the *Frame List Index* rolls over from its maximum value to 0. Since the PCH only supports the 1024-entry Frame List Size, the *Frame List Index* rolls over every time FRNUM13 toggles.

Bit	Description
2	**Port Change Detect—**R/WC. This bit is allowed to be maintained in the Auxiliary power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the EHCI HC device, this bit is loaded with the OR of all of the PORTSC change bits (including: Force port resume, overcurrent change, enable/disable change and connect status change). Regardless of the implementation, when this bit is readable (that is, in the D0 state), it must provide a valid view of the Port Status registers. 0 = No change bit transition from a 0 to 1 or No Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port. 1 = The Host controller sets this bit to 1 when any port for which the *Port Owner* bit is set to 0 has a change bit transition from a 0 to 1 or a Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port.
1	**USB Error Interrupt (USBERRINT)—**R/WC. 0 = No error condition. 1 = The Host controller sets this bit to 1 when completion of a USB transaction results in an error condition (such as DWord, error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit set, both this bit and Bit 0 are set. See the EHCI specification for a list of the USB errors that will result in this interrupt being asserted.
0	**USB Interrupt (USBINT)—**R/WC. 0 = No completion of a USB transaction whose Transfer Descriptor had its IOC bit set. No short packet is detected. 1 = The Host controller sets this bit to 1 when the cause of an interrupt is a completion of a USB transaction whose Transfer Descriptor had its IOC bit set. The Host controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes).

16.2.2.3 USB2.0_INTR—USB 2.0 Interrupt Enable Register

Offset:	MEM_BASE + 28h–2Bh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

This register enables and disables reporting of the corresponding interrupt to the software. When a bit is set and the corresponding interrupt is active, an interrupt is generated to the host. Interrupt sources that are disabled in this register still appear in the USB2.0_STS Register to allow the software to poll for events. Each interrupt enable bit description indicates whether it is dependent on the interrupt threshold mechanism (see Section 4 of the EHCI specification), or not.

Bit	Description
31:6	Reserved.
5	**Interrupt on Async Advance Enable—**R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the Interrupt on Async Advance bit (D29:F0, D26:F0:CAPLENGTH + 24h, bit 5) in the USB2.0_STS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
4	**Host System Error Enable—**R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the Host System Error Status bit (D29:F0, D26:F0:CAPLENGTH + 24h, bit 4) in the USB2.0_STS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	**Frame List Rollover Enable—**R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the Frame List Rollover bit (D29:F0, D26:F0:CAPLENGTH + 24h, bit 3) in the USB2.0_STS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	**Port Change Interrupt Enable—**R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the Port Change Detect bit (D29:F0, D26:F0:CAPLENGTH + 24h, bit 2) in the USB2.0_STS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Change Detect bit.
1	**USB Error Interrupt Enable—**R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the USBERRINT bit (D29:F0, D26:F0:CAPLENGTH + 24h, bit 1) in the USB2.0_STS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software by clearing the USBERRINT bit in the USB2.0_STS register.
0	**USB Interrupt Enable—**R/W. 0 = Disable. 1 = Enable. When this bit is a 1, and the USBINT bit (D29:F0, D26:F0:CAPLENGTH + 24h, bit 0) in the USB2.0_STS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software by clearing the USBINT bit in the USB2.0_STS register.

16.2.2.4 FRINDEX—Frame Index Register

Offset:	MEM_BASE + 2Ch–2Fh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

The SOF frame number value for the bus SOF token is derived or alternatively managed from this register. Refer to Section 4 of the EHCI specification for a detailed explanation of the SOF value management requirements on the host controller. The value of FRINDEX must be within 125 µs (1 micro-frame) ahead of the SOF token value. The SOF value may be implemented as an 11-bit shadow register. For this discussion, this shadow register is 11 bits and is named SOFV. SOFV updates every 8 micro-frames (1 millisecond). An example implementation to achieve this behavior is to increment SOFV each time the FRINDEX[2:0] increments from 0 to 1.

Software must use the value of FRINDEX to derive the current micro-frame number, both for high-speed isochronous scheduling purposes and to provide the **get** micro-frame number function required to client drivers. Therefore, the value of FRINDEX and the value of SOFV must be kept consistent if chip is reset or software writes to FRINDEX. Writes to FRINDEX must also **write-through** FRINDEX[13:3] to SOFV[10:0]. In order to keep the update as simple as possible, software should never write a FRINDEX value where the three least significant bits are 111b or 000b.

Note: This register is used by the host controller to index into the periodic frame list. The register updates every 125 microseconds (once each micro-frame). Bits [12:3] are used to select a particular entry in the Periodic Frame List during periodic schedule execution. The number of bits used for the index is fixed at 10 for the PCH since it only supports 1024-entry frame lists. This register must be written as a DWord. Word and byte writes produce undefined results. This register cannot be written unless the Host controller is in the Halted state as indicated by the *HCHalted* bit (D29:F0, D26:F0:CAPLENGTH + 24h, bit 12). A write to this register while the Run/Stop bit (D29:F0, D26:F0:CAPLENGTH + 20h, bit 0) is set to a 1 (USB2.0_CMD register) produces undefined results. Writes to this register also effect the SOF value. See Section 4 of the EHCI specification for details.

Bit	Description
31:14	Reserved
13:0	**Frame List Current Index/Frame Number**—R/W. The value in this register increments at the end of each time frame (e.g., micro-frame). Bits [12:3] are used for the Frame List current index. This means that each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index.

16.2.2.5 CTRLDSSEGMENT—Control Data Structure Segment Register

Offset:	MEM_BASE + 30h–33h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

This 32-bit register corresponds to the most significant address bits [63:32] for all EHCI data structures. Since the PCH hardwires the 64-bit Addressing Capability field in HCCPARAMS to 1, this register is used with the link pointers to construct 64-bit addresses to EHCI control data structures. This register is concatenated with the link pointer from either the PERIODICLISTBASE, ASYNCLISTADDR, or any control data structure link field to construct a 64-bit address. This register allows the host software to locate all control data structures within the same 4 GB memory segment.

Bit	Description
31:12	**Upper Address[63:44]**—RO. Hardwired to 0s. The PCH EHC is only capable of generating addresses up to 16 terabytes (44 bits of address).
11:0	**Upper Address[43:32]**—R/W. This 12-bit field corresponds to address bits 43:32 when forming a control data structure address.

16.2.2.6 PERIODICLISTBASE—Periodic Frame List Base Address Register

Offset:	MEM_BASE + 34h–37h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

This 32-bit register contains the beginning address of the Periodic Frame List in the system memory. Since the PCH host controller operates in 64-bit mode (as indicated by the 1 in the 64-bit Addressing Capability field in the HCCSPARAMS register) (offset 08h, bit 0), then the most significant 32 bits of every control data structure address comes from the CTRLDSSEGMENT register. HCD loads this register prior to starting the schedule execution by the host controller. The memory structure referenced by this physical memory pointer is assumed to be 4-Kbyte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host controller to step through the Periodic Frame List in sequence.

Bit	Description
31:12	**Base Address (Low)**—R/W. These bits correspond to memory address signals [31:12], respectively.
11:0	Reserved.

16.2.2.7 ASYNCLISTADDR—Current Asynchronous List Address Register

Offset:	MEM_BASE + 38h–3Bh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

This 32-bit register contains the address of the next asynchronous queue head to be executed. Since the PCH host controller operates in 64-bit mode (as indicated by a 1 in 64-bit Addressing Capability field in the HCCPARAMS register) (offset 08h, bit 0), then the most significant 32 bits of every control data structure address comes from the CTRLDSSEGMENT register (offset 08h). Bits [4:0] of this register cannot be modified by system software and will always return 0s when read. The memory structure referenced by this physical memory pointer is assumed to be 32-byte aligned.

Bit	Description
31:5	**Link Pointer Low (LPL)**—R/W. These bits correspond to memory address signals [31:5], respectively. This field may only reference a Queue Head (QH).
4:0	Reserved.

16.2.2.8 CONFIGFLAG—Configure Flag Register

Offset:	MEM_BASE + 60h–63h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

This register is in the suspend power well. It is only reset by hardware when the suspend power is initially applied or in response to a host controller reset.

Bit	Description
31:1	Reserved.
0	**Configure Flag (CF)**—R/W. Host software sets this bit as the last action in its process of configuring the Host controller. This bit controls the default port-routing control logic. Bit values and side-effects are listed below. See section 4 of the EHCI specification for operation details. 0 = Compatibility debug only (default). 1 = Port routing control logic default-routes all ports to this host controller.

16.2.2.9 PORTSC—Port N Status and Control Register

Offset:	Port 0 RMH: MEM_BASE + 64h–67h Port 1 Debug Port: MEM_BASE + 68–6Bh Port 2 USB redirect (if enabled): MEM_BASE + 6C–6Fh
Attribute:	R/W, R/WC, RO
Default Value:	00003000h
Size:	32 bits

Note: This register is associated with the upstream ports of the EHCI controller and does not represent downstream hub ports. USB Hub class commands must be used to determine RMH port status and enable test modes. See Chapter 11 of the USB Specification, Revision 2.0 for more details. Rate Matching Hub wake capabilities can be configured by the RMHWKCTL Register (RCBA+35B0h) located in the Chipset Configuration chapter.

A host controller must implement one or more port registers. Software uses the N_Port information from the Structural Parameters Register to determine how many ports need to be serviced. All ports have the structure defined below. Software must not write to unreported Port Status and Control Registers.

This register is in the suspend power well. It is only reset by hardware when the suspend power is initially applied or in response to a host controller reset. The initial conditions of a port are:

- No device connected
- Port disabled.

When a device is attached, the port state transitions to the attached state and system software will process this as with any status change notification. Refer to Section 4 of the EHCI specification for operational requirements for how change events interact with port suspend mode.

Bit	Description
31:23	Reserved.
22	**Wake on Overcurrent Enable (WKOC_E)—**R/W. 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1 enables the setting of the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the overcurrent Active bit (bit 4 of this register) is set.
21	**Wake on Disconnect Enable (WKDSCNNT_E)—**R/W. 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1 enables the setting of the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (that is, bit 0 of this register changes from 1 to 0).
20	**Wake on Connect Enable (WKCNNT_E)—**R/W. 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1 enables the setting of the PME Status bit in the Power Management Control/Status Register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (that is, bit 0 of this register changes from 0 to 1).
19:16	**Port Test Control—**R/W. When this field is 0s, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b – 1111b are reserved): **Value** — **Maximum Interrupt Interval** 0000b — Test mode not enabled (default) 0001b — Test J_STATE 0010b — Test K_STATE 0011b — Test SE0_NAK 0100b — Test Packet 0101b — FORCE_ENABLE Refer to the USB Specification Revision 2.0, Chapter 7 for details on each test mode.
15:14	Reserved.
13	**Port Owner—**R/W. This bit unconditionally goes to a 0 when the Configured Flag bit in the USB2.0_CMD register makes a 0 to 1 transition. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a 1 to this bit when the attached device is not a high-speed device. A 1 in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details.
12	**Port Power (PP)**—RO. Read-only with a value of 1. This indicates that the port does have power.
11:10	**Line Status**—RO.These bits reflect the current logical levels of the D+ (bit 11) and D– (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is 0 and the current connect status bit is set to a 1. 00 = SE0 10 = J-state 01 = K-state 11 = Undefined
9	Reserved.

Bit	Description
8	**Port Reset**—R/W. When software writes a 1 to this bit (from a 0), the bus reset sequence as defined in the USB Specification, Revision 2.0 is started. Software writes a 0 to this bit to terminate the bus reset sequence. Software must keep this bit at a 1 long enough to ensure the reset sequence completes as specified in the USB Specification, Revision 2.0. 1 = Port is in Reset. 0 = Port is not in Reset. ***Note:*** When software writes a 0 to this bit, there may be a delay before the bit status changes to a 0. The bit status will not read as a 0 until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g., set the *Port Enable* bit to a 1). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from 0 to 1. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2 ms of software writing this bit to a 0. The HCHalted bit (D29:F0, D26:F0:CAPLENGTH + 24h, bit 12) in the USB2.0_STS register should be a 0 before software attempts to use this bit. The host controller may hold Port Reset asserted to a 1 when the HCHalted bit is a 1. This bit is 0 if Port Power is 0 ***Note:*** System software should not attempt to reset a port if the *HCHalted* bit in the USB2.0_STS register is a 1. Doing so will result in undefined behavior.
7	**Suspend—**R/W. 0 = Port not in suspend state.(Default) 1 = Port in suspend state. Port Enabled Bit and Suspend bit of this register define the port states as follows: **Port Enabled** / **Suspend** / **Port State** 0 / X / Disabled 1 / 0 / Enabled 1 / 1 / Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port depending on the activity on the port. The host controller will unconditionally set this bit to a 0 when software sets the *Force Port Resume* bit to a 0 (from a 1). A write of 0 to this bit is ignored by the host controller. If host software sets this bit to a 1 when the port is not enabled (that is, Port enabled bit is a 0) the results are undefined.
6	**Force Port Resume—**R/W. 0 = No resume (K-state) detected/driven on port. (Default) 1 = Resume detected/driven on port. Software sets this bit to a 1 to drive resume signaling. The Host controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a 1 because a J-to-K transition is detected, the Port Change Detect bit (D29:F0, D26:F0:CAPLENGTH + 24h, bit 2) in the USB2.0_STS register is also set to a 1. If software sets this bit to a 1, the host controller must not set the Port Change Detect bit. ***Note:*** When the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification, Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a 1. Software must appropriately time the Resume and set this bit to a 0 when the appropriate amount of time has elapsed. Writing a 0 (from 1) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a 1 until the port has switched to the high-speed idle.
5	**Overcurrent Change—**R/WC. The functionality of this bit is not dependent upon the port owner. Software clears this bit by writing a 1 to it. 0 = No change. (Default) 1 = There is a change to Overcurrent Active.
4	**Overcurrent Active—**RO. 0 = This port does not have an overcurrent condition. (Default) 1 = This port currently has an overcurrent condition. This bit will automatically transition from 1 to 0 when the over current condition is removed. The PCH automatically disables the port when the overcurrent active bit is 1.

Bit	Description
3	**Port Enable / Disable Change**—R/WC. For the root hub, this bit gets set to a 1 only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it. 0 = No change in status. (Default). 1 = Port enabled/disabled status has changed.
2	**Port Enabled / Disabled**—R/W. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a 1 to this bit. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. 0 = Disable 1 = Enable (Default)
1	**Connect Status Change**—R/WC. This bit indicates a change has occurred in the port's Current Connect Status. Software sets this bit to 0 by writing a 1 to it. 0 = No change (Default). 1 = Change in Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit (that is, the bit will remain set).
0	**Current Connect Status**—RO. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. 0 = No device is present. (Default) 1 = Device is present on port.

16.2.3 USB 2.0-Based Debug Port Registers

The Debug port's registers are located in the same memory area, defined by the Base Address Register (MEM_BASE), as the standard EHCI registers. The base offset for the debug port registers (A0h) is declared in the Debug Port Base Offset Capability Register at Configuration offset 5Ah (D29:F0, D26:F0:offset 5Ah). The specific EHCI port that supports this debug capability (Port 1 for D29:F0 and Port 9 for D26:F0) is indicated by a 4-bit field (bits 20–23) in the HCSPARAMS register of the EHCI controller. The address map of the Debug Port registers is shown in Table 16-4.

Table 16-4. Debug Port Register Address Map

MEM_BASE + Offset	Mnemonic	Register Name	Default	Type
A0–A3h	CNTL_STS	Control/Status	00000000h	R/W, R/WC, RO
A4–A7h	USBPID	USB PIDs	00000000h	R/W, RO
A8–AFh	DATABUF[7:0]	Data Buffer (Bytes 7:0)	00000000 00000000h	R/W
B0–B3h	CONFIG	Configuration	00007F01h	R/W

Notes:
1. All of these registers are implemented in the core well and reset by PLTRST#, EHC HCRESET, and a EHC D3-to-D0 transition.
2. The hardware associated with this register provides no checks to ensure that software programs the interface correctly. How the hardware behaves when programmed improperly is undefined.

16.2.3.1 CNTL_STS—Control/Status Register

Offset:	MEM_BASE + A0h	Attribute:	R/W, R/WC, RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31	Reserved
30	**OWNER_CNT—**R/W. 0 = Ownership of the debug port is NOT forced to the EHCI controller (Default) 1 = Ownership of the debug port is forced to the EHCI controller (that is, immediately taken away from the companion Classic USB Host controller) If the port was already owned by the EHCI controller, then setting this bit has no effect. This bit overrides all of the ownership-related bits in the standard EHCI registers.
29	Reserved
28	**ENABLED_CNT—**R/W. 0 = Software can clear this by writing a 0 to it. The hardware clears this bit for the same conditions where the Port Enable/Disable Change bit (in the PORTSC register) is set. (Default) 1 = Debug port is enabled for operation. Software can directly set this bit if the port is already enabled in the associated PORTSC register (this is enforced by the hardware).
27:17	Reserved
16	**DONE_STS—**R/WC. Software can clear this by writing a 1 to it. 0 = Request Not complete 1 = Set by hardware to indicate that the request is complete.
15:12	LINK_ID_STS—RO. This field identifies the link interface. 0h = Hardwired. Indicates that it is a USB Debug Port.
11	Reserved.
10	**IN_USE_CNT—**R/W. Set by software to indicate that the port is in use. Cleared by software to indicate that the port is free and may be used by other software. This bit is cleared after reset. (This bit has no affect on hardware.)
9:7	**EXCEPTION_STS—**RO. This field indicates the exception when the ERROR_GOOD#_STS bit is set. This field should be ignored if the ERROR_GOOD#_STS bit is 0. 000 = No Error. (Default) ***Note:*** This should not be seen since this field should only be checked if there is an error. 001 = Transaction error: Indicates the USB 2.0 transaction had an error (CRC, bad PID, timeout, etc.) 010 = Hardware error. Request was attempted (or in progress) when port was suspended or reset. All Other combinations are reserved
6	**ERROR_GOOD#_STS—**RO. 0 = Hardware clears this bit to 0 after the proper completion of a read or write. (Default) 1 = Error has occurred. Details on the nature of the error are provided in the Exception field.
5	**GO_CNT—**R/W. 0 = Hardware clears this bit when hardware sets the DONE_STS bit. (Default) 1 = Causes hardware to perform a read or write request. ***Note:*** Writing a 1 to this bit when it is already set may result in undefined behavior.
4	**WRITE_READ#_CNT—**R/W. Software clears this bit to indicate that the current request is a read. Software sets this bit to indicate that the current request is a write. 0 = Read (Default) 1 = Write
3:0	**DATA_LEN_CNT—**R/W. This field is used to indicate the size of the data to be transferred. default = 0h. For write operations, this field is set by software to indicate to the hardware how many bytes of data in Data Buffer are to be transferred to the console. A value of 0h indicates that a zero-length packet should be sent. A value of 1–8 indicates 1–8 bytes are to be transferred. Values 9–Fh are invalid and how hardware behaves if used is undefined. For read operations, this field is set by hardware to indicate to software how many bytes in Data Buffer are valid in response to a read operation. A value of 0h indicates that a zero length packet was returned and the state of Data Buffer is not defined. A value of 1–8 indicates 1–8 bytes were received. Hardware is not allowed to return values 9–Fh. The transferring of data always starts with byte 0 in the data area and moves toward byte 7 until the transfer size is reached.

Notes:
1. Software should do Read-Modify-Write operations to this register to preserve the contents of bits not being modified. This include Reserved bits.
2. To preserve the usage of RESERVED bits in the future, software should always write the same value read from the bit until it is defined. Reserved bits will always return 0 when read.

16.2.3.2 USBPID—USB PIDs Register

Offset:	MEM_BASE + A4h–A7h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

This Dword register is used to communicate PID information between the USB debug driver and the USB debug port. The debug port uses some of these fields to generate USB packets, and uses other fields to return PID information to the USB debug driver.

Bit	Description
31:24	Reserved.
23:16	**RECEIVED_PID_STS[23:16]**—RO. Hardware updates this field with the received PID for transactions in either direction. When the controller is writing data, this field is updated with the handshake PID that is received from the device. When the host controller is reading data, this field is updated with the data packet PID (if the device sent data), or the handshake PID (if the device NAKs the request). This field is valid when the hardware clears the GO_DONE#_CNT bit.
15:8	**SEND_PID_CNT[15:8]**—R/W. Hardware sends this PID to begin the data packet when sending data to USB (that is, WRITE_READ#_CNT is asserted). Software typically sets this field to either DATA0 or DATA1 PID values.
7:0	**TOKEN_PID_CNT[7:0]**—R/W. Hardware sends this PID as the Token PID for each USB transaction. Software typically sets this field to either IN, OUT, or SETUP PID values.

16.2.3.3 DATABUF[7:0]—Data Buffer Bytes[7:0] Register

Offset:	MEM_BASE + A8h–AFh	Attribute:	R/W
Default Value:	0000000000000000h	Size:	64 bits

This register can be accessed as 8 separate 8-bit registers or 2 separate 32-bit register.

Bit	Description
63:0	**DATABUFFER[63:0]**—R/W. This field is the 8 bytes of the data buffer. Bits 7:0 correspond to least significant byte (byte 0). Bits 63:56 correspond to the most significant byte (byte 7). The bytes in the Data Buffer must be written with data before software initiates a write request. For a read request, the Data Buffer contains valid data when DONE_STS bit (offset A0, bit 16) is cleared by the hardware, ERROR_GOOD#_STS (offset A0, bit 6) is cleared by the hardware, and the DATA_LENGTH_CNT field (offset A0, bits 3:0) indicates the number of bytes that are valid.

16.2.3.4 CONFIG—Configuration Register

Offset:	MEM_BASE + B0–B3h	Attribute:	R/W
Default Value:	00007F01h	Size:	32 bits

Bit	Description
31:15	Reserved
14:8	**USB_ADDRESS_CNF**—R/W. This 7-bit field identifies the USB device address used by the controller for all Token PID generation. (Default = 7Fh)
7:4	Reserved
3:0	**USB_ENDPOINT_CNF**—R/W. This 4-bit field identifies the endpoint used by the controller for all Token PID generation. (Default = 1h)

§

17 Intel® High Definition Audio Controller Registers (D27:F0)

The Intel® High Definition Audio (Intel® HD Audio) controller resides in PCI Device 27, Function 0 on bus 0. This function contains a set of DMA engines that are used to move samples of digitally encoded data between system memory and external codecs.

Note: All registers in this function (including memory-mapped registers) must be addressable in byte, word, and DWord quantities. The software must always make register accesses on natural boundaries (that is, DWord accesses must be on DWord boundaries; word accesses on word boundaries, and so forth) Register access crossing the DWord boundary are ignored. In addition, the memory-mapped register space must not be accessed with the LOCK semantic exclusive-access mechanism. If software attempts exclusive-access mechanisms to the Intel HD Audio memory-mapped space, the results are undefined.

Note: Users interested in providing feedback on the Intel HD Audio specification or planning to implement the Intel HD Audio specification into a future product will need to execute the *Intel® High Definition Audio Specification Developer's Agreement*. For more information, contact nextgenaudio@intel.com.

17.1 Intel® HD Audio PCI Configuration Space (Intel® HD Audio—D27:F0)

Note: Address locations that are not shown should be treated as Reserved.

Table 17-1. Intel® High Definition Audio PCI Register Address Map (Intel HD Audio D27:F0) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Access
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0010h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	03h	RO
0Bh	BCC	Base Class Code	04h	RO
0Ch	CLS	Cache Line Size	00h	R/W
0Dh	LT	Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	00h	RO
10h–13h	HDBARL	Intel HD Audio Lower Base Address (Memory)	00000004h	R/W, RO
14h–17h	HDBARU	Intel HD Audio Upper Base Address (Memory)	00000000h	R/W
2Ch–2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2Eh–2Fh	SID	Subsystem Identification	0000h	R/WO
34h	CAPPTR	Capability List Pointer	50h	RO
3Ch	INTLN	Interrupt Line	00h	R/W
3Dh	INTPN	Interrupt Pin	See Register Description	RO

Table 17-1. Intel® High Definition Audio PCI Register Address Map (Intel HD Audio D27:F0) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Access
40h	HDCTL	Intel HD Audio Control	01h	R/W, RO
43h	HDINIT1	Intel High Definition Audio Initialization	07h	RO
4Ch–4Dh		Reserved	0000h	RO
50h–51h	PID	PCI Power Management Capability ID	6001h	R/WO, RO
52h–53h	PC	Power Management Capabilities	C842h	RO
54h–57h	PCS	Power Management Control and Status	00000000h	R/W, RO, R/WC
60h–61h	MID	MSI Capability ID	7005h	RO
62h–63h	MMC	MSI Message Control	0080h	R/W, RO
64h–67h	MMLA	MSI Message Lower Address	00000000h	R/W, RO
68h–6Bh	MMUA	MSI Message Upper Address	00000000h	R/W
6Ch–6Dh	MMD	MSI Message Data	0000h	R/W
70h–71h	PXID	PCI Express Capability Identifiers	0010h	RO
72h–73h	PXC	PCI Express Capabilities	0091h	RO
74h–77h	DEVCAP	Device Capabilities	10000000h	RO, R/WO
78h–79h	DEVC	Device Control	0800h	R/W, RO
7Ah–7Bh	DEVS	Device Status	0010h	RO
100h–103h	VCCAP	Virtual Channel Enhanced Capability Header	13010002h	R/WO
104h–107h	PVCCAP1	Port VC Capability Register 1	00000001h	RO
108h–10Bh	PVCCAP2	Port VC Capability Register 2	00000000h	RO
10Ch–10D	PVCCTL	Port VC Control	0000h	RO
10Eh–10Fh	PVCSTS	Port VC Status	0000h	RO
110h–113h	VC0CAP	VC0 Resource Capability	00000000h	RO
114h–117h	VC0CTL	VC0 Resource Control	800000FFh	R/W, RO
11Ah–11Bh	VC0STS	VC0 Resource Status	0000h	RO
11Ch–11Fh	VCiCAP	VCi Resource Capability	00000000h	RO
120h–123h	VCiCTL	VCi Resource Control	00000000h	R/W, RO
126h–127h	VCiSTS	VCi Resource Status	0000h	RO
130h–133h	RCCAP	Root Complex Link Declaration Enhanced Capability Header	00010005h	RO
134h–137h	ESD	Element Self Description	0F000100h	RO
140h–143h	L1DESC	Link 1 Description	00000001h	RO
148h–14Bh	L1ADDL	Link 1 Lower Address	See Register Description	RO
14Ch–14Fh	L1ADDU	Link 1 Upper Address	00000000h	RO

17.1.1 VID—Vendor Identification Register (Intel® HD Audio Controller—D27:F0)

Offset:	00h–01h	Attribute:	RO
Default Value:	8086h	Size:	16 bits

Bit	Description
15:0	**Vendor ID**—RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

17.1.2 DID—Device Identification Register (Intel® High Definition Audio Controller—D27:F0)

Offset Address:	02h–03h	Attribute:	RO
Default Value:	See bit description	Size:	16 bits

Bit	Description
15:0	**Device ID**—RO. This is a 16-bit value assigned to the PCH's Intel High Definition Audio controller. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Device ID Register.

17.1.3 PCICMD—PCI Command Register (Intel® HD Audio Controller—D27:F0)

Offset Address:	04h–05h	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable (ID)—**R/W. 0= The INTx# signals may be asserted. 1= The Intel HD Audio controller's INTx# signal will be de-asserted. ***Note:*** This bit does not affect the generation of MSIs.
9	Fast Back to Back Enable (FBE)—RO. Not implemented. Hardwired to 0.
8	**SERR# Enable (SERR_EN)—**R/W. SERR# is not generated by the PCH's Intel HD Audio Controller.
7	Wait Cycle Control (WCC)—RO. Not implemented. Hardwired to 0.
6	Parity Error Response (PER)—R/W. PER functionality not implemented.
5	VGA Palette Snoop (VPS). Not implemented. Hardwired to 0.
4	Memory Write and Invalidate Enable (MWIE)—RO. Not implemented. Hardwired to 0.
3	Special Cycle Enable (SCE). Not implemented. Hardwired to 0.
2	**Bus Master Enable (BME)**—R/W. Controls standard PCI Express* bus mastering capabilities for Memory and I/O, reads and writes. Note that this bit also controls MSI generation since MSI's are essentially Memory writes. 0 = Disable 1 = Enable
1	**Memory Space Enable (MSE)—**R/W. Enables memory space addresses to the Intel HD Audio controller. 0 = Disable 1 = Enable
0	I/O Space Enable (IOSE)—RO. Hardwired to 0 since the Intel HD Audio controller does not implement I/O space.

17.1.4 PCISTS—PCI Status Register (Intel® HD Audio Controller—D27:F0)

Offset Address:	06h–07h	Attribute:	RO, R/WC
Default Value:	0010h	Size:	16 bits

Bit	Description
15	Detected Parity Error (DPE)—RO. Not implemented. Hardwired to 0.
14	SERR# Status (SERRS)—RO. Not implemented. Hardwired to 0.
13	**Received Master Abort (RMA)—**R/WC. Software clears this bit by writing a 1 to it. 0 = No master abort received. 1 = The Intel High Definition Audio controller sets this bit when, as a bus master, it receives a master abort. When set, the Intel® High Definition Audio controller clears the run bit for the channel that received the abort.
12	Received Target Abort (RTA)—RO. Not implemented. Hardwired to 0.
11	Signaled Target Abort (STA)—RO. Not implemented. Hardwired to 0.
10:9	DEVSEL# Timing Status (DEV_STS)—RO. Does not apply. Hardwired to 0.
8	Data Parity Error Detected (DPED)—RO. Not implemented. Hardwired to 0.
7	Fast Back to Back Capable (FB2BC)—RO. Does not apply. Hardwired to 0.
6	Reserved
5	66 MHz Capable (66MHZ_CAP)—RO. Does not apply. Hardwired to 0.
4	**Capabilities List (CAP_LIST)—**RO. Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
3	**Interrupt Status (IS)**—RO. 0 = This bit is 0 after the interrupt is cleared. 1 = This bit is 1 when the INTx# is asserted. Note that this bit is not set by an MSI.
2:0	Reserved

17.1.5 RID—Revision Identification Register (Intel® HD Audio Controller—D27:F0)

Offset:	08h	Attribute:	RO
Default Value:	See bit description	Size:	8 Bits

Bit	Description
7:0	**Revision ID**—RO. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Revision ID Register.

17.1.6 PI—Programming Interface Register (Intel® HD Audio Controller—D27:F0)

Offset:	09h	Attribute:	RO
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	**Programming Interface**—RO.

17.1.7 SCC—Sub Class Code Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 0Ah Attribute: RO
Default Value: 03h Size: 8 bits

Bit	Description
7:0	**Sub Class Code (SCC)**—RO. 03h = Audio Device

17.1.8 BCC—Base Class Code Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 0Bh Attribute: RO
Default Value: 04h Size: 8 bits

Bit	Description
7:0	**Base Class Code (BCC)**—RO. 04h = Multimedia device

17.1.9 CLS—Cache Line Size Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 0Ch Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Cache Line Size**—R/W. Implemented as R/W register, but has no functional impact to the PCH

17.1.10 LT—Latency Timer Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 0Dh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	Latency Timer—RO. Hardwired to 00

17.1.11 HEADTYP—Header Type Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 0Eh Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	Header Type—RO. Hardwired to 00.

17.1.12 HDBARL—Intel® HD Audio Lower Base Address Register (Intel® HD Audio—D27:F0)

Address Offset: 10h–13h
Attribute: R/W, RO
Default Value: 00000004h
Size: 32 bits

Bit	Description
31:14	**Lower Base Address (LBA)—**R/W. Base address for the Intel HD Audio controller's memory mapped configuration registers. 16 Kbytes are requested by hardwiring bits 13:4 to 0s.
13:4	Reserved
3	Prefetchable (PREF)—RO. Hardwired to 0 to indicate that this BAR is NOT prefetchable
2:1	**Address Range (ADDRNG)**—RO. Hardwired to 10b, indicating that this BAR can be located anywhere in 64-bit address space.
0	**Space Type (SPTYP)**—RO. Hardwired to 0. Indicates this BAR is located in memory space.

17.1.13 HDBARU—Intel® HD Audio Upper Base Address Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 14h–17h
Attribute: R/W
Default Value: 00000000h
Size: 32 bits

Bit	Description
31:0	**Upper Base Address (UBA)—**R/W. Upper 32 bits of the Base address for the Intel High Definition Audio controller's memory mapped configuration registers.

17.1.14 SVID—Subsystem Vendor Identification Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 2Ch–2Dh
Attribute: R/WO
Default Value: 0000h
Size: 16 bits
Function Level Reset: No

The SVID register, in combination with the Subsystem ID register (D27:F0:2Eh), enable the operating environment to distinguish one audio subsystem from the other(s).

This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

This register is not affected by the $D3_{HOT}$ to D0 transition.

Bit	Description
15:0	**Subsystem Vendor ID**—R/WO.

17.1.15 SID—Subsystem Identification Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 2Eh–2Fh Attribute: R/WO
Default Value: 0000h Size: 16 bits
Function Level Reset: No

The SID register, in combination with the Subsystem Vendor ID register (D27:F0:2Ch) make it possible for the operating environment to distinguish one audio subsystem from the other(s).

This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

This register is not affected by the $D3_{HOT}$ to D0 transition.

Bit	Description
15:0	**Subsystem ID—**R/WO.

17.1.16 CAPPTR—Capabilities Pointer Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 34h Attribute: RO
Default Value: 50h Size: 8 bits

This register indicates the offset for the capability pointer.

Bit	Description
7:0	**Capabilities Pointer (CAP_PTR)**—RO. This field indicates that the first capability pointer offset is offset 50h (Power Management Capability)

17.1.17 INTLN—Interrupt Line Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 3Ch Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN)—**R/W. This data is not used by the PCH. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

17.1.18 INTPN—Interrupt Pin Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 3Dh Attribute: RO
Default Value: See Description Size: 8 bits

Bit	Description
7:4	Reserved
3:0	**Interrupt Pin**—RO. This reflects the value of D27IP.ZIP (Chipset Config Registers:Offset 3110h:bits 3:0).

17.1.19 HDCTL—Intel® HD Audio Control Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 40h
Attribute: RO
Default Value: 01h
Size: 8 bits

Bit	Description
7:1	Reserved
0	**Intel High Definition Signal Mode**—RO. This bit is hardwired to 1 (High Definition Audio mode)

17.1.20 HDINIT1—Intel® High Definition Audio Initialization Register 1 (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 43h
Attribute: RO
Default Value: 07h
Size: 8 bits

Bit	Description
7:3	Reserved
2:0	**HDINIT1 Field 1**—R/W. BIOS must program this field to 101b.

17.1.21 PID—PCI Power Management Capability ID Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 50h–51h
Attribute: R/WO, RO
Default Value: 6001h
Size: 16 bits
Function Level Reset: No (Bits 7:0 only)

Bit	Description
15:8	**Next Capability (Next)**—R/WO. Points to the next capability structure (MSI).
7:0	**Cap ID (CAP)**—RO. Hardwired to 01h. Indicates that this pointer is a PCI power management capability. These bits are not reset by Function Level Reset.

17.1.22 PC—Power Management Capabilities Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 52h–53h
Attribute: RO
Default Value: C842h
Size: 16 bits

Bit	Description
15:11	**PME Support**—RO. Hardwired to 11001b. Indicates PME# can be generated from D3 and D0 states.
10	D2 Support—RO. Hardwired to 0. Indicates that D2 state is not supported.
9	D1 Support—RO. Hardwired to 0. Indicates that D1 state is not supported.
8:6	**Aux Current**—RO. Hardwired to 001b. Reports 55 mA maximum suspend well current required when in the $D3_{COLD}$ state.
5	Device Specific Initialization (DSI)—RO. Hardwired to 0. Indicates that no device specific initialization is required.
4	Reserved
3	PME Clock (PMEC)—RO. Does not apply. Hardwired to 0.
2:0	**Version**—RO. Hardwired to 010b. Indicates support for version 1.1 of the PCI Power Management Specification.

17.1.23 PCS—Power Management Control and Status Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 54h–57h
Attribute: RO, R/W, R/WC
Default Value: 00000000h
Size: 32 bits
Function Level Reset: No

Bit	Description
31:24	**Data**—RO. Does not apply. Hardwired to 0.
23	Bus Power/Clock Control Enable—RO. Does not apply. Hardwired to 0.
22	B2/B3 Support—RO. Does not apply. Hardwired to 0.
21:16	Reserved
15	**PME Status (PMES)—**R/WC. 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the Intel HD Audio controller would normally assert the PME# signal independent of the state of the PME_EN bit (bit 8 in this register). This bit is in the resume well and is cleared by a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
14:9	Reserved
8	**PME Enable (PMEE)—**R/W. 0 = Disable 1 = When set and if corresponding PMES also set, the Intel HD Audio controller sets the PME_B0_STS bit in the GPE0_STS register (PMBASE +28h). This bit in the resume well and is cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
7:2	Reserved

Bit	Description
1:0	**Power State (PS)—**R/W. This field is used both to determine the current power state of the Intel High Definition Audio controller and to set a new power state. 00 = D0 state 11 = $D3_{HOT}$ state Others = reserved ***Notes:*** 1. If software attempts to write a value of 01b or 10b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. 2. When in the $D3_{HOT}$ states, the Intel HD Audio controller's configuration space is available, but the IO and memory space are not. Additionally, interrupts are blocked. 3. When software changes this value from $D3_{HOT}$ state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function.

17.1.24 MID—MSI Capability ID Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 60h–61h Attribute: RO
Default Value: 7005h Size: 16 bits

Bit	Description
15:8	**Next Capability (Next)**—RO. Hardwired to 70h. Points to the PCI Express capability structure.
7:0	**Cap ID (CAP)—**RO. Hardwired to 05h. Indicates that this pointer is a MSI capability

17.1.25 MMC—MSI Message Control Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 62h–63h Attribute: RO, R/W
Default Value: 0080h Size: 16 bits

Bit	Description
15:8	Reserved
7	**64b Address Capability (64ADD)**—RO. Hardwired to 1. Indicates the ability to generate a 64-bit message address
6:4	Multiple Message Enable (MME)—RO. Normally this is a R/W register. However since only 1 message is supported, these bits are hardwired to 000 = 1 message.
3:1	Multiple Message Capable (MMC)—RO. Hardwired to 0 indicating request for 1 message.
0	**MSI Enable (ME)—**R/W. 0 = an MSI may not be generated 1 = an MSI will be generated instead of an INTx signal.

17.1.26 MMLA—MSI Message Lower Address Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 64h–67h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:2	**Message Lower Address (MLA)—**R/W. Lower address used for MSI message.
1:0	Reserved

17.1.27 MMUA—MSI Message Upper Address Register (Intel® HD Audio Controller—D27:F0)

Address Offset:	68h–6Bh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	**Message Upper Address (MUA)—**R/W. Upper 32-bits of address used for MSI message.

17.1.28 MMD—MSI Message Data Register (Intel® HD Audio Controller—D27:F0)

Address Offset:	6Ch–6Dh	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15:0	**Message Data (MD)—**R/W. Data used for MSI message.

17.1.29 PXID—PCI Express* Capability ID Register (Intel® HD Audio Controller—D27:F0)

Address Offset:	70h–71h	Attribute:	RO
Default Value:	0010h	Size:	16 bits

Bit	Description
15:8	**Next Capability (Next)**—RO. Hardwired to 0. Indicates that this is the last capability structure in the list.
7:0	**Cap ID (CAP)**—RO. Hardwired to 10h. Indicates that this pointer is a PCI Express capability structure.

17.1.30 PXC—PCI Express* Capabilities Register (Intel® HD Audio Controller—D27:F0)

Address Offset:	72h–73h	Attribute:	RO
Default Value:	0091h	Size:	16 bits

Bit	Description
15:14	Reserved
13:9	Interrupt Message Number (IMN)—RO. Hardwired to 0.
8	Slot Implemented (SI)—RO. Hardwired to 0.
7:4	**Device/Port Type (DPT)—**RO. Hardwired to 1001b. Indicates that this is a Root Complex Integrated endpoint device.
3:0	**Capability Version (CV)**—RO. Hardwired to 0001b. Indicates version #1 PCI Express capability

17.1.31 DEVCAP—Device Capabilities Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 74h–77h
Attribute: R/WO, RO
Default Value: 10000000h
Size: 32 bits
Function Level Reset: No

Bit	Description
31:29	Reserved
28	**Function Level Reset (FLR)—**R/WO. A 1 indicates that the PCH Intel HD Audio Controller supports the Function Level Reset Capability.
27:26	Captured Slot Power Limit Scale (SPLS)—RO. Hardwired to 0.
25:18	Captured Slot Power Limit Value (SPLV)—RO. Hardwired to 0.
17:15	Reserved
14	Power Indicator Present—RO. Hardwired to 0.
13	Attention Indicator Present—RO. Hardwired to 0.
12	Attention Button Present—RO. Hardwired to 0.
11:9	Endpoint L1 Acceptable Latency—R/WO.
8:6	**Endpoint L0s Acceptable Latency**—R/WO.
5	**Extended Tag Field Support**—RO. Hardwired to 0. Indicates 5-bit tag field support
4:3	Phantom Functions Supported—RO. Hardwired to 0. Indicates that phantom functions not supported
2:0	**Max Payload Size Supported**—RO. Hardwired to 0. Indicates 128-B maximum payload size capability

17.1.32 DEVC—Device Control Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 78h–79h
Attribute: R/W, RO
Default Value: 0800h
Size: 16 bits
Function Level Reset: No (Bit 11 Only)

Bit	Description
15	**Initiate FLR (IF)**—R/W. This bit is used to initiate FLR transition. 1 = A write of 1 initiates FLR transition. Since hardware does not respond to any cycles until FLR completion, the read value by software from this bit is 0.
14:12	Max Read Request Size—RO. Hardwired to 0 enabling 128B maximum read request size.
11	**No Snoop Enable (NSNPEN)—**R/W. 0 = The Intel HD Audio controller will not set the No Snoop bit. In this case, isochronous transfers will not use VC1 (VCi) even if it is enabled since VC1 is never snooped. Isochronous transfers will use VC0. 1 = The Intel® High Definition Audio controller is permitted to set the No Snoop bit in the Requester Attributes of a bus master transaction. In this case, VC0 or VC1 may be used for isochronous transfers. ***Note:*** This bit is not reset on $D3_{HOT}$ to D0 transition; however, it is reset by PLTRST#. This bit is not reset by Function Level Reset.
10	Auxiliary Power Enable—RO. Hardwired to 0, indicating that Intel HD Audio device does not draw AUX power
9	Phantom Function Enable—RO. Hardwired to 0 disabling phantom functions.
8	**Extended Tag Field Enable**—RO. Hardwired to 0 enabling 5-bit tag.
7:5	**Max Payload Size**—RO. Hardwired to 0 indicating 128B.
4	Enable Relaxed Ordering—RO. Hardwired to 0 disabling relaxed ordering.
3	Unsupported Request Reporting Enable—R/W. Not implemented.
2	Fatal Error Reporting Enable—R/W. Not implemented.
1	Non-Fatal Error Reporting Enable—R/W. Not implemented.
0	Correctable Error Reporting Enable—R/W. Not implemented.

17.1.33 DEVS—Device Status Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 7Ah–7Bh
Attribute: RO
Default Value: 0010h
Size: 16 bits

Bit	Description
15:6	Reserved
5	**Transactions Pending—**RO. 0 = Indicates that completions for all non-posted requests have been received 1 = Indicates that Intel High Definition Audio controller has issued non-posted requests which have not been completed.
4	**AUX Power Detected**—RO. Hardwired to 1 indicating the device is connected to resume power
3	Unsupported Request Detected—RO. Not implemented. Hardwired to 0.
2	Fatal Error Detected—RO. Not implemented. Hardwired to 0.
1	Non-Fatal Error Detected—RO. Not implemented. Hardwired to 0.
0	Correctable Error Detected—RO. Not implemented. Hardwired to 0.

17.1.34 VCCAP—Virtual Channel Enhanced Capability Header (Intel® HD Audio Controller—D27:F0)

Address Offset:	100h–103h	Attribute:	R/WO
Default Value:	13010002h	Size:	32 bits

Bit	Description
31:20	**Next Capability Offset**—R/WO. Points to the next capability header. 130h = Root Complex Link Declaration Enhanced Capability Header 000h = Root Complex Link Declaration Enhanced Capability Header is not supported.
19:16	**Capability Version—**R/WO. 0h =PCI Express Virtual channel capability and the Root Complex Topology Capability structure are not supported. 1h =PCI Express Virtual channel capability and the Root Complex Topology Capability structure are supported.
15:0	**PCI Express Extended Capability**—R/WO. 0000h =PCI Express Virtual channel capability and the Root Complex Topology Capability structure are not supported. 0002h =PCI Express Virtual channel capability and the Root Complex Topology Capability structure are supported.

17.1.35 PVCCAP1—Port VC Capability Register 1 (Intel® HD Audio Controller—D27:F0)

Address Offset:	104h–107h	Attribute:	RO
Default Value:	00000001h	Size:	32 bits

Bit	Description
31:12	Reserved
11:10	Port Arbitration Table Entry Size—RO. Hardwired to 0 since this is an endpoint device.
9:8	Reference Clock—RO. Hardwired to 0 since this is an endpoint device.
7	Reserved
6:4	Low Priority Extended VC Count—RO. Hardwired to 0. Indicates that only VC0 belongs to the low priority VC group
3	Reserved
2:0	**Extended VC Count**—RO. Hardwired to 001b. Indicates that 1 extended VC (in addition to VC0) is supported by the Intel HD Audio controller.

17.1.36 PVCCAP2—Port VC Capability Register 2 (Intel® HD Audio Controller—D27:F0)

Address Offset:	108h–10Bh	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:24	VC Arbitration Table Offset—RO. Hardwired to 0 indicating that a VC arbitration table is not present.
23:8	Reserved
7:0	VC Arbitration Capability—RO. Hardwired to 0. These bits are not applicable since the Intel HD Audio controller reports a 0 in the Low Priority Extended VC Count bits in the PVCCAP1 register.

17.1.37 PVCCTL—Port VC Control Register (Intel® HD Audio Controller—D27:F0)

Address Offset:	10Ch–10Dh	Attribute:	RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:4	Reserved
3:1	VC Arbitration Select—RO. Hardwired to 0. Normally these bits are R/W. However, these bits are not applicable since the Intel HD Audio controller reports a 0 in the Low Priority Extended VC Count bits in the PVCCAP1 register
0	Load VC Arbitration Table—RO. Hardwired to 0 since an arbitration table is not present.

17.1.38 PVCSTS—Port VC Status Register (Intel® HD Audio Controller—D27:F0)

Address Offset:	10Eh–10Fh	Attribute:	RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:1	Reserved
0	VC Arbitration Table Status—RO. Hardwired to 0 since an arbitration table is not present.

17.1.39 VC0CAP—VC0 Resource Capability Register (Intel® HD Audio Controller—D27:F0)

Address Offset:	110h–113h	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:24	Port Arbitration Table Offset—RO. Hardwired to 0 since this field is not valid for endpoint devices
23	Reserved
22:16	Maximum Time Slots—RO. Hardwired to 0 since this field is not valid for endpoint devices
15	Reject Snoop Transactions—RO. Hardwired to 0 since this field is not valid for endpoint devices.
14	Advanced Packet Switching—RO. Hardwired to 0 since this field is not valid for endpoint devices
13:8	Reserved
7:0	Port Arbitration Capability—RO. Hardwired to 0 since this field is not valid for endpoint devices

17.1.40 VC0CTL—VC0 Resource Control Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 114h–117h
Attribute: R/W, RO
Default Value: 800000FFh
Size: 32 bits
Function Level Reset: No

Bit	Description
31	VC0 Enable—RO. Hardwired to 1 for VC0.
30:27	Reserved
26:24	VC0 ID—RO. Hardwired to 0 since the first VC is always assigned as VC0
23:20	Reserved
19:17	Port Arbitration Select—RO. Hardwired to 0 since this field is not valid for endpoint devices
16	Load Port Arbitration Table—RO. Hardwired to 0 since this field is not valid for endpoint devices
15:8	Reserved
7:0	**TC/VC0 Map—**R/W, RO. Bit 0 is hardwired to 1 since TC0 is always mapped VC0. Bits [7:1] are implemented as R/W bits.

17.1.41 VC0STS—VC0 Resource Status Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 11Ah–11Bh
Attribute: RO
Default Value: 0000h
Size: 16 bits

Bit	Description
15:2	Reserved
1	VC0 Negotiation Pending—RO. Hardwired to 0 since this bit does not apply to the integrated Intel HD Audio device
0	Port Arbitration Table Status—RO. Hardwired to 0 since this field is not valid for endpoint devices

17.1.42 VCiCAP—VCi Resource Capability Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 11Ch–11Fh
Attribute: RO
Default Value: 00000000h
Size: 32 bits

Bit	Description
31:24	Port Arbitration Table Offset—RO. Hardwired to 0 since this field is not valid for endpoint devices.
23	Reserved
22:16	Maximum Time Slots—RO. Hardwired to 0 since this field is not valid for endpoint devices
15	Reject Snoop Transactions—RO. Hardwired to 0 since this field is not valid for endpoint devices
14	Advanced Packet Switching—RO. Hardwired to 0 since this field is not valid for endpoint devices
13:8	Reserved
7:0	Port Arbitration Capability—RO. Hardwired to 0 since this field is not valid for endpoint devices

17.1.43 VCiCTL—VCi Resource Control Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 120h–123h
Attribute: R/W, RO
Default Value: 00000000h
Size: 32 bits
Function Level Reset: No

Bit	Description
31	**VCi Enable—**R/W. 0 = VCi is disabled 1 = VCi is enabled ***Note:*** This bit is not reset on $D3_{HOT}$ to D0 transition; however, it is reset by PLTRST#.
30:27	Reserved
26:24	**VCi ID**—R/W. This field assigns a VC ID to the VCi resource. This field is not used by the PCH hardware, but it is R/W to avoid confusing software.
23:20	Reserved
19:17	Port Arbitration Select—RO. Hardwired to 0 since this field is not valid for endpoint devices
16	Load Port Arbitration Table—RO. Hardwired to 0 since this field is not valid for endpoint devices
15:8	Reserved
7:0	**TC/VCi Map**—R/W, RO. This field indicates the TCs that are mapped to the VCi resource. Bit 0 is hardwired to 0 indicating that it cannot be mapped to VCi. Bits [7:1] are implemented as R/W bits. This field is not used by the PCH hardware, but it is R/W to avoid confusing software.

17.1.44 VCiSTS—VCi Resource Status Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 126h–127h
Attribute: RO
Default Value: 0000h
Size: 16 bits

Bit	Description
15:2	Reserved
1	VCi Negotiation Pending—RO. Does not apply. Hardwired to 0.
0	Port Arbitration Table Status—RO. Hardwired to 0 since this field is not valid for endpoint devices.

17.1.45 RCCAP—Root Complex Link Declaration Enhanced Capability Header Register (Intel® HD Audio Controller—D27:F0)

Address Offset: 130h
Attribute: RO
Default Value: 00010005h
Size: 32 bits

Bit	Description
31:20	**Next Capability Offset**—RO. Hardwired to 0 indicating this is the last capability.
19:16	**Capability Version—**RO. Hardwired to 1h.
15:0	**PCI Express Extended Capability ID**—RO. Hardwired to 0005h.

17.1.46 ESD—Element Self Description Register (Intel® HD Audio Controller—D27:F0)

Address Offset:	134h–137h	Attribute:	RO
Default Value:	0F000100h	Size:	32 bits

Bit	Description
31:24	**Port Number**—RO. Hardwired to 0Fh indicating that the Intel HD Audio controller is assigned as Port #15d.
23:16	**Component ID**—RO. This field returns the value of the ESD.CID field of the chip configuration section. ESD.CID is programmed by BIOS.
15:8	**Number of Link Entries**—RO. The Intel HD Audio only connects to one device, the PCH egress port. Therefore this field reports a value of 1h.
7:4	Reserved
3:0	**Element Type (ELTYP)**—RO. The Intel HD Audio controller is an integrated Root Complex Device. Therefore, the field reports a value of 0h.

17.1.47 L1DESC—Link 1 Description Register (Intel® HD Audio Controller—D27:F0)

Address Offset:	140h–143h	Attribute:	RO
Default Value:	00000001h	Size:	32 bits

Bit	Description
31:24	**Target Port Number**—RO. The Intel HD Audio controller targets the PCH's Port 0.
23:16	**Target Component ID**—RO. This field returns the value of the ESD.CID field of the chip configuration section. ESD.CID is programmed by BIOS.
15:2	Reserved
1	**Link Type—**RO. Hardwired to 0 indicating Type 0.
0	**Link Valid**—RO. Hardwired to 1.

17.1.48 L1ADDL—Link 1 Lower Address Register (Intel® HD Audio Controller—D27:F0)

Address Offset:	148h–14Bh	Attribute:	RO
Default Value:	See Register Description	Size:	32 bits

Bit	Description
31:14	**Link 1 Lower Address**—RO. Hardwired to match the RCBA register value in the PCI-LPC bridge (D31:F0:F0h).
13:0	Reserved

17.1.49 L1ADDU—Link 1 Upper Address Register (Intel® HD Audio Controller—D27:F0)

Address Offset:	14Ch–14Fh	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	**Link 1 Upper Address**—RO. Hardwired to 00000000h.

17.2 Intel® HD Audio Memory Mapped Configuration Registers (Intel® HD Audio—D27:F0)

The base memory location for these memory mapped configuration registers is specified in the HDBAR register (D27:F0:offset 10h and D27:F0:offset 14h). The individual registers are then accessible at HDBAR + Offset as indicated in the following table.

These memory mapped registers must be accessed in byte, word, or DWord quantities.

Note: Address locations that are not shown should be treated as Reserved.

Table 17-2. Intel® HD Audio PCI Register Address Map (Intel® HD Audio D27:F0) (Sheet 1 of 4)

HDBAR + Offset	Mnemonic	Register Name	Default	Access
00h–01h	GCAP	Global Capabilities	4401h	RO
02h	VMIN	Minor Version	00h	RO
03h	VMAJ	Major Version	01h	RO
04h–05h	OUTPAY	Output Payload Capability	003Ch	RO
06h–07h	INPAY	Input Payload Capability	001Dh	RO
08h–0Bh	GCTL	Global Control	00000000h	R/W
0Ch–0Dh	WAKEEN	Wake Enable	0000h	R/W
0Eh–0Fh	STATESTS	State Change Status	0000h	R/WC
10h–11h	GSTS	Global Status	0000h	R/WC
12h–13h	—	Reserved	0000h	RO
14h–17h	—	Reserved	00000000h	RO
18h–19h	OUTSTRMPAY	Output Stream Payload Capability	0030h	RO
1Ah–1Bh	INSTRMPAY	Input Stream Payload Capability	0018h	RO
1Ch–1Fh	—	Reserved	00000000h	RO
20h–23h	INTCTL	Interrupt Control	00000000h	R/W
24h–27h	INTSTS	Interrupt Status	00000000h	RO
30h–33h	WALCLK	Wall Clock Counter	00000000h	RO
34–37h	—	Reserved	00000000h	RO
38h–3Bh	SSYNC	Stream Synchronization	00000000h	R/W
40h–43h	CORBLBASE	CORB Lower Base Address	00000000h	R/W, RO
44h–47h	CORBUBASE	CORB Upper Base Address	00000000h	R/W
48h–49h	CORBWP	CORB Write Pointer	0000h	R/W
4Ah–4Bh	CORBRP	CORB Read Pointer	0000h	R/W, RO
4Ch	CORBCTL	CORB Control	00h	R/W
4Dh	CORBST	CORB Status	00h	R/WC
4Eh	CORBSIZE	CORB Size	42h	RO
50h–53h	RIRBLBASE	RIRB Lower Base Address	00000000h	R/W, RO
54h–57h	RIRBUBASE	RIRB Upper Base Address	00000000h	R/W
58h–59h	RIRBWP	RIRB Write Pointer	0000h	R/W, RO
5Ah–5Bh	RINTCNT	Response Interrupt Count	0000h	R/W

Table 17-2. Intel® HD Audio PCI Register Address Map (Intel® HD Audio D27:F0) (Sheet 2 of 4)

HDBAR + Offset	Mnemonic	Register Name	Default	Access
5Ch	RIRBCTL	RIRB Control	00h	R/W
5Dh	RIRBSTS	RIRB Status	00h	R/WC
5Eh	RIRBSIZE	RIRB Size	42h	RO
60h–63h	IC	Immediate Command	00000000h	R/W
64h–67h	IR	Immediate Response	00000000h	RO
68h–69h	ICS	Immediate Command Status	0000h	R/W, R/WC
70h–73h	DPLBASE	DMA Position Lower Base Address	00000000h	R/W, RO
74h–77h	DPUBASE	DMA Position Upper Base Address	00000000h	R/W
80–82h	ISD0CTL	Input Stream Descriptor 0 (ISD0) Control	040000h	R/W, RO
83h	ISD0STS	ISD0 Status	00h	R/WC, RO
84h–87h	ISD0LPIB	ISD0 Link Position in Buffer	00000000h	RO
88h–8Bh	ISD0CBL	ISD0 Cyclic Buffer Length	00000000h	R/W
8Ch–8Dh	ISD0LVI	ISD0 Last Valid Index	0000h	R/W
8Eh–8F	ISD0FIFOW	ISD0 FIFO Watermark	0004h	R/W
90h–91h	ISD0FIFOS	ISD0 FIFO Size	0077h	RO
92h–93h	ISD0FMT	ISD0 Format	0000h	R/W
98h–9Bh	ISD0BDPL	ISD0 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
9Ch–9Fh	ISD0BDPU	ISD0 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
A0h–A2h	ISD1CTL	Input Stream Descriptor 1(ISD01) Control	040000h	R/W, RO
A3h	ISD1STS	ISD1 Status	00h	R/WC, RO
A4h–A7h	ISD1LPIB	ISD1 Link Position in Buffer	00000000h	RO
A8h–ABh	ISD1CBL	ISD1 Cyclic Buffer Length	00000000h	R/W
ACh–ADh	ISD1LVI	ISD1 Last Valid Index	0000h	R/W
AEh–AFh	ISD1FIFOW	ISD1 FIFO Watermark	0004h	R/W
B0h–B1h	ISD1FIFOS	ISD1 FIFO Size	0077h	RO
B2h–B3h	ISD1FMT	ISD1 Format	0000h	R/W
B8h–BBh	ISD1BDPL	ISD1 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
BCh–BFh	ISD1BDPU	ISD1 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
C0h–C2h	ISD2CTL	Input Stream Descriptor 2 (ISD2) Control	040000h	R/W, RO
C3h	ISD2STS	ISD2 Status	00h	R/WC, RO
C4h–C7h	ISD2LPIB	ISD2 Link Position in Buffer	00000000h	RO
C8h–CBh	ISD2CBL	ISD2 Cyclic Buffer Length	00000000h	R/W
CCh–CDh	ISD2LVI	ISD2 Last Valid Index	0000h	R/W
CEh–CFh	ISD1FIFOW	ISD1 FIFO Watermark	0004h	R/W
D0h–D1h	ISD2FIFOS	ISD2 FIFO Size	0077h	RO
D2h–D3h	ISD2FMT	ISD2 Format	0000h	R/W
D8h–DBh	ISD2BDPL	ISD2 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO

Table 17-2. Intel® HD Audio PCI Register Address Map (Intel® HD Audio D27:F0) (Sheet 3 of 4)

HDBAR + Offset	Mnemonic	Register Name	Default	Access
DCh–DFh	ISD2BDPU	ISD2 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
E0h–E2h	ISD3CTL	Input Stream Descriptor 3 (ISD3) Control	040000h	R/W, RO
E3h	ISD3STS	ISD3 Status	00h	R/WC, RO
E4h–E7h	ISD3LPIB	ISD3 Link Position in Buffer	00000000h	RO
E8h–EBh	ISD3CBL	ISD3 Cyclic Buffer Length	00000000h	R/W
ECh–EDh	ISD3LVI	ISD3 Last Valid Index	0000h	R/W
EEh–EFh	ISD3FIFOW	ISD3 FIFO Watermark	0004h	R/W
F0h–F1h	ISD3FIFOS	ISD3 FIFO Size	0077h	RO
F2h–F3h	ISD3FMT	ISD3 Format	0000h	R/W
F8h–FBh	ISD3BDPL	ISD3 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
FCh–FFh	ISD3BDPU	ISD3 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
100h–102h	OSD0CTL	Output Stream Descriptor 0 (OSD0) Control	040000h	R/W, RO
103h	OSD0STS	OSD0 Status	00h	R/WC, RO
104h–107h	OSD0LPIB	OSD0 Link Position in Buffer	00000000h	RO
108h–10Bh	OSD0CBL	OSD0 Cyclic Buffer Length	00000000h	R/W
10Ch–10Dh	OSD0LVI	OSD0 Last Valid Index	0000h	R/W
10Eh–10Fh	OSD0FIFOW	OSD0 FIFO Watermark	0004h	R/W
110h–111h	OSD0FIFOS	OSD0 FIFO Size	00BFh	R/W
112–113h	OSD0FMT	OSD0 Format	0000h	R/W
118h–11Bh	OSD0BDPL	OSD0 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
11Ch–11Fh	OSD0BDPU	OSD0 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
120h–122h	OSD1CTL	Output Stream Descriptor 1 (OSD1) Control	040000h	R/W, RO
123h	OSD1STS	OSD1 Status	00h	R/WC, RO
124h–127h	OSD1LPIB	OSD1 Link Position in Buffer	00000000h	RO
128h–12Bh	OSD1CBL	OSD1 Cyclic Buffer Length	00000000h	R/W
12Ch–12Dh	OSD1LVI	OSD1 Last Valid Index	0000h	R/W
12Eh–12Fh	OSD1FIFOW	OSD1 FIFO Watermark	0004h	R/W
130h–131h	OSD1FIFOS	OSD1 FIFO Size	00BFh	R/W
132h–133h	OSD1FMT	OSD1 Format	0000h	R/W
138h–13Bh	OSD1BDPL	OSD1 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
13Ch–13Fh	OSD1BDPU	OSD1 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
140h–142h	OSD2CTL	Output Stream Descriptor 2 (OSD2) Control	040000h	R/W, RO
143h	OSD2STS	OSD2 Status	00h	R/WC, RO
144h–147h	OSD2LPIB	OSD2 Link Position in Buffer	00000000h	RO
148h–14Bh	OSD2CBL	OSD2 Cyclic Buffer Length	00000000h	R/W
14Ch–14Dh	OSD2LVI	OSD2 Last Valid Index	0000h	R/W

Table 17-2. Intel® HD Audio PCI Register Address Map (Intel® HD Audio D27:F0) (Sheet 4 of 4)

HDBAR + Offset	Mnemonic	Register Name	Default	Access
14Eh–14Fh	OSD2FIFOW	OSD2 FIFO Watermark	0004h	R/W
150h–151h	OSD2FIFOS	OSD2 FIFO Size	00BFh	R/W
152h–153h	OSD2FMT	OSD2 Format	0000h	R/W
158h–15Bh	OSD2BDPL	OSD2 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
15Ch–15Fh	OSD2BDPU	OSD2 Buffer Description List Pointer-Upper Base Address	00000000h	R/W
160h–162h	OSD3CTL	Output Stream Descriptor 3 (OSD3) Control	040000h	R/W, RO
163h	OSD3STS	OSD3 Status	00h	R/WC, RO
164h–167h	OSD3LPIB	OSD3 Link Position in Buffer	00000000h	RO
168h–16Bh	OSD3CBL	OSD3 Cyclic Buffer Length	00000000h	R/W
16Ch–16Dh	OSD3LVI	OSD3 Last Valid Index	0000h	R/W
16Eh–16Fh	OSD3FIFOW	OSD3 FIFO Watermark	0004h	R/W
170h–171h	OSD3FIFOS	OSD3 FIFO Size	00BFh	R/W
172h–173h	OSD3FMT	OSD3 Format	0000h	R/W
178h–17Bh	OSD3BDPL	OSD3 Buffer Descriptor List Pointer-Lower Base Address	00000000h	R/W, RO
17Ch–17Fh	OSD3BDPU	OSD3 Buffer Description List Pointer-Upper Base Address	00000000h	R/W

17.2.1 GCAP—Global Capabilities Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 00h Attribute: RO
Default Value: 4401h Size: 16 bits

Bit	Description
15:12	**Number of Output Stream Supported**—R/WO. 0100b indicates that the PCH's Intel® High Definition Audio controller supports 4 output streams.
11:8	**Number of Input Stream Supported**—R/WO. 0100b indicates that the PCH's Intel® High Definition Audio controller supports 4 input streams.
7:3	**Number of Bidirectional Stream Supported**—RO. Hardwired to 0 indicating that the PCH's Intel® High Definition Audio controller supports 0 bidirectional stream.
2:1	**Number of Serial Data Out Signals**—RO. Hardwired to 0 indicating that the PCH's Intel® High Definition Audio controller supports 1 serial data output signal.
0	**64-bit Address Supported**—R/WO. 1b indicates that the PCH's Intel® High Definition Audio controller supports 64-bit addressing for BDL addresses, data buffer addressees, and command buffer addresses.

17.2.2 VMIN—Minor Version Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 02h Attribute: RO
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Minor Version**—RO. Hardwired to 0 indicating that the PCH supports minor revision number 00h of the Intel HD Audio specification.

17.2.3 VMAJ—Major Version Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 03h Attribute: RO
Default Value: 01h Size: 8 bits

Bit	Description
7:0	**Major Version**—RO. Hardwired to 01h indicating that the PCH supports major revision number 1 of the Intel HD Audio specification.

17.2.4 OUTPAY—Output Payload Capability Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 04h Attribute: RO
Default Value: 003Ch Size: 16 bits

Bit	Description
15:7	Reserved
6:0	**Output Payload Capability**—RO. Hardwired to 3Ch indicating 60 word payload. This field indicates the total output payload available on the link. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 MHz frame. The default link clock of 24.000 MHz (the data is double pumped) provides 1000 bits per frame, or 62.5 words in total. 40 bits are used for command and control, leaving 60 words available for data payload. 00h = 0 word 01h = 1 word payload. ..... FFh = 256 word payload.

17.2.5 INPAY—Input Payload Capability Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 06h | Attribute: RO
Default Value: 001Dh | Size: 16 bits

Bit	Description
15:7	Reserved
6:0	**Input Payload Capability**—RO. Hardwired to 1Dh indicating 29 word payload. This field indicates the total output payload available on the link. This does not include bandwidth used for response. This measurement is in 16-bit word quantities per 48 MHz frame. The default link clock of 24.000 MHz provides 500 bits per frame, or 31.25 words in total. 36 bits are used for response, leaving 29 words available for data payload. 00h = 0 word 01h = 1 word payload. ..... FFh = 256 word payload.

17.2.6 GCTL—Global Control Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 08h | Attribute: R/W
Default Value: 00000000h | Size: 32 bits

Bit	Description
31:9	Reserved
8	**Accept Unsolicited Response Enable—**R/W. 0 = Unsolicited responses from the codecs are not accepted. 1 = Unsolicited response from the codecs are accepted by the controller and placed into the Response Input Ring Buffer.
7:2	Reserved
1	**Flush Control**—R/W. Writing a 1 to this bit initiates a flush. When the flush completion is received by the controller, hardware sets the Flush Status bit and clears this Flush Control bit. Before a flush cycle is initiated, the DMA Position Buffer must be programmed with a valid memory address by software, but the DMA Position Buffer bit 0 needs not be set to enable the position reporting mechanism. Also, all streams must be stopped (the associated RUN bit must be 0). When the flush is initiated, the controller will flush the pipelines to memory to ensure that the hardware is ready to transition to a D3 state. Setting this bit is not a critical step in the power state transition if the content of the FIFOs is not critical.
0	**Controller Reset #—**R/W. 0 = Writing a 0 causes the Intel HD Audio controller to be reset. All state machines, FIFOs and non-resume well memory mapped configuration registers (not PCI configuration registers) in the controller will be reset. The Intel HD Audio link RESET# signal will be asserted, and all other link signals will be driven to their default values. After the hardware has completed sequencing into the reset state, it will report a 0 in this bit. Software must read a 0 from this bit to verify the controller is in reset. 1 = Writing a 1 causes the controller to exit its reset state and deassert the Intel HD Audio link RESET# signal. Software is responsible for setting/clearing this bit such that the minimum Intel HD Audio link RESET# signal assertion pulse width specification is met. When the controller hardware is ready to begin operation, it will report a 1 in this bit. Software must read a 1 from this bit before accessing any controller registers. This bit defaults to a 0 after Hardware reset, therefore, software needs to write a 1 to this bit to begin operation. ***Notes:*** 1. The CORB/RIRB RUN bits and all stream RUN bits must be verified cleared to 0 before writing a 0 to this bit in order to assure a clean re-start. 2. When setting or clearing this bit, software must ensure that minimum link timing requirements (minimum RESET# assertion time, and so forth) are met. 3. When this bit is 0 indicating that the controller is in reset, writes to all Intel HD Audio memory mapped registers are ignored as if the device is not present. The only exception is this register itself. The Global Control register is write-able as a DWord, Word, or Byte even when CRST# (this bit) is 0 if the byte enable for the byte containing the CRST# bit (Byte Enable 0) is active. If Byte Enable 0 is not active, writes to the Global Control register will be ignored when CRST# is 0. When CRST# is 0, reads to Intel HD Audio memory mapped registers will return their default value except for registers that are not reset with PLTRST# or on a $D3_{HOT}$ to D0 transition.

17.2.7 WAKEEN—Wake Enable Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 0Ch Attribute: R/W
Default Value: 0000h Size: 16 bits
Function Level Reset: No

Bit	Description
15:4	Reserved
3:0	**SDIN Wake Enable Flags**—R/W. These bits control which SDI signal(s) may generate a wake event. A 1b in the bit mask indicates that the associated SDIN signal is enabled to generate a wake. Bit 0 is used for SDI[0] Bit 1 is used for SDI[1] Bit 2 is used for SDI[2] Bit 3 is used for SDI[3] ***Note:*** These bits are in the resume well and only cleared on a power on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

17.2.8 STATESTS—State Change Status Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 0Eh Attribute: R/WC
Default Value: 0000h Size: 16 bits
Function Level Reset: No

Bit	Description
15:4	Reserved
3:0	**SDIN State Change Status Flags**—R/WC. Flag bits that indicate which SDI signal(s) received a state change event. The bits are cleared by writing 1s to them. Bit 0 = SDI[0] Bit 1 = SDI[1] Bit 2 = SDI[2] Bit 3 = SDI[3] These bits are in the resume well and only cleared on a power on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

17.2.9 GSTS—Global Status Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 10h Attribute: R/WC
Default Value: 0000h Size: 16 bits

Bit	Description
15:2	Reserved
1	**Flush Status**—R/WC. This bit is set to 1 by hardware to indicate that the flush cycle initiated when the Flush Control bit (HDBAR + 08h, bit 1) was set has completed. Software must write a 1 to clear this bit before the next time the Flush Control bit is set to clear the bit.
0	Reserved

17.2.10 OUTSTRMPAY—Output Stream Payload Capability (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 18h Attribute: RO
Default Value: 0030h Size: 16 bits

Bit	Description
15:8	Reserved
7:0	**Output Stream Payload Capability (OUTSTRMPAY)**—RO: Indicates maximum number of words per frame for any single output stream. This measurement is in 16 bit word quantities per 48 kHz frame. 48 Words (96B) is the maximum supported, therefore a value of 30h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Output Stream Descriptor register. 00h = 0 words 01h = 1 word payload … FFh = 255h word payload

17.2.11 INSTRMPAY—Input Stream Payload Capability (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 1Ah Attribute: RO
Default Value: 0018h Size: 16 bits

Bit	Description
15:8	Reserved
7:0	**Input Stream Payload Capability (INSTRMPAY)**—RO. Indicates maximum number of words per frame for any single input stream. This measurement is in 16 bit word quantities per 48 kHz frame. 24 Words (48B) is the maximum supported, therefore a value of 18h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Input Stream Descriptor register. 00h = 0 words 01h = 1 word payload … FFh = 255h word payload

17.2.12 INTCTL—Interrupt Control Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:	HDBAR + 20h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31	**Global Interrupt Enable (GIE)—**R/W. Global bit to enable device interrupt generation. 1 = When set to 1, the Intel HD Audio function is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space, such as the Interrupt Enable bit in the PCI configuration space. ***Note:*** This bit is not affected by the $D3_{HOT}$ to D0 transition.
30	**Controller Interrupt Enable (CIE)—**R/W. Enables the general interrupt for controller functions. 1 = When set to 1, the controller generates an interrupt when the corresponding status bit gets set due to a Response Interrupt, a Response Buffer Overrun, and State Change events. ***Note:*** This bit is not affected by the $D3_{HOT}$ to D0 transition.
29:8	Reserved
7:0	**Stream Interrupt Enable (SIE)—**R/W. When set to 1, the individual streams are enabled to generate an interrupt when the corresponding status bits get set. A stream interrupt will be caused as a result of a buffer with IOC = 1in the BDL entry being completed, or as a result of a FIFO error (underrun or overrun) occurring. Control over the generation of each of these sources is in the associated Stream Descriptor. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set. Bit 0 = input stream 1 Bit 1 = input stream 2 Bit 2 = input stream 3 Bit 3 = input stream 4 Bit 4 = output stream 1 Bit 5 = output stream 2 Bit 6 = output stream 3 Bit 7 = output stream 4

17.2.13 INTSTS—Interrupt Status Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 24h | Attribute: RO
Default Value: 00000000h | Size: 32 bits

Bit	Description
31	**Global Interrupt Status (GIS)**—RO. This bit is an OR of all the interrupt status bits in this register. ***Note:*** This bit is not affected by the $D3_{HOT}$ to D0 transition.
30	**Controller Interrupt Status (CIS)—**RO. Status of general controller interrupt. 1 = Interrupt condition occurred due to a Response Interrupt, a Response Buffer Overrun Interrupt, or a SDIN State Change event. The exact cause can be determined by interrogating other registers. This bit is an OR of all of the stated interrupt status bits for this register. ***Notes:*** 1. This bit is set regardless of the state of the corresponding interrupt enable bit, but a hardware interrupt will not be generated unless the corresponding enable bit is set. 2. This bit is not affected by the $D3_{HOT}$ to D0 transition.
29:8	Reserved
7:0	**Stream Interrupt Status (SIS)—**RO. 1 = Interrupt condition occurred on the corresponding stream. This bit is an OR of all of the stream's interrupt status bits. ***Note:*** These bits are set regardless of the state of the corresponding interrupt enable bits. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set. Bit 0 = input stream 1 Bit 1 = input stream 2 Bit 2 = input stream 3 Bit 3 = input stream 4 Bit 4 = output stream 1 Bit 5 = output stream 2 Bit 6 = output stream 3 Bit 7 = output stream 4

17.2.14 WALCLK—Wall Clock Counter Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 30h | Attribute: RO
Default Value: 00000000h | Size: 32 bits

Bit	Description
31:0	**Wall Clock Counter**—RO. A 32 bit counter that is incremented on each link Bit Clock period and rolls over from FFFF FFFFh to 0000 0000h. This counter will roll over to 0 with a period of approximately 179 seconds. This counter is enabled while the Bit Clock bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset.

17.2.15 SSYNC—Stream Synchronization Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 38h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:8	Reserved
7:0	**Stream Synchronization (SSYNC)—**R/W. When set to 1, these bits block data from being sent on or received from the link. Each bit controls the associated stream descriptor (that is, bit 0 corresponds to the first stream descriptor, and so forth). To synchronously start a set of DMA engines, these bits are first set to 1. The RUN bits for the associated stream descriptors are then set to 1 to start the DMA engines. When all streams are ready (FIFORDY =1), the associated SSYNC bits can all be set to 0 at the same time, and transmission or reception of bits to or from the link will begin together at the start of the next full link frame. To synchronously stop the streams, fist these bits are set, and then the individual RUN bits in the stream descriptor are cleared by software. If synchronization is not desired, these bits may be left as 0, and the stream will simply begin running normally when the stream's RUN bit is set. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set. Bit 0 = input stream 1 Bit 1 = input stream 2 Bit 2 = input stream 3 Bit 3 = input stream 4 Bit 4 = output stream 1 Bit 5 = output stream 2 Bit 6 = output stream 3 Bit 7 = output stream 4

17.2.16 CORBLBASE—CORB Lower Base Address Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 40h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:7	**CORB Lower Base Address—**R/W. Lower address of the Command Output Ring Buffer, allowing the CORB base address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	**CORB Lower Base Unimplemented Bits**—RO. Hardwired to 0. This required the CORB to be allocated with 128B granularity to allow for cache line fetch optimizations.

17.2.17 CORBUBASE—CORB Upper Base Address Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 44h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	**CORB Upper Base Address—**R/W. Upper 32 bits of the address of the Command Output Ring buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.

17.2.18 CORBWP—CORB Write Pointer Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 48h Attribute: R/W
Default Value: 0000h Size: 16 bits

Bit	Description
15:8	Reserved
7:0	**CORB Write Pointer**—R/W. Software writes the last valid CORB entry offset into this field in DWord granularity. The DMA engine fetches commands from the CORB until the Read pointer matches the Write pointer. Supports 256 CORB entries (256x4B = 1 KB). This register field may be written when the DMA engine is running.

17.2.19 CORBRP—CORB Read Pointer Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 4Ah Attribute: R/W, RO
Default Value: 0000h Size: 16 bits

Bit	Description
15	**CORB Read Pointer Reset—**R/W. Software writes a 1 to this bit to reset the CORB Read Pointer to 0 and clear any residual prefetched commands in the CORB hardware buffer within the Intel High Definition Audio controller. The hardware will physically update this bit to 1 when the CORB Pointer reset is complete. Software must read a 1 to verify that the reset completed correctly. Software must clear this bit back to 0 and read back the 0 to verify that the clear completed correctly. The CORB DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted.
14:8	Reserved
7:0	**CORB Read Pointer (CORBRP)**—RO. Software reads this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB Read Pointer offset in Dword granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. Supports 256 CORB entries (256 x 4B=1 KB). This field may be read while the DMA engine is running.

17.2.20 CORBCTL—CORB Control Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 4Ch Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:2	Reserved
1	**Enable CORB DMA Engine—**R/W. 0 = DMA stop 1 = DMA run After software writes a 0 to this bit, the hardware may not stop immediately. The hardware will physically update the bit to 0 when the DMA engine is truly stopped. Software must read a 0 from this bit to verify that the DMA engine is truly stopped.
0	**CORB Memory Error Interrupt Enable—**R/W. If this bit is set the controller will generate an interrupt if the CMEI status bit (HDBAR + 4Dh: bit 0) is set.

17.2.21 CORBST—CORB Status Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 4Dh Attribute: R/WC
Default Value: 00h Size: 8 bits

Bit	Description
7:1	Reserved
0	**CORB Memory Error Indication (CMEI)—**R/WC. 1 = Controller detected an error in the path way between the controller and memory. This may be an ECC bit error or any other type of detectable data error which renders the command data fetched invalid. Software can clear this bit by writing a 1 to it. However, this type of error leaves the audio subsystem in an un-viable state and typically requires a controller reset by writing a 0 to the Controller Reset # bit (HDBAR + 08h: bit 0).

17.2.22 CORBSIZE—CORB Size Register Intel® HD Audio Controller—D27:F0using)

Memory Address: HDBAR + 4Eh Attribute: RO
Default Value: 42h Size: 8 bits

Bit	Description
7:4	**CORB Size Capability**—RO. Hardwired to 0100b indicating that the PCH only supports a CORB size of 256 CORB entries (1024B)
3:2	Reserved
1:0	**CORB Size**—RO. Hardwired to 10b which sets the CORB size to 256 entries (1024B)

17.2.23 RIRBLBASE—RIRB Lower Base Address Register (Intel® HD AudioController—D27:F0)

Memory Address: HDBAR + 50h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:7	**RIRB Lower Base Address—**R/W. Lower address of the Response Input Ring Buffer, allowing the RIRB base address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	RIRB Lower Base Unimplemented Bits—RO. Hardwired to 0. This required the RIRB to be allocated with 128-B granularity to allow for cache line fetch optimizations.

17.2.24 RIRBUBASE—RIRB Upper Base Address Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 54h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	**RIRB Upper Base Address—**R/W. Upper 32 bits of the address of the Response Input Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.

17.2.25 RIRBWP—RIRB Write Pointer Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 58h Attribute: R/W, RO
Default Value: 0000h Size: 16 bits

Bit	Description
15	**RIRB Write Pointer Reset—**R/W. Software writes a 1 to this bit to reset the RIRB Write Pointer to 0. The RIRB DMA engine must be stopped prior to resetting the Write Pointer or else DMA transfer may be corrupted. This bit is always read as 0.
14:8	Reserved
7:0	**RIRB Write Pointer (RIRBWP)**—RO. Indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB Write Pointer offset in 2 DWord RIRB entry units (since each RIRB entry is 2 DWords long). Supports up to 256 RIRB entries (256 x 8 B = 2 KB). This register field may be written when the DMA engine is running.

17.2.26 RINTCNT—Response Interrupt Count Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 5Ah Attribute: R/W
Default Value: 0000h Size: 16 bits

Bit	Description
15:8	Reserved
7:0	**N Response Interrupt Count—**R/W. 0000 0001b = 1 response sent to RIRB ..... 1111 1111b = 255 responses sent to RIRB 0000 0000b = 256 responses sent to RIRB The DMA engine should be stopped when changing this field or else an interrupt may be lost. Note that each response occupies 2 DWords in the RIRB. This is compared to the total number of responses that have been returned, as opposed to the number of frames in which there were responses. If more than one codecs responds in one frame, then the count is increased by the number of responses received in the frame.

17.2.27 RIRBCTL—RIRB Control Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 5Ch Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:3	Reserved
2	**Response Overrun Interrupt Control**—R/W. If this bit is set, the hardware will generate an interrupt when the Response Overrun Interrupt Status bit (HDBAR + 5Dh: bit 2) is set.
1	**Enable RIRB DMA Engine**—R/W. 0 = DMA stop 1 = DMA run After software writes a 0 to this bit, the hardware may not stop immediately. The hardware will physically update the bit to 0 when the DMA engine is truly stopped. Software must read a 0 from this bit to verify that the DMA engine is truly stopped.
0	**Response Interrupt Control**—R/W. 0 = Disable Interrupt 1 = Generate an interrupt after N number of responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI[x] inputs (whichever occurs first). The N counter is reset when the interrupt is generated.

17.2.28 RIRBSTS—RIRB Status Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 5Dh Attribute: R/WC
Default Value: 00h Size: 8 bits

Bit	Description
7:3	Reserved
2	**Response Overrun Interrupt Status**—R/WC. 1 = Software sets this bit to 1 when the RIRB DMA engine is not able to write the incoming responses to memory before additional incoming responses overrun the internal FIFO. When the overrun occurs, the hardware will drop the responses which overrun the buffer. An interrupt may be generated if the Response Overrun Interrupt Control bit is set. Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this bit by writing a 1 to it.
1	Reserved
0	**Response Interrupt**—R/WC. 1 = Hardware sets this bit to 1 when an interrupt has been generated after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI[x] inputs (whichever occurs first). Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this bit by writing a 1 to it.

17.2.29 RIRBSIZE—RIRB Size Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 5Eh Attribute: RO
Default Value: 42h Size: 8 bits

Bit	Description
7:4	**RIRB Size Capability**—RO. Hardwired to 0100b indicating that the PCH only supports a RIRB size of 256 RIRB entries (2048B)
3:2	Reserved
1:0	**RIRB Size**—RO. Hardwired to 10b which sets the CORB size to 256 entries (2048B)

17.2.30 IC—Immediate Command Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 60h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	**Immediate Command Write—R/W**. The command to be sent to the codec using the Immediate Command mechanism is written to this register. The command stored in this register is sent out over the link during the next available frame after a 1 is written to the ICB bit (HDBAR + 68h: bit 0)

17.2.31 IR—Immediate Response Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 64h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	**Immediate Response Read (IRR)**—RO. This register contains the response received from a codec resulting from a command sent using the Immediate Command mechanism. If multiple codecs responded in the same time, there is no assurance as to which response will be latched. Therefore, broadcast-type commands must not be issued using the Immediate Command mechanism.

17.2.32 ICS—Immediate Command Status Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 68h Attribute: R/W, R/WC
Default Value: 0000h Size: 16 bits

Bit	Description
15:2	Reserved
1	**Immediate Result Valid (IRV)**—R/WC. 1 = Set to 1 by hardware when a new response is latched into the Immediate Response register (HDBAR + 64). This is a status flag indicating that software may read the response from the Immediate Response register. Software must clear this bit by writing a 1 to it before issuing a new command so that the software may determine when a new response has arrived.
0	**Immediate Command Busy (ICB)**—R/W. When this bit is read as 0, it indicates that a new command may be issued using the Immediate Command mechanism. When this bit transitions from a 0 to a 1 (using software writing a 1), the controller issues the command currently stored in the Immediate Command register to the codec over the link. When the corresponding response is latched into the Immediate Response register, the controller hardware sets the IRV flag and clears the ICB bit back to 0. Software may write this bit to a 0 if the bit fails to return to 0 after a reasonable time out period. ***Note:*** An Immediate Command must not be issued while the CORB/RIRB mechanism is operating, otherwise the responses conflict. This must be enforced by software.

17.2.33 DPLBASE—DMA Position Lower Base Address Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 70h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:7	**DMA Position Lower Base Address—**R/W. Lower 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted. This same address is used by the Flush Control and must be programmed with a valid value before the Flush Control bit (HDBAR+08h:bit 1) is set.
6:1	DMA Position Lower Base Unimplemented bits—RO. Hardwired to 0 to force the 128-byte buffer alignment for cache line write optimizations.
0	**DMA Position Buffer Enable—**R/W. 1 = Controller will write the DMA positions of each of the DMA engines to the buffer in the main memory periodically (typically once per frame). Software can use this value to know what data in memory is valid data.

17.2.34 DPUBASE—DMA Position Upper Base Address Register (Intel® HD Audio Controller—D27:F0)

Memory Address: HDBAR + 74h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	**DMA Position Upper Base Address**—R/W. Upper 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted.

17.2.35 SDCTL—Stream Descriptor Control Register (Intel® HD Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 80h Attribute: R/W, RO
Input Stream[1]: HDBAR + A0h
Input Stream[2]: HDBAR + C0h
Input Stream[3]: HDBAR + E0h
Output Stream[0]: HDBAR + 100h
Output Stream[1]: HDBAR + 120h
Output Stream[2]: HDBAR + 140h
Output Stream[3]: HDBAR + 160h
Default Value: 040000h Size: 24 bits

Bit	Description
23:20	**Stream Number—**R/W. This value reflect the Tag associated with the data being transferred on the link. When data controlled by this descriptor is sent out over the link, it will have its stream number encoded on the SYNC signal. When an input stream is detected on any of the SDI signals that match this value, the data samples are loaded into FIFO associated with this descriptor. Note that while a single SDI input may contain data from more than one stream number, two different SDI inputs may not be configured with the same stream number. 0000 = Reserved 0001 = Stream 1 ..... 1110 = Stream 14 1111 = Stream 15

Bit	Description
19	Bidirectional Direction Control—RO. This bit is only meaningful for bidirectional streams; therefore, this bit is hardwired to 0.
18	**Traffic Priority**—RO. Hardwired to 1 indicating that all streams will use VC1 if it is enabled through the PCI Express* registers.
17:16	Stripe Control—RO. This bit is only meaningful for input streams; therefore, this bit is hardwired to 0.
15:5	Reserved
4	**Descriptor Error Interrupt Enable—**R/W. 0 = Disable 1 = An interrupt is generated when the Descriptor Error Status bit is set.
3	**FIFO Error Interrupt Enable—**R/W. This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	**Interrupt on Completion Enable—**R/W. This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur.
1	**Stream Run (RUN)—**R/W. 0 = DMA engine associated with this input stream will be disabled. The hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine. 1 = DMA engine associated with this input stream will be enabled to transfer data from the FIFO to the main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set.
0	**Stream Reset (SRST)—**R/W. 0 = Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. 1 = Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFOs for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. The RUN bit must be cleared before SRST is asserted.

17.2.36 SDSTS—Stream Descriptor Status Register (Intel® HD Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 83h
Input Stream[1]: HDBAR + A3h
Input Stream[2]: HDBAR + C3h
Input Stream[3]: HDBAR + E3h
Output Stream[0]: HDBAR + 103h
Output Stream[1]: HDBAR + 123h
Output Stream[2]: HDBAR + 143h
Output Stream[3]: HDBAR + 163h

Attribute: R/WC, RO

Default Value: 00h

Size: 8 bits

Bit	Description
7:6	Reserved
5	**FIFO Ready (FIFORDY)**—RO. For output streams, the controller hardware will set this bit to 1 while the output DMA FIFO contains enough data to maintain the stream on the link. This bit defaults to 0 on reset because the FIFO is cleared on a reset. For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set.
4	**Descriptor Error—**R/WC. 1 = A serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor list useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stopped. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
3	**FIFO Error—**R/WC. 1 = FIFO error occurred. This bit is set even if an interrupt is not enabled. The bit is cleared by writing a 1 to it. For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers do not increment and the incoming data is not written into the FIFO, thereby being lost. For an output stream, this indicates a FIFO underrun when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	**Buffer Completion Interrupt Status—**R/WC. This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to it.
1:0	Reserved

17.2.37 SDLPIB—Stream Descriptor Link Position in Buffer Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 84h
Input Stream[1]: HDBAR + A4h
Input Stream[2]: HDBAR + C4h
Input Stream[3]: HDBAR + E4h
Output Stream[0]: HDBAR + 104h
Output Stream[1]: HDBAR + 124h
Output Stream[2]: HDBAR + 144h
Output Stream[3]: HDBAR + 164h

Attribute: RO

Default Value: 00000000h

Size: 32 bits

Bit	Description
31:0	**Link Position in Buffer—**RO. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

17.2.38 SDCBL—Stream Descriptor Cyclic Buffer Length Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 88h
Input Stream[1]: HDBAR + A8h
Input Stream[2]: HDBAR + C8h
Input Stream[3]: HDBAR + E8h
Output Stream[0]: HDBAR + 108h
Output Stream[1]: HDBAR + 128h
Output Stream[2]: HDBAR + 148h
Output Stream[3]: HDBAR + 168h

Attribute: R/W

Default Value: 00000000h

Size: 32 bits

Bit	Description
31:0	**Cyclic Buffer Length—**R/W. Indicates the number of bytes in the complete cyclic buffer. This register represents an integer number of samples. Link Position in Buffer will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should be only modified when the RUN bit is 0. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfer may be corrupted.

17.2.39 SDLVI—Stream Descriptor Last Valid Index Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 8Ch
Input Stream[1]: HDBAR + ACh
Input Stream[2]: HDBAR + CCh
Input Stream[3]: HDBAR + ECh
Output Stream[0]: HDBAR + 10Ch
Output Stream[1]: HDBAR + 12Ch
Output Stream[2]: HDBAR + 14Ch
Output Stream[3]: HDBAR + 16Ch

Attribute: R/W

Default Value: 0000h

Size: 16 bits

Bit	Description
15:8	Reserved
7:0	**Last Valid Index—**R/W. The value written to this register indicates the index for the last valid Buffer Descriptor in BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. This field must be at least 1; that is, there must be at least 2 valid entries in the buffer descriptor list before DMA operations can begin. This value should only modified when the RUN bit is 0.

17.2.40 SDFIFOW—Stream Descriptor FIFO Watermark Register (Intel® HD Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 8Eh
Input Stream[1]: HDBAR + AEh
Input Stream[2]: HDBAR + CEh
Input Stream[3]: HDBAR + EEh
Output Stream[0]: HDBAR + 10Eh
Output Stream[1]: HDBAR + 12Eh
Output Stream[2]: HDBAR + 14Eh
Output Stream[3]: HDBAR + 16Eh

Attribute: R/W

Default Value: 0004h

Size: 16 bits

Bit	Description
15:3	Reserved
2:0	**FIFO Watermark (FIFOW)**—RO. Indicates the minimum number of bytes accumulated/free in the FIFO before the controller will start a fetch/eviction of data. The HD Audio Controller hardwires the FIFO Watermark to either 32 B or 64 B based on the number of bytes per frame for the configured input stream. 100 = 32B (Default) 101 = 64B Others = Unsupported ***Note:*** When the bit field is programmed to an unsupported size, the hardware sets itself to the default value. Software must read the bit field to test if the value is supported after setting the bit field.

17.2.41 ISDFIFOS—Stream Descriptor FIFO Size Register – Input Streams (Intel® High Definition Audio Controller—D27:F0)

Memory Address:	Input Stream[0]: HDBAR + 90h Input Stream[1]: HDBAR + B0h Input Stream[2]: HDBAR + D0h Input Stream[3]: HDBAR + F0h	Attribute:	RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:0	**FIFO Size**—RO. Indicates the maximum number of bytes that could be evicted by the controller at one time. This is the maximum number of bytes that may have been received from the link but not yet DMA'd into memory, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on factors including the stream format programmed in SDFMT register. As the default value is zero, SW must write to the respective SDFMT register to kick of the FIFO size calculation, and read back to find out the HW allocated FIFO size.

17.2.42 OSDFIFOS—Stream Descriptor FIFO Size Register – Output Streams (Intel® High Definition Audio Controller—D27:F0)

Memory Address:	Output Stream[0]: HDBAR + 110h Output Stream[1]: HDBAR + 130h Output Stream[2]: HDBAR + 150h Output Stream[3]: HDBAR + 170h	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15:0	**FIFO Size**—R/W. Indicates the maximum number of bytes that could be fetched by the controller at one time. This is the maximum number of bytes that may have been DMA'd into memory but not yet transmitted on the link, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on factors including the stream format programmed in SDFMT register. As the default value is zero, SW must write to the respective SDFMT register to kick of the FIFO size calculation, and read back to find out the HW allocated FIFO size.

17.2.43 SDFMT—Stream Descriptor Format Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 92h
Input Stream[1]: HDBAR + B2h
Input Stream[2]: HDBAR + D2h
Input Stream[3]: HDBAR + F2h
Output Stream[0]: HDBAR + 112h
Output Stream[1]: HDBAR + 132h
Output Stream[2]: HDBAR + 152h
Output Stream[3]: HDBAR + 172h

Attribute: R/W

Default Value: 0000h

Size: 16 bits

Bit	Description
15	Reserved
14	**Sample Base Rate—**R/W 0 = 48 kHz 1 = 44.1 kHz
13:11	**Sample Base Rate Multiple—**R/W 000 = 48 kHz, 44.1 kHz or less 001 = x2 (96 kHz, 88.2 kHz, 32 kHz) 010 = x3 (144 kHz) 011 = x4 (192 kHz, 176.4 kHz) Others = Reserved
10:8	**Sample Base Rate Devisor—**R/W. 000 = Divide by 1(48 kHz, 44.1 kHz) 001 = Divide by 2 (24 kHz, 22.05 kHz) 010 = Divide by 3 (16 kHz, 32 kHz) 011 = Divide by 4 (11.025 kHz) 100 = Divide by 5 (9.6 kHz) 101 = Divide by 6 (8 kHz) 110 = Divide by 7 111 = Divide by 8 (6 kHz)
7	Reserved
6:4	**Bits per Sample (BITS)—**R/W. 000 =8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001 =16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010 = 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries 011 =24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries 100 =32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries Others = Reserved
3:0	Number of Channels (CHAN)—R/W. Indicates number of channels in each frame of the stream. 0000 =1 0001 =2 ..... 1111 =16

17.2.44 SDBDPL—Stream Descriptor Buffer Descriptor List Pointer Lower Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 98h
Input Stream[1]: HDBAR + B8h
Input Stream[2]: HDBAR + D8h
Input Stream[3]: HDBAR + F8h
Output Stream[0]: HDBAR + 118h
Output Stream[1]: HDBAR + 138h
Output Stream[2]: HDBAR + 158h
Output Stream[3]: HDBAR + 178h

Attribute: R/W,RO

Default Value: 00000000h

Size: 32 bits

Bit	Description
31:7	**Buffer Descriptor List Pointer Lower Base Address—**R/W. Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0, or DMA transfer may be corrupted.
6:0	Hardwired to 0 forcing alignment on 128-B boundaries.

17.2.45 SDBDPU—Stream Descriptor Buffer Descriptor List Pointer Upper Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 9Ch
Input Stream[1]: HDBAR + BCh
Input Stream[2]: HDBAR + DCh
Input Stream[3]: HDBAR + FCh
Output Stream[0]: HDBAR + 11Ch
Output Stream[1]: HDBAR + 13Ch
Output Stream[2]: HDBAR + 15Ch
Output Stream[3]: HDBAR + 17Ch

Attribute: R/W

Default Value: 00000000h

Size: 32 bits

Bit	Description
31:0	**Buffer Descriptor List Pointer Upper Base Address—**R/W. Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0, or DMA transfer may be corrupted.

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18 SMBus Controller Registers (D31:F3)

18.1 PCI Configuration Registers (SMBus—D31:F3)

Table 18-1. SMBus Controller PCI Register Address Map (SMBus—D31:F3)

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0280h	RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	05h	RO
0Bh	BCC	Base Class Code	0Ch	RO
10h	SMBMBAR0	Memory Base Address Register 0 (Bit 31:0)	00000004h	R/W
14h	SMBMBAR1	Memory Based Address Register 1 (Bit 63:32)	00000000h	R/W
20h–23h	SMB_BASE	SMBus Base Address	00000001h	R/W, RO
2Ch–2Dh	SVID	Subsystem Vendor Identification	0000h	RO
2Eh–2Fh	SID	Subsystem Identification	0000h	R/WO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	See register description	RO
40h	HOSTC	Host Configuration	00h	R/W

Note: Registers that are not shown should be treated as Reserved.(See Section 9.2 for details.)

18.1.1 VID—Vendor Identification Register (SMBus—D31:F3)

Address: 00h–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Vendor ID—**RO. This is a 16-bit value assigned to Intel

18.1.2 DID—Device Identification Register (SMBus—D31:F3)

Address:	02h–03h	Attribute:	RO
Default Value:	See bit description	Size:	16 bits

Bit	Description
15:0	**Device ID**—RO. This is a 16-bit value assigned to the PCH's SMBus controller. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Device ID Register.

18.1.3 PCICMD—PCI Command Register (SMBus—D31:F3)

Address:	04h–05h	Attributes:	RO, R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable—**R/W. 0 = Enable 1 = Disables SMBus to assert its PIRQB# signal.
9	Fast Back to Back Enable (FBE)—RO. Hardwired to 0.
8	**SERR# Enable (SERR_EN)—**R/W. 0 = Enables SERR# generation. 1 = Disables SERR# generation.
7	Wait Cycle Control (WCC)—RO. Hardwired to 0.
6	**Parity Error Response (PER)**—R/W. 0 = Disable 1 = Sets Detected Parity Error bit (D31:F3:06, bit 15) when a parity error is detected.
5	VGA Palette Snoop (VPS)—RO. Hardwired to 0.
4	Postable Memory Write Enable (PMWE)—RO. Hardwired to 0.
3	Special Cycle Enable (SCE)—RO. Hardwired to 0.
2	Bus Master Enable (BME)—RO. Hardwired to 0.
1	**Memory Space Enable (MSE)**—R/W. 0 = Disables memory mapped config space. 1 = Enables memory mapped config space.
0	**I/O Space Enable (IOSE)—**R/W. 0 = Disable 1 = Enables access to the SMBus I/O space registers as defined by the Base Address Register.

18.1.4 PCISTS—PCI Status Register (SMBus—D31:F3)

Address:	06h–07h	Attributes:	RO
Default Value:	0280h	Size:	16 bits

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	**Detected Parity Error (DPE)**—R/WC. 0 = No parity error detected. 1 = Parity error detected.
14	**Signaled System Error (SSE)—**R/WC. 0 = No system error detected. 1 = System error detected.
13	Received Master Abort (RMA)—RO. Hardwired to 0.
12	Received Target Abort (RTA)—RO. Hardwired to 0.
11	**Signaled Target Abort (STA)—**RO. Hardwired to 0.
10:9	**DEVSEL# Timing Status** (DEVT)—RO. This 2-bit field defines the timing for DEVSEL# assertion for positive decode. 01 = Medium timing.
8	Data Parity Error Detected (DPED)—RO. Hardwired to 0.
7	Fast Back to Back Capable (FB2BC)—RO. Hardwired to 1.
6	User Definable Features (UDF)—RO. Hardwired to 0.
5	66 MHz Capable (66MHZ_CAP)—RO. Hardwired to 0.
4	Capabilities List (CAP_LIST)—RO. Hardwired to 0 because there are no capability list structures in this function
3	**Interrupt Status (INTS)**—RO. This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the PCI Command register.
2:0	Reserved

18.1.5 RID—Revision Identification Register (SMBus—D31:F3)

Offset Address:	08h	Attribute:	RO
Default Value:	See bit description	Size:	8 bits

Bit	Description
7:0	**Revision ID**—RO. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Revision ID Register.

18.1.6 PI—Programming Interface Register (SMBus—D31:F3)

Offset Address:	09h	Attribute:	RO
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	Reserved

18.1.7 SCC—Sub Class Code Register (SMBus—D31:F3)

Address Offset:	0Ah	Attributes:	RO
Default Value:	05h	Size:	8 bits

Bit	Description
7:0	**Sub Class Code** (SCC)—RO. 05h = SMBus serial controller

18.1.8 BCC—Base Class Code Register (SMBus—D31:F3)

Address Offset:	0Bh	Attributes:	RO
Default Value:	0Ch	Size:	8 bits

Bit	Description
7:0	**Base Class Code** (BCC)—RO. 0Ch = Serial controller.

18.1.9 SMBMBAR0—D31_F3_SMBus Memory Base Address 0 Register (SMBus—D31:F3)

Address Offset:	10–13h	Attributes:	R/W, RO
Default Value:	00000004h	Size:	32 bits

Bit	Description
31:8	**Base Address—**R/W. Provides the 32 byte system memory base address for the PCH SMB logic.
7:4	Reserved
3	Prefetchable (PREF)—RO. Hardwired to 0. Indicates that SMBMBAR is not pre-fetchable.
2:1	**Address Range (ADDRNG)—**RO. Indicates that this SMBMBAR can be located anywhere in 64 bit address space. Hardwired to 10b.
0	**Memory Space Indicator—**RO. This read-only bit always is 0, indicating that the SMB logic is Memory mapped.

18.1.10 SMBMBAR1—D31_F3_SMBus Memory Base Address 1 Register (SMBus—D31:F3)

Address Offset:	14h–17h	Attributes:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	**Base Address—**R/W. Provides bits 63–32 system memory base address for the PCH SMB logic.

18.1.11 SMB_BASE—SMBus Base Address Register (SMBus—D31:F3)

Address Offset:	20–23h	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32-bits

Bit	Description
31:16	Reserved—RO
15:5	**Base Address—**R/W. This field provides the 32-byte system I/O base address for the PCH's SMB logic.
4:1	Reserved—RO
0	IO Space Indicator—RO. Hardwired to 1 indicating that the SMB logic is I/O mapped.

18.1.12 SVID—Subsystem Vendor Identification Register (SMBus—D31:F2/F4)

Address Offset:	2Ch–2Dh	Attribute:	RO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Subsystem Vendor ID (SVID)—**RO. The SVID register, in combination with the Subsystem ID (SID) register, enables the operating system (OS) to distinguish subsystems from each other. The value returned by reads to this register is the same as that which was written by BIOS into the IDE SVID register. ***Note:*** Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

18.1.13 SID—Subsystem Identification Register (SMBus—D31:F2/F4)

Address Offset:	2Eh–2Fh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Subsystem ID (SID)—**R/WO. The SID register, in combination with the SVID register, enables the operating system (OS) to distinguish subsystems from each other. The value returned by reads to this register is the same as that which was written by BIOS into the IDE SID register. ***Note:*** Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

18.1.14 INT_LN—Interrupt Line Register (SMBus—D31:F3)

Address Offset:	3Ch	Attributes:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	**Interrupt Line (INT_LN)—**R/W. This data is not used by the PCH. It is to communicate to software the interrupt line that the interrupt pin is connected to PIRQB#.

18.1.15 INT_PN—Interrupt Pin Register (SMBus—D31:F3)

Address Offset:	3Dh	Attributes:	RO
Default Value:	See description	Size:	8 bits

Bit	Description
7:0	**Interrupt PIN (INT_PN)**—RO. This reflects the value of D31IP.SMIP in chipset configuration space.

18.1.16 HOSTC—Host Configuration Register (SMBus—D31:F3)

Address Offset:	40h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:4	Reserved
3	**SSRESET – Soft SMBus Reset**—R/W. 0 = The hardware will reset this bit to 0 when SMBus reset operation is completed. 1 = The SMBus state machine and logic in the PCH is reset.
2	**I^2C_EN**—R/W. 0 = SMBus behavior. 1 = The PCH is enabled to communicate with I^2C devices. This will change the formatting of some commands.
1	**SMB_SMI_EN—**R/W. 0 = SMBus interrupts will not generate an SMI#. 1 = Any source of an SMB interrupt will instead be routed to generate an SMI#. Refer to Section 5.21.5 (Interrupts / SMI#). This bit needs to be set for SMBALERT# to be enabled.
0	**SMBus Host Enable (HST_EN)—**R/W. 0 = Disable the SMBus Host controller. 1 = Enable. The SMB Host controller interface is enabled to execute commands. The INTREN bit (offset SMB_BASE + 02h, bit 0) needs to be enabled for the SMB Host controller to interrupt or SMI#. Note that the SMB Host controller will not respond to any new requests until all interrupt requests have been cleared.

18.2 SMBus I/O and Memory Mapped I/O Registers

The SMBus registers (see Table 18-2)can be accessed through I/O BAR or Memory BAR registers in PCI configuration space. The offsets are the same for both I/O and Memory Mapped I/O registers.

Table 18-2. SMBus I/O and Memory Mapped I/O Register Address Map

SMB_BASE + Offset	Mnemonic	Register Name	Default	Type
00h	HST_STS	Host Status	00h	R/WC, RO
02h	HST_CNT	Host Control	00h	R/W, WO
03h	HST_CMD	Host Command	00h	R/W
04h	XMIT_SLVA	Transmit Slave Address	00h	R/W
05h	HST_D0	Host Data 0	00h	R/W
06h	HST_D1	Host Data 1	00h	R/W
07h	HOST_BLOCK_DB	Host Block Data Byte	00h	R/W
08h	PEC	Packet Error Check	00h	R/W
09h	RCV_SLVA	Receive Slave Address	44h	R/W
0Ah–0Bh	SLV_DATA	Receive Slave Data	0000h	RO
0Ch	AUX_STS	Auxiliary Status	00h	R/WC, RO
0Dh	AUX_CTL	Auxiliary Control	00h	R/W
0Eh	SMLINK_PIN_CTL	SMLink Pin Control (TCO Compatible Mode)	See register description	R/W, RO
0Fh	SMBus_PIN_CTL	SMBus Pin Control	See register description	R/W, RO
10h	SLV_STS	Slave Status	00h	R/WC
11h	SLV_CMD	Slave Command	00h	R/W
14h	NOTIFY_DADDR	Notify Device Address	00h	RO
16h	NOTIFY_DLOW	Notify Data Low Byte	00h	RO
17h	NOTIFY_DHIGH	Notify Data High Byte	00h	RO

18.2.1 HST_STS—Host Status Register (SMBus—D31:F3)

Register Offset:	SMB_BASE + 00h	Attribute:	R/WC, RO
Default Value:	00h	Size:	8-bits

All status bits are set by hardware and cleared by the software writing a one to the particular bit position. Writing a 0 to any bit position has no effect.

Bit	Description
7	**Byte Done Status (DS)**—R/WC. 0 = Software can clear this by writing a 1 to it. 1 = Host controller received a byte (for Block Read commands) or if it has completed transmission of a byte (for Block Write commands) when the 32-byte buffer is not being used. Note that this bit will be set, even on the last byte of the transfer. This bit is not set when transmission is due to the LAN interface heartbeat. This bit has no meaning for block transfers when the 32-byte buffer is enabled. ***Note:*** When the last byte of a block message is received, the host controller will set this bit. However, it will not immediately set the INTR bit (bit 1 in this register). When the interrupt handler clears the DS bit, the message is considered complete, and the host controller will then set the INTR bit (and generate another interrupt). Thus, for a block message of n bytes, the PCH will generate n+1 interrupts. The interrupt handler needs to be implemented to handle these cases. When not using the 32 Byte Buffer, hardware will drive the SMBCLK signal low when the DS bit is set until Software clears the bit. This includes the last byte of a transfer. Software must clear the DS bit before it can clear the BUSY bit.
6	**INUSE_STS**—R/W. This bit is used as semaphore among various independent software threads that may need to use the PCH's SMBus logic, and has no other effect on hardware. 0 = After a full PCI reset, a read to this bit returns a 0. 1 = After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the host controller.
5	**SMBALERT_STS**—R/WC. 0 = Interrupt or SMI# was not generated by SMBALERT#. Software clears this bit by writing a 1 to it. 1 = The source of the interrupt or SMI# was the SMBALERT# signal. This bit is only cleared by software writing a 1 to the bit position or by RSMRST# going low. If the signal is programmed as a GPIO, then this bit will never be set.
4	**FAILED—**R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = The source of the interrupt or SMI# was a failed bus transaction. This bit is set in response to the KILL bit being set to terminate the host transaction.
3	**BUS_ERR**—R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = The source of the interrupt of SMI# was a transaction collision.
2	**DEV_ERR**—R/WC. 0 = Software clears this bit by writing a 1 to it. The PCH will then deassert the interrupt or SMI#. 1 = The source of the interrupt or SMI# was due to one of the following: • Invalid Command Field, • Unclaimed Cycle (host initiated), • Host Device Time-out Error.
1	**INTR—**R/WC. This bit can only be set by termination of a command. INTR is not dependent on the INTREN bit (offset SMB_BASE + 02h, bit 0) of the Host controller register (offset 02h). It is only dependent on the termination of the command. If the INTREN bit is not set, then the INTR bit will be set, although the interrupt will not be generated. Software can poll the INTR bit in this non-interrupt case. 0 = Software clears this bit by writing a 1 to it. The PCH then deasserts the interrupt or SMI#. 1 = The source of the interrupt or SMI# was the successful completion of its last command.
0	**HOST_BUSY**—R/WC. 0 = Cleared by the PCH when the current transaction is completed. 1 = Indicates that the PCH is running a command from the host interface. No SMB registers should be accessed while this bit is set, except the BLOCK DATA BYTE Register. The BLOCK DATA BYTE Register can be accessed when this bit is set only when the SMB_CMD bits in the Host Control Register are programmed for Block command or I^2C Read command. This is necessary in order to check the DONE_STS bit.

18.2.2 HST_CNT—Host Control Register (SMBus—D31:F3)

Register Offset:	SMB_BASE + 02h	Attribute:	R/W, WO
Default Value:	00h	Size:	8-bits

Note: A read to this register will clear the byte pointer of the 32-byte buffer.

Bit	Description
7	**PEC_EN**.—R/W. 0 = SMBus host controller does not perform the transaction with the PEC phase appended. 1 = Causes the host controller to perform the SMBus transaction with the Packet Error Checking phase appended. For writes, the value of the PEC byte is transferred from the PEC Register. For reads, the PEC byte is loaded in to the PEC Register. This bit must be written prior to the write in which the **START** bit is set.
6	**START—**WO. 0 = This bit will always return 0 on reads. The HOST_BUSY bit in the Host Status register (offset 00h) can be used to identify when the PCH has finished the command. 1 = Writing a 1 to this bit initiates the command described in the SMB_CMD field. All registers should be setup prior to writing a 1 to this bit position.
5	**LAST_BYTE—**WO. This bit is used for Block Read commands. 1 = Software sets this bit to indicate that the next byte will be the last byte to be received for the block. This causes the PCH to send a NACK (instead of an ACK) after receiving the last byte. ***Note:*** Once the SECOND_TO_STS bit in TCO2_STS register (D31:F0, TCOBASE+6h, bit 1) is set, the LAST_BYTE bit also gets set. While the SECOND_TO_STS bit is set, the LAST_BYTE bit cannot be cleared. This prevents the PCH from running some of the SMBus commands (Block Read/Write, I^2C Read, Block I^2C Write).
4:2	**SMB_CMD—**R/W. The bit encoding below indicates which command the PCH is to perform. If enabled, the PCH will generate an interrupt or SMI# when the command has completed If the value is for a non-supported or reserved command, the PCH will set the device error (DEV_ERR) status bit (offset SMB_BASE + 00h, bit 2) and generate an interrupt when the START bit is set. The PCH will perform no command, and will not operate until DEV_ERR is cleared. 000 = **Quick**: The slave address and read/write value (bit 0) are stored in the transmit slave address register. 001 = **Byte**: This command uses the transmit slave address and command registers. Bit 0 of the slave address register determines if this is a read or write command. 010 = **Byte Data**: This command uses the transmit slave address, command, and DATA0 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, the DATA0 register will contain the read data. 011 = **Word Data**: This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, after the command completes, the DATA0 and DATA1 registers will contain the read data. 100 = **Process Call:** This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. After the command completes, the DATA0 and DATA1 registers will contain the read data. 101 = **Block**: This command uses the transmit slave address, command, DATA0 registers, and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block reads, the count is received and stored in the DATA0 register. Bit 0 of the slave address register selects if this is a read or write command. For writes, data is retrieved from the first n (where n is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. 110 = **I^2C Read**: This command uses the transmit slave address, command, DATA0, DATA1 registers, and the Block Data Byte register. The read data is stored in the Block Data Byte register. The PCH continues reading data until the NAK is received. 111 **= Block Process:** This command uses the transmit slave address, command, DATA0 and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block read, the count is received and stored in the DATA0 register. Bit 0 of the slave address register always indicate a write command. For writes, data is retrieved from the first m (where m is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. ***Note:*** E32B bit in the Auxiliary Control register must be set for this command to work.

Bit	Description
1	**KILL**—R/W. 0 = Normal SMBus host controller functionality. 1 = Kills the current host transaction taking place, sets the FAILED status bit, and asserts the interrupt (or SMI#). This bit, once set, must be cleared by software to allow the SMBus host controller to function normally.
0	**INTREN**—R/W. 0 = Disable. 1 = Enable the generation of an interrupt or SMI# upon the completion of the command.

18.2.3 HST_CMD—Host Command Register (SMBus—D31:F3)

Register Offset: SMB_BASE + 03h Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	This 8-bit field is transmitted by the host controller in the command field of the SMBus protocol during the execution of any command.

18.2.4 XMIT_SLVA—Transmit Slave Address Register (SMBus—D31:F3)

Register Offset: SMB_BASE + 04h Attribute: R/W
Default Value: 00h Size: 8 bits

This register is transmitted by the host controller in the slave address field of the SMBus protocol.

Bit	Description
7:1	**Address**—R/W. This field provides a 7-bit address of the targeted slave.
0	**RW**—R/W. Direction of the host transfer. 0 = Write 1 = Read

18.2.5 HST_D0—Host Data 0 Register (SMBus—D31:F3)

Register Offset: SMB_BASE + 05h Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Data0/Count**—R/W. This field contains the 8-bit data sent in the DATA0 field of the SMBus protocol. For block write commands, this register reflects the number of bytes to transfer. This register should be programmed to a value between 1 and 32 for block counts. A count of 0 or a count above 32 will result in unpredictable behavior. The host controller does not check or log invalid block counts.

18.2.6 HST_D1—Host Data 1 Register (SMBus—D31:F3)

Register Offset: SMB_BASE + 06h Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Data1**—R/W. This 8-bit register is transmitted in the DATA1 field of the SMBus protocol during the execution of any command.

18.2.7 Host_BLOCK_DB—Host Block Data Byte Register (SMBus—D31:F3)

Register Offset:	SMB_BASE + 07h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	**Block Data (BDTA)—**R/W. This is either a register, or a pointer into a 32-byte block array, depending upon whether the E32B bit is set in the Auxiliary Control register. When the E32B bit (offset SMB_BASE + 0Dh, bit 1) is cleared, this is a register containing a byte of data to be sent on a block write or read from on a block read. When the E32B bit is set, reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array, which is reset to 0 by reading the HCTL register (offset 02h). The index pointer then increments automatically upon each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0. When the E2B bit is set, for writes, software will write up to 32-bytes to this register as part of the setup for the command. After the Host controller has sent the Address, Command, and Byte Count fields, it will send the bytes in the SRAM pointed to by this register. When the E2B bit is cleared for writes, software will place a single byte in this register. After the host controller has sent the address, command, and byte count fields, it will send the byte in this register. If there is more data to send, software will write the next series of bytes to the SRAM pointed to by this register and clear the DONE_STS bit. The controller will then send the next byte. During the time between the last byte being transmitted to the next byte being transmitted, the controller will insert wait-states on the interface. When the E2B bit is set for reads, after receiving the byte count into the Data0 register, the first series of data bytes go into the SRAM pointed to by this register. If the byte count has been exhausted or the 32-byte SRAM has been filled, the controller will generate an SMI# or interrupt (depending on configuration) and set the DONE_STS bit. Software will then read the data. During the time between when the last byte is read from the SRAM to when the DONE_STS bit is cleared, the controller will insert wait-states on the interface.

18.2.8 PEC—Packet Error Check (PEC) Register (SMBus—D31:F3)

Register Offset:	SMB_BASE + 08h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	**PEC_DATA—**R/W. This 8-bit register is written with the 8-bit CRC value that is used as the SMBus PEC data prior to a write transaction. For read transactions, the PEC data is loaded from the SMBus into this register and is then read by software. Software must ensure that the INUSE_STS bit is properly maintained to avoid having this field over-written by a write transaction following a read transaction.

18.2.9 RCV_SLVA—Receive Slave Address Register (SMBus—D31:F3)

Register Offset:	SMB_BASE + 09h	Attribute:	R/W
Default Value:	44h	Size:	8 bits
Lockable:	No	Power Well:	Resume

Bit	Description
7	Reserved
6:0	**SLAVE_ADDR—**R/W. This field is the slave address that the PCH decodes for read and write cycles. the default is not 0, so the SMBus Slave Interface can respond even before the processor comes up (or if the processor is dead). This register is cleared by RSMRST#, but not by PLTRST#.

18.2.10 SLV_DATA—Receive Slave Data Register (SMBus—D31:F3)

Register Offset:	SMB_BASE + 0Ah–0Bh	Attribute:	RO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Resume

This register contains the 16-bit data value written by the external SMBus master. The processor can then read the value from this register. This register is reset by RSMRST#, but not PLTRST#.

Bit	Description
15:8	**Data Message Byte 1 (DATA_MSG1)**—RO. See Section 5.21.8 for a discussion of this field.
7:0	**Data Message Byte 0 (DATA_MSG0)**—RO. See Section 5.21.8 for a discussion of this field.

18.2.11 AUX_STS—Auxiliary Status Register (SMBus—D31:F3)

Register Offset:	SMB_BASE + 0Ch	Attribute:	R/WC, RO
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Resume

Bit	Description
7:2	Reserved
1	**SMBus TCO Mode (STCO)**—RO. This bit reflects the strap setting of TCO compatible mode vs. Advanced TCO mode. 0 = The PCH is in the compatible TCO mode. 1 = The PCH is in the advanced TCO mode.
0	**CRC Error (CRCE)—**R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set if a received message contained a CRC error. When this bit is set, the DERR bit of the host status register will also be set. This bit will be set by the controller if a software abort occurs in the middle of the CRC portion of the cycle or an abort happens after the PCH has received the final data bit transmitted by an external slave.

18.2.12 AUX_CTL—Auxiliary Control Register (SMBus—D31:F3)

Register Offset:	SMB_BASE + 0Dh	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Resume

Bit	Description
7:2	Reserved
1	**Enable 32-Byte Buffer (E32B)—**R/W. 0 = Disable. 1 = Enable. When set, the Host Block Data register is a pointer into a 32-byte buffer, as opposed to a single register. This enables the block commands to transfer or receive up to 32-bytes before the PCH generates an interrupt.
0	**Automatically Append CRC (AAC)—**R/W. 0 = The PCH will Not automatically append the CRC. 1 = The PCH will automatically append the CRC. This bit must not be changed during SMBus transactions or undetermined behavior will result. It should be programmed only once during the lifetime of the function.

18.2.13 SMLINK_PIN_CTL—SMLink Pin Control Register (SMBus—D31:F3)

Register Offset:	SMB_BASE + 0Eh	Attribute:	R/W, RO
Default Value:	See below	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

This register is only applicable in the TCO compatible mode.

Bit	Description
7:3	Reserved
2	**SMLINK_CLK_CTL**—R/W. 0 = The PCH will drive the SML0CLK pin low, independent of what the other SMLink logic would otherwise indicate for the SML0CLK pin. 1 = The SML0CLK pin is **not** overdriven low. The other SMLink logic controls the state of the pin. (Default)
1	**SML0DATA_CUR_STS**—RO. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SML0DATA pin. This allows software to read the current state of the pin. 0 = Low 1 = High
0	**SML0CLK_CUR_STS**—RO. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SML0CLK pin. This allows software to read the current state of the pin. 0 = Low 1 = High

18.2.14 SMBus_PIN_CTL—SMBus Pin Control Register (SMBus—D31:F3)

Register Offset:	SMB_BASE + 0Fh	Attribute:	R/W, RO
Default Value:	See below	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:3	Reserved
2	**SMBCLK_CTL**—R/W. 1 = The SMBCLK pin is **not** overdriven low. The other SMBus logic controls the state of the pin. 0 = The PCH drives the SMBCLK pin low, independent of what the other SMB logic would otherwise indicate for the SMBCLK pin. (Default)
1	**SMBDATA_CUR_STS**—RO. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SMBDATA pin. This allows software to read the current state of the pin. 0 = Low 1 = High
0	**SMBCLK_CUR_STS**—RO. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SMBCLK pin. This allows software to read the current state of the pin. 0 = Low 1 = High

18.2.15 SLV_STS—Slave Status Register (SMBus—D31:F3)

Register Offset:	SMB_BASE + 10h	Attribute:	R/WC
Default Value:	00h	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

All bits in this register are implemented in the 64 kHz clock domain. Therefore, software must poll this register until a write takes effect before assuming that a write has completed internally.

Bit	Description
7:1	Reserved
0	**HOST_NOTIFY_STS—**R/WC. The PCH sets this bit to a 1 when it has completely received a successful Host Notify Command on the SMBus pins. Software reads this bit to determine that the source of the interrupt or SMI# was the reception of the Host Notify Command. Software clears this bit after reading any information needed from the Notify address and data registers by writing a 1 to this bit. Note that the PCH will allow the Notify Address and Data registers to be over-written once this bit has been cleared. When this bit is 1, the PCH will NACK the first byte (host address) of any new "Host Notify" commands on the SMBus pins. Writing a 0 to this bit has no effect.

18.2.16 SLV_CMD—Slave Command Register (SMBus—D31:F3)

Register Offset:	SMB_BASE + 11h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:2	Reserved
2	**SMBALERT_DIS—**R/W. 0 = Allows the generation of the interrupt or SMI#. 1 = Software sets this bit to block the generation of the interrupt or SMI# due to the SMBALERT# source. This bit is logically inverted and ANDed with the SMBALERT_STS bit (offset SMB_BASE + 00h, bit 5). The resulting signal is distributed to the SMI# and/or interrupt generation logic. This bit does not effect the wake logic.
1	**HOST_NOTIFY_WKEN—**R/W. Software sets this bit to 1 to enable the reception of a Host Notify command as a wake event. When enabled this event is "OR'd" in with the other SMBus wake events and is reflected in the SMB_WAK_STS bit of the General Purpose Event 0 Status register. 0 = Disable 1 = Enable
0	**HOST_NOTIFY_INTREN—**R/W. Software sets this bit to 1 to enable the generation of interrupt or SMI# when HOST_NOTIFY_STS (offset SMB_BASE + 10h, bit 0) is 1. This enable does not affect the setting of the HOST_NOTIFY_STS bit. When the interrupt is generated, either PIRQB# or SMI# is generated, depending on the value of the SMB_SMI_EN bit (D31:F3:40h, bit 1). If the HOST_NOTIFY_STS bit is set when this bit is written to a 1, then the interrupt (or SMI#) will be generated. The interrupt (or SMI#) is logically generated by AND'ing the STS and INTREN bits. 0 = Disable 1 = Enable

18.2.17 NOTIFY_DADDR—Notify Device Address Register (SMBus—D31:F3)

Register Offset:	SMB_BASE + 14h	Attribute:	RO
Default Value:	00h	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:1	**DEVICE_ADDRESS—**RO. This field contains the 7-bit device address received during the Host Notify protocol of the SMBus 2.0 Specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit (D31:F3:SMB_BASE +10, bit 0) is set to 1.
0	Reserved

18.2.18 NOTIFY_DLOW—Notify Data Low Byte Register (SMBus—D31:F3)

Register Offset:	SMB_BASE + 16h	Attribute:	RO
Default Value:	00h	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:0	**DATA_LOW_BYTE—**RO. This field contains the first (low) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit (D31:F3:SMB_BASE +10, bit 0) is set to 1.

18.2.19 NOTIFY_DHIGH—Notify Data High Byte Register (SMBus—D31:F3)

Register Offset:	SMB_BASE + 17h	Attribute:	RO
Default Value:	00h	Size:	8 bits

Note: This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:0	**DATA_HIGH_BYTE—**RO. This field contains the second (high) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit (D31:F3:SMB_BASE +10, bit 0) is set to 1.

§

19 PCI Express* Configuration Registers

19.1 PCI Express* Configuration Registers (PCI Express—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Note: Register address locations that are not shown in Table 19-1, should be treated as Reserved.

Note: This section assumes the default PCI Express Function Number-to-Root Port mapping is used. Function numbers for a given root port are assignable through the "Root Port Function Number and Hide for PCI Express Root Ports" registers (RCBA+0404h).

Table 19-1. PCI Express* Configuration Registers Address Map (PCI Express—D28:F0/F1/F2/F3/F4/F5/F6/F7/) (Sheet 1 of 3)

Offset	Mnemonic	Register Name	Function 0-5 Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0010h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	04h	RO
0Bh	BCC	Base Class Code	06h	RO
0Ch	CLS	Cache Line Size	00h	R/W
0Dh	PLT	Primary Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	81h	RO
18h–1Ah	BNUM	Bus Number	000000h	R/W
1Bh	SLT	Secondary Latency Timer	00h	RO
1Ch–1Dh	IOBL	I/O Base and Limit	0000h	R/W, RO
1Eh–1Fh	SSTS	Secondary Status Register	0000h	R/WC
20h–23h	MBL	Memory Base and Limit	00000000h	R/W
24h–27h	PMBL	Prefetchable Memory Base and Limit	00010001h	R/W, RO
28h–2Bh	PMBU32	Prefetchable Memory Base Upper 32 Bits	00000000h	R/W
2Ch–2Fh	PMLU32	Prefetchable Memory Limit Upper 32 Bits	00000000h	R/W
34h	CAPP	Capabilities List Pointer	40h	RO
3Ch–3Dh	INTR	Interrupt Information	See bit description	R/W, RO
3Eh–3Fh	BCTRL	Bridge Control Register	0000h	R/W
40h–41h	CLIST	Capabilities List	8010	RO
42h–43h	XCAP	PCI Express Capabilities	0041	R/WO, RO

Table 19-1. PCI Express* Configuration Registers Address Map (PCI Express—D28:F0/F1/F2/F3/F4/F5/F6/F7/) (Sheet 2 of 3)

Offset	Mnemonic	Register Name	Function 0-5 Default	Type
44h–47h	DCAP	Device Capabilities	00000FE0h	RO
48h–49h	DCTL	Device Control	0000h	R/W, RO
4Ah–4Bh	DSTS	Device Status	0010h	R/WC, RO
4Ch–4Fh	LCAP	Link Capabilities	See bit description	R/W, RO, R/WO
50h–51h	LCTL	Link Control	0000h	R/W, WO, RO
52h–53h	LSTS	Link Status	See bit description	RO
54h–57h	SLCAP	Slot Capabilities	00000060h	R/WO, RO
58h–59h	SLCTL	Slot Control	0000h	R/W, RO
5Ah–5Bh	SLSTS	Slot Status	0000h	R/WC, RO
5Ch–5Dh	RCTL	Root Control	0000h	R/W
60h–63h	RSTS	Root Status	00000000h	R/WC, RO
64h–67h	DCAP2	Device Capabilities 2	00000016h	RO
68h–69h	DCTL2	Device Control 2	0000h	R/W, RO
70h–71h	LCTL2	Link Control 2	0002h	RO
72h–73h	LSTS2	Link Status 2	0000h	RO
80h–81h	MID	Message Signaled Interrupt Identifiers	9005h	RO
82h–83h	MC	Message Signaled Interrupt Message Control	0000h	R/W, RO
84h–87h	MA	Message Signaled Interrupt Message Address	00000000h	R/W
88h–89h	MD	Message Signaled Interrupt Message Data	0000h	R/W
90h–91h	SVCAP	Subsystem Vendor Capability	A00Dh	RO
94h–97h	SVID	Subsystem Vendor Identification	00000000h	R/WO
A0h–A1h	PMCAP	Power Management Capability	0001h	RO
A2h–A3h	PMC	PCI Power Management Capability	C802h	RO
A4–A7h	PMCS	PCI Power Management Control and Status	00000000h	R/W, RO
D4–D7h	MPC2	Miscellaneous Port Configuration 2	00000000h	R/W, RO
D8–DBh	MPC	Miscellaneous Port Configuration	08110000h	R/W
DC–DFh	SMSCS	SMI/SCI Status Register	00000000h	R/WC
E1h	RPDCGEN	Rort Port Dynamic Clock Gating Enable	00h	R/W
E8–EBh	PECR1	PCI Express Configuration Register 1	00000020h	R/W
EC–EFh	PECR3	PCI Express Configuration Register 3	00000000h	R/W
11Ch–143h	—	Reserved	—	—
104h–107h	UES	Uncorrectable Error Status	See bit description	R/WC, RO
108h–10Bh	UEM	Uncorrectable Error Mask	00000000h	R/WO, RO
10Ch–10Fh	UEV	Uncorrectable Error Severity	00060011h	RO
110h–113h	CES	Correctable Error Status	00000000h	R/WC
114h–117h	CEM	Correctable Error Mask	00000000h	R/WO

Table 19-1. PCI Express* Configuration Registers Address Map (PCI Express—D28:F0/F1/F2/F3/F4/F5/F6/F7/) (Sheet 3 of 3)

Offset	Mnemonic	Register Name	Function 0-5 Default	Type
118h–11Bh	AECC	Advanced Error Capabilities and Control	00000000h	RO
130h–133h	RES	Root Error Status	00000000h	R/WC, RO
300–303h	PECR2	PCI Express Configuration Register 2	60005007h	R/W
318h	PEETM	PCI Express Extended Test Mode	See bit description	RO
324h–327h	PEC1	PCI Express Configuration Register 1	00000000h	RO, R/W

19.1.1 VID—Vendor Identification Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset: 00h–01h
Attribute: RO
Default Value: 8086h
Size: 16 bits

Bit	Description
15:0	**Vendor ID**—RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

19.1.2 DID—Device Identification Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset: 02h–03h
Attribute: RO
Default Value: Port 1= Bit Description
Port 2= Bit Description
Port 3= Bit Description
Port 4= Bit Description
Port 5= Bit Description
Port 6= Bit Description
Port 7= Bit Description
Port 8= Bit Description
Size: 16 bits

Bit	Description
15:0	**Device ID**—RO. This is a 16-bit value assigned to the PCH's PCI Express controller. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Device ID Register.

19.1.3 PCICMD—PCI Command Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset: 04h–05h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable**—R/W. This disables pin-based INTx# interrupts on enabled Hot-Plug and power management events. This bit has no effect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt for Hot-Plug or power management and MSI is not enabled. 1 = Internal INTx# messages will not be generated. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set.
9	Fast Back to Back Enable (FBE)—Reserved per the *PCI Express Base Specification*.
8	**SERR# Enable (SEE)**—R/W. 0 = Disable. 1 = Enables the root port to generate an SERR# message when PSTS.SSE is set.
7	Wait Cycle Control (WCC)—Reserved per the *PCI Express Base Specification*.
6	**Parity Error Response (PER)**—R/W. 0 = Disable. 1 = Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	VGA Palette Snoop (VPS)—Reserved per the *PCI Express Base Specification*.
4	Postable Memory Write Enable (PMWE)—Reserved per the *PCI Express Base Specification*.
3	Special Cycle Enable (SCE)—Reserved per the *PCI Express Base Specification*.
2	**Bus Master Enable (BME)**—R/W. 0 = Disable. Memory and I/O requests received at a Root Port must be handled as Unsupported Requests 1 = Enable. Allows the root port to forward cycles onto the backbone from a PCI Express device. ***Note:*** This bit does not affect forwarding of completions in either upstream or downstream direction nor controls forwarding of requests other than memory or I/O.PCI Express
1	**Memory Space Enable (MSE)**—R/W. 0 = Disable. Memory cycles within the range specified by the memory base and limit registers are master aborted on the backbone. 1 = Enable. Allows memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI Express device.
0	**I/O Space Enable (IOSE)**—R/W. This bit controls access to the I/O space registers. 0 = Disable. I/O cycles within the range specified by the I/O base and limit registers are master aborted on the backbone. 1 = Enable. Allows I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI Express device.

19.1.4 PCISTS—PCI Status Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset: 06h–07h
Default Value: 0010h
Attribute: R/WC, RO
Size: 16 bits

Bit	Description
15	**Detected Parity Error (DPE)—**R/WC. 0 = No parity error detected. 1 = Set when the root port receives a command or data from the backbone with a parity error. This is set even if PCIMD.PER (D28:F0/F1/F2/F3:04, bit 6) is not set.
14	**Signaled System Error (SSE)—**R/WC. 0 = No system error signaled. 1 = Set when the root port signals a system error to the internal SERR# logic.
13	**Received Master Abort (RMA)—**R/WC. 0 = Root port has not received a completion with unsupported request status from the backbone. 1 = Set when the root port receives a completion with unsupported request status from the backbone.
12	**Received Target Abort (RTA)—**R/WC. 0 = Root port has not received a completion with completer abort from the backbone. 1 = Set when the root port receives a completion with completer abort from the backbone.
11	**Signaled Target Abort (STA)—**R/WC. 0 = No target abort received. 1 = Set whenever the root port forwards a target abort received from the downstream device onto the backbone.
10:9	DEVSEL# Timing Status (DEV_STS)—Reserved per the *PCI Express Base Specification*.
8	**Master Data Parity Error Detected (DPED)**—R/WC. 0 = No data parity error received. 1 = Set when the root port receives a completion with a data parity error on the backbone and PCIMD.PER (D28:F0/F1/F2/F3:04, bit 6) is set.
7	Fast Back to Back Capable (FB2BC)—Reserved per the *PCI Express Base Specification*.
6	Reserved
5	66 MHz Capable—Reserved per the *PCI Express Base Specification*.
4	**Capabilities List**—RO. Hardwired to 1. Indicates the presence of a capabilities list.
3	**Interrupt Status**—RO. Indicates status of Hot-Plug and power management interrupts on the root port that result in INTx# message generation. 0 = Interrupt is deasserted. 1 = Interrupt is asserted. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of PCICMD.Interrupt Disable bit (D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7:04h:bit 10).
2:0	Reserved

19.1.5 RID—Revision Identification Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Offset Address: 08h
Default Value: See bit description
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Revision ID**—RO. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Revision ID Register.

19.1.6 PI—Programming Interface Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset: 09h
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Programming Interface**—RO. 00h = No specific register level programming interface defined.

19.1.7 SCC—Sub Class Code Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset: 0Ah
Default Value: 04h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Sub Class Code (SCC)**—RO. This field is determined by bit 2 of the MPC register (D28:F0-5:Offset D8h, bit 2). 04h = PCI-to-PCI bridge. 00h = Host Bridge.

19.1.8 BCC—Base Class Code Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset: 0Bh
Default Value: 06h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Base Class Code (BCC)**—RO. 06h = Indicates the device is a bridge device.

19.1.9 CLS—Cache Line Size Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset: 0Ch
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Cache Line Size (CLS)**—R/W. This is read/write but contains no functionality, per the *PCI Express Base Specification*.

19.1.10 PLT—Primary Latency Timer Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset: 0Dh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:3	Latency Count. Reserved per the *PCI Express Base Specification*.
2:0	Reserved

19.1.11 HEADTYP—Header Type Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset: 0Eh
Default Value: 81h
Attribute: RO
Size: 8 bits

Bit	Description
7	**Multi-Function Device**—RO. 0 = Single-function device. 1 = Multi-function device.
6:0	**Configuration Layout**—RO. This field is determined by bit 2 of the MPC register (D28:F0-5:Offset D8h, bit 2). 00h = Indicates a Host Bridge. 01h = Indicates a PCI-to-PCI bridge.

19.1.12 BNUM—Bus Number Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset: 18–1Ah
Default Value: 000000h
Attribute: R/W
Size: 24 bits

Bit	Description
23:16	**Subordinate Bus Number (SBBN)**—R/W. Indicates the highest PCI bus number below the bridge.
15:8	**Secondary Bus Number (SCBN)**—R/W. Indicates the bus number the port.
7:0	**Primary Bus Number (PBN)**—R/W. Indicates the bus number of the backbone.

19.1.13 SLT—Secondary Latency Timer (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset: 1Bh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	Secondary Latency Timer—Reserved for a Root Port per the *PCI Express Base Specification*.

19.1.14 IOBL—I/O Base and Limit Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset: 1Ch–1Dh
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:12	**I/O Limit Address (IOLA)**—R/W. I/O Base bits corresponding to address lines 15:12 for 4-KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	**I/O Limit Address Capability (IOLC)**—RO. Indicates that the bridge does not support 32-bit I/O addressing.
7:4	**I/O Base Address (IOBA)**—R/W. I/O Base bits corresponding to address lines 15:12 for 4-KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	**I/O Base Address Capability (IOBC)**—RO. Indicates that the bridge does not support 32-bit I/O addressing.

19.1.15 SSTS—Secondary Status Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset:	1Eh–1Fh	Attribute:	R/WC
Default Value:	0000h	Size:	16 bits

Bit	Description
15	**Detected Parity Error (DPE)**—R/WC. 0 = No error. 1 = The port received a poisoned TLP
14	**Received System Error (RSE)**—R/WC. 0 = No error. 1 = The port received an ERR_FATAL or ERR_NONFATAL message from the device.
13	**Received Master Abort (RMA)**—R/WC. 0 = Unsupported Request not received. 1 = The port received a completion with "Unsupported Request" status from the device.
12	**Received Target Abort (RTA)**—R/WC. 0 = Completion Abort not received. 1 = The port received a completion with "Completion Abort" status from the device.
11	**Signaled Target Abort (STA)**—R/WC. 0 = Completion Abort not sent. 1 = The port generated a completion with "Completion Abort" status to the device.
10:9	Secondary DEVSEL# Timing Status (SDTS): Reserved per *PCI Express Base Specification*.
8	**Data Parity Error Detected (DPD)**—R/WC. 0 = Conditions below did not occur 1 = Set when the BCTRL.PERE (D28:FO/F1/F2/F3/F4/F5:3E: bit 0) is set, and either of the following two conditions occurs: • Port receives completion marked poisoned. • Port poisons a write request to the secondary side.
7	Secondary Fast Back to Back Capable (SFBC): Reserved per *PCI Express Base Specification*.
6	Reserved
5	Secondary 66 MHz Capable (SC66): Reserved per *PCI Express Base Specification*.
4:0	Reserved

19.1.16 MBL—Memory Base and Limit Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset:	20h–23h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE (D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7:04:bit 1) is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME (D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7:04:bit 2) is set. The comparison performed is MB ≥ AD[31:20] ≤ ML.

Bit	Description
31:20	**Memory Limit (ML)—**R/W. These bits are compared with bits 31:20 of the incoming address to determine the upper 1-MB aligned value of the range.
19:16	Reserved
15:4	**Memory Base (MB)**—R/W. These bits are compared with bits 31:20 of the incoming address to determine the lower 1-MB aligned value of the range.
3:0	Reserved

19.1.17 PMBL—Prefetchable Memory Base and Limit Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset:	24h–27h	Attribute:	R/W, RO
Default Value:	00010001h	Size:	32 bits

Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE (D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7;04, bit 1) is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME (D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7;04, bit 2) is set. The comparison performed is PMBU32:PMB ≥ AD[63:32]:AD[31:20] ≤ PMLU32:PML.

Bit	Description
31:20	**Prefetchable Memory Limit (PML)—**R/W. These bits are compared with bits 31:20 of the incoming address to determine the upper 1-MB aligned value of the range.
19:16	**64-bit Indicator (I64L)**—RO. Indicates support for 64-bit addressing
15:4	**Prefetchable Memory Base (PMB)**—R/W. These bits are compared with bits 31:20 of the incoming address to determine the lower 1-MB aligned value of the range.
3:0	**64-bit Indicator (I64B)**—RO. Indicates support for 64-bit addressing

19.1.18 PMBU32—Prefetchable Memory Base Upper 32 Bits Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset:	28h–2Bh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	**Prefetchable Memory Base Upper Portion (PMBU)—**R/W. Upper 32-bits of the prefetchable address base.

19.1.19 PMLU32—Prefetchable Memory Limit Upper 32 Bits Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset: 2Ch–2Fh
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**Prefetchable Memory Limit Upper Portion (PMLU)—**R/W. Upper 32-bits of the prefetchable address limit.

19.1.20 CAPP—Capabilities List Pointer Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset: 34h
Default Value: 40h
Attribute: R0
Size: 8 bits

Bit	Description
7:0	**Capabilities Pointer (PTR)—**RO. Indicates that the pointer for the first entry in the capabilities list is at 40h in configuration space.

19.1.21 INTR—Interrupt Information Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset: 3Ch–3Dh
Default Value: See bit description
Function Level Reset: No (Bits 7:0 only)
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:8	**Interrupt Pin (IPIN)—**RO. Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values, which reflect the reset state of the D28IP register in chipset config space: **Port** — **Reset Value** 1 — D28IP.P1IP 2 — D28IP.P2IP 3 — D28IP.P3IP 4 — D28IP.P4IP 5 — D28IP.P5IP 6 — D28IP.P6IP 7 — D28IP.P7IP 8 — D28IP.P8IP ***Note:*** The value that is programmed into D28IP is always reflected in this register.
7:0	**Interrupt Line (ILINE)—**R/W. Default = 00h. Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register. These bits are not reset by FLR.

19.1.22 BCTRL—Bridge Control Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7/F6/F7)

Address Offset: 3Eh–3Fh
Attribute: R/W
Default Value: 0000h
Size: 16 bits

Bit	Description
15:12	Reserved
11	Discard Timer SERR# Enable (DTSE): Reserved per *PCI Express Base Specification*, Revision 1.0a
10	Discard Timer Status (DTS): Reserved per *PCI Express Base Specification*, Revision 1.0a.
9	Secondary Discard Timer (SDT): Reserved per *PCI Express Base Specification*, Revision 1.0a.
8	Primary Discard Timer (PDT): Reserved per *PCI Express Base Specification*, Revision 1.0a.
7	Fast Back to Back Enable (FBE): Reserved per *PCI Express Base Specification*, Revision 1.0a.
6	**Secondary Bus Reset (SBR)**—R/W. Triggers a hot reset on the PCI Express port.
5	Master Abort Mode (MAM): Reserved per Express specification.
4	**VGA 16-Bit Decode (V16)—**R/W. 0 = VGA range is enabled. 1 = The I/O aliases of the VGA range (see BCTRL:VE definition below), are not enabled, and only the base I/O ranges can be decoded
3	**VGA Enable (VE)**—R/W. 0 = The ranges below will not be claimed off the backbone by the root port. 1 = The following ranges will be claimed off the backbone by the root port: • Memory ranges A0000h–BFFFFh • I/O ranges 3B0h – 3BBh and 3C0h – 3DFh, and all aliases of bits 15:10 in any combination of 1s
2	**ISA Enable (IE)**—R/W. This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64 KB of PCI I/O space. 0 = The root port will not block any forwarding from the backbone as described below. 1 = The root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1-KB block (offsets 100h to 3FFh).
1	**SERR# Enable (SE)**—R/W. 0 = The messages described below are not forwarded to the backbone. 1 = ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone.
0	**Parity Error Response Enable (PERE)**—R/W. When set, 0 = Poisoned write TLPs and completions indicating poisoned TLPs will not set the SSTS.DPD (D28:F0/F1/F2/F3/F4/F5/F6/F7:1E, bit 8). 1 = Poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD (D28:F0/F1/F2/F3/F4/F5/F6/F7:1E, bit 8).

19.1.23 CLIST—Capabilities List Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset: 40–41h
Attribute: RO
Default Value: 8010h
Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT)—**RO. Value of 80h indicates the location of the next pointer.
7:0	**Capability ID (CID)—**RO. Indicates this is a PCI Express capability.

19.1.24 XCAP—PCI Express* Capabilities Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	42h–43h	Attribute:	R/WO, RO
Default Value:	0042h	Size:	16 bits

Bit	Description
15:14	Reserved
13:9	**Interrupt Message Number (IMN)**—RO. The PCH does not have multiple MSI interrupt numbers.
8	**Slot Implemented (SI)—**R/WO. Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
7:4	**Device / Port Type (DT)**—RO. Indicates this is a PCI Express root port.
3:0	**Capability Version (CV)**—RO. Indicates PCI Express 2.0.

19.1.25 DCAP—Device Capabilities Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	44h–47h	Attribute:	RO
Default Value:	00008000h	Size:	32 bits

Bit	Description
31:28	Reserved
27:26	Captured Slot Power Limit Scale (CSPS)—RO. Not supported.
25:18	Captured Slot Power Limit Value (CSPV)—RO. Not supported.
17:16	Reserved
15	**Role Based Error Reporting (RBER)—**RO. Indicates that this device implements the functionality defined in the Error Reporting ECN as required by the PCI Express 2.0 specification.
14:12	Reserved
11:9	Endpoint L1 Acceptable Latency (E1AL)—RO. This field is reserved with a setting of 000b for devices other than Endpoints, per the PCI Express 2.0 specification.
8:6	Endpoint L0s Acceptable Latency (E0AL)—RO. This field is reserved with a setting of 000b for devices other than Endpoints, per the PCI Express 2.0 specification.
5	**Extended Tag Field Supported (ETFS)**—RO. Indicates that 8-bit tag fields are supported.
4:3	**Phantom Functions Supported (PFS)**—RO. No phantom functions supported.
2:0	**Max Payload Size Supported (MPS)**—RO. Indicates the maximum payload size supported is 128B.

19.1.26 DCTL—Device Control Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	48h–49h	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15	Reserved
14:12	Max Read Request Size (MRRS)—RO. Hardwired to 0.
11	Enable No Snoop (ENS)—RO. Not supported. The root port will never issue non-snoop requests.
10	**Aux Power PM Enable (APME)**—R/W. The operating system will set this bit to 1 if the device connected has detected aux power. It has no effect on the root port otherwise.
9	Phantom Functions Enable (PFE)—RO. Not supported.
8	Extended Tag Field Enable (ETFE)—RO. Not supported.
7:5	**Max Payload Size (MPS)**—R/W. The root port only supports 128-B payloads, regardless of the programming of this field.
4	Enable Relaxed Ordering (ERO)—RO. Not supported.
3	**Unsupported Request Reporting Enable (URE)**—R/W. 0 = The root port will ignore unsupported request errors. 1 = Allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	**Fatal Error Reporting Enable (FEE)**—R/W. 0 = The root port will ignore fatal errors. 1 = Enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	**Non-Fatal Error Reporting Enable (NFE)**—R/W. 0 = The root port will ignore non-fatal errors. 1 = Enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	**Correctable Error Reporting Enable (CEE)**—R/W. 0 = The root port will ignore correctable errors. 1 = Enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

19.1.27 DSTS—Device Status Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	4Ah–4Bh	Attribute:	R/WC, RO
Default Value:	0010h	Size:	16 bits

Bit	Description
15:6	Reserved
5	**Transactions Pending (TDP)**—RO. This bit has no meaning for the root port since only one transaction may be pending to the PCH, so a read of this bit cannot occur until it has already returned to 0.
4	**AUX Power Detected (APD)—**RO. The root port contains AUX power for wakeup.
3	**Unsupported Request Detected (URD)**—R/WC. Indicates an unsupported request was detected.
2	**Fatal Error Detected (FED)**—R/WC. Indicates a fatal error was detected. 0 = Fatal has not occurred. 1 = A fatal error occurred from a data link protocol error, link training error, buffer overflow, or malformed TLP.
1	**Non-Fatal Error Detected (NFED)**—R/WC. Indicates a non-fatal error was detected. 0 = Non-fatal has not occurred. 1 = A non-fatal error occurred from a poisoned TLP, unexpected completions, unsupported requests, completer abort, or completer timeout.
0	**Correctable Error Detected (CED)**—R/WC. Indicates a correctable error was detected. 0 = Correctable has not occurred. 1 = The port received an internal correctable error from receiver errors / framing errors, TLP CRC error, DLLP CRC error, replay num rollover, replay timeout.

19.1.28 LCAP—Link Capabilities Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	4Ch–4Fh	Attribute:	R/WO, RO
Default Value:	See bit description	Size:	32 bits

Bit	Description
31:24	**Port Number (PN)**—RO. Indicates the port number for the root port. This value is different for each implemented port: Function / Port # / Value of PN Field D28:F0 / 1 / 01h D28:F1 / 2 / 02h D28:F2 / 3 / 03h D28:F3 / 4 / 04h D28:F4 / 5 / 05h D28:F5 / 6 / 06h D28:F6 / 7 / 07h D28:F7 / 8 / 08h
23:21	Reserved
20	**Link Active Reporting Capable (LARC)**—RO. Hardwired to 1 to indicate that this port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19:18	Reserved

Bit	Description
17:15	**L1 Exit Latency (EL1)—**RO. 000b = Less than 1 us 001b = 1 us to less than 2 us 010b = 2 us to less than 4 us 011b = 4 us to less than 8 us 100b = 8 us to less than 16 us 101b = 16 us to less than 32 us 110b = 32 us to 64 us 111b = more than 64 us
14:12	**L0s Exit Latency (EL0)**—R/WO. Indicates as exit latency based upon common-clock configuration. **.CLT.CCC** — **Value of EL0 (these bits)** 0 — MPC.UCEL (D28:F0/F1/F2/F3:D8h:bits20:18) 1 — MPC.CCEL (D28:F0/F1/F2/F3:D8h:bits17:15) ***Note:*** LCLT.CCC is at D28:F0/F1/F2/F3/F4/F5/F6/F7:50h:bit 6
11:10	**Active State Link PM Support (APMS)**—R/WO. Indicates what level of active state link power management is supported on the root port. **Bits** — **Definition** 00b — Neither L0s nor L1 are supported 01b — L0s Entry Supported 10b — L1 Entry Supported 11b — Both L0s and L1 Entry Supported
9:4	**Maximum Link Width (MLW)**—RO. For the root ports, several values can be taken, based upon the value of the chipset config register field RPC.PC1 (Chipset Config Registers:Offset 0224h:bits1:0) for Ports 1-4 and RPC.PC2 (Chipset Config Registers:Offset 0224h:bits1:0) for Ports 5 and 6 **Value of MLW Field** **Port #** — **RPC.PC1=00b** — **RPC.PC1=11b** 1 — 01h — 04h 2 — 01h — 01h 3 — 01h — 01h 4 — 01h — 01h **Port #** — **RPC.PC2=00b** — **RPC.PC2=11b** 5 — 01h — 04h 6 — 01h — 01h 7 — 01h — 01h 8 — 01h — 01h
3:0	**Maximum Link Speed (MLS)**—RO. 0001b = indicates the link speed is 2.5 Gb/s 0010b = 5.0 Gb/s and 2.5Gb/s link speeds supported These bits report a value of 0001b if Gen2 disable bit 14 is set in the MPC register, else the value reported is 0010b

19.1.29 LCTL—Link Control Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	50h–51h	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:10	Reserved
9	**Hardware Autonomous Width Disable** – RO. Hardware never attempts to change the link width except when attempting to correct unreliable Link operation.
8	Reserved
7	**Extended Synch (ES)**—R/W. 0 = Extended synch disabled. 1 = Forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0.
6	**Common Clock Configuration (CCC)—**R/W. 0 = The PCH and device are not using a common reference clock. 1 = The PCH and device are operating with a distributed common reference clock.
5	**Retrain Link (RL)**—R/W. 0 = This bit always returns 0 when read. 1 = The root port will train its downstream link. ***Note:*** Software uses LSTS.LT (D28:F0/F1/F2/F3/F4/F5/F6/F7:52, bit 11) to check the status of training. ***Note:*** It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that is already in progress.
4	**Link Disable (LD)**—R/W. 0 = Link enabled. 1 = The root port will disable the link.
3	**Read Completion Boundary Control (RCBC)**—RO. Indicates the read completion boundary is 64 bytes.
2	Reserved
1:0	**Active State Link PM Control (APMC)**—R/W. Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled

19.1.30 LSTS—Link Status Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	52h–53h	Attribute:	RO
Default Value:	See bit description	Size:	16 bits

Bit	Description
15:14	Reserved
13	**Data Link Layer Active (DLLA)**—RO. Default value is 0b. 0 = Data Link Control and Management State Machine is not in the DL_Active state 1 = Data Link Control and Management State Machine is in the DL_Active state
12	**Slot Clock Configuration (SCC)**—RO. Set to 1b to indicate that the PCH uses the same reference clock as on the platform and does not generate its own clock.
11	**Link Training (LT)—**RO. Default value is 0b. 0 = Link training completed. 1 = Link training is occurring.
10	Link Training Error (LTE)—RO. Not supported. Set value is 0b.
9:4	**Negotiated Link Width (NLW)**—RO. This field indicates the negotiated width of the given PCI Express link. The contents of this NLW field is undefined if the link has not successfully trained. **Port #** — **Possible Values** 1 — 000001b, 000010b, 000100b 2 — 000001b 3 — 000001b, 000010b 4 — 000001b 5 — 000001b, 000010b, 000100b 6 — 000001b 7 — 000001b, 000010b 8 — 000001b ***Note:*** 000001b = x1 link width, 000010b =x2 linkwidth, 000100b = x4 linkwidth
3:0	**Link Speed (LS)**—RO. This field indicates the negotiated Link speed of the given PCI Express link. 0001h = Link is 2.5 Gb/s. 0010h = Link is 5.0 Gb/s

19.1.31 SLCAP—Slot Capabilities Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset: 54h–57h
Attribute: R/WO, RO
Default Value: 00040060h
Size: 32 bits

Bit	Description
31:19	**Physical Slot Number (PSN)**—R/WO. This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
18:17	Reserved
16:15	**Slot Power Limit Scale (SLS)—**R/WO. Specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:7	**Slot Power Limit Value (SLV)**—R/WO. Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	**Hot Plug Capable (HPC)**—R/WO. 1b = Indicates that Hot-Plug is supported.
5	**Hot Plug Surprise (HPS)**—R/WO. 1b = Indicates the device may be removed from the slot without prior notification.
4	**Power Indicator Present (PIP)**—RO. 0b = Indicates that a power indicator LED is not present for this slot.
3	**Attention Indicator Present (AIP)**—RO. 0b = Indicates that an attention indicator LED is not present for this slot.
2	**MRL Sensor Present (MSP)**—RO. 0b = Indicates that an MRL sensor is not present.
1	**Power Controller Present (PCP)**—RO. 0b = Indicates that a power controller is not implemented for this slot.
0	**Attention Button Present (ABP)**—RO. 0b = Indicates that an attention button is not implemented for this slot.

19.1.32 SLCTL—Slot Control Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset: 58h–59h
Attribute: R/W, RO
Default Value: 0000h
Size: 16 bits

Bit	Description
15:13	Reserved
12	**Link Active Changed Enable (LACE)—**R/W. When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field (D28:F0/F1/F2/F3/F4/F5/F6/F7:52h:bit 13) is changed.
11	Reserved
10	**Power Controller Control (PCC)—**RO.This bit has no meaning for module based Hot-Plug.
9:6	Reserved
5	**Hot-Plug Interrupt Enable (HPE)**—R/W. 0 = Hot-plug interrupts based on Hot-Plug events is disabled. 1 = Enables generation of a Hot-Plug interrupt on enabled hot-plug events.
4	Reserved
3	**Presence Detect Changed Enable (PDE)**—R/W. 0 = Hot-plug interrupts based on presence detect logic changes is disabled. 1 = Enables the generation of a hot-plug interrupt or wake message when the presence detect logic changes state.
2:0	Reserved

19.1.33 SLSTS—Slot Status Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	5Ah–5Bh	Attribute:	R/WC, RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:9	Reserved
8	**Link Active State Changed (LASC)**—R/WC. This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register (D28:F0/F1/F2/F3/F4/F5/F6/F7:52h:bit 13) is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device.
7	Reserved
6	**Presence Detect State (PDS)**—RO. If XCAP.SI (D28:F0/F1/F2/F3/F4/F5/F6/F7:42h:bit 8) is set (indicating that this root port spawns a slot), then this bit: 0 = Indicates the slot is empty. 1 = Indicates the slot has a device connected. Otherwise, if XCAP.SI is cleared, this bit is always set (1).
5	MRL Sensor State (MS)—Reserved as the MRL sensor is not implemented.
4	Reserved
3	**Presence Detect Changed (PDC)**—R/WC. 0 = No change in the PDS bit. 1 = The PDS bit changed states.
2	**MRL Sensor Changed (MSC)**—Reserved as the MRL sensor is not implemented.
1	**Power Fault Detected (PFD)**—Reserved as a power controller is not implemented.
0	Reserved

19.1.34 RCTL—Root Control Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset: 5Ch–5Dh
Attribute: R/W
Default Value: 0000h
Size: 16 bits

Bit	Description
15:4	Reserved
3	**PME Interrupt Enable (PIE)**—R/W. 0 = Interrupt generation disabled. 1 = Interrupt generation enabled when PCISTS.Inerrupt Status (D28:F0/F1/F2/F3/F4/F5/F6/F7:60h, bit 16) is in a set state (either due to a 0 to 1 transition, or due to this bit being set with RSTS.IS already set).
2	**System Error on Fatal Error Enable (SFE)—**R/W. 0 = An SERR# will not be generated. 1 = An SERR# will be generated, assuming CMD.SEE (D28:F0/F1/F2/F3/F4/F5/F6/F7:04, bit 8) is set, if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port.
1	**System Error on Non-Fatal Error Enable (SNE)**—R/W. 0 = An SERR# will not be generated. 1 = An SERR# will be generated, assuming CMD.SEE (D28:F0/F1/F2/F3/F4/F5/F6/F7:04, bit 8) is set, if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port.
0	**System Error on Correctable Error Enable (SCE)**—R/W. 0 = An SERR# will not be generated. 1 = An SERR# will be generated, assuming CMD.SEE (D28:F0/F1/F2/F3/F4/F5/F6/F7:04, bit 8) if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port.

19.1.35 RSTS—Root Status Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset: 60h–63h
Attribute: R/WC, RO
Default Value: 00000000h
Size: 32 bits

Bit	Description
31:18	Reserved
17	**PME Pending (PP)**—RO. 0 = When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. 1 = Indicates another PME is pending when the PME status bit is set.
16	**PME Status (PS)—**R/WC. 0 = PME was not asserted. 1 = Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	**PME Requestor ID (RID)**—RO. Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set.

19.1.36 DCAP2—Device Capabilities 2 Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	64h–67h	Attribute:	RO
Default Value:	00000016h	Size:	32 bits

Bit	Description
31:5	Reserved
4	**Completion Timeout Disable Supported (CTDS)—**RO. A value of 1b indicates support for the Completion Timeout Disable mechanism.
3:0	**Completion Timeout Ranges Supported (CTRS) –** RO. This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is hardwired to support 10 ms to 250 ms and 250 ms to 4 s.

19.1.37 DCTL2—Device Control 2 Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	68h–69h	Attribute:	RO, R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15:5	Reserved
4	**Completion Timeout Disable (CTD)—**R/W. When set to 1b, this bit disables the Completion Timeout mechanism. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued.
3:0	**Completion Timeout Value (CTV)—**R/W. This field allows system software to modify the Completion Timeout value. 0000b = Default range: 40–50 ms (specification range 50 us to 50 ms) 0101b = 40–50 ms (specification range is 16 ms to 55 ms) 0110b = 160–170 ms (specification range is 65 ms to 210 ms) 1001b = 400–500 ms (specification range is 260 ms to 900 ms) 1010b = 1.6–1.7 s (specification range is 1 s to 3.5 s) All other values are Reserved. ***Note:*** Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either on when this value was changed or on when each request w as issued.

19.1.38 LCTL2—Link Control 2 Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	70h–71h	Attribute:	RO
Default Value:	0002h	Size:	16 bits

Bit	Description
15:13	Reserved
12	**Compliance De-Emphasis (CD)—**R/W. This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 0 = 6 dB 1 = 3.5 dB When the Link is operating at 2.5 GT/s, the setting of this bit has no effect. The default value of this bit is 0b. This bit is intended for debug, compliance testing purposes. System firmware and software are allowed to modify this bit only during debug or compliance testing.
11:5	Reserved
4	**Enter Compliance (EC)—**R/W. Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link.
3:0	**Target Link Speed (TLS)**—RO. This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. 0001b = 2.5 GT/s Target Link Speed 0010b = 5.0 GT/s and 2.5 GT/s Target Link Speeds All other values reserved.

19.1.39 LSTS2—Link Status 2 Register (PCI Express**—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	72h–73h	Attribute:	RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:1	Reserved
0	**Current De-emphasis Level (CDL)**—RO. When the Link is operating at 5 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 0 = 6 dB 1 = 3.5 dB The value in this bit is undefined when the Link is operating at 2.5 GT/s speed.

19.1.40 MID—Message Signaled Interrupt Identifiers Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	80h–81h	Attribute:	RO
Default Value:	9005h	Size:	16 bits

Bit	Description
15:8	**Next Pointer (NEXT)**—RO. Indicates the location of the next pointer in the list.
7:0	**Capability ID (CID)—**RO. Capabilities ID indicates MSI.

19.1.41 MC—Message Signaled Interrupt Message Control Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset: 82–83h
Attribute: R/W, RO
Default Value: 0000h
Size: 16 bits

Bit	Description
15:8	Reserved
7	**64 Bit Address Capable (C64)—**RO. Capable of generating a 32-bit message only.
6:4	**Multiple Message Enable (MME)—**R/W. These bits are R/W for software compatibility, but only one message is ever sent by the root port.
3:1	**Multiple Message Capable (MMC)—**RO. Only one message is required.
0	**MSI Enable (MSIE)—**R/W. 0 = MSI is disabled. 1 = MSI is enabled and traditional interrupt pins are not used to generate interrupts. ***Note:*** CMD.BME (D28:F0/F1/F2/F3/F4/F5/F6/F7:04h:bit 2) must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.

19.1.42 MA—Message Signaled Interrupt Message Address Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset: 84h–87h
Attribute: R/W
Default Value: 00000000h
Size: 32 bits

Bit	Description
31:2	**Address (ADDR)**—R/W. Lower 32 bits of the system specified message address, always DW aligned.
1:0	Reserved

19.1.43 MD—Message Signaled Interrupt Message Data Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset: 88h–89h
Attribute: R/W
Default Value: 0000h
Size: 16 bits

Bit	Description
15:0	**Data (DATA)**—R/W. This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[15:0]) during the data phase of the MSI memory write transaction.

19.1.44 SVCAP—Subsystem Vendor Capability Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset: 90h–91h
Attribute: RO
Default Value: A00Dh
Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT)**—RO. Indicates the location of the next pointer in the list.
7:0	**Capability Identifier (CID)**—RO. Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

19.1.45 SVID—Subsystem Vendor Identification Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	94h–97h	Attribute:	R/WO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:16	**Subsystem Identifier (SID)**—R/WO. Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	**Subsystem Vendor Identifier (SVID)**—R/WO. Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

19.1.46 PMCAP—Power Management Capability Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	A0h–A1h	Attribute:	RO
Default Value:	0001h	Size:	16 bits

Bit	Description
15:8	**Next Capability (NEXT)**—RO. Indicates this is the last item in the list.
7:0	**Capability Identifier (CID)**—RO. Value of 01h indicates this is a PCI power management capability.

19.1.47 PMC—PCI Power Management Capabilities Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	A2h–A3h	Attribute:	RO
Default Value:	C802h	Size:	16 bits

Bit	Description
15:11	**PME_Support (PMES)**—RO. Indicates PME# is supported for states D0, $D3_{HOT}$ and $D3_{COLD}$. The root port does not generate PME#, but reporting that it does is necessary for some legacy operating systems to enable PME# in devices connected behind this root port.
10	D2_Support (D2S)—RO. The D2 state is not supported.
9	D1_Support (D1S)—RO The D1 state is not supported.
8:6	**Aux_Current (AC)**—RO. Reports 375 mA maximum suspend well current required when in the $D3_{COLD}$ state.
5	**Device Specific Initialization (DSI)**—RO. 1 = Indicates that no device-specific initialization is required.
4	Reserved
3	**PME Clock (PMEC)—**RO. 1 = Indicates that PCI clock is not required to generate PME#.
2:0	**Version (VS)**—RO. Indicates support for *Revision 1.1 of the PCI Power Management Specification*.

19.1.48 PMCS—PCI Power Management Control and Status Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	A4h–A7h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:24	Reserved
23	Bus Power / Clock Control Enable (BPCE)—Reserved per *PCI Express Base Specification, Revision 1.0a*.
22	B2/B3 Support (B23S)—Reserved per *PCI Express Base Specification, Revision 1.0a*.
21:16	Reserved
15	**PME Status (PMES)—**RO. 1 = Indicates a PME was received on the downstream link.
14:9	Reserved
8	**PME Enable (PMEE)—**R/W. 1 = Indicates PME is enabled. The root port takes no action on this bit, but it must be R/W for some legacy operating systems to enable PME# on devices connected to this root port. This bit is sticky and resides in the resume well. The reset for this bit is RSMRST# which is not asserted during a warm reset.
7:2	Reserved
1:0	**Power State (PS)—**R/W. This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 = D0 state 11 = $D3_{HOT}$ state ***Note:*** When in the $D3_{HOT}$ state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into $D3_{HOT}$. If software attempts to write a '10' or '01' to these bits, the write will be ignored.

19.1.49 MPC2—Miscellaneous Port Configuration Register 2 (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	D4h–D7h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:5	Reserved
4	**ASPM Control Override Enable (ASPMCOEN)—**R/W. 1 = Root port will use the values in the ASPM Control Override registers 0 = Root port will use the ASPM Registers in the Link Control register. ***Notes:*** This register allows BIOS to control the root port ASPM settings instead of the operating system.
3:2	**ASPM Control Override (ASPMO)—**R/W. Provides BIOS control of whether root port should enter L0s or L1 or both. 00 = Disabled 01 = L0s Entry Enabled 10 = L1 Entry Enabled 11 = L0s and L1 Entry Enabled.
1	**EOI Forwarding Disable (EOIFD)—**R/W. When set, EOI messages are not claimed on the backbone by this port an will not be forwarded across the PCIe link. 0 = EOI forwarding is enabled. 1 = EOI forwarding is disabled.
0	**L1 Completion Timeout Mode (LICTM)—**R/W. 0 = PCI Express Specification Compliant. Completion timeout is disabled during software initiated L1, and enabled during ASPM initiate L1. 1 = Completion timeout is enabled during L1, regardless of how L1 entry was initiated.

19.1.50 MPC—Miscellaneous Port Configuration Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	D8h–DBh	Attribute:	R/W, RO
Default Value:	08110000h	Size:	32 bits

Bit	Description
31	**Power Management SCI Enable (PMCE)—**R/W. 0 = SCI generation based on a power management event is disabled. 1 = Enables the root port to generate SCI whenever a power management event is detected.
30	**Hot-Plug SCI Enable (HPCE)**—R/W. 0 = SCI generation based on a Hot-Plug event is disabled. 1 = Enables the root port to generate SCI whenever a hot-plug event is detected.
29	**Link Hold Off (LHO)**—R/W. 1 = Port will not take any TLP. This is used during loopback mode to fill up the downstream queue.
28	**Address Translator Enable (ATE)**—R/W. This bit is used to enable address translation using the AT bits in this register during loopback mode. 0 = Disable 1 = Enable
27	**Reserved**
26	**Invalid Receive Bus Number Check Enable (IRBNCE)**—R/W. When set, the receive transaction layer will signal an error if the bus number of a Memory request does not fall within the range between SCBN and SBBN. If this check is enabled and the request is a memory write, it is treated as an Unsupported Request. If this check is enabled and the request is a non-posted memory read request, the request is considered a Malformed TLP and a fatal error. Messages, I/O, Config, and Completions are never checked for valid bus number.

Bit	Description
25	**Invalid Receive Range Check Enable (IRRCE)**—R/W. When set, the receive transaction layer will treat the TLP as an Unsupported Request error if the address range of a Memory request does not outside the range between prefetchable and non-prefetchable base and limit. Messages, I/O, Configuration, and Completions are never checked for valid address ranges.
24	**BME Receive Check Enable (BMERCE)**—R/W. When set, the receive transaction layer will treat the TLP as an Unsupported Request error if a memory read or write request is received and the Bus Master Enable bit is not set. Messages, IO, Config, and Completions are never checked for BME.
23	Reserved
22	**Detect Override (FORCEDET)—**R/W. 0 = Normal operation. Detected output from AFE is sampled for presence detection. 1 = Override mode. Ignores AFE detect output and link training proceeds as if a device were detected.
21	**Flow Control During L1 Entry (FCDL1E)—**R/W. 0 = No flow control update DLLPs sent during L1 Ack transmission. 1 = Flow control update DLLPs sent during L1 Ack transmission as required to meet the 30 µs periodic flow control update.
20:18	**Unique Clock Exit Latency (UCEL)—**R/W. This value represents the L0s Exit Latency for unique-clock configurations (LCTL.CCC = 0) (D28:F0/F1/F2/F3/F4/F5/F6/F7:Offset 50h:bit 6). It defaults to 512 ns to less than 1 µs, but may be overridden by BIOS.
17:15	**Common Clock Exit Latency (CCEL)—**R/W. This value represents the L0s Exit Latency for common-clock configurations (LCTL.CCC = 1) (D28:F0/F1/F2/F3/F4/F5/F6/F7:Offset 50h:bit 6). It defaults to 128 ns to less than 256 ns, but may be overridden by BIOS.
14:8	Reserved
7	**Port I/OxApic Enable (PAE)—**R/W. 0 = Hole is disabled. 1 = A range is opened through the bridge for the following memory addresses: **Port #** — **Address** 1 — FEC1_0000h – FEC1_7FFFh 2 — FEC1_8000h – FEC1_FFFFh 3 — FEC2_0000h – FEC2_7FFFh 4 — FEC2_8000h – FEC2_FFFFh 5 — FEC3_0000h – FEC3_7FFFh 6 — FEC3_8000h – FEC3_FFFFh 7 — FEC4_0000h – FEC4_7FFFh 8 — FEC4_8000h – FEC4_FFFFh
6:3	Reserved
2	**Bridge Type (BT)—**RO. This register can be used to modify the Base Class and Header Type fields from the default P2P bridge to a Host Bridge. Having the root port appear as a Host Bridge is useful in some HEDT configurations. 0 = The root port bridge type is a P2P Bridge, Header Sub-Class = 04h, and Header Type = Type 1. 1 = The root port bridge type is a P2P Bridge, Header Sub-Class = 00h, and Header Type = Type 0.
1	**Hot Plug SMI Enable (HPME)—**R/W. 0 = SMI generation based on a Hot-Plug event is disabled. 1 = Enables the root port to generate SMI whenever a Hot-Plug event is detected.
0	**Power Management SMI Enable (PMME)—**R/W. 0 = SMI generation based on a power management event is disabled. 1 = Enables the root port to generate SMI whenever a power management event is detected.

19.1.51 SMSCS—SMI/SCI Status Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	DCh–DFh	Attribute:	R/WC
Default Value:	00000000h	Size:	32 bits

Bit	Description
31	**Power Management SCI Status (PMCS)—**R/WC. 1 = PME control logic needs to generate an interrupt, and this interrupt has been routed to generate an SCI.
30	**Hot-Plug SCI Status (HPCS)**—R/WC. 1 = Hot-Plug controller needs to generate an interrupt, and has this interrupt been routed to generate an SCI.
29:5	Reserved
4	**Hot-Plug Link Active State Changed SMI Status (HPLAS)**—R/WC. 1 = SLSTS.LASC (D28:F0/F1/F2/F3/F4/F5/F6/F7:5A, bit 8) transitioned from 0-to-1, and MPC.HPME (D28:F0/F1/F2/F3/F4/F5/F6/F7:D8, bit 1) is set. When this bit is set, an SMI# will be generated.
3	**Hot-Plug Command Completed SMI Status (HPCCM)**—R/WC. 1 = SLSTS.CC (D28:F0/F1/F2/F3/F4/F5/F6/F7:5A, bit 4) transitioned from 0-to-1, and MPC.HPME (D28:F0/F1/F2/F3/F4/F5/F6/F7:D8, bit 1) is set. When this bit is set, an SMI# will be generated.
2	**Hot-Plug Attention Button SMI Status (HPABM)**—R/WC. 1 = SLSTS.ABP (D28:F0/F1/F2/F3/F4/F5/F6/F7:5A, bit 0) transitioned from 0-to-1, and MPC.HPME (D28:F0/F1/F2/F3/F4/F5/F6/F7:D8, bit 1) is set. When this bit is set, an SMI# will be generated.
1	**Hot-Plug Presence Detect SMI Status (HPPDM)**—R/WC. 1 = SLSTS.PDC (D28:F0/F1/F2/F3/F4/F5/F6/F7:5A, bit 3) transitioned from 0-to-1, and MPC.HPME (D28:F0/F1/F2/F3/F4/F5/F6/F7:D8, bit 1) is set. When this bit is set, an SMI# will be generated.
0	**Power Management SMI Status (PMMS)**—R/WC. 1 = RSTS.PS (D28:F0/F1/F2/F3/F4/F5/F6/F7:60, bit 16) transitioned from 0-to-1, and MPC.PMME (D28:F0/F1/F2/F3/F4/F5/F6/F7:D8, bit 1) is set.

19.1.52 RPDCGEN—Root Port Dynamic Clock Gating Enable (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	E1h	Attribute:	R/W
Default Value:	00h	Size:	8-bits

Bits	Description
7:4	Reserved. RO
3	**Shared Resource Dynamic Link Clock Gating Enable (SRDLCGEN)—**R/W. 0 = Disables dynamic clock gating of the shared resource link clock domain. 1 = Enables dynamic clock gating on the root port shared resource link clock domain. Only the value from Port 1 is used for ports 1–4. Only the value from Port 5 is used for ports 5-8.
2	**Shared Resource Dynamic Backbone Clock Gate Enable (SRDBCGEN)—**R/W. 0 = Disables dynamic clock gating of the shared resource backbone clock domain. 1 = Enables dynamic clock gating on the root port shared resource backbone clock domain. Only the value from Port 1 is used for ports 1–4. Only the value from Port 5 is used for ports 5-8.
1	**Root Port Dynamic Link Clock Gate Enable (RPDLCGEN)—**R/W. 0 = Disables dynamic clock gating of the root port link clock domain. 1 = Enables dynamic clock gating on the root port link clock domain.
0	**Root Port Dynamic Backbone Clock Gate Enable (RPDBCGEN)—**R/W. 0 = Disables dynamic clock gating of the root port backbone clock domain. 1 = Enables dynamic clock gating on the root port backbone clock domain.

19.1.53 PECR1—PCI Express* Configuration Register 1 (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	E8h–EBh	Attribute:	R/W
Default Value:	00000020h	Size:	32 bits

Bit	Description
31:2	Reserved
1	**PECR1 Field 2**—R/W. BIOS may set this bit to 1.
0	Reserved

19.1.54 PECR3—PCI Express* Configuration Register 3 (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	ECh–EFh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:2	Reserved
1	**Subtractive Decode Compatibility Device ID (SDCDID)**—R/W. 0 = This function reports the device Device ID value assigned to the PCI Express Root Ports listed in the *Intel® X79 Express Chipset Specification Update*. 1 = This function reports a Device ID of 244Eh. If subtractive decode (SDE) is enabled, having this bit as '0' allows the function to present a Device ID that is recognized by the operating system.
0	**Subtractive Decode Enable (SDE)**—R/W. 0 = Subtractive decode is disabled this function and will only claim transactions positively. 1 = This port will subtractively forward transactions across the PCIe link downstream memory and IO transactions that are not positively claimed any internal device or bridge. Software must ensure that only one PCH device is enabled for Subtractive decode at a time.

19.1.55 UES—Uncorrectable Error Status Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	104h–107h	Attribute:	R/WC, RO
Default Value:	00000000000x0xxx0x0x0000000x0000b	Size:	32 bits

This register maintains its state through a platform reset. It loses its state upon suspend.

Bit	Description
31:21	Reserved
20	**Unsupported Request Error Status (URE)**—R/WC. Indicates an unsupported request was received.
19	ECRC Error Status (EE)—RO. ECRC is not supported.
18	**Malformed TLP Status (MT)**—R/WC. Indicates a malformed TLP was received.
17	**Receiver Overflow Status (RO)**—R/WC. Indicates a receiver overflow occurred.
16	**Unexpected Completion Status (UC)**—R/WC. Indicates an unexpected completion was received.
15	**Completion Abort Status (CA)**—R/WC. Indicates a completer abort was received.
14	**Completion Timeout Status (CT)**—R/WC. Indicates a completion timed out. This bit is set if Completion Timeout is enabled and a completion is not returned within the time specified by the Completion TImeout Value
13	Flow Control Protocol Error Status (FCPE)—RO. Flow Control Protocol Errors not supported.
12	**Poisoned TLP Status (PT)**—R/WC. Indicates a poisoned TLP was received.
11:5	Reserved
4	**Data Link Protocol Error Status (DLPE)**—R/WC. Indicates a data link protocol error occurred.
3:1	Reserved
0	**Training Error Status (TE)**—RO. Training Errors not supported.

19.1.56 UEM—Uncorrectable Error Mask (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	108h–10Bh	Attribute:	R/WO, RO
Default Value:	00000000h	Size:	32 bits

When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled.

Bit	Description
31:21	Reserved
20	**Unsupported Request Error Mask (URE)**—R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5/F6/F7:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5/F6/F7:144) is masked.
19	ECRC Error Mask (EE)—RO. ECRC is not supported.
18	**Malformed TLP Mask (MT)**—R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5/F6/F7:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5/F6/F7:144) is masked.
17	**Receiver Overflow Mask (RO)**—R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5/F6/F7:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5/F6/F7:144) is masked.
16	**Unexpected Completion Mask (UC)**—R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5/F6/F7:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5/F6/F7:144) is masked.
15	**Completion Abort Mask (CA)**—R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5/F6/F7:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5/F6/F7:144) is masked.
14	**Completion Timeout Mask (CT)**—R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5/F6/F7:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5/F6/F7:144) is masked.
13	**Flow Control Protocol Error Mask (FCPE)—**RO. Flow Control Protocol Errors not supported.
12	**Poisoned TLP Mask (PT)**—R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5/F6/F7:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5/F6/F7:144) is masked.
11:5	Reserved
4	**Data Link Protocol Error Mask (DLPE)**—R/WO. 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5/F6/F7:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5/F6/F7:144) is masked.
3:1	Reserved
0	**Training Error Mask (TE)**—RO. Training Errors not supported

19.1.57 UEV—Uncorrectable Error Severity (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	10Ch–10Fh	Attribute:	RO, R/W
Default Value:	00060011h	Size:	32 bits

Bit	Description
31:21	Reserved
20	**Unsupported Request Error Severity (URE)**—R/W. 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
19	**ECRC Error Severity (EE)**—RO. ECRC is not supported.
18	**Malformed TLP Severity (MT)**—R/W. 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
17	**Receiver Overflow Severity (RO)**—R/W. 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
16	Reserved
15	**Completion Abort Severity (CA)—**R/W. 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
14	Reserved
13	**Flow Control Protocol Error Severity (FCPE)**—RO. Flow Control Protocol Errors not supported.
12	**Poisoned TLP Severity (PT)**—R/W. 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
11:5	Reserved
4	**Data Link Protocol Error Severity (DLPE)**—R/W. 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
3:1	Reserved
0	Training Error Severity (TE)—R/W. TE is not supported.

19.1.58 CES—Correctable Error Status Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	110h–113h	Attribute:	R/WC
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:14	Reserved
13	**Advisory Non-Fatal Error Status (ANFES)—**R/WC. 0 = Advisory Non-Fatal Error did not occur. 1 = Advisory Non-Fatal Error did occur.
12	**Replay Timer Timeout Status (RTT)**—R/WC. Indicates the replay timer timed out.
11:9	Reserved
8	**Replay Number Rollover Status (RNR)—**R/WC. Indicates the replay number rolled over.
7	**Bad DLLP Status (BD)**—R/WC. Indicates a bad DLLP was received.
6	**Bad TLP Status (BT)—**R/WC. Indicates a bad TLP was received.
5:1	Reserved
0	**Receiver Error Status (RE)—**R/WC. Indicates a receiver error occurred.

19.1.59 CEM—Correctable Error Mask Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	114h–117h	Attribute:	R/WO
Default Value:	00002000h	Size:	32 bits

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled.

Bit	Description
31:14	Reserved
13	**Advisory Non-Fatal Error Mask (ANFEM)**—R/WO. 0 = Does not mask Advisory Non-Fatal errors. 1 = Masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting. ***Note:*** The correctable error detected bit in device status register is set whenever the Advisory Non-Fatal error is detected, independent of this mask bit.
12	**Replay Timer Timeout Mask (RTT)**—R/WO. Mask for replay timer timeout.
11:9	Reserved
8	**Replay Number Rollover Mask (RNR)—**R/WO. Mask for replay number rollover.
7	**Bad DLLP Mask (BD)**—R/WO. Mask for bad DLLP reception.
6	**Bad TLP Mask (BT)—**R/WO. Mask for bad TLP reception.
5:1	Reserved
0	**Receiver Error Mask (RE)—**R/WO. Mask for receiver errors.

19.1.60 AECC—Advanced Error Capabilities and Control Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset: 118h–11Bh Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:9	Reserved
8	ECRC Check Enable (ECE)—RO. ECRC is not supported.
7	ECRC Check Capable (ECC)—RO. ECRC is not supported.
6	ECRC Generation Enable (EGE)—RO. ECRC is not supported.
5	ECRC Generation Capable (EGC)—RO. ECRC is not supported.
4:0	First Error Pointer (FEP)—RO. Identifies the bit position of the last error reported in the Uncorrectable Error Status Register.

19.1.61 RES—Root Error Status Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset: 130h–133h Attribute: R/WC, RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:27	**Advanced Error Interrupt Message Number (AEMN)**—RO. There is only one error interrupt allocated.
26:7	Reserved
6	**Fatal Error Messages Received (FEMR)—**RO. Set when one or more Fatal Uncorrectable Error Messages have been received.
5	**Non-Fatal Error Messages Received (NFEMR)—**RO. Set when one or more Non-Fatal Uncorrectable error messages have been received
4	**First Uncorrectable Fatal (FUF)—**RO. Set when the first Uncorrectable Error message received is for a fatal error.
3	**Multiple ERR_FATAL/NONFATAL Received (MENR)**—RO. For the PCH, only one error will be captured.
2	**ERR_FATAL/NONFATAL Received (ENR)**—R/WC. 0 = No error message received. 1 = Either a fatal or a non-fatal error message is received.
1	**Multiple ERR_COR Received (MCR)**—RO. For the PCH, only one error will be captured.
0	**ERR_COR Received (CR)**—R/WC. 0 = No error message received. 1 = A correctable error message is received.

19.1.62 PECR2—PCI Express* Configuration Register 2 (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	320–323h	Attribute:	R/W
Default Value:	60005007h	Size:	32 bits

Bit	Description
31:20	Reserved
21	**PECR2 Field 1**—R/W. BIOS must set this bit to 1b.
20:0	Reserved

19.1.63 PEETM—PCI Express* Extended Test Mode Register (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	324–327h	Attribute:	RO
Default Value:	See Description	Size:	32 bits

Bit	Description
31:5	Reserved
4	**Lane Reversal (LR)** — RO. This bit reads the setting of the PCIELR1 soft strap for port 1 and the PCIELR2 soft strap for port 5. 0 = No Lane reversal (default). 1 = PCI Express lanes 0-3 (register in port 1) or lanes 4-7 (register in port 5) are reversed. ***Notes:*** 1. The port configuration straps must be set such that Port 1 or Port 5 is configured as a x4 port using lanes 0–3, or 4–7 when Lane Reversal is enabled. x2 lane reversal is not supported. 2. This bit is only valid on port 1 (for ports 1–4) or port 5 (for ports 5–8).
3	Reserved
2	**Scrambler Bypass Mode (BAU)**—R/W. 0 = Normal operation. Scrambler and descrambler are used. 1 = Bypasses the data scrambler in the transmit direction and the data de-scrambler in the receive direction. ***Note:*** This functionality intended for debug/testing only. ***Note:*** If bypassing scrambler with the PCH root port 1 in x4 configuration, each PCH root port must have this bit set.
1:0	Reserved

19.1.64 PEC1—PCI Express* Configuration Register 1 (PCI Express*—D28:F0/F1/F2/F3/F4/F5/F6/F7)

Address Offset:	330h	Attribute:	RO, R/W
Default Value:	14000016h	Size:	32 bits

Bit	Description
31:8	Reserved
7:0	**PEC1 Field 1**—R/W. BIOS must program this field to 40h.

§

20 High Precision Event Timer Registers

The timer registers are memory-mapped in a non-indexed scheme. This allows the processor to directly access each register without having to use an index register. The timer register space is 1024 bytes. The registers are generally aligned on 64-bit boundaries to simplify implementation with IA64 processors. There are four possible memory address ranges beginning at 1) FED0_0000h, 2) FED0_1000h, 3) FED0_2000h, 4) FED0_3000h. The choice of address range will be selected by configuration bits in the High Precision Timer Configuration Register (Chipset Config Registers:Offset 3404h).

Behavioral Rules:

1. Software must not attempt to read or write across register boundaries. For example, a 32-bit access should be to offset x0h, x4h, x8h, or xCh. 32-bit accesses should not be to 01h, 02h, 03h, 05h, 06h, 07h, 09h, 0Ah, 0Bh, 0Dh, 0Eh, or 0Fh. Any accesses to these offsets will result in an unexpected behavior, and may result in a master abort. However, these accesses should not result in system hangs. 64-bit accesses can only be to x0h and must not cross 64-bit boundaries.
2. Software should not write to read-only registers.
3. Software should not expect any particular or consistent value when reading reserved registers or bits.

20.1 Memory Mapped Registers

Table 20-1. Memory-Mapped Registers (Sheet 1 of 2)

Offset	Mnemonic	Register	Default	Type
000–007h	GCAP_ID	General Capabilities and Identification	0429B17F80 86A201h	RO
008–00Fh	—	Reserved	—	—
010–017h	GEN_CONF	General Configuration	00000000 00000000h	R/W
018–01Fh	—	Reserved	—	—
020–027h	GINTR_STA	General Interrupt Status	00000000 00000000h	R/WC, R/W
028–0EFh	—	Reserved	—	—
0F0–0F7h	MAIN_CNT	Main Counter Value	N/A	R/W
0F8–0FFh	—	Reserved	—	—
100–107h	TIM0_CONF	Timer 0 Configuration and Capabilities	N/A	R/W, RO
108–10Fh	TIM0_COMP	Timer 0 Comparator Value	N/A	R/W
110–11Fh	—	Reserved	—	—
120–127h	TIM1_CONF	Timer 1 Configuration and Capabilities	N/A	R/W, RO
128–12Fh	TIM1_COMP	Timer 1 Comparator Value	N/A	R/W
130–13Fh	—	Reserved	—	—
140–147h	TIM2_CONF	Timer 2 Configuration and Capabilities	N/A	R/W, RO
148–14Fh	TIM2_COMP	Timer 2 Comparator Value	N/A	R/W

Table 20-1. Memory-Mapped Registers (Sheet 2 of 2)

Offset	Mnemonic	Register	Default	Type
150–15Fh	—	Reserved	—	—
160–167h	TIM3_CONG	Timer 3 Configuration and Capabilities	N/A	R/W, RO
168–16Fh	TIM3_COMP	Timer 3 Comparator Value	N/A	R/W
180–187h	TIM4_CONG	Timer 4 Configuration and Capabilities	N/A	R/W, RO
188–18Fh	TIM4_COMP	Timer 4 Comparator Value	N/A	R/W
190–19Fh	—	Reserved	—	—
1A0–1A7h	TIM5_CONG	Timer 5 Configuration and Capabilities	N/A	R/W, RO
1A8–1AFh	TIM5_COMP	Timer 5 Comparator Value	N/A	R/W
1B0–1BFh	—	Reserved	—	—
1C0–1C7h	TIM6_CONG	Timer 6 Configuration and Capabilities	N/A	R/W, RO
1C8–1CFh	TIM6_COMP	Timer 6 Comparator Value	N/A	R/W
1D0–1DFh	—	Reserved	—	—
1E0–1E7h	TIM7_CONG	Timer 7 Configuration and Capabilities	N/A	R/W, RO
1E8–1EFh	TIM7_COMP	Timer 7 Comparator Value	N/A	R/W
1F0–19Fh	—	Reserved	—	—
200–3FFh	—	Reserved	—	—

Notes:
1. Reads to reserved registers or bits will return a value of 0.
2. Software must not attempt locks to the memory-mapped I/O ranges for High Precision Event Timers. If attempted, the lock is not honored, which means potential deadlock conditions may occur.

20.1.1 GCAP_ID—General Capabilities and Identification Register

Address Offset: 00h Attribute: RO
Default Value: 0429B17F8086A201h Size: 64 bits

Bit	Description
63:32	**Main Counter Tick Period (COUNTER_CLK_PER_CAP)**—RO. This field indicates the period at which the counter increments in femptoseconds (10^-15 seconds). This will return 0429B17F when read. This indicates a period of 69841279 fs (69.841279 ns).
31:16	**Vendor ID Capability (VENDOR_ID_CAP)**—RO. This is a 16-bit value assigned to Intel.
15	**Legacy Replacement Rout Capable (LEG_RT_CAP)**—RO. Hardwired to 1. Legacy Replacement Interrupt Rout option is supported.
14	Reserved. This bit returns 0 when read.
13	**Counter Size Capability (COUNT_SIZE_CAP)**—RO. Hardwired to 1. Counter is 64-bit wide.
12:8	**Number of Timer Capability (NUM_TIM_CAP)**—RO. This field indicates the number of timers in this block. 07h = Eight timers.
7:0	**Revision Identification (REV_ID)—**RO. This indicates which revision of the function is implemented. Default value will be 01h.

20.1.2 GEN_CONF—General Configuration Register

Address Offset: 010h Attribute: R/W
Default Value: 00000000 00000000h Size: 64 bits

Bit	Description
63:2	Reserved. These bits return 0 when read.
1	**Legacy Replacement Rout (LEG_RT_CNF)**—R/W. If the ENABLE_CNF bit and the LEG_RT_CNF bit are both set, then the interrupts will be routed as follows: • Timer 0 is routed to IRQ0 in 8259 or IRQ2 in the I/O APIC • Timer 1 is routed to IRQ8 in 8259 or IRQ8 in the I/O APIC • Timer 2-n is routed as per the routing in the timer n config registers. • If the Legacy Replacement Rout bit is set, the individual routing bits for Timers 0 and 1 (APIC) will have no impact. • If the Legacy Replacement Rout bit is not set, the individual routing bits for each of the timers are used. • This bit will default to 0. BIOS can set it to 1 to enable the legacy replacement routing, or 0 to disable the legacy replacement routing.
0	**Overall Enable (ENABLE_CNF)**—R/W. This bit must be set to enable any of the timers to generate interrupts. If this bit is 0, then the main counter will halt (will not increment) and no interrupts will be caused by any of these timers. For level-triggered interrupts, if an interrupt is pending when the ENABLE_CNF bit is changed from 1 to 0, the interrupt status indications (in the various Txx_INT_STS bits) will not be cleared. Software must write to the Txx_INT_STS bits to clear the interrupts. ***Note:*** This bit will default to 0. BIOS can set it to 1 or 0.

20.1.3 GINTR_STA—General Interrupt Status Register

Address Offset: 020h Attribute: R/W, R/WC
Default Value: 00000000 00000000h Size: 64 bits

Bit	Description
63:8	Reserved. These bits will return 0 when read.
7	**Timer 7Interrupt Active (T07_INT_STS)**—R/WC. Same functionality as Timer 0.
6	**Timer 6Interrupt Active (T06_INT_STS)**—R/WC. Same functionality as Timer 0.
5	**Timer 5Interrupt Active (T05_INT_STS)**—R/WC. Same functionality as Timer 0.
4	**Timer 4Interrupt Active (T04_INT_STS)**—R/WC. Same functionality as Timer 0.
3	**Timer 3Interrupt Active (T03_INT_STS)**—R/WC. Same functionality as Timer 0.
2	**Timer 2 Interrupt Active (T02_INT_STS)**—R/WC. Same functionality as Timer 0.
1	**Timer 1 Interrupt Active (T01_INT_STS)**—R/WC. Same functionality as Timer 0.
0	**Timer 0 Interrupt Active (T00_INT_STS)**—R/WC. The functionality of this bit depends on whether the edge or level-triggered mode is used for this timer. (default = 0) If set to level-triggered mode: This bit will be set by hardware if the corresponding timer interrupt is active. Once the bit is set, it can be cleared by software writing a 1 to the same bit position. Writes of 0 to this bit will have no effect. If set to edge-triggered mode: This bit should be ignored by software. Software should always write 0 to this bit. ***Note:*** Defaults to 0. In edge triggered mode, this bit will always read as 0 and writes will have no effect.

20.1.4 MAIN_CNT—Main Counter Value Register

Address Offset:	0F0h	Attribute:	R/W
Default Value:	N/A	Size:	64 bits

Bit	Description
63:0	**Counter Value (COUNTER_VAL[63:0])**—R/W. Reads return the current value of the counter. Writes load the new value to the counter. ***Notes:*** 1. Writes to this register should only be done while the counter is halted. 2. Reads to this register return the current value of the main counter. 3. 32-bit counters will always return 0 for the upper 32-bits of this register. 4. If 32-bit software attempts to read a 64-bit counter, it should first halt the counter. Since this delays the interrupts for all of the timers, this should be done only if the consequences are understood. It is strongly recommended that 32-bit software only operate the timer in 32-bit mode. 5. Reads to this register are monotonic. No two consecutive reads return the same value. The second of two reads always returns a larger value (unless the timer has rolled over to 0).

20.1.5 TIMn_CONF—Timer n Configuration and Capabilities Register

Address Offset:	Timer 0:	100–107h,	Attribute:	RO, R/W
	Timer 1:	120–127h,		
	Timer 2:	140–147h,		
	Timer 3:	160–167h,		
	Timer 4:	180–187h,		
	Timer 5:	1A0–1A7h,		
	Timer 6:	1C0–1C7h,		
	Timer 7:	1E0–1E7h,		
Default Value:	N/A		Size:	64 bit

Note: The letter n can be 0, 1, 2, 3, 4, 5, 6, or 7 referring to Timer 0, 1, 2, 3, 4, 5, 6, or 7.

Bit	Description
63:56	Reserved. These bits will return 0 when read.
55:52, 43	**Timer Interrupt Rout Capability (TIMERn_INT_ROUT_CAP)**—RO. Timer 0, 1:Bits 52, 53, 54, and 55 in this field (corresponding to IRQ 20, 21, 22, and 23) have a value of 1. Writes will have no effect. Timer 2: Bits 43, 52, 53, 54, and 55 in this field (corresponding to IRQ 11, 20, 21, 22, and 23) have a value of 1. Writes will have no effect. Timer 3: Bits 44, 52, 53, 54, and 55 in this field (corresponding to IRQ 11, 20, 21, 22, and 23) have a value of 1. Writes will have no effect. Timer 4, 5, 6, 7 This field is always 0 as interrupts from these timers can only be delivered using direct processor interrupt messages. ***Note:*** If IRQ 11 is used for HPET #2, software should ensure IRQ 11 is not shared with any other devices to ensure the proper operation of HPET #2. ***Note:*** If IRQ 12 is used for HPET #3, software should ensure IRQ 12 is not shared with any other devices to ensure the proper operation of HPET #3.
51:45, 42:16	Reserved. These bits return 0 when read.
15	Timer n Processor Message Interrupt Delivery (Tn_PROCMSG_INT_DEL_CAP)—RO. This bit is always read as '1', since the PCH HPET implementation supports the direct processor interrupt delivery.

Bit	Description
14	**Timer n Processor Message Interrupt Enable (Tn_PROCMSG_EN_CNF)**—R/W / RO. If the Tn_PROCMSG_INT_DEL_CAP bit is set for this timer, then the software can set the Tn_PROCMSG_EN_CNF bit to force the interrupts to be delivered directly as processor messages, rather than using the 8259 or I/O (x) APIC. In this case, the Tn_INT_ROUT_CNF field in this register will be ignored. The Tn_PROCMSG_ROUT register will be used instead. Timer 0, 1, 2, 3 Specific: This bit is a read/write bit. Timer 4, 5, 6, 7 Specific: This bit is always Read Only '1' as interrupt from these timers can only be delivered using direct processor interrupt messages.
13:9	**Timer n Interrupt Rout (Tn_INT_ROUT_CNF)—**R/W / RO. This 5-bit field indicates the routing for the interrupt to the 8259 or I/O (x) APIC. Software writes to this field to select which interrupt in the 8259 or I/O (x) will be used for this timer's interrupt. If the value is not supported by this particular timer, then the value read back will not match what is written. The software must only write valid values. Timer 4, 5, 6, 7: This field is Read-only and reads will return 0. ***Notes:*** 1. If the interrupt is handled using the 8259, only interrupts 0-15 are applicable and valid. Software must not program any value other than 0-15 in this field. 2. If the Legacy Replacement Rout bit is set, then Timers 0 and 1 will have a different routing, and this bit field has no effect for those two timers. 3. Timer 0,1: Software is responsible to make sure it programs a valid value (20, 21, 22, or 23) for this field. The PCH logic does not check the validity of the value written. 4. Timer 2: Software is responsible to make sure it programs a valid value (11, 20, 21, 22, or 23) for this field. The PCH logic does not check the validity of the value written. 5. Timer 3: Software is responsible to make sure it programs a valid value (12, 20, 21, 22, or 23) for this field. The PCH logic does not check the validity of the value written. 6. Timers 4, 5, 6, 7: This field is always Read Only 0 as interrupts from these timers can only be delivered using direct processor interrupt messages.
8	**Timer n 32-bit Mode (TIMERn_32MODE_CNF)—**R/W or RO. Software can set this bit to force a 64-bit timer to behave as a 32-bit timer. Timer 0:Bit is read/write (default to 0). 0 = 64 bit; 1 = 32 bit Timers 1, 2, 3, 4, 5, 6, 7:Hardwired to 0. Writes have no effect (since these seven timers are 32-bits). ***Note:*** When this bit is set to '1', the hardware counter will do a 32-bit operation on comparator match and rollovers, thus the upper 32-bit of the Timer 0 Comparator Value register is ignored. The upper 32-bit of the main counter is not involved in any rollover from lower 32-bit of the main counter and becomes all zeros.
7	Reserved**.** This bit returns 0 when read.
6	**Timer n Value Set (TIMERn_VAL_SET_CNF)**—R/W. Software uses this bit only for Timer 0 if it has been set to periodic mode. By writing this bit to a 1, the software is then allowed to directly set the timer's accumulator. Software does **not** have to write this bit back to 1 (it automatically clears). Software should not write a 1 to this bit position if the timer is set to non-periodic mode. ***Note:*** This bit will return 0 when read. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1, 2, 3, 4, 5, 6, 7.
5	**Timer n Size (TIMERn_SIZE_CAP)**—RO. This read only field indicates the size of the timer. Timer 0:Value is 1 (64-bits). Timers 1, 2, 3, 4, 5, 6, 7.:Value is 0 (32-bits).
4	**Periodic Interrupt Capable (TIMERn_PER_INT_CAP)**—RO. If this bit is 1, the hardware supports a periodic mode for this timer's interrupt. Timer 0: Hardwired to 1 (supports the periodic interrupt). Timers 1, 2, 3, 4, 5, 6, 7.: Hardwired to 0 (does not support periodic interrupt).
3	**Timer n Type (TIMERn_TYPE_CNF)**—R/W or RO. Timer 0:Bit is read/write. 0 = Disable timer to generate periodic interrupt; 1 = Enable timer to generate a periodic interrupt. Timers 1, 2, 3, 4, 5, 6, 7.: Hardwired to 0. Writes have no affect.

Bit	Description
2	**Timer n Interrupt Enable (TIMERn_INT_ENB_CNF)—**R/W. This bit must be set to enable timer n to cause an interrupt when it times out. 0 = Disable (Default). The timer can still count and generate appropriate status bits, but will not cause an interrupt. 1 = Enable.
1	**Timer Interrupt Type (TIMERn_INT_TYPE_CNF)**—R/W. 0 = The timer interrupt is edge triggered. This means that an edge-type interrupt is generated. If another interrupt occurs, another edge will be generated. 1 = The timer interrupt is level triggered. This means that a level-triggered interrupt is generated. The interrupt will be held active until it is cleared by writing to the bit in the General Interrupt Status Register. If another interrupt occurs before the interrupt is cleared, the interrupt will remain active. Timer 4, 5, 6, 7: This bit is Read-Only, and will return 0 when read
0	Reserved**.** These bits will return 0 when read.

Note: Reads or writes to unimplemented timers should not be attempted. Read from any unimplemented registers will return an undetermined value.

20.1.6 TIMn_COMP—Timer n Comparator Value Register

Address Offset: Timer 0: 108h–10Fh,
Timer 1: 128h–12Fh,
Timer 2: 148h–14Fh,
Timer 3: 168h–16Fh,
Timer 4: 188h – 18Fh,
Timer 5: 1A8h – 1AFh,
Timer 6: 1C8h – 1CFh,
Timer 7: 1E8h – 1EFh

Attribute: R/W
Default Value: N/A Size: 64 bit

Bit	Description

63:0	**Timer Compare Value**—R/W. Reads to this register return the current value of the comparator
	if Timers n are configured to non-periodic mode:
	Writes to this register load the value against which the main counter should be compared for this timer.
	• When the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled).
	• The value in this register does not change based on the interrupt being generated.
	Timer 0 is configured to periodic mode:
	• When the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled).
	• After the main counter equals the value in this register, the value in this register is increased by the value last written to the register.
	For example, if the value written to the register is 00000123h, then
	1. An interrupt will be generated when the main counter reaches 00000123h.
	2. The value in this register will then be adjusted by the hardware to 00000246h.
	3. Another interrupt will be generated when the main counter reaches 00000246h
	4. The value in this register will then be adjusted by the hardware to 00000369h
	• As each periodic interrupt occurs, the value in this register will increment. When the incremented value is greater than the maximum value possible for this register (FFFFFFFFh for a 32-bit timer or FFFFFFFFFFFFFFFFh for a 64-bit timer), the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000h, then after the next interrupt the value will change to 00010000h
	Default value for each timer is all 1s for the bits that are implemented. For example, a 32-bit timer has a default value of 00000000FFFFFFFFh. A 64-bit timer has a default value of FFFFFFFFFFFFFFFFh.

20.1.7 TIMERn_PROCMSG_ROUT—Timer n Processor Message Interrupt Rout Register

Address Offset:	Timer 0:	110–117h,	Attribute:	R/W
	Timer 1:	130–137h,		
	Timer 2:	150–157h,		
	Timer 3:	170–177h,		
	Timer 4:	190–197h,		
	Timer 5:	1B0–1B7h,		
	Timer 6:	1D0–1D7h,		
	Timer 7:	1F0–1F7h,		
Default Value:	N/A		Size:	64 bit

Note: The letter n can be 0, 1, 2, 3, 4, 5, 6, or 7 referring to Timer 0, 1, 2, 3, 4, 5, 6, or 7.

Software can access the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses can be done to offset 1x0h or 1x4h. 64-bit accesses can be done to 1x0h. 32-bit accesses must not be done to offsets 1x1h, 1x2h, 1x3h, 1x5h, 1x6h, or 1x7h.

Bit	Description
63:32	**Tn_PROCMSG_INT_ADDR—R/W**. Software sets this 32-bit field to indicate the location that the direct processor interrupt message should be written.
31:0	**Tn_PROCMSG_INT_VAL—R/W**. Software sets this 32-bit field to indicate that value that is written during the direct processor interrupt message.

§

21 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface resides in memory mapped space. This function contains registers that allow for the setup and programming of devices that reside on the SPI interface.

Note: All registers in this function (including memory-mapped registers) must be addressable in byte, word, and DWord quantities. The software must always make register accesses on natural boundaries (that is, DWord accesses must be on DWord boundaries; word accesses on word boundaries, and so forth) In addition, the memory-mapped register space must not be accessed with the LOCK semantic exclusive-access mechanism. If software attempts exclusive-access mechanisms to the SPI memory-mapped space, the results are undefined.

21.1 Serial Peripheral Interface Memory Mapped Configuration Registers

The SPI Host Interface registers are memory-mapped in the RCRB (Root Complex Register Block) Chipset Register Space with a base address (SPIBAR) of 3800h and are located within the range of 3800h to 39FFh. The address for RCRB can be found in RCBA Register see Section 13.1.40. The individual registers are then accessible at SPIBAR + Offset as indicated in the following table.

These memory mapped registers must be accessed in byte, word, or DWord quantities.

Table 21-1. Serial Peripheral Interface (SPI) Register Address Map (SPI Memory Mapped Configuration Registers) (Sheet 1 of 2)

SPIBAR + Offset	Mnemonic	Register Name	Default
00h–03h	BFPR	BIOS Flash Primary Region	00000000h
04h–05h	HSFS	Hardware Sequencing Flash Status	0000h
06h–07h	HSFC	Hardware Sequencing Flash Control	0000h
08h–0Bh	FADDR	Flash Address	00000000h
10h–13h	FDATA0	Flash Data 0	00000000h
14h–4Fh	FDATAN	Flash Data N	00000000h
50h–53h	FRAP	Flash Region Access Permissions	00000202h
54h–57h	FREG0	Flash Region 0	00000000h
58h–5Bh	FREG1	Flash Region 1	00000000h
5Ch–5F	FREG2	Flash Region 2	00000000h
60h–63h	FREG3	Flash Region 3	00000000h
64h–67h	FREG4	Flash Region 4	00000000h
68h–73h	Reserved	Reserved for Future Flash Regions	00000000h
74h–77h	PR0	Protected Range 0	00000000h
78h–7Bh	PR1	Protected Range 1	00000000h
7Ch–7Fh	PR2	Protected Range 2	00000000h
80–83h	PR3	Protected Range 3	00000000h
84h–87h	PR4	Protected Range 4	00000000h

Table 21-1. Serial Peripheral Interface (SPI) Register Address Map (SPI Memory Mapped Configuration Registers) (Sheet 2 of 2)

SPIBAR + Offset	Mnemonic	Register Name	Default
90h	SSFS	Software Sequencing Flash Status	00h
91h–93h	SSFC	Software Sequencing Flash Control	0000h
94h–95h	PREOP	Prefix Opcode Configuration	0000h
96h–97h	OPTYPE	Opcode Type Configuration	0000h
98h–9Fh	OPMENU	Opcode Menu Configuration	00000000 00000000h
A0h–A3h	BBAR	BIOS Base Address Configuration	00000000h
B0h–B3h	FDOC	Flash Descriptor Observability Control	00000000h
B4h–B7h	FDOD	Flash Descriptor Observability Data	00000000h
C0h–C3h	AFC	Additional Flash Control	00000000h
C4–C7h	LVSCC	Lower Vendor Specific Component Capabilities	00000000h
C8–CBh	UVSCC	Upper Vendor Specific Component Capabilities	00000000h
D0–D3h	FPB	Flash Partition Boundary	00000000h
F0–F3H	SRDL	Soft Reset Data Lock	00000000h
F4–F7H	SRDC	Soft Reset Data Control	00000000h
F8–FBH	SRD	Soft Reset Data	00000000h

21.1.1 BFPR –BIOS Flash Primary Region Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 00h Attribute: RO
Default Value: 00000000h Size: 32 bits

Note: This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:29	Reserved
28:16	**BIOS Flash Primary Region Limit (PRL)—**RO. This specifies address bits 24:12 for the Primary Region Limit. The value in this register loaded from the contents in the Flash Descriptor.FLREG1.Region Limit
15:13	Reserved
12:0	**BIOS Flash Primary Region Base (PRB)**—RO. This specifies address bits 24:12 for the Primary Region Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base

21.1.2 HSFS—Hardware Sequencing Flash Status Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 04h
Default Value: 0000h
Attribute: RO, R/WC, R/W
Size: 16 bits

Bit	Description
15	**Flash Configuration Lock-Down (FLOCKDN)—**R/W/L. When set to 1, those Flash Program Registers that are locked down by this FLOCKDN bit cannot be written. Once set to 1, this bit can only be cleared by a hardware reset due to a global reset or host partition reset in an Intel ME-enabled system.
14	**Flash Descriptor Valid (FDV)—**RO. This bit is set to a 1 if the Flash Controller read the correct Flash Descriptor Signature. If the Flash Descriptor Valid bit is not 1, software cannot use the Hardware Sequencing registers, but must use the software sequencing registers. Any attempt to use the Hardware Sequencing registers will result in the FCERR bit being set.
13	**Flash Descriptor Override Pin-Strap Status (FDOPSS)**—RO: This bit indicates the condition of the Flash Descriptor Security Override / Intel ME Debug Mode Pin-Strap. 0 = The Flash Descriptor Security Override / Intel ME Debug Mode strap is set using external pull-up on HDA_SDO 1 = No override
12:6	Reserved
5	**SPI Cycle In Progress (SCIP)—**RO. Hardware sets this bit when software sets the Flash Cycle Go (FGO) bit in the Hardware Sequencing Flash Control register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0. ***Note:*** This field is only applicable when in Descriptor mode and Hardware sequencing is being used.
4:3	**Block/Sector Erase Size (BERASE)**—RO. This field identifies the erasable sector size for all Flash components. Valid Bit Settings: 00 = 256 Byte 01 = 4 K Byte 10 = 8 K Byte 11 = 64 K Byte If the FLA is less than FPBA then this field reflects the value in the LVSCC.LBES register. If the FLA is greater or equal to FPBA then this field reflects the value in the UVSCC.UBES register. ***Note:*** This field is only applicable when in Descriptor mode and Hardware sequencing is being used.
2	**Access Error Log (AEL)—**R/W/C. Hardware sets this bit to a 1 when an attempt was made to access the BIOS region using the direct access method or an access to the BIOS Program Registers that violated the security restrictions. This bit is simply a log of an access security violation. This bit is cleared by software writing a 1. ***Note:*** This field is only applicable when in Descriptor mode and Hardware sequencing is being used.
1	**Flash Cycle Error (FCERR)**—R/W/C. Hardware sets this bit to 1 when an program register access is blocked to the FLASH due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or until hardware reset occurs due to a global reset or host partition reset in an Intel ME enabled system. Software must clear this bit before setting the FLASH Cycle GO bit in this register. ***Note:*** This field is only applicable when in Descriptor mode and Hardware sequencing is being used.
0	**Flash Cycle Done (FDONE)**—R/W/C. The PCH sets this bit to 1 when the SPI Cycle completes after software previously set the FGO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset due to a global reset or host partition reset in an Intel ME enabled system. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access. ***Note:*** This field is only applicable when in Descriptor mode and Hardware sequencing is being used.

21.1.3 HSFC—Hardware Sequencing Flash Control Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 06h | Attribute: R/W, R/WS
Default Value: 0000h | Size: 16 bits

Note: This register is only applicable when SPI device is in descriptor mode.

Bit	Description
15	**Flash SPI SMI# Enable (FSMIE)**—R/W. When set to 1, the SPI asserts an SMI# request whenever the Flash Cycle Done bit is 1.
14	Reserved
13:8	**Flash Data Byte Count (FDBC)—**R/W. This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The contents of this register are 0s based with 0b representing 1 byte and 111111b representing 64 bytes. The number of bytes transferred is the value of this field plus 1. This field is ignored for the Block Erase command.
7:3	Reserved
2:1	**FLASH Cycle (FCYCLE)**—R/W. This field defines the Flash SPI cycle type generated to the FLASH when the FGO bit is set as defined below: 00 = Read (1 up to 64 bytes by setting FDBC) 01 = Reserved 10 = Write (1 up to 64 bytes by setting FDBC) 11 = Block Erase
0	**Flash Cycle Go (FGO)—**R/W/S. A write to this register with a 1 in this bit initiates a request to the Flash SPI Arbiter to start a cycle. This register is cleared by hardware when the cycle is granted by the SPI arbiter to run the cycle on the SPI bus. When the cycle is complete, the FDONE bit is set. Software is forbidden to write to any register in the HSFLCTL register between the FGO bit getting set and the FDONE bit being cleared. Any attempt to violate this rule will be ignored by hardware. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write. This bit always returns 0 on reads.

21.1.4 FADDR—Flash Address Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 08h | Attribute: R/W
Default Value: 00000000h | Size: 32 bits

Bit	Description
31:25	Reserved
24:0	**Flash Linear Address (FLA)**—R/W. The FLA is the starting byte linear address of a SPI Read or Write cycle or an address within a Block for the Block Erase command. The Flash Linear Address must fall within a region for which BIOS has access permissions. Hardware must convert the FLA into a Flash Physical Address (FPA) before running this cycle on the SPI bus.

21.1.5 FDATA0—Flash Data 0 Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 10h
Attribute: R/W
Default Value: 00000000h
Size: 32 bits

Bit	Description
31:0	**Flash Data 0 (FD0)**—R/W. This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13-…8-23-22-…16-31…24 Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

21.1.6 FDATAN—Flash Data [N] Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 14h
SPIBAR + 18h
SPIBAR + 1Ch
SPIBAR + 20h
SPIBAR + 24h
SPIBAR + 28h
SPIBAR + 2Ch
SPIBAR + 30h
SPIBAR + 34h
SPIBAR + 38h
SPIBAR + 3Ch
SPIBAR + 40h
SPIBAR + 44h
SPIBAR + 48h
SPIBAR + 4Ch
Attribute: R/W
Default Value: 00000000h
Size: 32 bits

Bit	Description
31:0	**Flash Data N (FD[N])**—R/W. Similar definition as Flash Data 0. However, this register does not begin shifting until FD[N-1] has completely shifted in/out.—R/W.

21.1.7 FRAP—Flash Regions Access Permissions Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 50h Attribute: RO, R/W
Default Value: 00000202h Size: 32 bits

Note: This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:24	**BIOS Master Write Access Grant (BMWAG)**—R/W. Each bit [31:29] corresponds to Master[7:0]. BIOS can grant one or more masters write access to the BIOS region 1 overriding the permissions in the Flash Descriptor. Master[1] is Host processor/BIOS, Master[2] is Intel ME, Master[3] is Host processor/GbE. Master[0] and Master[7:4] are reserved. The contents of this register are locked by the FLOCKDN bit.
23:16	**BIOS Master Read Access Grant (BMRAG)**—R/W. Each bit [28:16] corresponds to Master[7:0]. BIOS can grant one or more masters read access to the BIOS region 1 overriding the read permissions in the Flash Descriptor. Master[1] is Host processor/BIOS, Master[2] is Intel ME, Master[3] is Host processor/GbE. Master[0] and Master[7:4] are reserved. The contents of this register are locked by the FLOCKDN bit
15:8	**BIOS Region Write Access (BRWA)**—RO. Each bit [15:8] corresponds to Regions [7:0]. If the bit is set, this master can erase and write that particular region through register accesses. The contents of this register are that of the Flash Descriptor. Flash Master 1 Master Region Write Access OR a particular master has granted BIOS write permissions in their Master Write Access Grant register or the Flash Descriptor Security Override strap is set.
7:0	**BIOS Region Read Access (BRRA)**—RO. Each bit [7:0] corresponds to Regions [7:0]. If the bit is set, this master can read that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Write Access OR a particular master has granted BIOS read permissions in their Master Read Access Grant register or the Flash Descriptor Security Override strap is set.

21.1.8 FREG0—Flash Region 0 (Flash Descriptor) Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 54h Attribute: RO
Default Value: 00000000h Size: 32 bits

Note: This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:29	Reserved
28:16	**Region Limit (RL)—**RO. This specifies address bits 24:12 for the Region 0 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Limit
15:13	Reserved
12:0	**Region Base (RB) / Flash Descriptor Base Address Region (FDBAR)**—RO. This specifies address bits 24:12 for the Region 0 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Base.

21.1.9 FREG1—Flash Region 1 (BIOS Descriptor) Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 58h Attribute: RO
Default Value: 00000000h Size: 32 bits

Note: This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:29	Reserved
28:16	**Region Limit (RL)**—RO. This specifies address bits 24:12 for the Region 1 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit.
15:13	Reserved
12:0	**Region Base (RB)**—RO. This specifies address bits 24:12 for the Region 1 Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base.

21.1.10 FREG2—Flash Region 2 (Intel® ME) Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 5Ch Attribute: RO
Default Value: 00000000h Size: 32 bits

Note: This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:29	Reserved
28:16	**Region Limit (RL)**—RO. This specifies address bits 24:12 for the Region 2 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Limit.
15:13	Reserved
12:0	**Region Base (RB)**—RO. This specifies address bits 24:12 for the Region 2 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Base.

21.1.11 FREG3—Flash Region 3 (GbE) Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 60h Attribute: RO
Default Value: 00000000h Size: 32 bits

Note: This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:29	Reserved
28:16	**Region Limit (RL)**—RO. This specifies address bits 24:12 for the Region 3 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Limit.
15:13	Reserved
12:0	**Region Base (RB)**—RO. This specifies address bits 24:12 for the Region 3 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Base.

21.1.12 FREG4—Flash Region 4 (Platform Data) Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 64h	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Note: This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:29	Reserved
28:16	**Region Limit (RL)—**RO. This specifies address bits 24:12 for the Region 4 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Limit.
15:13	Reserved
12:0	**Region Base (RB)**—RO. This specifies address bits 24:12 for the Region 4 Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Base.

21.1.13 PR0—Protected Range 0 Register (SPI Memory Mapped Configuration Registers)

Memory Address:	SPIBAR + 74h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Note: This register can not be written when the FLOCKDN bit is set to 1.

Bit	Description
31	**Write Protection Enable—**R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	Reserved
28:16	**Protected Range Limit—**R/W. This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	**Read Protection Enable—**R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	Reserved
12:0	**Protected Range Base—**R/W. This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

21.1.14 PR1—Protected Range 1 Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 78h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Note: This register can not be written when the FLOCKDN bit is set to 1.

Bit	Description
31	**Write Protection Enable—**R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	Reserved
28:16	**Protected Range Limit—**R/W. This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	**Read Protection Enable—**R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	Reserved
12:0	**Protected Range Base—**R/W. This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

21.1.15 PR2—Protected Range 2 Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 7Ch Attribute: R/W
Default Value: 00000000h Size: 32 bits

Note: This register can not be written when the FLOCKDN bit is set to 1.

Bit	Description
31	**Write Protection Enable—**R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	Reserved
28:16	**Protected Range Limit—**R/W. This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	**Read Protection Enable—**R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	Reserved
12:0	**Protected Range Base—**R/W. This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

21.1.16 PR3—Protected Range 3 Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 80h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Note: This register can not be written when the FLOCKDN bit is set to 1.

Bit	Description
31	**Write Protection Enable**—R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	Reserved
28:16	**Protected Range Limit**—R/W. This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	**Read Protection Enable**—R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	Reserved
12:0	**Protected Range Base**—R/W. This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

21.1.17 PR4—Protected Range 4 Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 84h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Note: This register can not be written when the FLOCKDN bit is set to 1.

Bit	Description
31	**Write Protection Enable**—R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	Reserved
28:16	**Protected Range Limit**—R/W. This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	**Read Protection Enable**—R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	Reserved
12:0	**Protected Range Base**—R/W. This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

21.1.18 SSFS—Software Sequencing Flash Status Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 90h | Attribute: RO, R/WC
Default Value: 00h | Size: 8 bits

Note: The Software Sequencing control and status registers are reserved if the hardware sequencing control and status registers are used.

Bit	Description
7:5	Reserved
4	**Access Error Log (AEL)**—RO. This bit reflects the value of the Hardware Sequencing Status AEL register.
3	**Flash Cycle Error (FCERR)—**R/WC. Hardware sets this bit to 1 when a programmed access is blocked from running on the SPI interface due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or hardware reset due to a global reset or host partition reset in an Intel® ME enabled system.
2	**Cycle Done Status—**R/WC. The PCH sets this bit to 1 when the SPI Cycle completes (that is, SCIP bit is 0) after software sets the GO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset due to a global reset or host partition reset in an Intel® ME enabled system. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.
1	Reserved
0	**SPI Cycle In Progress (SCIP)**—RO. Hardware sets this bit when software sets the SPI Cycle Go bit in the Command register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.

21.1.19 SSFC—Software Sequencing Flash Control Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 91h Attribute: R/W
Default Value: F80000h Size: 24 bits

Bit	Description
23:19	Reserved – BIOS must set this field to '11111'b
18:16	**SPI Cycle Frequency (SCF)**—R/W. This register sets frequency to use for all SPI software sequencing cycles (write, erase, fast read, read status, etc.) except for the read cycle which always run at 20 MHz. 000 = 20 MHz 001 = 33 MHz 100 = 50 MHz All other values reserved. This register is locked when the SPI Configuration Lock-Down bit is set.
15	**SPI SMI# Enable (SME)**—R/W. When set to 1, the SPI asserts an SMI# request whenever the Cycle Done Status bit is 1.
14	**Data Cycle (DS)**—R/W. When set to 1, there is data that corresponds to this transaction. When 0, no data is delivered for this cycle, and the DBC and data fields themselves are don't cares.
13:8	**Data Byte Count (DBC)—**R/W. This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The valid settings (in decimal) are any value from 0 to 63. The number of bytes transferred is the value of this field plus 1. Note that when this field is 00_0000b, then there is 1 byte to transfer and that 11_1111b means there are 64 bytes to transfer.
7	Reserved
6:4	**Cycle Opcode Pointer (COP)**—R/W. This field selects one of the programmed opcodes in the Opcode Menu to be used as the SPI Command/Opcode. In the case of an Atomic Cycle Sequence, this determines the second command.—R/W.
3	**Sequence Prefix Opcode Pointer (SPOP)—**R/W. This field selects one of the two programmed prefix opcodes for use when performing an Atomic Cycle Sequence. A value of 0 points to the opcode in the least significant byte of the Prefix Opcodes register. By making this programmable, the PCH supports flash devices that have different opcodes for enabling writes to the data space vs. status register.
2	**Atomic Cycle Sequence (ACS)—**R/W. When set to 1 along with the SCGO assertion, the PCH will execute a sequence of commands on the SPI interface without allowing the LAN component to arbitrate and interleave cycles. The sequence is composed of: • Atomic Sequence Prefix Command (8-bit opcode only) • Primary Command specified below by software (can include address and data) • Polling the Flash Status Register (opcode 05h) until bit 0 becomes 0b. The SPI Cycle in Progress bit remains set and the Cycle Done Status bit remains unset until the Busy bit in the Flash Status Register returns 0.
1	**SPI Cycle Go (SCGO)—**R/WS. This bit always returns 0 on reads. However, a write to this register with a 1 in this bit starts the SPI cycle defined by the other bits of this register. The "SPI Cycle in Progress" (SCIP) bit gets set by this action. Hardware must ignore writes to this bit while the Cycle In Progress bit is set. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write.
0	Reserved

21.1.20 PREOP—Prefix Opcode Configuration Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 94h Attribute: R/W
Default Value: 0000h Size: 16 bits

Bit	Description
15:8	**Prefix Opcode 1**—R/W. Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.
7:0	**Prefix Opcode 0**—R/W. Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.

Note: This register is not writable when the Flash Configuration Lock-Down bit (SPIBAR + 04h:15) is set.

21.1.21 OPTYPE—Opcode Type Configuration Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 96h Attribute: R/W
Default Value: 0000h Size: 16 bits

Entries in this register correspond to the entries in the Opcode Menu Configuration register.

Note: The definition below only provides write protection for opcodes that have addresses associated with them. Therefore, any erase or write opcodes that do not use an address should be avoided (for example, "Chip Erase" and "Auto-Address Increment Byte Program")

Bit	Description
15:14	**Opcode Type 7**—R/W. See the description for bits 1:0
13:12	**Opcode Type 6**—R/W. See the description for bits 1:0
11:10	**Opcode Type 5**—R/W. See the description for bits 1:0
9:8	**Opcode Type 4**—R/W. See the description for bits 1:0
7:6	**Opcode Type 3**—R/W. See the description for bits 1:0
5:4	**Opcode Type 2**—R/W. See the description for bits 1:0
3:2	**Opcode Type 1**—R/W. See the description for bits 1:0
1:0	**Opcode Type 0**—R/W. This field specifies information about the corresponding Opcode 0. This information allows the hardware to 1) know whether to use the address field and 2) provide BIOS and Shared Flash protection capabilities. The encoding of the two bits is: 00 = No address associated with this Opcode; Read cycle type 01 = No address associated with this Opcode; Write cycle type 10 = Address required; Read cycle type 11 = Address required; Write cycle type

Note: This register is not writable when the SPI Configuration Lock-Down bit (SPIBAR + 00h:15) is set.

21.1.22 OPMENU—Opcode Menu Configuration Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 98h Attribute: R/W
Default Value: 0000000000000000h Size: 64 bits

Eight entries are available in this register to give BIOS a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices.

Note: It is recommended that BIOS avoid programming Write Enable opcodes in this menu. Malicious software could then perform writes and erases to the SPI flash without using the atomic cycle mechanism. This could cause functional failures in a shared flash environment. Write Enable opcodes should only be programmed in the Prefix Opcodes.

Bit	Description
63:56	**Allowable Opcode 7**—R/W. See the description for bits 7:0
55:48	**Allowable Opcode 6**—R/W. See the description for bits 7:0
47:40	**Allowable Opcode 5**—R/W. See the description for bits 7:0
39:32	**Allowable Opcode 4**—R/W. See the description for bits 7:0
31:24	**Allowable Opcode 3**—R/W. See the description for bits 7:0
23:16	**Allowable Opcode 2**—R/W. See the description for bits 7:0
15:8	**Allowable Opcode 1**—R/W. See the description for bits 7:0
7:0	**Allowable Opcode 0**—R/W. Software programs an SPI opcode into this field for use when initiating SPI commands through the Control Register.

This register is not writable when the SPI Configuration Lock-Down bit (SPIBAR + 00h:15) is set.

21.1.23 BBAR—BIOS Base Address Configuration Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + A0h Attribute: R/W, RO
Default Value: 00000000h Size: 32 bits

Eight entries are available in this register to give BIOS a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices.

Bit	Description
31:24	Reserved
23:8	**Bottom of System Flash**—R/W. This field determines the bottom of the System BIOS. The PCH will not run programmed commands nor memory reads whose address field is less than this value. this field corresponds to bits 23:8 of the 3-byte address; bits 7:0 are assumed to be 00h for this vector when comparing to a potential SPI address. ***Note:*** The SPI host controller prevents any programmed cycle using the address register with an address less than the value in this register. Some flash devices specify that the Read ID command must have an address of 0000h or 0001h. If this command must be supported with these devices, it must be performed with the BIOS BAR
7:0	Reserved

21.1.24 FDOC—Flash Descriptor Observability Control Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + B0h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Note: This register that can be used to observe the contents of the Flash Descriptor that is stored in the PCH Flash Controller. This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:15	Reserved
14:12	**Flash Descriptor Section Select (FDSS)**—R/W. Selects which section within the loaded Flash Descriptor to observe. 000 = Flash Signature and Descriptor Map 001 = Component 010 = Region 011 = Master 111 = Reserved
11:2	**Flash Descriptor Section Index (FDSI)—**R/W. Selects the DW offset within the Flash Descriptor Section to observe.
1:0	Reserved

21.1.25 FDOD—Flash Descriptor Observability Data Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + B4h Attribute: RO
Default Value: 00000000h Size: 32 bits

Note: This register that can be used to observe the contents of the Flash Descriptor that is stored in the PCH Flash Controller.

Bit	Description
31:0	**Flash Descriptor Section Data (FDSD)—**RO. Returns the DW of data to observe as selected in the Flash Descriptor Observability Control.

21.1.26 AFC—Additional Flash Control Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + C0h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits.

Bit	Description
31:3	Reserved
2:1	**Flash Controller Interface Dynamic Clock Gating Enable—**R/W. 0 = Flash Controller Interface Dynamic Clock Gating is Disabled 1 = Flash Controller Interface Dynamic Clock Gating is Enabled Other configurations are Reserved.
0	**Flash Controller Core Dynamic Clock Gating Enable—**R/W. 0 = Flash Controller Core Dynamic Clock Gating is Disabled 1 = Flash Controller Core Dynamic Clock Gating is Enabled

21.1.27 LVSCC—Host Lower Vendor Specific Component Capabilities Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + C4h Attribute: RO, R/WL
Default Value: 00000000h Size: 32 bits

Note: All attributes described in LVSCC must apply to all flash space below the FPBA, even if it spans between two separate flash parts. This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:24	Reserved
23	**Vendor Component Lock (LVCL)—**R/W. This register locks itself when set. 0 = The lock bit is not set 1 = The Vendor Component Lock bit is set. ***Note:*** This bit applies to both UVSCC and LVSCC registers.
22:16	Reserved
15:8	**Lower Erase Opcode (LEO)**—R/W. This register is programmed with the Flash erase instruction opcode required by the vendor's Flash component. This register is locked by the Vendor Component Lock (LVCL) bit.
7:5	Reserved
4	**Write Enable on Write Status (LWEWS)**—R/W. This register is locked by the Vendor Component Lock (LVCL) bit. 0 = No automatic write of 00h will be made to the SPI flash's status register) 1 = A write of 00h to the SPI flash's status register will be sent on EVERY write and erase to the SPI flash. 06h 01h 00h is the opcode sequence used to unlock the Status register. ***Notes:*** 1. This bit should not be set to '1' if there are non volatile bits in the SPI flash's status register. This may lead to premature flash wear out 2. This is not an atomic sequence. If the SPI component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. 3. Bit 3 and bit 4 should NOT be both set to '1'.
3	**Lower Write Status Required (LWSR)**—R/W. This register is locked by the Vendor Component Lock (LVCL) bit. 0 = No automatic write of 00h will be made to the SPI flash's status register) 1 = A write of 00h to the SPI flash's status register will be sent on EVERY write and erase to the SPI flash. 50h 01h 00h is the opcode sequence used to unlock the Status register. ***Notes:*** 1. This bit should not be set to '1' if there are non volatile bits in the SPI flash's status register. This may lead to premature flash wear out. 2. This is not an atomic sequence. If the SPI component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. 3. Bit 3 and bit 4 should NOT be both set to '1'.
2	**Lower Write Granularity (LWG)—**R/W**.** This register is locked by the Vendor Component Lock (LVCL) bit. 0 = 1 Byte 1 = 64 Byte ***Notes:*** 1. If more than one Flash component exists, this field must be set to the lowest common write granularity of the different Flash components. 2. If using 64 B write, BIOS must ensure that multiple byte writes do not occur over 256 B boundaries. This will lead to corruption as the write will wrap around the page boundary on the SPI flash part. This is a a feature page writable SPI flash.
1:0	**Lower Block/Sector Erase Size (LBES)—**R/W. This field identifies the erasable sector size for all Flash components. 00 = 256 Byte 01 = 4 KB 10 = 8 KB 11 = 64 KB This register is locked by the Vendor Component Lock (LVCL) bit. Hardware takes no action based on the value of this register. The contents of this register are to be used only by software and can be read in the HSFSTS.BERASE register in both the BIOS and the GbE program registers if FLA is less than FPBA.

21.1.28 UVSCC—Host Upper Vendor Specific Component Capabilities Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + C8h Attribute: RO, R/WL
Default Value: 00000000h Size: 32 bits

Note: All attributes described in UVSCC must apply to all flash space equal to or above the FPBA, even if it spans between two separate flash parts. This register is only applicable when SPI device is in descriptor mode.

Note: To prevent this register from being modified you must use LVSCC.VCL bit.

Bit	Description
31:16	Reserved
15:8	**Upper Erase Opcode (UEO)**—R/W. This register is programmed with the Flash erase instruction opcode required by the vendor's Flash component. This register is locked by the Vendor Component Lock (UVCL) bit.
7:5	Reserved
4	**Write Enable on Write Status (UWEWS)**—R/W. This register is locked by the Vendor Component Lock (UVCL) bit. 0 = No automatic write of 00h will be made to the SPI flash's status register) 1 = A write of 00h to the SPI flash's status register will be sent on EVERY write and erase to the SPI flash. 06h 01h 00h is the opcode sequence used to unlock the Status register. ***Notes:*** 1. This bit should not be set to '1' if there are non volatile bits in the SPI flash's status register. This may lead to premature flash wear out 2. This is not an atomic sequence. If the SPI component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. 3. Bit 3 and bit 4 should NOT be both set to '1'.
3	**Upper Write Status Required (UWSR)**—R/W. This register is locked by the Vendor Component Lock (UVCL) bit. 0 = No automatic write of 00h will be made to the SPI flash's status register) 1 = A write of 00h to the SPI flash's status register will be sent on EVERY write and erase to the SPI flash. 50h 01h 00h is the opcode sequence used to unlock the Status register. ***Notes:*** 1. This bit should not be set to '1' if there are non volatile bits in the SPI flash's status register. This may lead to premature flash wear out 2. This is not an atomic sequence. If the SPI component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. 3. Bit 3 and bit 4 should NOT be both set to '1'.
2	**Upper Write Granularity (UWG)—**R/W. This register is locked by the Vendor Component Lock (UVCL) bit. 0 = 1 Byte 1 = 64 Byte ***Notes:*** 1. If more than one Flash component exists, this field must be set to the lowest common write granularity of the different Flash components. 2. If using 64 B write, BIOS must ensure that multiple byte writes do not occur over 256 B boundaries. This will lead to corruption as the write will wrap around the page boundary on the SPI flash part. This is a a feature page writable SPI flash.
1:0	**Upper Block/Sector Erase Size (UBES)—**R/W. This field identifies the erasable sector size for all Flash components. Valid Bit Settings: 00 = 256 Byte 01 = 4 KB 10 = 8 KB 11 = 64 KB This register is locked by the Vendor Component Lock (UVCL) bit. Hardware takes no action based on the value of this register. The contents of this register are to be used only by software and can be read in the HSFSTS.BERASE register in both the BIOS and the GbE program registers if FLA is greater or equal to FPBA.

21.1.29 FPB—Flash Partition Boundary (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + D0h Attribute: RO
Default Value: 00000000h Size: 32 bits

Note: This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:13	Reserved
12:0	**Flash Partition Boundary Address (FPBA)—**RO. This register reflects the value of Flash Descriptor Component FPBA field.

21.1.30 SRDL—Soft Reset Data Lock (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + F0h Attribute: R/WL
Default Value: 00000000h Size: 32 bits

Bit	Description
31:1	Reserved
0	**Set_Strap Lock (SSL)**—R/WL. 0 = The SRDL (this register), SRDC (SPIBAR+F4h), and SRD (SPIBAR+F4h) registers are writable. 1 = The SRDL (this register), SRDC (SPIBAR+F4h), and SRD (SPIBAR+F4h) registers are locked. ***Note:*** That this bit is reset to '0' on CF9h resets.

21.1.31 SRDC—Soft Reset Data Control (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + F4h Attribute: R/WL
Default Value: 00000000h Size: 32 bits

Bit	Description
31:1	Reserved
0	**Soft Reset Data Select (SRDS)**—R/WL. 0 = The Set_Strap data sends the default processor configuration data. 1 = The Set_Strap message bits come from the Set_Strap Msg Data register. ***Notes:*** 1. This bit is reset by the RSMRST# or when the Resume well loses power. 2. This bit is locked by the SSL bit (SPIBAR+F0h:bit 0).

21.1.32 SRD—Soft Reset Data (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + F8h Attribute: R/WL
Default Value: 00000000h Size: 32 bits

Bit	Description
31:14	Reserved
13:0	**Set_Stap Data (SSD)**—R/WL. ***Notes:*** 1. These bits are reset by the RSMRST#, or when the Resume well loses power. 2. These bits are locked by the SSL bit (SPIBAR+F0h:bit 0).

21.2 Flash Descriptor Records

The following sections describe the data structure of the Flash Descriptor on the SPI device. These are not registers within the PCH.

21.3 OEM Section

Memory Address: F00h Default Value: Size:256 Bytes

256 Bytes are reserved at the top of the Flash Descriptor for use by the OEM. The information stored by the OEM can only be written during the manufacturing process as the Flash Descriptor read/write permissions must be set to Read Only when the computer leaves the manufacturing floor. The PCH Flash controller does not read this information. FFh is suggested to reduce programming time.

21.4 GbE SPI Flash Program Registers

The GbE Flash registers are memory-mapped with a base address MBARB found in the GbE LAN register chapter Device 25: Function 0: Offset 14h. The individual registers are then accessible at MBARB + Offset as indicated in the following table.

These memory mapped registers must be accessed in byte, word, or DWord quantities.

Note: These registers are only applicable when SPI flash is used in descriptor mode.

Table 21-2. Gigabit LAN SPI Flash Program Register Address Map (GbE LAN Memory Mapped Configuration Registers) (Sheet 1 of 2)

MBARB + Offset	Mnemonic	Register Name	Default	Access
00h–03h	GLFPR	Gigabit LAN Flash Primary Region	00000000h	
04h–05h	HSFS	Hardware Sequencing Flash Status	0000h	
06h–07h	HSFC	Hardware Sequencing Flash Control	0000h	
08h–0Bh	FADDR	Flash Address	00000000h	
0Ch–0Fh	Reserved	Reserved	00000000h	
10h–13h	FDATA0	Flash Data 0	00000000h	
14h–4Fh	Reserved	Reserved	00000000h	
50h–53h	FRAP	Flash Region Access Permissions	00000000h	
54h–57h	FREG0	Flash Region 0	00000000h	
58h–5Bh	FREG1	Flash Region 1	00000000h	
5Ch–5Fh	FREG2	Flash Region 2	00000000h	
60h–63h	FREG3	Flash Region 3	00000000h	
64h–73h	Reserved	Reserved for Future Flash Regions		
74h–77h	PR0	Protected Range 0	00000000h	
78h–7Bh	PR1	Protected Range 1	00000000h	
7Ch–8Fh	Reserved	Reserved		
90h	SSFS	Software Sequencing Flash Status	00h	
91h–93h	SSFC	Software Sequencing Flash Control	000000h	
94h–95h	PREOP	Prefix Opcode Configuration	0000h	
96h–97h	OPTYPE	Opcode Type Configuration	0000h	

Table 21-2. Gigabit LAN SPI Flash Program Register Address Map (GbE LAN Memory Mapped Configuration Registers) (Sheet 2 of 2)

MBARB + Offset	Mnemonic	Register Name	Default	Access
98h–9Fh	OPMENU	Opcode Menu Configuration	00000000 00000000h	
A0h–DFh	Reserved	Reserved		

21.4.1 GLFPR –Gigabit LAN Flash Primary Region Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 00h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:29	Reserved
28:16	**GbE Flash Primary Region Limit (PRL)—**RO. This specifies address bits 24:12 for the Primary Region Limit. The value in this register loaded from the contents in the Flash Descriptor.FLREG3.Region Limit
15:13	Reserved
12:0	**GbE Flash Primary Region Base (PRB)**—RO. This specifies address bits 24:12 for the Primary Region Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Base

21.4.2 HSFS—Hardware Sequencing Flash Status Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 04h
Default Value: 0000h
Attribute: RO, R/WC, R/W
Size: 16 bits

Bit	Description
15	**Flash Configuration Lock-Down (FLOCKDN)**—R/W. When set to 1, those Flash Program Registers that are locked down by this FLOCKDN bit cannot be written. Once set to 1, this bit can only be cleared by a hardware reset due to a global reset or host partition reset in an Intel® ME enabled system.
14	**Flash Descriptor Valid (FDV)—**RO. This bit is set to a 1 if the Flash Controller read the correct Flash Descriptor Signature. If the Flash Descriptor Valid bit is not '1', software cannot use the Hardware Sequencing registers, but must use the software sequencing registers. Any attempt to use the Hardware Sequencing registers will result in the FCERR bit being set.
13	**Flash Descriptor Override Pin Strap Status (FDOPSS)—**RO. his bit indicates the condition of the Flash Descriptor Security Override / Intel ME Debug Mode Pin-Strap. 0 = The Flash Descriptor Security Override / Intel ME Debug Mode strap is set using external pull-up on HDA_SDO 1 = No override
12:6	Reserved
5	**SPI Cycle In Progress (SCIP)—**RO. Hardware sets this bit when software sets the Flash Cycle Go (FGO) bit in the Hardware Sequencing Flash Control register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.
4:3	**Block/Sector Erase Size (BERASE)**—RO. This field identifies the erasable sector size for all Flash components. 00 = 256 Byte 01 = 4 K Byte 10 = 8 K Byte 11 = 64 K Byte If the Flash Linear Address is less than FPBA then this field reflects the value in the LVSCC.LBES register. If the Flash Linear Address is greater or equal to FPBA then this field reflects the value in the UVSCC.UBES register.
2	**Access Error Log (AEL)**—R/W/C. Hardware sets this bit to a 1 when an attempt was made to access the BIOS region using the direct access method or an access to the BIOS Program Registers that violated the security restrictions. This bit is simply a log of an access security violation. This bit is cleared by software writing a '1.'
1	**Flash Cycle Error (FCERR)**—R/W/C. Hardware sets this bit to 1 when an program register access is blocked to the FLASH due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or until hardware reset occurs due to a global reset or host partition reset in an Intel® ME enabled system. Software must clear this bit before setting the FLASH Cycle GO bit in this register.
0	**Flash Cycle Done (FDONE)**—R/W/C. The PCH sets this bit to 1 when the SPI Cycle completes after software previously set the FGO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset due to a global reset or host partition reset in an Intel® ME enabled system. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.

21.4.3 HSFC—Hardware Sequencing Flash Control Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 06h Attribute: R/W, R/WS
Default Value: 0000h Size: 16 bits

Bit	Description
15:10	Reserved
9:8	**Flash Data Byte Count (FDBC)—**R/W. This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The content's of this register are 0s based with 0b representing 1 byte and 11b representing 4 bytes. The number of bytes transferred is the value of this field plus 1. This field is ignored for the Block Erase command.
7:3	Reserved
2:1	**FLASH Cycle (FCYCLE)**—R/W. This field defines the Flash SPI cycle type generated to the FLASH when the FGO bit is set as defined below: 00 = Read (1 up to 4 bytes by setting FDBC) 01 = Reserved 10 = Write (1 up to 4 bytes by setting FDBC) 11 = Block Erase
0	**Flash Cycle Go (FGO)—**R/W/S. A write to this register with a '1' in this bit initiates a request to the Flash SPI Arbiter to start a cycle. This register is cleared by hardware when the cycle is granted by the SPI arbiter to run the cycle on the SPI bus. When the cycle is complete, the FDONE bit is set. Software is forbidden to write to any register in the HSFLCTL register between the FGO bit getting set and the FDONE bit being cleared. Any attempt to violate this rule will be ignored by hardware. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write. This bit always returns 0 on reads.

21.4.4 FADDR—Flash Address Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 08h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:25	Reserved
24:0	**Flash Linear Address (FLA)**—R/W. The FLA is the starting byte linear address of a SPI Read or Write cycle or an address within a Block for the Block Erase command. The Flash Linear Address must fall within a region for which BIOS has access permissions.

21.4.5 FDATA0—Flash Data 0 Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 10h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	**Flash Data 0 (FD0)**—R/W. This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13-…8-23-22-…16-31…24 Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

21.4.6 FRAP—Flash Regions Access Permissions Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 50h Attribute: RO, R/W
Default Value: 00000808h Size: 32 bits

Bit	Description
31:28	Reserved
27:25	**GbE Master Write Access Grant (GMWAG)**—R/W. Each bit 27:25 corresponds to Master[3:1]. GbE can grant one or more masters write access to the GbE region 3 overriding the permissions in the Flash Descriptor. Master[1] is Host Processor/BIOS, Master[2] is Intel ME, Master[3] is Host processor/GbE. The contents of this register are locked by the FLOCKDN bit.
24:20	Reserved
19:17	**GbE Master Read Access Grant (GMRAG)**—R/W. Each bit 19:17 corresponds to Master[3:1]. GbE can grant one or more masters read access to the GbE region 3 overriding the read permissions in the Flash Descriptor. Master[1] is Host processor/BIOS, Master[2] is Intel ME, Master[3] is GbE. The contents of this register are locked by the FLOCKDN bit
16:12	Reserved
11:8	**GbE Region Write Access (GRWA)**—RO. Each bit 11:8 corresponds to Regions 3:0. If the bit is set, this master can erase and write that particular region through register accesses. The contents of this register are that of the Flash Descriptor. Flash Master 3.Master Region Write Access OR a particular master has granted GbE write permissions in their Master Write Access Grant register OR the Flash Descriptor Security Override strap is set.
7:4	Reserved
3:0	**GbE Region Read Access (GRRA)**—RO. Each bit 3:0 corresponds to Regions 3:0. If the bit is set, this master can read that particular region through register accesses. The contents of this register are that of the Flash Descriptor. Flash Master 3.Master Region Write Access OR a particular master has granted GbE read permissions in their Master Read Access Grant register.

21.4.7 FREG0—Flash Region 0 (Flash Descriptor) Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 54h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:29	Reserved
28:16	**Region Limit (RL)—**RO. This specifies address bits 24:12 for the Region 0 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Limit.
15:13	Reserved
12:0	**Region Base (RB)**—RO. This specifies address bits 24:12 for the Region 0 Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Base.

21.4.8 FREG1—Flash Region 1 (BIOS Descriptor) Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 58h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:29	Reserved
28:16	**Region Limit (RL)—**RO. This specifies address bits 24:12 for the Region 1 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit.
15:13	Reserved
12:0	**Region Base (RB)**—RO. This specifies address bits 24:12 for the Region 1 Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base.

21.4.9 FREG2—Flash Region 2 (Intel® ME) Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 5Ch Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:29	Reserved
28:16	**Region Limit (RL)—**RO. This specifies address bits 24:12 for the Region 2 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Limit.
15:13	Reserved
12:0	**Region Base (RB)**—RO. This specifies address bits 24:12 for the Region 2 Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Base.

21.4.10 FREG3—Flash Region 3 (GbE) Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 60h Attribute: RO
Default Value: 00000000h Size: 32 bits

Bit	Description
31:29	Reserved
28:16	**Region Limit (RL)**—RO. This specifies address bits 24:12 for the Region 3 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Limit.
15:13	Reserved
12:0	**Region Base (RB)**—RO. This specifies address bits 24:12 for the Region 3 Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Base.

21.4.11 PR0—Protected Range 0 Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 74h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Note: This register can not be written when the FLOCKDN bit is set to 1.

Bit	Description
31	**Write Protection Enable—**R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	Reserved
28:16	**Protected Range Limit—**R/W. This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	**Read Protection Enable—**R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	Reserved
12:0	**Protected Range Base—**R/W. This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

21.4.12 PR1—Protected Range 1 Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 78h Attribute: R/W
Default Value: 00000000h Size: 32 bits

Note: This register can not be written when the FLOCKDN bit is set to 1.

Bit	Description
31	**Write Protection Enable—**R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	Reserved
28:16	**Protected Range Limit—**R/W. This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	**Read Protection Enable—**R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	Reserved
12:0	**Protected Range Base—**R/W. This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

21.4.13 SSFS—Software Sequencing Flash Status Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 90h Attribute: RO, R/WC
Default Value: 00h Size: 8 bits

Note: The Software Sequencing control and status registers are reserved if the hardware sequencing control and status registers are used.

Bit	Description
7:5	Reserved
4	**Access Error Log (AEL)**—RO. This bit reflects the value of the Hardware Sequencing Status AEL register.
3	**Flash Cycle Error (FCERR)—**R/WC. Hardware sets this bit to 1 when a programmed access is blocked from running on the SPI interface due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or hardware reset due to a global reset or host partition reset in an Intel ME enabled system.
2	**Cycle Done Status—**R/WC. The PCH sets this bit to 1 when the SPI Cycle completes (that is, SCIP bit is 0) after software sets the GO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset due to a global reset or host partition reset in an Intel® ME enabled system. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.
1	Reserved
0	**SPI Cycle In Progress (SCIP)**—RO. Hardware sets this bit when software sets the SPI Cycle Go bit in the Command register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.

21.4.14 SSFC—Software Sequencing Flash Control Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address:	MBARB + 91h	Attribute:	R/W
Default Value:	000000h	Size:	24 bits

Bit	Description
23:19	Reserved
18:16	**SPI Cycle Frequency (SCF)**—R/W. This register sets frequency to use for all SPI software sequencing cycles (write, erase, fast read, read status, etc.) except for the read cycle which always run at 20 MHz. 000 = 20 MHz 001 = 33 MHz All other values = Reserved. This register is locked when the SPI Configuration Lock-Down bit is set.
15	Reserved
14	**Data Cycle (DS)**—R/W. When set to 1, there is data that corresponds to this transaction. When 0, no data is delivered for this cycle, and the DBC and data fields themselves are don't cares.
13:8	**Data Byte Count (DBC)—**R/W. This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The valid settings (in decimal) are any value from 0 to 3. The number of bytes transferred is the value of this field plus 1. Note that when this field is 00b, then there is 1 byte to transfer and that 11b means there are 4 bytes to transfer.
7	Reserved
6:4	**Cycle Opcode Pointer (COP)**—R/W. This field selects one of the programmed opcodes in the Opcode Menu to be used as the SPI Command/Opcode. In the case of an Atomic Cycle Sequence, this determines the second command.
3	**Sequence Prefix Opcode Pointer (SPOP)—**R/W. This field selects one of the two programmed prefix opcodes for use when performing an Atomic Cycle Sequence. A value of 0 points to the opcode in the least significant byte of the Prefix Opcodes register. By making this programmable, the PCH supports flash devices that have different opcodes for enabling writes to the data space vs. status register.
2	**Atomic Cycle Sequence (ACS)—**R/W. When set to 1 along with the SCGO assertion, the PCH will execute a sequence of commands on the SPI interface without allowing the LAN component to arbitrate and interleave cycles. The sequence is composed of: • Atomic Sequence Prefix Command (8-bit opcode only) • Primary Command specified below by software (can include address and data) • Polling the Flash Status Register (opcode 05h) until bit 0 becomes 0b. The SPI Cycle in Progress bit remains set and the Cycle Done Status bit remains unset until the Busy bit in the Flash Status Register returns 0.
1	**SPI Cycle Go (SCGO)—**R/WS. This bit always returns 0 on reads. However, a write to this register with a '1' in this bit starts the SPI cycle defined by the other bits of this register. The "SPI Cycle in Progress" (SCIP) bit gets set by this action. Hardware must ignore writes to this bit while the Cycle In Progress bit is set. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write.
0	Reserved

21.4.15 PREOP—Prefix Opcode Configuration Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 94h | Attribute: R/W
Default Value: 0000h | Size: 16 bits

Bit	Description
15:8	**Prefix Opcode 1**—R/W. Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.
7:0	**Prefix Opcode 0**—R/W. Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.

Note: This register is not writable when the SPI Configuration Lock-Down bit (MBARB + 00h:15) is set.

21.4.16 OPTYPE—Opcode Type Configuration Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 96h | Attribute: R/W
Default Value: 0000h | Size: 16 bits

Entries in this register correspond to the entries in the Opcode Menu Configuration register.

Note: The definition below only provides write protection for opcodes that have addresses associated with them. Therefore, any erase or write opcodes that do not use an address should be avoided (for example, "Chip Erase" and "Auto-Address Increment Byte Program").

Bit	Description
15:14	**Opcode Type 7**—R/W. See the description for bits 1:0
13:12	**Opcode Type 6**—R/W. See the description for bits 1:0
11:10	**Opcode Type 5**—R/W. See the description for bits 1:0
9:8	**Opcode Type 4**—R/W. See the description for bits 1:0
7:6	**Opcode Type 3**—R/W. See the description for bits 1:0
5:4	**Opcode Type 2**—R/W. See the description for bits 1:0
3:2	**Opcode Type 1**—R/W. See the description for bits 1:0
1:0	**Opcode Type 0**—R/W. This field specifies information about the corresponding Opcode 0. This information allows the hardware to 1) know whether to use the address field and 2) provide BIOS and Shared Flash protection capabilities. The encoding of the two bits is: 00 = No address associated with this Opcode; Read cycle type 01 = No address associated with this Opcode; Write cycle type 10 = Address required; Read cycle type 11 = Address required; Write cycle type

Note: This register is not writable when the SPI Configuration Lock-Down bit (MBARB + 00h:15) is set.

21.4.17 OPMENU—Opcode Menu Configuration Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 98h Attribute: R/W
Default Value: 0000000000000000h Size: 64 bits

Eight entries are available in this register to give GbE a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices.

Note: It is recommended that GbE avoid programming Write Enable opcodes in this menu. Malicious software could then perform writes and erases to the SPI flash without using the atomic cycle mechanism. This could cause functional failures in a shared flash environment. Write Enable opcodes should only be programmed in the Prefix Opcodes.

Bit	Description
63:56	**Allowable Opcode 7**—R/W. See the description for bits 7:0
55:48	**Allowable Opcode 6**—R/W. See the description for bits 7:0
47:40	**Allowable Opcode 5**—R/W. See the description for bits 7:0
39:32	**Allowable Opcode 4**—R/W. See the description for bits 7:0
31:24	**Allowable Opcode 3**—R/W. See the description for bits 7:0
23:16	**Allowable Opcode 2**—R/W. See the description for bits 7:0
15:8	**Allowable Opcode 1**—R/W. See the description for bits 7:0
7:0	**Allowable Opcode 0**—R/W. Software programs an SPI opcode into this field for use when initiating SPI commands through the Control Register.

Note: This register is not writable when the SPI Configuration Lock-Down bit (MBARB + 00h:15) is set.

§

22 Thermal Sensor Registers (D31:F6)

22.1 PCI Bus Configuration Registers

Table 22-1. Thermal Sensor Register Address Map

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	1D24h	RO
04h–05h	CMD	Command Register	0000h	R/W, RO
06h–07h	STS	Device Status	0010h	R/WC, RO
08h	RID	Revision ID	00h	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	80h	RO
0Bh	BCC	Base Class Code	11h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	LT	Latency Timer	00h	RO
0Eh	HTYPE	Header Type	00h	RO
0Fh	BIST	Built-in Self Test	00h	RO
10h–13h	TBAR	Thermal Base Address (Memory)	00000004h	R/W, RO
14h–17h	TBARH	Thermal Base Address High DWord	00000000h	RO
2Ch–2Dh	SVID	Subsystem Vendor Identifier	0000h	R/WO
2Eh–2Fh	SID	Subsystem Identifier	0000h	R/WO
34h	CAP_PTR	Capabilities Pointer	50h	RO
3Ch	INTLN	Interrupt Line	00h	R/W
3Dh	INTPN	Interrupt Pin	03h	RO
40h–43h	TBARB	BIOS Assigned Thermal Base Address	00000004h	R/W, RO
44h–47h	TBARBH	BIOS Assigned Thermal Base High DWord	00000000h	R/W
50h–51h	PID	Power Management Identifiers	8001h	RO
52h–53h	PC	Power Management Capabilities	0023h	RO
54–57h	PCS	Power Management Control and Status	0008h	R/W, RO

22.1.1 VID—Vendor Identification Register

Offset Address:	00h–01h	Attribute:	RO
Default Value:	8086h	Size:	16 bit
Lockable:	No	Power Well:	Core

Bit	Description
15:0	**Vendor ID**—RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

22.1.2 DID—Device Identification Register

Offset Address:	02h–03h	Attribute:	RO
Default Value:	1D24h	Size:	16 bits

Bit	Description
15:0	**Device ID (DID)—**RO. Indicates the device number assigned by the SIG.

22.1.3 CMD—Command Register

Address Offset:	04h–05h	Attribute:	RO, R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable (ID)—**R/W. Enables the device to assert an INTx#. 0 = When cleared, the INTx# signal may be asserted. 1 = When set, the Thermal logic's INTx# signal will be deasserted.
9	**FBE (Fast Back to Back Enable)—**RO. Not implemented. Hardwired to 0.
8	**SEN (SERR Enable)—**RO. Not implemented. Hardwired to 0.
7	**WCC (Wait Cycle Control)—**RO. Not implemented. Hardwired to 0.
6	**PER (Parity Error Response)—**RO. Not implemented. Hardwired to 0.
5	**VPS (VGA Palette Snoop)**—RO. Not implemented. Hardwired to 0.
4	**MWI (Memory Write and Invalidate Enable)**—RO. Not implemented. Hardwired to 0.
3	**SCE (Special Cycle Enable)—**RO. Not implemented. Hardwired to 0.
2	**BME (Bus Master Enable)—**R/W. 0 = Function disabled as bus master. 1 = Function enabled as bus master.
1	**Memory Space Enable (MSE)—**R/W. 0 = Disable 1 = Enable. Enables memory space accesses to the Thermal registers.
0	**IOS (I/O Space)—**RO. The Thermal logic does not implement IO Space; therefore, this bit is hardwired to 0.

22.1.4 STS—Status Register

Address Offset: 06h–07h
Attribute: R/WC, RO
Default Value: 0010h
Size: 16 bits

Bit	Description
15	**Detected Parity Error (DPE)**—R/WC. This bit is set whenever a parity error is seen on the internal interface for this function, regardless of the setting of bit 6 in the command register. Software clears this bit by writing a 1 to this bit location.
14	SERR# Status (SERRS)—RO. Not implemented. Hardwired to 0.
13	Received Master Abort (RMA)—RO. Not implemented. Hardwired to 0.
12	Received Target Abort (RTA)—RO. Not implemented. Hardwired to 0.
11	Signaled Target-Abort (STA)—RO. Not implemented. Hardwired to 0.
10:9	DEVSEL# Timing Status (DEVT)—RO. Does not apply. Hardwired to 0.
8	Master Data Parity Error (MDPE)—RO. Not implemented. Hardwired to 0.
7	Fast Back to Back Capable (FBC)—RO. Does not apply. Hardwired to 0.
6	Reserved
5	66 MHz Capable (C66)—RO. Does not apply. Hardwired to 0.
4	**Capabilities List Exists (CLIST)**—RO. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
3	**Interrupt Status (IS)**—RO. Reflects the state of the INTx# signal at the input of the enable/disable circuit. This bit is a 1 when the INTx# is asserted. This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register).
2:0	Reserved

22.1.5 RID—Revision Identification Register

Address Offset: 08h
Attribute: RO
Default Value: 00h
Size: 8 bits

Bit	Description
7:0	**Revision ID (RID)**—RO. Indicates the device specific revision identifier.

22.1.6 PI—Programming Interface Register

Address Offset: 09h
Attribute: RO
Default Value: 00h
Size: 8 bits

Bit	Description
7:0	**Programming Interface (PI)**—RO. The PCH Thermal logic has no standard programming interface.

22.1.7 SCC—Sub Class Code Register

Address Offset: 0Ah
Default Value: 80h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Sub Class Code (SCC)—**RO. Value assigned to the PCH Thermal logic.

22.1.8 BCC—Base Class Code Register

Address Offset: 0Bh
Default Value: 11h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Base Class Code (BCC)—**RO. Value assigned to the PCH Thermal logic.

22.1.9 CLS—Cache Line Size Register

Address Offset: 0Ch
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Cache Line Size (CLS)—**RO. Does not apply to PCI Bus Target-only devices.

22.1.10 LT—Latency Timer Register

Address Offset: 0Dh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7:0	**Latency Timer (LT)—**RO. Does not apply to PCI Bus Target-only devices.

22.1.11 HTYPE—Header Type Register

Address Offset: 0Eh
Default Value: 00h
Attribute: RO
Size: 8 bits

Bit	Description
7	**Multi-Function Device (MFD)—**RO. This bit is 0 because a multi-function device only needs to be marked as such in Function 0, and the Thermal registers are not in Function 0.
6:0	**Header Type (HTYPE)—**RO. Implements Type 0 Configuration header.

22.1.12 TBAR—Thermal Base Register

Address Offset:	10h–13h	Attribute:	R/W, RO
Default Value:	00000004h	Size:	32 bits

This BAR creates 4K bytes of memory space to signify the base address of Thermal memory mapped configuration registers. This memory space is active when the Command (CMD) register Memory Space Enable (MSE) bit is set and either TBAR[31:12] or TBARH are programmed to a non-zero address. This BAR is owned by the operating system, and allows the operating system to locate the Thermal registers in system memory space.

Bit	Description
31:12	**Thermal Base Address (TBA)—**R/W. This field provides the base address for the Thermal logic memory mapped configuration registers. 4 KB bytes are requested by hardwiring bits 11:4 to 0s.
11:4	Reserved
3	**Prefetchable (PREF)—**RO. Indicates that this BAR is NOT pre-fetchable.
2:1	**Address Range (ADDRNG)—**RO. Indicates that this BAR can be located anywhere in 64 bit address space.
0	**Space Type (SPTYP)—**RO. Indicates that this BAR is located in memory space.

22.1.13 TBARH—Thermal Base High DWord Register

Address Offset:	14h–17h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

This BAR extension holds the high 32 bits of the 64 bit TBAR. In conjunction with TBAR, it creates 4 KB of memory space to signify the base address of Thermal memory mapped configuration registers.

Bit	Description
31:0	**Thermal Base Address High (TBAH)—**R/W. TBAR bits 63:32.

22.1.14 SVID—Subsystem Vendor ID Register

Address Offset:	2Ch–2Dh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits

This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other(s).

Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SID to create one 32-bit write. This register is not affected by $D3_{HOT}$ to D0 reset.

Bit	Description
15:0	**SVID (SVID)—**R/WO. These R/WO bits have no PCH functionality.

22.1.15 SID—Subsystem ID Register

Address Offset:	2Eh–2Fh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits

This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one subsystem from the other(s).

Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SVID to create one 32-bit write. This register is not affected by $D3_{HOT}$ to D0 reset.

Bit	Description
15:0	**SID (SAID)**—R/WO. These R/WO bits have no PCH functionality.

22.1.16 CAP_PTR—Capabilities Pointer Register

Address Offset:	34h	Attribute:	RO
Default Value:	50h	Size:	8 bits

Bit	Description
7:0	**Capability Pointer (CP)**—RO. Indicates that the first capability pointer offset is offset 50h (Power Management Capability).

22.1.17 INTLN—Interrupt Line Register

Address Offset:	3Ch	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	**Interrupt Line**—R/W. PCH hardware does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

22.1.18 INTPN—Interrupt Pin Register

Address Offset:	3Dh	Attribute:	RO
Default Value:	See Description	Size:	8 bits

Bit	Description
7:4	RsvdP Reserved
3:0	**Interrupt Pin**—RO. This reflects the value of the Device 31 interrupt pin bits 27:24 (TTIP) in chipset configuration space.

22.1.19 TBARB—BIOS Assigned Thermal Base Address Register

Address Offset:	40h–43h	Attribute:	R/W, RO
Default Value:	00000004h	Size:	32 bits

This BAR creates 4 KB of memory space to signify the base address of Thermal memory mapped configuration registers. This memory space is active when TBARB.SPTYPEN is asserted. This BAR is owned by the BIOS, and allows the BIOS to locate the Thermal registers in system memory space. If both TBAR and TBARB are programmed, then the operating system and BIOS each have their own independent "view" of the Thermal registers, and must use the TSIU register to denote Thermal registers ownership/ availability.

Bit	Description
31:12	**Thermal Base Address (TBA)—**R/W. This field provides the base address for the Thermal logic memory mapped configuration registers. 4 KB bytes are requested by hardwiring bits 11:4 to 0s.
11:4	Reserved
3	**Prefetchable (PREF)—**RO. Indicates that this BAR is NOT pre-fetchable.
2:1	**Address Range (ADDRNG)—**RO. Indicates that this BAR can be located anywhere in 64 bit address space.
0	**Space Type Enable (SPTYPEN)—**R/W. 0 = Disable. 1 = Enable. When set to 1b by software, enables the decode of this memory BAR.

22.1.20 TBARBH—BIOS Assigned Thermal Base High DWord Register

Address Offset:	44h–47h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

This BAR extension holds the high 32 bits of the 64 bit TBARB.

Bit	Description
31:0	**Thermal Base Address High (TBAH)—**R/W. TBAR bits 61:32.

22.1.21 PID—PCI Power Management Capability ID Register

Address Offset:	50h–51h	Attribute:	RO
Default Value:	0001h	Size:	16 bits

Bit	Description
15:8	**Next Capability (NEXT)—**RO. Indicates that this is the last capability structure in the list.
7:0	**Cap ID (CAP)—**RO. Indicates that this pointer is a PCI power management capability

22.1.22 PC—Power Management Capabilities Register

Address Offset: 52h–53h
Default Value: 0023h
Attribute: RO
Size: 16 bits

Bit	Description
15:11	**PME_Support**—RO. Indicates PME# is not supported
10	**D2_Support**—RO. The D2 state is not supported.
9	**D1_Support**—RO. The D1 state is not supported.
8:6	**Aux_Current**—RO. PME# from D3COLD state is not supported, therefore this field is 000b.
5	**Device Specific Initialization (DSI)**—RO. Indicates that device-specific initialization is required.
4	**Reserved**
3	PME Clock (PMEC)—RO. Does not apply. Hardwired to 0.
2:0	**Version (VS)**—RO. Indicates support for Revision 1.2 of the *PCI Power Management Specification.*

22.1.23 PCS—Power Management Control And Status Register

Address Offset: 54h–57h
Default Value: 00000008h
Attribute: RO, R/W
Size: 32 bits

Bit	Description
31:24	**Data**—RO. Does not apply. Hardwired to 0s.
23	**Bus Power/Clock Control Enable (BPCCE)**—RO. Hardwired to 0.
22	**B2/B3 Support (B23)**—RO. Does not apply. Hardwired to 0.
21:16	Reserved
15	**PME Status (PMES)**—RO. This bit is always 0, since this PCI Function does not generate PME#
14:9	**Reserved**
8	**PME Enable (PMEE)**—RO. This bit is always zero, since this PCI Function does not generate PME#
7:4	Reserved
3	**No Soft Reset**—RO. When set to 1, this bit indicates that devices transitioning from $D3_{HOT}$ to D0 because of PowerState commands do not perform an internal reset. Configuration context is preserved. Upon transition from $D3_{HOT}$ to D0 initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.
2	Reserved
1:0	**Power State (PS)**—R/W. This field is used both to determine the current power state of the Thermal controller and to set a new power state. The values are: 00 = D0 state 11 = $D3_{HOT}$ state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the $D3_{HOT}$ states, the Thermal controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. When software changes this value from the $D3_{HOT}$ state to the D0 state, **no** internal warm (soft) reset is generated.

22.2 Thermal Memory Mapped Configuration Registers (Thermal Sensor – D31:F26)

The base memory for these thermal memory mapped configuration registers is specified in the TBARB (D31:F6:Offset 40h). The individual registers are then accessible at TBARB + Offset.

Table 22-2. Thermal Memory Mapped Configuration Register Address Map

Offset	Mnemonic	Register Name	Default	Host Access
0h	TSIU	Thermal Sensor In Use	00h	RO, R/W
1h	TSE	Thermal Sensor Enable	00h	R/W
2h	TSS	Thermal Sensor Status	00h	R/W
3h	TSTR	Thermal Sensor Thermometer Read	FFh	RO
4–7h	TSTTP	Thermal Sensor Temperature Trip Point	00000000h	R/W
8h	TSC0	Thermal Sensor Catastrophic Lock Down	00h	R/W
0Ch	TSES	Thermal Sensor Error Status	00h	R/WC
0Dh	TSGPEN	Thermal Sensor General Purpose Event Enable	00h	R/W
0Eh	TSPC	Thermal Sensor Policy Control	00h	R/W, RO
14–15h	PTA	PCH Temperature Adjust	0000h	R/W
1A–1Bh	TRC	Thermal Reporting control	0000h	R/W
3Fh	AE	Alert enable	00h	R/W
56–57h	PTL	Processor Temperature Limit	0000h	R/W
60–61h	PTV	Processor Temperature Value	0000h	RO
6C–6Fh	TT	Thermal Throttling	00000000h	R/W
70h	PHL	PCH Hot Level	00h	R/W
82h	TSPIEN	Thermal Sensor PCI Interrupt Event enable	00h	R/W
83H	TSLOCK	Thermal Sensor Register Lock Controls	00h	R/W
AC–AFh	TC2	Thermal Compares 2	00000000h	RO
B0–B3h	DTV	DIMM Temperature values	00000000h	RO
D8–DBh	ITV	Internal Temperature Values	00000000h	RO

22.2.1 TSIU—Thermal Sensor In Use Register

Offset Address: TBARB+00h
Attribute: RO, R/W
Default Value: 00h
Size: 8 bit

Bit	Description
7:1	Reserved
0	**Thermal Sensor In Use (TSIU)—**R/W. This is a software semaphore bit. After a core well reset, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the thermal sensor. This bit has no other effect on the hardware, and is only used as a semaphore among various independent software threads that may need to use the thermal sensor. Software that reads this register but does not intend to claim exclusive access of the thermal sensor must write a 1 to this bit if it reads a 0, in order to allow other software threads to claim it.

22.2.2 TSE—Thermal Sensor Enable Register

Offset Address:	TBARB+01h	Attribute:	R/W
Default Value:	00h	Size:	8 bit

Bit	Description
7:0	**Thermal Sensor Enable (TSE)—**R/W. BIOS programs this register to enable the thermal sensor.

22.2.3 TSS—Thermal Sensor Status Register

Offset Address:	TBARB+02h	Attribute:	RO
Default Value:	00h	Size:	8 bit

Bit	Description
7	**Catastrophic Trip Indicator (CTI)**—RO. 0 = The temperature is below the catastrophic setting. 1 = The temperature is above the catastrophic setting.
6	**Hot Trip Indicator (HTI)**—RO. 0 = The temperature is below the Hot setting. 1 = The temperature is above the Hot setting.
5	**Auxiliary Trip Indicator (ATI)**—RO. 0 = The temperature is below the Auxiliary setting. 1 = The temperature is above the Auxiliary setting.
4	Reserved
3	**Auxiliary2 Trip Indicator (ATI)**—RO. 0 = The temperature is below the Auxiliary2 setting. 1 = The temperature is above the Auxiliary2 setting.
2:0	Reserved

22.2.4 TSTR—Thermal Sensor Thermometer Read Register

Offset Address:	TBARB+03h	Attribute:	RO
Default Value:	FFh	Size:	8 bit

This register generally provides the calibrated temperature from the thermometer circuit when the thermometer is enabled.

Bit	Description
7:0	**Thermometer Reading (TR)**—RO. Value corresponds to the thermal sensor temperature. This register has a straight binary encoding that ranges from 0h to FFh. The value in this field is valid **only** if the TR value is between 00h and 7Fh.

22.2.5 TSTTP—Thermal Sensor Temperature Trip Point Register

Offset Address: TBARB+04h Attribute: R/W
Default Value: 00000000h Size: 32 bit

Bit	Description
31:24	**Auxiliary2 Trip Point Setting (A2TPS)**—R/W. These bits set the Auxiliary2 trip point. These bits are lockable by programming the policy-lock down bit (bit 7) of TSPC register. These bits may only be programmed from 0h to 7Fh. Setting bit 31 is illegal.
23:16	**Auxiliary Trip Point Setting (ATPS)**—R/W. These bits set the Auxiliary trip point. These bits are lockable using programming the policy-lock down bit (bit 7) of TSPC register. These bits may only be programmed from 0h to 7Fh. Setting bit 23 is illegal.
15:8	**Hot Trip Point Setting (HTPS)**—R/W. These bits set the Hot trip point. These bits are lockable by programming the policy-lock down bit (bit 7) of TSPC register. These bits may only be programmed from 0h to 7Fh. Setting bit 15 is illegal. BIOS should program to 3Ah for setting Hot Trip Point to 108 °C.
7:0	**Catastrophic Trip Point Setting (CTPS)**—R/W. These bits set the catastrophic trip point. These bits are lockable using TSCO.bit 7. These bits may only be programmed from 0h to 7Fh. Setting bit 7 is illegal. BIOS should program to 2Bh for setting Catastrophic Trip Point to 120 °C.

22.2.6 TSCO—Thermal Sensor Catastrophic Lock-Down Register

Offset Address: TBARB+08h Attribute: R/W
Default Value: 00h Size: 8 bit

Bit	Description
7	**Lock bit for Catastrophic (LBC)**—R/W 0 = Catastrophic programming interface is unlocked 1 = Locks the Catastrophic programming interface including TSTTP.bits[7:0]. This bit may only be set to a 0 by a host partitioned reset (note that CF9 warm reset is a host partitioned reset). Writing a 0 to this bit has no effect. TSCO.[7] is unlocked by default and can be locked through BIOS.
6:0	Reserved

22.2.7 TSES—Thermal Sensor Error Status Register

Offset Address:	TBARB+0Ch	Attribute:	R/WC
Default Value:	00h	Size:	8 bit

Bit	Description
7	**Auxiliary2 High-to-LowEvent—**R/WC. 0 = No trip occurs. 1 = Indicates that an Auxiliary2 Thermal Sensor trip event occurred based on a higher to lower temperature transition through the trip point. Software must write a 1 to clear this status bit.
6	**Catastrophic High-to-LowEvent—**R/WC. 0 = No trip occurs. 1 = Indicates that a Catastrophic Thermal Sensor trip event occurred based on a higher to lower temperature transition through the trip point. 1 = Software must write a 1 to clear this status bit.
5	**Hot High-to-LowEvent—**R/WC. 0 = No trip occurs. 1 = Indicates that a Hot Thermal Sensor trip event occurred based on a higher to lower temperature transition through the trip point. Software must write a 1 to clear this status bit.
4	**Auxiliary High-to-LowEvent—**R/WC. 0 = No trip occurs. 1 = Indicates that an Auxiliary Thermal Sensor trip event occurred based on a higher to lower temperature transition through the trip point. Software must write a 1 to clear this status bit.
3	**Auxiliary2 Low-to-High Event—**R/WC. 0 = No trip occurs. 1 = Indicates that an Auxiliary2 Thermal Sensor trip event occurred based on a lower to higher temperature transition through the trip point. Software must write a 1 to clear this status bit.
2	**Catastrophic Low-to-High Event—**R/WC. 0 = No trip occurs. 1 = Indicates that a Catastrophic Thermal Sensor trip event occurred based on a lower to higher temperature transition through the trip point. Software must write a 1 to clear this status bit.
1	**Hot Low-to-High Event—**R/WC. 0 = No trip occurs. 1 = Indicates that a hot Thermal Sensor trip event occurred based on a lower to higher temperature transition through the trip point. Software must write a 1 to clear this status bit.
0	**Auxiliary Low-to-High Event—**R/WC. 0 = No trip occurs. 1 = Indicates that an Auxiliary Thermal Sensor trip event occurred based on a lower to higher temperature transition through the trip point. Software must write a 1 to clear this status bit.

22.2.8 TSGPEN—Thermal Sensor General Purpose Event Enable Register

Offset Address:	TBARB+0Dh	Attribute:	R/W
Default Value:	00h	Size:	8 bit

This register controls the conditions that result in General Purpose Events to be signalled from Thermal Sensor trip events.

Bit	Description
7	**Auxiliary2 High-to-Low Enable—**R/W. 0 = Corresponding status bit does not result in General Purpose event. 1 = General purpose event is signaled when the corresponding status bit is set in the Thermal Error Status Register.
6	**Catastrophic High-to-Low Enable—**R/W. 0 = Corresponding status bit does not result in General Purpose event. 1 = General purpose event is signaled when the corresponding status bit is set in the Thermal Error Status Register.
5	**Hot High-to-Low Enable—**R/W. 0 = Corresponding status bit does not result in General Purpose event. 1 = General purpose event is signaled when the corresponding status bit is set in the Thermal Error Status Register.
4	**Auxiliary High-to-Low Enable—**R/W. 0 = Corresponding status bit does not result in General Purpose event. 1 = General purpose event is signaled when the corresponding status bit is set in the Thermal Error Status Register.
3	**Auxiliary2 Low-to-High Enable—**R/W. 0 = Corresponding status bit does not result in General Purpose event. 1 = General purpose event is signaled when the corresponding status bit is set in the Thermal Error Status Register.
2	**Catastrophic Low-to-High Enable—**R/W. 0 = Corresponding status bit does not result in General Purpose event. 1 = General purpose event is signaled when the corresponding status bit is set in the Thermal Error Status Register.
1	**Hot Low-to-High Enable**—R/W. 0 = Corresponding status bit does not result in General Purpose event. 1 = General purpose event is signaled when the corresponding status bit is set in the Thermal Error Status Register.
0	**Auxiliary Low-to-High Enable—**R/W. 0 = Corresponding status bit does not result in General Purpose event. 1 = General purpose event is signaled when the corresponding status bit is set in the Thermal Error Status Register.

22.2.9 TSPC—Thermal Sensor Policy Control Register

Offset Address:	TBARB+0Eh	Attribute:	R/W, RO
Default Value:	00h	Size:	8 bit

Bit	Description
7	**Policy Lock-Down Bit**—R/W. 0 = This register can be programmed and modified. 1 = Prevents writes to this register and TSTTP.bits [31:16] (offset 04h). ***Note:*** TSCO.bit 7 (offset 08h) and TSLOCK.bit2 (offset 83h) must also be 1 when this bit is set to 1. This bit is reset to 0 by a host partitioned reset (note that CF9 warm reset is a host partitioned reset). Writing a 0 to this bit has no effect.
6	**Catastrophic Power-Down Enable—**R/W. When set to 1, the power management logic unconditionally transitions to the S5 state when a catastrophic temperature is detected by the sensor. ***Note:*** BIOS should set this bit to 1 to enable Catastrophic power-down.
5:4	Reserved
3	**SMI Enable on Auxiliary2 Thermal Sensor Trip**—R/W. 0 = Disables SMI# assertion for Auxiliary2 Thermal Sensor events. 1 = Enables SMI# assertions on Auxiliary2 Thermal Sensor events for either low-to-high or high-to-low events. (Both edges are enabled by this bit.)
2	**SMI Enable on Catastrophic Thermal Sensor Trip**—R/W. 0 = Disables SMI# assertion for Catastrophic Thermal Sensor events. 1 = Enables SMI# assertions on Catastrophic Thermal Sensor events for either low-to-high or high-to-low events. (Both edges are enabled by this bit.)
1	**SMI Enable on Hot Thermal Sensor Trip**—R/W. 0 = Disables SMI# assertion for Hot Thermal Sensor events. 1 = Enables SMI# assertions on Hot Thermal Sensor events for either low-to-high or high-to-low events. (Both edges are enabled by this bit.)
0	**SMI Enable on Auxiliary Thermal Sensor Trip**—R/W. 0 = Disables SMI# assertion for Auxiliary Thermal Sensor events. 1 = Enables SMI# assertions on Auxiliary Thermal Sensor events for either low-to-high or high-to-low events. (Both edges are enabled by this bit.)

22.2.10 PTA—PCH Temperature Adjust Register

Offset Address:	TBARB+14h	Attribute:	R/W
Default Value:	0000h	Size:	16 bit

Bit	Description
15:8	**PCH Slope (PSLOPE)—**R/W. This field contains the PCH slope for calculating PCH temperature. The bits are locked by AE.bit7 (offset 3Fh). ***Note:*** When thermal reporting is enabled, BIOS must write DEh into this field.
7:0	**Offset (POFFSET)—**R/W This field contains the PCH offset for calculating PCH temperature. The bits are locked by AE.bit7 (offset 3Fh). ***Note:*** When thermal reporting is enabled, BIOS must write 87h into this field.

22.2.11 TRC—Thermal Reporting Control Register

Offset Address: TBARB+1Ah Attribute: R/W
Default Value: 0000h Size: 16 bit

Bit	Description
15:13	Reserved
12	**SMBUS Thermal Data Reporting Enable**—R/W. 0 = Disable 1 = Enable
11:6	Reserved
5	**PCH Temperature Read Enable**—R/W. 0 = Disables reads of the PCH temperature. 1 = Enables reads of the PCH temperature.
4	Reserved – This bit must be set to 0.
3	**DIMM4 Temperature Read Enable**—R/W 0 = Disables reads of DIMM4 temperature. 1 = Enables reads of DIMM4 temperature.
2	**DIMM3 Temperature Read Enable**—R/W 0 = Disables reads of DIMM3 temperature. 1 = Enables reads of DIMM3 temperature.
1	**DIMM2 Temperature Read Enable**—R/W 0 = Disables reads of DIMM2 temperature. 1 = Enables reads of DIMM2 temperature.
0	**DIMM1 Temperature Read Enable**—R/W. 0 = Disables reads of DIMM1 temperature. 1 = Enables reads of DIMM1 temperature.

22.2.12 AE—Alert Enable Register

Offset Address: TBARB+3Fh Attribute: R/W
Default Value: 00h Size: 8 bit

Bit	Description
7	**Lock Enable**—R/W. 0 = Lock Disabled. 1 = Lock Enabled. This will lock this register (including this bit) This bit is reset by a Host Partitioned Reset. Note that CF9 warm reset is a Host Partitioned Reset.
6:5	Reserved
4	**PCH Alert Enable**—R/W. 0 = Alert Disabled 1 = Alert Enabled When this bit is set, it will assert the PCH's TEMP_ALERT# signal if the PCH temperature is outside the temperature limits. This bit is lockable by bit 7 in this register.
3	**DIMM 1-4 Alert Enable**—R/W. 0 = Alert Disabled 1 = Alert Enabled When this bit is set, it will assert the PCH's TEMP_ALERT# signal if DIMM1-4 temperature is outside of the temperature limits. ***Note:*** The actual DIMMs that are read and used for the alert are enabled in the TRC register (offset 1Ah). This bit is lockable by bit 7 in this register. ***Note:*** Same Upper and Lower limits for triggering TEMP_ALERT# are used for all enabled DIMMs in the system.
2:0	Reserved

22.2.13 PTL—Processor Temperature Limit Register

Offset Address: TBARB+56h Attribute: R/W
Default Value: 0000h Size: 16 bit

Bit	Description
15:0	**Processor Temperature Limit**—R/W. These bits are programmed by BIOS

22.2.14 PTV—Processor Temperature Value Register

Offset Address: TBARB+60h Attribute: RO
Default Value: 0000h Size: 16 bit

Bit	Description
15:8	Reserved
7:0	**Processor Temperature Value**—RO. These bits contain the processor package temperature.

22.2.15 TT—Thermal Throttling Register

Offset Address: TBARB+6Ch Attribute: R/W
Default Value: 00000000h Size: 32 bit

Bit	Description
31:0	BIOS must program this field to 05201B16h

22.2.16 PHL—PCH Hot Level Register

Offset Address: TBARB+70h Attribute: R/W
Default Value: 00h Size: 8 bit

Bit	Description
7:0	PCH Hot Level (PHL)—R/W. When temperature reading in Thermal Sensor Thermometer Read (TSTR) is less than PHL programmed here, this will assert PCHHOT# (active low). (Note that TSTR reading of 00h is the hottest temperature and 7Fh is the lowest temperature.) Default state for this register is PHL disabled (00h). For using the PCHHOT# functionality, a soft strap has to be configured and BIOS programs this PHL value.

22.2.17 TSPIEN—Thermal Sensor PCI Interrupt Enable Register

Offset Address: TBARB+82h Attribute: R/W
Default Value: 00h Size: 8 bit

This register controls the conditions that result in PCI interrupts to be signalled from Thermal Sensor trip events. Software (device driver) needs to ensure that it can support PCI interrupts, even though BIOS may enable PCI interrupt capability through this register.

Bit	Description
7	**Auxiliary2 High-to-Low Enable—**R/W. 0 = Corresponding status bit does not result in PCI interrupt. 1 = PCI interrupt is signaled when the corresponding status bit is set in the Thermal Error Status Register.
6	**Catastrophic High-to-Low Enable—**R/W. 0 = Corresponding status bit does not result in PCI interrupt. 1 = PCI interrupt is signalled when the corresponding status bit is set in the Thermal Error Status Register.
5	**Hot High-to-Low Enable—**R/W. 0 = Corresponding status bit does not result in PCI interrupt. 1 = PCI interrupt is signaled when the corresponding status bit is set in the Thermal Error Status Register.
4	**Auxiliary High-to-Low Enable—**R/W. 0 = Corresponding status bit does not result in PCI interrupt. 1 = PCI interrupt is signaled when the corresponding status bit is set in the Thermal Error Status Register.
3	**Auxiliary2 Low-to-High Enable—**R/W. 0 = Corresponding status bit does not result in PCI interrupt. 1 = PCI interrupt is signaled when the corresponding status bit is set in the Thermal Error Status Register.
2	**Catastrophic Low-to-High Enable—**R/W. 0 = Corresponding status bit does not result in PCI interrupt. 1 = PCI interrupt is signalled when the corresponding status bit is set in the Thermal Error Status Register.
1	**Hot Low-to-High Enable**—R/W. 0 = Corresponding status bit does not result in PCI interrupt. 1 = PCI interrupt is signaled when the corresponding status bit is set in the Thermal Error Status Register.
0	**Auxiliary Low-to-High Enable—**R/W. 0 = Corresponding status bit does not result in PCI interrupt. 1 = PCI interrupt is signaled when the corresponding status bit is set in the Thermal Error Status Register.

22.2.18 TSLOCK—Thermal Sensor Register Lock Control Register

Offset Address:	TBARB+83h	Attribute:	R/W
Default Value:	00h	Size:	8 bit

Bit	Description
7:3	Reserved
2	**Lock Control**—R/W. This bit can only be set to a 0 by a host-partitioned reset. Writing a 0 to this bit has no effect. 1 = Hot Trip programming interface (bits [15:8] of TSTTP. is locked. ***Note:*** CF9 warm reset is a host-partitioned reset.
1:0	Reserved

22.2.19 TC2—Thermal Compares 2 Register

Offset Address:	TBARB+ACh	Attribute:	RO
Default Value:	00000000h	Size:	32 bit

Bits [31:16] of this register are set when an external controller (for example, EC) does the Write DIMM Temp Limits Command. Refer to Section 5.22.2 for more information.

Bits [15:0] of this register are set when an external controller (for example, EC) does the Write PCH Temp Limits Command. Refer to Section 5.22.2 for more information.

Bit	Description
31:24	**DIMM Thermal Compare Upper Limit—**RO. This is the upper limit used to compare against the DIMM's temperature. If the DIMM's temperature is greater than this value, then the PCH's alert GPIOl is asserted if enabled.
23:16	**DIMM Thermal Compare Lower Limit—**RO. This is the lower limit used to compare against the DIMM's temperature. If the DIMM's temperature is lower than this value, then the PCH's alert GPIO is asserted if enabled.
15:8	**PCH Thermal Compare Upper Limit—**RO. This is the upper limit used to compare against the PCH temperature. If the PCH temperature is greater than this value, then the PCH's alert GPIO is asserted if enabled.
7:0	**PCH Thermal Compare Lower Limit—**RO. This is the lower limit used to compare against the PCH temperature. If the PCH temperature is lower than this value, then the PCH's alert GPIO is asserted if enabled.

22.2.20 DTV—DIMM Temperature Values Register

Offset Address: TBARB+B0h Attribute: RO
Default Value: 00000000h Size: 32 bit

Bit	Description
31:24	**DIMM3 Temperature**—RO The bits contain DIMM3 temperature data in absolute degrees Celsius. These bits are data byte 8 provided to the external controller when it does a read over SMLink1. Refer to Section 5.22.2 for more details.
23:16	**DIMM2 Temperature**—RO The bits contain DIMM2 temperature data in absolute degrees Celsius. These bits are data byte 7 provided to the external controller when it does a read over SMLink1. Refer to Section 5.22.2 for more details.
15:8	**DIMM1 Temperature**—RO The bits contain DIMM1 temperature data in absolute degrees Celsius. These bits are data byte 6 provided to the external controller when it does a read over SMLink1. Refer to Section 5.22.2 for more details.
7:0	**DIMM0 Temperature**—RO The bits contain DIMM0 temperature data in absolute degrees Celsius. These bits are data byte 5 provided to the external controller when it does a read over SMLink1. Refer to Section 5.22.2 for more details.

22.2.21 ITV—Internal Temperature Values Register

Offset Address: TBARB+D8h Attribute: RO
Default Value: 00000000h Size: 32 bit

Bit	Description
31:24	Reserved
23:16	**Sequence Number**—RO Provides a sequence number which can be used by the host to detect if the Intel ME FW has hung. The value will roll over to 00h from 0Fh. The count is updated at approximately 200 ms. Host software can check this value and if it isn't incriminated over a second or so, software should assume that the ME FW is hung. ***Note:*** If Intel ME is reset, then this value will not change during the reset. After the reset is done, which may take up to 30 seconds, the Intel ME may be on again and this value will start incrementing, indicating that the thermal values are valid again. These bits are data byte 9 provided to the external controller when it does a read over SMLink1. Refer to Section 5.22.2 for more details.
15:8	Reserved
7:0	**PCH Temperature**—RO The bits contain PCH temperature data in absolute degrees Celsius. These bits are data byte 1 provided to the external controller when it does a read over SMLink1. Refer to Section 5.22.2 for more details.

§

23 Intel® Management Engine Subsystem Registers (D22:F0)

23.1 First Intel® Management Engine Interface (Intel® MEI) Configuration Registers (Intel® MEI—D22:F0)

Table 23-1. Intel® MEI Configuration Registers Address Map (Intel® MEI—D22:F0) (Sheet 1 of 2)

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0010h	RO
08h	RID	Revision Identification	See register description	RO
09h–0Bh	CC	Class Code	0C8000h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	PLT	Primary Latency Timer	00h	RO
0Eh	HTYPE	Header Type	00h	RO
10h–17h	MEI0_MBAR	MEI0 MMIO Base Address	00000000 00000004h	R/W, RO
2Ch–2Dh	SVID	Subsystem Vendor ID	0000h	R/WO
2Eh–2Fh	SID	Subsystem ID	0000h	R/WO
34h	CAPP	Capabilities List Pointer	50h	RO
3Ch–3Dh	INTR	Interrupt Information	0000h	R/W, RO
40h–43h	HFS	Host Firmware Status	00000000h	RO
44h–47h	ME_UMA	Intel ME UMA Register	00000000h	RO
48–4Bh	GMES	General Intel ME Status	00000000h	RO
4Ch–4Fh	H_GS	Host General Status	00000000h	RO
50h–51h	PID	PCI Power Management Capability ID	8C01h	RO
52h–53h	PC	PCI Power Management Capabilities	C803h	RO
54h–55h	PMCS	PCI Power Management Control and Status	0008h	R/WC, R/W, RO
8Ch–8Dh	MID	Message Signaled Interrupt Identifiers	0005h	RO
8Eh–8Fh	MC	Message Signaled Interrupt Message Control	0080h	R/W, RO
90h–93h	MA	Message Signaled Interrupt Message Address	00000000h	R/W, RO
94h–97h	MUA	Message Signaled Interrupt Upper Address	00000000h	R/W
98h–99h	MD	Message Signaled Interrupt Message Data	0000h	R/W

Table 23-1. Intel® MEI Configuration Registers Address Map (Intel® MEI—D22:F0) (Sheet 2 of 2)

Offset	Mnemonic	Register Name	Default	Type
A0h	HIDM	Intel MEI Interrupt Delivery Mode	00h	R/W
BC–BF	HERS	Intel MEI Extended Register Status	40000000h	RO
C0–DF	HER[1:8]	Intel MEI Extended Register DW[1:8]	00000000h	RO

23.1.1 VID—Vendor Identification Register (Intel® MEI—D22:F0)

Address Offset: 00h–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Vendor ID (VID)—**RO. This is a 16-bit value assigned to Intel.

23.1.2 DID—Device Identification Register (Intel® MEI—D22:F0)

Address Offset: 02h–03h
Default Value: See bit description
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Device ID (DID)**—RO. This is a 16-bit value assigned to the Intel MEI controller. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Device ID Register.

23.1.3 PCICMD—PCI Command Register (Intel® MEI—D22:F0)

Address Offset: 04h–05h
Default Value: 0000h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable (ID)—**R/W. Disables this device from generating PCI line based interrupts. This bit does not have any effect on MSI operation.
9:3	Reserved
2	Bus Master Enable (BME): This bit controls the Intel MEI host controller's ability to act as a system memory master for data transfers. When this bit is cleared, Intel MEI bus master activity stops and any active DMA engines return to an idle condition. This bit is made visible to firmware through the H_PCI_CSR register, and changes to this bit may be configured by the H_PCI_CSR register to generate an Intel ME MSI. When this bit is 0, Intel MEI is blocked from generating MSI to the host CPU. ***Note:*** This bit does not block Intel MEI accesses to Intel ME-UMA; that is, writes or reads to the host and Intel ME circular buffers through the read window and write window registers still cause Intel ME backbone transactions to Intel ME-UMA.
1	**Memory Space Enable (MSE)**—R/W. This bit controls access to the Intel MEI's memory mapped register space. 0 = Disable. Memory cycles within the range specified by the memory base and limit registers are master aborted. 1 = Enable. Allows memory cycles within the range specified by the memory base and limit registers accepted.
0	I/O Space Enable (IOSE)—RO. Not implemented, hardwired to 0.

23.1.4 PCISTS—PCI Status Register (Intel® MEI—D22:F0)

Address Offset: 06h–07h Attribute: RO
Default Value: 0010h Size: 16 bits

Bit	Description
15:5	Reserved
4	Capabilities List (CL)—RO. Indicates the presence of a capabilities list, hardwired to 1.
3	**Interrupt Status**—RO. Indicates the interrupt status of the device. 0 = Interrupt is deasserted. 1 = Interrupt is asserted.
2:0	Reserved

23.1.5 RID—Revision Identification Register (Intel® MEI—D22:F0)

Offset Address: 08h Attribute: RO
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	**Revision ID**—RO. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Revision ID Register.

23.1.6 CC—Class Code Register (Intel® MEI—D22:F0)

Address Offset: 09h–0Bh Attribute: RO
Default Value: 078000h Size: 24 bits

Bit	Description
23:16	**Base Class Code (BCC)—**RO. Indicates the base class code of the Intel MEI device.
15:8	**Sub Class Code (SCC)**—RO. Indicates the sub class code of the Intel MEI device.
7:0	**Programming Interface (PI)—**RO. Indicates the programming interface of the Intel MEI device.

23.1.7 HTYPE—Header Type Register (Intel® MEI—D22:F0)

Address Offset: 0Eh Attribute: RO
Default Value: 80h Size: 8 bits

Bit	Description
7	**Multi-Function Device** (MFD)—RO. Indicates the Intel MEI host controller is part of a multifunction device.
6:0	Header Layout (HL)—RO. Indicates that the Intel MEI uses a target device layout.

23.1.8 MEI0_MBAR—MEI0 MMIO Base Address Register (Intel® MEI—D22:F0)

Address Offset:	10h–17h	Attribute:	R/W, RO
Default Value:	0000000000000004h	Size:	64 bits

This register allocates space for the MEI0 memory mapped registers.

Bit	Description
63:4	**Base Address (BA)—R/W**. Software programs this field with the base address of this region.
3	**Prefetchable Memory (PM)—**RO. Indicates that this range is not pre-fetchable.
2:1	**Type (TP)**—RO. Set to 10b to indicate that this range can be mapped anywhere in 64-bit address space.
0	**Resource Type Indicator (RTE)**—RO. Indicates a request for register memory space.

23.1.9 SVID—Subsystem Vendor ID Register (Intel® MEI—D22:F0)

Address Offset:	2Ch–2Dh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:0	**Subsystem Vendor ID (SSVID)—**R/WO. Indicates the sub-system vendor identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.

Note: Register must be written as a Word write or as a DWord write with SID register.

23.1.10 SID—Subsystem ID Register (Intel® MEI—D22:F0)

Address Offset:	2Eh–2Fh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:0	**Subsystem ID (SSID)**—R/WO. Indicates the sub-system identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.

Note: Register must be written as a Word write or as a DWord write with SVID register.

23.1.11 CAPP—Capabilities List Pointer Register (Intel® MEI—D22:F0)

Address Offset:	34h	Attribute:	RO
Default Value:	50h	Size:	8 bits

Bit	Description
7:0	**Capabilities Pointer (PTR)—**RO. Indicates that the pointer for the first entry in the capabilities list is at 50h in configuration space.

23.1.12 INTR—Interrupt Information Register (Intel® MEI—D22:F0)

Address Offset:	3Ch–3Dh	Attribute:	R/W, RO
Default Value:	0100h	Size:	16 bits

Bit	Description
15:8	**Interrupt Pin (IPIN)—**RO. This indicates the interrupt pin the Intel MEI host controller uses. A value of 1h/2h/3h/4h indicates that this function implements legacy interrupt on INTA/INTB/INTC/INTD, respectively.
7:0	**Interrupt Line (ILINE)—**R/W. Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

23.1.13 HFS—Host Firmware Status Register (Intel® MEI—D22:F0)

Address Offset:	40h–43h	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	**Host Firmware Status (HFS)**—RO. This register field is used by Firmware to reflect the operating environment to the host.

23.1.14 ME_UMA—Intel® Management Engine UMA Register (Intel® MEI—D22:F0)

Address Offset:	44h–47h	Attribute:	RO
Default Value:	80000000h	Size:	32 bits

Bit	Description
31	**Reserved**—RO. Hardwired to 1. Can be used by host software to discover that this register is valid.
30:7	Reserved
16	**Intel ME UMA Size Valid—**RO. This bit indicates that FW has written to the MUSZ field.
15:6	Reserved
5:0	**Intel ME UMA Size (MUSZ)—**RO. This field reflect Intel ME Firmware's desired size of MEUMA memory region. This field is set by Intel ME firmware prior to core power bringup allowing BIOS to initialize memory. 000000b = 0 MB, No memory allocated to MEUMA 000001b = 1 MB 000010b = 2 MB 000100b = 4 MB 001000b = 8 MB 010000b = 16 MB 100000b = 32 MB

23.1.15 PID—PCI Power Management Capability ID Register (Intel® MEI—D22:F0)

Address Offset:	50h–51h	Attribute:	RO
Default Value:	8C01h	Size:	16 bits

Bit	Description
15:8	**Next Capability (NEXT)—**RO. Value of 8Ch indicates the location of the next pointer.
7:0	**Capability ID (CID)—**RO. Indicates the linked list item is a PCI Power Management Register.

23.1.16 GMES—General Intel® ME Status (Intel® MEI—D22:F0)

Address Offset:	48h–4Bh	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	**General Intel ME Status (ME_GS)**—RO. This field is populated by Intel ME.

23.1.17 H_GS—Host General Status (Intel® MEI—D22:F0)

Address Offset:	4Ch–4Fh	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	**Host General Status(H_GS)**—RO. General Status of Host, this field is not used by Hardware

23.1.18 PC—PCI Power Management Capabilities Register (Intel® MEI—D22:F0)

Address Offset:	52h–53h	Attribute:	RO
Default Value:	C803h	Size:	16 bits

Bit	Description
15:11	**PME_Support (PSUP)**—RO. This five-bit field indicates the power states in which the function may assert PME#. Intel MEI can assert PME# from any D-state except D1 or D2 which are not supported by Intel MEI.
10	**D2_Support (D2S)**—RO. The D2 state is not supported.
9	**D1_Support (D1S)—**RO. The D1 state is not supported.
8:6	**Aux_Current (AC)**—RO. Reports the maximum Suspend well current required when in the $D3_{cold}$ state. Value of 00b is reported.
5	**Device Specific Initialization (DSI)**—RO. Indicates whether device-specific initialization is required.
4	Reserved
3	**PME Clock (PMEC)**—RO. Indicates that PCI clock is not required to generate PME#.
2:0	**Version (VS)**—RO. Hardwired to 011b to indicate support for *Revision 1.2 of the PCI Power Management Specification*.

23.1.19 PMCS—PCI Power Management Control and Status Register (Intel® MEI—D22:F0)

Address Offset:	54h–55h	Attribute:	R/WC, R/W, RO
Default Value:	0008h	Size:	16 bits

Bit	Description
15	**PME Status (PMES)—**R/WC. Bit is set by Intel ME Firmware. Host software clears bit by writing 1 to bit. This bit is reset when CL_RST0# asserted.
14:9	Reserved
8	**PME Enable (PMEE)—**R/W. This bit is read/write and is under the control of host SW. It does not directly have an effect on PME events. However, this bit is shadowed so Intel ME FW can monitor it. Intel ME FW will not cause the PMES bit to transition to '1' while the PMEE bit is '0', indicating that host SW had disabled PME. This bit is reset when PLTRST# asserted.
7:4	Reserved
3	**No_Soft_Reset (NSR)**—RO. This bit indicates that when the Intel MEI host controller is transitioning from $D3_{hot}$ to D0 due to a power state command, it does not perform an internal reset. Configuration context is preserved.
2	Reserved
1:0	**Power State (PS)—**R/W. This field is used both to determine the current power state of the Intel MEI host controller and to set a new power state. The values are: 00 = D0 state (default) 11 = $D3_{hot}$ state The D1 and D2 states are not supported for the Intel MEI host controller. When in the $D3_{hot}$ state, the Intel MEI's configuration space is available, but the register memory spaces are not. Additionally, interrupts are blocked.

23.1.20 MID—Message Signaled Interrupt Identifiers Register (Intel® MEI—D22:F0)

Address Offset:	8Ch–8Dh	Attribute:	RO
Default Value:	0005h	Size:	16 bits

Bit	Description
15:8	**Next Pointer (NEXT)**—RO. Value of 00h indicates that this is the last item in the list.
7:0	**Capability ID (CID)**—RO. Capabilities ID indicates MSI.

23.1.21 MC—Message Signaled Interrupt Message Control Register (Intel® MEI—D22:F0)

Address Offset:	8Eh–8Fh	Attribute:	R/W, RO
Default Value:	0080h	Size:	16 bits

Bit	Description
15:8	Reserved
7	**64 Bit Address Capable** (C64)—RO. Specifies that function is capable of generating 64-bit messages.
6:4	Multiple Message Enable (MME)—RO. Not implemented, hardwired to 0.
3:1	Multiple Message Capable (MMC)—RO. Not implemented, hardwired to 0.
0	**MSI Enable (MSIE)**—R/W. If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.

23.1.22 MA—Message Signaled Interrupt Message Address Register (Intel® MEI—D22:F0)

Address Offset: 90h–93h
Attribute: R/W, RO
Default Value: 00000000h
Size: 32 bits

Bit	Description
31:2	**Address (ADDR)**—R/W. Lower 32 bits of the system specified message address, always DW aligned.
1:0	Reserved

23.1.23 MUA—Message Signaled Interrupt Upper Address Register (Intel® MEI—D22:F0)

Address Offset: 94h–97h
Attribute: R/W
Default Value: 00000000h
Size: 32 bits

Bit	Description
31:0	**Upper Address (UADDR)**—R/W. Upper 32 bits of the system specified message address, always DW aligned.

23.1.24 MD—Message Signaled Interrupt Message Data Register (Intel® MEI—D22:F0)

Address Offset: 98h–99h
Attribute: R/W
Default Value: 0000h
Size: 16 bits

Bit	Description
15:0	**Data (DATA)**—R/W. This 16-bit field is programmed by system software if MSI is enabled. Its content is driven during the data phase of the MSI memory write transaction.

23.1.25 HIDM—Intel® MEI Interrupt Delivery Mode (Intel® MEI—D22:F0)

Address Offset: A0h
Attribute: R/W
Default Value: 00h
Size: 8 bits

Bit	Description
7:2	Reserved
1:0	**Intel MEI Interrupt Delivery Mode (HIDM)**—R/W. These bits control what type of interrupt the Intel MEI will send the host. They are interpreted as follows: 00 = Generate Legacy or MSI interrupt 01 = Generate SCI 10 = Generate SMI 11 = Reserved

23.1.26 HERES—Intel® MEI Extend Register Status (Intel® MEI—D22:F0)

Address Offset:	BCh–BFh	Attribute:	RO
Default Value:	00h	Size:	32 bits

Bit	Description
31	Extend Register Valid (ERV)—RO. Set by firmware after all firmware has been loaded. If ERA field is SHA-1, the result of the extend operation is in HER:5-1. If ERA field is SHA-256, the result of the extend operation is in HER:8-1.
30	Extend Feature Present (EFP)—RO. This bit is hardwired to 1 to allow driver software to easily detect the chipset supports the Extend Register FW measurement feature.
29:4	Reserved
3:0	Extend Register Algorithm (ERA)—RO. This field indicates the hash algorithm used in the FW measurement extend operations. Encodings are: 0h = SHA-1 2h = SHA-256 Other values = Reserved

23.1.27 HERX—Intel® MEI Extend Register DWX (Intel® MEI—D22:F0)

Address Offset:	HER1: C0h–C3h HER2: C4h–C7h HER3: C8h–CBh HER4: CCh–CFh HER5: D0h–D3h HER6: D4h–D7h HER7: D8h–DBh HER8: DCh–DFh	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	Extend Register DWX (ERDWX)—RO. Nth DWORD result of the extend operation. ***Note:*** N Extend Operation is HER[5:1] if using SHA-1. If using SHA-2, then Extend Operation is HER[8:1]

23.2 Second Host Embedded Controller Interface (MEI1) Configuration Registers (Intel® MEI—D22:F1)

Table 23-1. MEI1 Configuration Registers Address Map (Intel® MEI—D22:F1)

Offset	Mnemonic	Register Name	Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0010h	RO
08h	RID	Revision Identification	See register description	RO
09h–0Bh	CC	Class Code	0C8000h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	PLT	Primary Latency Timer	00h	RO
0Eh	HTYPE	Header Type	00h	RO
10h–17h	MEI1_MBAR	MEI1 MMIO Base Address	00000000 00000004h	R/W, RO
2Ch–2Dh	SVID	Subsystem Vendor ID	0000h	R/WO
2Eh–2Fh	SID	Subsystem ID	0000h	R/WO
34h	CAPP	Capabilities List Pointer	50h	RO
3Ch–3Dh	INTR	Interrupt Information	0000h	R/W, RO
40h–43h	HFS	Host Firmware Status	00000000h	RO
48–4Bh	GMES	General Intel ME Status	00000000h	RO
4Ch–4Fh	H_GS	Host General Status	00000000h	RO
50h–51h	PID	PCI Power Management Capability ID	8C01h	RO
52h–53h	PC	PCI Power Management Capabilities	C803h	RO
54h–55h	PMCS	PCI Power Management Control and Status	0008h	R/WC, R/W, RO
8Ch–8Dh	MID	Message Signaled Interrupt Identifiers	0005h	RO
8Eh–8Fh	MC	Message Signaled Interrupt Message Control	0080h	R/W, RO
90h–93h	MA	Message Signaled Interrupt Message Address	00000000h	R/W, RO
94h–97h	MUA	Message Signaled Interrupt Upper Address	00000000h	R/W
98h–99h	MD	Message Signaled Interrupt Message Data	0000h	R/W
A0h	HIDM	Intel MEI Interrupt Delivery Mode	00h	R/W
BC–BF	HERS	Intel MEI Extended Register Status	40000000h	RO
C0–DF	HER[1:8]	Intel MEI Extended Register DW[1:8]	00000000h	RO

23.2.1 VID—Vendor Identification Register (Intel® MEI—D22:F1)

Address Offset:	00h–01h	Attribute:	RO
Default Value:	8086h	Size:	16 bits

Bit	Description
15:0	**Vendor ID (VID)—**RO. This is a 16-bit value assigned to Intel.

23.2.2 DID—Device Identification Register (Intel® MEI—D22:F1)

Address Offset:	02h–03h	Attribute:	RO
Default Value:	See bit description	Size:	16 bits

Bit	Description
15:0	**Device ID (DID)**—RO. This is a 16-bit value assigned to the PCH Intel MEI controller. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Device ID Register.

23.2.3 PCICMD—PCI Command Register (Intel® MEI—D22:F1)

Address Offset:	04h–05h	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable (ID)—**R/W. Disables this device from generating PCI line based interrupts. This bit does not have any effect on MSI operation.
9:3	Reserved
2	Bus Master Enable (BME): Controls the Intel MEI host controller's ability to act as a system memory master for data transfers. When this bit is cleared, Intel MEI bus master activity stops and any active DMA engines return to an idle condition. This bit is made visible to firmware through the H_PCI_CSR register, and changes to this bit may be configured by the H_PCI_CSR register to generate an Intel ME MSI. When this bit is '0', Intel MEI is blocked from generating MSI to the host CPU. ***Note:*** This bit does not block Intel MEI accesses to Intel ME-UMA; that is, writes or reads to the host and Intel ME circular buffers through the read window and write window registers still cause Intel ME backbone transactions to Intel ME-UMA.
1	**Memory Space Enable (MSE)**—R/W. Controls access to the Intel MEI's memory mapped register space. 0 = Disable. Memory cycles within the range specified by the memory base and limit registers are master aborted. 1 = Enable. Allows memory cycles within the range specified by the memory base and limit registers accepted.
0	I/O Space Enable (IOSE)—RO. Not implemented, hardwired to 0.

23.2.4 PCISTS—PCI Status Register (Intel® MEI—D22:F1)

Address Offset:	06h–07h	Attribute:	RO
Default Value:	0010h	Size:	16 bits

Bit	Description
15:5	Reserved
4	Capabilities List (CL)—RO. Indicates the presence of a capabilities list, hardwired to 1.
3	**Interrupt Status**—RO. Indicates the interrupt status of the device. 0 = Interrupt is deasserted. 1 = Interrupt is asserted.
2:0	Reserved

23.2.5 RID—Revision Identification Register (Intel® MEI—D22:F1)

Offset Address:	08h	Attribute:	RO
Default Value:	See bit description	Size:	8 bits

Bit	Description
7:0	**Revision ID**—RO. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Revision ID Register.

23.2.6 CC—Class Code Register (Intel® MEI—D22:F1)

Address Offset:	09h–0Bh	Attribute:	RO
Default Value:	078000h	Size:	24 bits

Bit	Description
23:16	**Base Class Code (BCC)—**RO. Indicates the base class code of the Intel MEI device.
15:8	**Sub Class Code (SCC)**—RO. Indicates the sub class code of the Intel MEI device.
7:0	**Programming Interface (PI)—**RO. Indicates the programming interface of the Intel MEI device.

23.2.7 HTYPE—Header Type Register (Intel® MEI—D22:F1)

Address Offset:	0Eh	Attribute:	RO
Default Value:	80h	Size:	8 bits

Bit	Description
7	**Multi-Function Device** (MFD)—RO. Indicates the Intel MEI host controller is part of a multifunction device.
6:0	Header Layout (HL)—RO. Indicates that the Intel MEI uses a target device layout.

23.2.8 MEI_MBAR—MEI MMIO Base Address Register (Intel® MEI—D22:F1)

Address Offset:	10h–17h	Attribute:	R/W, RO
Default Value:	0000000000000004h	Size:	64 bits

This register allocates space for the Intel MEI memory mapped registers.

Bit	Description
63:4	**Base Address (BA)—R/W**. Software programs this field with the base address of this region.
3	**Prefetchable Memory (PM)—**RO. Indicates that this range is not pre-fetchable.
2:1	**Type (TP)**—RO. Set to 10b to indicate that this range can be mapped anywhere in 64-bit address space.
0	**Resource Type Indicator (RTE)**—RO. Indicates a request for register memory space.

23.2.9 SVID—Subsystem Vendor ID Register (Intel® MEI—D22:F1)

Address Offset:	2Ch–2Dh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:0	**Subsystem Vendor ID (SSVID)—**R/WO. Indicates the sub-system vendor identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.

Note: Register must be written as a Word write or as a DWord write with SID register.

23.2.10 SID—Subsystem ID Register (Intel® MEI—D22:F1)

Address Offset:	2Eh–2Fh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:0	**Subsystem ID (SSID)**—R/WO. Indicates the sub-system identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.

Note: Register must be written as a Word write or as a DWord write with SVID register.

23.2.11 CAPP—Capabilities List Pointer Register (Intel® MEI—D22:F1)

Address Offset:	34h	Attribute:	RO
Default Value:	50h	Size:	8 bits

Bit	Description
7:0	**Capabilities Pointer (PTR)—**RO. Indicates that the pointer for the first entry in the capabilities list is at 50h in configuration space.

23.2.12 INTR—Interrupt Information Register (Intel® MEI—D22:F1)

Address Offset: 3Ch–3Dh
Attribute: R/W, RO
Default Value: 0100h
Size: 16 bits

Bit	Description
15:8	Interrupt Pin (IPIN)—RO. TRO. This field indicates the interrupt pin the Intel MEI host controller uses. A value of 1h/2h/3h/4h indicates that this function implements legacy interrupt on INTA/INTB/INTC/INTD, respectively.
7:0	**Interrupt Line (ILINE)—**R/W. Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

23.2.13 HFS—Host Firmware Status Register (Intel® MEI—D22:F1)

Address Offset: 40h–43h
Attribute: RO
Default Value: 00000000h
Size: 32 bits

Bit	Description
31:0	**Host Firmware Status (HFS)**—RO. This register field is used by Firmware to reflect the operating environment to the host.

23.2.14 GMES—General Intel® ME Status (Intel® MEI—D22:F1)

Address Offset: 48h–4Bh
Attribute: RO
Default Value: 00000000h
Size: 32 bits

Bit	Description
31:0	**General Intel ME Status (ME_GS)**—RO. This field is populated by Intel ME.

23.2.15 H_GS—Host General Status (Intel® MEI—D22:F1)

Address Offset: 4Ch–4Fh
Attribute: RO
Default Value: 00000000h
Size: 32 bits

Bit	Description
31:0	**Host General Status(H_GS)**—RO. General Status of Host, this field is not used by Hardware

23.2.16 PID—PCI Power Management Capability ID Register (Intel® MEI—D22:F1)

Address Offset: 50h–51h
Attribute: RO
Default Value: 8C01h
Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT)—**RO. Value of 8Ch indicates the location of the next pointer.
7:0	**Capability ID (CID)—**RO. Indicates the linked list item is a PCI Power Management Register.

23.2.17 PC—PCI Power Management Capabilities Register (Intel® MEI—D22:F1)

Address Offset: 52h–53h
Default Value: C803h
Attribute: RO
Size: 16 bits

Bit	Description
15:11	**PME_Support (PSUP)**—RO. This five-bit field indicates the power states in which the function may assert PME#. Intel MEI can assert PME# from any D-state except D1 or D2 which are not supported by Intel MEI.
10	**D2_Support (D2S)**—RO. The D2 state is not supported.
9	**D1_Support (D1S)—**RO. The D1 state is not supported.
8:6	**Aux_Current (AC)**—RO. Reports the maximum Suspend well current required when in the $D3_{cold}$ state. Value of 00b is reported.
5	**Device Specific Initialization (DSI)**—RO. Indicates whether device-specific initialization is required.
4	Reserved
3	**PME Clock (PMEC)**—RO. Indicates that PCI clock is not required to generate PME#.
2:0	**Version (VS)**—RO. Hardwired to 011b to indicate support for *Revision 1.2 of the PCI Power Management Specification*.

23.2.18 PMCS—PCI Power Management Control and Status Register (Intel® MEI—D22:F1)

Address Offset: 54h–55h
Default Value: 0008h
Attribute: R/WC, R/W, RO
Size: 16 bits

Bit	Description
15	**PME Status (PMES)—**R/WC. Bit is set by Intel ME Firmware. Host software clears bit by writing '1' to bit. This bit is reset when CL_RST0# asserted.
14:9	Reserved
8	**PME Enable (PMEE)—**R/W. This bit is read/write and is under the control of host SW. It does not directly have an effect on PME events. However, this bit is shadowed so Intel ME FW can monitor it. Intel ME FW will not cause the PMES bit to transition to '1' while the PMEE bit is '0', indicating that host SW had disabled PME. This bit is reset when PLTRST# asserted.
7:4	Reserved
3	**No_Soft_Reset (NSR)**—RO. This bit indicates that when the Intel MEI host controller is transitioning from $D3_{hot}$ to D0 due to a power state command, it does not perform an internal reset. Configuration context is preserved.
2	Reserved
1:0	**Power State (PS)—**R/W. This field is used both to determine the current power state of the Intel MEI host controller and to set a new power state. The values are: 00 = D0 state (default) 11 = $D3_{hot}$ state The D1 and D2 states are not supported for the Intel MEI host controller. When in the $D3_{hot}$ state, the Intel MEI's configuration space is available, but the register memory spaces are not. Additionally, interrupts are blocked.

23.2.19 MID—Message Signaled Interrupt Identifiers Register (Intel® MEI—D22:F1)

Address Offset: 8Ch–8Dh
Default Value: 0005h
Attribute: RO
Size: 16 bits

Bit	Description
15:8	**Next Pointer (NEXT)**—RO. Value of 00h indicates that this is the last item in the list.
7:0	**Capability ID (CID)**—RO. Capabilities ID indicates MSI.

23.2.20 MC—Message Signaled Interrupt Message Control Register (Intel® MEI—D22:F1)

Address Offset: 8Eh–8Fh
Default Value: 0080h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:8	Reserved
7	**64 Bit Address Capable** (C64)—RO. Specifies that function is capable of generating 64-bit messages.
6:4	Multiple Message Enable (MME)—RO. Not implemented, hardwired to 0.
3:1	Multiple Message Capable (MMC)—RO. Not implemented, hardwired to 0.
0	**MSI Enable (MSIE)**—R/W. If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.

23.2.21 MA—Message Signaled Interrupt Message Address Register (Intel® MEI—D22:F1)

Address Offset: 90h–93h
Default Value: 00000000h
Attribute: R/W, RO
Size: 32 bits

Bit	Description
31:2	**Address (ADDR)**—R/W. Lower 32 bits of the system specified message address, always DW aligned.
1:0	Reserved

23.2.22 MUA—Message Signaled Interrupt Upper Address Register (Intel® MEI—D22:F1)

Address Offset: 94h–97h
Default Value: 00000000h
Attribute: R/W
Size: 32 bits

Bit	Description
31:0	**Upper Address (UADDR)**—R/W. Upper 32 bits of the system specified message address, always DW aligned.

23.2.23 MD—Message Signaled Interrupt Message Data Register (Intel® MEI—D22:F1)

Address Offset:	98h–99h	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15:0	**Data (DATA)**—R/W. This 16-bit field is programmed by system software if MSI is enabled. Its content is driven during the data phase of the MSI memory write transaction.

23.2.24 HIDM—Intel® MEI Interrupt Delivery Mode (Intel® MEI—D22:F1)

Address Offset:	A0h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:2	Reserved
1	**Intel MEI Interrupt Delivery Mode (HIDM)**—R/W. These bits control what type of interrupt the Intel MEI will send when ARC writes to set the M_IG bit in AUX space. They are interpreted as follows: 00 = Generate Legacy or MSI interrupt 01 = Generate SCI 10 = Generate SMI
0	**Synchronous SMI Occurrence (SSMIO)**—R/WC. This bit is used by firmware to indicate that a synchronous SMI source has been triggered. Host BIOS SMM handler can use this bit as status indication and clear it once processing is completed. A write of '1' from host SW clears this status bit. ***Note:*** It is possible that an async SMI has occurred prior to sync SMI occurrence and when the BIOS enters the SMM handler, it is possible that both bit 0 and bit 1 of this register could be set.

23.2.25 HERES—Intel® MEI Extend Register Status (Intel® MEI—D22:F1)

Address Offset:	BCh–BFh	Attribute:	RO
Default Value:	00h	Size:	32 bits

Bit	Description
31	Extend Register Valid (ERV)—RO Set by firmware after all firmware has been loaded. If ERA field is SHA-1, the result of the extend operation is in HER:5-1. If ERA field is SHA-256, the result of the extend operation is in HER:8-1.
30	Extend Feature Present (EFP)—RO This bit is hardwired to 1 to allow driver software to easily detect the chipset supports the Extend Register FW measurement feature.
29:4	Reserved
3:0	Extend Register Algorithm (ERA)—RO This field indicates the hash algorithm used in the FW measurement extend operations. Encodings are: 0h = SHA-1 2h = SHA-256 Other values = Reserved

23.2.26 HERX—Intel® MEI Extend Register DWX (Intel® MEI—D22:F1)

Address Offset:	HER1: C0h–C3h HER2: C4h–C7h HER3: C8h–CBh HER4: CCh–CFh HER5: D0h–D3h HER6: D4h–D7h HER7: D8h–DBh HER8: DCh–DFh	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	Extend Register DWX (ERDWX)—RO Xth DWORD result of the extend operation. ***Note:*** Extend Operation is HER[5:1] if using SHA-1. If using SHA-2 then Extend Operation is HER[8:1]

23.3 MEI0_MBAR—MEI0 MMIO Registers

These MMIO registers are accessible starting at the Intel MEI MMIO Base Address (MEI_MBAR) which gets programmed into D22:F0:Offset 10-17h. These registers are reset by PLTRST# unless otherwise noted.

Table 23-2. Intel® MEI MMIO Register Address Map (VE—D23:F0)

MEI_MBAR+ Offset	Mnemonic	Register Name	Default	Type
00–03h	H_CB_WW	Host Circular Buffer Write Window	00000000h	RO
04h–07h	H_CSR	Host Control Status	02000000h	R/W, R/WC, RO
08h–0Bh	ME_CB_RW	Intel ME Circular Buffer Read Window	00000000h	RO
0Ch–0Fh	ME CSR_HA	Intel ME Control Status Host Access	02000000h	RO

23.3.1 H_CB_WW—Host Circular Buffer Write Window (Intel® MEI MMIO Register)

Address Offset:	MEI0_MBAR + 00h	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	**Host Circular Buffer Write Window Field (H_CB_WWF)**—RO. This bit field is for host to write into its circular buffer. The host's circular buffer is located at the Intel ME subsystem address specified in the Host CB Base Address register. This field is write only, reads will return arbitrary data. Writes to this register will increment the H_CBWP as long as ME_RDY is 1. When ME_RDY is 0, writes to this register have no effect and are not delivered to the H_CB, nor is H_CBWP incriminated.

23.3.2 H_CSR—Host Control Status (Intel® MEI MMIO Register)

Address Offset:	MEI0_MBAR + 04h	Attribute:	RO, R/W, R/WC
Default Value:	02000000h	Size:	32 bits

Bit	Description
31:24	**Host Circular Buffer Depth (H_CBD)**—RO. This field indicates the maximum number of 32 bit entries available in the host circular buffer (H_CB). Host software uses this field along with the H_CBRP and H_CBWP fields to calculate the number of valid entries in the H_CB to read or # of entries available for write. This field is implemented with a "1-hot" scheme. Only one bit will be set to a "1" at a time. Each bit position represents the value n of a buffer depth of (2^n). For example, when bit# 1 is 1, the buffer depth is 2; when bit#2 is 1, the buffer depth is 4, etc. The allowed buffer depth values are 2, 4, 8, 16, 32, 64 and 128.
23:16	**Host CB Write Pointer (H_CBWP)**—RO. Points to next location in the H_CB for host to write the data. Software uses this field along with H_CBRP and H_CBD fields to calculate the number of valid entries in the H_CB to read or number of entries available for write.
15:8	**Host CB Read Pointer (H_CBRP)**—RO. Points to next location in the H_CB where a valid data is available for embedded controller to read. Software uses this field along with H_CBWR and H_CBD fields to calculate the number of valid entries in the host CB to read or number of entries available for write.
7:5	Reserved ***Note:*** For writes to this register, these bits shall be written as 000b.
4	**Host Reset (H_RST)**—R/W. Setting this bit to 1 will initiate a Intel MEI reset sequence to get the circular buffers into a known good state for host and Intel ME communication. When this bit transitions from 0 to 1, hardware will clear the H_RDY and ME_RDY bits.
3	**Host Ready (H_RDY)**—R/W. This bit indicates that the host is ready to process messages.
2	**Host Interrupt Generate (H_IG)**—R/W. Once message(s) are written into its CB, the host sets this bit to one for the HW to set the ME_IS bit in the ME_CSR and to generate an interrupt message to Intel ME. HW will send the interrupt message to Intel ME only if the ME_IE is enabled. HW then clears this bit to 0.
1	**Host Interrupt Status (H_IS)**—R/WC. Hardware sets this bit to 1 when ME_IG bit is set to 1. Host clears this bit to 0 by writing a 1 to this bit position. H_IE has no effect on this bit.
0	**Host Interrupt Enable (H_IE)**—R/W. Host sets this bit to 1 to enable the host interrupt (INTR# or MSI) to be asserted when H_IS is set to 1.

23.3.3 ME_CB_RW—ME Circular Buffer Read Window (Intel® MEI MMIO Register)

Address Offset:	MEI0_MBAR + 08h	Attribute:	RO
Default Value:	FFFFFFFFh	Size:	32 bits

Bit	Description
31:0	Intel ME Circular Buffer Read Window Field (ME_CB_RWF)—RO. This bit field is for host to read from the Intel ME Circular Buffer. The Intel ME's circular buffer is located at the Intel ME subsystem address specified in the Intel ME CB Base Address register. This field is read only, writes have no effect. Reads to this register will increment the ME_CBRP as long as ME_RDY is 1. When ME_RDY is 0, reads to this register have no effect, all 1s are returned, and ME_CBRP is not incremented.

23.3.4 Intel® ME CSR_HA—ME Control Status Host Access (Intel® MEI MMIO Register)

Address Offset: MEI0_MBAR + 0Ch
Default Value: 02000000h
Attribute: RO
Size: 32 bits

Bit	Description
31:24	Intel ME Circular Buffer Depth Host Read Access (ME_CBD_HRA)—RO. Host read only access to ME_CBD.
23:16	Intel ME CB Write Pointer Host Read Access (ME_CBWP_HRA)—RO. Host read only access to ME_CBWP.
15:8	Intel ME CB Read Pointer Host Read Access (ME_CBRP_HRA)—RO. Host read only access to ME_CBRP.
7:5	Reserved
4	Intel ME Reset Host Read Access (ME_RST_HRA)—RO. Host read access to ME_RST.
3	Intel ME Ready Host Read Access (ME_RDY_HRA)—RO. Host read access to ME_RDY.
2	**Intel ME Interrupt Generate Host Read Access (ME_IG_HRA)**—RO. Host read only access to ME_IG.
1	Intel ME Interrupt Status Host Read Access (ME_IS_HRA)—RO. Host read only access to ME_IS.
0	Intel ME Interrupt Enable Host Read Access (ME_IE_HRA)—RO. Host read only access to ME_IE.

23.4 MEI1_MBAR—MEI1 MMIO Registers

These MMIO registers are accessible starting at the MEI1 MMIO Base Address (MEI1_MBAR) which gets programmed into D22:F1:Offset 10–17h. These registers are reset by PLTRST# unless otherwise noted.

Table 23-3. Intel® MEI MMIO Register Address Map (VE—D23:F0)

MEI_MBAR + Offset	Mnemonic	Register Name	Default	Type
00–03h	H_CB_WW	Host Circular Buffer Write Window	00000000h	RO
04h–07h	H_CSR	Host Control Status	02000000h	R/W, R/WC, RO
08h–0Bh	ME_CB_RW	Intel ME Circular Buffer Read Window	00000000h	RO
0Ch–0Fh	Intel ME CSR_HA	Intel ME Control Status Host Access	02000000h	RO

23.4.1 H_CB_WW—Host Circular Buffer Write Window (Intel® MEI MMIO Register)

Address Offset:	MEI1_MBAR + 00h	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	Host Circular Buffer Write Window Field (H_CB_WWF)—RO. This bit field is for host to write into its circular buffer. The host's circular buffer is located at the Intel ME subsystem address specified in the Host CB Base Address register. This field is write only, reads will return arbitrary data. Writes to this register will increment the H_CBWP as long as ME_RDY is 1. When ME_RDY is 0, writes to this register have no effect and are not delivered to the H_CB, nor is H_CBWP incremented.

23.4.2 H_CSR—Host Control Status (Intel® MEI MMIO Register)

Address Offset:	MEI1_MBAR + 04h	Attribute:	RO, R/W, R/WC
Default Value:	02000000h	Size:	32 bits

Bit	Description
31:24	Host Circular Buffer Depth (H_CBD)—RO. This field indicates the maximum number of 32 bit entries available in the host circular buffer (H_CB). Host software uses this field along with the H_CBRP and H_CBWP fields to calculate the number of valid entries in the H_CB to read or # of entries available for write. ***Note:*** This field is implemented with a "1-hot" scheme. Only one bit will be set to a "1" at a time. Each bit position represents the value n of a buffer depth of (2^n). For example, when bit# 1 is 1, the buffer depth is 2; when bit#2 is 1, the buffer depth is 4, etc. The allowed buffer depth values are 2, 4, 8, 16, 32, 64 and 128.
23:16	**Host CB Write Pointer (H_CBWP)**—RO. Points to next location in the H_CB for host to write the data. Software uses this field along with H_CBRP and H_CBD fields to calculate the number of valid entries in the H_CB to read or number of entries available for write.
15:8	**Host CB Read Pointer (H_CBRP)**—RO. Points to next location in the H_CB where a valid data is available for embedded controller to read. Software uses this field along with H_CBWR and H_CBD fields to calculate the number of valid entries in the host CB to read or number of entries available for write.
7:5	Reserved ***Note:*** For writes to this register, these bits shall be written as 000b.
4	**Host Reset (H_RST)**—R/W. Setting this bit to 1 will initiate a Intel MEI reset sequence to get the circular buffers into a known good state for host and Intel ME communication. When this bit transitions from 0 to 1, hardware will clear the H_RDY and ME_RDY bits.
3	**Host Ready (H_RDY)**—R/W. This bit indicates that the host is ready to process messages.
2	**Host Interrupt Generate (H_IG)**—R/W. Once message(s) are written into its CB, the host sets this bit to one for the HW to set the ME_IS bit in the ME_CSR and to generate an interrupt message to Intel ME. HW will send the interrupt message to Intel ME only if the ME_IE is enabled. HW then clears this bit to 0.
1	**Host Interrupt Status (H_IS)**—R/WC. Hardware sets this bit to 1 when ME_IG bit is set to 1. Host clears this bit to 0 by writing a 1 to this bit position. H_IE has no effect on this bit.
0	**Host Interrupt Enable (H_IE)**—R/W. Host sets this bit to 1 to enable the host interrupt (INTR# or MSI) to be asserted when H_IS is set to 1.

23.4.3 ME_CB_RW—ME Circular Buffer Read Window (Intel® MEI MMIO Register)

Address Offset:	MEI1_MBAR + 08h	Attribute:	RO
Default Value:	FFFFFFFFh	Size:	32 bits

Bit	Description
31:0	Intel ME Circular Buffer Read Window Field (ME_CB_RWF)—RO. This bit field is for host to read from the Intel ME Circular Buffer. The Intel ME's circular buffer is located at the Intel ME subsystem address specified in the Intel ME CB Base Address register. This field is read only, writes have no effect. Reads to this register will increment the ME_CBRP as long as ME_RDY is 1. When ME_RDY is 0, reads to this register have no effect, all 1s are returned, and ME_CBRP is not incremented.

23.4.4 Intel® ME CSR_HA—ME Control Status Host Access (Intel® MEI MMIO Register)

Address Offset:	MEI1_MBAR + 0Ch	Attribute:	RO
Default Value:	02000000h	Size:	32 bits

Bit	Description
31:24	Intel ME Circular Buffer Depth Host Read Access (ME_CBD_HRA)—RO. Host read only access to ME_CBD.
23:16	Intel ME CB Write Pointer Host Read Access (ME_CBWP_HRA)—RO. Host read only access to ME_CBWP.
15:8	Intel ME CB Read Pointer Host Read Access (ME_CBRP_HRA)—RO. Host read only access to ME_CBRP.
7:5	Reserved
4	Intel ME Reset Host Read Access (ME_RST_HRA)—RO. Host read access to ME_RST.
3	Intel ME Ready Host Read Access (ME_RDY_HRA)—RO. Host read access to ME_RDY.
2	Intel ME Interrupt Generate Host Read Access (ME_IG_HRA)—RO. Host read only access to ME_IG.
1	Intel ME Interrupt Status Host Read Access (ME_IS_HRA)—RO. Host read only access to ME_IS.
0	Intel ME Interrupt Enable Host Read Access (ME_IE_HRA)—RO. Host read only access to ME_IE.

23.5 IDE Function for Remote Boot and Installations PT IDER Registers (IDER—D22:F2)

Table 23-4. IDE Function for Remote Boot and Installations PT IDER Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Attribute
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	RO, R/W
06h–07h	PCISTS	PCI Status	00B0h	RO
08h	RID	Revision ID	See register description	RO
09–0Bh	CC	Class Codes	010185h	RO
0Ch	CLS	Cache Line Size	00h	RO
10–13h	PCMDBA	Primary Command Block IO Bar	00000001h	RO, R/W
14–17h	PCTLBA	Primary Control Block Base Address	00000001h	RO, R/W
18–1Bh	SCMDBA	Secondary Command Block Base Address	00000001h	RO, R/W
1C–1Fh	SCTLBA	Secondary Control Block base Address	00000001h	RO, R/W
20–23h	LBAR	Legacy Bus Master Base Address	00000001h	RO, R/W
2Ch–2Dh	SVID	Subsystem Vendor ID	0000h	R/WO
2Eh–2Fh	SID	Subsystem ID	8086h	R/WO
34h	CAPP	Capabilities Pointer	C8h	RO
3C–3Dh	INTR	Interrupt Information	0300h	R/W, RO
C8–C9h	PID	PCI Power Management Capability ID	D001h	RO
CA–CBh	PC	PCI Power Management Capabilities	0023h	RO
CC–CFh	PMCS	PCI Power Management Control and Status	00000000h	RO, R/W, RO/V
D0–D1h	MID	Message Signaled Interrupt Capability ID	0005h	RO
D2–D3h	MC	Message Signaled Interrupt Message Control	0080h	RO, R/W
D4–D7h	MA	Message Signaled Interrupt Message Address	00000000h	R/W, RO
D8–DBh	MAU	Message Signaled Interrupt Message Upper Address	00000000h	RO, R/W
DC–DDh	MD	Message Signaled Interrupt Message Data	0000h	R/W

23.5.1 VID—Vendor Identification Register (IDER—D22:F2)

Address Offset: 00–01h
Default Value: 8086h
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Vendor ID (VID)—**RO. This is a 16-bit value assigned by Intel.

23.5.2 DID—Device Identification Register (IDER—D22:F2)

Address Offset: 02–03h
Default Value: See bit description
Attribute: RO
Size: 16 bits

Bit	Description
15:0	**Device ID (DID)**—RO. This is a 16-bit value assigned to the PCH IDER controller. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Device ID Register.

23.5.3 PCICMD—PCI Command Register (IDER—D22:F2)

Address Offset: 04–05h
Default Value: 0000h
Attribute: RO, R/W
Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable (ID)**—R/W**.** This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt **and** MSI is not enabled.
9:3	Reserved
2	**Bus Master Enable (BME)**—RO. This bit controls the PT function's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands.
1	**Memory Space Enable (MSE)**—RO. PT function does not contain target memory space.
0	**I/O Space enable (IOSE)**—RO. This bit controls access to the PT function's target I/O space.

23.5.4 PCISTS—PCI Device Status Register (IDER—D22:F2)

Address Offset: 06–07h
Attribute: RO
Default Value: 00B0h
Size: 16 bits

Bit	Description
15:11	Reserved
10:9	**DEVSEL# Timing Status (DEVT)**—RO. This bit controls the device select time for the PT function's PCI interface.
8:5	Reserved
4	**Capabilities List (CL)**—RO. This bit indicates that there is a capabilities pointer implemented in the device.
3	**Interrupt Status (IS)**—RO. This bit reflects the state of the interrupt in the function. Setting of the Interrupt Disable bit to 1 has no affect on this bit. Only when this bit is a 1 and ID bit is 0 is the INTc interrupt asserted to the Host.
2:0	Reserved

23.5.5 RID—Revision Identification Register (IDER—D22:F2)

Address Offset: 08h
Attribute: RO
Default Value: See bit description
Size: 8 bits

Bit	Description
7:0	**Revision ID**—RO. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Revision ID Register.

23.5.6 CC—Class Codes Register (IDER—D22:F2)

Address Offset: 09–0Bh
Attribute: RO
Default Value: 010185h
Size: 24 bits

Bit	Description
23:16	**Base Class Code (BCC)**—RO. This field indicates the base class code of the IDER host controller device.
15:8	**Sub Class Code (SCC)**—RO. This field indicates the sub class code of the IDER host controller device.
7:0	**Programming Interface (PI)**—RO. This field indicates the programming interface of the IDER host controller device.

23.5.7 CLS—Cache Line Size Register (IDER—D22:F2)

Address Offset: 0Ch
Attribute: RO
Default Value: 00h
Size: 8 bits

Bit	Description
7:0	**Cache Line Size (CLS)**—RO. All writes to system memory are memory writes.

23.5.8 PCMDBA—Primary Command Block IO Bar Register (IDER—D22:F2)

Address Offset: 10–13h
Default Value: 00000001h
Attribute: RO, R/W
Size: 32 bits

Bit	Description
31:16	Reserved
15:3	**Base Address (BAR)**—R/W Base Address of the BAR0 I/O space (8 consecutive I/O locations).
2:1	Reserved
0	**Resource Type Indicator (RTE)**—RO. This bit indicates a request for I/O space.

23.5.9 PCTLBA—Primary Control Block Base Address Register (IDER—D22:F2)

Address Offset: 14–17h
Default Value: 00000001h
Attribute: RO, R/W
Size: 32 bits

Bit	Description
31:16	Reserved
15:2	**Base Address (BAR)**—R/W. Base Address of the BAR1 I/O space (4 consecutive I/O locations)
1	Reserved
0	**Resource Type Indicator (RTE)**—RO. This bit indicates a request for I/O space

23.5.10 SCMDBA—Secondary Command Block Base Address Register (IDER—D22:F2)

Address Offset: 18–1Bh
Default Value: 00000001h
Attribute: RO, R/W
Size: 32 bits

Bit	Description
31:16	Reserved
15:3	**Base Address (BAR)**—R/W. Base Address of the I/O space (8 consecutive I/O locations).
2:1	Reserved
0	**Resource Type Indicator (RTE)**—RO. This bit indicates a request for I/O space.

23.5.11 SCTLBA—Secondary Control Block base Address Register (IDER—D22:F2)

Address Offset: 1C–1Fh
Default Value: 00000001h1
Attribute: RO, R/W
Size: 32 bits

Bit	Description
31:16	Reserved
15:2	**Base Address (BAR)**—R/W. Base Address of the I/O space (4 consecutive I/O locations).
1	Reserved
0	**Resource Type Indicator (RTE)**—RO. This bit indicates a request for I/O space.

23.5.12 LBAR—Legacy Bus Master Base Address Register (IDER—D22:F2)

Address Offset:	20–23h	Attribute:	RO, R/W
Default Value:	00000001h	Size:	32 bits

Bit	Description
31:16	Reserved
15:4	**Base Address (BA)**—R/W. Base Address of the I/O space (16 consecutive I/O locations).
3:1	Reserved
0	**Resource Type Indicator (RTE)**—RO. This bit indicates a request for I/O space.

23.5.13 SVID—Subsystem Vendor ID Register (IDER—D22:F2)

Address Offset:	2Ch–2Dh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:0	**Subsystem Vendor ID (SSVID)—**R/WO. Indicates the sub-system vendor identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.

Note: Register must be written as a DWord write with SID register.

23.5.14 SID—Subsystem ID Register (IDER—D22:F2)

Address Offset:	2Eh–2Fh	Attribute:	R/WO
Default Value:	8086h	Size:	16 bits

Bit	Description
15:0	**Subsystem ID (SSID)**—R/WO. Indicates the sub-system identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.

Note: Register must be written as a DWord write with SVID register.

23.5.15 CAPP—Capabilities List Pointer Register (IDER—D22:F2)

Address Offset:	34h	Attribute:	RO
Default Value:	C8h	Size:	8 bits

Bit	Description
7:0	**Capability Pointer (CP)**—R/WO. This field indicates that the first capability pointer is offset C8h (the power management capability).

23.5.16 INTR—Interrupt Information Register (IDER—D22:F2)

Address Offset: 3C–3Dh
Default Value: 0300h
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:8	**Interrupt Pin (IPIN)—**RO. A value of 1h/2h/3h/4h indicates that this function implements legacy interrupt on INTA/INTB/INTC/INTD, respectively **FunctionValueINTx** (2 IDE) 03h INTC
7:0	**Interrupt Line (ILINE)**—R/W. The value written in this register indicates which input of the system interrupt controller, the device's interrupt pin is connected to. This value is used by the OS and the device driver, and has no affect on the hardware.

23.5.17 PID—PCI Power Management Capability ID Register (IDER—D22:F2)

Address Offset: C8–C9h
Default Value: D001h
Attribute: RO
Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT)—**RO. Its value of D0h points to the MSI capability.
7:0	**Cap ID (CID)**—RO. This field indicates that this pointer is a PCI power management.

23.5.18 PC—PCI Power Management Capabilities Register (IDER—D22:F2)

Address Offset: CA–CBh
Default Value: 0023h
Attribute: RO
Size: 16 bits

Bit	Description
15:11	**PME_Support (PSUP)**—RO. This five-bit field indicates the power states in which the function may assert PME#. IDER can assert PME# from any D-state except D1 or D2 which are not supported by IDER.
10:9	Reserved
8:6	**Aux_Current (AC)**—RO. Reports the maximum Suspend well current required when in the $D3_{cold}$ state. Value of 00b is reported.
5	**Device Specific Initialization (DSI)**—RO. Indicates whether device-specific initialization is required.
4	Reserved
3	**PME Clock (PMEC)**—RO. Indicates that PCI clock is not required to generate PME#.
2:0	**Version (VS)**—RO. Hardwired to 011b to indicate support for *Revision 1.2 of the PCI Power Management Specification*.

23.5.19 PMCS—PCI Power Management Control and Status Register (IDER—D22:F2)

Address Offset:	CC–CFh	Attribute:	RO, R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:4	Reserved
3	**No Soft Reset (NSR)—**RO. 0 = Devices do perform an internal reset upon transitioning from D3hot to D0 using software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full re-initialization sequence is needed to return the device to D0 Initialized. 1 = This bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.
2	Reserved
1:0	**Power State (PS)**—R/W. This field is used both to determine the current power state of the PT function and to set a new power state. The values are: 00 = D0 state 11 = $D3_{HOT}$ state When in the $D3_{HOT}$ state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. If software attempts to write a '10' or '01' to these bits, the write will be ignored.

23.5.20 MID—Message Signaled Interrupt Capability ID Register (IDER—D22:F2)

Address Offset:	D0–D1h	Attribute:	RO
Default Value:	0005h	Size:	16 bits

Bit	Description
15:8	**Next Pointer (NEXT)—**RO. This value indicates this is the last item in the capabilities list.
7:0	**Capability ID (CID)—**RO. The Capabilities ID value indicates device is capable of generating an MSI.

23.5.21 MC—Message Signaled Interrupt Message Control Register (IDER—D22:F2)

Address Offset:	D2–D3h	Attribute:	RO, R/W
Default Value:	0080h	Size:	16 bits

Bit	Description
15:8	Reserved
7	**64 Bit Address Capable (C64)—**RO. Capable of generating 64-bit and 32-bit messages.
6:4	**Multiple Message Enable (MME)—**R/W. These bits are R/W for software compatibility, but only one message is ever sent by the PT function.
3:1	**Multiple Message Capable (MMC)—**RO. Only one message is required.
0	**MSI Enable (MSIE)—**R/W. If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.

23.5.22 MA—Message Signaled Interrupt Message Address Register (IDER—D22:F2)

Address Offset:	D4–D7h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:2	**Address (ADDR)—**R/W. This field contains the Lower 32 bits of the system specified message address, always DWord aligned
1:0	Reserved

23.5.23 MAU—Message Signaled Interrupt Message Upper Address Register (IDER—D22:F2)

Address Offset:	D8–DBh	Attribute:	RO, R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:4	Reserved
3:0	**Address (ADDR)—**R/W. This field contains the Upper 4 bits of the system specified message address.

23.5.24 MD—Message Signaled Interrupt Message Data Register (IDER—D22:F2)

Address Offset:	DC–DDh	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15:0	**Data (DATA)—**R/W. This content is driven onto the lower word of the data bus of the MSI memory write transaction.

23.6 IDE BAR0

Table 23-5. IDE BAR0 Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Attribute
0h	IDEDATA	IDE Data Register	00h	R/W
1h	IDEERD1	IDE Error Register DEV1	00h	R/W
1h	IDEERD0	IDE Error Register DEV0	00h	R/W
1h	IDEFR	IDE Features Register	00h	R/W
2h	IDESCIR	IDE Sector Count In Register	00h	R/W
2h	IDESCOR1	IDE Sector Count Out Register Device 1	00h	R/W
2h	IDESCOR0	IDE Sector Count Out Register Device 0	00h	R/W
3h	IDESNOR0	IDE Sector Number Out Register Device 0	00h	R/W
3h	IDESNOR1	IDE Sector Number Out Register Device 1	00h	R/W
3h	IDESNIR	IDE Sector Number In Register	00h	R/W
4h	IDECLIR	IDE Cylinder Low In Register	00h	R/W
4h	IDCLOR1	IDE Cylinder Low Out Register Device 1	00h	R/W
4h	IDCLOR0	IDE Cylinder Low Out Register Device 0	00h	R/W
5h	IDCHOR0	IDE Cylinder High Out Register Device 0	00h	R/W
5h	IDCHOR1	IDE Cylinder High Out Register Device 1	00h	R/W
5h	IDECHIR	IDE Cylinder High In Register	00h	R/W
6h	IDEDHIR	IDE Drive/Head In Register	00h	R/W
6h	IDDHOR1	IDE Drive Head Out Register Device 1	00h	R/W
6h	IDDHOR0	IDE Drive Head Out Register Device 0	00h	R/W
7h	IDESD0R	IDE Status Device 0 Register	80h	R/W
7h	IDESD1R	IDE Status Device 1 Register	80h	R/W
7h	IDECR	IDE Command Register	00h	R/W

23.6.1 IDEDATA—IDE Data Register (IDER—D22:F2)

Address Offset:	0h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

The IDE data interface is a special interface that is implemented in the HW. This data interface is mapped to IO space from the host and takes read and write cycles from the host targeting master or slave device.

Writes from host to this register result in the data being written to Intel ME memory.

Reads from host to this register result in the data being fetched from Intel ME memory.

Data is typically written/ read in WORDs. Intel ME-FW must enable hardware to allow it to accept Host initiated Read/ Write cycles, else the cycles are dropped.

Bit	Description
7:0	**IDE Data Register (IDEDR)—**R/W. Data Register implements the data interface for IDE. All writes and reads to this register translate into one or more corresponding write/reads to Intel ME memory

23.6.2 IDEERD1—IDE Error Register DEV1 (IDER—D22:F2)

Address Offset:	01h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register implements the Error register of the command block of the IDE function. This register is read only by the HOST interface when DEV = 1 (slave device).

Bit	Description
7:0	**IDE Error Data (IDEED)—**R/W. Drive reflects its error/ diagnostic code to the host using this register at different times.

23.6.3 IDEERD0—IDE Error Register DEV0 (IDER—D22:F2)

Address Offset:	01h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register implements the Error register of the command block of the IDE function. This register is read only by the HOST interface when DEV = 0 (master device).

Bit	Description
7:0	**IDE Error Data (IDEED)**—R/W. Drive reflects its error/ diagnostic code to the host using this register at different times.

23.6.4 IDEFR—IDE Features Register (IDER—D22:F2)

Address Offset:	01h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register implements the Feature register of the command block of the IDE function. This register can be written only by the Host.

When the HOST reads the same address, it reads the Error register of Device 0 or Device 1 depending on the device_select bit (bit 4 of the drive/head register).

Bit	Description
7:0	**IDE Feature Data (IDEFD)—**R/W. IDE drive specific data written by the Host

23.6.5 IDESCIR—IDE Sector Count In Register (IDER—D22:F2)

Address Offset:	02h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register implements the Sector Count register of the command block of the IDE function. This register can be written only by the Host. When host writes to this register, all 3 registers (IDESCIR, IDESCOR0, IDESCOR1) are updated with the written value.

A host read to this register address reads the IDE Sector Count Out Register IDESCOR0 if DEV=0 or IDESCOR1 if DEV=1

Bit	Description
7:0	**IDE Sector Count Data (IDESCD)**—R/W. Host writes the number of sectors to be read or written.

23.6.6 IDESCOR1—IDE Sector Count Out Register Device 1 Register (IDER—D22:F2)

Address Offset:	02h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register is read by the HOST interface if DEV = 1. Intel ME-Firmware writes to this register at the end of a command of the selected device.

When the host writes to this address, the IDE Sector Count In Register (IDESCIR), this register is updated.

Bit	Description
7:0	**IDE Sector Count Out Dev1 (ISCOD1)—**R/W. Sector Count register for Slave Device (that is, Device 1)

23.6.7 IDESCOR0—IDE Sector Count Out Register Device 0 Register (IDER—D22:F2)

Address Offset:	02h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register is read by the HOST interface if DEV = 0. Intel ME-Firmware writes to this register at the end of a command of the selected device.

When the host writes to this address, the IDE Sector Count In Register (IDESCIR), this register is updated.

Bit	Description
7:0	**IDE Sector Count Out Dev0 (ISCOD0)—**R/W. Sector Count register for Master Device (that is, Device 0).

23.6.8 IDESNOR0—IDE Sector Number Out Register Device 0 Register (IDER—D22:F2)

Address Offset:	03h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register is read by the Host if DEV = 0. Intel ME-Firmware writes to this register at the end of a command of the selected device.

When the host writes to the IDE Sector Number In Register (IDESNIR), this register is updated with that value.

Bit	Description
7:0	**IDE Sector Number Out DEV 0 (IDESNO0)—**R/W. Sector Number Out register for Master device.

23.6.9 IDESNOR1—IDE Sector Number Out Register Device 1 Register (IDER—D22:F2)

Address Offset:	03h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register is read by the Host if DEV = 1. Intel ME-Firmware writes to this register at the end of a command of the selected device.

When the host writes to the IDE Sector Number In Register (IDESNIR), this register is updated with that value.

Bit	Description
7:0	**IDE Sector Number Out DEV 1 (IDESNO1)—**R/W. Sector Number Out register for Slave device.

23.6.10 IDESNIR—IDE Sector Number In Register Register (IDER—D22:F2)

Address Offset:	03h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register implements the Sector Number register of the command block of the IDE function. This register can be written only by the Host. When host writes to this register, all 3 registers (IDESNIR, IDESNOR0, IDESNOR1) are updated with the written value.

Host read to this register address reads the IDE Sector Number Out Register IDESNOR0 if DEV=0 or IDESNOR1 if DEV=1.

Bit	Description
7:0	**IDE Sector Number Data (IDESND)—**R/W. This register contains the number of the first sector to be transferred.

23.6.11 IDECLIR—IDE Cylinder Low In Register Register (IDER—D22:F2)

Address Offset:	04h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register implements the Cylinder Low register of the command block of the IDE function. This register can be written only by the Host. When host writes to this register, all 3 registers (IDECLIR, IDECLOR0, IDECLOR1) are updated with the written value.

Host read to this register address reads the IDE Cylinder Low Out Register IDECLOR0 if DEV=0 or IDECLOR1 if DEV=1.

Bit	Description
7:0	**IDE Cylinder Low Data (IDECLD)—**R/W. Cylinder Low register of the command block of the IDE function.

23.6.12 IDCLOR1—IDE Cylinder Low Out Register Device 1 Register (IDER—D22:F2)

Address Offset:	04h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register is read by the Host if DEV = 1. Intel ME-Firmware writes to this register at the end of a command of the selected device. When the host writes to the IDE Cylinder Low In Register (IDECLIR), this register is updated with that value.

Bit	Description
7:0	**IDE Cylinder Low Out DEV 1. (IDECLO1)—**R/W. Cylinder Low Out Register for Slave Device.

23.6.13 IDCLOR0—IDE Cylinder Low Out Register Device 0 Register (IDER—D22:F2)

Address Offset:	04h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register is read by the Host if DEV = 0. Intel ME-Firmware writes to this register at the end of a command of the selected device. When the host writes to the IDE Cylinder Low In Register (IDECLIR), this register is updated with that value.

Bit	Description
7:0	**IDE Cylinder Low Out DEV 0. (IDECLO0)**—R/W. Cylinder Low Out Register for Master Device.

23.6.14 IDCHOR0—IDE Cylinder High Out Register Device 0 Register (IDER—D22:F2)

Address Offset:	05h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register is read by the Host if DEVice = 0. Intel ME-Firmware writes to this register at the end of a command of the selected device. When the host writes to the IDE Cylinder High In Register (IDECHIR), this register is updated with that value.

Bit	Description
7:0	**IDE Cylinder High Out DEV 0 (IDECHO0)**—R/W. Cylinder High out register for Master device.

23.6.15 IDCHOR1—IDE Cylinder High Out Register Device 1 Register (IDER—D22:F2)

Address Offset:	05h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register is read by the Host if Device = 1. Intel ME-Firmware writes to this register at the end of a command of the selected device. When the host writes to the IDE Cylinder High In Register (IDECHIR), this register is updated with that value.

Bit	Description
7:0	**IDE Cylinder High Out DEV 1 (IDECHO1)**—R/W. Cylinder High out register for Slave device.

23.6.16 IDECHIR—IDE Cylinder High In Register (IDER—D22:F2)

Address Offset:	05h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register implements the Cylinder High register of the command block of the IDE function. This register can be written only by the Host. When host writes to this register, all 3 registers (IDECHIR, IDECHOR0, IDECHOR1) are updated with the written value.

Host read to this register address reads the IDE Cylinder High Out Register IDECHOR0 if DEV=0 or IDECHOR1 if DEV=1.

Bit	Description
7:0	**IDE Cylinder High Data (IDECHD)—**R/W. Cylinder High data register for IDE command block.

23.6.17 IDEDHIR—IDE Drive/Head In Register (IDER—D22:F2)

Address Offset:	06h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register implements the Drive/Head register of the command block of the IDE. This register can be written only by the Host. When host writes to this register, all 3 registers (IDEDHIR, IDEDHOR0, IDEDHOR1) are updated with the written value.

Host read to this register address reads the IDE Drive/Head Out Register (IDEDHOR0) if DEV=0 or IDEDHOR1 if DEV=1.

Bit 4 of this register is the DEV (master/slave) bit. This bit is cleared by hardware on IDE software reset (S_RST toggles to '1') in addition to Host system reset and D3->D0 transition of the function.

Bit	Description
7:0	**IDE Drive/Head Data (IDEDHD)—**R/W. Register defines the drive number, head number and addressing mode.

23.6.18 IDDHOR1—IDE Drive Head Out Register Device 1 Register (IDER—D22:F2)

Address Offset:	06h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register is read only by the Host. Host read to this Drive/head In register address reads the IDE Drive/Head Out Register (IDEDHOR0) if DEV=1

Bit 4 of this register is the DEV (master/slave) bit. This bit is cleared by hardware on IDE software reset (S_RST toggles to '1') in addition to the Host system reset and D3 to D0 transition of the IDE function.

When the host writes to this address, it updates the value of the IDEDHIR register.

Bit	Description
7:0	**IDE Drive Head Out DEV 1 (IDEDHO1)—**R/W. Drive/Head Out register of Slave device.

23.6.19 IDDHOR0—IDE Drive Head Out Register Device 0 Register (IDER—D22:F2)

Address Offset:	06h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register is read only by the Host. Host read to this Drive/head In register address reads the IDE Drive/Head Out Register (IDEDHOR0) if DEV=0.

Bit 4 of this register is the DEV (master/slave) bit. This bit is cleared by hardware on IDE software reset (S_RST toggles to 1) in addition to the Host system reset and D3 to D0 transition of the IDE function.

When the host writes to this address, it updates the value of the IDEDHIR register.

Bit	Description
7:0	**IDE Drive Head Out DEV 0 (IDEDHO0)—**R/W. Drive/Head Out register of Master device.

23.6.20 IDESD0R—IDE Status Device 0 Register (IDER—D22:F2)

Address Offset:	07h	Attribute:	R/W
Default Value:	80h	Size:	8 bits

This register implements the status register of the Master device (DEV = 0). This register is read only by the Host. Host read of this register clears the Master device's interrupt.

When the HOST writes to the same address it writes to the command register

The bits description is for ATA mode.

Bit	Description
7	**Busy (BSY)—**R/W. This bit is set by hardware when the IDECR is being written and DEV=0, or when SRST bit is asserted by Host or host system reset or D3-to-D0 transition of the IDE function. This bit is cleared by FW write of 0.
6	**Drive Ready (DRDY)—**R/W. When set, this bit indicates drive is ready for command.
5	**Drive Fault (DF)**—R/W. Indicates Error on the drive.
4	**Drive Seek Complete (DSC)**—R/W. Indicates Heads are positioned over the desired cylinder.
3	**Data Request (DRQ)**—R/W. Set when, the drive wants to exchange data with the Host using the data register.
2	**Corrected Data (CORR)**—R/W. When set, this bit indicates a correctable read error has occurred.
1	**Index (IDX)**—R/W. This bit is set once per rotation of the medium when the index mark passes under the read/write head.
0	**Error (ERR)**—R/W. When set, this bit indicates an error occurred in the process of executing the previous command. The Error Register of the selected device contains the error information.

23.6.21 IDESD1R—IDE Status Device 1 Register (IDER—D22:F2)

Address Offset:	07h	Attribute:	R/W
Default Value:	80h	Size:	8 bits

This register implements the status register of the slave device (DEV = 1). This register is read only by the Host. Host read of this register clears the slave device's interrupt.

When the HOST writes to the same address it writes to the command register.

The bits description is for ATA mode.

Bit	Description
7	**Busy (BSY)**—R/W. This bit is set by hardware when the IDECR is being written and DEV=0, or when SRST bit is asserted by the Host or host system reset or D3-to-D0 transition of the IDE function. This bit is cleared by FW write of 0.
6	**Drive Ready (DRDY)**—R/W. When set, indicates drive is ready for command.
5	**Drive Fault (DF)**—R/W. Indicates Error on the drive.
4	**Drive Seek Complete (DSC)—R/W.** Indicates Heads are positioned over the desired cylinder.
3	**Data Request (DRQ)—R/W.** Set when the drive wants to exchange data with the Host using the data register.
2	**Corrected Data (CORR)—R/W.** When set indicates a correctable read error has occurred.
1	**Index (IDX)—R/W.** This bit is set once per rotation of the medium when the index mark passes under the read/write head.
0	**Error (ERR)—R/W.** When set, this bit indicates an error occurred in the process of executing the previous command. The Error Register of the selected device contains the error information

23.6.22 IDECR—IDE Command Register (IDER—D22:F2)

Address Offset:	07h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register implements the Command register of the command block of the IDE function. This register can be written only by the Host.

When the HOST reads the same address it reads the Status register DEV0 if DEV=0 or Status Register DEV1 if DEV=1 (Drive/Head register bit [4]).

Bit	Description
7:0	**IDE Command Data (IDECD)—R/W.** Host sends the commands (read/ write, etc.) to the drive using this register.

23.7 IDE BAR1

Address Offset	Register Symbol	Register Name	Default Value	Attribute
2h	IDDCR	IDE Device Control Register	00h	RO, WO
2h	IDASR	IDE Alternate status Register	00h	RO

23.7.1 IDDCR—IDE Device Control Register (IDER—D22:F2)

Address Offset: 2h
Attribute: WO
Default Value: 00h
Size: 8 bits

This register implements the Device Control register of the Control block of the IDE function. This register is Write only by the Host.

When the HOST reads to the same address it reads the Alternate Status register.

Bit	Description
7:3	Reserved
2	**Software reset (S_RST)—**WO. When this bit is set by the Host, it forces a reset to the device.
1	**Host interrupt Disable (nIEN)—**WO. When set, this bit disables hardware from sending interrupt to the Host.
0	Reserved

23.7.2 IDASR—IDE Alternate status Register (IDER—D22:F2)

Address Offset: 2h
Attribute: RO
Default Value: 00h
Size: 8 bits

This register implements the Alternate Status register of the Control block of the IDE function. This register is a mirror register to the status register in the command block. Reading this register by the HOST does not clear the IDE interrupt of the DEV selected device

Host read of this register when DEV=0 (Master), Host gets the mirrored data of IDESD0R register.

Host read of this register when DEV=1 (Slave), host gets the mirrored data of IDESD1R register.

Bit	Description
7:0	**IDE Alternate Status Register (IDEASR)**—RO. This field mirrors the value of the DEV0/ DEV1 status register, depending on the state of the DEV bit on Host reads.

23.8 IDE BAR4

Table 23-6. IDE BAR4 Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Attribute
0h	IDEPBMCR	IDE Primary Bus Master Command Register	00h	RO, R/W
1h	IDEPBMDS0R	IDE Primary Bus Master Device Specific 0 Register	00h	R/W
2h	IDEPBMSR	IDE Primary Bus Master Status Register	80h	RO, R/W
3h	IDEPBMDS1R	IDE Primary Bus Master Device Specific 1 Register	00h	R/W
4h	IDEPBMDTPR0	IDE Primary Bus Master Descriptor Table Pointer Register Byte 0	00h	R/W
5h	IDEPBMDTPR1	IDE Primary Bus Master Descriptor Table Pointer Register Byte 1	00h	R/W
6h	IDEPBMDTPR2	IDE Primary Bus Master Descriptor Table Pointer Register Byte 2	00h	R/W
7h	IDEPBMDTPR3	IDE Primary Bus Master Descriptor Table Pointer Register Byte 3	00h	R/W
8h	IDESBMCR	IDE Secondary Bus Master Command Register	00h	RO, R/W
9h	IDESBMDS0R	IDE Secondary Bus Master Device Specific 0 Register	00h	R/W
Ah	IDESBMSR	IDE Secondary Bus Master Status Register	00h	R/W, RO
Bh	IDESBMDS1R	IDE Secondary Bus Master Device Specific 1 Register	00h	R/W
Ch	IDESBMDTPR0	IDE Secondary Bus Master Descriptor Table Pointer Register Byte 0	00h	R/W
Dh	IDESBMDTPR1	IDE Secondary Bus Master Descriptor Table Pointer Register Byte 1	00h	R/W
Eh	IDESBMDTPR2	IDE Secondary Bus Master Descriptor Table Pointer Register Byte 2	00h	R/W
Fh	IDESBMDTPR3	IDE Secondary Bus Master Descriptor Table Pointer Register Byte 3	00h	R/W

23.8.1 IDEPBMCR—IDE Primary Bus Master Command Register (IDER—D22:F2)

Address Offset: 00h Attribute: RO, R/W
Default Value: 00h Size: 8 bits

This register implements the bus master command register of the primary channel. This register is programmed by the Host.

Bit	Description
7:4	Reserved
3	**Read Write Command (RWC)—**R/W. This bit sets the direction of bus master transfer. 0 = Reads are performed from system memory 1 = Writes are performed to System Memory. This bit should not be changed when the bus master function is active.
2:1	Reserved
0	**Start/Stop Bus Master (SSBM)—**R/W. This bit gates the bus master operation of IDE function when 0. Writing 1 enables the bus master operation. Bus master operation can be halted by writing a 0 to this bit. Operation cannot be stopped and resumed. This bit is cleared after data transfer is complete as indicated by either the BMIA bit or the INT bit of the Bus Master status register is set or both are set.

23.8.2 IDEPBMDS0R—IDE Primary Bus Master Device Specific 0 Register (IDER—D22:F2)

Address Offset: 01h Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Device Specific Data0 (DSD0)—**R/W. Device Specific

23.8.3 IDEPBMSR—IDE Primary Bus Master Status Register (IDER—D22:F2)

Address Offset: 02h Attribute: RO, R/W
Default Value: 80h Size: 8 bits

Bit	Description
7	**Simplex Only (SO)—**RO. Value indicates whether both Bus Master Channels can be operated at the same time or not. 0 = Both can be operated independently 1 = Only one can be operated at a time.
6	**Drive 1 DMA Capable (D1DC)—**R/W. This bit is read/write by the host (not write 1 clear).
5	**Drive 0 DMA Capable (D0DC)—**R/W. This bit is read/write by the host (not write 1 clear).
4:3	Reserved
2	**Interrupt (INT)—**R/W. This bit is set by the hardware when it detects a positive transition in the interrupt logic (refer to IDE host interrupt generation diagram).The hardware will clear this bit when the Host SW writes 1 to it.
1	**Error (ER)—**R/W. Bit is typically set by FW. Hardware will clear this bit when the Host SW writes 1 to it.
0	**Bus Master IDE Active (BMIA)—**RO. This bit is set by hardware when SSBM register is set to 1 by the Host. When the bus master operation ends (for the whole command) this bit is cleared by FW. This bit is not cleared when the HOST writes 1 to it.

23.8.4 IDEPBMDS1R—IDE Primary Bus Master Device Specific 1 Register (IDER—D22:F2)

Address Offset: 03h Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Device Specific Data1 (DSD1)—**R/W. Device Specific Data.

23.8.5 IDEPBMDTPR0—IDE Primary Bus Master Descriptor Table Pointer Byte 0 Register (IDER—D22:F2)

Address Offset: 04h Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Descriptor Table Pointer Byte 0 (DTPB0)**—R/W. This register implements the Byte 0 (1 of 4 bytes) of the descriptor table Pointer (four I/O byte addresses) for bus master operation of the primary channel. This register is read/write by the HOST interface.

23.8.6 IDEPBMDTPR1—IDE Primary Bus Master Descriptor Table Pointer Byte 1 Register (IDER—D22:F2)

Address Offset: 05h Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Descriptor Table Pointer Byte 1 (DTPB1)—**R/W. This register implements the Byte 1 (of four bytes) of the descriptor table Pointer (four I/O byte addresses) for bus master operation of the primary channel. This register is programmed by the Host.

23.8.7 IDEPBMDTPR2—IDE Primary Bus Master Descriptor Table Pointer Byte 2 Register (IDER—D22:F2)

Address Offset: 06h Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Descriptor Table Pointer Byte 2 (DTPB2)—**R/W. This register implements the Byte 2 (of four bytes) of the descriptor table Pointer (four I/O byte addresses) for bus master operation of the primary channel. This register is programmed by the Host.

23.8.8 IDEPBMDTPR3—IDE Primary Bus Master Descriptor Table Pointer Byte 3 Register (IDER—D22:F2)

Address Offset: 07h Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Descriptor Table Pointer Byte 3 (DTPB3)—**R/W. This register implements the Byte 3 (of four bytes) of the descriptor table Pointer (four I/O byte addresses) for bus master operation of the primary channel. This register is programmed by the Host

23.8.9 IDESBMCR—IDE Secondary Bus Master Command Register (IDER—D22:F2)

Address Offset: 08h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:4	Reserved
3	**Read Write Command (RWC)**—R/W. This bit sets the direction of bus master transfer. When 0, Reads are performed from system memory; when 1, writes are performed to System Memory. This bit should not be changed when the bus master function is active.
2:1	Reserved
0	**Start/Stop Bus Master (SSBM)**—R/W. This bit gates the bus master operation of IDE function when zero. Writing 1 enables the bus master operation. Bus master operation can be halted by writing a 0 to this bit. Operation cannot be stopped and resumed. This bit is cleared after data transfer is complete as indicated by either the BMIA bit or the INT bit of the Bus Master status register is set or both are set.

23.8.10 IDESBMDS0R—IDE Secondary Bus Master Device Specific 0 Register (IDER—D22:F2)

Address Offset: 09h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Device Specific Data0 (DSD0)**—R/W. This register implements the bus master Device Specific 1 register of the secondary channel. This register is programmed by the Host.

23.8.11 IDESBMSR—IDE Secondary Bus Master Status Register (IDER—D22:F2)

Address Offset: 0Ah
Default Value: 80h
Attribute: R/W, RO
Size: 8 bits

Bit	Description
7	**Simplex Only (SO)**—R/W. This bit indicates whether both Bus Master Channels can be operated at the same time or not. 0 = Both can be operated independently 1 = Only one can be operated at a time.
6	**Drive 1 DMA Capable (D1DC)**—R/W. This bit is read/write by the host.
5	**Drive 0 DMA Capable (D0DC)**—R/W. This bit is read/write by the host.
4:0	Reserved

23.8.12 IDESBMDS1R—IDE Secondary Bus Master Device Specific 1 Register (IDER—D22:F2)

Address Offset: 0Bh
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Device Specific Data1 (DSD1)**—R/W. This register implements the bus master Device Specific 1 register of the secondary channel. This register is programmed by the Host for device specific data if any.

23.8.13 IDESBMDTPR0—IDE Secondary Bus Master Descriptor Table Pointer Byte 0 Register (IDER—D22:F2)

Address Offset: 0Ch Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Descriptor Table Pointer Byte 0 (DTPB0)—**R/W. This register implements the Byte 0 (1 of 4 bytes) of the descriptor table Pointer (four I/O byte addresses) for bus master operation of the secondary channel. This register is read/write by the HOST interface.

23.8.14 IDESBMDTPR1—IDE Secondary Bus Master Descriptor Table Pointer Byte 1 Register (IDER—D22:F2)

Address Offset: 0Dh Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Descriptor Table Pointer Byte 1 (DTPB1)—**R/W. This register implements the Byte 1 (of four bytes) of the descriptor table Pointer (four I/O byte addresses) for bus master operation of the secondary channel. This register is programmed by the Host.

23.8.15 IDESBMDTPR2—IDE Secondary Bus Master Descriptor Table Pointer Byte 2 Register (IDER—D22:F2)

Address Offset: 0Eh Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Descriptor Table Pointer Byte 2 (DTPB2)—**R/W. This register implements the Byte 2 (of four bytes) of the descriptor table Pointer (four I/O byte addresses) for bus master operation of the secondary channel. This register is programmed by the Host.

23.8.16 IDESBMDTPR3—IDE Secondary Bus Master Descriptor Table Pointer Byte 3 Register (IDER—D22:F2)

Address Offset: 0Fh Attribute: R/W
Default Value: 00h Size: 8 bits

Bit	Description
7:0	**Descriptor Table Pointer Byte 3 (DTPB3)—**R/W. This register implements the Byte 3 (of four bytes) of the descriptor table Pointer (four I/O byte addresses) for bus master operation of the secondary channel. This register is programmed by the Host.

23.9 Serial Port for Remote Keyboard and Text (KT) Redirection (KT—D22:F3)

Table 23-7. Serial Port for Remote Keyboard and Text (KT) Redirection Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Attribute
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	See Register description	RO
04–05h	CMD	Command Register	0000h	RO, R/W
06–07h	STS	Device Status	00B0h	RO
08h	RID	Revision ID	See Register description	RO
09–0Bh	CC	Class Codes	070002h	RO
0Ch	CLS	Cache Line Size	00h	RO
10–13h	KTIBA	KT IO Block Base Address	00000001h	RO, R/W
14–17h	KTMBA	KT Memory Block Base Address	00000000h	RO, R/W
2Ch–2Dh	SVID	Subsystem Vendor ID	0000h	R/WO
2Eh–2Fh	SID	Subsystem ID	8086h	R/WO
30–33h	EROM	Expansion ROM Base Address	00000000h	RO
34h	CAP	Capabilities Pointer	C8h	RO
3C–3Dh	INTR	Interrupt Information	0200h	R/W, RO
C8–C9h	PID	PCI Power Management Capability ID	D001h	RO
CA–CBh	PC	PCI Power Management Capabilities	0023h	RO
CC–CFh	PMCS	PCI Power Management Control and Status	00000000h	RO, R/W
D0–D1h	MID	Message Signaled Interrupt Capability ID	0005h	RO
D2–D3h	MC	Message Signaled Interrupt Message Control	0080h	RO, R/W
D4–D7h	MA	Message Signaled Interrupt Message Address	00000000h	RO, R/W
D8–DBh	MAU	Message Signaled Interrupt Message Upper Address	00000000h	RO, R/W
DC–DDh	MD	Message Signaled Interrupt Message Data	0000h	R/W

23.9.1 VVID—Vendor Identification Register (KT—D22:F3)

Address Offset: 00–01h Attribute: RO
Default Value: 8086h Size: 16 bits

Bit	Description
15:0	**Vendor ID (VID)**—RO. This is a 16-bit value assigned by Intel.

23.9.2 DID—Device Identification Register (KT—D22:F3)

Address Offset: 02–03h Attribute: RO
Default Value: See bit description Size: 16 bits

Bit	Description
15:0	**Device ID (DID)**—RO. This is a 16-bit value assigned to the PCH KT controller. Refer to for the value of the Device ID Register.

23.9.3 CMD—Command Register Register (KT—D22:F3)

Address Offset: 04–05h Attribute: RO, R/W
Default Value: 0000h Size: 16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable (ID)**—R/W. This bit disables pin-based INTx# interrupts. This bit has no effect on MSI operation. 1 = Internal INTx# messages will not be generated. 0 = Internal INTx# messages are generated if there is an interrupt **and** MSI is not enabled.
9:3	Reserved
2	**Bus Master Enable (BME)**—R/W. This bit controls the KT function's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands. For KT, the only bus mastering activity is MSI generation.
1	**Memory Space Enable (MSE)**—R/W. This bit controls Access to the PT function's target memory space.
0	**I/O Space enable (IOSE)**—R/W. This bit controls access to the PT function's target I/O space.

23.9.4 STS—Device Status Register (KT—D22:F3)

Address Offset: 06–07h Attribute: RO
Default Value: 00B0h Size: 16 bits

Bit	Description
15:11	Reserved
10:9	**DEVSEL# Timing Status (DEVT)**—RO. This field controls the device select time for the PT function's PCI interface.
8:5	Reserved
4	**Capabilities List (CL)**—RO. This bit indicates that there is a capabilities pointer implemented in the device.
3	**Interrupt Status (IS)**—RO. This bit reflects the state of the interrupt in the function. Setting of the Interrupt Disable bit to 1 has no affect on this bit. Only when this bit is a 1 and ID bit is 0 is the INTB interrupt asserted to the Host.
2:0	Reserved

23.9.5 RID—Revision ID Register (KT—D22:F3)

Address Offset: 08h
Attribute: RO
Default Value: See bit description
Size: 8 bits

Bit	Description
7:0	Revision ID (RID)—RO. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Revision ID Register.

23.9.6 CC—Class Codes Register (KT—D22:F3)

Address Offset: 09–0Bh
Attribute: RO
Default Value: 070002h
Size: 24 bits

Bit	Description
23:16	**Base Class Code (BCC)**—RO This field indicates the base class code of the KT host controller device.
15:8	**Sub Class Code (SCC)**—RO This field indicates the sub class code of the KT host controller device.
7:0	**Programming Interface (PI)**—RO This field indicates the programming interface of the KT host controller device.

23.9.7 CLS—Cache Line Size Register (KT—D22:F3)

Address Offset: 0Ch
Attribute: RO
Default Value: 00h
Size: 8 bits

This register defines the system cache line size in DWORD increments. Mandatory for master which use the Memory-Write and Invalidate command.

Bit	Description
7:0	**Cache Line Size (CLS)**—RO. All writes to system memory are Memory Writes.

23.9.8 KTIBA—KT IO Block Base Address Register (KT—D22:F3)

Address Offset: 10–13h
Attribute: RO, R/W
Default Value: 00000001h
Size: 32 bits

Bit	Description
31:16	Reserved
15:3	**Base Address (BAR)**—R/W. This field provides the base address of the I/O space (8 consecutive I/O locations).
2:1	Reserved
0	**Resource Type Indicator (RTE)**—RO. This bit indicates a request for I/O space

23.9.9 KTMBA—KT Memory Block Base Address Register (KT—D22:F3)

Address Offset: 14–17h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

Bit	Description
31:12	**Base Address (BAR)**—R/W. This field provides the base address for Memory Mapped I,O BAR. Bits 31:12 correspond to address signals 31:12.
11:4	Reserved
3	**Prefetchable (PF)**—RO. This bit indicates that this range is not pre-fetchable.
2:1	**Type (TP)**—RO. This field indicates that this range can be mapped anywhere in 32-bit address space.
0	**Resource Type Indicator (RTE)**—RO. This bit indicates a request for register memory space.

23.9.10 SVID—Subsystem Vendor ID Register (KT—D22:F3)

Address Offset: 2Ch–2Dh Attribute: R/WO
Default Value: 0000h Size: 16 bits

Bit	Description
15:0	**Subsystem Vendor ID (SSVID)—**R/WO. Indicates the sub-system vendor identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.

Note: Register must be written as a DWord write with SID register.

23.9.11 SID—Subsystem ID Register (KT—D22:F3)

Address Offset: 2Eh–2Fh Attribute: R/WO
Default Value: 8086h Size: 16 bits

Bit	Description
15:0	**Subsystem ID (SSID)**—R/WO. Indicates the sub-system identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.

Note: Register must be written as a DWord write with SVID register.

23.9.12 CAP—Capabilities Pointer Register (KT—D22:F3)

Address Offset: 34h Attribute: RO
Default Value: C8h Size: 8 bits

This optional register is used to point to a linked list of new capabilities implemented by the device.

Bit	Description
7:0	**Capability Pointer (CP)**—RO. This field indicates that the first capability pointer is offset C8h (the power management capability).

23.9.13 INTR—Interrupt Information Register (KT—D22:F3)

Address Offset: 3C–3Dh Attribute: R/W, RO
Default Value: 0200h Size: 16 bits

Bit	Description
15:8	**Interrupt Pin (IPIN)**—RO. A value of 1h/2h/3h/4h indicates that this function implements legacy interrupt on INTA/INTB/INTC/INTD, respectively. **FunctionValueINTx** (3 KT/Serial Port) 02h INTB
7:0	**Interrupt Line (ILINE)**—R/W. The value written in this register tells which input of the system interrupt controller, the device's interrupt pin is connected to. This value is used by the OS and the device driver, and has no affect on the hardware.

23.9.14 PID—PCI Power Management Capability ID Register (KT—D22:F3)

Address Offset: C8–C9h Attribute: RO
Default Value: D001h Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT)**—RO. A value of D0h points to the MSI capability.
7:0	**Cap ID (CID)**—RO. This field indicates that this pointer is a PCI power management.

23.9.15 PC—PCI Power Management Capabilities ID Register (KT—D22:F3)

Address Offset: CA–CBh Attribute: RO
Default Value: 0023h Size: 16 bits

Bit	Description
15:11	**PME Support (PME)**—RO.This field indicates no PME# in the PT function.
10:6	Reserved
5	**Device Specific Initialization (DSI)**—RO. This bit indicates that no device-specific initialization is required.
4	Reserved
3	**PME Clock (PMEC)**—RO. This bit indicates that PCI clock is not required to generate PME#
2:0	**Version (VS)**—RO. This field indicates support for the *PCI Power Management Specification, Revision 1.2*.

23.9.16 MID—Message Signaled Interrupt Capability ID Register (KT—D22:F3)

Address Offset: D0–D1h Attribute: RO
Default Value: 0005h Size: 16 bits

Message Signalled Interrupt is a feature that allows the device/function to generate an interrupt to the host by performing a DWORD memory write to a system specified address with system specified data. This register is used to identify and configure an MSI capable device.

Bit	Description
15:8	**Next Pointer (NEXT)**—RO. This value indicates this is the last item in the list.
7:0	**Capability ID (CID)**—RO. This field value of Capabilities ID indicates device is capable of generating MSI.

23.9.17 MC—Message Signaled Interrupt Message Control Register (KT—D22:F3)

Address Offset: D2–D3h Attribute: RO, R/W
Default Value: 0080h Size: 16 bits

Bit	Description
15:8	Reserved
7	**64 Bit Address Capable (C64)**—RO. Capable of generating 64-bit and 32-bit messages.
6:4	**Multiple Message Enable (MME)**—R/W.These bits are R/W for software compatibility, but only one message is ever sent by the PT function.
3:1	**Multiple Message Capable (MMC)**—RO. Only one message is required.
0	**MSI Enable (MSIE)**—R/W. If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.

23.9.18 MA—Message Signaled Interrupt Message Address Register (KT—D22:F3)

Address Offset: D4–D7h Attribute: RO, R/W
Default Value: 00000000h Size: 32 bits

This register specifies the DWORD aligned address programmed by system software for sending MSI.

Bit	Description
31:2	**Address (ADDR)**—R/W. Lower 32 bits of the system specified message address, always DWord aligned.
1:0	Reserved

23.9.19 MAU—Message Signaled Interrupt Message Upper Address Register (KT—D22:F3)

Address Offset:	D8–DBh	Attribute:	RO, R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:4	Reserved
3:0	**Address (ADDR)**—R/W. Upper 4 bits of the system specified message address.

23.9.20 MD—Message Signaled Interrupt Message Data Register (KT—D22:F3)

Address Offset:	DC–DDh	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

This 16-bit field is programmed by system software if MSI is enabled

Bit	Description
15:0	**Data (DATA)**—R/W. This MSI data is driven onto the lower word of the data bus of the MSI memory write transaction.

23.10 KT IO/ Memory Mapped Device Registers

Table 23-8. KT IO/ Memory Mapped Device Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Attribute
0h	KTRxBR	KT Receive Buffer Register	00h	RO
0h	KTTHR	KT Transmit Holding Register	00h	WO
0h	KTDLLR	KT Divisor Latch LSB Register	00h	R/W
1h	KTIER	KT Interrupt Enable register	00h	R/W RO
1h	KTDLMR	KT Divisor Latch MSB Register	00h	R/W
2h	KTIIR	KT Interrupt Identification register	01h	RO
2h	KTFCR	KT FIFO Control register	00h	WO
3h	KTLCR	KT Line Control register	03h	R/W
4h	KTMCR	KT Modem Control register	00h	RO, R/W
5h	KTLSR	KT Line Status register	00h	RO
6h	KTMSR	KT Modem Status register	00h	RO

23.10.1 KTRxBR—KT Receive Buffer Register (KT—D23:F3)

Address Offset: 00h
Default Value: 00h
Attribute: RO
Size: 8 bits

This implements the KT Receiver Data register. Host access to this address, depends on the state of the DLAB bit (KTLCR[7]). It must be 0 to access the KTRxBR.

RxBR

Host reads this register when FW provides it the receive data in non-FIFO mode. In FIFO mode, host reads to this register translate into a read from Intel ME memory (RBR FIFO).

Bit	Description
7:0	**Receiver Buffer Register (RBR)**—RO. Implements the Data register of the Serial Interface. If the Host does a read, it reads from the Receive Data Buffer.

23.10.2 KTTHR—KT Transmit Holding Register (KT—D23:F3)

Address Offset:	00h	Attribute:	RO
Default Value:	00h	Size:	8 bits

This implements the KT Transmit Data register. Host access to this address, depends on the state of the DLAB bit (KTLCR[7]). It must be 0 to access the KTTHR.

THR

When host wants to transmit data in the non-FIFO mode, it writes to this register. In FIFO mode, writes by host to this address cause the data byte to be written by hardware to Intel ME memory (THR FIFO).

Bit	Description
7:0	**Transmit Holding Register (THR)**—WO. Implements the Transmit Data register of the Serial Interface. If the Host does a write, it writes to the Transmit Holding Register.

23.10.3 KTDLLR—KT Divisor Latch LSB Register (KT—D23:F3)

Address Offset:	00h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This register implements the KT DLL register. Host can Read/Write to this register only when the DLAB bit (KTLCR[7]) is 1. When this bit is 0, Host accesses the KTTHR or the KTRBR depending on Read or Write.

This is the standard Serial Port Divisor Latch register. This register is only for software compatibility and does not affect performance of the hardware.

Bit	Description
7:0	**Divisor Latch LSB (DLL)**—R/W. Implements the DLL register of the Serial Interface.

23.10.4 KTIER—KT Interrupt Enable Register (KT—D23:F3)

Address Offset:	01h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

This implements the KT Interrupt Enable register. Host access to this address, depends on the state of the DLAB bit (KTLCR[7]). It must be "0" to access this register. The bits enable specific events to interrupt the Host.

Bit	Description
7:4	Reserved
3	**MSR (IER2)**—R/W. When set, this bit enables bits in the Modem Status register to cause an interrupt to the host.
2	**LSR (IER1)**—R/W.When set, this bit enables bits in the Receiver Line Status Register to cause an Interrupt to the Host.
1	**THR (IER1)**—R/W. When set, this bit enables an interrupt to be sent to the Host when the transmit Holding register is empty.
0	**DR (IER0)**—R/W. When set, the Received Data Ready (or Receive FIFO Timeout) interrupts are enabled to be sent to Host.

23.10.5 KTDLMR—KT Divisor Latch MSB Register (KT—D23:F3)

Address Offset:	01h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Host can Read/Write to this register only when the DLAB bit (KTLCR[7]) is 1. When this bit is 0, Host accesses the KTIER.

This is the standard Serial interface's Divisor Latch register's MSB. This register is only for SW compatibility and does not affect performance of the hardware.

Bit	Description
7:0	**Divisor Latch MSB (DLM)**—R/W. Implements the Divisor Latch MSB register of the Serial Interface.

23.10.6 KTIIR—KT Interrupt Identification Register (KT—D23:F3)

Address Offset:	02h	Attribute:	RO
Default Value:	00h	Size:	8 bits

The KT IIR register prioritizes the interrupts from the function into 4 levels and records them in the IIR_STAT field of the register. When Host accesses the IIR, hardware freezes all interrupts and provides the priority to the Host. Hardware continues to monitor the interrupts but does not change its current indication until the Host read is over. Table in the Host Interrupt Generation section shows the contents.

Bit	Description
7	**FIFO Enable (FIEN1)**—RO. This bit is connected by hardware to bit 0 in the FCR register.
6	**FIFO Enable (FIEN0)**—RO. This bit is connected by hardware to bit 0 in the FCR register.
5:4	Reserved
3:1	**IIR STATUS (IIRSTS)**—RO. These bits are asserted by the hardware according to the source of the interrupt and the priority level.
0	**Interrupt Status (INTSTS)**—RO. 0 = Pending interrupt to Host 1 = No pending interrupt to Host

23.10.7 KTFCR—KT FIFO Control Register (KT—D23:F3)

Address Offset:	02h	Attribute:	WO
Default Value:	00h	Size:	8 bits

When Host writes to this address, it writes to the KTFCR. The FIFO control Register of the serial interface is used to enable the FIFOs, set the receiver FIFO trigger level and clear FIFOs under the direction of the Host.

When Host reads from this address, it reads the KTIIR.

Bit	Description
7:6	**Receiver Trigger Level (RTL)**—WO. Trigger level in bytes for the RCV FIFO. Once the trigger level number of bytes is reached, an interrupt is sent to the Host. 00 = 01 01 = 04 10 = 08 11 = 14
5:3	Reserved
2	**XMT FIFO Clear (XFIC)**—WO. When the Host writes one to this bit, the hardware will clear the XMT FIFO. This bit is self-cleared by hardware.
1	**RCV FIFO Clear (RFIC)**—WO. When the Host writes one to this bit, the hardware will clear the RCV FIFO. This bit is self-cleared by hardware.
0	**FIFO Enable (FIE)**—WO.When set, this bit indicates that the KT interface is working in FIFO node. When this bit value is changed the RCV and XMT FIFO are cleared by hardware.

23.10.8 KTLCR—KT Line Control Register (KT—D23:F3)

Address Offset:	03h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

The line control register specifies the format of the asynchronous data communications exchange and sets the DLAB bit. Most bits in this register have no affect on hardware and are only used by the FW.

Bit	Description
7	**Divisor Latch Address Bit (DLAB)**—R/W. This bit is set when the Host wants to read/write the Divisor Latch LSB and MSB Registers. This bit is cleared when the Host wants to access the Receive Buffer Register or the Transmit Holding Register or the Interrupt Enable Register.
6	**Break Control (BC)**—R/W. This bit has no affect on hardware.
5:4	**Parity Bit Mode (PBM)**—R/W. This bit has no affect on hardware.
3	**Parity Enable (PE)**—R/W.This bit has no affect on hardware.
2	**Stop Bit Select (SBS)**—R/W. This bit has no affect on hardware.
1:0	**Word Select Byte (WSB)**—R/W. This bit has no affect on hardware.

23.10.9 KTMCR—KT Modem Control Register (KT—D23:F3)

Address Offset:	04h	Attribute:	R/W
Default Value:	00h	Size:	8 bits

The Modem Control Register controls the interface with the modem. Since the FW emulates the modem, the Host communicates to the FW using this register. Register has impact on hardware when the Loopback mode is on.

Bit	Description
7:5	Reserved
4	**Loop Back Mode (LBM)**—R/W. When set by the Host, this bit indicates that the serial port is in loop Back mode. This means that the data that is transmitted by the host should be received. Helps in debug of the interface.
3	**Output 2 (OUT2)**—R/W. This bit has no affect on hardware in normal mode. In loop back mode the value of this bit is written by hardware to the Modem Status Register bit 7.
2	**Output 1 (OUT1)**—R/W. This bit has no affect on hardware in normal mode. In loop back mode the value of this bit is written by hardware to Modem Status Register bit 6.
1	**Request to Send Out (RTSO)**—R/W. This bit has no affect on hardware in normal mode. In loopback mode, the value of this bit is written by hardware to Modem Status Register bit 4.
0	**Data Terminal Ready Out (DRTO)**—R/W. This bit has no affect on hardware in normal mode. In loopback mode, the value in this bit is written by hardware to Modem Status Register Bit 5.

23.10.10 KTLSR—KT Line Status Register (KT—D23:F3)

Address Offset:	05h	Attribute:	WO
Default Value:	00h	Size:	8 bits

This register provides status information of the data transfer to the Host. Error indication, etc. are provided by the HW/FW to the host using this register.

Bit	Description
7	**RX FIFO Error (RXFER)**—RO. This bit is cleared in non FIFO mode. This bit is connected to BI bit in FIFO mode.
6	**Transmit Shift Register Empty (TEMT)**—RO. This bit is connected by HW to bit 5 (THRE) of this register.
5	**Transmit Holding Register Empty (THRE)**—RO. This bit is always set when the mode (FIFO/ Non-FIFO) is changed by the Host. This bit is active only when the THR operation is enabled by the FW. This bit has acts differently in the different modes: **Non FIFO**: This bit is cleared by hardware when the Host writes to the THR registers and set by hardware when the FW reads the THR register. **FIFO mode**: This bit is set by hardware when the THR FIFO is empty, and cleared by hardware when the THR FIFO is not empty. This bit is reset on Host system reset or D3->D0 transition.
4	**Break Interrupt (BI)**—RO. This bit is cleared by hardware when the LSR register is being read by the Host.
3:2	Reserved
1	**Overrun Error (OE):** This bit is cleared by hardware when the LSR register is being read by the Host. The FW typically sets this bit, but it is cleared by hardware when the host reads the LSR.
0	**Data Ready (DR)**—RO. **Non-FIFO Mode:** This bit is set when the FW writes to the RBR register and cleared by hardware when the RBR register is being Read by the Host. **FIFO Mode:** This bit is set by hardware when the RBR FIFO is not empty and cleared by hardware when the RBR FIFO is empty. This bit is reset on Host System Reset or D3->D0 transition.

23.10.11 KTMSR—KT Modem Status Register (KT—D23:F3)

Address Offset:	06h	Attribute:	RO
Default Value:	00h	Size:	8 bits

The functionality of the Modem is emulated by the FW. This register provides the status of the current state of the control lines from the modem.

Bit	Description
7	**Data Carrier Detect (DCD)**—RO. In Loop Back mode this bit is connected by hardware to the value of MCR bit 3.
6	**Ring Indicator (RI)**—RO. In Loop Back mode this bit is connected by hardware to the value of MCR bit 2.
5	**Data Set Ready (DSR)**—RO. In Loop Back mode this bit is connected by hardware to the value of MCR bit 0.
4	**Clear To Send (CTS)**—RO. In Loop Back mode this bit is connected by hardware to the value of MCR bit 1.
3	**Delta Data Carrier Detect (DDCD)**—RO. This bit is set when bit 7 is changed. This bit is cleared by hardware when the MSR register is being read by the HOST driver.
2	**Trailing Edge of Read Detector (TERI)**—RO. This bit is set when bit 6 is changed from 1 to 0. This bit is cleared by hardware when the MSR register is being read by the Host driver.
1	**Delta Data Set Ready (DDSR)**—RO. This bit is set when bit 5 is changed. This bit is cleared by hardware when the MSR register is being read by the Host driver.
0	**Delta Clear To Send (DCTS)**—RO. This bit is set when bit 4 is changed. This bit is cleared by hardware when the MSR register is being read by the Host driver.

§

24 PCI Express* Virtual Root Port Configuration Registers

24.1 PCI Express* Virtual Root Port Configuration Registers (PCI Express*—B0:D17:F0/Bn+1:D8:F0)

Note: Register address locations that are not shown in Table 19-1 and should be treated as Reserved.

Table 24-1. PCI Express* Virtual Root Port Configuration Registers Address MAP (PCI Express*—B0:D17:F0/Bn+1:D8:F0) (Sheet 1 of 3)

Offset	Mnemonic	Register Name	Function 0-5 Default	Type
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0010h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09–0Bh	PI	Programming Interface Register	see description	RO
0Ch	CLS	Cache Line Size	00h	R/W
0Dh	PLT	Primary Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	81h	RO
18h	PRINUM	Primary Bus Number	00h	R/W
19h	SECBUS	Secondary Bus Number	00h	R/W
1Ah	SUBBUS	Subordinate Bus Number	00h	R/W
1Chh	IOBL	I/O Base	00h	R/W, RO
1D	IOBL	I/O Limit Register	00h	R/W, RO
1Eh–1Fh	SSTS	Secondary Status Register	0000h	R/WC
20h–21h	MBL	Memory Base	0000h	R/W
22–23h	MBL	Memory Limit	0000h	R/W
24h–25h	PMBL	Prefetchable Memory Base	0001h	R/W, RO
26–27h	PMBL	Prefetchable Limit	0001h	R/W, RO
28h–2Bh	PMBU32	Prefetchable Memory Base Upper 32 Bits	00000000h	R/W
2Ch–2Fh	PMLU32	Prefetchable Memory Limit Upper 32 Bits	00000000h	R/W
34h	CAPP	Capabilities List Pointer	40h	RO
3Ch–3Dh	INTR	Interrupt Information	See bit description	R/W, RO
3Eh–3Fh	BCTRL	Bridge Control Register	0000h	R/W
40h–41h	CLIST	Capabilities List	8010	RO
42h–43h	XCAP	PCI Express* Capabilities	See Description	R/WO, RO

Table 24-1. PCI Express* Virtual Root Port Configuration Registers Address MAP (PCI Express*—B0:D17:F0/Bn+1:D8:F0) (Sheet 2 of 3)

Offset	Mnemonic	Register Name	Function 0-5 Default	Type
44h–47h	DCAP	Device Capabilities	00008001h	RO
48h–49h	DCTL	Device Control	2000h	R/W, RO
4Ah–4Bh	DSTS	Device Status	0000h	R/WC, RO
4Ch–4Fh	LCAP	Link Capabilities	See bit description	R/W, RO, R/WO
50h–51h	LCTL	Link Control	0000h	R/W, WO, RO
52h–53h	LSTS	Link Status	See bit description	RO
5C–5Dh	ROOTCTL	Root control	00000000	RO, R/W
5E–FFh	ROOTCAP	Root Capabilities	0000	RO
60–63h	ROOTSTS	Root Status	00000000	RO, R/WC
64h–67h	DCAP2	Device Capabilities 2 Register	00000016h	RO
68h–69h	DCTL2	Device Control 2 Register	0000h	R/W, RO
6A–6Bh	DEVSTS2	Device Status 2 Register	0000	RO
6C–6Dh	LINKCAP2	Link Capabilities 2 Register	000E	RO
70h–71h	L2	Link Control 2 Register	0003h	RO
72–73h	LINKSTS2	Link Status 2	0000	RO
80h–81h	PMCAP	Power Management Capability	0001	RO
82h–83h	PMC	PCI Power Management Capabilities	C803	R/W, RO
84h–85h	PMCSR	PCI Power Management Control and Status	0004	R/W, RO
86h	PMBSE	Power Management Bridge Support Extensions	00	RO
88–89h	SVCAP	Susbsytem Capability List	000D	RO
8C–8Dh	SVID	Subsystem Vendor Identification	8086	R/WO
8E–8F	SVID	Subsytem ID Register	0000	R/WO
90–91h	MSICAPLST	MSI Capability List	0005	RO
92–93h	MSICTL	MSI Message Control	0000h	RO, R/W
94–97h	MSIADDR	MSI Message Address Register	00000000	RO, R/W
98–99	MSIDATA	MIS Message Data Register	0000	R/W
100–103h	AERCAPHDR	Advanced Error Reporting Capabilities	see description	RO, R/WO
104h–107h	UES	Uncorrectable Error Status	See bit description	R/WC, RO
108h–10Bh	UEM	Uncorrectable Error Mask	00000000h	R/WO, RO
10Ch–10Fh	UEV	Uncorrectable Error Severity	See Description	RO
110h–113h	CES	Correctable Error Status	00000000h	R/WC
114h–117h	CEM	Correctable Error Mask	00000000h	RO, R/WO
118h–11Bh	AECC	Advanced Error Capabilities and Control	00000000h	RO
11C–11Fh	AEHRDLOG1	Advanced Header Log	0000h	RO
120–123h	AEHRDLOG2	Advanced Header Log	0000h	RO
124–127h	AEHRDLOG3	Advanced Header Log	0000h	RO

Table 24-1. PCI Express* Virtual Root Port Configuration Registers Address MAP (PCI Express*—B0:D17:F0/Bn+1:D8:F0) (Sheet 3 of 3)

Offset	Mnemonic	Register Name	Function 0-5 Default	Type
128–12Bh	AEHDRLOG4	Advanced Header Log	0000h	RO
12C–12Fh	ROOTERRCMD	Root Error Command Register	00000000h	RO, R/W
130–133h	ROOTERRSTS	Root Error Status	00000000	RO, R/WC
134–137h	ERRSRCID	Err Source Identification	00000000	RO
138–13Bh	ACSCAPHDER	Access Control Services Extended Capabilities	0001000D	RO
13C–13Dh	ACSCAP	Access Control Services Capability	005F	RO
13E–13Fh	ACSCAP	Access Control Services Capability	0000	RO, R/W
140h–143h	ERRUNCDETMSK	Uncorrectable Error Detect Mask	00000000h	R/WO, RO
144h–147h	ERRCORDETMSK	Correctable Error Detect Mask	00000000	R/WO, RO
148–14Bh	ROOTERRDETMSK	Root Error Detect Mask	0000E000	RO, R/WO

24.1.1 VID—Vendor Identification Register (Virtual Root Port—B0:D17:F0)

Address Offset: 00h–01h
Attribute: RO
Default Value: 8086h
Size: 16 bits

Bit	Description
15:0	**Vendor ID**—RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

24.1.2 DID—Device Identification Register (Virtual Root Port—B0:D17:F0)

Address Offset: 02h–03h
Attribute: RO
Default Value: Bit Description
Size: 16 bits

Bit	Description
15:0	**Device ID—**RO. This is a 16-bit value assigned to the PCH's PCI Express controller. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Device ID Register.

24.1.3 PCICMD—PCI Command Register (Virtual Root Port—B0:D17:F0)

Address Offset:	04h–05h	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:11	Reserved
10	**Interrupt Disable**—R/W. This bit controls the ability of the PCI-Express Function to generate legacy INTx interrupt message 0 = Internal INTx# messages are generated for PCI-Express errors detected internally in this port (for example, Malformed TLP, CRC error, completion time out etc.) or when receiving root port error messages or interrupts due to HP/PM events generated in legacy mode. 1 = Internal INTx# messages will not be generated. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set.
9	Fast Back to Back Enable (FBE)—Reserved per the *PCI Express* Base Specification*.
8	**SERR# Enable (SEE)**—R/W. 0 = Disable. 1 = this bit enables reporting of Non-Fatal and Fatal errors detected by the Function of the Root Complex. For Type 1 Configuration Space headers, this bit controls transmission by the primary interface of ERR_NONFATAL and ERR_FATAL error messages forwarded from the secondary interface. ERR_COR messages are not affected by this bit...
7	Wait Cycle Control (WCC)—Reserved per the *PCI Express Base Specification*.
6	**Parity Error Response (PER)**—R/W. 0 = Disable. 1 = This bit controls the setting of the master data parity error bit in the Status Register in response to a parity error received on the PCI Express interface.
5	VGA Palette Snoop (VPS)—Reserved per the *PCI Express* Base Specification*.
4	Postable Memory Write Enable (PMWE)—Reserved per the *PCI Express* Base Specification*.
3	Special Cycle Enable (SCE)—Reserved per the *PCI Express* Base Specification*.
2	**Bus Master Enable (BME)**—R/W. 0 = Disable. memory and I/O requests received at the root port or downstream side of a switch port (secondary side) must be handled as an Unsupported Request (UR). For Non-posted requests, a completion with UR completion status must be returned. 1 = Enable. Allows the root port or switch to forward memory and I/O read or write requests in the upstream direction.
1	**Memory Space Enable (MSE)**—R/W. 0 = Disable. The function will handle memory transactions targeting the Function as an Unsupported Request (UR). 1 = Enable. Allows memory cycles within the range specified by the memory base and limit registers can be forwarded.
0	**I/O Space Enable (IOSE)**—R/W. This bit controls access to the I/O space registers. 0 = Disable. The function will handle I/O transactions targeting the Function as an Unsupported Request (UR). 1 = Enable. Allows I/O cycles within the range specified by the I/O base and limit registers can be forwarded.

24.1.4 PCISTS—PCI Status Register (Virtual Root Port—B0:D17:F0)

Address Offset: 06h–07h
Default Value: 0010h
Attribute: R/WC, RO
Size: 16 bits

Bit	Description
15	**Detected Parity Error (DPE)—**R/WC. 0 = No parity error detected. 1 = This bit is set when a poisoned TLP is received from PCI Express. This bit is set even when the parity error response enable bit (bit[6] of the PCICMD Register) is not set. On Type 1 configuration header functions, the bit is set when the poisoned TLP is received on the primary sideSet when the...
14	**Signaled System Error (SSE)—**R/WC. 0 = No system error signaled. 1 = This bit is set when ERR_FATAL or ERR_NONFATAL messages are sent to the root complex and the SERR enable bit in the PCICMD Register is set.
13	**Received Master Abort (RMA)—**R/WC. 0 = Port has not received a completion with unsupported request status. 1 = This bit is set when the requester receives a completion with an UR completion status. On Type 1 configuration header functions, the bit is set when a UR completions status is received on the primary side.
12	**Received Target Abort (RTA)—**R/WC. 0 = Port has not received a completion with completer abort. 1 = This bit is set when a requester receives a CA completions status. On Type 1 configuration header functions, the bit is set when a "Completer Abort" is received on the primary side.
11	**Signaled Target Abort (STA)—**R/WC. 0 = No target abort received. **Signaled Target Abort (STA):** 1 = This bit is Set when the port completes a Posted or Non-Posted Request as a Completer Abort error. This applies to a Function with a Type 1 Configuration header when the Completer Abort was generated by its Primary Side.
10:9	DEVSEL# Timing Status (DEV_STS)—Reserved per the *PCI Express* Base Specification*.
8	**Master Data Parity Error Detected (DPED)**—R/WC. 0 = No data parity error received. 1 = This bit is set by a requester (primary side for type1 configuration header functions) if the parity error response enable bit (PERE) in the Command Register is set and either of the following two conditions occur: •Requester receives a completion marked poisoned. •Requester sends a poisoned request (includes writes and messages) If the parity error bit is 0b, this bit is never set.
7	Fast Back to Back Capable (FB2BC)—Reserved per the *PCI Express* Base Specification*.
6	Reserved
5	66 MHz Capable—Reserved per the *PCI Express* Base Specification*.
4	**Capabilities List**—RO. Hardwired to 1. Indicates the presence of a capabilities list.
3	**Interrupt Status**—RO. 0 = Interrupt is deasserted. 1 = this bit indicates that an INTx emulation interrupt is pending internally in this functionFor Type 1 configuration header functions, forwarded INTx messages are not reflected in this bit. unless the INTx messages is being generated from the Type 1 configuration header functioned.
2:0	Reserved

24.1.5 RID—Revision Identification Register (Virtual Root Port—B0:D17:F0,)

Offset Address:	08h	Attribute:	RO
Default Value:	See bit description	Size:	8 bits

Bit	Description
7:0	**Revision ID**—RO. Refer to the *Intel® X79 Express Chipset Specification Update* for the value of the Revision ID Register.

24.1.6 PI—Programming Interface Register (Virtual Root Port—B0:D17:F0)

Address Offset:	09h	Attribute:	RO
Default Value:	00h	Size:	24 bits

Bit	Description
23-16	**Base Class**—RO. 06h = This is a bridge device.
15:8	**SubClass Interface**—RO 04h = this device is a PCI to PCI bridge
7:0	**Programming Interface**—RO. 00h = No specific register level programming interface defined.

24.1.7 CLS—Cache Line Size Register (Virtual Root Port—B0:D17:F0)

Address Offset:	0Ch	Attribute:	R/W
Default Value:	00h	Size:	8 bits

Bit	Description
7:0	**Cache Line Size (CLS)**—R/W. This is read/write but contains no functionality, per the *PCI Express* Base Specification*.

24.1.8 PLT—Primary Latency Timer Register (Virtual Root Port—B0:D17:F0)

Address Offset:	0Dh	Attribute:	RO
Default Value:	00h	Size:	8 bits

Bit	Description
7:3	Latency Count. Reserved per the *PCI Express* Base Specification*.
2:0	Reserved

24.1.9 HEADTYP—Header Type Register (Virtual Root Port—B0:D17:F0)

Address Offset: 0Eh
Default Value: 01h
Attribute: RO
Size: 8 bits

Bit	Description
7	**Multi-Function Device**—RO. 0= Not a Multi-function device.
6:0	**Configuration Layout**—RO. These bits define the layout of addresses 10h through 3Fh in the configuration space. These bits read as 01h to indicate that the register layout conforms to the standard PCI-to-PCI Bridge layout.

24.1.10 PRIBUS—Primiary Bus Number Register (Virtual Root Port—B0:D17:F0)

Address Offset: 18h
Default Value: 00h
Attribute: R/W
Size: 24 bits

Bit	Description
7:0	**Primary Bus Number (PBN)**—R/W. These bits indicate the PCI Express bus number. Any Type 1 configuration cycle with a bus number less than this number is not accepted by this bridge (in other words, it may still match the other bridge). Indicates the bus number of the backbone.

24.1.11 SECBUS—Secondary Bus Number Register (Virtual Root Port—B0:D17:F0)

Address Offset: 19h
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Secondary Bus Number (SCBN)**—R/W. These bits indicate the bus number of the PCI device to which the secondary interface is connected. Any Type 1 configuration cycle matching this bus number is translated to a Type 0 configuration cycle and run on the PCI bus.

24.1.12 SUBBus—Subordinate Bus Number Register (Virtual Root Port—B0:D17:F0)

Address Offset: 1Ah
Default Value: 00h
Attribute: R/W
Size: 8 bits

Bit	Description
7:0	**Subordinate Bus Number (SBBN)**—R/W. These bits indicate the highest PCI bus number downstream of this bridge. Every Type 1 configuration cycle on PCI Express with a bus number greater than the secondary bus number and less than or equal to the subordinate bus number is forwarded as a Type 1 configuration cycle to the secondary PCI bus.

24.1.13 IOBL—I/O Base Register (Virtual Root Port—B0:D17:F0)

Address Offset: 1Ch
Default Value: 00h
Attribute: R/W, RO
Size: 8 bits

Bit	Description
7:4	**I/O Base Address Bits (IOBA):** These bits define the bottom address of an address range to determine when to forward I/O transactions from one interface to another. These bits correspond to address lines[15:12] for 4 KB alignment. Bits[11:0] are assumed to be 000h.
3:0	**I/O Base Addressing Capability (IOBC):** Each of these bits is hard-wired to 0, indicating support for 16-bit I/O addressing only.

24.1.14 IOBL—I/O Limit Register (Virtual Root Port—B0:D17:F0)

Address Offset: 1Dh
Default Value: 0000h
Attribute: R/W, RO
Size: 8 bits

Bit	Description
15:12	**I/O Limit Address Bits (IOLA):** These bits define the top address of an address range to determine when to forward I/O transactions from PCI Express to PCI. These bits correspond to address lines[15:12] for 4 KB aligned window. Bits[11:0] are assumed to be FFFh.
11:8	**I/O Limit Addressing Capability (IOLC):** Each of these bits is hard-wired to 0, indicating support for 16-bit I/O addressing only.

24.1.15 SSTS—Secondary Status Register (Virtual Root Port—B0:D17:F0)

Address Offset: 1Eh–1Fh
Default Value: 0000h
Attribute: R/WC
Size: 16 bits

Bit	Description
15	**Detected Parity Error (DPE)**—R/WC. 0 = No error. 1 = This bit is set by the secondary side for a Type 1 Configuration Space header function whenever it receives a Poisoned TLP, regardless of the state in the Parity Error Response Enable (PERE) field of the Bridge Control Register (BCTL)
14	**Received System Error (RSE)**—R/WC. 0 = No error. 1 = This bit is set by the secondary side for a Type 1 Configuration Space header function whenever it receives an ERR_FATAL or ERR_NONFATAL message.
13	**Received Master Abort (RMA)**—R/WC. 0 = Unsupported Request not received. 1 = This bit is set when the secondary side for Type 1 configuration space header function (for requests initiated by the Type 1 header function itself) receives a completion with Unsupported Requests Completion Status...
12	**Received Target Abort (RTA)**—R/WC. 0 = Completion Abort not received. 1 = This bit is set when the secondary side for Type 1 Configuration Space Header Function (for Requests initiated by the Type 1 header Function itself) receives a completion with Completer About Completion Status...

Bit	Description
11	**Signaled Target Abort (STA)**—R/WC. 0 = Completion Abort not sent. 1 = This bit is set when the secondary side for Type 1 configuration space header function (for requests completed by type 1 header functions itself) completes a Posted or Non-posted request as a Completer Abort error.
10:9	Secondary DEVSEL# Timing Status (SDTS): Reserved per *PCI Express* Base Specification*.
8	**Data Parity Error Detected (DPD)**—R/WC. 0 = Conditions below did not occur. 1 = This bit is set by the secondary side requester if the Parity Error Response Enable (PERE) bit in the Bridge Control Register (BCTL) is set and either of the following conditions occur • Requester receives completion marked poisoned • Requester sends a poisoned request (includes writes and messages).
7	Secondary Fast Back to Back Capable (SFBC): Reserved per *PCI Express* Base Specification*.
6	Reserved
5	Secondary 66 MHz Capable (SC66): Reserved per *PCI Express* Base Specification*.
4:0	Reserved

24.1.16 MBL—Memory Base Register (Virtual Root Port—B0:D17:F0)

Address Offset:	20h–21h	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15:4	**Memory Base (MB)**—R/W. These bits are compared with bits 31:20 of the incoming address to determine the lower 1 MB-aligned value (inclusive) of the range. The incoming address must be greater than or equal to this value.
3:0	Reserved

24.1.17 MBL—Memory Limit Register (Virtual Root Port—B0:D17:F0)

Address Offset:	22h–23h	Attribute:	R/W
Default Value:	00000000h	Size:	16 bits

Bit	Description
15:4	**Memory Limit (ML)—**R/W. These bits are compared with bits 31:20 of the incoming address to determine the upper 1 MB-aligned value (exclusive) of the range. The incoming address must be less than this value.
3:0	Reserved

24.1.18 PMBL—Prefetchable Memory Base (Virtual Root Port—B0:D17:F0)

Address Offset:	24h–25h	Attribute:	R/W, RO
Default Value:	0001h	Size:	16 bits

Bit	Description
15:4	**Prefetchable Memory Base (PMB)**—R/W. These bits are compared with bits 31:20 of the incoming address to determine the lower 1 MB-aligned value (inclusive) of the range. The incoming address must be greater than or equal to this value.
3:0	**64-bit Indicator (I64B)**—RO 0 = 32-bit Prefetchable Memory addressing. 1 = 64-bit Prefetchable Memory addressing,. This field indicates that 64-bit addressing is supported for the limit.

24.1.19 PMBL—Prefetchable Limit Register (Virtual Root Port—B0:D17:F0)

Address Offset:	26h–27h	Attribute:	R/W, RO
Default Value:	0001h	Size:	32 bits

Bit	Description
15:4	**Prefetchable Memory Limit (PML)—**R/W. These bits are compared with bits 31:20 of the incoming address to determine the upper 1 MB-aligned value (inclusive) of the range. The incoming address must be less than this value.
3:0	**64-bit Indicator (I64L)**—RO. Indicates support for 64-bit addressing

24.1.20 PMBU32—Prefetchable Memory Base Upper 32 Bits Register (Virtual Root Port—B0:D17:F0)

Address Offset:	28h–2Bh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	**Prefetchable Memory Base Upper Portion (PMBU)—**R/W. Lower 32-bits of the prefetchable address base.

24.1.21 PMLU32—Prefetchable Memory Limit Upper 32 Bits Register (Virtual Root Port—B0:D17:F0)

Address Offset:	2Ch–2Fh	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:0	**Prefetchable Memory Limit Upper Portion (PMLU)—**R/W. Upper 32-bits of the prefetchable address limit.

24.1.22 CAPP—Capabilities List Pointer Register (Virtual Root Port—B0:D17:F0)

Address Offset: 34h
Default Value: 40h
Attribute: R0
Size: 8 bits

Bit	Description
7:0	**Capabilities Pointer (PTR)—**RO. Indicates that the pointer for the first entry in the capabilities list is at 40h in configuration space.

24.1.23 INTR—Interrupt Information Register (Virtual Root Port—B0:D17:F0)

Address Offset: 3Ch–3Dh
Default Value: 0100
Function Level Reset: No (Bits 7:0 only)
Attribute: R/W, RO
Size: 16 bits

Bit	Description
15:8	**Interrupt Pin (IPIN)—**RO. This register tells which interrupt pin the function uses. 01h = Generate INTA 02h = Generate INTB 03h = Generate INTC 04h = Generate INTD Others = Reserved BIOS has the ability to write this register once during boot to setup the correct interrupt for the Function. ***Note:*** Lock Key bit is located in the Personality Lock Key Control Register.
7:0	**Interrupt Line (ILINE)—**R/W. Default = 00h. Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register. These bits are not reset by FLR.

24.1.24 BCTRL—Bridge Control Register (Virtual Root Port—B0:D17:F0)

Address Offset: 3Eh–3Fh
Default Value: 0000h
Attribute: R/W
Size: 16 bits

Bit	Description
15:12	Reserved
11	Discard Timer SERR# Enable (DTSE): Reserved per *PCI Express* Base Specification*, Revision 2.1
10	Discard Timer Status (DTS): Reserved per *PCI Express* Base Specification*, Revision 2.1.
9	Secondary Discard Timer (SDT): Reserved per *PCI Express* Base Specification*, Revision 2.1.
8	Primary Discard Timer (PDT): Reserved per *PCI Express* Base Specification*, Revision 2.1.
7	Fast Back to Back Enable (FBE): Reserved per *PCI Express* Base Specification*, Revision 2.1.

Bit	Description
6	**Secondary Bus Reset (SBR)**—R/W. Setting this bit triggers a hot reset on the downstream link for the corresponding PCIE Express port and the PCI Express hierarchy domain subordinate to the port. Software must ensure a minimum reset duration of 1us as defined in the *PCI Local Bus Specification*, Revision 3.0. Hardware will continue to maintain the hot reset state as long as the SBR bit is set. For Root Ports/switch, it is recommended that software assert this field for a minimum of 2 ms to ensure that all downstream links enters hot reset state. For a Switch, the following must cause a hot reset to be sent on all Downstream Ports: • Setting the Secondary Bus Reset bit of the Bridge Control register associated with the Upstream Port • The Data Link Layer of the Upstream Port reporting DL_Down status 30 • Receiving a hot reset on the Upstream Port A secondary bus reset will not reset any register of a Type 1 configuration space header function.
5	Master Abort Mode (MAM): Reserved per Express specification.
4	**VGA 16-Bit Decode (V16)—**R/W. This bit enables the bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of VGA alias addresses every 1 KB. This bit requires the VGA enable bit (bit 3 of this register) to be set to 1. 0 = Execute 10-bit address decode on VGA I/O accesses 1 = Execute 16-bit address decode on VGA I/O accesses
3	**VGA Enable (VE)**—R/W. The ranges below will not be claimed off the backbone by the root port. 1 = This bit modifies the response to VGA-compatible addresses. When set to 1b, the bridge positively decodes and forwards the following transactions from primary side to secondary side regardless of the value of the I/O base and limit registers. The transactions are qualified by the memory enable and I/O enable in the command register. **Memory addresses:** 000A 0000h–000B FFFFh **I/O addresses:** 3B0h–3BBh and 3C0h–3DFh in first 64 KB of I/O address space (Inclusive of ISA address aliases when IO address bits[15:10] are not decoded) The following ranges will be claimed off the backbone by the root port: • Memory ranges A0000h–BFFFFh • I/O ranges 3B0h–3BBh and 3C0h–3DFh, and all aliases of bits 15:10 in any combination of 1s
2	**ISA Enable (IE)**—R/W. This bit modifies the response by the bridge to ISA I/O addresses. This field applies only to I/O addresses that are enabled by the I/O base and I/O limit registers and are in the first 64 KB of PCI I/O space. When this bit is set, the bridge blocks all forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1 KB block (offsets 100h to 3FFh). In the opposite direction (secondary to primary), I/O transactions will be forwarded if they address the last 768B in each 1 KB block. 1 = Forward upstream ISA I/O addresses in the address range defined yb the I/O Base and I/O Limit registers that are in the firsts 64KB of PCI I/O address space (Top 768B of each 1K block). 0 = Forward downstream all I/O addresses in the address range defined by the I/O Base and I/O Limit registers.
1	**SERR# Enable (SE)**—R/W. This bit controls the forwarding of PCI Express ERR_COR, ERR_NONFATAL and ERR_FATAL messages to the primary side. 1 = Enables forwarding of ERR_COR, ERR_NONFATAL, ERR_FATAL messages. 0 = Disables forwarding of ERR_COR, ERR_NONFATAL, ERR_FATAL messages.
0	**Parity Error Response Enable (PERE)**—R/W. This bit controls the response to poisoned TLPs in the PCI Express port. 1 = Enables reporting of poisoned TLP errors. 0 = Disables reporting of poisoned TLP errors

24.1.25 CLIST—Capabilities List Register (Virtual Root Port—B0:D17:F0)

Address Offset:	40–41h	Attribute:	RO
Default Value:	8010h	Size:	16 bits

Bit	Description
15:8	**Next Capability (NEXT)—**RO. Value of 80h indicates the location of the next pointer.
7:0	**Capability ID (CID)—**RO. Indicates this is a PCI Express* capability.

24.1.26 XCAP—PCI Express* Capabilities Register (Virtual Root Port—B0:D17:F0)

Address Offset:	42h–43h	Attribute:	R/WO, RO
Default Value:	0042h or 0062h	Size:	16 bits

Bit	Description
15:14	Reserved
13:9	**Interrupt Message Number (IMN)**—RO. The PCH does not have multiple MSI interrupt numbers.
8	**Slot Implemented (SI)—**RO. Hardwired to 0 for non root ports and non DP
7:4	**Device / Port Type (DT)**—RO. 4h = Virtual Root Port
3:0	**Capability Version (CV)**—RO. Indicates PCI Express 2.0.

24.1.27 DCAP—Device Capabilities Register (Virtual Root Port—B0:D17:F0)

Address Offset:	44h–47h	Attribute:	RO
Default Value:	00008000 or 00008001h	Size:	32 bits

Bit	Description
31:28	Reserved
27:26	Captured Slot Power Limit Scale (CSPS)—RO-V. In combination with the Slot Power Limit value (bits 25:18, this field specifies the upper limit of the power supplied by slot. The power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Value field. This value is set by the Set_Slot_Power_Limit message.
25:18	Captured Slot Power Limit Value (CSPV)—RO-V. In combination with the Slot Power Limit Scale value (bits 27:26), this field specifies the upper limit of the power supplied by slot. The power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. This value is set by the Set_Slot_Power_Limit message.
17:16	Reserved
15	**Role Based Error Reporting (RBER)—**RO. Indicates that this device implements the functionality defined in the Error Reporting ECN as required by the PCI Express 1.1 specification.
14:12	Reserved
11:9	Endpoint L1 Acceptable Latency (E1AL)—RO. This field is reserved with a setting of 000b for devices other than Endpoints, per the PCI Express 1.1 specification.
8:6	Endpoint L0s Acceptable Latency (E0AL)—RO. This field is reserved with a setting of 000b for devices other than Endpoints, per the PCI Express 1.1 Specification.
5	**Extended Tag Field Supported (ETFS)**—RO. Indicates that a 5-bit tag fields are supported.
4:3	**Phantom Functions Supported (PFS)**—RO. No phantom functions supported.
2:0	**Max Payload Size Supported (MPS)**—RO. Indicates the maximum payload size VRP: 000 = 128B VSP: 001 = 256B

24.1.28 DCTL—Device Control Register (Virtual Root Port—B0:D17:F0)

Address Offset:	48h–49h	Attribute:	R/W, RO
Default Value:	2000h	Size:	16 bits

Bit	Description
15	Reserved
14:12	Max Read Request Size (MRRS)—R/W. 512 bytes is the maximum read request size.
11	Enable No Snoop (ENS)—RO. Not supported. The root port will never issue non-snoop requests.
10	**Aux Power PM Enable (APME)**—R0. Not supported, hardwired to 0.
9	Phantom Functions Enable (PFE)—RO. Not supported.
8	Extended Tag Field Enable (ETFE)—RO. Not supported.
7:5	**Max Payload Size (MPS)**—R/W. 128 bytes is the default, but 256 is also supported. No other sizes are supported.
4	Enable Relaxed Ordering (ERO)—RO. Not supported.
3	**Unsupported Request Reporting Enable (URE)**—R/W. 0 = Disable. The root port will ignore unsupported request errors. 1 = Enable. Allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	**Fatal Error Reporting Enable (FEE)**—R/W. 0 = Disable. The root port will ignore fatal errors. 1 = Enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	**Non-Fatal Error Reporting Enable (NFE)**—R/W. 0 = Disable. The root port will ignore non-fatal errors. 1 = Enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	**Correctable Error Reporting Enable (CEE)**—R/W. 0 = Disable. The root port will ignore correctable errors. 1 = Enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

24.1.29 DSTS—Device Status Register (Virtual Root Port—B0:D17:F0)

Address Offset:	4Ah–4Bh	Attribute:	R/WC, RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:6	Reserved
5	**Transactions Pending (TDP)**—RO. Functions that do not issue Non-Posted requests on their own behalf should hardwire this bit to 0b.
4	**AUX Power Detected (APD)—**RO. Auxiliary Power is not supported.
3	**Unsupported Request Detected (URD)**—R/WC. Indicates an unsupported request was detected.
2	**Fatal Error Detected (FED)**—R/WC. Indicates a fatal error was detected. 0 = Fatal has not occurred. 1 = This bit indicates that this function has detected a Fatal error. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.
1	**Non-Fatal Error Detected (NFED)**—R/WC. Indicates a non-fatal error was detected. 0 = Non-fatal has not occurred. 1 = This bit indicates that this function has detected a Non-Fatal error. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register...
0	**Correctable Error Detected (CED)**—R/WC. Indicates a correctable error was detected. 0 = Correctable has not occurred. 1 = This bit indicates that this function has detected a Correctable error. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.

24.1.30 LCAP—Link Capabilities Register (Virtual Root Port—B0:D17:F0)

Address Offset:	4Ch–4Fh	Attribute:	R/WO, RO
Default Value:	see description	Size:	32 bits

Bit	Description
31:24	**Port Number (PN)**—RO. This field indicates the PCI Express port number assigned to this link. VRP = 11h VSP = 08h
23	Reserved
22	**SPM Optionality Compliance (ASPMOPCMP):** The ASPM Optionality Compliance bit was created as a tool to set clear expectations for hardware and software interaction. This bit is Set to indicate hardware that conforms to the current specification.
21	**Link Bandwidth Notification Capability (LBNC)—**R0. Hardwired to 0
20	**Data Link Layer Active Error Reporting Capable (DLLERC)**—RO. Not supported, hardwired to 0
19	**Surprise Link Down Error Reporting Capable (SLDERC)**—RO. Hardwired to 0
18	**Clock Power Management Capable (CPMC)**—RO. Hardwired to 0
17:15	**L1 Exit Latency (EL1)—**RO. Set to 000b to indicate an exit latency of less than 1 µs.
14:12	**L0s Exit Latency (EL0)**—RO. Set to 000 to indicate an exit latency of less than 64 ns

Bit	Description
11:10	**Active State Link PM Support (APMS)**—RO. 11b Indicates both L1 and L0s supported
9:4	**Maximum Link Width (MLW)**—RO 01h indicating the maximum width is a x1.
3:0	**Maximum Link Speed (MLS)**—RO. 0001b = 2.5 Gb/s link speed is supported 0010b = 5.0 Gb/s and 2.5 Gb/s link speed supported 0011b = 8.0 Gb/s and 5.0 and 2.5 Gb/s link speed supported A 1h is reported in this field.

24.1.31 LCTL—Link Control Register (Virtual Root Port—B0:D17:F0)

Address Offset: 50h–51h
Attribute: R/W, RO
Default Value: 0000h
Size: 16 bits

Bit	Description
15:12	Reserved
11	**Link Autonomous Bandwidth Interrupt Enable (LABIE)**—RO. Hardwired to 0 as not applicable.
10	**Link Bandwidth Management Interrupt Enable (LBMIE)**—RO. Hardwired to 0 as not applicable
9	**Hardware Autonomous Width Disable** – RO. Components that do not implement the ability such as (Upstream Ports, Virtual Switch Ports) to autonomously change link width are permitted to hardwire this bit to 0b
8	Reserved
7	**Extended Synch (ES)**—R/W. 0 = Extended synch disabled. 1 = Forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0.
6	**Common Clock Configuration (CCC)—**R/W. 0 = The PCH and device are not using a common reference clock. 1 = The PCH and device are operating with a distributed common reference clock. After changing the value in this bit in bother components on a link, software must trigger the link to retrain by writing a 1b to the Retrain Link bit of the Downstream Port.
5	**Retrain Link (RL)**—RO. Hardwired to 0. For the upstream port or virtual switch port, it is read-only
4	**Link Disable (LD)**—R/W. This bit disables the link when set.
3	**Read Completion Boundary Control (RCBC)**—RO. Indicates the read completion boundary is 64 bytes.
2	Reserved
1:0	**Active State Link PM Control (APMC)**—R/W. Indicates whether the upstream port should enter L0s or L1 or both. 00 = Disabled 01 = L0s Entry Enabled 10 = L1 Entry Enabled 11 =L0s and L1 Entry Enabled

24.1.32 LSTS—Link Status Register (Virtual Root Port—B0:D17:F0)

Address Offset:	52h–53h	Attribute:	RO
Default Value:	See bit description	Size:	16 bits

Bit	Description
15	**Link Autonomous Bandwidth Status (LABS)**—RO. Not applicable, hardwired to 0
14	**Link Bandwidth Management Status (LBMS)**—RO. Hardwired to 0. This bit is not applicable and is reserved for endpoints, PCI Express-to-PCI/PCI-X bridges, and upstream ports of switches.
13	**Data Link Layer Active (DLLA)**—RO. Default value is 0b. 0 = Data Link Control and Management State Machine is not in the DL_Active state 1 = Data Link Control and Management State Machine is in the DL_Active state
12	**Slot Clock Configuration (SCC)**—RO. Set to 1b to indicate that the PCH uses the same reference clock as on the platform and does not generate its own clock.
11	**Link Training (LT)—**RO. This field is not applicable and reserved for the upstream port, end point and must be hardwired to 0b.
10	**Undefined:** hard wired to zero.
9:4	**Negotiated Link Width (NLW)**—RO. This field indicates the negotiated width of the given PCI Express* link. The contents of this NLW field is undefined if the link has not successfully trained. 00 0001b = x1 00 0010b = X2 00 0100b = x4 Only valid width is 00_0001b
3:0	**Link Speed (LS)**—RO. This field indicates the negotiated Link speed of the given PCI Express* link. Only valid value is 1h 0001b = 2.5 Gb/s PCI Express Link 0010b = 5.0 Gb/s PCI Express Link 0011b = 8.0 Gb/s PCI Express Link Others = Reserved ***Note:*** The encoding is the binary value of the bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. ***Note:*** The value in this field is undefined when the link is not up.

24.1.33 ROOTCTL—Root Control Register (Virtual Root Port—B0:D17:F0)

Address Offset:	5C–5Dh	Attribute:	RO, R/W
Default Value:	00000000h	Size:	16 bits

Bit	Description
15:5	Reserved
4	CRS Software Visibility Enable (CRSSVE)—RO. 0 = The VRP does not support CRS Enablement
3	PME Interrupt Enable (PMEIE)—R/W. 0 = Disables interrupt generation for PME messages (default) 1 = Enables interrupt generation upon receipt of PME message
2	**System Error on Fatal Error Enable (SEFEE)**—R/W. 0 = No system error should be generated on a fatal error reported by any of the devices in the hierarchy. 1 = A system error should be generated if a fatal error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with and including this PCI Express port.
1	**System Error on non-Fatal Error Enable (SENFEE)**—R/W. 0 = No system error should be generated on a non-fatal error reported by any of the devices in the hierarchy. 1 = A system error should be generated if a non-fatal error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with and including this PCI Express port.
0	**System Error on Correctable Error Enable (SECEE)**—R/W. 0 = No system error should be generated on a correctable error reported by any of the devices in the hierarchy. 1 = A system error should be generated if a correctable error (ERR_COR) is reported by any of the devices in the hierarchy associated with and including this PCI Express port.

24.1.34 ROOTCAP—Root Capabilities Register (Virtual Root Port—B0:D17:F0)

Address Offset:	5E–5Fh	Attribute:	RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:1	Reserved
0	**CRS Software Visibility (CRSSV)**—RO. This bit, when set, indicates that the root port is capable of returning Configuration Retry Status on completions to software. This port does not support this capability and is set to “0”

24.1.35 ROOTSTS—Root Status Register (Virtual Root Port—B0:D17:F0)

Address Offset: 60–63h Attribute: RO, R/W1C
Default Value: 00000000h Size: 32 bits

Bit	Description
31:18	Reserved
17	**PME Pending (PMEPEND)**—RO. This field indicates that another PME is pending when the PME status bit is set. When the PME status bit is cleared by software, the pending PME is delivered by hardware by setting the PME status bit again and updating the Requester ID appropriately. The PME pending bit is cleared by hardware if no more PMEs are pending. The root port can handle two outstanding PM_PME messages in it's internal queues of the power management controller per port.
16	**PME Status (PMESTS)**—R/WC. When set, this bit indicates that a PME was asserted by a requester as indicated by the PMEREQID field. This bit is cleared by writing a "1" to it. Subsequent PMEs are kept pending until the PME Status is cleared.
15;0	**PME Requester ID (PMERID)**—RO. This field indicates the PCI Requester ID of the last PME requestor.

24.1.36 DCAP2—Device Capabilities 2 Register (Virtual Root Port—B0:D17:F0)

Address Offset: 64h–67h Attribute: RO
Default Value: 00000020h Size: 32 bits

Bit	Description
31:5	Reserved
19:18	**OBFF Supported (OBFFS)**—RO. 00b = OBFF Not Supported Applicable only to Root Ports, Switch Ports, and Endpoints that support this capability. Must be 00b for other function types.
17:14	Reserved
13:12	**TPH Completer Supported (TPHCS)**—RO. Applicable only to Root Ports and Endpoints. Must be 00b for other function types
11	**LTBWR Mechanism Supported (LTBWRMS)**—RO. his bit must be hardwired to 0b for function that do not implement this capability.
10	**No RO-enabled PR-PR Passing (NROEPRPASS)**—RO Hardwiired to 0b. This bit applies only for Switches and RCs that support peer-to-peer traffic between ports
9	**AD128 CAS Completer Supported (AD128ACS)**—RO. hardwired to 0b
8	**AD64-bit AtomicOp Completer Supported (AD64ACS)**—RO. Hardwired to 0b
7	**AD32 bit AtomicOp Completer Supported (AD32ACS)**—RO Hardwired to 0b
6	**AtomicOp Routing Supported (ARS)**—R/WO. Default is 0b
5	**Alternative RID Interpretation Capable (ARI)**—RO. This bit is set to 1b indicating that the downstream port supports this capability.
4	**Completion Timeout Disable Supported (CTDS)—**RO. Hardwired to 0.
3:0	**Completion Timeout Ranges Supported (CTRS)—**RO. Hardwired to 0000b

24.1.37 DCTL2—Device Control 2 Register (Virtual Root Port—B0:D17:F0)

Address Offset:	68h–69h	Attribute:	RO, R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15	Reserved
14:13	**OBFF Enable (OBFFE)**—RO. Hardwired to 00b
12;11	Reserved
10	**LTBWR Mechanism Enable (LTBWRME)**—RO. Not supported so hardwired to 0b
9	**IDO Completion Enable (IDOCE)**—RO. Hardwired to 0b. Applicable only to Endpoints including RC integrated Endpoints and Root Ports.
8	**IDO Request Enable (IDORE)**—RO. Hardwired to 0b. Applicable only to Endpoints including RC integrated Endpoints and Root Ports.
7	**AtomicOp Egress Blocking (AEB)**—R/W 0 = AtomicOp requests that target this out going Egress port are permitted 1 = AtomicOp requests that target this out going Egress port must be blocked.
6	**AtomicOp Requester Enable (ARE)**—RO. Applicable only to Endpoints and Root Ports; must be hardwired to 0b for other Function types.
5	**Alternative RID Interpretation Enable (ARIE)**—R/W. When set to 1b, ARI is enabled for the downstream port or root ports.
4	**Completion Timeout Disable (CTD)—**RO. Hardwired to 0b. 1 = Disable the completions timeout mechanism for all NP transactions. 0 = Completion timeout is enabled for all NP transactions.
3:0	**Completion Timeout Value (CTV)—**R0. Hardwired to 0000b.

24.1.38 DEVSTS2—Device Status 2 Register (Virtual Root Port—B0:D17:F0)

Address Offset:	6Ah–6Bh	Attribute:	RO
Default Value:	0000h	Size:	16 bits

Bit	Description
15:0	Reserved

24.1.39 LINKCAP2—Link Capabilities 2 Register (Virtual Root Port—B0:D17:F0)

Address Offset:	6Ch–6Ch	Attribute:	RO
Default Value:	0002h	Size:	16 bits

Bit	Description
15:8	Reserved. Hardwired to 00h
7:1	**Supported Link Speeds Vector (SLNKSPV)—RO.** Hardwired to 01h This field indicates the supported Link speed(s) of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. Bit definitions are: 0000001 = 2.5 GT/s 0000011 = 5.0 GT/s and 2.5 GT/s 0000111 = 8.0 GT/s and 5.0 GT/s and 2.5 GT/s Others = Reserved
0	Reserved. Hardwired to 0b

24.1.40 L2—Link Control 2 Register (Virtual Root Port—B0:D17:F0)

Address Offset:	70h–71h	Attribute:	RO, RWS
Default Value:	0001h	Size:	16 bits

Bit	Description
15:13	Reserved. Hardwired to 00b
12	**Compliance De-emphasis (CD)**—RO. This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit (EC) (bit 4) in this register being 1b. 1 = -3.5 dB 0 = -6 dB When the link is operating at 2.5 Gb/s, the setting of this bit has no effect. Only cleared to default with a power good reset
11	**Compliance SOS (CSOS)**—RO. Set to 0b
10	**Enter Modified Compliance (EMC)**—RO. Set to 0b
9:7	**Transmit Margin (TM)**—RO. Set to 000b
6	**Selectable De-emphasis (SD)**—RO. Hardwired to 0b This bit is not applicable and reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and upstream ports of switches.
5	**Hardware Autonomous Speed Disable (HASD)**—RO. Set to 0b
4	**Enter Compliance (EC)**—RO. Set to 0b
3:0	**Target Link Speed (TLS)**—RO. Set to 0001b. 0001b = 2.5 Gb/s Target Link Speed 0010b = 5.0 Gb/s Target Link Speed 0011b = 8.0 Gb/s Target Link Speed

24.1.41 LINKSTS2—Link STatus2 Register (Virtual Root Port—B0:D17:F0)

Address Offset: 72h–73h
Attribute: RO
Default Value: 0000h
Size: 16 bits

Bit	Description
15:1	Reserved
0	**Current De-emphasis Level (CDL)**—RO. When the link is operating at 5 Gb/s speed, this bit reflects the level of de-emphasis. 1 = -3.5 dB 0 = -6dB

24.1.42 PMCAP—Power Management Capability Register (Virtual Root Port—B0:D17:F0)

Address Offset: 80h–81h
Attribute: RO
Default Value: 0001h
Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT)**—RO. Indicates this is the last item in the list.
7:0	**Capability Identifier (CID)**—RO. Value of 01h indicates this is a PCI power management capability.

24.1.43 PMC—PCI Power Management Capabilities Register (Virtual Root Port—B0:D17:F0)

Address Offset: 82h–83h
Attribute: RO
Default Value: C803h
Size: 16 bits

Bit	Description
15:11	**PME_Support (PMES)**—RO. Indicates PME# is supported for states D0, $D3_{HOT}$ and $D3_{COLD}$...
10	D2_Support (D2S)—RO. The D2 state is not supported.
9	D1_Support (D1S)—RO The D1 state is not supported.
8:6	**Aux_Current (AC)**—RO. Aux current is not supported
5	**Device Specific Initialization (DSI)**—RO. Device-specific initialization is not required when transitioning to D0 from D3hot state. This bit is zero.
4	Reserved
3	**PME Clock (PMEC)—**RO. Does not apply to PCI Express. Hard-wired to 0.
2:0	**Version (VS)**—RO. Indicates support for *Revision 1.2 of the PCI Power Management Specification*.

24.1.44 PMCSR—PCI Power Management Control and Status Register (Virtual Root Port—B0:D17:F0)

Address Offset:	84h–85h	Attribute:	R/W, RO
Default Value:	0004h	Size:	16 bits

Bit	Description
15	**PME Status (PMES)—**R/WC. 0 = Indicates no PME received from downstream link 1 = Indicates a PME was received on the downstream link.
14:13	**Data Scale (DC)**—RO. Not supported. Hardwired to 0
12:9	**Data Select (DS)**—RO. Not supported, hardwired to 0
8	**PME Enable (PMEE)—**RWS. 0 = PME messages are gated and PME messages are not generated 1 = PME messages are enabled
7:4	Reserved
3	**No Soft Reset (NSR)**—RW-L. This bit when 1b indicates that a device transitioning from D3hot to D0 does not perform an internal reset. The configuration context is preserved.
2	Reserved
1:0	**Power State (PS)—**R/W. This field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the supported values is given below: 0h = D0 3h = D3hot If software attempts to write an unsupported, optional state to this field, the write operation must complete normally; however, the data is discarded and no state change occurs.

24.1.45 PMBSE—Power Management Bridge Support Extensions Register (Virtual Root Port—B0:D17:F0)

Address Offset:	86h	Attribute:	RO
Default Value:	00h	Size:	0 bits

Bit	Description
7	**Bus Power/Clock Control Enable (BPCC_EN)**—RO. Neither bus or clock control of PCI is supported when in D3hot state. This bit is hardwired to 0.
6	**B2/B3# (B23EN)**—RO. Not supported. This bit has no meaning since the BPCC_En bit is hardwired to 0.
5:0	**Reserved**

24.1.46 SVCAP—Subsystem Capability List Register (Virtual Root Port—B0:D17:F0)

Address Offset: 88h–89h
Attribute: RO
Default Value: 900Dh
Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT)**—RO. Contains the offset of the next item in the capabilities list
7:0	**Capability Identifier (CID)**—RO. Identifies the function as Subsystem Identification capable.

24.1.47 SVID—Subsystem Vendor ID Register (Virtual Root Port—B0:D17:F0)

Address Offset: 8Ch–8Dh
Attribute: R/WO
Default Value: 8086h
Size: 16 bits

Bit	Description
15:0	**Subsystem Vendor Identifier (SVID)**—R/WO. Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

24.1.48 SVID—Subsystem ID Register (Virtual Root Port—B0:D17:F0)

Address Offset: 8Eh–8Fh
Attribute: R/WO
Default Value: 0000h
Size: 16 bits

Bit	Description
15:00	**Subsystem Identifier (SID)**—R/WO. Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

24.1.49 MSICAPLST—MSI Capability List Register (Virtual Root Port—B0:D17:F0)

Address Offset: 88h–89h
Attribute: RO
Default Value: 0005h
Size: 16 bits

Bit	Description
15:8	**Next Capability (NEXT)**—RO. Contains the offset of the next item in the capabilities list. A null value is used to indicate that this is the last capability
7:0	**Capability Identifier (CID)**—RO. Identifies the function as MSI capable.

24.1.50 MSICTL—MSI Message Control Register (Virtual Root Port—B0:D17:F0)

Address Offset: 92h
Attribute: RO, R/W
Default Value: 0000h
Size: 16 bits

Bit	Description
15:8	Reserved
7	**Address 64-bit Capable (AD64C)**—RO. 0b means the function is not capable of 64 bit message addresses
6:4	**Multiple Message Enable (MMEN)**—R/W. Only one message is supported. These bits are R/W for software compatibility.
3:1	**Multiple Message Capable (MMC)**—RO. Only one message is supported so these bits are wired 000b
0	MSI Enable (MSIE)—R/W. When set, MSI is enabled and traditional pins are not used to generate interrupts.

24.1.51 MSIADDR—MSI Message Address Register (Virtual Root Port—B0:D17:F0)

Address Offset: 94h
Attribute: RO, R/W
Default Value: 00000000h
Size: 32 bits

Bit	Description
31:2	**Address**—R/W. Message address specified by the system, always DWORD aligned
1:0	Reserved

24.1.52 MSIDATA—MSI Message Data Register (Virtual Root Port—B0:D17:F0)

Address Offset: 98h
Attribute: R/W
Default Value: 0000h
Size: 16 bits

Bit	Description
15:0	DATA—R/W. This 16 bit field is programmed by system software when MSI is enabled. The content is driven on the lower work of the MSI Memory write transaction.

24.1.53 AERCAPHDR—Advanced Error Reporting Capabilities Header (Virtual Root Port—B0:D17:F0)

Address Offset:	100–103h	Attribute:	RO, R/WO
Default Value:	13810001h	Size:	16 bits

Bit	Description
31:20	**Next Capability Offset (NCO)**—RW-L. Contains the offset of the next structure in the Extended Capabilities list for endpoint.
19i:16	**Capability Version (CV)**—RO. Indicates the version of the Capability structure present.
15:0	**Extended Capability ID (EXCAPID)**—RO. Identifies the function as Advanced Error Reporting capable.

24.1.54 UES—Uncorrectable Error Status Register (Virtual Root Port—B0:D17:F0)

Address Offset:	104h–107h	Attribute:	R/WC, RO
Default Value:	00000000h	Size:	32 bits

This register maintains its state through a platform reset. It loses its state upon suspend.

Bit	Description
31:25	**Reserved.** Hardwired to 0
24	**Atomic Egress Blocked Error (AEBE)**—R/WC. Default 0b. This bit is set whenever an Atomic OP TLP is blocked on any egress port
23	**MC Blocked TLP Error (MCE)**—RO. Not supported, set to 0b
22	**Uncorrectable Internal Error (UIE)**—R/WC. Default 0b This bit is set whenever an uncorrectable internal error is detected.
21	**ACS Violation Error (ACSE)**—R/WC. Default = 0b This bit is set whenever an ACS violation is detected by the PCI Express port.
20	**Unsupported Request Error Status (URE)**—R/WC. Default 0b. Indicates an unsupported request was received.
19	ECRC Error Status (EE)—RO. ECRC is not supported.
18	**Malformed TLP Status (MT)**—R/WC. Default 0b. Indicates a malformed TLP was received.
17	**Receiver Overflow Status (RO)**—R/WC. Default 0b. Indicates a receiver overflow occurred.
16	**Unexpected Completion Status (UC)**—R/WC. Default 0b. This bit is set whenever a completion is received with a requestor ID that does not match side A or side B, or when a completion is received with a matching requestor ID but an unexpected tag field. Header logging is performed.
15	**Completion Abort Status (CA)**—R/WC. Default 0b. The bridge sets this bit and logs the header associated with the request when the configuration unit signals a completer abort.
14	**Completion Timeout Status (CT)**—RO. Not supported, set to 0b
13	**Flow Control Error (FCE)**—R/WC. Default 0b. This bit is set when a flow control protocol error is detected.
12	**Poisoned TLP Error (PTLPE)**—R/WC. Default 0b. This bit is set and the bridge logs the header when a poisoned TLP is received from PCI Express.
11:6	**Reserved** Software must write 0 to these bits
5	**Surprise Link Down Error (SLDE)**—R/WC. Default 0b. This bit is set when a surprise link down error is detected.
4	**Data Link Protocol Error Status (DLPE)**—R/WC. Indicates a data link protocol error occurred.
3:0	**Reserved** Set to 0h

24.1.55 UEM—Uncorrectable Error Mask (Virtual Root Port—B0:D17:F0)

Address Offset:	108h–10Bh	Attribute:	RWS, RO
Default Value:	00000000h	Size:	32 bits

When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled.

Bit	Description
31:25	**Reserved**
24	**AtomicOp Egress Blocked Error Mask (AEBEM)**—RWS.
23	**MC Blocked TLP Error Mask (MCEM)**—RO.
22	**Uncorrectable Internal Error Mask (UIEM)**—RWS.
21	**ACS Violation Error Mask (ACSEM)**—RWS.
20	**Unsupported Request Error Mask (URE)**—RWS.
19	**ECRC Error Mask (EE)**—RO. ECRC is not supported.
18	**Malformed TLP Mask (MT)**—RWS.
17	**Receiver Overflow Mask (RO)**—RWS.
16	**Unexpected Completion Mask (UC)**—RWS.
15	**Completion Abort Mask (CA)**—RWS.
14	**Completion Timeout Mask (CT)**—RO Hardwired to 0
13	**Flow Control Protocol Error Mask (FCPE)—**RWS.
12	**Poisoned TLP Mask (PT)**—RWS.
11:6	Reserved
5	**Surprise Link Down Error Mask (SLDEM)**—RWS.
4	**Data Link Protocol Error Mask (DLPE)**—RWS.
3:0	Reserved

24.1.56 UEV—Uncorrectable Error Severity (Virtual Root Port—B0:D17:F0)

Address Offset:	10Ch–10Fh	Attribute:	RO, R/W
Default Value:	00462030h	Size:	32 bits

Bit	Description
31:25	Reserved
24	**AtomicOp Egress Blocked Severity (AEBES):** 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
23	**MC Blocked TLP Error Severity (MCES)**—RO. Hardwired to 0b
22	**Uncorrectable Internal Error Severity (UIES):** 0 = Error considered non-fatal. 1 = Error is fatal.(default)
21	**ACS Violation Error Severity (ACSES)**—RO 0 = Error considered non-fatal. (default) 1 = Error is fatal.
20	**Unsupported Request Error Severity (URE)** 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
19	**ECRC Error Severity (EE)**—RO. ECRC is not supported.
18	**Malformed TLP Severity (MT)**—R/W. 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
17	**Receiver Overflow Severity (RO)**—R/W. 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
16	**Unexpected Completion Error Severity (UCES):** 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
15	**Completion Abort Severity (CA)—**R/W. 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
14	**Completion Timeout Error Severity (CTES)**—RO. Hardwired to 0b
13	**Flow Control Protocol Error Severity (FCPE)** 0 = Error considered non-fatal. 1 = Error is fatal (Default).
12	**Poisoned TLP Severity (PT)**—R/W. 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
11:6	Reserved
5	**Surprise Link Down Severity (SLDES)**: 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
4	**Data Link Protocol Error Severity (DLPE)**—R/W. 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
3:0	Reserved

24.1.57 CES—Correctable Error Status Register (Virtual Root Port—B0:D17:F0)

Address Offset: 110h–113h Attribute: R/WC
Default Value: 00000000h Size: 32 bits

Bit	Description
31:16	Reserved
15	**Header Log Overflow Error (HLOE)—**R/WC. Indicates a Header Log Overflow occurred
14	**Correctable Internal Error (CIE)—**R/WC. Indicates a correctable Internal Error occurred
13	**Advisory Non-Fatal Error Status (ANFES)—**R/WC. 0 = Advisory Non-Fatal Error did not occur. 1 = Advisory Non-Fatal Error did occur.
12	**Replay Timer Timeout Status (RTT)**—R/WC. Indicates the replay timer timed out.
11:9	Reserved
8	**Replay Number Rollover Status (RNR)—**R/WC. Indicates the replay number rolled over.
7	**Bad DLLP Status (BD)**—R/WC. Indicates CRC Error on a DLLP was received.
6	**Bad TLP Status (BT)—**R/WC. Indicates a CRC error on a TLP was received.
5:1	Reserved
0	**Receiver Error Status (RE)—**R/WC. Indicates a receiver error occurred.

24.1.58 CEM—Correctable Error Mask Register (Virtual Root Port—B0:D17:F0)

Address Offset: 114h–117h Attribute: R/WO
Default Value: 0000E000h Size: 32 bits

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled.

Bit	Description
31:16	Reserved
15	**Header Log Overflow Error Mask (HLOEM)—**RO. Mask for Header Log Overflow
14	**Correctable Internal Error Mask (CIEM)—**RO. Mask for Correctable Internal Error
13	**Advisory Non-Fatal Error Mask (ANFEM)**—R/WO. 0 = Does not mask Advisory Non-Fatal errors. 1 = Masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting. ***Note:*** The correctable error detected bit in device status register is set whenever the Advisory Non-Fatal error is detected, independent of this mask bit.
12	**Replay Timer Timeout Mask (RTT)**—RO. Mask for replay timer timeout.
11:9	Reserved
8	**Replay Number Rollover Mask (RNR)—**RO. Mask for replay number rollover.
7	**Bad DLLP Mask (BD)**—RO. Mask for bad DLLP reception.
6	**Bad TLP Mask (BT)—**RO. Mask for bad TLP reception.
5:1	Reserved
0	**Receiver Error Mask (RE)—**RO. Mask for receiver errors.

24.1.59 AECC—Advanced Error Capabilities and Control Register (Virtual Root Port—B0:D17:F0)

Address Offset:	118h–11Bh	Attribute:	RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:11	Reserved
10	**Multiple Header Recording Enable (MHRE)—**RO. Not supported, hardwired to 0b
9	**Multiple Header Recording Capable (MHRC)—**RO. Not supported, hardwired to 0b
8	ECRC Check Enable (ECE)—RO. ECRC is not supported. Hardwired to 0b
7	ECRC Check Capable (ECC)—RO. ECRC is not supported.Hardwired to 0b
6	ECRC Generation Enable (EGE)—RO. ECRC is not supported. Hardwired to 0b
5	ECRC Generation Capable (EGC)—RO. ECRC is not supported. Hardwired to 0b
4:0	First Error Pointer (FEP)—RO. This field identifies the bit position of the first error reported in the Uncorrectable Error Status Register (xref). This register re-arms itself (which does not change its current value) as soon as the error status bit indicated by the pointer is cleared by the software by writing a 1 to that status bit.

24.1.60 AEHRDLOG [1–4]—Advanced Error Header Log (Virtual Root Port—B0:D17:F0)

Address Offset:	11Ch–128hFh	Attribute:	RRO
Default Value:	0000h	Size:	32 bits

Bit	Description
31:0	**TLP Header Log (TLPHDRLOG):** As soon as an error is logged in this register, it remains locked for further error-logging until the software clears the status bit that caused the header log (in other words, until the error pointer is re-armed for logging again).

24.1.61 ROOTERRCMD—Root Error Command Register (Virtual Root Port—B0:D17:F0)

Address Offset:	12Ch	Attribute:	RO, R/W
Default Value:	0000h	Size:	32 bits

Bit	Description
31:3	**Reserved**
2	**Fatal Error Report Enable (FERE)**—R/W. When set, enables the generation of an interrupt when a Fatal error is reported by any of the functions in the hierarchy associated with this root port.
1	**Non-Fatal Error Report Enable (NFERE)**—R/W. When set, enables the generation of an interrupt when a Non-Fatal error is reported by any of the functions in the hierarchy associated with this root port.
0	**Correctable Error Report Enable (CERE)**—R/W. When set, enables the generation of an interrupt when a correctable error is reported by any of the functions in the hierarchy associated with this root port.

24.1.62 ROOTERRSTS—Root Error Status Register (Virtual Root Port—B0:D17:F0)

Address Offset: 130h
Default Value: 00000000h
Attribute: RO, R/WC
Size: 32 bits

Bit	Description
31:27	**Advanced Error Interrupt Message Number (AEMN)**
26:7	**Reserved**
6	**Fatal Error Message Received (FEMR)**—R/WC. Set by hardware, cleared by writing a 1 to this bit
5	**Non-Fatal Error Message Received (NFEMR)**—R/WC. Set by hardware, cleared by writing a 1 to this bit
4	**First Uncorrectable Fatal (FUF)**—R/WC. Set by hardware, cleared by writing a 1 to this bit
3	**Multiple Error Fatal/Non-Fatal Received (MEFR)**—R/WC. Set by hardware, cleared by writing a 1 to this bit
2	**Error Fatal/Non-Fatal Received (EFR)**—R/WC. Set by hardware, cleared by writing a 1 to this bit
1	**Multiple Error Correctable Received (MCER)**—R/WC. Set by hardware, cleared by writing a 1 to this bit
0	**Correctable Error Received (CER)**—R/WC. Set by hardware, cleared by writing a 1 to this bit

24.1.63 ERRSRCID—Error Source Identification Register (Virtual Root Port—B0:D17:F0)

Address Offset: 134h
Default Value: 00000000h
Attribute: RO
Size: 32 bits

Bit	Description
31:16	**Fatal/Non-Fatal Error Source ID (EFSID)**—RO. Requester ID of the source when a Fatal or Non-Fatal error is received.
15:0	**Correctable Error Source ID (ECSID)**—RO. Requester ID of the source when a correctable error is received.

24.1.64 ACSCAPHDR—Access Control Services Extended Capabilities Header (Virtual Root Port—B0:D17:F0)

Address Offset: 138–13Bh
Default Value: 0001000Dh
Attribute: RO, RW-L
Size: 32 bits

Bit	Description
31:20	**Next Capability Offset (NCO)**—RW-L. A value of 000h indicates that this is the last capability.
19i:16	**Capability Version (CV)**—RO. Indicates the version of the Capability structure present.
15:0	**Extended Capability ID (EXCAPID)**—RO. Identifies the function as Access control services capable.

24.1.65 ACSCAP—Access Control Services Capability Register (Virtual Root Port—B0:D17:F0)

Address Offset:	13Ch	Attribute:	RO
Default Value:	005Fh	Size:	16 bits

Bit	Description
15:8	**Egress Control Vector Size (ECVS)**—RO. Indicates the number of bits in the Egress Control Vector. This is set to 00h as the ACS P2P Egress Control (ACSP2PEC) bit 5 in this register is 0b
7	**Reserved**
6	**ACS Direct Translated P2P (T) (ACSDTP2P)**—RO. Indicates that the component does implement ACS Direct Translated P2P
5	**ACS P2P Egress Control (E) (ACSP2PEC)**—RO. Hardwired to 0, this component does not implement ACS P2P Egress Control.
4	**ACS Upstream Forwarding U (ACSUF)**—RO. Indicates that the component implements ACS Upstream Forwarding
3	**xACS P2P Completion Redirect (C) (ACSP2PRR)**—RO. Indicates the component implements ACS P2P Completion redirect.
2	**ACS P2P Request Redirect (R) (ACSP2PRR)**—RO. Indicates that the component implements ACS P2P Request redirect.
1	**ACS Translation Blocking (B) (ACSTB)**—RO. Indicates that the component implements ACS Translation Blocking.
0	**ACS Source Validation (V) (ACSSV)**—RO. Indicates the component implements ACS Source Validation.

24.1.66 ACSCAP—Access Control Services Capability Register (Virtual Root Port—B0:D17:F0)

Address Offset:	13E–13Fh	Attribute:	RO, R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15:7	Reserved. Hardwired to 00h
6	**ACS Direct Translated P2P Enable (T) (ACSDTP2PE)**—R/W. When set, overrides the ACS P2P request Redirect and ACS P2P Egress Control mechanisms with P2P memory requests whose Address Translation (AT) field indicates a Translated Address ***Note:*** This bit is ignored if ACS Translation blocking is enabled.
5	**ACS P2P Egress Control (E) (ACSP2PEC)**—RO. Hardwired to 0, this component does not implement ACS P2P Egress Control.
4	**ACS Upstream Forwarding Enable U (ACSUFE)**—R/W. When set, the port forwards upstream any Request or Completion TLPs it receives that were redirected upstream by a component lower in the hierarchy. Note the U bit only applies to upstream TLPS arriving at a downstream port, and whose normal routing targets the same downstream port.
3	**ACS P2P Completion Redirect Enable (C) (ACSP2PCRE)**—R/W. Determines when the component redirects peer-to-peer completions upstream; applicable only to Read Completions who relaxed ordering attribute is clear.
2	**ACS P2P Request Redirect Enable (R) (ACSP2PRRE)**—R/W. This bit determines when the component redirects peer-to-peer requests upstream.
1	**ACS Translation Blocking Enable (B) (ACSTBE)**—R/W. When set, the port blocks all upstream memory requests whose address translation (AT) field is not set to the default value.
0	**ACS Source Validation Enable (V) (ACSSVE)**—R/W. When set, the port validates the bus number from the Requester ID of upstream requests against the secondary/subordinate bus number.

24.1.67 ERRUNCDETMSK—Uncorrectable Error Detect Mask Register (Virtual Root Port—B0:D17:F0)

Address Offset:	140h–143h	Attribute:	R/WC, RO
Default Value:	00000000h	Size:	32 bits

Bit	Description
31:25	Reserved
24	**AtomicOp Egress Blocked Error Detect Mask (AEBEDM)**—RWS. 0 = Detection and logging enabled 1 = Detection and logging disabled
23	**MC Blocked TLP Error Detect Mask (MCEDM)**—R/W. 0 = Detection and logging enabled
22	**Uncorrectable Internal Error Detect Mask (UIEDM)**—RWS. 0 = Detection and logging enabled 1 = Detection and logging disabled
21	**ACS Violation Error Detect Mask (ACSEDM)**—RWS. 0 = Detection and logging enabled 1 = Detection and logging disabled
20	**Unsupported Request Error Detect Mask (UREDM)**—RWS. 0 = Detection and logging enabled 1 = Detection and logging disabled
19	**ECRC Check Error Mask (ECRCEDM)**—RO. Not supported. Hardwired to 0
18	**Malformed TLP Error Detect Mask (MTLPEDM)**—RWS 0 = Detection and logging enabled 1 = Detection and logging disabled
17	**Receiver Overflow Error Detect Mask (ROEDM)**—RWS 0 = Detection and logging enabled 1 = Detection and logging disabled
16	**Unexpected Completion Error Detect Mask (UCEDM)**—RWS 0 = Detection and logging enabled 1 = Detection and logging disabled
15	**Completer Abort Error Detect Mask (CAEDM)**—RWS 0 = Detection and logging enabled 1 = Detection and logging disabled
14	**Completion Timeout Error Detect Mask (CTEDM)**—RWS 0 = Detection and logging enabled 1 = Detection and logging disabled
13	**Flow Control Error Detect Mask (FCEDM)**—RWS 0 = Detection and logging enabled 1 = Detection and logging disabled
12	**Poisoned TLP Error Detect Mask (PTLPEDM)**—RWS 0 = Detection and logging enabled 1 = Detection and logging disabled
11:6	Reserved
5	**Surprise Link Down Error Detect Mask (SLDEDM)**:R/WS 0 = Detection and logging enabled 1 = Detection and logging disabled
4	**Data Link Protocol Error Detect Mask (DLPEDM)**—RWS 0 = Detection and logging enabled 1 = Detection and logging disabled
3:0	Reserved

24.1.68 ERRCORDETMSK—Correctable Error Detect Mask Register (Virtual Root Port—B0:D17:F0)

Address Offset:	144h–147h	Attribute:	R/WO, RO
Default Value:	0000E000h	Size:	32 bits

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled.

Bit	Description
31:16	Reserved
15	**Header Log Overflow Error Mask (HLOEM)**—R/WO. Mask for Header Log Overflow
14	**Correctable Internal Error Mask (CIEM)**—R/WO. Mask for Correctable Internal Error
13	**Advisory Non-Fatal Error Mask (ANFEM)**—R/WO. 0 = Does not mask Advisory Non-Fatal errors. 1 = Masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting. ***Note:*** The correctable error detected bit in device status register is set whenever the Advisory Non-Fatal error is detected, independent of this mask bit.
12	**Replay Timer Timeout Mask (RTT)**—R/WO. Mask for replay timer timeout.
11:9	Reserved
8	**Replay Number Rollover Mask (RNR)—**R/WO. Mask for replay number rollover.
7	**Bad DLLP Mask (BD)**—R/WO. Mask for bad DLLP reception.
6	**Bad TLP Mask (BT)—**R/WO. Mask for bad TLP reception.
5:1	Reserved
0	**Receiver Error Mask (RE)—**R/WO. Mask for receiver errors.

24.1.69 ROOTERRDETMSK—Root Error Detect Mask Register (Virtual Root Port—B0:D17:F0)

Address Offset:	148h–149h	Attribute:	R/WO, RO
Default Value:	0000E000h	Size:	32 bits

Bit	Description
31:3	Reserved
2	**Received Fatal Message Detect Mask (RFMDM)—**R/WO. Masks detection and logging of Fatal Messages
1	**Received Non-Fatal Message Detect Mask (RNFMDM)**—R/WO. Masks detecting and logging of non-Fatal messages
0	**Received Correctable Error Detect Mask (RCEMDM)—**R/WO. Masks detection and logging of correctable messages

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