

1. Description

1.1. Project

Project Name	Sync_contention_F7
Board Name	custom
Generated with:	STM32CubeMX 6.6.1
Date	09/27/2024

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M7

2. Pinout Configuration

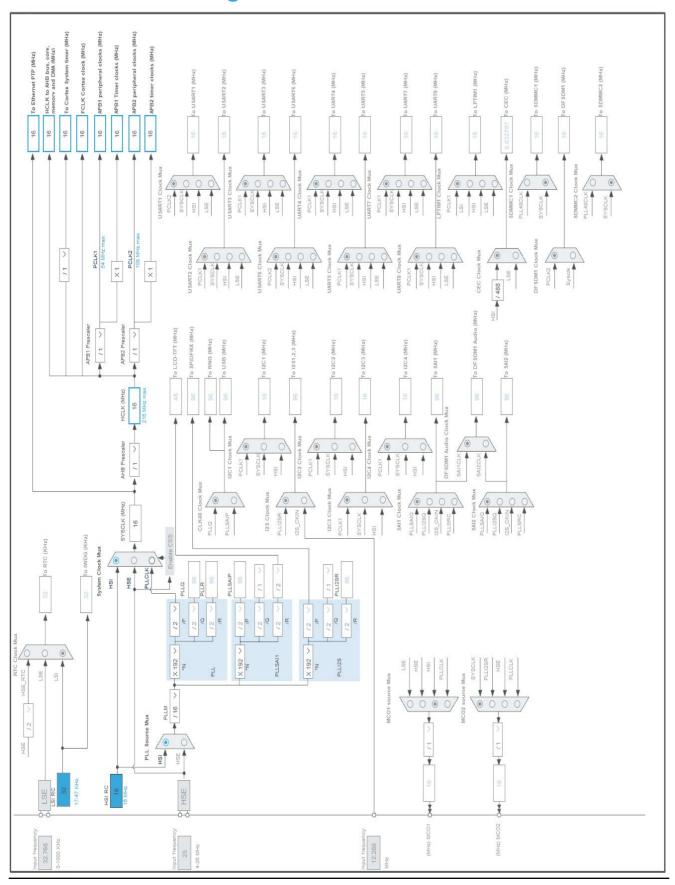


3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP144	(function after		Function(s)	
	reset)			
6	VBAT	Power		
16	VSS	Power		
17	VDD	Power		
25	NRST	Reset		
26	PC0 *	I/O	GPIO_Output	EBlue
29	PC3 *	I/O	GPIO_Output	ERed
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
37	PA3 *	I/O	GPIO_Output	EGreen
38	VSS	Power		
39	VDD	Power		
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VCAP_1	Power		
72	VDD	Power		
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDDUSB	Power		
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
120	VSS	Power		
121	VDDSDMMC	Power		
130	VSS	Power		
131	VDD	Power		
138	воото	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



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5. Software Project

5.1. Project Settings

Name	Value	
Project Name	Sync_contention_F7	
Project Folder	E:\Mysrc\EmbeddedSystems\RTOS\F767ZIT6\2_Synchronization\Sync_contentio	
Toolchain / IDE	STM32CubeIDE	
Firmware Package Name and Version	STM32Cube FW_F7 V1.17.2	
Application Structure	Advanced	
Generate Under Root	Yes	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
мси	STM32F767ZITx
Datasheet	DS11532_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Alkaline(9V)	
Capacity	625.0 mAh	
Self Discharge	0.3 %/month	
Nominal Voltage	9.0 V	
Max Cont Current	200.0 mA	
Max Pulse Current	0.0 mA	
Cells in series	1	
Cells in parallel	1	

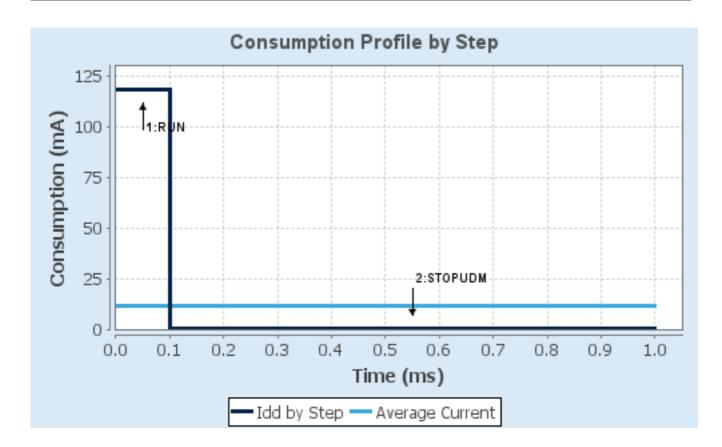
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ICTM FLASH-SingleBank REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	118 mA	130 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	89.42	104.98
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	11.92 mA
Battery Life	2 days, 4 hours	Average DMIPS	462.24005
			DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. CORTEX_M7

7.1.1. Parameter Settings:

Speculation default mode Settings:

Speculation default mode Enabled

Cortex Interface Settings:

Flash Interface AXI Interface
ART ACCELERATOR Disabled
Instruction Prefetch Disabled
CPU ICache Disabled
CPU DCache Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode Background Region Privileged accesses only + MPU Disabled during hard fault,

NMI and FAULTMASK handlers

Cortex Memory Protection Unit Region 0 Settings:

MPU Region Enabled

MPU Region Base Address 0x0 *
MPU Region Size 4GB
MPU SubRegion Disable 0x87 *

MPU TEX field level level 0

MPU Access Permission ALL ACCESS NOT PERMITTED

MPU Instruction AccessDISABLEMPU Shareability PermissionENABLEMPU Cacheable PermissionDISABLEMPU Bufferable PermissionDISABLE

Cortex Memory Protection Unit Region 1 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 2 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 3 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 4 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 5 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 6 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 7 Settings:

MPU Region Disabled

7.2. RCC

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3

Flash Latency(WS) 0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

TIM Prescaler Selection Disabled
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Over Drive Disabled

Power Regulator Voltage Scale Power Regulator Voltage Scale 3

7.3. SYS

Timebase Source: TIM1

7.4. FREERTOS

Interface: CMSIS V2

7.4.1. Config parameters:

API:

FreeRTOS API CMSIS v2

Versions:

FreeRTOS version 10.2.1 CMSIS-RTOS version 2.00

MPU/FPU:

ENABLE_MPU Disabled ENABLE_FPU Disabled

Kernel settings:

USE_PREEMPTION Enabled

CPU_CLOCK_HZ SystemCoreClock

TICK_RATE_HZ 1000 MAX_PRIORITIES 56 MINIMAL_STACK_SIZE 128 16 MAX_TASK_NAME_LEN Disabled USE_16_BIT_TICKS Enabled IDLE_SHOULD_YIELD Enabled USE_MUTEXES Enabled USE_RECURSIVE_MUTEXES Enabled USE_COUNTING_SEMAPHORES 8 QUEUE_REGISTRY_SIZE USE_APPLICATION_TASK_TAG Disabled Enabled ENABLE_BACKWARD_COMPATIBILITY USE_PORT_OPTIMISED_TASK_SELECTION Disabled USE_TICKLESS_IDLE Disabled Enabled USE_TASK_NOTIFICATIONS Disabled RECORD_STACK_HIGH_ADDRESS

Memory management settings:

Memory Allocation Dynamic / Static

TOTAL_HEAP_SIZE 15360

Memory Management scheme heap_4

Hook function related definitions:

USE_IDLE_HOOK Disabled
USE_TICK_HOOK Disabled
USE_MALLOC_FAILED_HOOK Disabled
USE_DAEMON_TASK_STARTUP_HOOK Disabled
CHECK_FOR_STACK_OVERFLOW Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS Disabled
USE_TRACE_FACILITY Enabled
USE_STATS_FORMATTING_FUNCTIONS Disabled

Co-routine related definitions:

USE_CO_ROUTINES Disabled MAX_CO_ROUTINE_PRIORITIES 2

Software timer definitions:

USE_TIMERS Enabled
TIMER_TASK_PRIORITY 2
TIMER_QUEUE_LENGTH 10
TIMER_TASK_STACK_DEPTH 256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY 15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY 5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE size_t
USE_POSIX_ERRNO Disabled

7.4.2. Include parameters:

Include definitions:

vTaskPrioritySet Enabled uxTaskPriorityGet Enabled Enabled vTaskDelete vTaskCleanUpResources Disabled Enabled vTaskSuspend Enabled vTaskDelayUntil Enabled vTaskDelay xTaskGetSchedulerState Enabled xTaskResumeFromISR Enabled Enabled xQueueGetMutexHolder Disabled xSemaphoreGetMutexHolder Disabled pcTaskGetTaskName Enabled uxTaskGetStackHighWaterMark Disabled xTaskGetCurrentTaskHandle Enabled eTaskGetState Disabled xEventGroupSetBitFromISR Enabled xTimerPendFunctionCall Disabled xTaskAbortDelay Disabled xTaskGetHandle uxTaskGetStackHighWaterMark2Disabled

7.4.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT Disabled

Project settings (see parameter description first):

Use FW pack heap file Enabled

^{*} User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max Speed	User Label
GPIO	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EBlue
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ERed
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EGreen

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	15	0	
System tick timer	true	15	0	
TIM1 update interrupt and TIM10 global interrupt	true	15	0	
PVD interrupt through EXTI line 16	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
FPU global interrupt	unused			

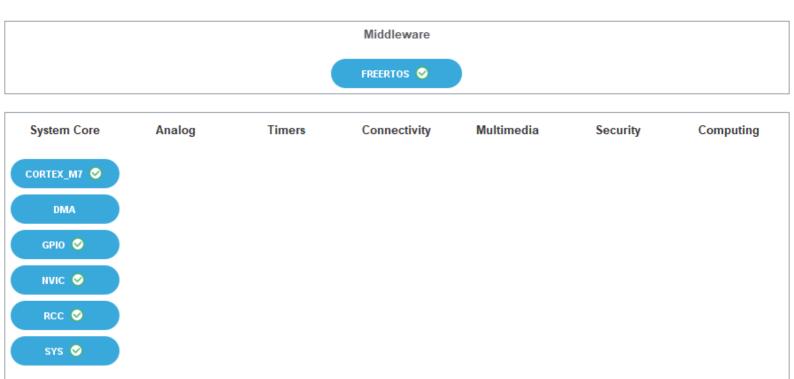
8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
TIM1 update interrupt and TIM10 global interrupt	false	true	true

* User modified value

9. System Views

- 9.1. Category view
- 9.1.1. Current



10. Docs & Resources

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BSDL files https://www.st.com/resource/en/bsdl_model/stm32f7_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32f7_ibis.zip

System View https://www.st.com/resource/en/svd/stm32f7-svd.zip

Description

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