



1. Description

1.1. Project

Project Name	IHC_circular_buffer
Board Name	custom
Generated with:	STM32CubeMX 6.6.1
Date	07/14/2023

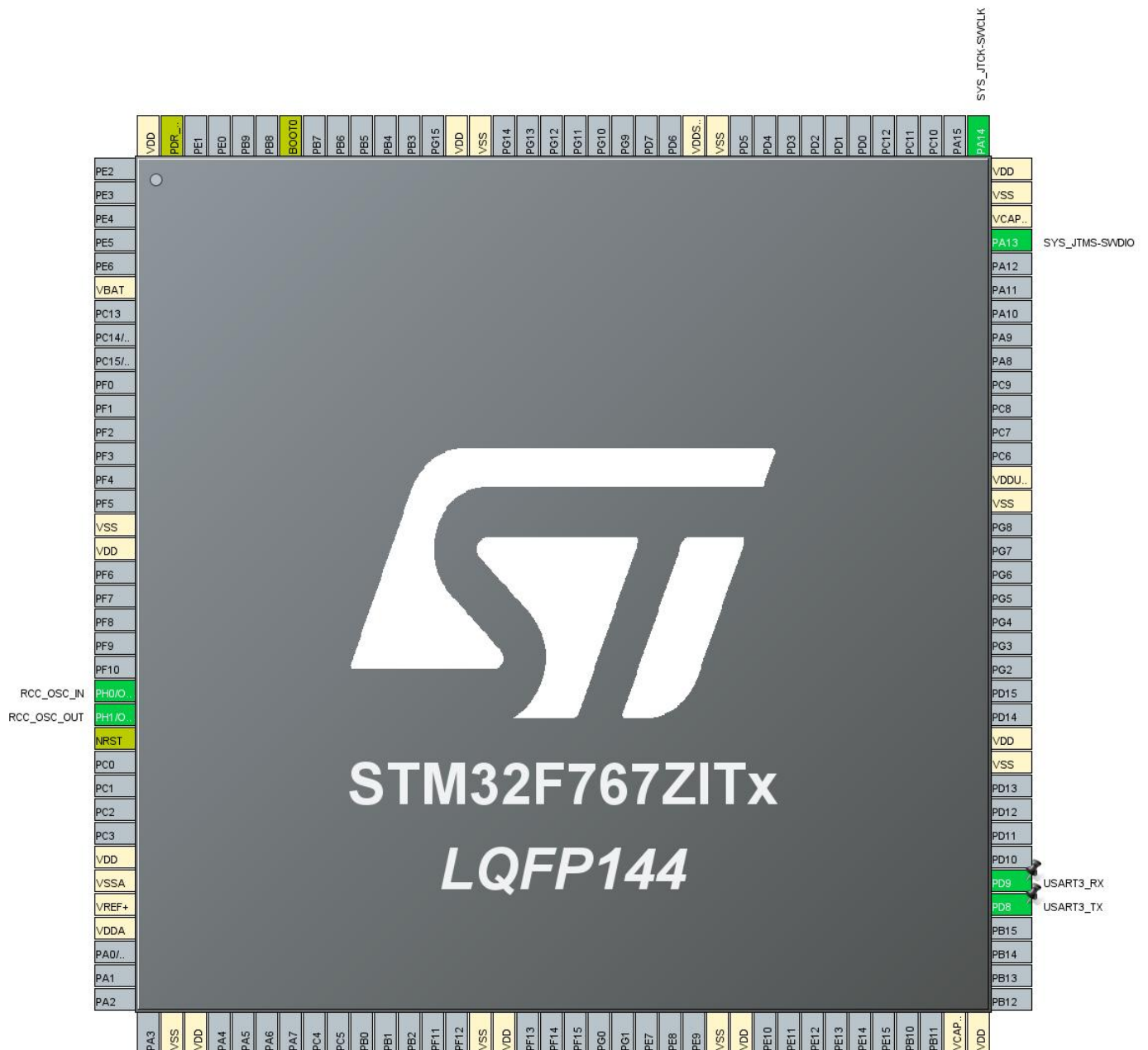
1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M7
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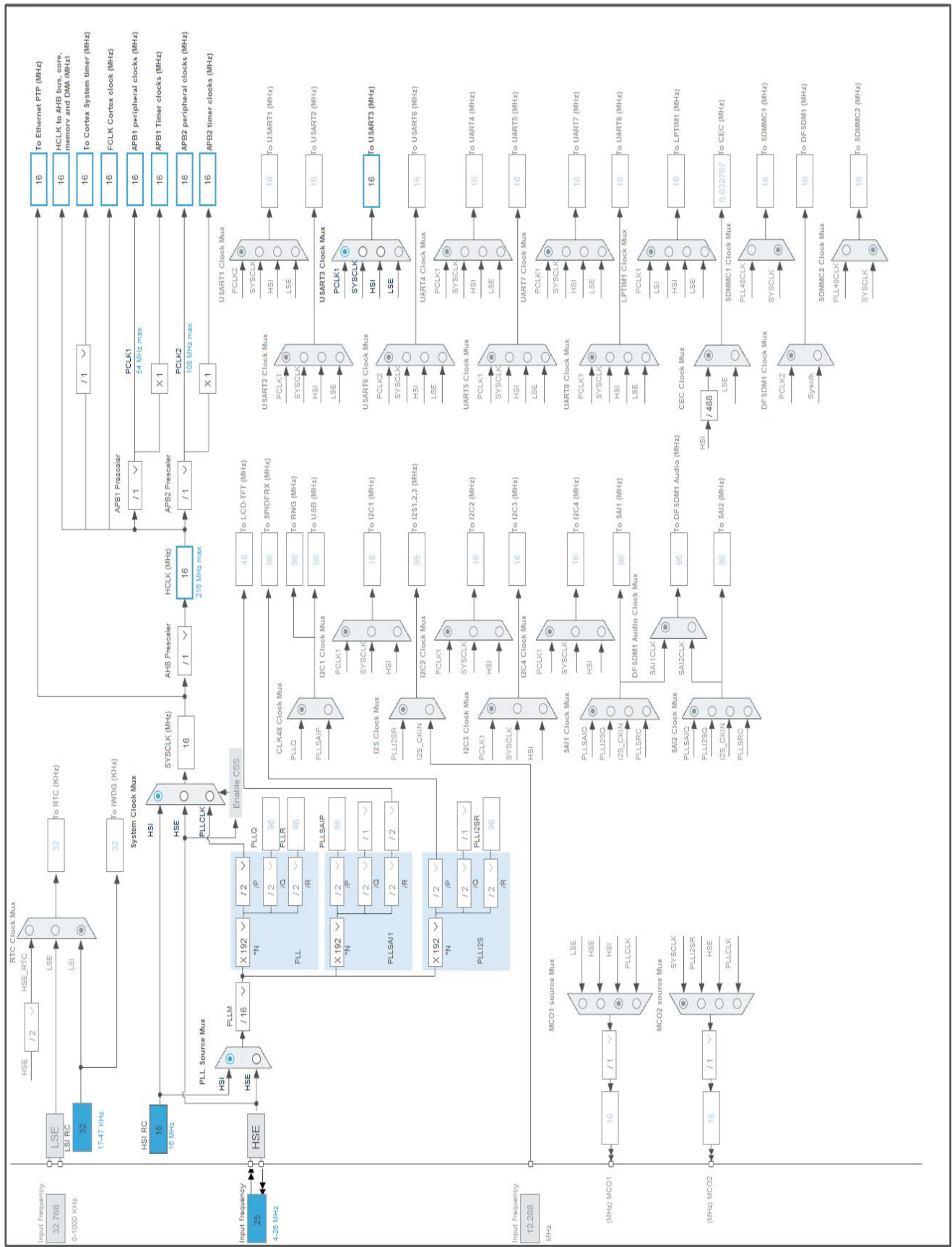
2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
16	VSS	Power		
17	VDD	Power		
23	PH0/OSC_IN	I/O	RCC_OSC_IN	
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
38	VSS	Power		
39	VDD	Power		
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VCAP_1	Power		
72	VDD	Power		
77	PD8	I/O	USART3_TX	
78	PD9	I/O	USART3_RX	
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDDUSB	Power		
105	PA13	I/O	SYS_JTMS-SWDIO	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
120	VSS	Power		
121	VDDSDMMC	Power		
130	VSS	Power		
131	VDD	Power		
138	BOOT0	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	IHC_circular_buffer
Project Folder	E:\Mysrc\EmbeddedSystems\RTOS\F767ZIT6\IHC_circular_buffer
Toolchain / IDE	EWARM V8.50
Firmware Package Name and Version	STM32Cube FW_F7 V1.17.0
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_USART3_UART_Init	USART3
4	MX_DMA_Init	DMA

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767ZITx
Datasheet	DS11532_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

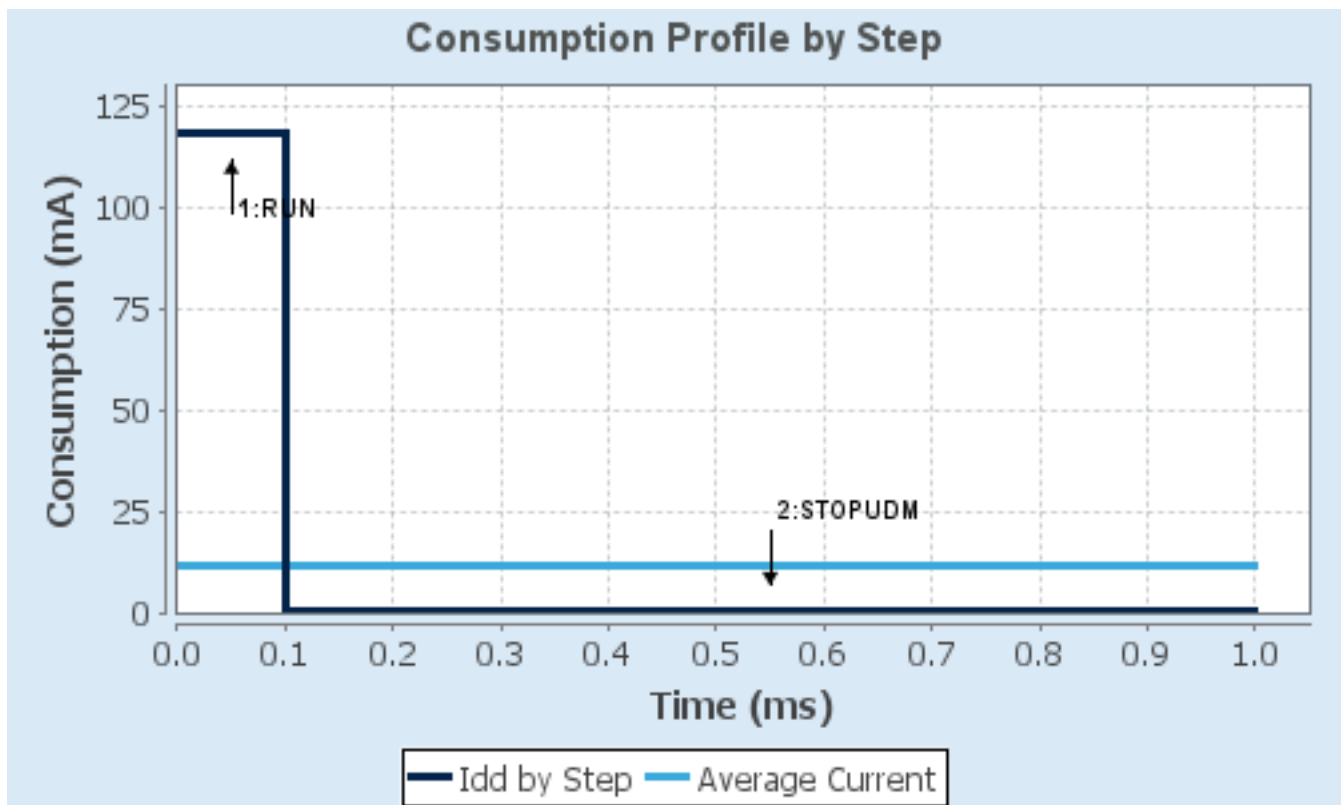
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ICTM FLASH-SingleBank REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	118 mA	130 μ A
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	89.42	104.98
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	11.92 mA
Battery Life	2 days, 4 hours	Average DMIPS	462.24005 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. CORTEX_M7

7.1.1. Parameter Settings:

Speculation default mode Settings:

Speculation default mode Enabled

Cortex Interface Settings:

Flash Interface AXI Interface

ART ACCELERATOR Disabled

Instruction Prefetch Disabled

CPU ICache Disabled

CPU DCache Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers

Cortex Memory Protection Unit Region 0 Settings:

MPU Region Enabled

MPU Region Base Address **0x0 ***

MPU Region Size 4GB

MPU SubRegion Disable **0x87 ***

MPU TEX field level level 0

MPU Access Permission ALL ACCESS NOT PERMITTED

MPU Instruction Access DISABLE

MPU Shareability Permission ENABLE

MPU Cacheable Permission DISABLE

MPU Bufferable Permission DISABLE

Cortex Memory Protection Unit Region 1 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 2 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 3 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 4 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 5 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 6 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 7 Settings:

MPU Region Disabled

7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Flash Latency(WS) 0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
TIM Prescaler Selection Disabled
HSE Startup Timeout Value (ms) 100
LSE Startup Timeout Value (ms) 5000

Power Parameters:

Power Over Drive Disabled
Power Regulator Voltage Scale Power Regulator Voltage Scale 3

7.3. SYS

Debug: Serial Wire

Timebase Source: TIM1

7.4. USART3

Mode: Asynchronous

7.4.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200
Word Length 8 Bits (including Parity)
Parity None
Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit
Over Sampling 16 Samples
Single Sample Disable

Advanced Features:

Auto Baudrate Disable

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART3_RX	DMA1_Stream1	Peripheral To Memory	Medium *

USART3_RX: DMA1_Stream1 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
DMA1 stream1 global interrupt	true	0	0
TIM1 update interrupt and TIM10 global interrupt	true	15	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USART3 global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream1 global interrupt	false	true	true
TIM1 update interrupt and TIM10 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
CORTEX_M7 ✓			USART3 ✓			
DMA ✓						
GPIO ✓						
IVIC ✓						
RCC ✓						
SYS ✓						

10. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32f7_bsd.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32f7_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32f7-svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
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Application Notes https://www.st.com/resource/en/application_note/an5394-getting-started-with-projects-based-on-the-stm32l5-series-in-stm32cubeide-stmicroelectronics.pdf

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Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5731-stm32cubemx-and-stm32cubeide-threadsafe-solution-stmicroelectronics.pdf
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Design Notes & Tips	https://www.st.com/resource/en/design_tip/dt0117-microphone-array-beamforming-in-the-pcm-and-pdm-domain-stmicroelectronics.pdf
Errata Sheets	https://www.st.com/resource/en/errata_sheet/es0334-stm32f76xxx-and-stm32f77xxx-device-errata-stmicroelectronics.pdf
Datasheet	https://www.st.com/resource/en/datasheet/dm00273119.pdf
Programming Manuals	https://www.st.com/resource/en/programming_manual/pm0253-stm32f7-series-and-stm32h7-series-cortexm7-processor-programming-manual-stmicroelectronics.pdf
Reference Manuals	https://www.st.com/resource/en/reference_manual/rm0410-stm32f76xxx-and-stm32f77xxx-advanced-armbased-32bit-mcus-stmicroelectronics.pdf
Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1163-description-of-wlcsp-for-microcontrollers-and-recommendations-for-its-use-stmicroelectronics.pdf
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