

1. Description

1.1. Project

Project Name	SEN_T6713_C02
Board Name	custom
Generated with:	STM32CubeMX 6.6.1
Date	07/05/2023

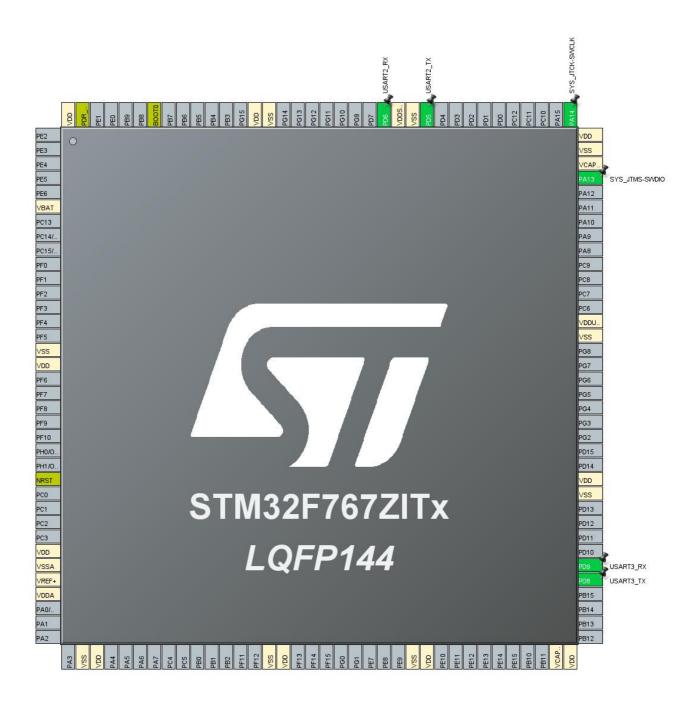
1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M7

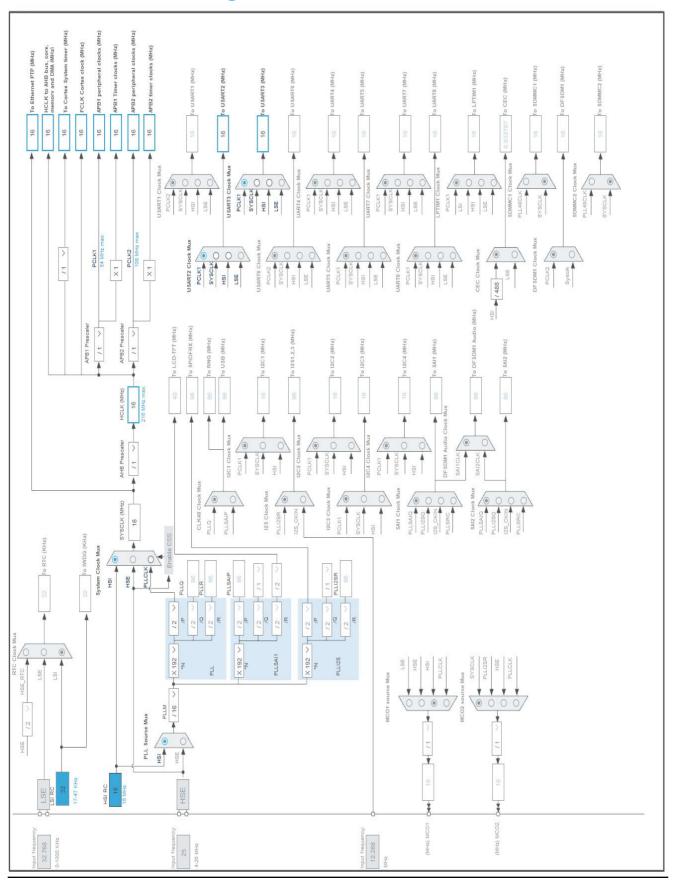
2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after	Pin Type	Alternate Function(s)	Label
•	reset)	-		
6	VBAT	Power		
16	VSS	Power		
17	VDD	Power		
25	NRST	Reset		
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
38	VSS	Power		
39	VDD	Power		
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VCAP_1	Power		
72	VDD	Power		
77	PD8	I/O	USART3_TX	
78	PD9	I/O	USART3_RX	
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDDUSB	Power		
105	PA13	I/O	SYS_JTMS-SWDIO	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
119	PD5	I/O	USART2_TX	
120	VSS	Power		
121	VDDSDMMC	Power		
122	PD6	I/O	USART2_RX	
130	VSS	Power	OUNITZ_IM	
131	VDD	Power		
138	BOOT0	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

4. Clock Tree Configuration



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5. Software Project

5.1. Project Settings

Name	Value	
Project Name	SEN_T6713_C02	
Project Folder	E:\Mysrc\EmbeddedSystems\RTOS\F767ZIT6\SEN_T6713_C02	
Toolchain / IDE	STM32CubeIDE	
Firmware Package Name and Version	STM32Cube FW_F7 V1.17.0	
Application Structure	Advanced	
Generate Under Root	Yes	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name	
1	SystemClock_Config	RCC	
2	MX_GPIO_Init	GPIO	
3	MX_USART3_UART_Init	USART3	
4	MX_USART2_UART_Init	USART2	

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
мси	STM32F767ZITx
Datasheet	DS11532_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Alkaline(9V)	
Capacity	625.0 mAh	
Self Discharge	0.3 %/month	
Nominal Voltage	9.0 V	
Max Cont Current	200.0 mA	
Max Pulse Current	0.0 mA	
Cells in series	1	
Cells in parallel	1	

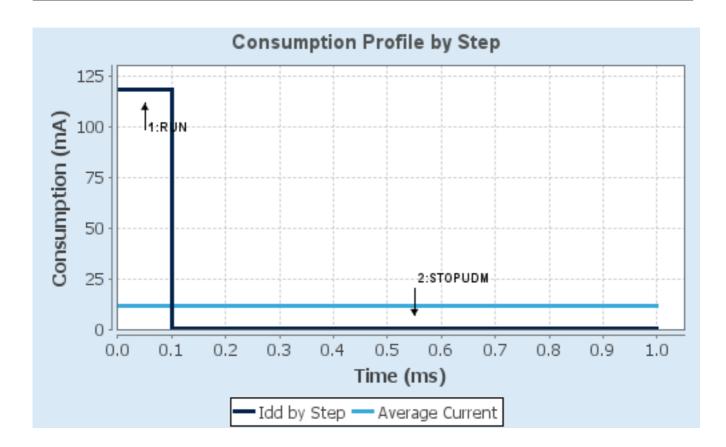
6.4. Sequence

	1		
Step	Step1	Step2	
Mode	RUN	STOP UDM (Under Drive)	
Vdd	3.3	3.3	
Voltage Source	Battery	Battery	
Range	Scale1-High	No Scale	
Fetch Type	ICTM FLASH-SingleBank REGON	n/a	
CPU Frequency	216 MHz	0 Hz	
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn	
Clock Source Frequency	4 MHz	0 Hz	
Peripherals			
Additional Cons.	0 mA	0 mA	
Average Current	118 mA	130 μΑ	
Duration	0.1 ms	0.9 ms	
DMIPS	462.0	0.0	
Ta Max	89.42	104.98	
Category	In DS Table	In DS Table	

6.5. Results

Sequence Time	1 ms	Average Current	11.92 mA
Battery Life	2 days, 4 hours	Average DMIPS	462.24005
			DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. RCC

7.1.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3

Flash Latency(WS) 0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

TIM Prescaler Selection Disabled

HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Over Drive Disabled

Power Regulator Voltage Scale Power Regulator Voltage Scale 3

7.2. SYS

Debug: Serial Wire

Timebase Source: TIM1

7.3. USART2

Mode: Asynchronous

7.3.1. Parameter Settings:

Basic Parameters:

Baud Rate 19200 *

Word Length 9 Bits (including Parity) *

Parity Even *

Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

Advanced Features:

Auto Baudrate Disable
TX Pin Active Level Inversion Disable
RX Pin Active Level Inversion Disable

Data InversionDisableTX and RX Pins SwappingDisableOverrunEnableDMA on RX ErrorEnableMSB FirstDisable

7.4. USART3

Mode: Asynchronous

7.4.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable RX Pin Active Level Inversion Disable Disable **Data Inversion** Disable TX and RX Pins Swapping Enable Overrun DMA on RX Error Enable MSB First Disable

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	
USART2	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	15	0	
TIM1 update interrupt and TIM10 global interrupt	true	15	0	
USART2 global interrupt	true	0	0	
PVD interrupt through EXTI line 16		unused		
Flash global interrupt	unused			
RCC global interrupt		unused		
USART3 global interrupt	unused			
FPU global interrupt	unused			

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
TIM1 update interrupt and TIM10 global interrupt	false	true	true
USART2 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

			Middleware			
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
CORTEX_M7 ❷			USART2 ♥			
DMA			USART3 ♥			
GPIO ❤						
NVIC ⊘						
RCC ♥						
sys 🤡						

10. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32f7_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32f7_ibis.zip

System View https://www.st.com/resource/en/svd/stm32f7_svd.zip

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