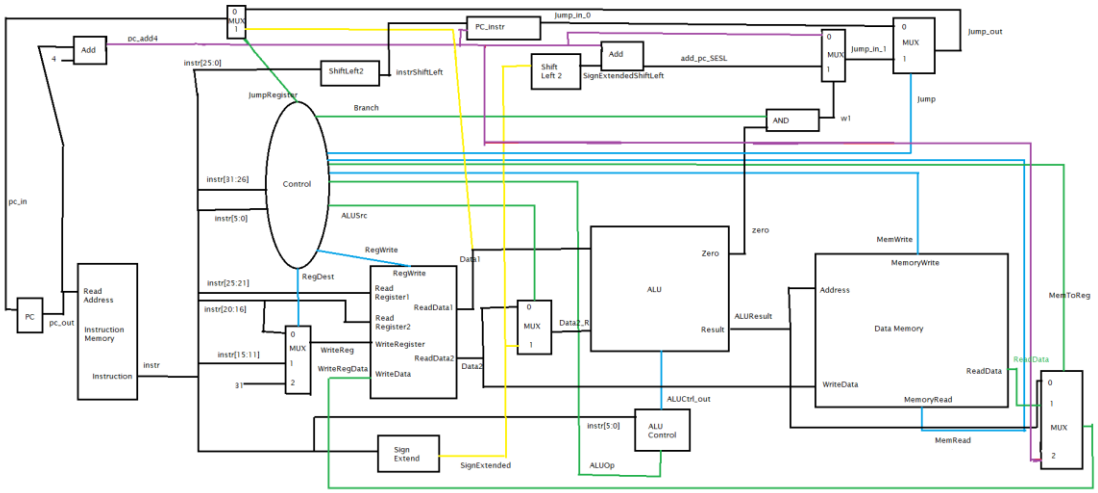
Computer Organization Lab3

Architecture diagrams:



電路設計如上圖所示。

Hardware module analysis:

這次的設計與上次的電路圖大致相同，比較不同之處為 decoder 增加了許多新的 output，用於控制此次新增的 operation(多數為 jal/jr/beq)。在控制 program counter 上我也新增了一個 MUX 來決定是否為 JR。

參考資料： https://goo.gl/fWmXaY

Finished part:

```
Data Memory =       1,      2,      0,      0,      0,      0,      0,      0
Data Memory =       0,      0,      0,      0,      0,      0,      0,      0
Data Memory =       0,      0,      0,      0,      0,      0,      0,      0
Data Memory =       0,      0,      0,      0,      0,      0,      0,      0
Registers
R0 =        0, R1 =         1, R2 =         2, R3 =         3, R4 =         4, R5 =         5, R6 =         1, R7 =         2
R8 =        4, R9 =         2, R10 =        0, R11 =        0, R12 =        0, R13 =        0, R14 =        0, R15 =        0
R16 =       0, R17 =        0, R18 =        0, R19 =        0, R20 =        0, R21 =        0, R22 =        0, R23 =        0
R24 =       0, R25 =        0, R26 =        0, R27 =        0, R28 =        0, R29 =        0, R30 =        128, R31 =      0
```

上圖為測資一之截圖。

```
Data Memory =       0,      0,      0,      0,      0,      0,      0,      0
Data Memory =       0,      0,      0,      0,      0,      0,      0,      0
Data Memory =       0,      0,      0,      0,      68,     2,      1,      68
Data Memory =       2,      1,      68,     4,      3,      16,     0,      0
Registers
R0 =        0, R1 =         0, R2 =         5, R3 =         0, R4 =         0, R5 =         0, R6 =         0, R7 =         0
R8 =        0, R9 =         1, R10 =        0, R11 =        0, R12 =        0, R13 =        0, R14 =        0, R15 =        0
R16 =       0, R17 =        0, R18 =        0, R19 =        0, R20 =        0, R21 =        0, R22 =        0, R23 =        0
R24 =       0, R25 =        0, R26 =        0, R27 =        0, R28 =        0, R29 =        0, R30 =        128, R31 =      16
```

上圖為測資二之截圖。