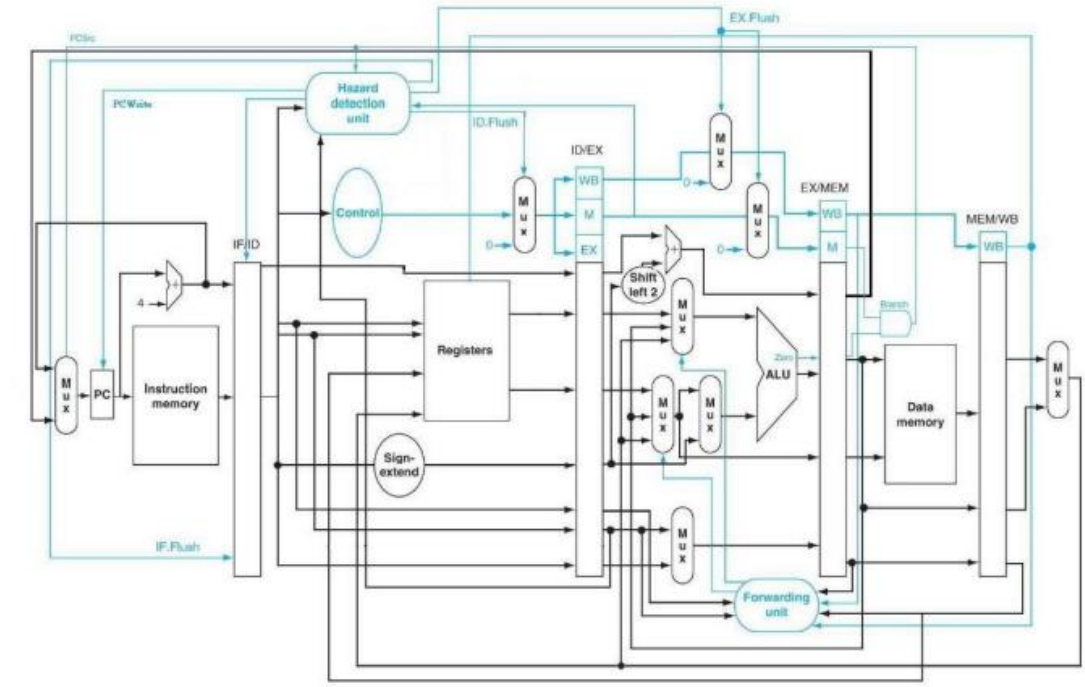
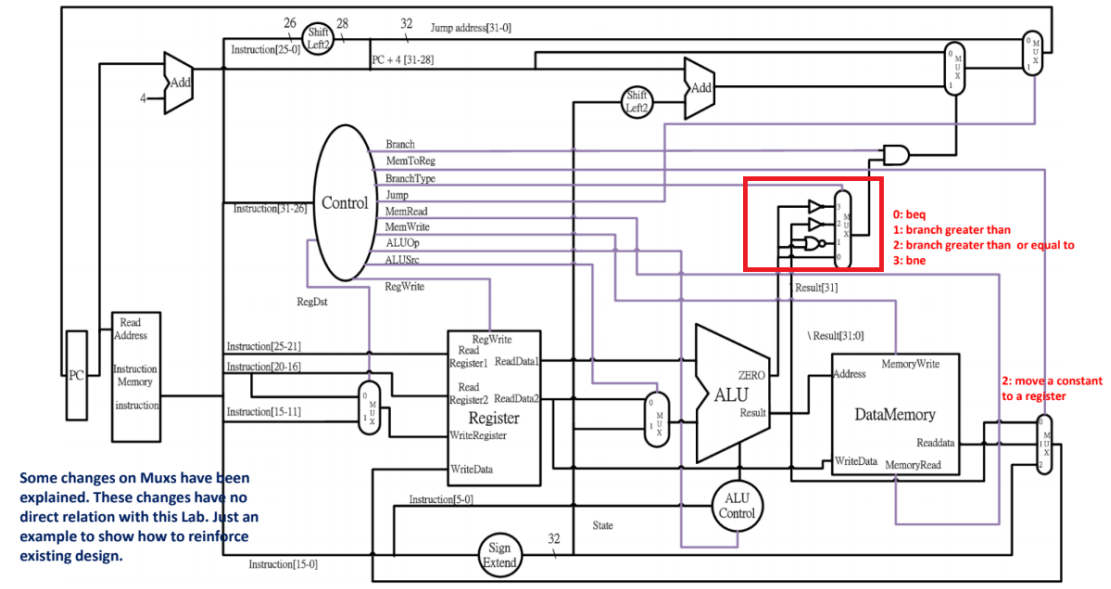
Computer Organization Lab5

Architecture diagrams:





這次的電路圖設計是以上圖為基準，再在上圖的 Branch 之前加上下圖紅框內的部分以實作這次 Advanced instruction 的部分。

Hardware module analysis:

這次的架構與 Lab4 大致相同，多的部分只在 forwarding 以及 hazard detection，forwarding 使 CPU 能夠實現 pipeline 的功能，hazard detection 則會在必要的時候 stall instruction，使 pipeline CPU 能夠順利運作。

Finished part:

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Register==========================================================

r0=          0, r1=         16, r2=        256, r3=          8, r4=         16, r5=          8, r6=         24, r7=         26

r8=          8, r9=          1, r10=          0, r11=          0, r12=          0, r13=          0, r14=          0, r15=          0

r16=          0, r17=          0, r18=          0, r19=          0, r20=          0, r21=          0, r22=          0, r23=          0

r24=          0, r25=          0, r26=          0, r27=          0, r28=          0, r29=          0, r30=          0, r31=          0


Memory============================================================

m0=          0, m1=         16, m2=          0, m3=          0, m4=          0, m5=          0, m6=          0, m7=          0

m8=          0, m9=          0, m10=          0, m11=          0, m12=          0, m13=          0, m14=          0, m15=          0

r16=          0, m17=          0, m18=          0, m19=          0, m20=          0, m21=          0, m22=          0, m23=          0

m24=          0, m25=          0, m26=          0, m27=          0, m28=          0, m29=          0, m30=          0, m31=          0
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