A Time-Domain Short Circuit Study for a VSC Based Battery Energy Storage System

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***Abstract*—A phasor domain short circuit study for a battery energy storage system was performed per ANSI C37.010-2016. Results showed high short circuit asymmetrical currents. Two time-domain models were also built— simplified and detailed —to compare the results with the phasor domain study. The results of both the simplified and the detailed time-domain models agree to a large degree with the simplified model on the conservative side. However, the results of both models differ dramatically from the phasor domain model. The results in this paper show the need to update the ANSI C37.010-2016 to account for battery energy storage and inverter based-generation in general.**

***Index Terms*—Electromagnetic transients, EMTDC, Energy storage, Short-circuit currents, Storage battery, Voltage source inverters.**

NOMENCLATURE

BESS	Battery Energy Storage System
MPT	Main Power Transformer
MV	Medium Voltage
PCS	Power Conversion Unit
PMT	Padmount Transformer
PWM	Pulse-Width Modulation
POI	Point of Interconnection
RMS	Root Mean Square
VSC	Voltage Source Converter

I. Introduction

ANY battery energy storage system (BESS) project goes through what is known as conceptual design. This conceptual design incorporates realistic assumptions about the grid. The most critical assumptions are the short circuit contribution from the interconnecting utility and the transfer power capability of the interconnecting transmission lines. This conceptual design becomes an integral part of the financial model of the project. This design eventually becomes complete by filling in the details once a project developer decides to move on with the project if a financial institution chooses to finance a project. The conceptual design involves the determination of the ratings of the major components of the project, such as the substation switchgear, the main power transformer (MPT) size, and the ratings of the battery container inverter technology, which is better known as in the industry as power conversion unit (PCS). The PCS converts the DC battery energy into AC energy and vice versa for charging and discharging operations.

In this paper, we perform short circuit studies for a large BESS project consisting of 68 voltage source converter (VSC) PCS with a total capacity of 204 MW connected to a 230 kV substation. Each PCS contains an inverter, switchgear, and a 0.63kV/34.5 kV 3.45 MVA padmount transformer (PMT), all in one assembly. The studies are performed using three methods: (1) ASPEN OneLiner phasor-domain simulation [1], (2) PSCAD®/EMTDC® [2] simplified time-domain simulations, and (3) PSCAD detailed time-domain simulations. The comparison of the studies shows that phasor-domain short-circuit levels are conservative as compared to time-domain results. Also, a sensitivity analysis is carried out for detailed time-domain simulations to show the dependencies of the short-circuit level on the system operating and modeling conditions, e.g., BESS connection status, MPT tap, utility source state.

The phasor domain short circuit study was done in ASPEN based on the IEEE ANSI C37.010-1979 [3] and IEEE Violet Book [4]. The IEEE ANSI C37.010-1979 is what has been historically programmed in all phasor domain commercial short circuit packages to calculate breaker duty ratings. The IEEE ANSI C37.010-1979 was later updated to IEEE ANSI C37.010-2016 [5], and the updated version is essentially the same. IEEE Violet Book was later updated to IEEE 3002.3-2018 [6]. The most important aspect of the IEEE C37.010-2016 is the multiplication factor for determining the asymmetrical current component in case the X/R ratio is not 17. Both IEEE standards go into depth to create sequence networks that would produce worst case X/R ratios that tend to conservatively size the breaker.

Several articles have discussed fault current contributions from inverter-based generation; however, the literature is lacking in comparing asymmetrical fault current contributions from BESS based on the phasor and time-domain simulation. The asymmetrical current peak of 1-5 per unit (p.u.) of inverter's rated peak current for up to a quarter of a cycle is documented in [7], [8]— 4-5 p.u. for single-phase inverters and 2-3 p.u. for three-phase inverters. Since the asymmetrical fault characteristics of inverter-based generators differ from conventional synchronous generators [9], it is required to review and update the relevant standard for selecting the circuit breaker capacities.

The paper is organized as follows: Section §II provides details of the BESS project. The phasor domain study is given in Section §III. The simplified and detailed time-domain studies are provided in Section §IV and Section §V, respectively.

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Section §VI discusses the comparison of phasor and time-domain simulations. Section §VII summarizes the findings.

II. BESS PROJECT DESCRIPTION

Figure 1 shows the PCS layout used in the BESS project under study, which is a voltage source converter PCS capable of black-start. The PCS consists of an inverter, switchgear, and a PMT, all in one assembly. In this sense, a PCS is more than an inverter: it is the whole DC/AC conversion system. What makes this PCS unique is the existence of switchgear that serves a specific function in the overall topology. The overcurrent protection settings of this switchgear are not adjustable due to this functionality. The switchgear model used in this project is rated for 20 kA RMS current interruption, while the closing and latching is 54.6 kA peak. The DC side runs at a voltage between 900 V to 1300 V, and the AC output voltage is 630 V. The PMT is 0.63 kV/34.5 kV rated at 3.45 MVA with a vector group of Dy1. The bushing is capable of withstanding 20 kA RMS symmetrical current for two seconds and 52 kA peak current for ten cycles per the IEEE C37.20.3 standard [10]. The PCS vendor rates the whole PCS assembly for 52 kA peak withstand for ten cycles.

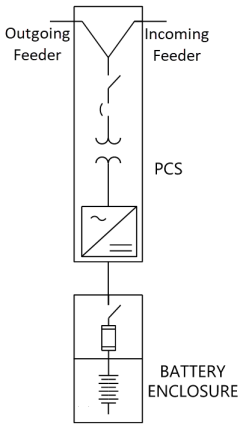

Fig. 1. Power conversion unit (PCS) used in the battery energy storage energy system (BESS) project under study.

The project consists of sixty-eight (68) PCSs. Each PCS is connected to one battery enclosure. The PCSs are arranged in strings, and all strings are connected in parallel. Each string contains several PCSs in series.

Figure 2 outlines the interconnection of the BESS project under study (shown in red). The BESS project has a total capacity of 204 MW. The MPT of this project is a three-winding transformer that is top rated for 265 MVA. The MPT impedance is 8.4% at the top rating (16R tap and 16L tap impedances are 8.74% and 8.26%, respectively), and the vector group is YN1yn1d1. The BESS interconnects to the transmission grid through two 230 kV transmission lines that connect to a 500 kV level through a 500 kV/230 kV step-up substation. The black buses at the end of the 230 kV tie lines (floating buses on the right of Figure 2) are proposed for substations for future inverter-based generation and storage.

The original conceptual design assumed a short circuit current of 25 kA at the 230 kV bus at the step-up substation.

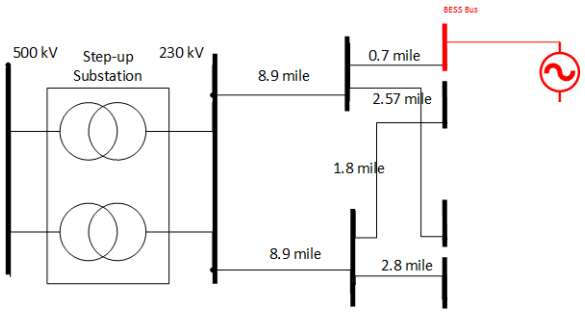

Fig. 2. Interconnection of the understudy (red) BESS project.

The inverter short circuit was considered to be 1.1 p.u. Using these assumptions, the short circuit at the low side of the MPT within the BESS project is 24.7 kA. The designer decided to use 40 kA low side breakers.

The current utility short circuit level is 24.5 kA, the maximum build out is 34.3 kA, while the emergency condition is 49.9 kA. The PCS subtransient reactance is 0.96pu while the synchronous reactance is 0.99 pu. The first thing to notice about the current utility short circuit is that it is very close to the assumed utility short circuit in the conceptual design. The second thing to notice is that the inverter steady-state short circuit contribution is one p.u., which is lower than the assumption in the conceptual design. The third thing is that the PCS short circuit impedance has no resistive component even though it contains the PMT resistance. Upon contacting the PMT vendor, it was made clear that the PCS contribution is on the 34.5 kV side and does not include any resistance for conservative results. However, what was not known in conceptual design stage is that the 230 kV bus at the step-up substation can have a short circuit of 49.9 kA. The step-up substation has two large transformers, and the grid operator would parallel them in case of specific emergency conditions. Also, what was not known during conceptual design is that the grid short circuit can go up by 10 kA in case all of the projects get built in the area.

III. PHASOR DOMAIN STUDY

This section describes the phasor domain modeling and short circuit study results.

A detailed phasor-domain short circuit study was performed using ASPEN utilizing the grid emergency short circuit condition. The results at the substation are given in Table I. The BESS collection system is short; thus, the fault at the first PCS can be considered the same as the fault at the low side bus. One thing that stands out in these results is the abnormally high X/R ratio at the low side bus. Due to the high X/R ratios, the calculated peak currents are also high and are given in Table I and are calculated using the equations in IEEE Std 551-2006 [11]. The standard contains different ways of calculating the peak currents, but it did not significantly differ. It should be noted that using the emergency grid short circuit is not making a lot of difference at the low side three phase short circuit because of the long tie lines and the impedance of the MPT.

Based on the results, the short circuit currents at the first PCS on the string are higher than the PCS unit's rated short

TABLE I
SUBSTATION SHORT CIRCUIT

	3-Phase Short Circuit	Peak Current	X/R
230 kV High Side Bus	20.1 kA	53.6 kA	16.9
34.5 kV High Side Bus	23.1 kA	63.2 kA	43.1

circuit capability. The theoretical maximum peak current is $2 \times \sqrt{2} \times Fault\ Current\ RMS$. Based on that, the theoretical maximum peak is 65.3 kA. The calculated peak current from the short circuit study is due to the high X/R and the equations used in the standards. Since the peak current is much higher than the capability, a safety concern has arisen. High peak currents can cause high forces, and the breaker may shatter. Since the peak current at the low side in the fault study was close to the maximum theoretical, a time-domain study was warranted to obtain more accurate results.

While the time-domain study in Section §IV and Section §V were performed, the authors reached out to the PCS vendor to see if the vendor can produce test data to verify the peak withstand of the switchgear of the PCS. The vendor performed more testing and showed that the PCS switchgear and disconnect switch assembly can withstand 63.6 kA peak current.

IV. SIMPLIFIED TIME-DOMAIN MODEL

This section describes the simplified time-domain modeling and short circuit study results. PSCAD, a general-purpose time-domain simulation tool for studying the transient behavior of electrical networks, is used for the simulations.

For this study, the phasor-domain short circuit study model of Section §III was converted to a time-domain model. All transmission lines and underground cables were converted to pi-equivalent segments. The grid was represented as an ideal voltage source behind an impedance. The impedance was chosen to produce the emergency condition fault current at the 230 kV point of interconnection (POI) bus. The PCS was represented as an ideal voltage behind a 0.962 pu impedance at the 34.5 kV level. The purpose of the time-domain study is to:

1) Quantify the effect of the cable and transmission line charging capacitance
2) Obtain a more realistic estimate of the peak current
3) Perform a sensitivity study regarding the MPT tap changer, transmission line temperature, and generation level in the project

A worst-case analysis showed that the peak current is 57 kA and is shown in Figure 3. This is 10% less than the phasor domain short circuit study. For this reason, it was decided to perform a detailed time-domain analysis that considers the PCS inverter response and this is given in the next section.

V. DETAILED TIME-DOMAIN MODEL

This section describes the detailed PSCAD time-domain modeling, simulated cases, and short circuit study results.

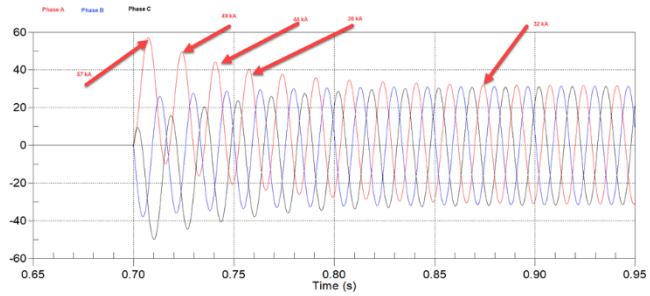

Fig. 3. Fault current using simplified PSCAD study.

A. PCS Model Benchmarking

The PCS vendor provided the PSCAD model, which can be parameterized to represent a single PCS and an aggregated model of the whole BESS. It should be noted that the vendor PSCAD model contains a transformer with zero resistance as well. First, the single PCS model short-circuit contributions are validated with the laboratory-tested values by applying a three-phase-to-ground fault on the medium voltage (MV) side. Figure 4, Figure 5, and Figure 6 show the simulated results—(1) currents at the MV side, (2) currents at the low-voltage side, (3) pulse-width modulation (PWM) output voltage, and (4) power frequency filtered PWM output voltage. The figures display that a current spike of 1.87 p.u. appears for a short duration because inverter control takes around 200 µs to decrease PWM average voltage. These simulated results match well with the PCS laboratory tests as given in Figure 7.

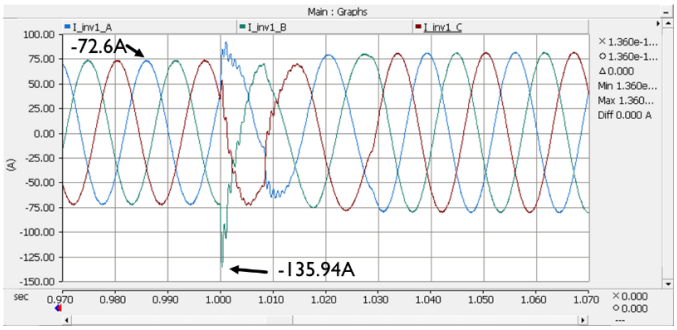

Fig. 4. Single PCS current contribution of detailed PSCAD model (all phases) at the MV side for a 3-phase-to-ground fault on the MV side at 1 second.

B. PCS Reduced Order Model

The vendor-provided PCS model has a limitation that only six to seven instances can be executed using a typical computer. Therefore, the PCS aggregation approach is adopted to perform simulation for the BESS project—a single equivalent PCS model is used for multiple instances by changing the parameters following the vendor instructions.

The short circuit contributions of four and eight PCS instances and their equivalent aggregates are validated by applying a three-phase-to-ground fault at 1 s on the MV side of the PMT. A one second is used to ensure that the models

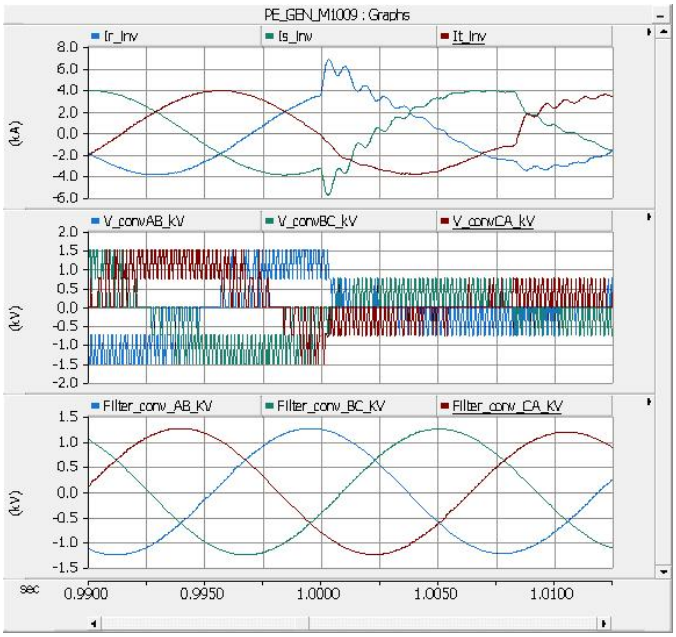

Fig. 5. Currents using detailed PSCAD model at the low-voltage side (top), PWM output voltage (middle), PWM output voltage filtered for power frequency (bottom).

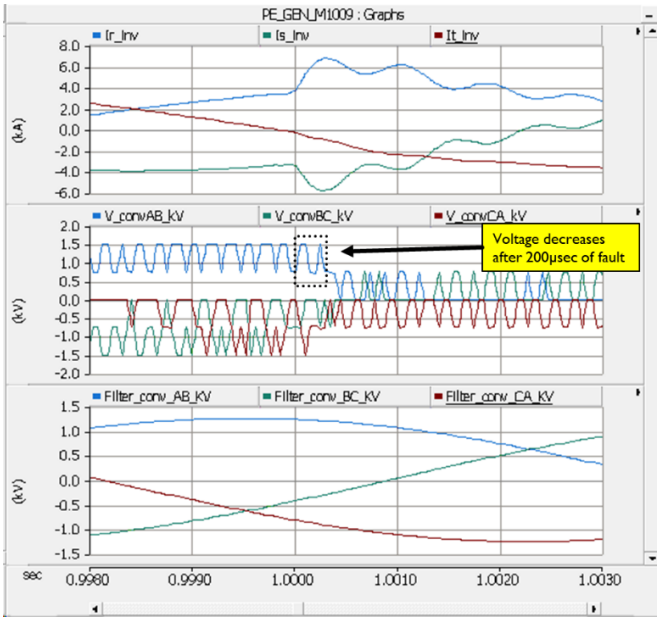

Fig. 6. Currents using detailed PSCAD model at the low-voltage side of the PMT (top), PWM output voltage (middle), PWM output voltage filtered for power frequency (bottom).

have reached steady state before introducing the fault. In the multiple instances case, a short (50 ft) 500 kcmil cable is also considered between inverters to imitate the actual field installation. Figure 8, Figure 9, Figure 10 and Figure 11 show the simulation setups and results. The total fault contributions are approximately the same as their model equivalents for both four and eight PCS instances.

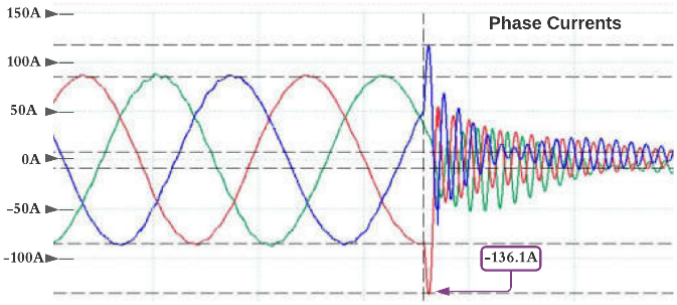

Fig. 7. Single PCS laboratory test current measurements at the MV side of the PMT for a 3-phase-to-ground fault on the MV side.

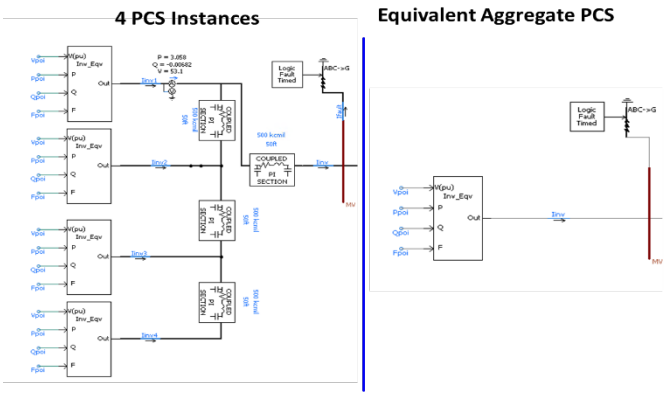

Fig. 8. Simulation setup for 4 PCS instances vs. aggregate model.

C. System Model

Figure 12 shows the PSCAD snapshot of the system model setup. A 230 kV voltage source equivalent is used for the system upstream of POI. The system model consists of two 230 kV transmission line sections, MPT, and two 34.5 kV short MV cable sections, and 68 PCS' equivalent aggregate 233.24 MVA BESS. The accuracy of the PSCAD simulation model was verified using steady-state quantities, such as bus voltages and the collection cable charging MVAR.

D. Study Cases

Table II shows six case studies that are performed for a three-phase-to-ground fault on the 34.5 kV BESS collector system. Case 1 is the base case that considers all PCS of BESS, transmission capacitance, ultimate build-out utility bus 34.3 kA fault level, and neutral tap for MPT. The other cases are for sensitivity analysis to find the dependencies of the short-circuit current on the system operating and modeling conditions. The sequence of events for the simulation are:

- t = 0-1 s: Simulation starts and steady-state operation
- t = 1 s: Three-phase-to-ground fault on 34.5 kV BESS collector system

For this study, the inverter voltage and frequency protection and power plant controller functions (e.g., voltage, reactive power, frequency, power factor control modes) are disabled to ensure worst case results are obtained.

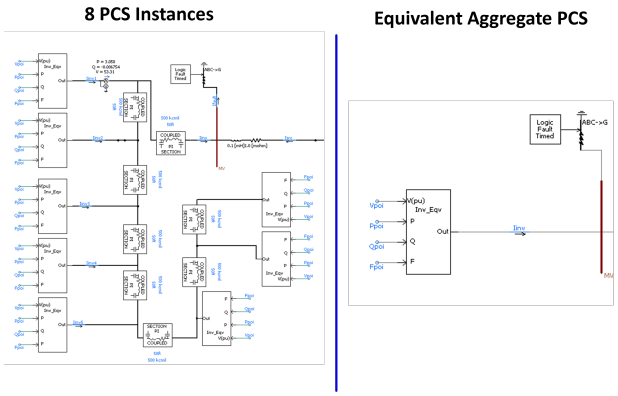

Fig. 9. Simulation setup for 8 PCS instances vs. aggregate model.

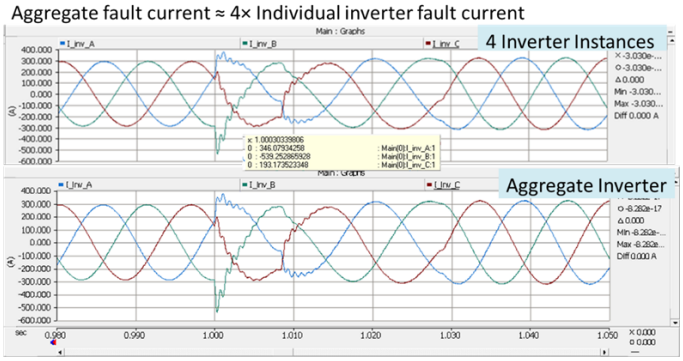

Fig. 10. Fault contributions from 4 PCS instances vs. aggregate model.

E. Results

This section furnishes short circuit contribution results for all cases in Table II.

1) Case 1: Figure 13 shows the total fault current, contributions from the 68 inverters, and contribution from the grid for a three-phase-to-ground fault at BESS collector systems. The following observations can be made from the figure:

- Inverters slightly increase the asymmetrical fault current peak (first peak after the fault at 1 s)—total 51.5 kA, utility contribution 50.6 kA, and inverter contribution 9.1 kA.
- The contributions of the inverters in symmetrical fault current peak (after a few cycles from the fault) are higher— total 33.1 kA, utility contribution 27.7 kA, and inverter contribution 5.5 kA. The inverter contributions are equal to around one p.u. of their ratings.

2) Sensitivity Analysis Results: Table III displays the asymmetrical peak fault current for all the cases. The results indicate that:1) The effect of system capacitance is not significant, 2) MPT tap position does not have a big effect on the results.

VI. Comparison of Phasor and Time-Domain Results

The phasor-domain analysis depicts the highest (63.2 kA) fault current, followed by the simplified (57 kA) and detailed (53 kA) time-domain analyses values.

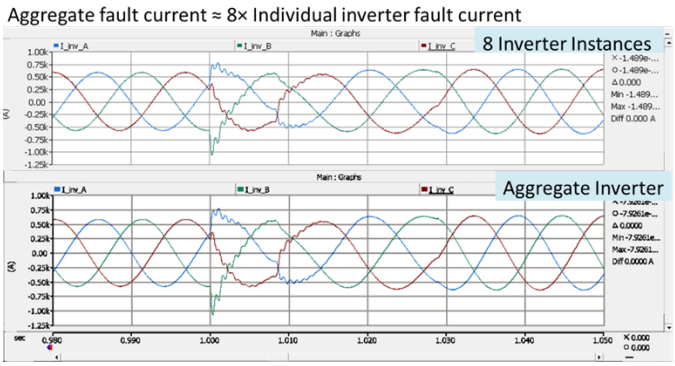

Fig. 11. Fault contributions from 8 PCS instances vs. aggregate model.

TABLE II
Case List for Detailed Time-Domain Simulations

Case	Number of PCS	Transmission Capacitance	Utility Fault kA	MPT Tap
1	68	Yes	34.3	N
2	0	Yes	34.3	N
3	0	No	34.3	N
4	68	Yes	49.9	N
5	68	Yes	34.3	16R
6	68	Yes	34.3	16L

The difference in asymmetrical current is solely due to the inverter contribution which is not mentioned in the standards. It is the authors' experience that the inverters do not contribute any substantial asymmetrical current regardless of their technology. This stems from the fact that the PWM control reacts fast to control the current to protect the inverter components. In this paper, it is clear from the simulations that the high X/R ratio is causing a conservative asymmetrical current. The C37.010-2016 calls for a 20% margin in switchgear sizing. The results of this paper shows that IEEE calculations adds another 10% margin. This 30% margin is making it more expensive to design renewable energy projects.

In the end, a costly decision was made to redesign the project substation to include current limiting reactors to limit the grid short circuit contribution to limit the asymmetrical current. The main reason for that decision was that the study performed in this paper was out of step with the IEEE standards and the project's owner did not want to take risks even if it were based on deep engineering analysis. This shows the need to update the related IEEE standards to include inverter short circuit behavior.

VII. Conclusions

This paper has compared the fault current for a large 204 MW BESS project calculated using three methods: (1) ASPEN phasor-domain simulation, (2) PSCAD simplified time-domain simulations, and (3) PSCAD detailed time-domain simulations. The comparison indicated that phasor-domain short-

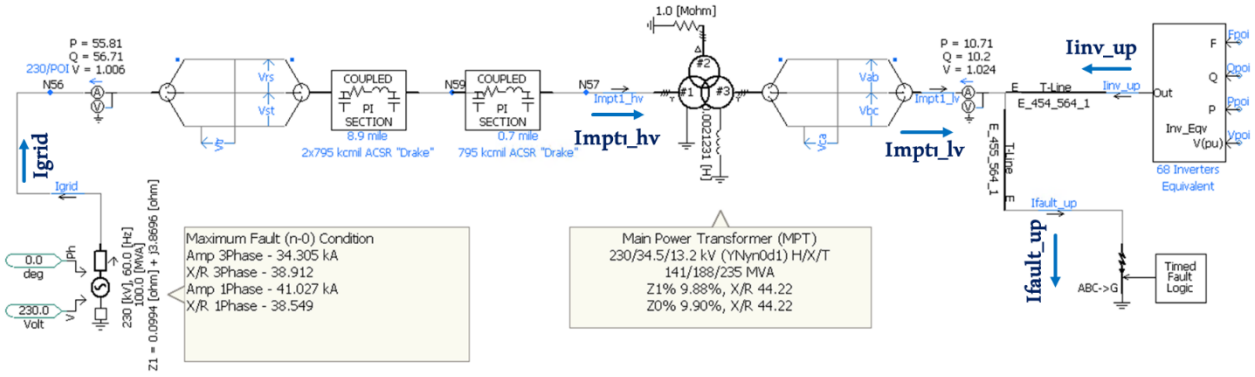

Fig. 12. Snapshot of the detailed PSCAD model setup for the study.

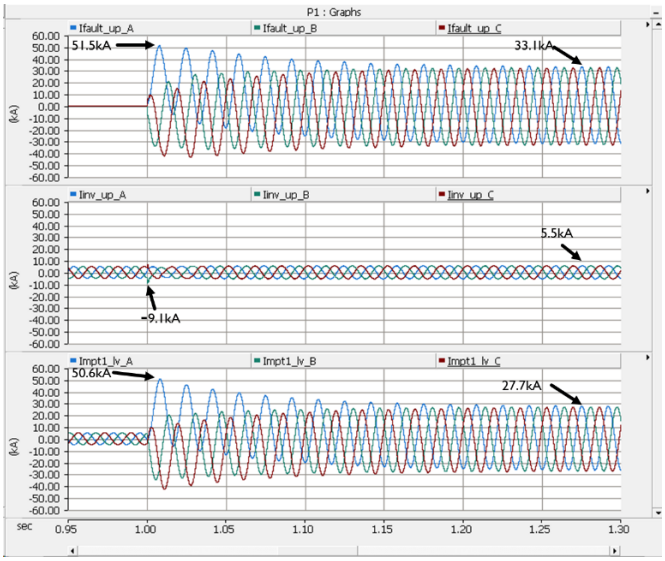

Fig. 13. Case 1 fault currents: Total current (top), inverter contributions (middle), and utility grid contribution (bottom).

TABLE III
ASYMMETRIC PEAK FAULT CURRENT

Case	Case Description	Asymmetrical Peak kA
1	68 PCS; Tie line capacitance; Utility fault level: 34.305 kA; MPT Tap: N	51.5
2	No PCS	51.4
3	No PCS; No transmission line capacitance	51.4
4	Emergency higher fault level (49.9) at the source	53
5	MPT tap at 16R	50.8
6	MPT tap at 16L	49.6

circuit asymmetrical peak levels are conservative as compared to time-domain results.

Furthermore, sensitivity analysis results have shown that PCSs do not increase the asymmetrical peak current significantly. Moreover, the results exhibited that the inverter contributions to symmetrical fault current are equal to around one p.u. of their ratings. Also, for the project under study, the operating conditions of the MPT tap position decreased the asymmetric peak, and modeling of transmission line capacitance did not change the peak current significantly.

The results of this paper shows the need to update the IEEE standards to include the right way of modeling inverter short circuit contribution.

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